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Ultra Low Power Frequency Synthesizer

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Abstract.

A power and jitter FOM state of art integer-N all digital phase locked loop (ADPLL) frequency synthesizer implemented in a commercially available 22nm FD-SOI process is presented in this paper. Achieved was a power consumption of 95 μW with 12 oscillator phases at 816 MHz, a jitter FOM of -225 dB, and an active area of 0.00365 mm^2. This was obtained through an emphasis on power reducing architectural choices for application to low duty cycle wake up receivers (WUR), utilizing low complexity, bias and reference-free circuits. Included is a novel, pseudo-differential voltage controlled ring oscillator using FD-SOI backgates to implement both frequency tuning and differential behavior. This voltage controlled oscillator achieves high frequency tuning gain linearity with rail-to-rail input range, while using no static current biasing. The proposed oscillator enables 2.448 GHz IQ sampling through oversampling at the 1/3 subharmonic (816 MHz). Capacitive DACs are used to provide digital control to the oscillator with minimum power draw. A low complexity band-bang phase detector (BBPD) and an all digital proportional-integral (PI) loop filter with divider-free operation implement the remaining portions of the PLL. Furthermore, a mathematical model regarding the novel oscillator is introduced, a phase noise optimization theory is presented for PI loop-filter design in BBPD-PLLs, and theory regarding DAC resolution determination is also outlined. Finally, a theoretical limit for achievable PLL FOM$_{jitter}$ in the proposed design is established.

Preface.

Simplicity is the ultimate sophistication.

Leonardo da Vinci

I would like to thank my advisors Trond Ytterdal and Carsten Wulff for providing me the opportunities to further my knowledge and experience in the dark arts of circuit design.

I also thank my family for their continual open support of my life endeavors.

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Problem description.

The intent of this project is to develop an ultra low power, integer-N all-digital PLL (ADPLL) frequency synthesizer for application to wake up receiver (WUR) radio circuits. The target technology is a commercially available fully-depleted silicon on insulator (FD-SOI) process with 22nm node size. The implemented PLL is intended for use in duty cycled WUR circuit applications, with on the order of 1% active time. Due to the duty cycled requirement, the design must enable rapid locking times such that fast wake-up from a sleep state can be achieved. The required specifications for this PLL design are given in table 1. Given the radio application of the work, a direct phase noise requirement is not provided, rather, performance is constrained in terms of the modulation scheme and target bit error rate of the radio system. Therefore, the implemented PLL must enable satisfactory operation of this radio system.

Parameter	Specification	Unit
Power	≤ 100	μW
Reference frequency[1]	32	MHz
Synthesized frequency[2]	2.448	GHz
BER[3]	$\leq 10^{-3}$	
Lock time	≤ 5	μs

Table 1: Design required specifications.

This work is in part a continuation of the author's previous work [1] on the optimization and simulation of integer-N ADPLLs, which focused on automation of loop filter design. This previous work has motivated the architectural choices of this work, particularly the usage of a bang-bang phase detector with a proportional-integral (PI) controller based loop filter. This architecture was found to be advantageous in terms of complexity and optimizability, providing for a known good starting point on this project.

[1] Frequencies derived from the reference, for example through division, are also acceptable.
[2] Or equivalent through sampling.
[3] At 250 Kbps with symbols encoded as $\pm 2\pi$ phase shifts.

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Abbreviations.

ADC	Analog to digital converter
ADPLL	All digital phase locked loop
ASM	Algorithmic state machine
BBPD	Bang-bang phase detector
BER	Bit error rate
BOX	Buried-oxide
BW	Bandwidth
CDAC	Capacitive digital to analog converter
CDF	Cumulative distribution function
CM	Common mode
CMOS	Complementary metal oxide semiconductor
CMRR	Common mode rejection ratio
CNR	Carrier to noise ratio
CP	Charge pump
DAC	Digital to analog converter
DC	Direct current
DCO	Digitally controlled oscillator
DFF	D flip-flop
FET	Field effect transistor
FOM	Figure of merit
FSK	Frequency shift keying
GMSK	Gaussian minimum shift keying
HVTPMOS	High voltage threshold PMOS
IIR	Infinite impulse response
IQ	In phase - Quadrature phase
KDCO	DCO Gain
LC	Inductor-capacitor
LF	Loop filter
LO	Local oscillator
LSB	Least significant bit
LVTNMOS	Low voltage threshold NMOS
MMSE	Minimum mean squared error

MOM	Metal-oxide-metal
MOSFET	Metal oxide semiconductor field effect transistor
MSB	Most significant bit
MSE	Mean squared error
NMOS	N-channel metal oxide semiconductor
OTW	Oscillator tuning word
PD	Phase detector
PDF	Probability distribution function
PFD	Phase frequency detector
PI	Proportional-integral
PLL	Phase locked loop
PMOS	P-channel metal oxide semiconductor
PN	Phase noise
PSD	Power spectral density
PSK	Phase shift keying
RC	Resistor-capacitor
RF	Radio frequency
RMS	Root mean squared
RO	Ring oscillator
RST	Reset
RVT	Regular voltage threshold
RVTPMOS	Regular voltage threshold PMOS
SLVTNMOS	Super-low voltage threshold NMOS
SOI	Silicon on insulator
SSB	Single side band
TDC	Time to digital converter
TSPC	True single phase circuit
VCO	Voltage controlled oscillator
WUC	Wake up call
WUR	Wake up receiver

1 Introduction

Phase locked loops (PLLs) are the fundamental building block to virtually all wired and wireless communication systems of today. To meet industrial demands of continual and uncompromising advancement of communication system performance, e.g. higher data rates, lower power, it is paramount that PLL performance is continually improved. Of perpetually growing importance is the application of PLLs to radios in battery powered mobile and internet of things (IoT) devices, for which reduction of power is highly sought after. A recent approach to reducing power consumption in such wireless applications is through usage of wake up receivers (WURs). These are ultra low power, low data rate radio receivers that listen for requests (i.e. "wake up calls", or WUCs) for activity from some external source. Upon a WUC, the device powers on and activates a higher powered radio supporting faster data rates for only the time required. In devices that are inactive for substantial periods of time, waiting for requests for activity (e.g. as with sensor networks or wireless headphones), such a scheme can enable great power reduction, for example achieving 4.5 nW in [2] and 365 nW in [3] for 2.4 GHz band WUC reception. When this is compared to utilizing a full data rate receiver to poll the radio spectrum for activity requests, which for a state of art Bluetooth design may draw on the order of 1.9 mW [4], it is seen that upwards of 10^6 improvement in power is obtainable, undoubtedly reducing the overall achievable system power consumption for many wireless applications.

Thus, in this work, the design of a low power PLL which enables WUR applications is considered. Ultra low power consumption has been achieved with PLL-less on-off keying receivers, for example accomplishing 4.5 nW with 0.3 kbps of data at 2.4 GHz in [2]. However, this work will be catered to PLL-based designs that maintain backwards-compatibility with FSK and PSK modulation schemes supported by existing wireless standards such as 802.15.4, WiFi and Bluetooth. A review of current literature shows that the state of art within ultra low power PLLs in the 2.4 GHz band regime achieve power consumption on the order of hundreds of μW, for example 170 μW in [5], and 265 μW in [6]. Therefore, to advance the boundary of the current state of art, this work seeks to set a new record for PLL power consumption, namely $\leq$ 100 μW for use in 2.4 GHz band radio operation. Furthermore, an attempt will be made to minimize implemented area of the PLL. Current state of art for PLL area rests in the sub-0.01 mm^2 regime, with as small as 0.0036 mm^2 being seen in 5nm process technology [7]. It will be attempted to obtain a similar area to the current state of art.

A brief outline of the paper is as follows. An introduction to PLL and FD-SOI theory is in section 3. The undertaken PLL design is discussed in sections 4-8. Simulation results of the implemented design are in section 9. Comparison to the state of art and general discussion regarding this work are in section 10. Finally, section 11 concludes.

1.1 Main Contributions

(1) Implementation of a sub-100 μW ultra-low power, 0.00365 mm^2 area CMOS PLL in a 22nm FD-SOI process technology, with state of art FOM$_{jitter}$ within its power regime, and comparable area to the current state of art.

(2) Presentation of a novel pseudodifferential ring oscillator circuit topology and theory of operation, utilizing FD-SOI backgates to implement both frequency tuning and differential operation.

(3) Realization of a highly linear voltage controlled oscillator with rail-to-rail input range.

(4) Loop filter optimization theory for proportional-integral controller bang-bang phase detector PLLs with noisy phase detectors.

(5) Theoretical figure for the FOM$_{jitter}$ performance limit of proportional-integral controller bang-bang phase detector PLLs.

(6) DAC resolution and oscillator frequency gain optimization theory.

(7) A novel pseudodifferential buffer presenting common mode rejection characteristics.

(8) Implementation of low power CDACs.

(9) Implementation of a low power bang-bang phase detector.

(10) Implementation of a low power digital loop filter.

(11) Demonstration of bias current and reference free PLL design.

2 Redefining Requirements

With the purpose of this work to be applied to a radio system, the high level requirements of the PLL are constrained by the performance requirements of end use radio system. The target for this work is to enable a bit error rate of $\leq 10^{-3}$ using a slightly modified Gaussian minimum shift keying (GMSK) [8] modulation scheme. The transmitted signal is to have a nominal 1 Mbps data rate and a bandwidth-time (BT) product of 0.5, where 1 and 0 respectively are encoded as $\pm\pi/2$ phase shift per symbol in the signal. The receiver, however, is to be operated at lower symbol rate of 250 kbps. To match data rates, the transmitter therefore must transmit four identical symbols at 1 Mbps to encode one symbol as seen by the receiver. The result of such a scheme is that one received symbol will be constituted by a phase shift of $\pm 2\pi$, or a full rotation of the signal constellation, which increases the detectability of the received signal. To determine PLL requirements for this scheme, a simulation of bit error rate versus carrier-to-noise ratio (CNR) of the modulated signal has been performed, with the results in figure 1. It is found that for a BER of 10^{-3}, a minimum of 6.4 dB of CNR is required for the radio system. In the case of this work, where the PLL is constrained to ultra low power, it is now assumed that the PLL will be the limiting factor in terms of noise in the implemented radio system. Therefore, the CNR of the oscillator, that is the ratio of the main tone power to phase noise power, must be at least the determined value of 6.4 dB. To provide a slight margin due to the inevitable presence of other noise sources in the radio system, a specification for CNR ≥ 10 dB for the PLL has been selected. It is more typical to define PLL performance in terms of root mean square (RMS) jitter, accordingly table 2 contains the final translated requirements of the PLL to meet the intended radio system performance targets. Another relevant requirement for the PLL is it must enable IQ sampling of RF signals at 2.448 GHz.

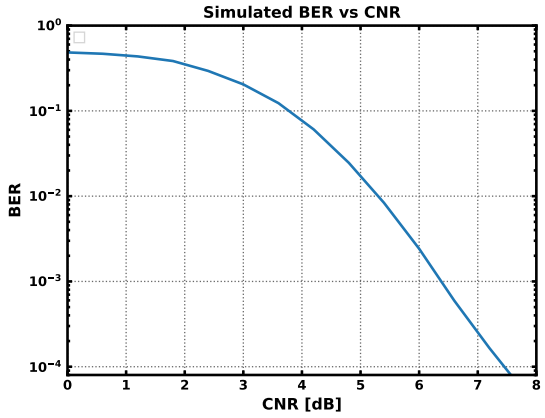


Figure 1: Bit error rate versus carrier to noise ratio of targeted radio system modulation scheme.

Parameter	Value	Units
CNR (at 2.448 GHz)	≥ 10	dB
RMS Jitter	≤ 20.56	ps
Frequency	2.448	GHz
Power	≤ 100	μW

Table 2: Radio system derived PLL performance specifications.

3 Theory

3.1 Fully Depleted Silicon on Insulator (FD-SOI) Process

FD-SOI is a process technology that implements complementary metal oxide semiconductor (CMOS) transistors with an insulating layer of oxide, referred to as a buried oxide (BOX), between the channel of the transistors and the silicon substrate [9]. The addition of such an oxide reduces capacitances of the fabricated transistors to the silicon substrate, resulting in lower overall device capacitance than in bulk CMOS technologies. Thus higher frequency of operation is possible versus similar sized bulk process nodes. A further feature introduced by FD-SOI technology is the ability to form isolated wells beneath fabricated devices [10], which remain electrically isolated from the transistors via the BOX and from the substrate due to PN junctions inherent in well formation. This opens the possibility to achieve biasing across a wide voltage range in the regions below individual transistors (both for PMOS and NMOS devices), which enables a substantial degree of in-situ tuning of individual transistor threshold voltages by exploitation of the body effect of MOS transistors. The well beneath a FD-SOI transistor is referred to in this work as the "backgate". The implementation of these features in a typical FD-SOI process is shown in figure 2.

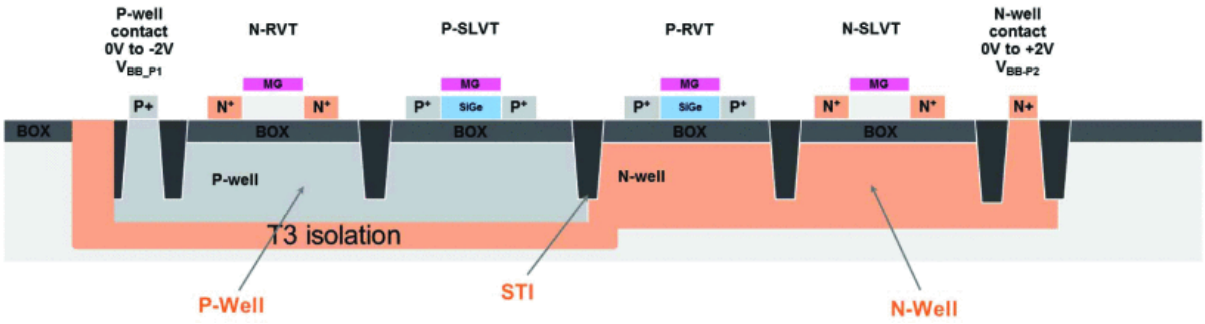


Figure 2: FD-SOI cross-sectional construction of active devices [10], showing BOX separation of well/-substrate and devices.

3.2 MOSFET Models

3.2.1 I-V Relations

Basic models that describe the large signal current-voltage relations of a Metal Oxide Semiconductor Field Effect Transistor (MOSFET) are introduced here, based wholly from [11]. For the purposes of this work, a MOSFET is schematically represented in the manner of figure 3, with gate (G), drain (D), source (S) and backgate (B) terminals. Several operating regimes occur depending on the relation of the terminal voltages. Relevant to the scope of this work,

are the linear, saturated and velocity saturated regions of MOSFET operation. Nominally, it is expected that when configured as in figure 4, sweeping the gate-source voltage (V_{GS}), with the drain-source voltage (V_{DS}) set greater than zero in the case of a NMOS device, that an increasing amount of current will enter the MOSFET drain after crossing a threshold voltage (V_{TH}). V_{TH} is predominantly dependent on physical configuration of a FET (dimensions, doping, material), however, it is also impacted by the backgate bias in what is termed "the body effect". A more detailed description of each operating regime will be given in the following discourse.

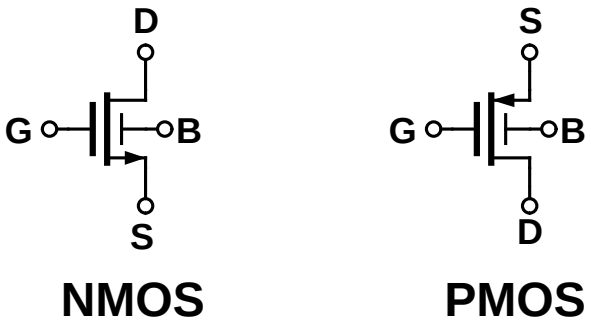


Figure 3: MOSFET symbols.

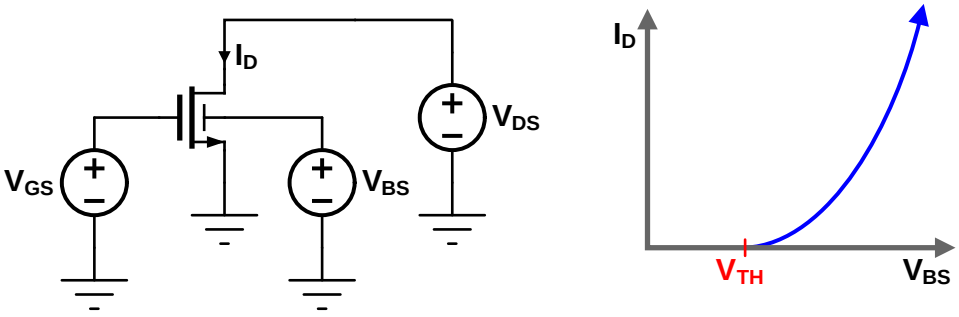


Figure 4: Drain current versus gate-source bias.

Linear Region Linear MOSFET operation occurs under the circumstances where $|V_{GS} - V_{TH}| > |V_{DS}|$. The following equation is the I-V relation in this regime, where μ_n represents the electron mobility of the semiconductor in use (within the FET channel), C_{ox} represents the areal oxide capacitance.

$$I_D = \mu_x C_{ox} \left(\frac{W}{L}\right) \left[(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2\right] \tag{1}$$

Saturation Region Saturation region occurs when $|V_{DS}| > |V_{GS} - V_{TH}|$. Notably, dependence of drain current on V_{DS} is reduced, and in the case of the ideal models considered here, the effect of V_{DS} on drain current is completely negated.

$$I_D = \frac{1}{2}\mu_n C_{ox} \left(\frac{W}{L}\right) (V_{GS} - V_{TH})^2 \tag{2}$$

Velocity-saturation Region In the scenario of high applied fields which arise in a short MOS-

FET channels, carrier velocity can saturate to a limited velocity, v_{sat}. The point at which this effect takes place is device dependent. For approximate consideration it can be understood to occur when $|V_{DS}/L > E_{crit}|$, where E_{crit} is the electric field which the carrier velocity-electric field relation ($v = \mu E$) of the channel semiconductor becomes sub-linear. Below is the MOSFET model under such circumstances.

$$I_D = WC_{ox}(V_{GS} - V_{TH})v_{sat} \tag{3}$$

3.2.2 FD-SOI Body Effect

Application of a bias to the substrate below a bulk MOSFET, or to the well below a FD-SOI MOSFET, has a direct effect on the threshold voltage of that device. For a bulk MOSFET, change of body bias affects the width of source-body and drain-body depletions, which consequently can increase or decrease the magnitude of the channel depletion charge as seen by the gate terminal needed to achieve channel inversion. This corresponds to a differential in the threshold voltage. In the case of FD-SOI transistors, the nature of the body effect is modified due to the presence of the BOX. Thus, an approximate derivation for body effect will be provided here. In FD-SOI, the active channel region is thin, and under strong inversion, the entire channel region is depleted of charge. Supposing a channel height Z and channel doping concentration N_A, the total charge per unit area to deplete the channel for inversion to occur is $Q_d = qN_AZ$. With oxide capacitance per unit area $C_{ox,fg}$ associated with the front gate, the portion of the threshold voltage associated with total depletion of the channel is, from the front gate perspective:

$$V_{d,fg} = \frac{Q_d}{C_{ox,fg}} = \frac{qN_AZ}{C_{ox,fg}} \tag{4}$$

Supposing that the back gate has capacitance of $C_{ox,bg}$, with bias applied V_{BS}, the back gate can be seen to "rob" the front gate of a charge $Q_{bg} = C_{ox,bg}V_{BS}$ when in inversion. Thus results in a partial change of the front gate-referred voltage required to obtain channel depletion:

$$V'_{d,fg} = \frac{Q_d - Q_{bg}}{C_{ox,fg}} = \frac{Q_d}{C_{ox,fg}} - \frac{C_{ox,bg}}{C_{ox,fg}}V_{BS} = V_{d,fg} - \Delta V_{th,bg} \tag{5}$$

It is noted that this can be written as the nominal value of $V_{d,fg}$ minus a differential. This differential is the resulting change in threshold voltage due to back gate bias, $\Delta V_{th,bg}$:

$$\Delta V_{th,bg} = \frac{C_{ox,bg}}{C_{ox,fg}}V_{BS} \tag{6}$$

This is linear with applied back gate bias, and the strength of the coupling is tunable by the ratio of front gate and back gate capacitances. Typically this ratio is $<< 1$. In this work, the body

effect coefficient is defined as γ, given in equation 7.

$$\gamma = \frac{C_{ox,bg}}{C_{ox,fg}} \tag{7}$$

Given a nominal threshold voltage of V_{TH0} with no backgate bias, the threshold voltage including the body effect in FD-SOI technology can be modeled as such:

$$V_{TH} = V_{TH0} - \gamma V_{BS} \tag{8}$$

3.2.3 Linearization of MOSFET Models

Under conditions where a MOSFET is held at near constant bias levels, with only minor variations around the DC operating level, simpler linearized models of the transistors can be developed. For the different operating regions of the MOSFET, the I-V relations can be generalized in terms of the function $I_D(V_{GS}, V_{DS}, V_{BS})$. Linearization is then obtained by calculating the slope of I_D with respect to the potentials V_{GS}, V_{DS}, V_{BS}. The resulting parameters (given as equations 9 to 11) are the transconductance g_m, relating gate drive to drain current, transconductance g_{mb}, relating body drive to drain current, and resistance r_o, relating drain voltage to drain current. Due to linearization, the current contributions are superimposed to determine total drain current. The linearized circuit which replaces the four terminal MOSFET symbols of figure 3 is given by the linearized circuit of figure 6.

$$g_m = \frac{\partial}{\partial V_{GS}} I_D(V_{GS}, V_{DS}, V_{BS}) \tag{9}$$

$$g_{mb} = \frac{\partial}{\partial V_{BS}} I_D(V_{GS}, V_{DS}, V_{BS}) \tag{10}$$

$$r_o = \left(\frac{\partial}{\partial V_{DS}} I_D(V_{GS}, V_{DS}, V_{BS}) \right)^{-1} \tag{11}$$

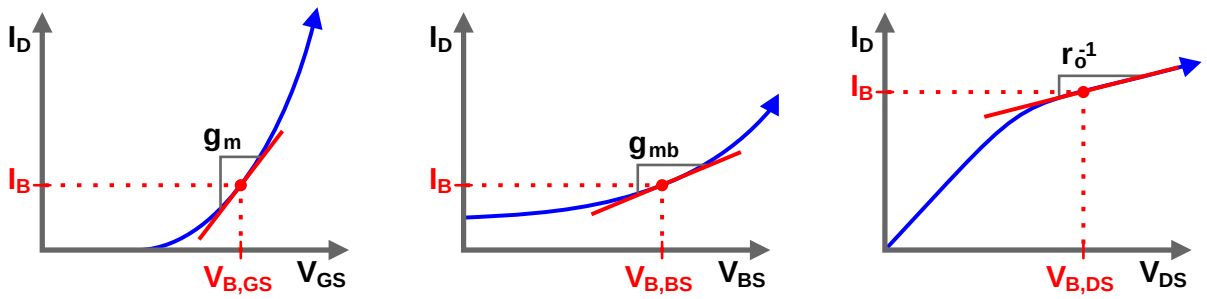


Figure 5: Transconductances as slope localized at operating point of I-V curve.

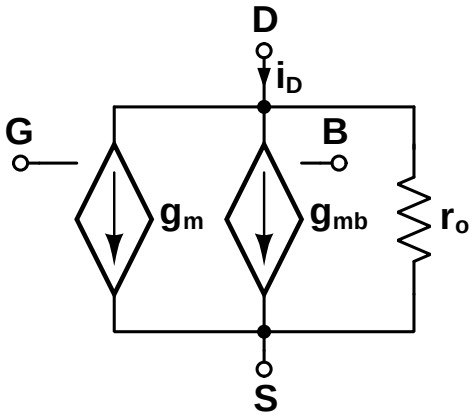


Figure 6: Linearized (small-signal) MOSFET model.

A useful relation based on this linearization can be determined, based on the FD-SOI body effect equation 8, and the I-V relations for the three MOSFET operation regions discussed in section 3.2.1. Computation of g_m and g_{mb} for all three regions with the FD-SOI body effect yields the same result given in equation 12. This is that g_{mb} and g_m are related by the body effect coefficient γ.

$$g_{mb} = \gamma g_m \tag{12}$$

3.3 Basic PLL

A phase locked loop (PLL) is a feedback system whose output tracks or maintains a fixed phase relationship to an input signal. PLLs are well suited for frequency synthesis, which is the process of generating derivative frequencies from some reference frequency. Given a reference signal with phase trajectory Φ_{ref} and output signal with phase Φ_{out}, a PLL can be modeled as in figure 7 using an elementary feedback system, with feedforward and feedback networks A(s) and B(s).

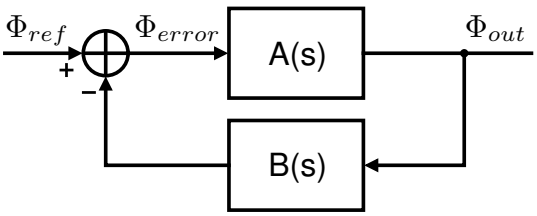


Figure 7: Phase locked loop as elementary feedback system.

The closed loop phase response for Φ_{ref} to Φ_{out} is therefore:

$$\frac{\Phi_{out}(s)}{\Phi_{ref}(s)} = \frac{A(s)}{1 + A(s)B(s)} \tag{13}$$

A case of interest is when B(s) = 1/N, where N is a constant, and the loop gain L(s) = A(s)B(s) $>>$ 1. The closed loop response for this case is:

$$\frac{\Phi_{out}(s)}{\Phi_{ref}(s)} \approx \frac{A(s)}{A(s)B(s)} = \frac{1}{B(s)} = N \tag{14}$$

We see that the phase through the PLL is multiplied by a factor of N. If the input phase signal is sinusoidal with frequency ω_{ref}, and likewise the output with ω_{out}, then $\phi_{ref}(t) = \omega_{ref}t$ and $\phi_{out}(t) = \omega_{out}t$. Accordingly:

$$\frac{\Phi_{out}(t)}{\Phi_{ref}(t)} = \frac{\omega_{out}t}{\omega_{ref}t} \approx N \quad \rightarrow \quad \omega_{out} \approx N\omega_{ref} \tag{15}$$

Therefore, it is observed that a PLL allows for the generation of a new frequency from a reference frequency signal, which is termed as "frequency synthesis". With a feedback division ratio of 1/N, the PLL multiplies the reference frequency by a factor of N. Hereon, the B(s) portion of a PLL feedback network is referred to as a divider, with associated division ratio N.

3.4 PLL Frequency Synthesizer Architecture

A typical architecture for implementing a physically realizable PLL frequency synthesizer [12] is shown in figure 8. This PLL is comprised of four components: (1) a phase detector, herein PD, (2) a loop filter, herein $H_{LF}(s)$, (3) a voltage controlled oscillator, herein VCO, and (4) a divider, indicated as "÷ N" in figure 8. In control systems parlance, the loop filter corresponds to a controller, the VCO an actuator, and the divider as feedback.

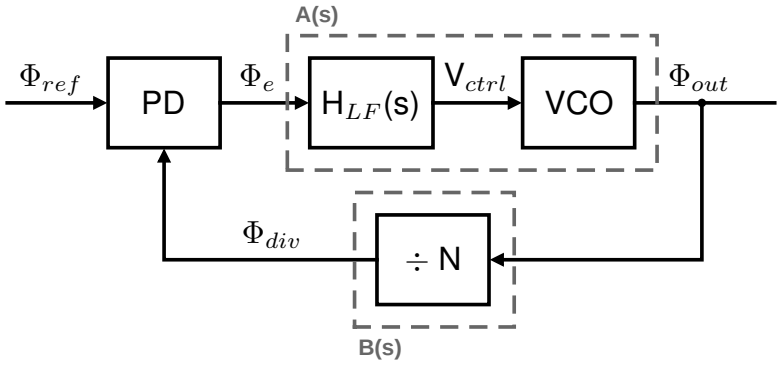


Figure 8: High-level PLL Synthesizer Architecture.

Further explanation of these components will be hereafter made.

3.4.1 Phase Detector

A phase detector acts as the summation point of figure 7, which measures the phase error Φ_e between the reference signal and the output of the PLL. The phase error is then used by the controller, which is implemented as the loop filter, to adjust the PLL's state. Such a phase detector may also have intrinsic gain, given by K_{PD}. Mathematically a phase detector is modeled as in equation 16.

$$\Phi_e(s) = K_{PD}(\Phi_{ref}(s) - \Phi_{div}(s)) \tag{16}$$

3.4.2 Bang-bang Phase Detector

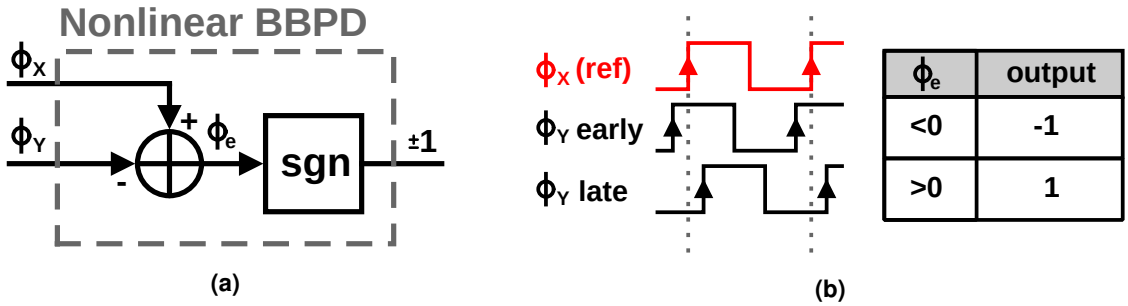


Figure 9: (a) BBPD schematic, **(b)** BBPD timing.

A simple implementation of a phase detector is a bang-bang phase detector (BBPD) [13]. As exhibited in figure 9, a BBPD outputs a value of 1 if the input Φ_Y is late relative to the reference Φ_X (representing a clock signal), and -1 if it is early. A BBPD shows abrupt nonlinearity in its transfer characteristics. If the error signal variance $\sigma^2_{\Phi_e}$ is constant, which is expected in steady-state PLL operation, a linearized model for phase detector gain can be established [14], given in equation 17.

A linearized version of the BBPD is illustrated in figure 10. The output z valued as ± 1 (its variance σ_z^2=1).

$$K_{BBPD} = \frac{\mathbb{E}[\Phi_e(t) \cdot \mathrm{z}(t)]}{\mathbb{E}[\Phi_e^2(t)]} = \sqrt{\frac{2}{\pi}} \frac{1}{\sigma_{\Phi_e}} \tag{17}$$

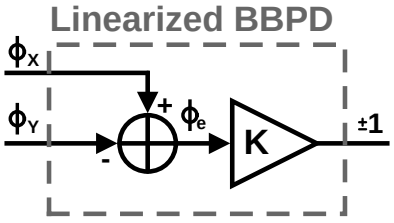


Figure 10: Linearized bang-bang phase detector.

BBPD Noise

Given the output of the BBPD is of fixed power σ_z^2 = 1, a linearized gain of K_{BBPD}, a phase error power of $\mathrm{Var}[\Phi_e(t)] = \sigma_{\Phi_e}^2$, and $\mathbb{E}[\Phi_e(t)] = 0$, the noise power $\sigma_{n_{BBPD}}^2$ out of the BBPD is in equation 18. $K_{BBPD}^2\sigma_{\Phi_e}^2$ represents the power of the phase error signal component post-detector, and it is assumed that noise power and signal power are uncorrelated.

$$\sigma_{n_{BBPD}}^2 = \sigma_z^2 - K_{BBPD}^2\sigma_{\Phi_e}^2 = 1 - \frac{2}{\pi} \tag{18}$$

Observe that the BBPD noise power is constant valued. If the reference signal is a clock signal with frequency f_{ref}, the BBPD noise spectral density is in equation 19.

$$S_{n_{BBPD}(f)} = \frac{\sigma_{n_{BBPD}}^2}{\Delta f} = \frac{\left(1 - \frac{2}{\pi}\right)}{f_{ref}} \tag{19}$$

3.4.3 Divider

A divider is used as the feedback path in the PLL, where the division ratio N controls the frequency multiplication of a PLL synthesizer. The transfer function of the divider is:

$$\mathrm{H}_{div}(s) = \frac{\Phi_{div}(s)}{\Phi_{out}(s)} = \frac{1}{\mathrm{N}} \tag{20}$$

3.4.4 Loop Filter

A loop filter behaves as the controller of a PLL, namely controlling the phase-frequency response of PLL. The choice of the loop filter transfer function significantly affects transient PLL behavior, as well as phase noise performance, as is later described. Here, a pole-zero based controller is defined for use in this work. This is designed to have P poles and Z zeros, and can be represented in the general form of equation 21 as a rational function of polynomials of s with filter coefficients given as $\{a_0, ..., a_P\}$ and $\{b_0, ..., b_Z\}$.

$$\mathrm{H}_{LF}(s) = \frac{\sum_{j=0}^{Z} b_j s^j}{\sum_{k=0}^{P} a_k s^k} \tag{21}$$

3.4.5 Loop Filter Discretization and Digitization

In PLLs which sample on a fixed interval defined by a reference clock frequency f_{ref}, derivation of a discrete time controller model is necessary. This is derived from the general form continuous loop filter (equation 21) via application of a continuous s-domain to discrete z-domain

transformation. Strictly speaking, $z^{-1} = e^{-s\Delta T_s}$ for values on the unit circle, i.e. r = 1 [15]. If the PLL sampling rate $f_s = f_{ref}$ is constrained to be sufficiently higher than the implemented filter bandwidth (i.e. PLL loop bandwidth, BW_{loop}), a simpler transformation using a truncated Taylor series approximation is applicable. Given the $1/\Delta T_s = f_s$ as the relation for sampling rate, then:

$$\begin{aligned} z^{-1} &= e^{-s\Delta T_s} && \text{(definition of z on unit circle)} \\ &= \sum_{k=0}^{\infty} \frac{(-s\Delta T_s)^k}{k!} && \text{(exponential Taylor series)} \\ &\approx 1 - s\Delta T_s && (\text{if } |s\Delta T_s| = 2\pi \mathrm{BW}_{loop} \cdot \Delta T_s << 1) \end{aligned}$$

Thus the s-to-z and z-to-s identities for the approximate transform are:

$$z^{-1} = 1 - s\Delta T_s \tag{22}$$

$$s = \frac{1}{\Delta T_s}(1 - z^{-1}) \tag{23}$$

Applying equation 23 to the general loop filter of equation 21 yields the z-domain loop filter:

$$\mathrm{H}_{LF}(z) = \mathrm{H}_{LF}(s)|_{s=\frac{1}{\Delta T_s}(1-z^{-1})} = \left.\frac{\sum_{j=0}^{Z} b_j s^j}{\sum_{k=0}^{P} a_k s^k}\right|_{s=\frac{1}{\Delta T_s}(1-z^{-1})} \tag{24}$$

$$= \frac{\sum_{j=0}^{Z} \frac{b_j}{\Delta T_s^j}(1 - z^{-1})^j}{\sum_{k=0}^{P} \frac{a_k}{\Delta T_k}(1 - z^{-1})^k} \tag{25}$$

Equation 25 is translated into a digitally realizable form by reorganizing into the general representation of equation 26. The coefficients of equation 26 determine the final filter coefficients for the sampled-time difference equation in equation 27.

$$\mathrm{H}_{LF}(z) = \frac{\sum_{j=0}^{P} b_j' z^{-j}}{1 + \sum_{k=1}^{Z} a_k' z^{-k}} \tag{26}$$

$$y[n] = -\sum_{k=1}^{P} a_k' y[n-k] + \sum_{j=0}^{Z} b_j' x[n-j] \tag{27}$$

The obtained difference equation is directly implementable in digital hardware with a direct form-I IIR filter [16] shown in figure 11. Such a design is a candidate for automatic synthesis of digital logic. The filter coefficients $\{a_1', ..., a_P'\}$ and $\{b_0', ..., b_Z'\}$ must be quantized into finite resolution fixed point words for a complete digital implementation. The delay elements (z^{-1} blocks) are implementable digitally as registers, the filter coefficient gains are implementable with array multipliers, and the adders are implementable with digital adders.

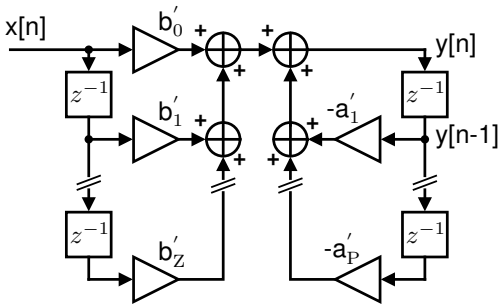


Figure 11: Direct form I implementation of IIR filter.

3.4.6 Voltage/Digitally Controlled Oscillator

A controlled oscillator is an oscillator with frequency controlled by an input signal. When this input signal takes the form of an analog voltage V_{ctrl}, it is referred to as a voltage controlled oscillator (VCO). Otherwise, when controlled digitally with an oscillator tuning word (OTW) u[n], it is referred to as a digitally controlled oscillator (DCO). Nominally, a controlled oscillator is characterized by its gain, in the case of a VCO is $K_{VCO} = \partial f / \partial \mathrm{V}_{ctrl}$. With a DCO, the gain is $K_{DCO} = \Delta f / LSB$, that is the change in frequency per least significant bit of the control word. Analyzed in terms of phase (for the VCO case), an oscillator can be seen as a time-phase integrator, provided a nominal oscillator frequency of f_0:

$$\Phi_{VCO}(t) = \Phi_{out}(t) = \int 2\pi(K_{VCO}\mathrm{V}_{ctrl}(t) + f_0)\mathrm{dt} \tag{28}$$

In the s-domain, the transfer function for a VCO is in equation 29 and equation 30 for a DCO.

$$\mathrm{H}_{VCO}(s) = \frac{\Phi_{VCO}(s)}{\mathrm{V}_{ctrl}(s)} = \frac{2\pi K_{VCO}}{s} \tag{29}$$

$$\mathrm{H}_{DCO}(s) = \frac{\Phi_{VCO}(s)}{\mathrm{u}(s)} = \frac{2\pi K_{DCO}}{s} \tag{30}$$

3.4.7 Closed Loop PLL Transfer Function

With a PLL described at the component level, the closed loop dynamics of the PLL can be computed. A PLL loop gain L(s) can be first determined as in equation 31.

$$\mathrm{L}(s) = K_{PD}\mathrm{H}_{LF}(s)\mathrm{H}_{DCO}(s)\mathrm{H}_{div}(s) = \frac{2\pi K_{PD}K_{DCO}}{\mathrm{N}}\frac{1}{s}\frac{\sum_{j=0}^{Z} b_j s^j}{\sum_{k=0}^{P} a_k s^k} \tag{31}$$

Closing the loop with the phase detector as the feedback summation point, the response of the PLL from reference to output is in equation 32.

$$\mathrm{T}(s) = \frac{\Phi_{out}(s)}{\Phi_{ref}(s)} = \frac{2\pi K_{PD} K_{DCO} \sum_{j=0}^{Z} b_j s^j}{\sum_{k=0}^{P} a_k s^{k+1} + \frac{2\pi K_{PD} K_{DCO}}{\mathrm{N}} \sum_{j=0}^{Z} b_j s^j} = \mathrm{N} \frac{\mathrm{L}(s)}{1 + \mathrm{L}(s)} \tag{32}$$

3.5 Phase noise

Phase noise can be described as undesired variation in an oscillator's phase trajectory from ideal. If an oscillator's frequency is ω_{osc}, then with additive phase noise, the phase of an oscillator is given in equation 33.

$$\Phi_{osc}(t) = \omega_{osc} t + \Phi_n(t) \tag{33}$$

This is composed of a linear phase component $\omega_{osc} t$ and a noise component $\Phi_n(t)$. In the frequency domain, the effect of phase noise is that it broadens the tone of the oscillator, as shown in figure 12. Phase noise can be viewed as instability in terms of oscillator frequency.

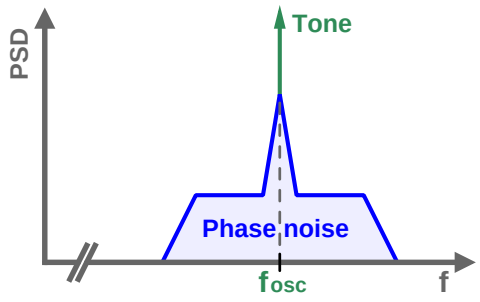


Figure 12: Effect of phase noise on frequency tone.

3.5.1 Phase Noise Relation to Oscillator Power Spectral Density

An oscillator's voltage waveform can be described in terms of a phase trajectory function $\Phi_{osc}(t)$ and amplitude A_0 in the following manner (ignoring higher harmonics):

$$V_{osc}(t) = \Re\left\{A_0 e^{j\Phi_{osc}(t)}\right\} \tag{34}$$

In an oscillator, it is desirable for phase noise to be small, and zero mean ($\mathbb{E}[\Phi_n(t)] = 0$). Using a constraint $\mathrm{Var}[\Phi_n(t)] << 1$, the following approximations can be applied to determine the

oscillator's spectral density in terms of the phase noise component $\Phi_n(t)$.

$$V_{osc}(t) = \Re\left\{A_0 e^{j\omega_{osc}t} e^{j\Phi_n(t)}\right\} \quad \text{(oscillator waveform)} \tag{35}$$

$$= \Re\left\{A_0 e^{j\omega_{osc}t} \sum_{k=0}^{\infty} \frac{(j\Phi_n(t))^k}{k!}\right\} \quad \text{(apply exponential Taylor series)} \tag{36}$$

$$\approx \Re\left\{A_0 e^{j\omega_{osc}t} + j\Phi_n(t) A_0 e^{j\omega_{osc}t}\right\} \quad \text{(truncate series at k=1 given } \mathrm{Var}[\Phi_n(t)] << 1) \tag{37}$$

$$= A_0 \cos(\omega_{osc}t) - \Phi_n(t) A_0 \sin(\omega_{osc}t) \quad \text{(taking the real component)} \tag{38}$$

The result is a carrier cosine signal, and an orthogonal sine signal modulated by the phase noise Φ_n. From this, the spectral density of the phase noise relative to the carrier can be estimated. The power spectral density $S_{V_{osc}}$ is computed in equations 39-41. Due to orthogonality of the sine/cosine components of equation 38, the cross terms that appear in the PSD computation are zero.

$$S_{V_{out}}(f) = \lim_{\Delta T \to \infty} \frac{1}{\Delta T} |\mathcal{F}\{V_{out}(t) \cdot \mathrm{rect}(t/\Delta T)\}|^2 \tag{39}$$

$$= \lim_{\Delta T \to \infty} \frac{A_0^2}{\Delta T} |\mathcal{F}\{\cos(\omega_{osc}t) \cdot \mathrm{rect}(t/\Delta T)\}|^2 \tag{40}$$

$$+ \lim_{\Delta T \to \infty} \frac{A_0^2}{\Delta T} |\mathcal{F}\{\Phi_n(t) \cdot \mathrm{rect}(t/\Delta T)\} * \mathcal{F}\{\sin(\omega_{osc}t) \cdot \mathrm{rect}(t/\Delta T)\}|^2 \tag{41}$$

The noise power spectral density function of the output waveform $\mathcal{L}(\Delta f)$ is defined as the noise PSD at offset Δf from the carrier frequency f_{osc}, normalized to the carrier power. Here the PSD of the carrier component is given by equation 40, and the noise component by equation 41. Shifting equation 41 by $-\omega_{osc}$ and performing normalization for carrier power results in:

$$\mathcal{L}(\Delta f) = \lim_{\Delta T \to \infty} \frac{1}{\Delta T} |\mathcal{F}\{\Phi_n(t) \cdot \mathrm{rect}(t/\Delta T)\}|^2 \Big|_{f=\Delta f} = S_{\Phi_n}(\Delta f) \tag{42}$$

Thus, the noise PSD $\mathcal{L}(\Delta f)$ of the PLL output waveform relative to the carrier is equal to the PSD of the phase noise signal $\Phi_n(t)$, provided $\mathrm{Var}[\Phi_n(t)] << 1$. The PSD of $\Phi_n(t)$ is notated as $S_{\Phi_n}(\Delta f)$.

3.5.2 Leeson's Model

Oscillator noise from thermal and stochastic sources is typical represented mathematically using Leeson's model for oscillator phase noise [17]. Leeson's model considers noise power density at an offset Δf from the oscillator tone (carrier). Noise power density is represented with the function $\mathcal{L}(\Delta f)$, which is the noise power density normalized to the power of the oscillator carrier tone, in other words in units of dBc/Hz. Leeson's model divides phase noise into three regions, illustrated in figure 13: (1) flicker-noise dominated, with a slope of -30 dB/decade,

(2) white frequency-noise dominated, with -20 dB per decade, and (3) a flat region, limited by the thermal noise floor or amplitude noise. It is noted that phase noise components are at frequencies different than the carrier, hence are orthogonal, and can be treated as independent components that are added to the main oscillator tone signal for analysis.

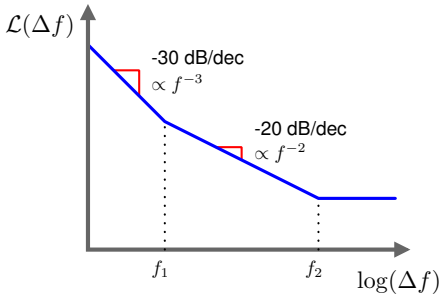


Figure 13: Phase noise regions of Leeson's model.

The equation for $\mathcal{L}(\Delta f)$ [18] is in equation 43, and is dependent on temperature T, excess noise factor F, DC oscillator power P_{DC}, oscillator Q factor, and the transition frequencies f_1 and f_2 that separate the different noise regions. It is of interest to note that the phase noise relative to the carrier will increase as power decreases, which provides challenge for creating low power oscillators with acceptable phase noise characteristics.

$$\mathcal{L}(\Delta f) = 10\log_{10}\left[\frac{2\mathrm{F}k_B\mathrm{T}}{P_{DC}}\left(1+\left(\frac{f_2}{2Q\Delta f}\right)^2\right)\left(1+\frac{f_1}{|\Delta f|}\right)\right] = S_{\Phi n_{DCO}}(\Delta f) \tag{43}$$

For notational consistency, the following redefinition is used in the remainder of this paper: $S_{\Phi n_{DCO}}(f) = \mathcal{L}(\Delta f)|_{\Delta f = f}$

3.5.3 Phase Noise Figures of Merit

A common method to assign a figure of merit (FOM) to oscillator phase noise performance is to utilize the below relation [19]. Such a model assumes linear tradeoffs between power, frequency, and phase noise, and assumes that the rolloff of phase noise will occur with -20 dB/decade. A Lower FOM here is better.

$$\mathrm{FOM}_{\mathrm{pn}} = \mathcal{L}(\Delta f) + 10\log_{10}\left(\left(\frac{\Delta f}{f_0}\right)^2\frac{P_{DC}}{1\ \mathrm{mW}}\right) \tag{44}$$

Another FOM applied to PLLs is provided below, based on the RMS jitter of the PLL [20]. Here, RMS jitter σ_{t_j} is used as the phase spectrum of a PLL is often more complicated than a simple oscillator, containing spurs, in-band phase noise suppression, and peaking resulting from the PLL loop filter. It should be noted that RMS jitter (in time) is tied directly to total phase

noise power, as expected by Parseval's theorem [21]. Lower is better again with this FOM.

$$\text{FOM}_{\text{jitter}} = 10\log_{10}\left(\frac{\sigma_{t_j}^2}{(1\text{ s})^2}\cdot\frac{P_{DC}}{1\text{ mW}}\right) \tag{45}$$

$$\sigma_{t_j}^2 = \frac{\text{Var}[\Phi_n(t)]}{\omega_0^2} \tag{46}$$

In general, a good figure of merit is arrived to by decreasing power and/or minimizing total phase noise power.

3.5.4 Ring Oscillator Phase Noise

Oscillator phase noise for ring oscillators has a well defined limit as determined through analysis of noise of ideal RC circuits [22], which is provided in equation 47. Note that this model is limited to analyzing the -20 dB/decade part of an oscillator's spectrum as seen by Leeson's model.

$$\mathcal{L}_{min}(\Delta f) = 10\log 10\left(\frac{7.33k_BT}{P_{DC}}\left(\frac{f_0}{\Delta f}\right)^2\right) \tag{47}$$

Applying this to the phase noise FOM equation 44, a limit for ring oscillator phase noise FOM is determined in equation 48.

$$\text{FOM}_{\text{pn,min}} = 10\log 10\left(7330k_BT\right) \tag{48}$$

At 300K, it is expected that the phase noise FOM for a ring oscillator should approach -165.2 dB. An example state of art comparison in figure 14 shows clustering by oscillator type for phase noise FOM calculated in various published works in [23]. It is seen the FOM value calculated from theory is close to that obtained in implemented ring oscillator hardware.

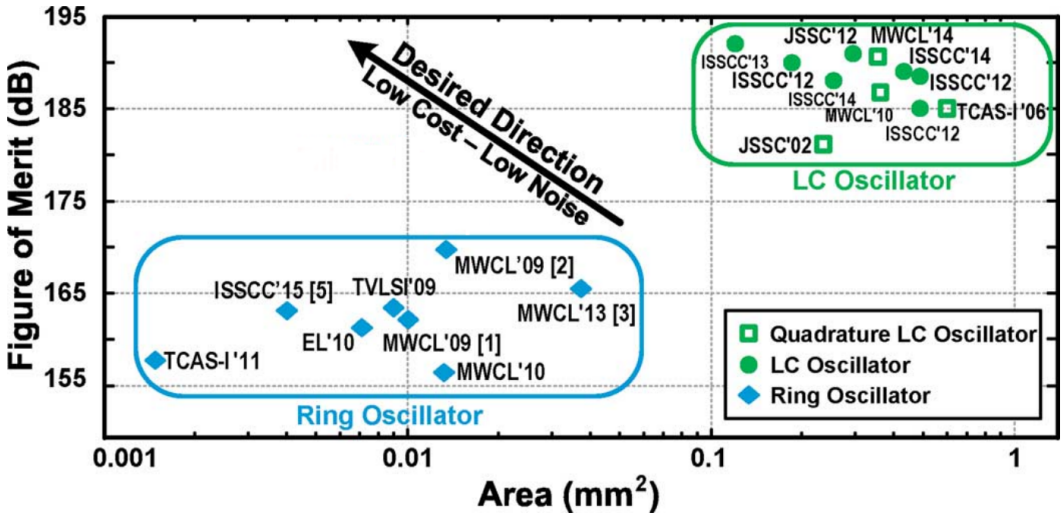


Figure 14: FOM$_{jitter}$ of various LC and ring oscillators, modified from [23].

3.6 PLL Phase Noise Theory

Having an understanding of PLL theory, individual PLL component characteristics, and phase noise, a model for PLL phase noise can be constructed. To begin, noise sensitivity transfer functions are defined to refer each noise source to the PLL output. Here, all noise sources have been defined as additive signal components to each PLL component output. The full system noise model is in figure 15.

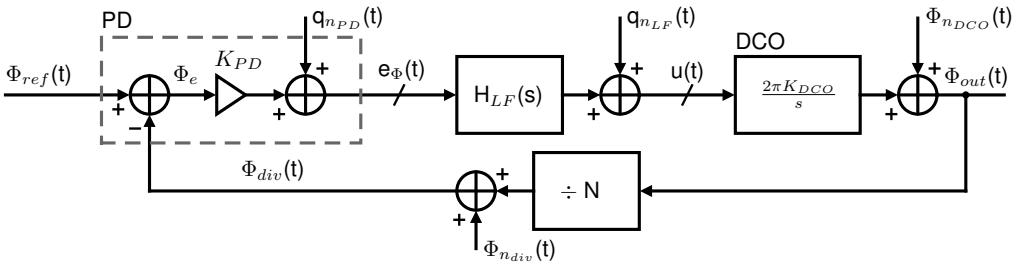


Figure 15: Full PLL additive noise model.

3.6.1 PLL Noise Transfer Functions

Following the approach of [24], a transfer function $\hat{\mathrm{T}}(s)$ is defined in equation 49 which characterizes the normalized closed loop phase response from reference input to output of the PLL. $L(s)$ is the PLL loop gain and $T(s)$ is the PLL closed loop transfer function.

$$\hat{\mathrm{T}}(s) = \frac{\mathrm{L}(s)}{1+\mathrm{L}(s)} \quad \text{s.t.} \quad \mathrm{T}(s) = \frac{\Phi_{out}}{\Phi_{ref}} = \mathrm{N}\hat{\mathrm{T}}(s) \tag{49}$$

Solving for the closed transfer functions between each noise source ($q_{n_{BBPD}}$, $q_{n_{LF}}$, $\Phi_{n_{DCO}}$ and $\Phi_{n_{div}}$) to the output Φ_{out} in the s-domain yields equations 50-53.

$$\frac{\Phi_{out}(s)}{q_{n_{PD}}(s)} = \frac{2\pi\frac{K_{DCO}}{s}\mathrm{H}_{LF}(s)}{1+\mathrm{L}(s)} = \frac{\mathrm{N}}{\mathrm{K_{PD}}}\frac{\mathrm{L}(s)}{1+\mathrm{L}(s)} = \frac{\mathrm{N}}{\mathrm{K_{PD}}}\hat{\mathrm{T}}(s) \tag{50}$$

$$\frac{\Phi_{out}(s)}{\Phi_{n_{DCO}}(s)} = \frac{1}{1+\mathrm{L}(s)} = 1-\hat{\mathrm{T}}(s) \tag{51}$$

$$\frac{\Phi_{out}(s)}{q_{n_{LF}}(s)} = \frac{2\pi\frac{K_{DCO}}{s}}{1+\mathrm{L}(s)} = 2\pi\frac{K_{DCO}}{s}(1-\hat{\mathrm{T}}(s)) \tag{52}$$

$$\frac{\Phi_{out}(s)}{\Phi_{n_{div}}(s)} = \frac{K_{BBPD}2\pi\frac{K_{DCO}}{s}\mathrm{H}_{LF}(s)}{1+\mathrm{L}(s)} = \mathrm{N}\frac{\mathrm{L}(s)}{1+\mathrm{L}(s)} = \mathrm{N}\hat{\mathrm{T}}(s) \tag{53}$$

3.6.2 PLL Output-referred Noise

Using the noise transfer functions, the expressions for noise power spectrum of the BBPD (equation 19) and the noise spectrum of a ring oscillator (equation 47), the PLL output phase noise spectrum of each component is determined by multiplying the magnitude squared of each noise transfer function with the respective noise spectral density. Here it is found that the BBPD noise component out of the PLL is given in equation 54, and the oscillator component is given in equation 55. The loop filter and divider noise components are here ignored, as in this work they will be reduced to the point of insignificance.

$$S_{\Phi n_{BBPD,out}}(f) = S_{n_{BBPD}}(f)\left|\frac{\Phi_{out}(f)}{q_{n_{BBPD}}(f)}\right|^2 = \frac{\left(\frac{\pi}{2}-1\right)}{f_{ref}}\left|\sigma_{\Phi_e}\mathrm{N}\hat{\mathrm{T}}(f)\right|^2 \tag{54}$$

$$S_{\Phi n_{DCO,out}}(f) = \mathcal{L}_{min}(f)\left|\frac{\Phi_{out}(f)}{q_{n_{DCO}}(f)}\right|^2 = \frac{7.33k_BT}{P}\left(\frac{f_0}{f}\right)^2|1-\hat{\mathrm{T}}(f)|^2 \tag{55}$$

The total output noise power spectral density is given as the sum of the components, presuming independence of all noise sources. Following the results of section 3.5.1, which determined that oscillator power spectrum is equivalent to the phase noise power spectrum for zero mean phase noise with low power, the final oscillator power spectrum at Δf from the carrier is in equation 56.

$$S_{n_{PLL}}(f_{osc}+\Delta f) = S_{\Phi n_{BBPD,out}}(\Delta f) + S_{\Phi n_{DCO,out}}(\Delta f) \tag{56}$$

$$= \frac{\left(\frac{\pi}{2}-1\right)}{f_{ref}}\left|\sigma_{\Phi_e}\mathrm{N}\hat{\mathrm{T}}(\Delta f)\right|^2 + \frac{7.33k_BT}{P}\left(\frac{f_0}{\Delta f}\right)^2|1-\hat{\mathrm{T}}(\Delta f)|^2 \tag{57}$$

A complexity arises in equation 56 due to the fact that the power spectrum is a function of the root mean squared (RMS) phase error, σ_{Φ_e}. σ_{Φ_e} may be calculated as equation 58. It is seen that the spectrum and σ_{Φ_e} are circularly defined, so a system of equations formed by the two must be solved to determine the final noise spectrum.

$$\sigma_{\Phi_e} = \sqrt{2\int_0^\infty S_{n_{PLL}}(f_{osc}+\Delta f)d\Delta f} \tag{58}$$

4 PLL Architecture

To meet the goals of this work to achieve a state of art power consumption of $\leq 100\mu$W for 2.448 GHz operation, while maintaining better than 20.56 ps RMS of phase jitter, the PLL architecture of figure 16 has been devised. It comprises primarily of three main components:

1. A bang-bang phase detector.
2. An all digital proportional-integral controller loop filter.
3. A DCO implemented as a VCO digitized by capacitive DACs.

The high level rationale for this architecture will be described in the following subsections. Furthermore, section 5 details the design and implementation of the phase detector, section 6 details the design and implementation of the loop filter, and section 7 describes the design and implementation of the DCO.

4.1 Block Diagram

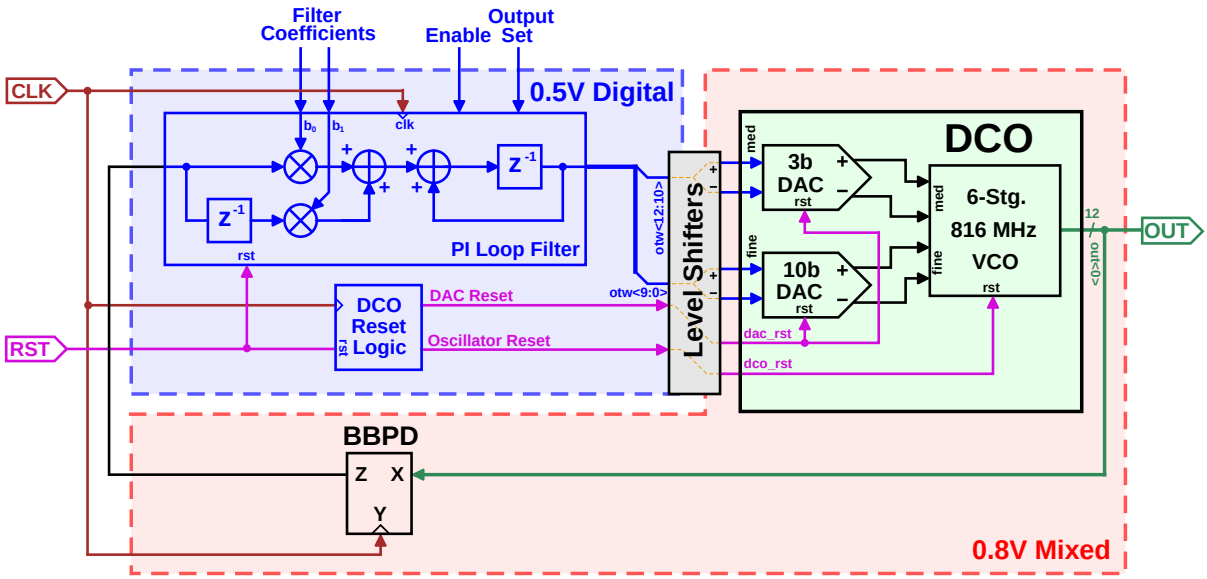


Figure 16: ADPLL Architecture.

4.2 Power Saving Driven Approach

The general design philosophy of this work is tailored to save power by pursuing simplicity wherever possible. Reduction of complexity will reduce number of sources of power draw, and will also reduce noise generated due to fewer devices providing contributions. Several measures have been employed to these ends. First of which is the omission of a divider in this design.

As will be later described, such a modification allows for reduction in phase noise contribution of the phase detector, and total removal of divider noise contributions. Furthermore, any power draw associated with the divider is avoided. The removal of the divider, however, requires that accurate calibration of the PLL frequency tuning range must be performed during cold start of the PLL. Implementation of such a calibration scheme should be expected to add minimal power consumption as any excess calibration circuitry required can be disabled during normal operation. Additional power improvements are obtained in the usage of digital logic to implement the loop filter in this work, using a simple PI-controller architecture. As shown in figure 16, the application of split power domains is used, with supplies of (a) 0.5V for loop filter, and (b) 0.8V for the DCO and phase detector. The multiple power domains allows for reduction of the digital logic supply voltage to just the level needed for reliable operation, saving power, while allowing for sufficient voltage for proper oscillator function. The digital nature of the loop filter lends itself to low sensitivity to process, voltage, and temperature (PVT) variation, and is expected that compared to analog designs, a smaller margin of safety in the power can be employed to ensure satisfactory performance with variation. The final architectural power saving move is implemented in a DCO based on the combination of several CDACs with a voltage controlled ring oscillator. This reduces to near zero the DC current draw associated with control of the VCO. The resulting overall design is therefore implemented with no static current paths (other than that associated with leakage), in hopes of achieving better energy efficiency than designs that require extraneous power draw, for example in those that utilize current mirrors needing reference current generation.

4.3 PLL Sleep Capability

As motivated by the end application of this PLL to wake up receivers, the architecture of the PLL has been developed to support duty cycled operation. Specifically, the architecture has been designed to enable rapid locking, such that duty cycling at high frequencies can be performed with a small level of overhead for relocking of PLL when returning to an active state. This is implemented through the usage of an all-digital architecture, which allows for the PLL to save digitally the loop filter state when entering a sleep state. The implication of this is that all unneeded portions of the PLL may be powered down during inactive periods, saving power, and upon resuming to an on-state, the PLL can be restored rapidly to its pre-sleep state. If the time interval of sleep is sufficiently short, it is expected that the oscillator and supply characteristics will only drift minorly, thus the PLL will be either in a locked state, or near-locked state when it resumes from the stored state. Compared to restarting from a totally unlocked state (for example in a cold start up), the time spent locking is expected to be greatly reduced with this architectural decision. Figure 17 demonstrates such operation described, where t_{l1} is the lock time from cold start, and t_{l2} is the time to relock from a resume state.

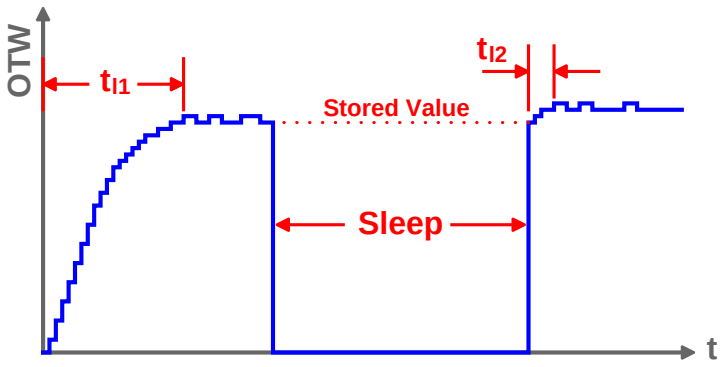


Figure 17: PLL sleep and resume operation.

4.4 Dividerless PLL

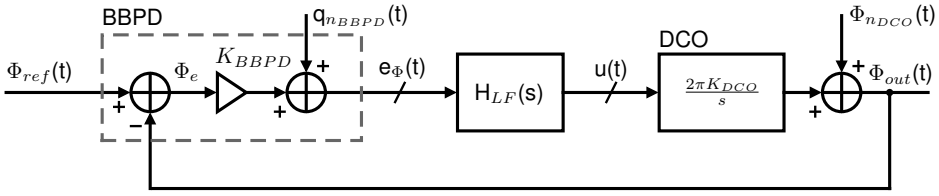


Figure 18: BBPD-PLL full noise model.

In the divider-based PLL theory (section 3.6.2), the derived PLL detector phase noise component (equation 54) contains a term proportional to N^2, that is the detector noise will grow with the square of the PLL divider ratio. It is, however, possible to remove this N^2 dependency by (a) removing the divider from the PLL, and (b) using a sub-sampling phase detector [25]. A subsampling phase detector operates by directly sampling the PLL output at a rate equivalent to the reference frequency. In this work, the sub-sampling phase detector is implemented in the form of a bang-bang phase detector.

In a dividerless PLL, it must be guaranteed that the PLL frequency at the start of sub-sampling operation be well within $f_{ref}/2$ of the target frequency (the PLL will lock to the nearest multiple of the reference frequency). In this work, although not implemented, it is suggested to implement a coarse frequency calibration scheme which can reliably tune the oscillator frequency within a small enough tolerance that the PLL can lock when BBPD-based operation is started.

In accordance to the change to dividerless operation, the PLL closed loop transfer function has been rederived in equation 59. Furthermore, new expressions for PLL output phase noise with a BBPD is given in equation 60, and PLL output oscillator noise with a ring oscillator is given in equation 61, for the BBPD-PLL noise model in figure 18. Noise due to the loop filter here is ignored, as it will be possible to adjust the loop filter datapath resolution to make digital

quantization noise effects negligible.

$$\mathrm{T}(s) = \frac{\Phi_{out}(s)}{\Phi_{ref}(s)} = \frac{2\pi K_{BBPD} K_{DCO} \sum_{j=0}^{Z} b_j s^j}{\sum_{k=0}^{P} a_k s^{k+1} + 2\pi K_{BBPD} K_{DCO} \sum_{j=0}^{Z} b_j s^j} = \frac{\mathrm{L}(s)}{1 + \mathrm{L}(s)} \tag{59}$$

$$S_{\Phi n_{BBPD,out}}(f) = S_{n_{BBPD}}(f) \left| \frac{\Phi_{out}(f)}{q_{n_{BBPD}}(f)} \right|^2 = \frac{\left(\frac{\pi}{2} - 1\right)}{f_{ref}} \left| \sigma_{\Phi_e} \mathrm{T}(f) \right|^2 \tag{60}$$

$$S_{\Phi n_{DCO,out}}(f) = \mathcal{L}_{min}(f) \left| \frac{\Phi_{out}(f)}{q_{n_{DCO}}(f)} \right|^2 = \frac{7.33 k_B T}{P} \left(\frac{f_0}{f} \right)^2 \left| 1 - \mathrm{T}(f) \right|^2 \tag{61}$$

4.5 Floorplan

To meet the design goal to achieve state of art for implementation area, the below floor plan (dimensions in microns) has been devised such that the total area is $<<$ 0.01 mm^2. The final implemented dimensions are 82μm x 47μm, with an active area of 0.00365 mm^2.

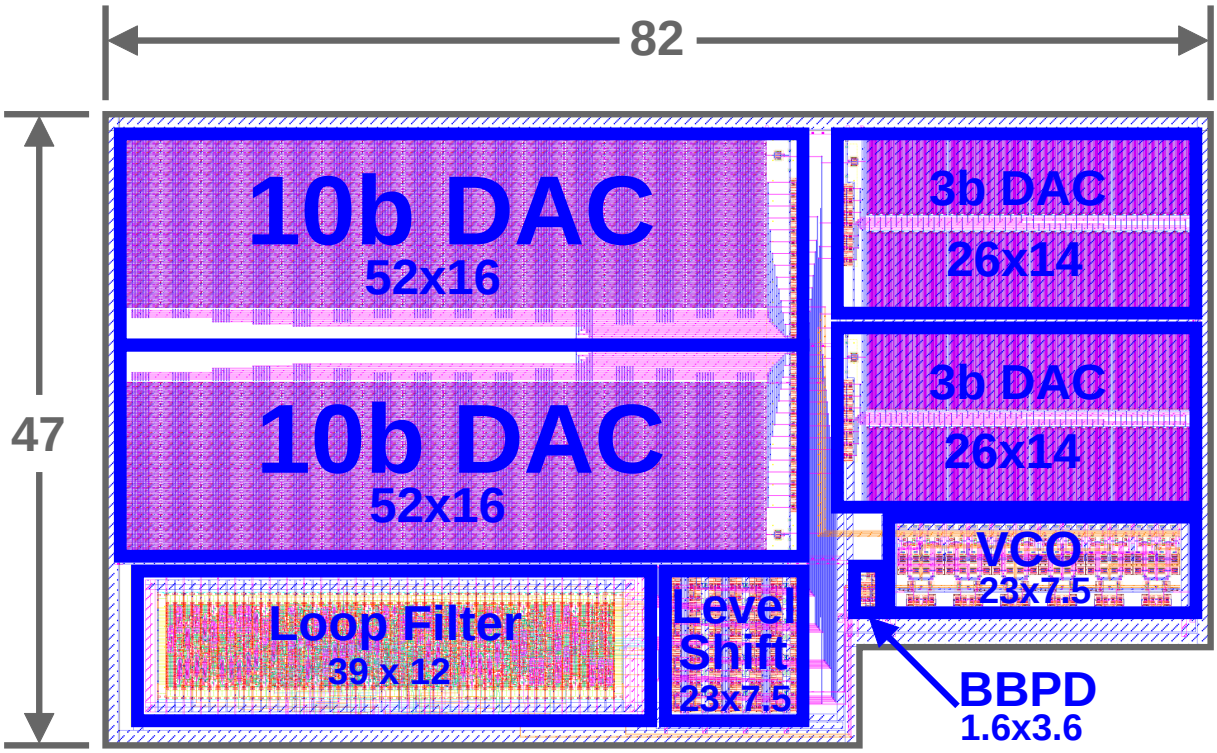


Figure 19: PLL floorplan (units in microns).

4.6 Power Budget

The below power budget was used in the design process to divide up the 100 μW allotment between the different PLL components. In order to minimize oscillator phase noise, the portion of power for the oscillator was chosen to be as large as possible.

DCO	Phase detector	Digital (LF)	Other	SUM
80 μW	5 μW	5 μW	5 μW	$\leq$ 95 μW

Table 3: Power budget for design process.

4.7 Note on Reference Frequency

The specified reference frequency for the PLL is 32 MHz, however, with a 2.448 GHz synthesized frequency, the ratio of reference to synthesized frequency is 76.5, which implies integer-N operation is not possible. Therefore, the reference frequency must be prescaled by a factor of 2 to 16 MHz, resulting in ratio of reference to synthesized frequency of 153, an integer. The reference value of 16 MHz is used in the remainder of this work.

5 Phase Detector Design

A bang-bang phase detector, as introduced in section 3.4.2, can be implemented physically with a D flip-flop [26] and logic to map the 0/1 valued output to a signed ± 1 value that may be passed into a digital loop filter. This is shown in figure 20.

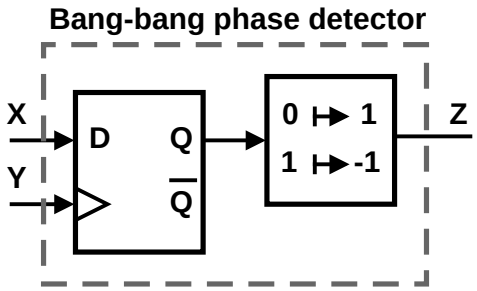


Figure 20: Bang-bang phase detector with D flip-flop.

The realization of a BBPD using a digital flip flop introduces additional noise to the system in the form of jitter. Jitter arises as an artifact of circuit and supply noise. For small time differentials between the BBPD inputs X and Y, the output can be stochastically corrupted due to the presence of noise. Furthermore, physical D flip flop implementations exhibit set-up and hold time requirements for data to be stable (to allow internal nodes to settle), so deterministic corruption of phase detection can be imparted if the inputs violate physical timing requirements. These sources of corruption cause BB-PD transfer characteristics in terms of output expectation, $\mathbb{E}[Z]$, with respect to input timing difference Δt_{XY} to deviate from an ideal step response, demonstrated in figure 21. Analytically, the corruption of the transfer characteristic can be viewed as being caused by an additive phase noise component before the signum operation in the BBPD, as shown in figure 22a. The expectation $\mathbb{E}[Z(\Delta t_{XY})]$ acts as a cumulative distribution function (CDF) for this phase noise component. Thus, differentiation of $\mathbb{E}[Z(\Delta t_{XY})]$ results in a probability distribution function (PDF) P(T=Δt_{xy}) of this phase noise signal. Statistical analysis of variance of the PDF provides an RMS value for timing jitter of this additive noise source, $\sqrt{\mathrm{Var}[T]} = \sigma_{tj}$. The RMS timing jitter may be converted to RMS phase error of the noise source as $\sigma_{\Phi_j} = 2\pi f_{osc}\sigma_{t_j}$. This statistical analysis approach has been applied in this work to evaluate BBPD performance.

With a model including BBPD noise due to implementation non-idealities, a modified linearized model for the BBPD will be established here. This model will reconcile the ideal BBPD noise introduced in section 3.4.2 with the noise due to the new additive jitter component just described. First, a phase noise component representing the non-ideal jitter component, Φ_j, is added into the noise model from figure 18. The result is the linearized model of figure 22b. We then define a modified phase error, $\hat{\Phi}_e$, which includes the nominal Φ_e and the jitter corruption:

$$\hat{\Phi}_e = \Phi_e + \Phi_j. \tag{62}$$

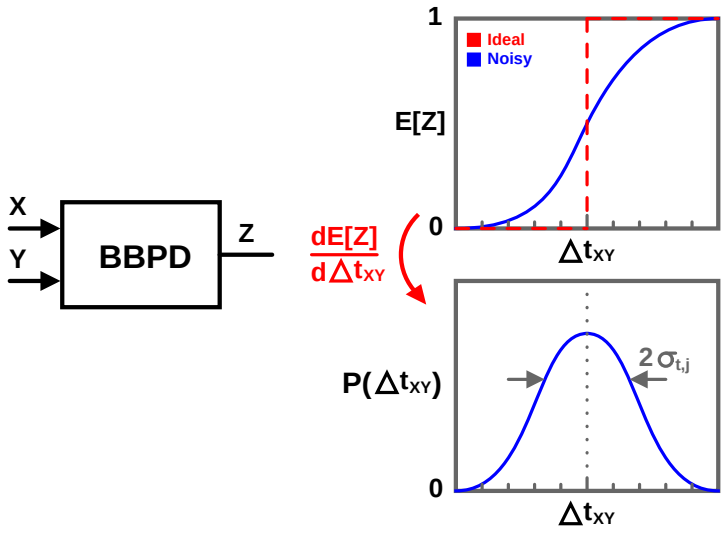


Figure 21: BBPD output expectation and jitter PDF versus input time differential.

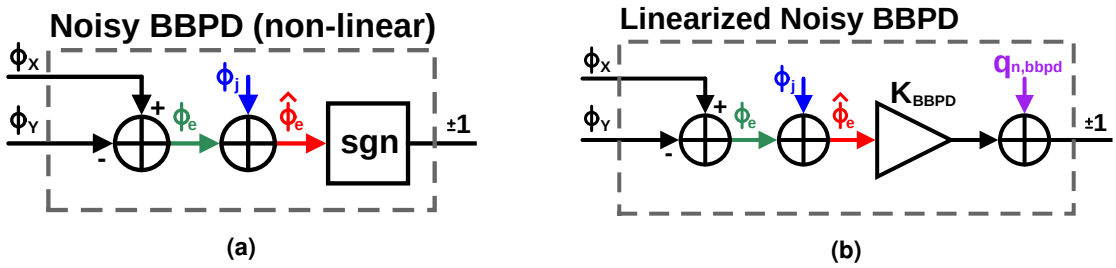


Figure 22: (a) Noisy BBPD nonlinear model **(b)** Noisy BBPD linearized model

$\hat{\Phi}_e$ has a variance defined as $\sigma^2_{\hat{\Phi}_e} = \sigma^2_{\Phi_e} + \sigma^2_{\Phi_j}$, assuming Φ_e and Φ_j are uncorrelated. Defining BBPD gain in terms of $\sigma_{\hat{\Phi}_e}$, using the equation from 17:

$$K_{BBPD} = \sqrt{\frac{2}{\pi}} \cdot \frac{1}{\sigma_{\hat{\Phi}_e}} = \sqrt{\frac{2}{\pi}} \cdot \frac{1}{\sqrt{\sigma^2_{\Phi_e} + \sigma^2_{\Phi_j}}} \tag{63}$$

It is then observed that the output Z is valued ± 1, thus its power is always $\sigma^2_Z = 1$. Furthermore:

$$\sigma^2_Z = 1 = K^2_{BBPD}(\sigma^2_{\phi_e} + \sigma^2_{\phi_j}) + \sigma^2_{q_{n,BBPD}} \tag{64}$$

As determined in section 3.4.2, $\sigma^2_{q_{n,BBPD}} = 1 - \frac{2}{\pi}$. The total output noise with detector jitter is then given in equation 65.

$$\sigma^2_{\phi_{n,BBPD}} = \sigma^2_{q_{n,BBPD}} + K^2_{BBPD}\sigma^2_{\phi_j} = 1 - \frac{2}{\pi}\frac{\sigma^2_{\phi_e}}{\sigma^2_{\phi_j} + \sigma^2_{\phi_e}} \tag{65}$$

If the BB-PD is connected directly to oscillator output, so $\sigma^2_{\phi_e} = \sigma^2_{\phi_n}$ (i.e. the PLL output phase

noise), the spectral density of the BB-PD phase noise is therefore:

$$S_{\phi_{n,BBPD}} = \frac{\sigma^2_{\phi_{n,BBPD}}}{f_{ref}} = \frac{1 - \frac{2}{\pi}\frac{\sigma^2_{\phi_n}}{\sigma^2_{\phi_j}+\sigma^2_{\phi_n}}}{f_{ref}} \tag{66}$$

$$S_{\Phi n_{BBPD,out}}(f) = S_{n_{BBPD}}(f)\left|\frac{\Phi_{out}(f)}{q_{n_{BBPD}}(f)}\right|^2 = \frac{\frac{\pi}{2}(\sigma^2_{\phi_j}+\sigma^2_{\phi_n}) - \sigma^2_{\phi_n}}{f_{ref}}\left|\mathrm{T}(f)\right|^2 \tag{67}$$

5.1 Circuit

The physical implementation of the bang-bang phase detector has been selected to utilize a true single phase clock (TSPC) D flip-flop [27]. The positive-edge triggered variant of this circuit has been implemented as shown in figure 23. Selection of this topology was based on the desire for the usage of a single ended clock as a reference signal.

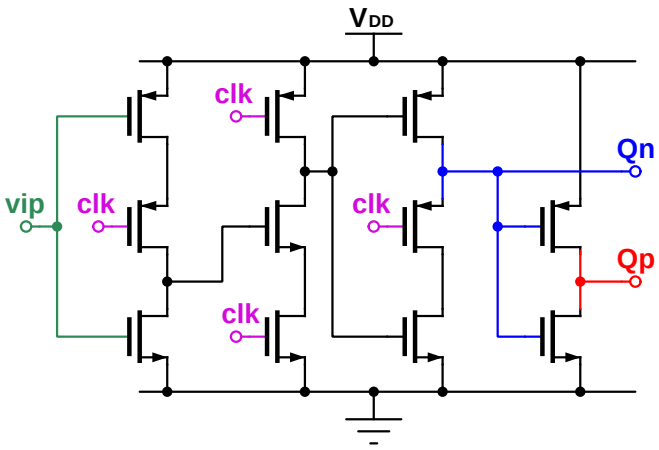


Figure 23: True single-phase clock (TSPC) D flip-flop, positive edge triggered.

This TSPC design was validated in simulation with regular voltage threshold (RVT) devices in the 22nm FD-SOI process with all devices set to have equal (W/L). (W/L) $\in$ {100n/20n, 200n/20n} were tested, and supply voltages of 0.5 and 0.8 volts were tested. It was determined that the implementation with (W/L) = 200n/20n for all devices and V_{DD} = 0.8 was satisfactory, as a low jitter value of 1.342 ps with 0.39 μW of power consumption was found, far lower than the 5 μW limit set in the power budget. The excess power allotment not used by the BBPD in the original power budget has been reassigned to the oscillator. Final simulation results for the BBPD are in the results section 9.6, and the layout in appendix B.6.

6 Loop Filter Design

For selection of the loop filter topology, some basic criteria have been selected for desirable synthesizer behavior:

1. Zero steady state error, for accuracy of the synthesized frequency.
2. Minimize complexity of implemented loop filter logic (i.e. minimize the number of loop filter poles and zeros).
3. Results in a closed-loop low pass response of the PLL.

From the author of this work's previous findings [1], it was established that the pole-zero filter that best satisfies these requirements is a proportional-integral controller.

6.1 Proportional-Integral Controller Loop Filter

A proportional-integral controller [28] is given in equation 68, containing an proportional gain term K_p, and an integral gain term K_i. This can be optionally represented using a pole at zero frequency and a zero at frequency $\omega_z = K_i/K_p$.

$$\mathrm{H}_{LF}(s) = K_p + \frac{K_i}{s} = \frac{K_i}{s}\left(\frac{s}{\omega_z} + 1\right) \tag{68}$$

Substitution of this controller into the PLL closed loop transfer function (equation 59) results in equation 69.

$$T(s) = \frac{\Phi_{out}(s)}{\Phi_{ref}(s)} = \frac{2\pi K_{BBPD} K_{DCO} K_i \left(\frac{s}{\omega_z} + 1\right)}{s^2 + 2\pi K_{BBPD} K_{DCO} K_i \left(\frac{s}{\omega_z} + 1\right)} \tag{69}$$

6.2 Discretization of the Loop Filter

Using the continuous filter discretization approach described in section 3.4.5 on the loop filter of equation 68 results in equation 70. When converting a continuous time PLL model into a discrete time controller implementation, a commonly cited rule of thumb in PLL literature states that the PLL loop bandwidth should be constrained as $BW_{loop} \leq 0.1 f_{ref}$ [29] (here $\Delta T_s = 1/f_{ref}$). This is due to the fact that low degrees of oversampling lead to deviations between continuous PLL models and real sampled-PLL performance, possibly causing instability or

sub-optimal performance versus an intended design.

$$\mathrm{H}_{LF}(z) = \frac{K_i}{s}\left(\frac{s}{\omega_z}+1\right)\Big|_{s=\frac{1}{\Delta T_s}(1-z^{-1})} = K_p\frac{(1+\omega_z\Delta T_s)-z^{-1}}{1-z^{-2}} \tag{70}$$

The transformation of equation 70 into a digitally implementable design as a direct form 1 IIR filter shown in figure 24. Its filter coefficients are given by equations 71 and 72.

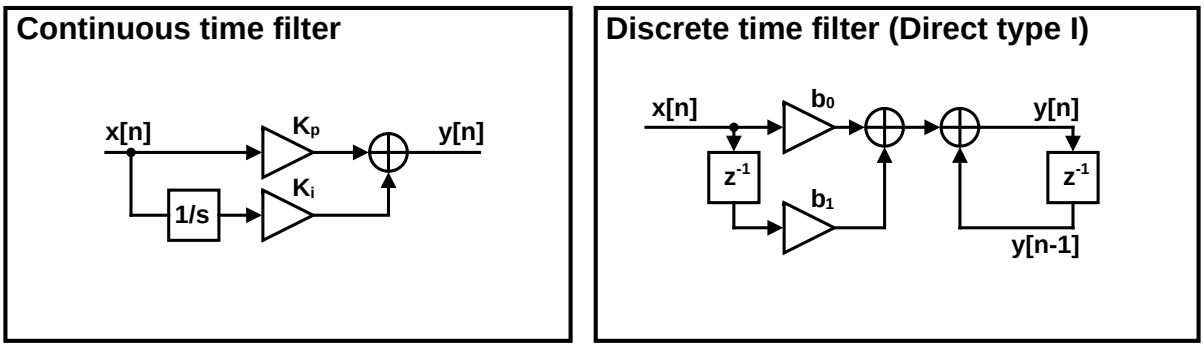


Figure 24: Implementation of filter.

$$b_0 = K_p(1+\omega_z\Delta T_s) \tag{71}$$

$$b_1 = -K_p \tag{72}$$

6.3 Filter Simplification

In order to aid later optimization of the loop filter, some mathematical simplifications of the PLL model are introduced here to the PI-filter design of equation 69. Rewriting equation 69 with substitutions $\omega_z = K_i/K_p$ and the gain constant $\mathrm{K} = 2\pi K_{BBPD}K_{DCO}K_i$:

$$T(s) = \frac{\Phi_{out}(s)}{\Phi_{ref}(s)} = \frac{s\frac{K}{\omega_z}+K}{s^2+s\frac{K}{\omega_z}+K} \tag{73}$$

The denominator can be redefined in terms of a natural frequency ω_n and damping ratio ζ:

$$s^2+s\frac{K}{\omega_z}+K = s^2+s2\zeta\omega_n+\omega_n^2 \tag{74}$$

Thus, $\omega_n = \sqrt{K}$, and $\omega_z = \sqrt{K}/2\zeta$. The poles of equation 73 are then located at s = $\zeta\sqrt{K} \pm j\sqrt{K}\sqrt{1-\zeta^2}$. The time constant of the PLL is obtained from the real portion of the dominant pole in equation 73:

$$\tau = \frac{1}{|\min(\Re(\{s_{p1}, s_{p2}\}))|} \tag{75}$$

It is of interest to minimize settling time of the PLL (i.e. time constant), thus maximizing the frequency of the dominant pole of the PLL is of interest. In the pole-zero plot of figure 25, the dominant pole of equation 73 is observed to be maximized with $\zeta = 1$ (loci are oriented based on increasing ζ values). Typically ζ is constrained in the range of $\sqrt{2}/2$ or 1 [11], to avoid excessive ringing. Accordingly it has been chosen to fix $\zeta = 1$ for the PI-controller.

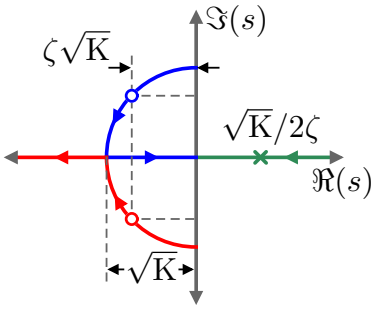


Figure 25: PI-controller PLL pole-zero locations.

With ζ is constrained to 1, the final simplified PLL closed loop transfer function is in equation 76. The form of this equation is favorable for computing integrations, allowing for a closed form solution to be found for the different PLL phase noise contributions. Furthermore, this transfer function only contains one parameter, K, which allows for simple single-variate optimization to be undertaken for the filter design.

$$T(s) = \frac{2\sqrt{K}s + K}{s^2 + 2\sqrt{K}s + K} = \frac{2\sqrt{K}s + K}{(s + \sqrt{K})^2} \tag{76}$$

6.4 Filter Optimization (Noisy BBPD)

Optimization of a loop filter under BBPD operation will be performed by minimizing the total integrated phase noise power out of the PLL. Accordingly, the PLL output referred noise power of the oscillator and BBPD will be calculated. First, the phase noise density of the oscillator (without the PLL) is defined as equation 77, where $S_{0_{osc}}$ is defined as the oscillator spectral density at 1 Hz frequency offset from the carrier. This is in the same form as the theoretical limit for ring oscillator phase noise in section 3.5.4. $S_{0_{osc}}$ can be found from a phase noise measurement of the oscillator $\mathcal{L}(f)$ at carrier offset f.

$$\mathcal{L}(f) = \frac{S_{0_{osc}}}{f^2} \quad \rightarrow \quad S_{0_{osc}} = \mathcal{L}(f)f^2 \tag{77}$$

The PLL output spectrum is then computed as:

$$S_{\Phi n_{DCO,out}}(f) = \mathcal{L}(f)|1 - \mathrm{T}(f)|^2 = \frac{S_{0_{osc}}}{f^2}|1 - \mathrm{T}(f)|^2 \tag{78}$$

Now, $|1 - \mathrm{T}(f)|^2$ is found to be after much simplification:

$$|1 - \mathrm{T}(f)|^2 = \frac{f^4}{\left(f^2 + \frac{K}{(2\pi)^2}\right)^2} \tag{79}$$

Thus, re-evaluating equation 78 yields:

$$S_{\Phi n_{DCO,out}}(f) = S_{0_{osc}} \frac{f^2}{\left(f^2 + \frac{K}{(2\pi)^2}\right)^2} \tag{80}$$

The total PLL phase noise power associated with the oscillator, $\sigma^2_{\Phi_{n,DCO}}$ is computed by integrating equation 80 with respect to frequency.

$$\sigma^2_{\Phi_{n,DCO}} = \int_{-\infty}^{\infty} S_{\Phi n_{DCO,out}}(f) df = S_{0_{osc}} \int_{-\infty}^{\infty} \frac{f^2}{\left(f^2 + \frac{K}{(2\pi)^2}\right)^2} df \tag{81}$$

$$= S_{0_{osc}} \frac{\pi^2}{\sqrt{K}} \tag{82}$$

Next, the total BBPD noise at the PLL output is computed. The expression for BBPD noise density in equation 67 will be used, and for which $|\mathrm{T}(f)|^2$ must be computed. This is:

$$|\mathrm{T}(f)|^2 = \frac{4\frac{K}{(2\pi)^2} f^2 + \frac{K^2}{(2\pi)^4}}{\left(f^2 + \frac{K}{(2\pi)^2}\right)^2} \tag{83}$$

The resulting BBPD spectral density equation is:

$$S_{\Phi n_{BBPD,out}}(f) = \frac{\frac{\pi}{2}(\sigma^2_{\phi_j} + \sigma^2_{\phi_n}) - \sigma^2_{\phi_n}}{f_{ref}} |\mathrm{T}(f)|^2 \tag{84}$$

$$= \frac{\frac{\pi}{2}(\sigma^2_{\phi_j} + \sigma^2_{\phi_n}) - \sigma^2_{\phi_n}}{f_{ref}} \cdot \frac{4\frac{K}{(2\pi)^2} f^2 + \frac{K^2}{(2\pi)^4}}{\left(f^2 + \frac{K}{(2\pi)^2}\right)^2} \tag{85}$$

The total PLL phase noise power associated with the BBPD, $\sigma^2_{\Phi_{n,BBPD}}$ is computed by integrating equation 84 with respect to frequency:

$$\sigma^2_{\Phi_{n,BBPD}} = \frac{\frac{\pi}{2}(\sigma^2_{\phi_j} + \sigma^2_{\phi_n}) - \sigma^2_{\phi_n}}{f_{ref}} \int_{-\infty}^{\infty} \frac{4\frac{K}{(2\pi)^2} f^2 + \frac{K^2}{(2\pi)^4}}{\left(f^2 + \frac{K}{(2\pi)^2}\right)^2} df \tag{86}$$

$$= \frac{5\sqrt{K}}{4 f_{ref}} \cdot \left[\frac{\pi}{2}(\sigma^2_{\phi_j} + \sigma^2_{\phi_n}) - \sigma^2_{\phi_n}\right] \tag{87}$$

The total phase noise power out of the PLL is therefore the sum of $\sigma^2_{\Phi_{n,BBPD}}$ and $\sigma^2_{\Phi_{n,DCO}}$:

$$\sigma^2_{\phi_n} = \sigma^2_{\Phi_{n,DCO}} + \sigma^2_{\Phi_{n,BBPD}} = S_{0_{osc}} \frac{\pi^2}{\sqrt{K}} + \frac{5\sqrt{K}}{4f_{ref}} \cdot \left[\frac{\pi}{2}(\sigma^2_{\phi_j} + \sigma^2_{\phi_n}) - \sigma^2_{\phi_n}\right] \tag{88}$$

Reorganization of equation 88 in terms of $\sigma^2_{\phi_n}$ yields:

$$\sigma^2_{\phi_n} = \frac{S_{0_{osc}} \frac{\pi^2}{\sqrt{K}} + \frac{5\pi\sqrt{K}}{8f_{ref}} \sigma^2_{\phi_j}}{1 - \frac{5\sqrt{K}}{4f_{ref}}(\frac{\pi}{2} - 1)} \tag{89}$$

In the presence of a non-ideal phase detector having phase noise power $\sigma^2_{\phi_j} = (2\pi f_{osc})^2 \sigma^2_{t_j}$, where σ_{t_j} is the detector's jitter in time, the optimal value K that minimizes phase noise is obtained as the solution of $d\sigma^2_{\phi_n}/dK = 0$. This result is given in equation 90. The obtained result for K_{opt} may be substituted into equation 89 to determine the total noise power $\sigma^2_{\phi_n}$.

$$K_{opt} = \left[\frac{S_{0_{osc}}\pi(\pi - 2)}{\sigma^2_{\phi_j}} - \sqrt{\frac{S^2_{0_{osc}}\pi^2(\pi - 2)^2}{\sigma^4_{\phi_j}} + \frac{S_{0_{osc}} 8\pi f_{ref}}{5\sigma^2_{\phi_j}}}\right]^2 \tag{90}$$

The parameter of K has a direct relationship to the closed loop bandwidth BW_{loop} of the PLL, which is determined by solving $|T(f)|^2 = 0.5$. The result of this is given in equation 91.

$$BW_{loop} = \frac{1}{2\pi}\sqrt{K}\sqrt{3 + \sqrt{10}} \tag{91}$$

As mentioned before, it is advisable to observe a limit of loop bandwidth of at most BW_{loop} = $0.1 f_{ref}$. The coefficient α is defined here now to describe the loop bandwidth-reference frequency ratio, where $BW_{loop} = \alpha f_{ref}$. In the potential case that α must be constrained for sampling reasons, equation 92 is found to determine K. Thus with a 16 MHz reference, and α = 0.1, it is found that $K \leq 1.64 \times 10^{13}$.

$$K_\alpha = \frac{(2\pi\alpha f_{ref})^2}{3 + \sqrt{10}} \tag{92}$$

Analyzing phase noise in terms of α, it is seen it is best to be as near to the optimal value of α as possible. Figure 26 demonstrates the effect of α on the phase noise power (normalized to the optimal value). The total phase noise asymptotically grows to infinity as α approaches 0 and 0.55. In the case of α = 0.1, the phase noise is expected to be 1.69 times the optimal value, resulting in a 2.3 dB degradation in phase noise power from optimal.

It is possible to derive a constraint for BBPD jitter $\sigma^2_{\phi_j}$ in terms of α and a target $\sigma^2_{\phi_n}$ (i.e. CNR value), providing a performance specification for the design of the physical BBPD. Equation 93 defines the maximum allowable phase noise power due to BBPD jitter, and equation 94 defines

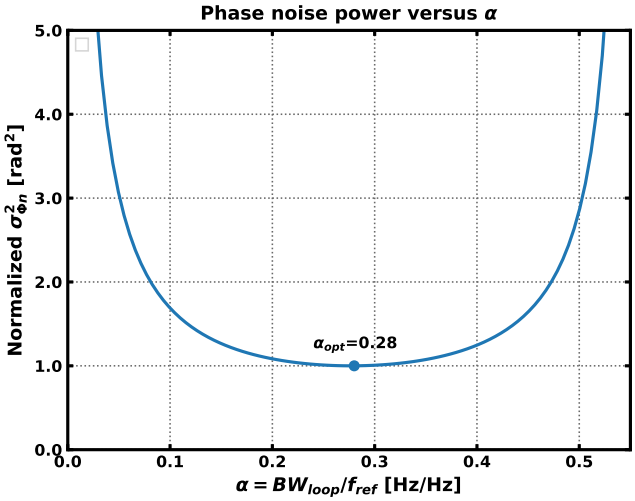


Figure 26: Phase noise power (normalized) versus α.

the maximum RMS jitter in time of the same detector.

$$\sigma_{\phi_j}^2 \leq \sigma_{\phi_n}^2 \left[\frac{4\sqrt{3+\sqrt{10}}}{5\pi^2\alpha} + \frac{2}{\pi} - 1 \right] - \frac{2S_{0_{osc}}(3+\sqrt{10})}{5\pi\alpha^2 f_{ref}} \tag{93}$$

$$\sigma_{t_j} \leq \frac{\sigma_{\phi_n}}{2\pi f_{osc}} \sqrt{\left[\frac{4\sqrt{3+\sqrt{10}}}{5\pi^2\alpha} + \frac{2}{\pi} - 1 \right] - \frac{2S_{0_{osc}}(3+\sqrt{10})}{5\pi\alpha^2 f_{ref}}} \tag{94}$$

Now with theory in place to optimize PLL performance, mapping of the optimal parameter K onto the loop filter of equation 68 will be considered. Recall that $\omega_z = K_i/K_p = \sqrt{K}/2\zeta$ and $K = 2\pi K_{BBPD} K_{DCO} K_i$. The parameters K_i, K_p, and ω_z are thus provided in equations 95-97.

$$\omega_z = \frac{\sqrt{K}}{2} \tag{95}$$

$$K_p = \frac{\sqrt{K}}{\pi K_{BBPD} K_{DCO}} = \frac{\sqrt{K}\sqrt{\sigma_{\phi_j}^2 + \sigma_{\phi_n}^2}}{\sqrt{2\pi} K_{DCO}} \tag{96}$$

$$K_i = \frac{K}{2\pi K_{BBPD} K_{DCO}} = \frac{K\sqrt{\sigma_{\phi_j}^2 + \sigma_{\phi_n}^2}}{2\sqrt{2\pi} K_{DCO}} \tag{97}$$

Converting the filter design into the discrete time equivalent results in equations 98 and 99

$$b_0 = \frac{\sqrt{K}\sqrt{\sigma_{\phi_j}^2 + \sigma_{\phi_n}^2}}{\sqrt{2\pi} K_{DCO}} \left(1 + \frac{\sqrt{K}}{2 f_{ref}} \right) \tag{98}$$

$$b_1 = -\frac{\sqrt{K}\sqrt{\sigma_{\phi_j}^2 + \sigma_{\phi_n}^2}}{\sqrt{2\pi} K_{DCO}} \tag{99}$$

If design of the PLL has a fixed target for $\sigma^2_{\phi_n}$ (CNR), a known $\sigma^2_{\phi_j}$ for the BBPD, and α is selected to be constant (e.g. α = 0.1), the filter coefficients may be calculated as in equations 100 and 101.

$$b_0 = \frac{\alpha f_{ref}\sqrt{2\pi}\sqrt{\sigma^2_{\phi_j} + \sigma^2_{\phi_n}}}{\sqrt{3+\sqrt{10}}K_{DCO}}\left(1 + \frac{\pi\alpha}{\sqrt{3+\sqrt{10}}}\right) \tag{100}$$

$$b_1 = -\frac{\alpha f_{ref}\sqrt{2\pi}\sqrt{\sigma^2_{\phi_j} + \sigma^2_{\phi_n}}}{\sqrt{3+\sqrt{10}}K_{DCO}} \tag{101}$$

6.5 Emergent Bang-Bang PLL Phase Noise

Since the output of BBPD is quantized to $\pm$ 1, the use of a PI loop filter architecture results in only 4 possible values that node **x** can be valued as shown in the simplified BBPD-PLL model of figure 27. These are $(b_0 + b_1)$, $(b_0 - b_1)$, $(-b_0 + b_1)$, and $(-b_0 - b_1)$. The result of this is the loop filter output **u** must increment by one of these four values every reference cycle.

The worst case scenario of this is the BBPD outputting an alternating sequence of +1/-1/+1/-1..., for which the output will toggle by increments $(b_0 - b_1)$ and $(-b_0 + b_1)$, alternating every cycle. In terms of frequency, the output will either alternate up or down by $K_{DCO}|b_0 - b_1|$ every cycle, which can be substantial depending on the product of those factors. In the phase domain, this results in a cyclostationary triangle wave-like phase trajectory (ignoring other sources of phase noise), as shown in figure 28a. The worst case increment in phase per cycle is given in equation 102. In the frequency domain, this cyclostationary behavior can result in spurs, as shown in figure 28b. When phase noise from other processes in the PLL are large enough that the they dwarf the worst case cyclostationary behavior, it is expected that the output of the BBPD will be stochastically scrambled and the cyclostationary effects will be subsided.

$$\Delta\Phi = \frac{2\pi|b_0 - b_1|K_{DCO}}{f_{ref}} \tag{102}$$

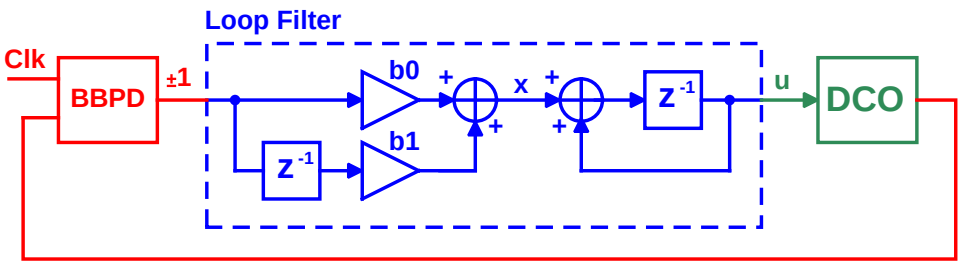


Figure 27: Simplified model of BBPD-PLL

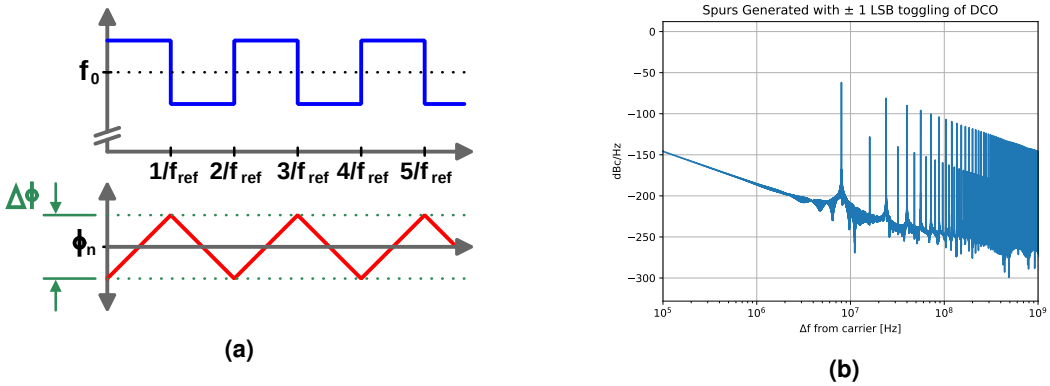


Figure 28: (a) Worst case cyclostationary behavior of BBPD-PLL, **(b)** Resulting spurs from worst case cyclostationary behavior.

Even if cyclostationary effects are avoided, the quantization of the loop filter output to increments of the four aforementioned values results in an additive phase noise contribution to the PLL. These increments result in a forced deterministic change in output phase error in every reference interval. The RMS contribution of phase noise to the PLL output due to the quantized steps in frequency from bang-bang operation has the relationship given in equation 103. This phase noise component will be termed "emergent bang-bang phase noise", represented by $\Phi_{n_{em}}$. Optimization of the PLL with inclusion of emergent bang-bang phase noise contributions will now be considered in the following section.

$$\sigma_{\Phi_{n_{em}}} \approx \frac{\pi |b_0 - b_1| K_{DCO}}{f_{ref}} \tag{103}$$

6.5.1 Filter Optimization (Emergent Bang-Bang PLL Phase Noise)

To optimize the PLL loop filter design for emergent bang-bang effects, the phase noise contribution for this component must be determined. Based on the findings of the previous section, equation 103 is modified by adding a proportionality constant β_1, resulting in equation 104. The value of this proportionality constant has been computed through simulation, as is later detailed.

$$\sigma_{\Phi_{n_{em}}} = \beta_1 \frac{\pi |b_0 - b_1| K_{DCO}}{f_{ref}} \tag{104}$$

Based on equations 100 and 101, the quantity $|b_0 - b_1|$ found to be that in equation 105. It will be shown that α is a constant under optimal conditions, so the optimized $|b_0 - b_1| = 2\beta_2 |b_1|$, where β_2 is a constant proportionality factor. Lumping proportionality constants together, we

define $\beta = \beta_1\beta_2$, thus $\sigma_{\Phi_{n_{em}}}$ is defined in equation 106.

$$|b_0 - b_1| = \left(2 + \frac{\pi\alpha}{\sqrt{3+\sqrt{10}}}\right)|b_1| = 2\beta_2|b_1| \tag{105}$$

$$\sigma_{\Phi_{n_{em}}} = \frac{2\pi\beta|b_1|K_{DCO}}{f_{ref}} \tag{106}$$

Including $\sigma^2_{\Phi_{n_{em}}}$, BBPD noise and oscillator noise, the total phase noise $\sigma^2_{\Phi_n}$ out of the PLL is in equation 107.

$$\sigma^2_{\Phi_n} = \sigma^2_{\Phi_{n,DCO}} + \sigma^2_{\Phi_{n_{BBPD}}} + \sigma^2_{\Phi_{n_{em}}} = S_{0_{osc}}\frac{\pi^2}{\sqrt{K}} + \sigma^2_{\phi_n}\frac{5\sqrt{K}}{4f_{ref}}\cdot\left(\frac{\pi}{2} - 1\right) + \sigma^2_{\Phi_{n_{em}}} \tag{107}$$

Redefining equation 99 using equation 107 as the phase noise power value results in equation 108.

$$b_1 = -\frac{\sqrt{K}\sqrt{\sigma^2_{\Phi_{n,em}} + \sigma^2_{\Phi_{n,DCO}} + \sigma^2_{\Phi_{n_{BBPD}}}}}{\sqrt{2\pi}K_{DCO}} \tag{108}$$

$$= -\frac{\sqrt{K}\sqrt{\sigma^2_{\Phi_{n_{em}}} + S_{0_{osc}}\frac{\pi^2}{\sqrt{K}} + \sigma^2_{\phi_n}\frac{5\sqrt{K}}{4f_{ref}}\left(\frac{\pi}{2} - 1\right)}}{\sqrt{2\pi}K_{DCO}} \tag{109}$$

An expression for $\sigma^2_{\Phi_{n_{em}}}$ given in equation 110 is obtained by solving the system of equations formed by equations 106 and 108. Redefining K in terms of α as defined by equation 92 results in the latter portion of the equation.

$$\sigma^2_{\Phi_n} = \frac{S_{0_{osc}}\frac{\pi^2}{\sqrt{K}}}{1 + \frac{2\pi K\beta^2}{f^2_{ref}} - \frac{5\sqrt{K}}{4f_{ref}}\left(\frac{\pi}{2} - 1\right)} = \frac{\frac{\pi S_{0_{osc}}\sqrt{3+\sqrt{10}}}{2f_{ref}}}{\alpha - \alpha^2\frac{5\pi}{2\sqrt{3+\sqrt{10}}}\left(\frac{\pi}{2} - 1\right) - \alpha^3\frac{8\pi^3\beta^2}{3+\sqrt{10}}} \tag{110}$$

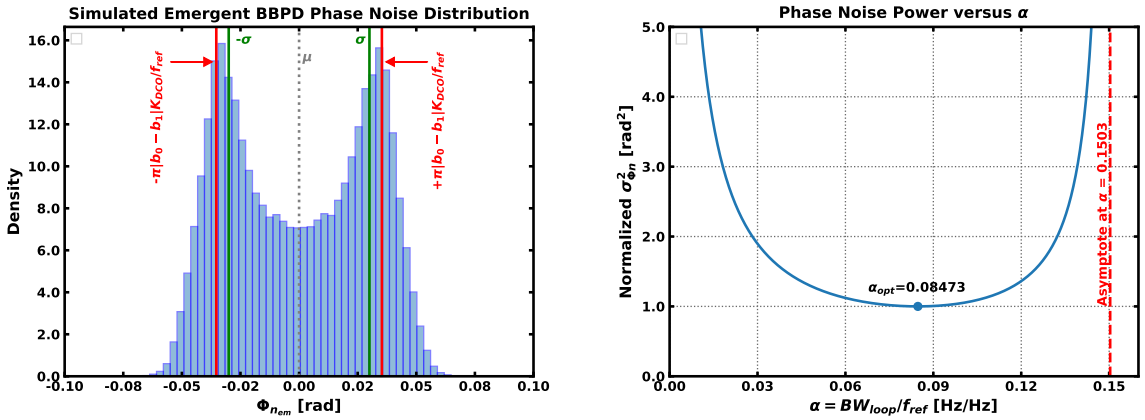
To minimize total phase noise power, $d\sigma^2_{\Phi_n}/d\alpha = 0$ is solved for, to yield the expression in equation 111 for optimal value of α.

$$\alpha_{opt} = -\frac{5\sqrt{3+\sqrt{10}}}{48\pi^2\beta^2} + \frac{1}{2}\sqrt{\frac{25(3+\sqrt{10})}{24^2\pi^4\beta^4}\left(\frac{\pi}{2} - 1\right)^2 + \frac{3+\sqrt{10}}{6\pi^3\beta^2}} \tag{111}$$

$$K_{opt} = \frac{(2\pi\alpha_{opt}f_{ref})^2}{3+\sqrt{10}} \tag{112}$$

Computation of the value of constant β is not straightforward, so it has been solved numerically through discrete time simulation of a PLL with a BBPD and PI-controller. This was obtained via a behavioral simulation in steady state over 1000000 reference cycles, with β varied until the prediction of $\sigma^2_{\Phi_{n_{em}}}$ and its value from simulation converged within a tolerance of 10^{-5}. It has been determined that at the optimum, β_{opt} = 0.895 and accordingly α_{opt} = 0.0847. Furthermore, β_1 = 0.850 and β_2 = 1.053. These values were observed to be independent of PLL frequency, oscillator phase noise, reference frequency and DCO gain. An example case of this simulation

is shown in figure 29a, where the ratio β_1 of equation 104 is seen with the vertical lines. Figure 29b shows the effect of α versus total integrated phase noise power. Total phase noise power grows asymptotically with $\alpha = 0$ and $\alpha = 0.1503$.



(a) (b)

Figure 29: (a) Simulated emergent bang bang phase noise component of PLL phase noise, **(b)** Total output phase noise (normalized) versus α.

Application of the determined optimal parameters into equation 110 results in equation 113.

$$\sigma^2_{\Phi_n}\Big|_{\alpha_{opt}} = 74.79376 \cdot \frac{S_{0_{osc}}}{f_{ref}} = 74.79376 \cdot \frac{\mathcal{L}_{osc}(f) f^2}{f_{ref}} \ [\text{rad}^2] \tag{113}$$

Computed discrete time filter coefficients for this optimization case are provided in equations 114 and 116.

$$b_0 = \frac{\alpha_{opt}\sqrt{74.79376 \cdot 2\pi S_{0_{osc}} f_{ref}}}{K_{DCO}\sqrt{3+\sqrt{10}}}\left(1 + \frac{\pi\alpha_{opt}}{\sqrt{3+\sqrt{10}}}\right) \tag{114}$$

$$= 0.8186975\frac{\sqrt{S_{0_{osc}} f_{ref}}}{K_{DCO}} \tag{115}$$

$$b_1 = -\frac{\alpha_{opt}\sqrt{74.79376 \cdot 2\pi S_{0_{osc}} f_{ref}}}{K_{DCO}\sqrt{3+\sqrt{10}}} \tag{116}$$

$$= -0.739456\frac{\sqrt{S_{0_{osc}} f_{ref}}}{K_{DCO}} \tag{117}$$

6.5.2 Choice of Optimization Strategy

Depending on the implementation, the noise contributions from the phase detector jitter may exceed the emergent bang bang phase noise components. This may be the case in high frequency PLLs, e.g. mm-wave PLLs, where cycle periods are short. For 2.4 GHz operation in 22nm technology, this poses less of a problem. In this work, two optimization theories have

been provided, for different noise regimes. The optimization theory of section 6.5.1 ignores detector jitter while considering emergent effects, and section 6.4 ignores emergent bang-bang behavior, while considering BBPD jitter. The recommended strategy for filter design is therefore to calculate the optimal filter design using both theories, and select the one that results in a larger total phase noise value $\sigma^2_{\Phi_n}$, as that will be the dominant noise mode.

In this work, using a -158.9 dB oscillator phase noise FOM at 2.448 GHz with 90μW of power, a 16 MHz reference, K_{DCO} = 4.2 kHz/LSB, and a detector jitter of 1.342 ps RMS, leads to a CNR of 15.5 dB when optimizing for oscillator plus jitter-inclusive BBPD noise, and a CNR of 13.6 dB when optimizing for oscillator noise plus emergent bang bang phase noise and jitterless detector noise. Selecting the worse valued result as the accurate model for this implementation then implies that this work should be optimized with the emergent bang-bang phase noise model.

The final optimized filter parameters for the design of this work are in the results section 9.7.

6.6 Loop Filter Implementation

The loop filter has been implemented digitally as shown in figure 30. Due to the fixed output possibilities of the BBPD (digital 0 or 1 corresponding to ± 1), the multipliers in the PI-controller have been replaced by multiplexers which select the appropriate signed version of the coefficients $\{b_0, b_1\}$, depending on the input sequence to the filter. Replacing the multipliers with multiplexers allows for substantial savings in terms of area and power, due to the significantly lower logical complexity to implement a parallel mux versus an array multiplier.

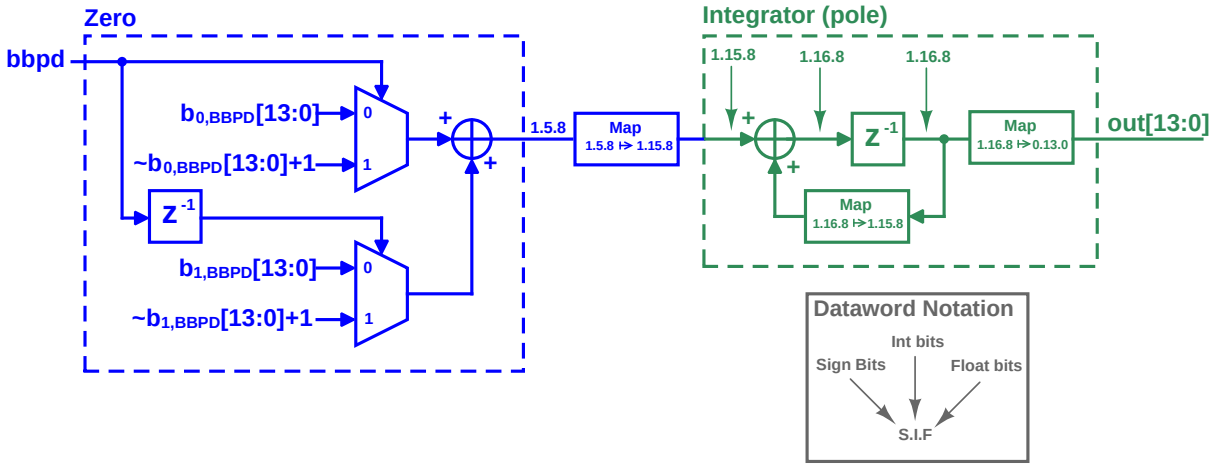


Figure 30: PI-controller implementation for combination of BBPD and synchronous counter usage.

The computed filter coefficients $\{b_0, b_1\}$ for the loop filter are digitized into finite length signed two's complement words. A two's complement data word contains one sign bit, and variable number of bits representing the integer and fractional portions of the encoded number. The

author of this work has previously devised a method [1] for automatically computing the number of bits required to represent a loop filter in an all digital PLL. First, the selection of number of integer bits `int_bits` is determined by considering the integer part of the filter coefficients. If the integer portions of the filter coefficients $\{b_0, b_1\}$ are divided into positive and negative valued sets `pos_ints` and `neg_ints`, the total integer bits required is therefore given in equation 120. Computation of the fractional portion is more complicated, and is based on reducing the quantization noise floor of the loop filter below the phase detector noise level of the PLL. The PLL design framework from [1] has been used in this work for determining the minimum digitized representation size of filter coefficients. This has been automatically computed such that the filter at most adds 0.1 dB of noise compared to BBPD noise components. Furthermore, the number of bits is optimized to minimize mean squared filter error below a limit, 0.1 dB is used in this work. Results from this optimization are shown in figure 31, where it has been found the minimum number of coefficient bits is 10, with 5 integer bits and 4 fractional bits. In order to further reduce quantization noise of the loop filter, the number of fractional bits has been set to 8 bits, bringing the total filter coefficient size to 14 bits. The output integrator of the loop filter has been implemented with 8 fractional bits, and 15 integer bits, where the output to the DCO is tapped of the integer portion of the integrator.

$$\texttt{pos\_int\_bits} = \lfloor \log_2 (\max (\lfloor \texttt{pos\_ints} \rfloor)) \rfloor + 1 \tag{118}$$

$$\texttt{neg\_int\_bits} = \lceil \log_2 (\max (\lfloor \texttt{neg\_ints} \rfloor)) \rceil \tag{119}$$

$$\texttt{int\_bits} = \max(\{\texttt{pos\_int\_bits}, \texttt{neg\_int\_bits}\}) \tag{120}$$

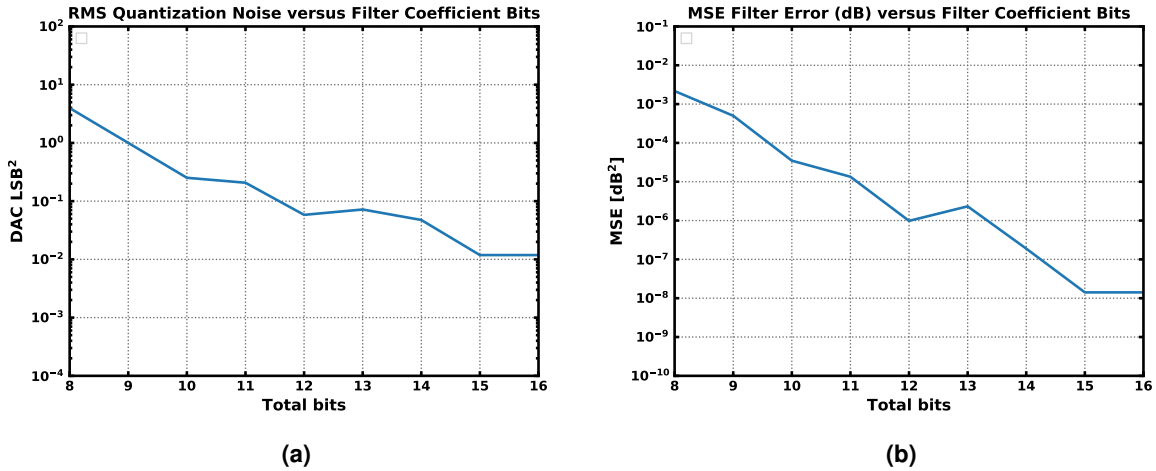


Figure 31: (a) Loop filter quantization noise versus coefficient dataword size, **(b)** Loop filter MSE versus coefficient dataword size.

The implemented loop filter Verilog hardware description used for logic synthesis is in appendix A.1.

7 DCO Design

The digitally controlled oscillator of this work has been implemented via the digitization of a voltage controlled oscillator (VCO) using digital to analog converters (DACs). The following sections will describe the implementation of a VCO, and the capacitive DACs used to digitize the VCO.

7.1 Selection of Oscillator Type

Oscillator circuits implemented in CMOS process technologies either fall under the category of resonant LC circuits, or RC based ring and relaxation oscillators. LC circuits provide favorable phase noise performance, as seen in figure 14, which shows typical phase noise improvements on the order of 20 dB for published LC designs over RC designs. This is due to the inherent nature of an LC circuit, as the higher the quality factor it has, the narrower the resonance line width and consequent phase noise is. In the ultra-low power domain of this work, however, ring oscillators pose several advantages over LC designs. These include substantially smaller integration area due to no need for integrated inductors, simpler design, convenient rail-to-rail signal levels, and lower achievable minimum power at a given frequency. Also significant is the ability to instantly startup a ring oscillator, which can be achieved with known initial phase if using appropriate phase reset circuitry. In a PLL using a BBPD, the ability to start the oscillator with a known zeroed-phase is highly beneficial. Due the simple nature of the BBPD, it is not possible to detect phase and frequency errors simultaneously, thus if a BBPD-PLL is started with both phase and frequency error, the PLL may not achieve lock. Initial zeroing of phase with a ring oscillator allows for phase uncertainty to be removed at start up, which allows for deterministic locking performance of the BBPD-PLL. With the intent of this design to allow for fast duty cycled operation, the need for deterministic locking and instant start up is imperative, thus, for this reason a ring oscillator topology has been selected for this work.

In this work, the ability of the FD-SOI backgate terminal to alter device threshold voltages has been utilized in order to implement a backgate voltage controlled ring oscillator as the main PLL VCO. The design process behind such an oscillator will be described in the following sections. A novel delay cell topology which exploits FD-SOI backgates to implement both differential operation and frequency is subsequently introduced. The described design enables usage of capacitive DACs to set oscillator control voltages, leading to minimal extra power consumption needed to convert the voltage controlled ring oscillator into a DCO.

7.2 Ring Oscillator Channel Length Consideration

Scaling of device channel lengths has a great impact on phase noise for ring oscillators. According to [7], ring oscillator phase noise takes the form of equation 121. V_{DD} is the supply voltage, V_t is the threshold voltage, P_{DC} is the oscillator power consumption, γp and γn are the respective PMOS and NMOS noise factors, f_0 is the oscillator frequency, and f is the offset from the carrier for the phase noise. It is expected that the excess noise factor of the transistor will increase with decreasing channel length [30], thus unavoidably phase noise will also increase with decreasing length following equation 121. To analyze the effect of channel length on ring oscillator performance in the 22nm technology used in this work, a 5-stage single ended ring oscillator was simulated for channel lengths between 20-500nm, with a fixed (W/L) = 5 and no external loading. The resulting phase noise FOM_{pn} data is shown in figure 32a, oscillator frequency in figure 32b. The phase noise FOM is that defined in equation 44. It is seen that FOM degrades as expected near minimum channel length, and improves asymptotically as the channel length grows. The asymptote closely correlates to that predicted theoretically for RC based oscillators, in equation 48. At 300K, as simulated, this is -165.2 dB. Better (i.e. lower valued) FOM corresponds to better phase noise per unit of oscillator power expenditure. Thus, based on the data of figure 32a, the best design strategy for this work to minimize phase noise for a fixed power budget is to use the longest possible channel length. Channel length limits frequency of operation, as seen in figure 32b, so there is an inherent trade off between frequency of operation and achievable FOM.

$$\mathcal{L}(f) = \frac{2kT}{P_{\text{DC}}}\left(\frac{V_{\text{DD}}}{V_{\text{DD}} - V_t}(\gamma_N + \gamma_P + 1)\right)\left(\frac{f_0}{f}\right)^2 \tag{121}$$

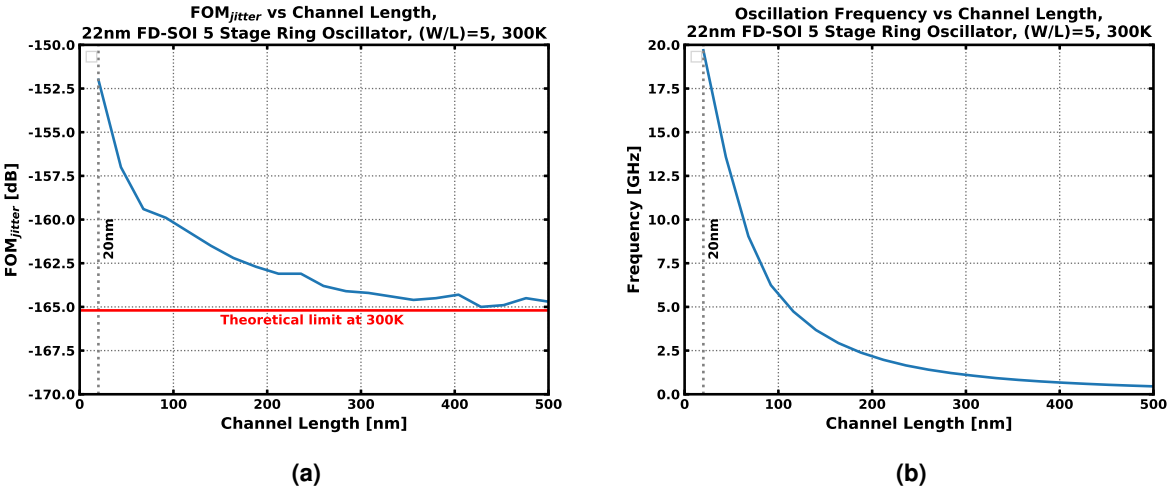


Figure 32: 22nm process ring oscillator channel length sweep versus **(a)** FOM, **(b)** Oscillation frequency.

7.3 Ring Oscillator Frequency Model

To analyze the effect of backgate tuning on a FD-SOI ring oscillator, a general mathematical model for CMOS ring oscillators will be developed first here. To begin, an approximate model for a CMOS inverter will first be considered. A typical model for delay in digital circuits is an RC circuit, where the MOSFET channels are approximated with an averaged conductance value $\langle g_{ch} \rangle$, and the output node is approximated to have a capacitance of C. With such a model, a ring oscillator is assumed to have waveforms that are decaying exponentials, with a time constant $\tau = \langle g_{ch} \rangle^{-1} C$. In context of the 3-stage ring oscillator of figure 33, figure 34 demonstrates the described inverter model and the resulting input and output waveforms.

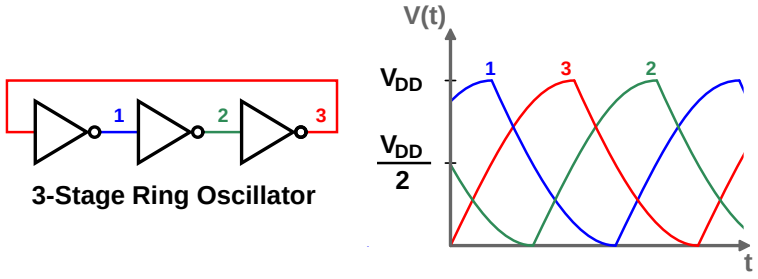
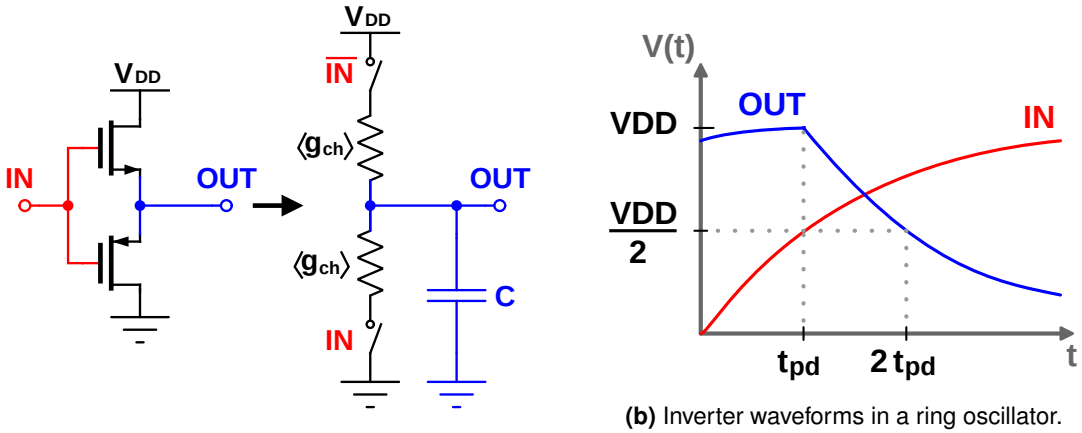


Figure 33: Model for ring oscillator.



(a) Inverter approximate model.

(b) Inverter waveforms in a ring oscillator.

Figure 34: Approximate model for ring oscillator inverter delay cell.

To calculate oscillation frequency of the ring oscillator from the RC model, several assumptions are made:

- The switching point V_M of the inverters is $V_{DD}/2$, based on the assumption that the NMOS and PMOS are of equal strength.
- The output of the inverters will be decaying exponentials which start coincident with the passing of V_M at the input.
- The propagation delay t_{pd} for an inverter will be the time differential between the V_M crossing points on the input and output.

- The oscillator frequency will be f_{osc} = $1/2Nt_{pd}$, where N is the number of stages (i.e. defined by 2N propagation delays).

Given the falling edge inverter waveform equation in 122, and observing that t_{pd} occurs at the point where $V(t) = V_{DD}/2$, it is found that t_{pd} = $\tau \ln(2)$. Finally, using the aforementioned assumptions, the equation for oscillator frequency is given in equation 123.

$$V(t) = V_{DD} \cdot e^{\frac{-t}{\tau}} \cdot u(t) \tag{122}$$

$$f_{osc}^{-1} = 2Nt_{pd} = \frac{2\ln(2)NC}{\langle g_{ch} \rangle} \tag{123}$$

7.3.1 Finding $\langle g_{ch} \rangle$ and C

The node capacitance C is trivial to find based on the inverter gate capacitance and a lumped load capacitance term C_L:

$$C = C_{ox}\left(W_N L_N + W_P L_N\right) + C_L \tag{124}$$

The average channel conductance $\langle g_{ch} \rangle$ is more involved to find. To do so, several assumptions are made:

- L >> L_{min}, so no velocity saturation, and therefore square law is applicable.
- NMOS and PMOS have equal V_{TH} and transconductance.
- Output transitions occur with the active FET in saturation from the start of the transition until t_{pd} after the start of the transition. This requires:
  - $V_{DD}/4 < V_{TH} < V_{DD}/2$

Following those assumptions, $\langle g_{ch} \rangle$ can be computed via integration within a period of t_{pd} from the start of a transition:

$$\langle g_{ch} \rangle = \frac{1}{t_{pd}} \int_0^{t_{pd}} \frac{I_{out}(t)}{V_{out}(t)} dt \tag{125}$$

I_{out} is computed using the saturated MOSFET square law model and the assumption of exponential waveforms. An I_{short} term is included to account for peak output current reduction from

short-circuit conduction when both PMOS and NMOS devices are on.

$$I_{out}(t) = \frac{k_n}{2}\left(\frac{W}{L}\right)_n \left[(V_{in}(t) - V_{TH})^2\right] - I_{short} \tag{126}$$

$$= \frac{k_n}{2}\left(\frac{W}{L}\right)_n \left[\left(V_{DD}\left(1 - e^{-t/\tau}\right) - V_{TH}\right)^2 - \left(\frac{V_{DD}}{2} - V_{TH}\right)^2\right] \tag{127}$$

$k_n = \mu_n C_{ox}$, and with assumption of equal PMOS/NMOS, $k_n \left(\frac{W}{L}\right)_n = k_p \left(\frac{W}{L}\right)_p$. V_{out} is simply a decaying exponential with a delay t_{pd} versus the input:

$$V_{out}(t) = V_{DD} e^{-(t-t_{pd})/\tau} u(t) \tag{128}$$

Now, computing the integral for $\langle g_{ch} \rangle$ yields:

$$\langle g_{ch} \rangle = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n \left[V_{DD}\left(\frac{7}{8\ln 2} - 1\right) - V_{TH}\left(\frac{1}{\ln 2} - 1\right)\right] \tag{129}$$

7.3.2 Oscillator Frequency and Power

Solving for oscillator frequency:

$$f_{osc} = \frac{\mu_n C_{ox}}{4\ln 2 NC}\left(\frac{W}{L}\right)_n \left[V_{DD}\left(\frac{7}{8\ln 2} - 1\right) - V_{TH}\left(\frac{1}{\ln 2} - 1\right)\right] \tag{130}$$

If gate capacitance is the dominant load component, and PMOS/NMOS are equal sized such that $C = 2WLC_{ox}$:

$$f_{osc} = \frac{\mu_n}{8\ln 2 N} \cdot \frac{1}{L^2}\left[V_{DD}\left(\frac{7}{8\ln 2} - 1\right) - V_{TH}\left(\frac{1}{\ln 2} - 1\right)\right] \tag{131}$$

Power can also be calculated, knowing in digital circuits $P = fC_\Sigma V_{DD}^2$, where C_Σ is the total capacitance of the active nodes. Thus:

$$P_{osc} = N f_{osc} C V_{DD}^2 = \frac{\mu_n C_{ox}}{4\ln 2}\left(\frac{W}{L}\right)_n \left[V_{DD}\left(\frac{7}{8\ln 2} - 1\right) - V_{TH}\left(\frac{1}{\ln 2} - 1\right)\right] \tag{132}$$

It should be noted that the power consumption is proportional to FET aspect ratio (W/L), regardless of the load or frequency.

7.3.3 Ring Oscillator Backgate Frequency Tuning

Using the basic expressions for ring oscillator frequency, the frequency characteristics under backgate biasing can be found. In FD-SOI, the threshold voltage of a FET varies with linear dependence on the applied back gate bias V_{BS} (relative to the source). Given the body effect

coefficient of a process, γ, V_{TH} is:

$$V_{TH} = V_{t0} - \gamma V_{BS} \tag{133}$$

Using this in the ring oscillator frequency equation:

$$f_{osc} = \frac{\mu_n C_{ox}}{4 \ln 2 NC} \left(\frac{W}{L}\right)_n \left[V_{DD}\left(\frac{7}{8\ln 2} - 1\right) - V_{t0}\left(\frac{1}{\ln 2} - 1\right) + \gamma V_{BS}\left(\frac{1}{\ln 2} - 1\right)\right] \tag{134}$$

Equivalently, $f_{osc} = f_{0,osc} + \Delta f_{osc}(V_{BS})$, provided $f_{0,osc}$ is the frequency with no backgate bias. Thus it is found that:

$$\Delta f_{osc}(V_{BS}) = \gamma V_{BS} \frac{\mu_n C_{ox}}{4 \ln 2 NC} \left(\frac{W}{L}\right)_n \left[\frac{1}{\ln 2} - 1\right] = K_{VCO} \tag{135}$$

The important finding here is that the change in oscillator frequency is linear with backgate voltage, that is $\Delta f_{osc} \propto V_{BS}$. The expression of 135 also happens to to be the VCO gain, K_{VCO}. Given the wide voltage range that FD-SOI backgates may be biased to, this implies that a highly linear VCO with a wide input range may be implemented with backgate tuning. If the backgate voltage is constrained in the range [0, V_{DD}], the center frequency f_c of such a VCO is then:

$$f_c = \frac{\mu_n C_{ox}}{4 \ln 2 NC} \left(\frac{W}{L}\right)_n \left[V_{DD}\left(\frac{7}{8\ln 2} - 1 + \frac{\gamma}{2\ln 2} - \frac{\gamma}{2}\right) - V_{t0}\left(\frac{1}{\ln 2} - 1\right)\right] \tag{136}$$

Correspondingly, the tuning range with $V_{BS} \in [0, V_{DD}]$ is:

$$\Delta f = \gamma V_{DD} \frac{\mu_n C_{ox}}{4 \ln 2 NC} \left(\frac{W}{L}\right)_n \left[\frac{1}{\ln 2} - 1\right] \tag{137}$$

Finally, the fractional tuning range of the oscillator is found to be that of equation 138. Notice that this is only a function of supply voltage V_{DD}, nominal threshold voltage V_{t0} and body effect coefficient γ.

$$\frac{\Delta f}{f_c} = \frac{\gamma V_{DD}(1 - \ln 2)}{V_{DD}\left(\frac{7}{8} - \ln 2 + \frac{\gamma}{2} - \frac{\gamma}{2}\ln 2\right) - V_{t0}(1 - \ln 2)} \tag{138}$$

If a N-bit DAC is used to control the oscillator, the resulting DCO gain is therefore:

$$K_{DCO} = \frac{\Delta f}{2^{N_{DAC}}} = \frac{f_c}{2^{N_{DAC}}} \cdot \frac{\gamma V_{DD}(1 - \ln 2)}{V_{DD}\left(\frac{7}{8} - \ln 2 + \frac{\gamma}{2} - \frac{\gamma}{2}\ln 2\right) - V_{t0}(1 - \ln 2)} \tag{139}$$

7.3.4 Backgate-controlled Ring Oscillator Sensitivity Analysis

The frequency tuning sensitivity of the ring oscillator for supply and backgate voltages will be compared. First the following is defined, seeing that the derived equations for oscillator

frequency versus backgate bias and supply voltage are linear.

$$f_{osc}(V_{DD} + \Delta V_{DD}) = f_{osc}(V_{DD}) + f_{osc}(\Delta V_{DD}) \tag{140}$$

$$f_{osc}(V_{DD}) = f_0 \tag{141}$$

$$f_{osc}(\Delta V_{DD}) = \Delta f \tag{142}$$

In the case of supply voltage tuning, the change as a proportion of nominal frequency per voltage of applied extra bias is (evaluated at zero back-gate bias):

$$S_{V_{DD}}^{f_{osc}} = \frac{\Delta f}{f_0} \cdot \frac{1}{\Delta V_{DD}} = \frac{\left(\frac{7}{8\ln 2} - 1\right)}{V_{DD}\left(\frac{7}{8\ln 2} - 1\right) - V_{t0}\left(\frac{1}{\ln 2} - 1\right)} \tag{143}$$

With V_{DD} = 0.8, V_{t0} = 0.3 (approximately true for the FD-SOI devices of this work), it is expected 340% change in frequency will result per extra volt of applied bias. Of course, this is linearized, and one does not expect to apply an extra 1V of supply bias to a 0.8V oscillator. Realistically, the supply can be tuned $\pm$ 10%, which corresponds to a $\pm$27.2% tuning range of the oscillator. Supply tuning stands as a viable coarse tuning mechanism for the oscillator, however, fine tuning is more limited due to difficulty in achieving a small resolution step. For example, 10 bits within V_{DD} = 0.8V $\pm$10% in this work corresponds to 156 μV/LSB, and 26 m%/LSB of frequency tuning.

In the case of backgate tuning, the change in proportion of frequency per volt of applied back-gate bias is:

$$S_{V_{BG}}^{f_{osc}} = \frac{\Delta f}{f_0} \cdot \frac{1}{\Delta V_{BG}} = \frac{\gamma\left(\frac{1}{\ln 2} - 1\right)}{V_{DD}\left(\frac{7}{8\ln 2} - 1\right) - V_{t0}\left(\frac{1}{\ln 2} - 1\right)} \tag{144}$$

With γ = 0.07, V_{DD} = 0.8, V_{t0} = 0.3, as is typical in the FD-SOI process in this work, it is expected a 29.5% change in frequency will result per volt applied of backgate bias. This is much finer than achieved with supply voltage tuning. The ratio of frequency sensitivity to supply and backgate voltage tuning is:

$$\frac{S_{V_{DD}}^{f_{osc}}}{S_{V_{BG}}^{f_{osc}}} = \frac{\frac{7}{8\ln 2} - 1}{\gamma\left(\frac{1}{\ln 2} - 1\right)} \tag{145}$$

Under the aforementioned biasing conditions, it is expected that 8.4x finer control can be achieved with backgate tuning per unit of applied bias. The wide backgate voltage range allowed for with FD-SOI technology furthermore permits for design of a voltage-DAC based control scheme which will achieve far smaller frequency resolution than with supply voltage tuning. Therefore, motivated by these findings, the pursuit of a backgate tuned ring oscillator has been undertaken in this work.

7.4 Pseudodifferential Backgate-Coupled Inverter Delay Cell

To utilize backgate tuning for frequency control, a suitable delay cell design must be devised. Accordingly, the delay topology used in this work has been derived from the FD-SOI pseudodifferential backgate coupled inverter delay cell of [31], whose construction is shown in figure 35. This inverter uses two single ended FD-SOI inverters, with the backgates of the transistors in a given inverter connected together. This is implemented with a common well structure below the two transistors of each inverter. Nominally, to avoid forward biasing of the well-substrate diodes, a N-doped well (or a triple well) is used, with well potentials constrained to be ≥ 0. The result of this well configuration and the FD-SOI BOX layer is that the backgate terminals of the PMOS and NMOS may be tuned in tandem across a wide positive voltage range. This is not possible in bulk technology. In the FD-SOI process used in this work, such well configurations allow biasing from 0 to +2V, which is inclusive of the full rail-to-rail range of a circuit supplied with V_{DD} = 0.8V, as in this work. Thus, in figure 35, when the two FD-SOI sub-cells inverter cells connected with the shown cross-coupled output and backgate configuration, safe well biasing is achieved. The backgate cross-coupled configuration has the effect of inducing differential behavior in the circuit, as positive feedback is introduced. It should be noted that the cell of figure 35 does not employ backgate-based tuning to tune cell delay. This work proposes a modification to the topology which implements both backgate differential coupling and backgate frequency (delay) tuning.

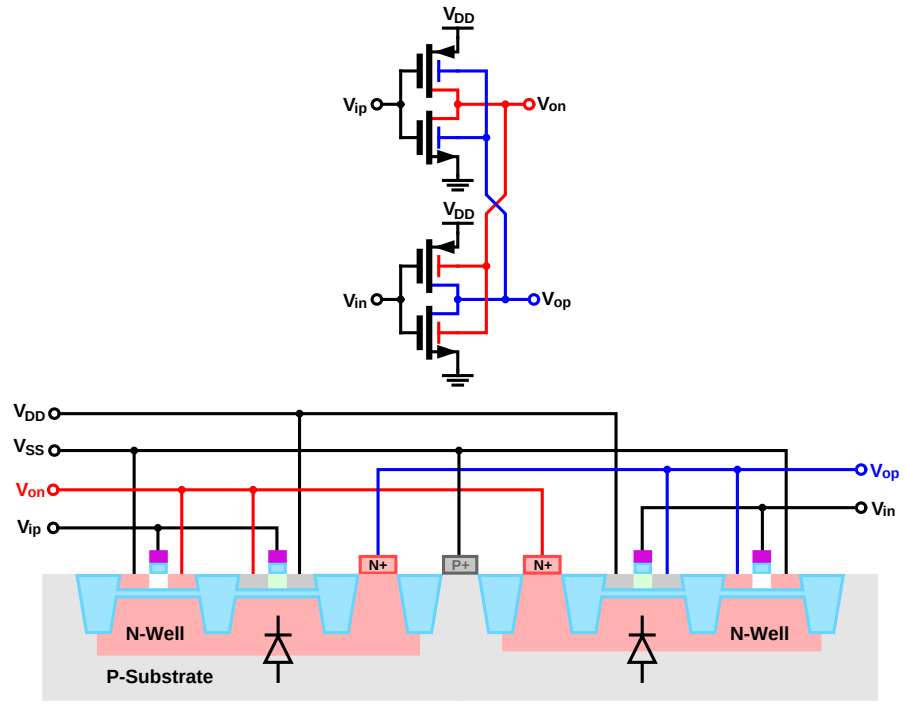


Figure 35: FD-SOI backgate-coupled inverter topology.

The emergence of differential behavior in this delay cell can be understood through circuit analysis. First, the common backgate inverter cell (figure 36a) is converted to a linearized

model, for an arbitrary bias point, in figure 36b. A simplification of the linearized model is arrived at by lumping terms together, giving figure 36c. Using the linearized model of figure 36c, a linearized version of the pseudodifferential inverter circuit is then arrived at in figures 37a and 37b. It is observed that the backgate transconductors (labeled as $-G_{mb}$) in figure 37b couple the two outputs with a positive feedback loop. Therefore, any differential components generated via the feed forward terms $-G_m R_o v_{in}$ and $-G_m R_o v_{ip}$ will be positively amplified by the cross coupling. Elementary circuit analysis for differential gain of the linear circuit in figure 37b leads to the expression in equation 146.

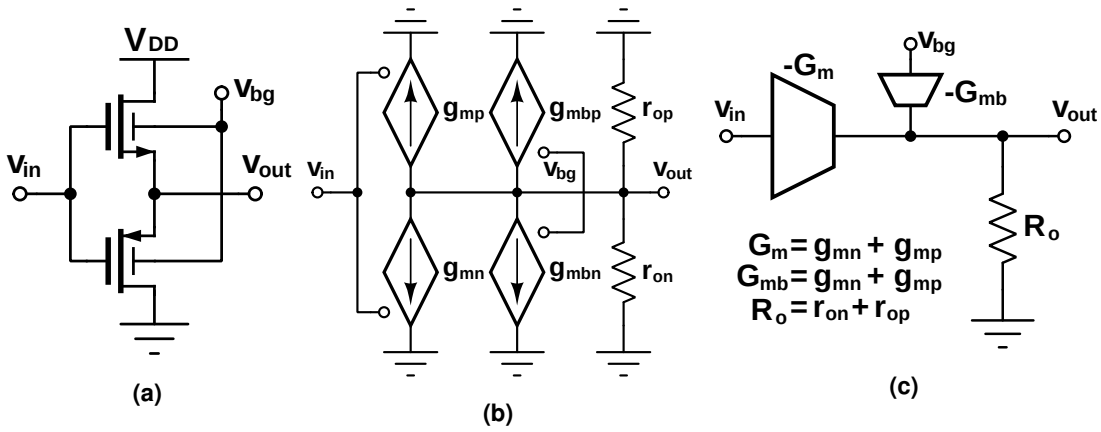


Figure 36: (a) Common backgate inverter, **(b)** Linearized circuit, **(c)** Simplified linearized model.

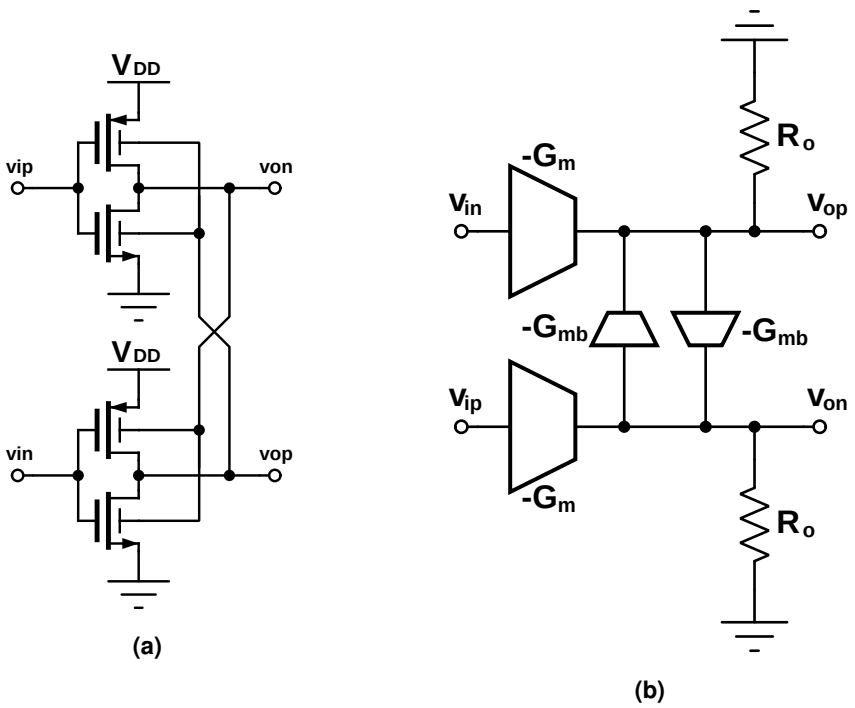


Figure 37: (a) Pseudodifferential backgate-coupled inverter circuit, **(b)** Linearized circuit.

$$A_{DM} = \frac{G_m R_o + G_{mb}^2 R_o^2}{1 - G_{mb}^2 R_o^2} \tag{146}$$

Using the relation $G_{mb} = \gamma G_m$ found in equation 12, equation 146 can be simplified to equa-

tion 147 (this is assuming PMOS and NMOS have approximately equal γ). In the special case where $\gamma G_m R_o \approx 1$, the differential gain of the delay cell can be very high, implying the pseudodifferential backgate coupling can be very effective at inducing differential behavior. A major advantage of this topology is that it is implemented using only two inverters, unlike typical differential pair circuits which rely on current biasing to achieve differential behavior. The removal of the need for current biasing reduces power consumption, as no reference current generation is required. Circuit noise is also reduced due to fewer total transistors generating noise in the circuit.

$$A_{DM} = \frac{G_m R_o}{1 - \gamma G_m R_o} \tag{147}$$

For the sake of completeness, the common mode gain of the circuit has also been determined through circuit analysis, given in equation 148.

$$A_{CM} = \frac{G_m R_o}{1 + \gamma G_m R_o} \tag{148}$$

7.4.1 Tunable Frequency Backgate-Coupled Pseudodifferential Delay Cell

To implement the backgate-coupled pseudo-differential inverter delay cell topology with backgate tuning, two candidate topologies have been devised. The first is the parallel configured topology of figure 38a, and the second is a telescopic configuration, shown in figure 38b. Tuning of the delay cells is done in accordance with figure 39, where the backgate voltages *vbgp* and *vbgn* change in a complementary fashion. Tuning for increased frequency results in greater $|V_{BS}|$ biasing for both PMOS and NMOS, such that the threshold voltage in both devices decreases, modulating the channel conductances to be higher and accordingly increasing frequency. These cells were devised with a priority to maintain overall symmetry, specifically in regards to rise and fall time behavior. Hajimiri's highly cited paper [32] on the effect of impulse injection on oscillator edges finds that it is favorable for an oscillator to have as symmetric rise and fall time in terms of phase noise. Specifically, it was found that higher symmetry of waveform in terms of rise and fall behavior results in a lower corner frequency for flicker noise, thus improving low frequency phase noise components of an oscillator.

The parallel configured topology employs a backgate-coupled pseudo-differential inverter in parallel with a second set of inverters, which the backgate voltages are set externally to control the oscillator frequency. The delay cell operates through superposition position of current, by connecting the inverters in parallel, their individual effects are combined to result in both frequency tuning and differential operation. The frequency gain of this delay cell is controlled by setting a ratio of the device widths utilized in the cross-coupled inverter to the widths of the frequency tuning inverters. If this ratio is defined as R = W_{1x}/W_{3x} = W_{2x}/W_{4x}, the VCO gain is defined in equation 149. In a simulation case with the 22nm FD-SOI technology of this work using LVTNMOS + RVTPMOS devices, a nominal (W/L) = 200nm/150 nm for all

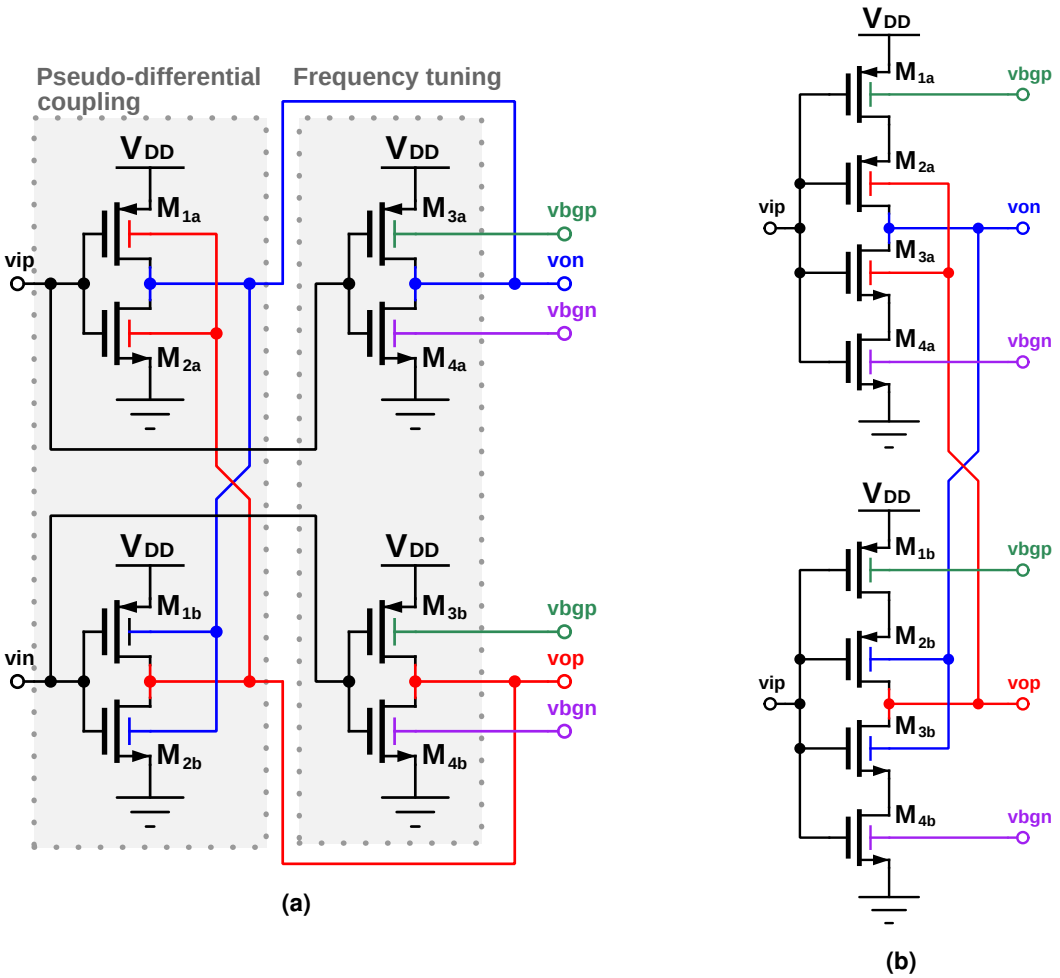


Figure 38: Backgate tunable backgate-coupled pseudodifferential delay cell in **(a)** Parallel, and **(b)** Telescopic implementations.

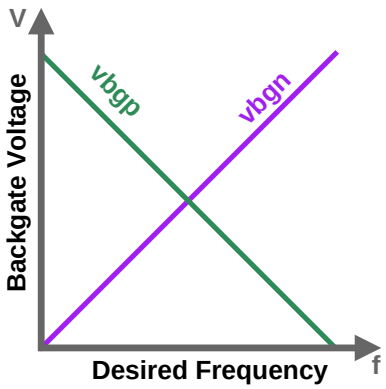


Figure 39: Complementary tuning of backgate voltages to achieve frequency tuning.

devices, V_{DD} = 0.8, and R = 1, a fractional tuning range of 14.9% was observed in the ring oscillator. Changing R = 2 results in 10.7% fractional tuning range. These are consistent with the predicted equation, and suggest a maximum fractional tuning range of 29.8%-32.1% for this backgate controlled oscillator (where R = 0). Based on the theoretical oscillator fractional frequency tuning range in equation 138, and the extracted body effect coefficient parameters

given in appendix C for the 22nm FD-SOI process, where $\gamma \approx 0.075$ and $V_{t0} \approx 0.3$, it is found that theoretically the maximum tuning range should be 29.4%, which agrees closely with the simulation results. This suggests validity of the developed oscillator theory.

$$K'_{VCO,parallel} = \frac{K_{VCO}}{R+1} \tag{149}$$

The telescopic topology is comprised of two sub-inverters each with a telescopic stack of four transistors. The header and footer transistor backgates are connected to external control voltages to adjust the frequency. Modulating the control voltages will modulate the conductance of the header and footer devices, resulting in a current-starving like behavior that tunes the oscillator frequency. The inner pair of transistors in each sub-inverter are configured with a common backgate, which are cross-coupled with the output of the other respective sub-inverter, to induce differential operation in the same manner as the basic backgate-coupled pseudo-differential inverter delay cell. Frequency gain of the cell is controlled via setting the ratio of the inner transistors to the header and footer transistors. Due to the telescopic arrangement, a simple argument of current superposition as in the parallel case can not be made. Also, the model assumptions made in the backgate-controlled oscillator theory of section 7.3 are not necessarily valid, as the FET operating regime of the telescopic devices cannot be guaranteed to be in saturation during the delay cell propagation period. Rather than a full circuit analysis of this topology, an approximate result backed by simulated observations has been devised. If a ratio R is defined as R = W_{1x}/W_{2x} = W_{4x}/W_{3x}, it was determined via simulation that the oscillator frequency gain is reduced by 1/R for R near unity. Combining the two aforementioned observations results in equation 150. In a simulation case with FD-SOI technology where LVTNMOS + RVTPMOS devices, a nominal (W/L) = 400nm/150 nm for all devices, and R = 1, a fractional tuning range of 10% was observed in the ring oscillator. Changing R = 2 resulted in a 4.8% fractional tuning range.

$$K'_{VCO,telescopic} = \frac{K_{VCO}}{R} \tag{150}$$

These two topologies present different trade offs between frequency and achievable power. Inspecting equation 132, it is seen that oscillator power consumption is proportional to device (W/L) used in the delay cells. For low power, low effective (W/L) is desirable. In the case of the parallel delay stage, an effective $(W/L)'_{parallel}$ is arrived at by adding the (W/L)'s of devices within the cross-coupled and frequency tuning sub-inverters, yielding $(W/L)'_{parallel}$ = (1+R)(W/L). This assumes equal NMOS and PMOS devices. In the telescopical case, assuming R = 1, it is observed that to two FETs with size (W/L) cascaded have an effective $(W/L)'_{tele}$ = 0.5(W/L). It is expected that minimum power attainable is achieved by utilizing the smallest available devices size in a technology, that is (W_{min}/L_{min}), with R = 1. Comparing the tele-

scopic and parallel cases, it is seen that $(W/L)'_{parallel}/(W/L)'_{tele} = 4$, implying that the power consumption of the parallel stage can be presumed to be four times that of the telescopic design with equal device sizes. In the case of this work, scaling of power is very important, and it has been found that the parallel topology was unable to achieve small enough K_{VCO} needed in this work with satisfactory power consumption. This is due to the need to increase R to reduce $K'_{VCO,parallel}$, which correspondingly increases power due to greater effective inverter width. Thus, a telescopic topology has been pursued in this work.

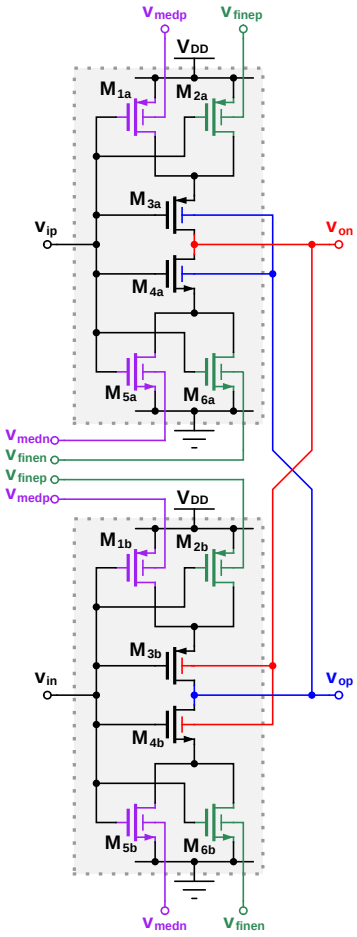


Figure 40: Pseudo-differential backgate-coupled inverter delay cell with fine and medium backgate-based tuning.

The final delay cell inverter topology employed in this work is shown in figure 40, which is the previous telescopic topology with a modification to enable simultaneous fine and coarse tuning ranges. This modification is achieved with the addition of a second transistor to each the header and footer of the telescopic stage. Transistors M_{1x} and M_{5x} implement medium granularity tuning, and transistors M_{2x} and M_{6x} implement fine granularity tuning. Defining R = $W_{1x}/W_{2x} = W_{5x}/W_{6x} > 1$, tuning the parameter R can be utilized to provide different tuning gains for the two ranges with respect to the applied backgate biases. This topology has been arrived at due to the finding that with the DACs implemented in this work, it was not possible to simultaneously achieve a wide tuning range with satisfactorily small K_{DCO} resolution with a single set of backgates. For sizing of devices, it is recommended to select a channel length

based on the findings for FOM$_{jitter}$ versus channel length in section 7.2, picking the longest channel length possible. Then, the width of all devices (set equal) should be varied until the target power is achieved. Finally, the header and footer device widths should be varied until satisfactory K_{VCO} values are found for the delay cell topology. Achieving design goals with this topology may require several iterations with layout.

7.5 Oscillator Implementation

7.5.1 Number of Ring Oscillator Stages

In the process of simulating the proposed delay cell in the 22nm FD-SOI technology, it has been determined that a two stage differential ring oscillator, generating in-phase and quadrature phase signals, will not oscillate. With a delay stage propagation time of t_{pd}, the cycle period is $1/f_{osc} = 2Nt_{pd}$, where in this case the number of stages N = 2. Every node is expected to switch two times per cycle, therefore it is determined that the switching period of a given node is equal to $2t_{pd}$. Previously, it has been determined that the propagation delay for the RC dominated ring oscillator is $\ln(2)\tau$, resulting in a switching period of $2\ln(2)\tau$. If the oscillator swings from 0 to V_{DD} with exponential dependence, in a time period of $2\ln(2)\tau$, a change of $0.75V_{DD}$ is expected at the oscillator nodes. This implies that a two stage ring oscillator will not fully saturate to the rails, and therefore results in an extinction of oscillation as seen via simulation. Originally, it was planned to implement a two-stage quadrature VCO at 2.448 GHz, however due to the infeasibility of this, alternative configurations were attempted. First was a 4-stage oscillator at 2.448 GHz, however, it was seen that it was not possible to achieve the desired power and phase noise requirements with the proposed telescopic backgate-coupled delay cell in the 22nm FD-SOI process used. Thus, another alternative, being a subharmonic oscillator operating at 1/3 of 2.448 GHz was considered. This was implemented as a 6-stage differential ring oscillator, as shown in figure 41, which oscillates at 816 MHz. With 6 differential stages, 12 oscillator phases are created, and it is possible to derive a quadrature 2.448 GHz sampling clock by combining with digital logic the different 816 MHz oscillator phases, as shown in figure 42. With this topology, it was found to be feasible to implement a 816 MHz, 6-stage oscillator in 22nm FD-SOI that meets power and phase noise requirements defined for the design.

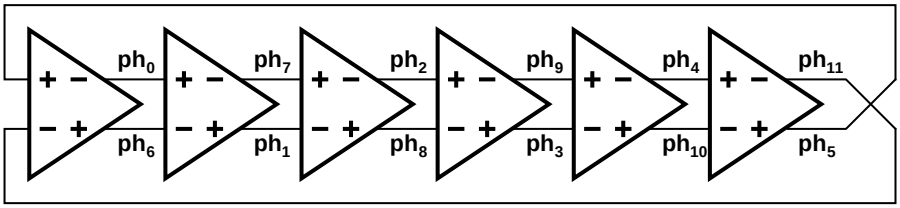


Figure 41: Basic differential ring oscillator circuit.

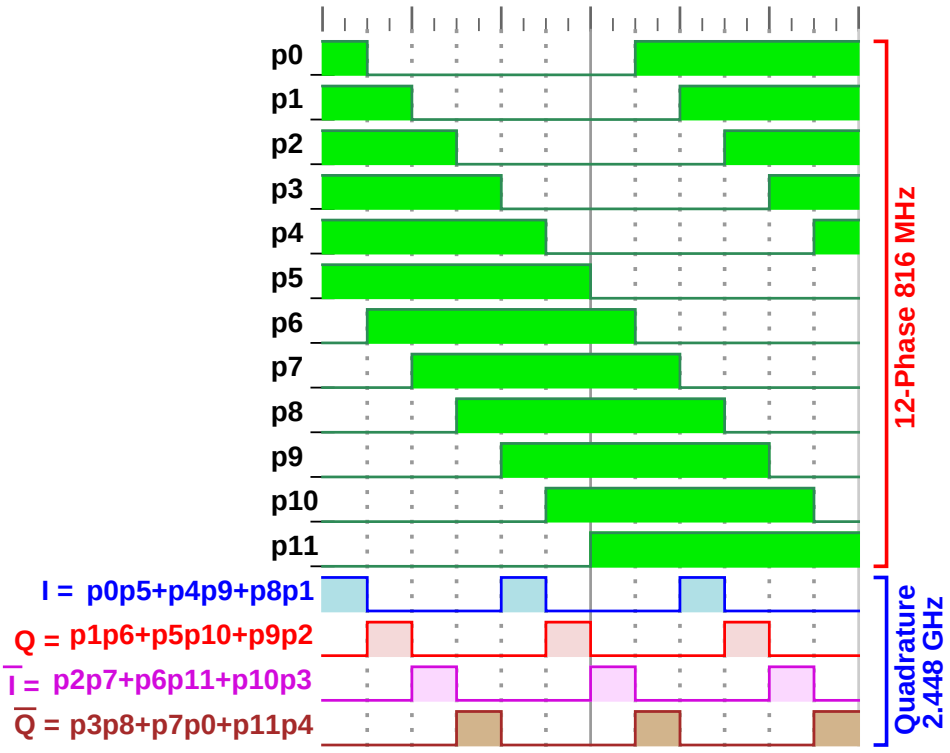


Figure 42: Third subharmonic to quadrature full rate conversion.

7.5.2 Final Oscillator Circuit

With a selection of the inverter topology and number of delay cells, the final oscillator circuit topology is described here. The oscillator is comprised of six basic delay cell elements shown in figure 43, which contain (1) a backgate-coupled and tunable pseudodifferential inverter, (2) reset switches, and (3), an output buffer. A simplified symbol for the delay cell is shown in figure 44a, and the placement of the delay cells into a full ring oscillator is shown in figure 45. This delay cell was devised from the base inverter topology in order to fulfill several goals. The first goal is to be able to reset the oscillator to a known phase at start up, which is implemented via addition of switches at the output nodes which force the nodes to rail levels when a reset condition is asserted. This is such that when reset is de-asserted in tandem with a clock edge for the PLL, the initial edge of the oscillator sampled by a phase detector will be in sync with the clock, as shown in figure 44b. The second goal is to remove any effect of external noise and loading on the oscillator, for which a buffer has been added to each delay cell, that the external world connects to. This is discussed in section 7.10. Table 4 contains the devices sizes used to implement the delay cell of figure 43. The devices types selected for implementation are low voltage threshold NMOS (LVTNMOS) and regular voltage threshold PMOS (RVTPMOS) in the 22nm FD-SOI process. These are selected based on the discourse in appendices C and D, which show these devices are well matched in terms of body coefficient and allow for near unity ratio of W_P/W_N for a $V_{DD}/2$ output crossing level.

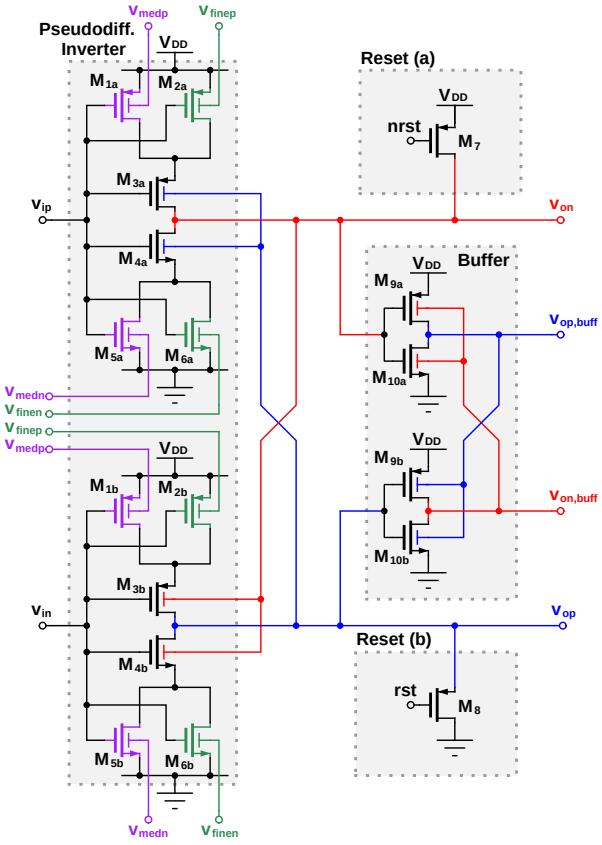


Figure 43: Ring oscillator delay cell full circuit.

Device	(W/L)
M_{1x}, M_{5x}	800n/40n
M_{2x}, M_{6x}	100n/40n
M_{3x}, M_{4x}	400n/40n
M_{7x}, M_{8x}	200n/20n
$M_{9,1}$, ..., $M_{9,n}$	100n/20n
M_{10x}, M_{11x}	200n/20n
C_L	200 aF

Table 4: Delay Stage Device Sizes.

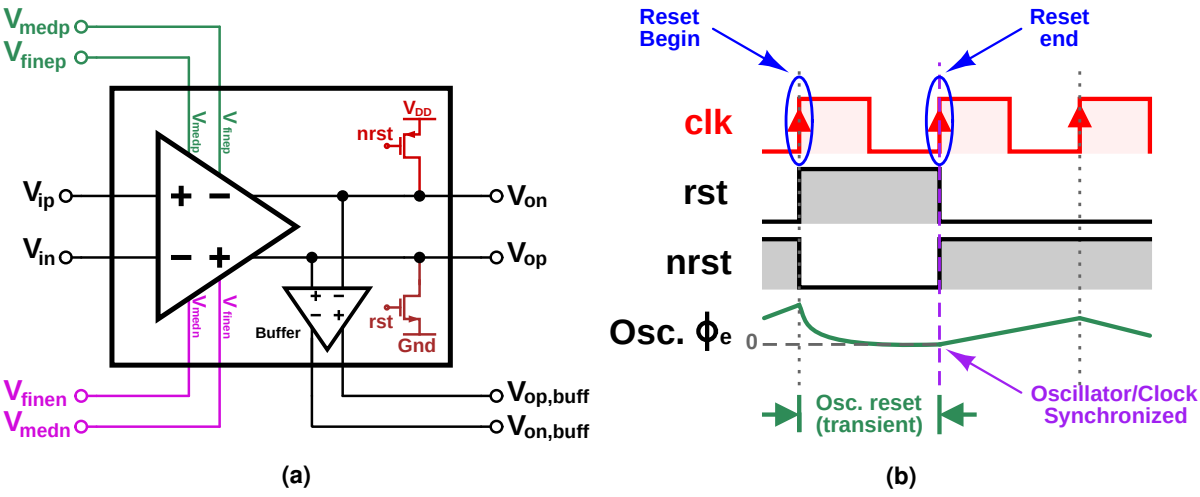


Figure 44: (a) Ring oscillator delay cell symbol, **(b)** Oscillator synchronous reset scheme.

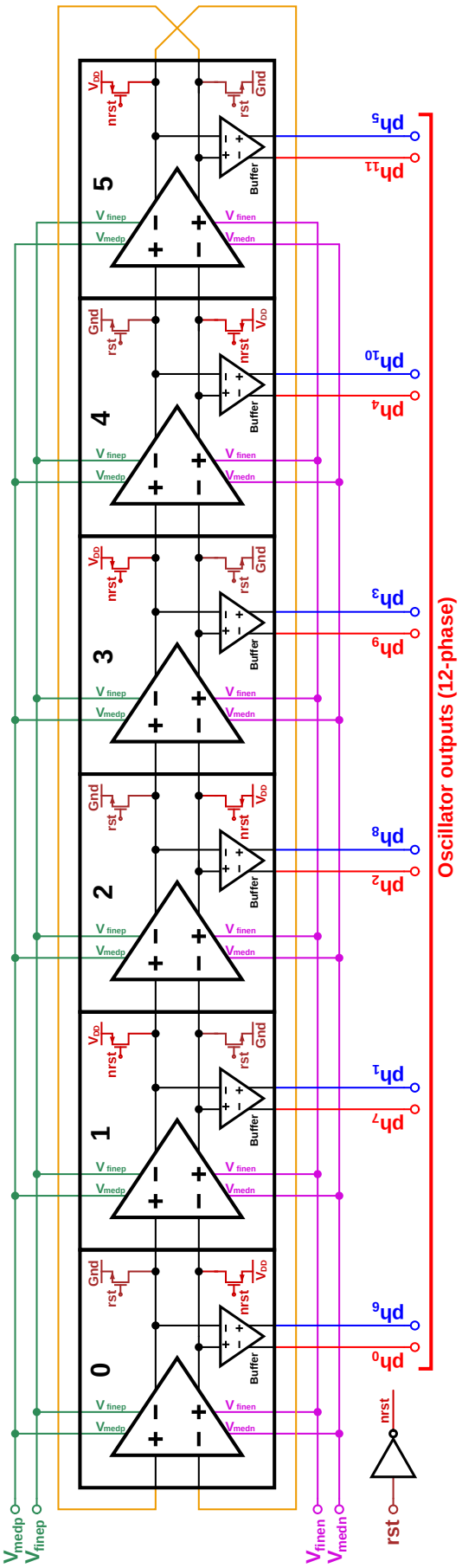


Figure 45: Ring oscillator full schematic.

7.5.3 Layout

In order to implement a compact oscillator core, the delay cells were laid out as slices, for which several slices are abutted together to make a full ring oscillator. This is similar to the approach of utilizing bit slices in a processor to implement a many bit architecture. The unit delay cell slice is shown in figure 46, where there pseudodifferential inverter, reset switch, and output buffer are placed in a row, 3.5 μm tall by 7.6 μm wide. Supply voltages, the fine and medium control voltages, and reset signals run vertically from top to bottom edge, to allow for abutment of delay cells to form the complete ring oscillator. The full oscillator layout is shown in figure 47 (rotated 90 degrees), where the delay cells are placed out of order (4,3,5,2,6,1) to assist in making wire lengths between all cells approximately the same. An in-order sequence (1,2,3,4,5,6) would result is short connections between all cells, except for between cells 1 and 6, which would result in excessive loading on stage 6 versus the other stages.

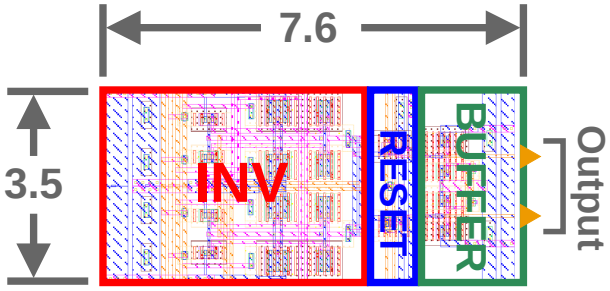


Figure 46: Delay cell slice layout (in microns).

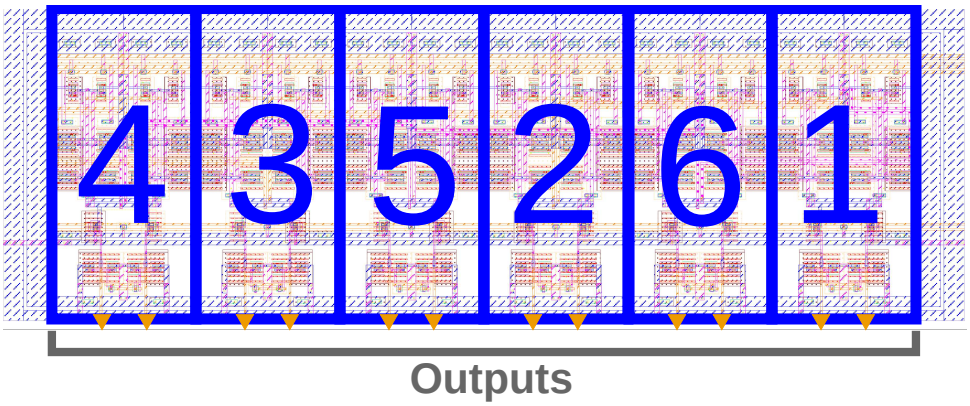


Figure 47: Delay cell arrangement in layout to result in similar wire lengths between stages.

Regarding the layout of of the pseudo-differential inverter delay cell, careful attention was paid to ensuring that the wells forming the backgates were successfully isolated. Figure 48 demonstrates the layout of the delay cell, with the implemented wells and devices annotated, corresponding to the circuit of figure 40. All backgate wells were made to be N-doped, allowing for the wells to be positively biased, when the substrate is tied to ground. This is because the substrate is P-type, and with the N-doped wells positively biased, the well-substrate parasitic diodes become reverse biased, resulting in isolation. In accordance to the process design rules for the 22nm FD-SOI technology used, all wells on electrically different nets were separated by

at least 250nm, ensure that these nets remain isolated from each other with process variation.

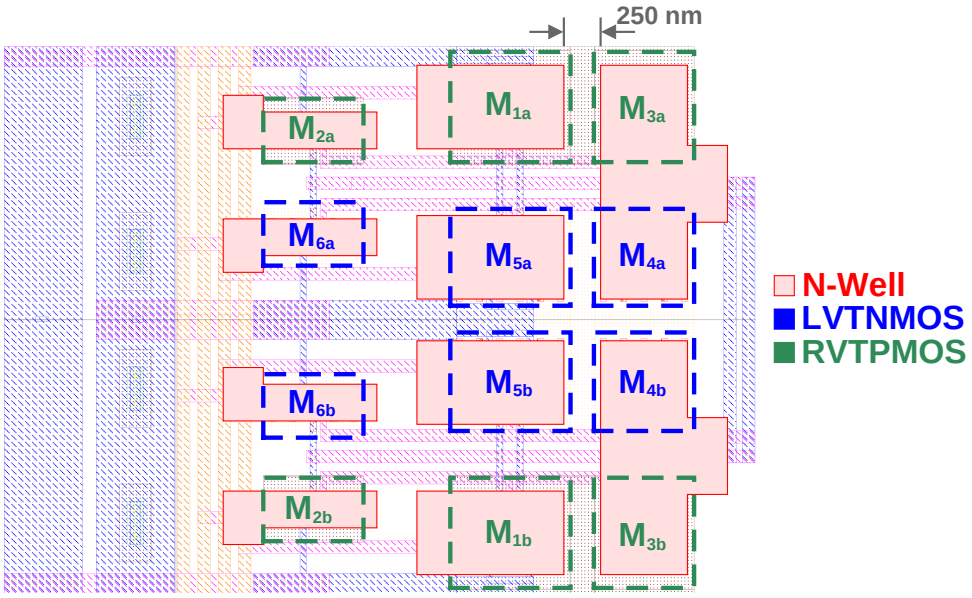


Figure 48: Well arrangement of pseudo-differential backgate-coupled inverter delay cell, non-well areas are P-doped substrate.

Simulation results pertaining to the ring oscillator are found in results section 9.4, and the full set of layout images are in appendix B.2.

7.6 Digitizing the VCO

In order to implement a DCO, the VCO core designed in this work (see figure 45) must be connected to a set of digital to analog converters (DACs). The oscillator topology implemented requires complementary (differential) generation of backgate biasing voltages in order to tune frequency, as seen in figure 39. Differential generation is necessary in order to tune both delay cell NMOS and PMOS device threshold voltages simultaneously with the same effect. This is because in an inverter configuration, NMOS devices see reduction in V_{TH} with *increasing* backgate bias relative to ground, while PMOS devices see reduction in V_{TH} with *decreasing* backgate bias relative to ground, i.e. they are complementary. The oscillator core has two differential sets of tuning connections, one each for fine and medium tuning ranges, so accordingly two differential DACs must be used to digitize the VCO. The base DAC design implemented in this work is single ended, so the scheme demonstrated in figure 49a is applied with two single ended DACs to implement a differential DAC. The design of the individual DACs is described in the following sections, employing a capacitive DAC (CDAC) topology.

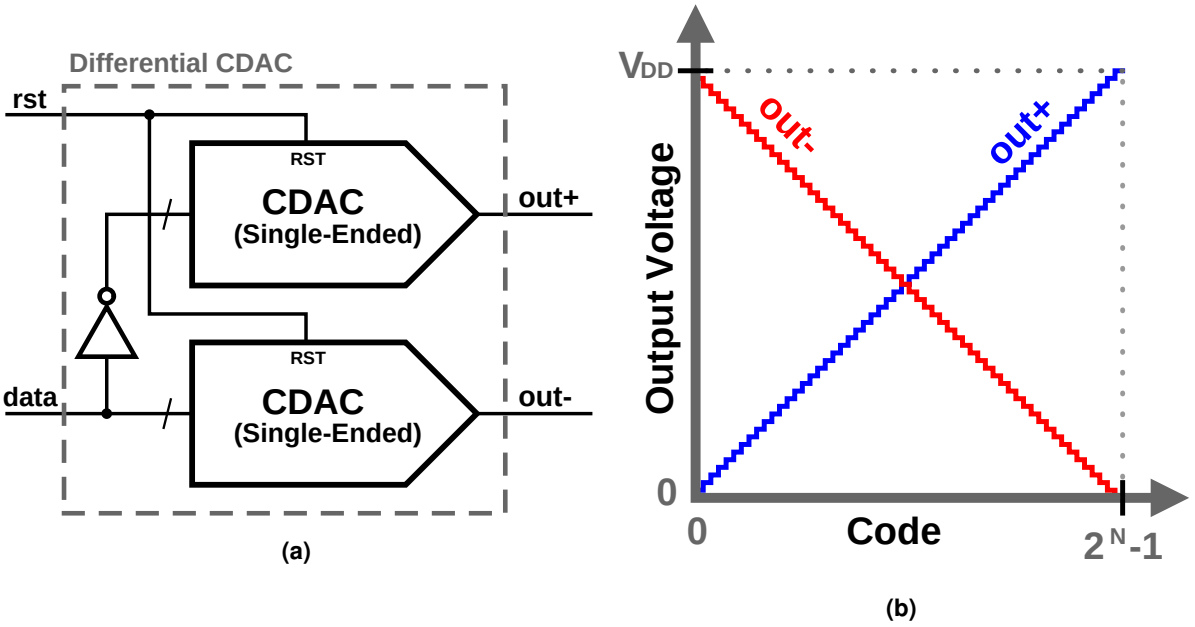


Figure 49: (a) Differential DAC implemented from two single ended CDACs, **(b)** Output voltages versus input code.

Using the differential DACs, the DCO is implemented as in figure 50a. A N_{med} bit differential CDAC is used for medium frequency tuning, and a N_{fine} bit differential CDAC is used for fine frequency tuning. Both tuning ranges are controlled by the same DCO control word, where the fine CDAC is connected to the lowest N_{fine} bits of the input (loop filter output), and the medium DAC is connected to the next N_{med} bits. Figure 50b illustrates the frequency tuning versus DCO control code characteristic, where it is expected there will be discontinuities observed for when the medium DAC output changes. With process, voltage and temperature variation, it

should not be expected that a perfectly linear DCO code-frequency trend exists with the divided medium and fine tuning range approach. Rather, it is safest to engineer the K_{VCO} of the tuning ranges and the DAC resolution such that all medium settings result in overlapping frequency ranges with the adjacent medium tuning codes, so that there are no gaps in frequency. Ideally, the overlap Δf_{OL} should much be larger than the expected RMS variation of the loop filter output while the PLL is in steady state. This ensures that a stable position for all frequencies in the tuning range exists, such that the PLL may stay locked in steady state without significant probability of the DCO code from hitting a discontinuity (possibly resulting in loss of lock).

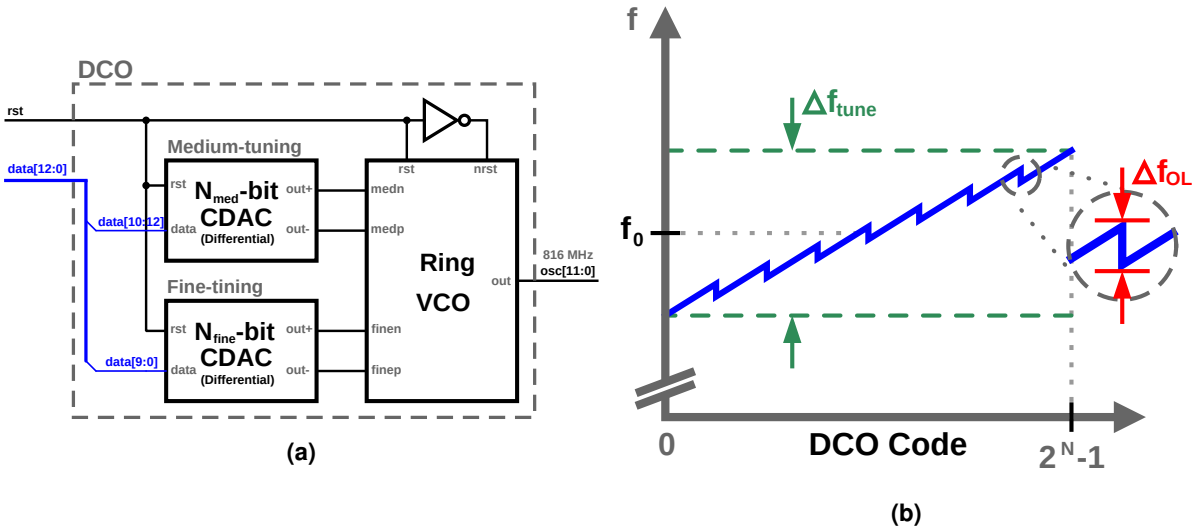


Figure 50: (a) DCO implementation from ring VCO and differential CDACs, **(b)** Resulting DCO frequency versus input code.

The RMS variation of the loop filter output may be calculated, using the filter coefficient results for the optimized BBPD-PLL PI-controller from section 6.5.1. It is observed that the optimal filter coefficients in equations 114 and 116 hold the proportionality in equation 151. It is also noted the PI-controller output with the BBPD may only increment by $\pm|b_0 - b_1|$, or $\pm|b_0 + b_1|$, accordingly the proportionality in equation 152 also holds. Thus if the magnitude by which the loop filter changes is constrained in proportion $\sqrt{S_{0_{osc}} f_{ref}}/K_{DCO}$, it is expected that the overall spread determined by RMS variation $\sigma_{u_{LF,SS}}$ of the loop filter output will hold the same proportionality. Analytically, it is hard to predict a BBPD output sequence and resulting distribution of the loop filter output in steady state due to emergent PLL behaviors, so a behavioral simulation utilizing optimized loop filter coefficients was run find to a factor of proportionality ξ for equation 153. It was found $\xi = 0.803$. Figure 51 demonstrates the relationship of equation 153 observed in the simulated loop filter output.

$$|b_0| \propto |b_1| \propto \frac{\sqrt{S_{0_{osc}} f_{ref}}}{K_{DCO}} \tag{151}$$

$$|b_0 - b1| \propto |b_0 - b_1| \frac{\sqrt{S_{0_{osc}} f_{ref}}}{K_{DCO}} \tag{152}$$

$$\sigma_{u_{LF,SS}} = \xi \frac{\sqrt{S_{0_{osc}} f_{ref}}}{K_{DCO,fine}} \tag{153}$$

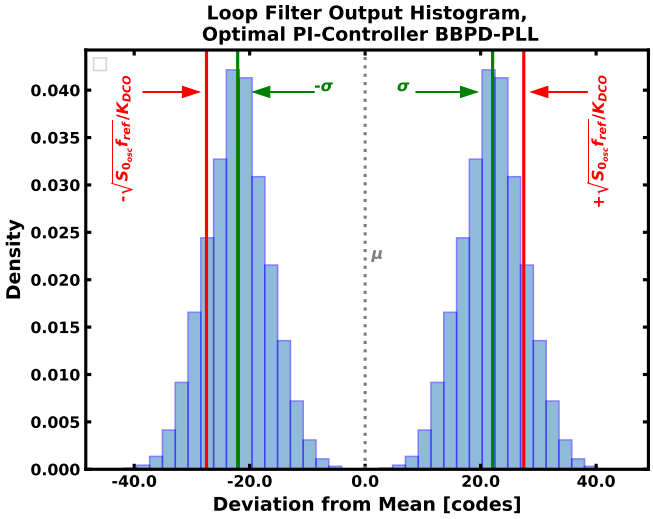


Figure 51: Loop filter output histogram of deviation from mean value in steady state.

The overlap between frequency ranges of adjacent medium tuning settings is given in equation 154, with DCO gains $K_{DCO,fine}$ for the fine range and $K_{DCO,med}$ for the medium range. Normalizing by $K_{DCO,fine}$ results in equation 155, giving the overlap in terms of fine DAC codes $\Delta u_{OL,fine}$. Noting the relationship of K_{VCO} and K_{DCO} takes the form in equation 156, the result in equation 157 is obtained. In order to constrain the overlap of the medium ranges to be much larger than the RMS variation $\sigma_{u_{LF,SS}}$ of the loop filter output, a constraint of $\Delta u_{OL,fine} > 6\sigma_{u_{LF,SS}}$ is used, yielding the expression in equation 158 for minimum number of medium bits. The overlap of $6\sigma_{u_{LF,SS}}$ allows for a guaranteed point of steady state operation for all frequencies within the DCO range with at least $\pm 3\sigma$ of separation from discontinuities.

$$\Delta f_{OL} = 2^{N_{fine}} K_{DCO,fine} - K_{DCO,med} \tag{154}$$

$$\Delta u_{OL,fine} = \frac{\Delta f_{OL}}{K_{DCO,fine}} = 2^{N_{fine}} - \frac{K_{DCO,med}}{K_{DCO,fine}} \tag{155}$$

$$K_{DCO,fine} = \frac{V_{DD} K_{VCO,fine}}{2^{N_{fine}}}, \qquad K_{DCO,med} = \frac{V_{DD} K_{VCO,med}}{2^{N_{med}}} \tag{156}$$

$$\Delta u_{OL,fine} = 2^{N_{fine}} \left(1 - 2^{-N_{med}} \frac{K_{VCO,med}}{K_{VCO,fine}} \right) \tag{157}$$

$$N_{med} = \left\lceil -\log_2 \left[\frac{K_{VCO,fine}}{K_{VCO,med}} \left(1 - \frac{6\xi \sqrt{S_{0_{osc}} f_{ref}}}{K_{DCO,fine} 2^{N_{fine}}} \right) \right] \right\rceil \tag{158}$$

7.7 CDAC - Fine Range

The required DAC resolution for using the VCO as a DCO may be determined by constraining the smallest possible change of the output of the loop filter to be greater than unity. This constraint ensures that changes in the loop filter are always manifested as changes in the DAC output, and not quantized to zero. In 6.5.1, it was found that the possible increments for the loop filter are $(b_0 + b_1)$, $(b_0 - b_1)$, $(-b_0 + b_1)$, $(-b_0 - b_1)$. Evaluating these different possibilities, it is determined that the smallest magnitude occurs as $\pm|b_0 + b_1|$. Using equations 98, 99, and $|b_0 + b_1| \geq 1$ results in equation 159.

$$|b_0 + b_1| = \frac{\sqrt{K}}{2f_{ref}} \geq 1 \tag{159}$$

Applying this to the filter coefficients in the case of the bang-bang emergent phase noise optimized PLL (equations 114 and 116) results in the constraint for K_{DCO} in equations 160 and 161.

$$|b_0 + b_1| = \frac{\pi\alpha_{opt}^2\sqrt{74.79376 \cdot 2\pi S_{0_{osc}} f_{ref}}}{K_{DCO}(3+\sqrt{10})} = 0.07924138 \cdot \frac{\sqrt{S_{0_{osc}} f_{ref}}}{K_{DCO}} \geq 1 \tag{160}$$

$$K_{DCO} \leq 0.07924138 \cdot \sqrt{S_{0_{osc}} f_{ref}} \tag{161}$$

With a reference level of V_{DD}, a voltage gain of the ring oscillator of K_{VCO} [Hz/V], and N bits in the CDAC, the DCO gain K_{DCO} is given in equation 162.

$$K_{DCO} = \frac{V_{DD}K_{VCO}}{2^N} \tag{162}$$

Combining 161 and 162 result in an expression for minimum number of DAC bits (using rail-to-rail reference levels), given in equation 163.

$$N_{min} = \left\lceil \log_2 \left(\frac{V_{DD}K_{VCO}}{0.07924138\sqrt{S_{0_{osc}} f_{ref}}} \right) \right\rceil \tag{163}$$

Using the values $S_{0_{osc}} = \mathcal{L}(f) \cdot f^2$ = 1389 (derived from the implemented oscillator phase noise FOM value of -159 dB), K_{VCO} = 5.529 kHz/mV obtained from phase noise simulation of the oscillator, f_{ref} = 16 MHz, V_{DD} = 0.8, the resulting minimum number of bits is N_{min} = 9 bits. A 10 bit CDAC for fine tuning was implemented, given sufficient area was available for doing so. The extra bit of resolution will result in lower quantization noise added into the system by the DAC.

7.7.1 Circuit

The capacitive DAC was implemented using the circuit of figure 52, which is in effect a reconfigurable capacitive voltage divider. It was attempted to maximize the total capacitance for the 10 bit CDAC with an area constrained to roughly 50 μm x 15 μm (arrived at from the target PLL floor plan). MOM capacitors with 2.185 fF per unit capacitor C_0 were implemented, with the total DAC capacitance being 2.24 pF. All transistors were implemented with (W/L) = 200n/20n, with RVT devices. A DAC reset scheme was devised which shorts both sides of all capacitors to ground when asserted, resetting the capacitor charges. The simulation results for this CDAC are in the results section 9.5.1.

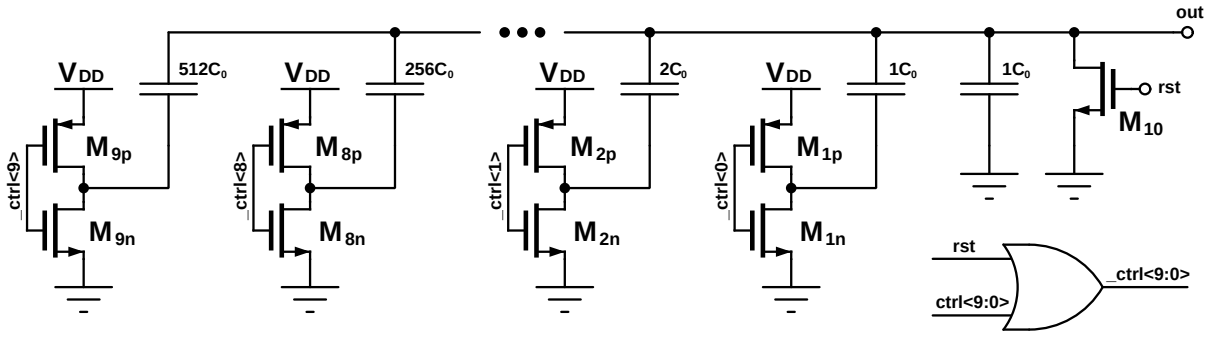


Figure 52: 10b CDAC.

7.7.2 Layout

The CDAC layout was performed similar to the CDAC in the successive-approximation ADC of [33], where the capacitors are metal-oxide-metal (MOM) capacitors formed using the metal layers of the process. A single unit capacitor, here 200 nm x 3 μm, occupying four metal layers, is repeated to form a bank of 64 capacitors, as in figure 53a. These capacitors have a common terminal, one free terminal, and a unit capacitance C. Seven bus wires running beneath the capacitor bank and are connected with vias to the capacitors as shown in figure 53a, such that parallel combinations of {1C, 1C, 2C, 4C, 8C, 16C, and 32C} are formed. To form the 10b CDAC, 16 of the 64-unit capacitor banks are combined as in figure 53b, with the necessary switches and routing. In total, 1024 unit capacitors are implemented in the full 10b CDAC design. The full set of layout images are in appendix B.3.

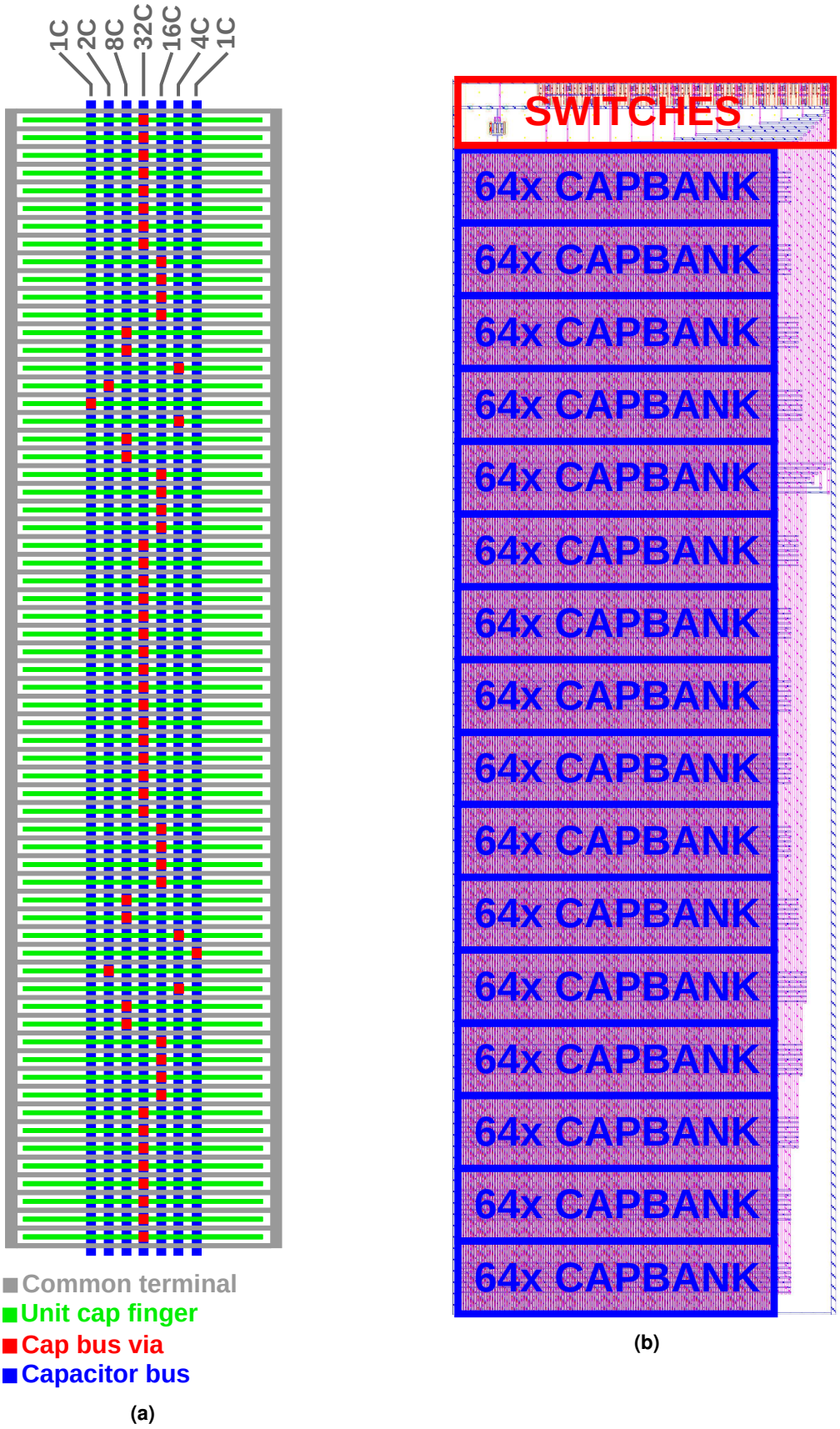


Figure 53: **(a)** 64 unit capacitor bank (rotated), **(b)** Full 10b CDAC layout using 16x 64 unit capacitor banks.

7.8 CDAC - Medium Range

Using the result of equation 158, the selection of a 10-bit fine CDAC, $K_{VCO,med}$ = 39.76 kHz/mV, and $K_{VCO,fine}$ = 5.529 kHz/mV, it is determined that at least 3 DAC bits are needed to provide satisfactory overlap of the DCO frequency ranges to be achieved through medium DAC tuning.

7.8.1 Circuit

The implemented circuit is in figure 54, being the same topology as the 10 bit CDAC. The unit capacitance C_0 here is 249 fF/capacitor, yielding 2 pF total capacitance. The size of the unit capacitor was selected to make the total capacitance near that of the 10b CDAC. The simulation results for this CDAC are in the results section 9.5.2, and the layout in appendix B.5.

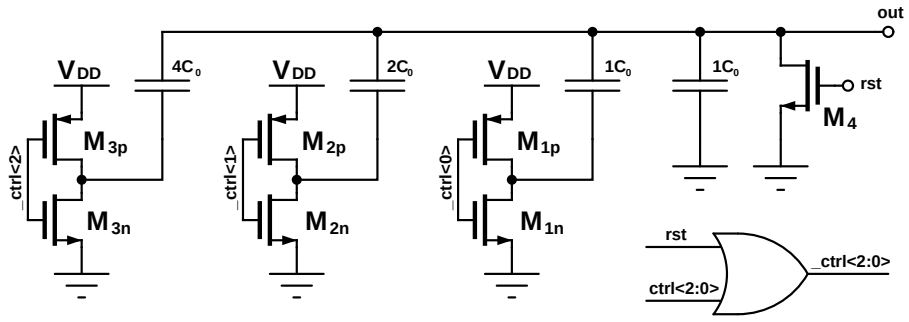


Figure 54: 3b CDAC.

7.9 Coordinated VCO and DAC Reset

When starting the PLL, the VCO and DACs must be reset to a predictable state for deterministic locking to occur with the BBPD. Importantly, the oscillator must begin from a zeroed phase state, aligned with a clock edge at its start. In this work, these resets are implemented in a synchronous manner, triggered by an external reset signal. The implemented reset sequence requires four reference cycles, and is illustrated in figure 55. The below description provides details on the individual steps of the reset sequence.

1. Assert VCO and DAC reset when external **rst** signal asserted.
2. De-asset DAC reset so DAC outputs can settle before starting the oscillator.
3. Start oscillator (synchronized with clock edge), wait one cycle before taking BBPD sample, do not update loop filter.
4. Take BBPD sample, do not update loop filter.

After the four reset cycles, the PLL enters normal operation where the BBPD is continually

sampled and the loop filter is continually updated. This reset scheme is implemented in the loop filter Verilog hardware description of appendix A.1, which has been hardened into digital logic in the physical PLL design.

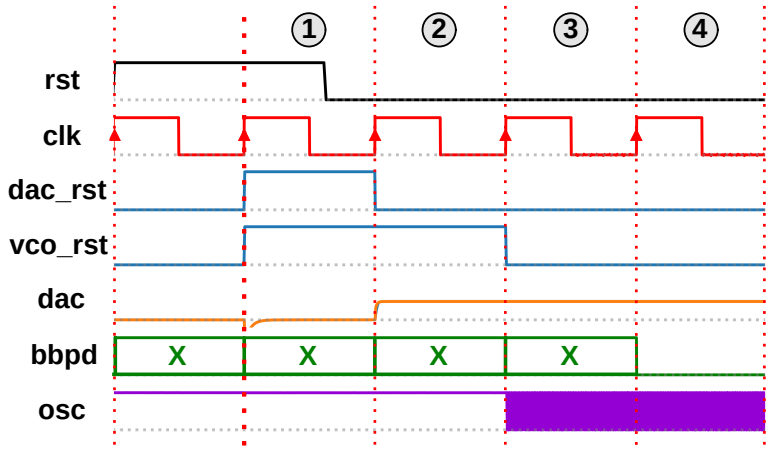


Figure 55: DCO reset scheme.

7.10 Output Buffer

Without a buffer, the frequency of the ring oscillator becomes external load dependent. Furthermore, as the output of the ring oscillator is rather slow in terms of edge time, this can result in issues with voltage-to-phase noise conversion. Thus, a buffered PLL output is beneficial to the PLL operation. Analyzing the voltage-to-phase noise conversion, the frequency of the oscillator is first defined as in equation 164 (from equation 123), where N is the stage count, t_{pd} is the stage propagation delay, and τ is the RC time constant of a stage.

$$f_{osc} = \frac{1}{2Nt_{pd}} = \frac{1}{2\ln(2)N\tau} \tag{164}$$

It is noted that 10-90% rise/fall time is equivalent to 2.2τ, given in equation 165. For a 6-stage oscillator, the rise/fall time is expected to be 26% of the oscillation period, which is rather slow.

$$t_{10-90} = 2.2\tau = \frac{2.2}{2\ln(2)Nf_{osc}} \tag{165}$$

With a supply voltage of V_{DD}, the transient waveform (single-ended) for a rising-edge transition of the oscillator is in equation 166.

$$V(t) = V_{DD}\left(1 - e^{-t/\tau}\right) \tag{166}$$

During a transition, noise will be most critical during the crossing of the common mode level V_{CM} , which acts as the switching point for the differential buffer. The buffer of this work is designed for the common mode level V_{CM} to be $V_{DD}/2$. Therefore it should be noted that $V(t) = V_{CM}$ at $t = \ln(2)\tau$. Evaluating the rate of change of the output at V_{CM} therefore results

in equation 167.

$$\left.\frac{dV}{dt}\right|_{V_{CM}} = \left.\frac{dV(t)}{dt}\right|_{t=\ln(2)\tau} = \frac{V_{DD}}{2\tau} \tag{167}$$

Noting that $\Phi = 2\pi f_{osc} t$, an expression that converts RMS voltage noise $\sigma_{V_{CM}}$ at V_{CM} to phase noise $\sigma_{\Phi_{CM}}$ is given in equation 168. This is based upon the linearized relation between phase noise (jitter) and voltage noise illustrated in figure 56.

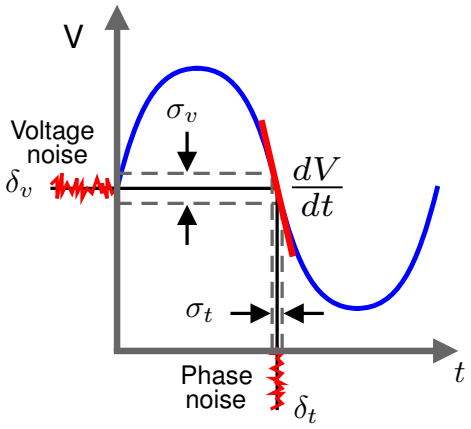


Figure 56: Voltage to phase noise conversion.

$$\sigma_{\Phi_{CM}} = 2\pi f_{osc} \left(\left.\frac{dV}{dt}\right|_{V_{CM}} \right)^{-1} \sigma_{V_{CM}} = \frac{2\pi}{V_{DD} \ln(2) N} \tag{168}$$

In the case of this work, where V_{DD} = 0.8V and N = 6 stages, 1 mV of RMS noise converts to 1.89 mrad RMS of phase noise. It is expected that supply noise can be a significant contributor to voltage noise seen on the internal oscillator nodes. To reduce supply coupling to phase noise, the pseudodifferential buffer circuit of figure 57 is implemented as it provides some advantages in terms of suppressing common mode noise present on the oscillator nodes. This circuit is identical to the backgate-coupled pseudodifferential inverter topology considered in section 7.4. Using the common mode gain A_{CM} in equation 148, and the differential mode gain A_{DM} for this circuit in equation 147, the common mode rejection ratio (CMRR) of this circuit can be defined as in equation 169. With proper selection of parameters, CMRR can be much greater than unity. Supply noise is expected to be manifested as a common mode component on the oscillator nodes (i.e. the input nodes of the differential buffer), so a CMRR greater than unity would imply that the buffer circuit can help suppress the common mode supply noise component, resulting in lower phase noise on the buffered outputs versus using a non-differentially buffered circuit.

$$CMRR = \left| \frac{1 + \gamma G_m R_o}{1 - \gamma G_m R_o} \right| \tag{169}$$

In a test simulation with the 22nm FD-SOI process used here, with RVTPMOS and LVTNMOS devices, both with (W/L) = 200n/20n, it was determined that $G_m R_o$ = 13.8, and $\gamma \approx$ 78 mV/V for both devices, thus a CMRR = 28 dB is obtained under these circumstances with the buffer.

7.10.1 Circuit

The implemented buffer circuit is shown in figure 57. All devices are (W/L) = 200n/20n, with LVTNMOS devices and RVTPMOS devices to allow for the usage of a common N-wells to form the common backgates for the sub-inverters. The layout of this buffer is in appendix B.2.3.

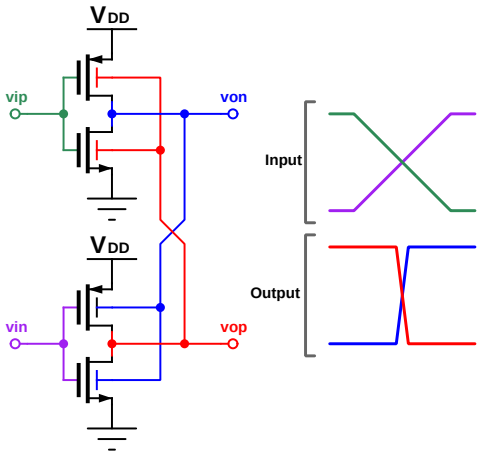


Figure 57: Backgate-coupled pseudodifferential buffer.

7.11 Level Shifter

Due to the split power domains of the implemented PLL, a level shifter is required interface the 0.8V oscillator to 0.5V logic. High domain to low domain transitions do not require any level conversion, but low voltage to high voltage domain conversion requires a level shifter circuit.

7.11.1 Circuit

The implemented level shifter is a standard low to high voltage domain latch-based shifter [34] shown in figure 58. All device dimensions are (W/L) = 200n/20n in RVT technology. The layout for this cell is provided in appendix B.7.

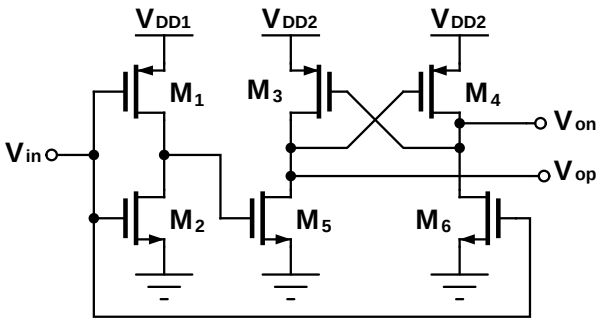


Figure 58: Basic low to high domain level shifter.

8 Behavioral Verification of Loop Filter/PLL

Using the extracted design parameters for ring oscillator phase noise, K_{VCO}, BBPD jitter (see results section, 9), and the proposed loop filter and DAC design methods, a behavioral discrete-time simulation of the PLL design was performed using a simulation framework [1] developed by the author of this work. The PLL simulation model used accurately allows for jitter and nonlinearity of the BBPD to be captured, as well as effects of quantization in the loop filter. This time domain simulation acts as a check for the loop filter design from the linearized filter optimization theory to be verified. Furthermore, this simulation allows for verification of PLL phase noise performance of the design at an ideal level first on short time scales before attempting a full transistor level PLL simulation. Figure 59 demonstrates the simulated and theoretically estimated power spectral density obtained for the PLL design, and table 5 contains results for theoretical and simulated PLL jitter values, along with an estimated lock time. In general, the theoretical and simulated values show close agreement, implying the linearized model of the BBPD-PLL and associated optimization theory developed in this work holds validity in the regime tested. Furthermore, the obtained values for RMS PLL jitter are below the value of 20.56 ps specified as a requirement for this design, suggesting that the phase noise requirements will be satisfied if the design is successfully translated into a transistor level implementation.

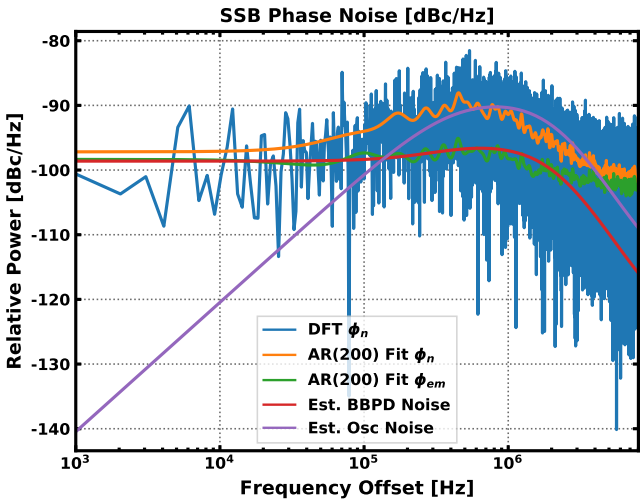


Figure 59: Behavioral simulation of PLL output phase noise power spectrum.

Parameter	Value	Unit
Lock time	664	ns
Theoretical RMS Jitter	13.59	ps
Simulated RMS Jitter	13.26	ps

Table 5: Estimated and simulated PLL performance parameters.

9 Implementation Results

The following sections provide system and component level performance results of the implemented PLL based from parasitic extracted transistor level simulations of the design.

9.1 Power Breakdown

The power consumption of the PLL is dominated by the oscillator and buffer, accounting for 76.4% and 19.1% of the total respectively as seen in figure 60 and table 6. The remaining portions of the PLL only account for a very small portion of the power consumption, being 4.6%, implying a high energy efficiency of those components.

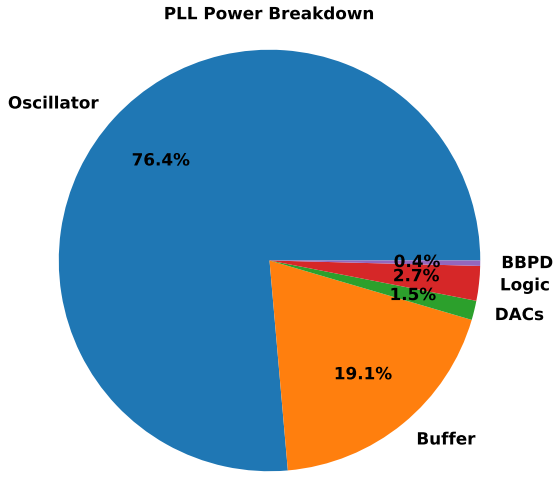


Figure 60: PLL Power breakdown.

Component	Power [μW]	% of Total
Oscillator	72.24	76.4
Buffer	18.03	19.1
3b CDAC	0.071	0.1
10b CDAC	1.33	1.4
BBPD	0.390	0.4
Logic	2.51	2.7
Total	**94.571**	**100**

Table 6: Power breakdown.

9.2 Area Breakdown

The area of the implemented PLL is dominated by the contributions from the differential 3b and 10b CDACs, accounting for a total of 64.2% of the active area as seen in figure 61 and table 7. This high proportion is due to the implementation of four single ended CDACs in total, requiring a large area. Routing and emtpy space outsize of the DACs, oscillator, logic and BBPD account for just 14.1% of the area, indicating a dense layout.

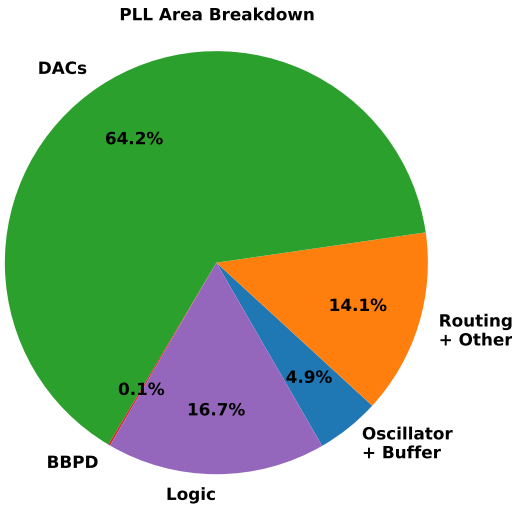


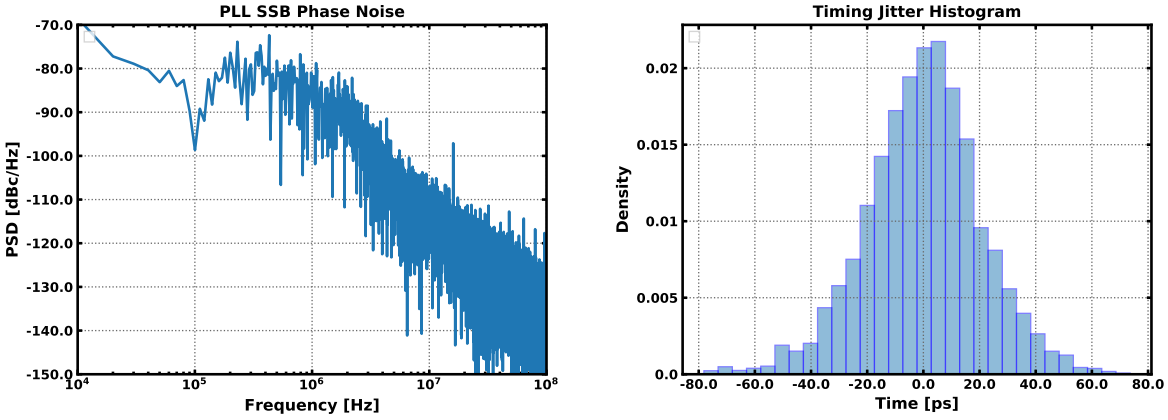
Figure 61: PLL Area breakdown.

Component	Area [μm^2]	% of Total
VCO + Buffer	177.1	4.9
3b CDAC	735.0	20.1
10b CDAC	1607.7	44.1
BBPD	5.31	0.1
Logic	610.2	16.7
Other/routing	514.7	14.1
Total	**3650**	**100**

Table 7: Area breakdown.

9.3 PLL Phase Noise

The single sideband phase noise power spectral density of the implemented PLL is in figure 62a. A histogram of absolute jitter of the simulated PLL is in figure 62b. A result for RMS integrated jitter of the PLL is in table 8, with additionally a calculated jitter FOM value using the power results in table 6.



(a) **(b)**

Figure 62: (a) PLL phase noise SSB spectral density, **(b)** PLL jitter histogram.

Parameter	Value	Units
RMS Integrated Jitter [4]	18.4	ps
FOM_{jitter}	-224.9	dB

Table 8: PLL phase noise and jitter performance values.

9.4 Voltage Controlled Oscillator

Results regarding phase noise, tuning and Monte Carlo variational analysis of the implemented voltage controlled oscillator are in this section.

9.4.1 Oscillator Phase Noise

The simulated single sideband phase noise power spectral density of the implemented voltage controlled oscillator is in figure 63, with lines fitted to the -30 dB/decade and -20 dB/decade regions of the phase noise. Table 9 provide extracted values for phase noise FOM of the PLL (see equation 44) for phase noise offsets of 1 MHz and 10 MHz from the carrier, and a measured value for the flicker noise corner frequency. The corner frequency is rather high, at 2 MHz, and results in the 1 MHz FOM value to be degraded by 4.16 dB versus the 10 MHz measurement.

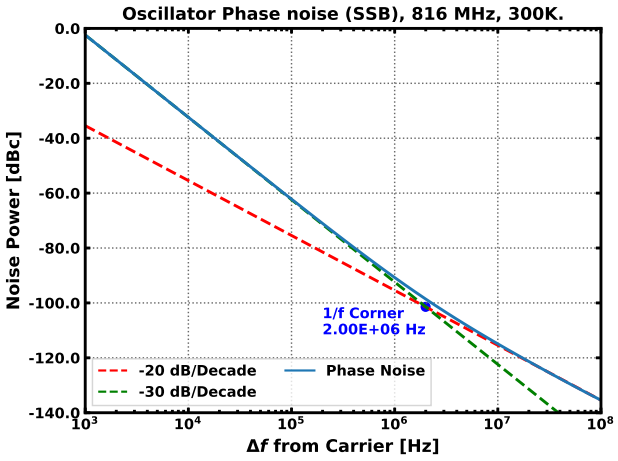


Figure 63: Ring oscillator phase noise (SSB).

Parameter	Value	Units
FOM$_{pn}$, Δf = 1 MHz	-160.4	dB
FOM$_{pn}$ Δf, = 10 MHz	-164.56	dB
Flicker corner	2.00	MHz

Table 9: Ring oscillator performance parameters.

9.4.2 VCO Tuning

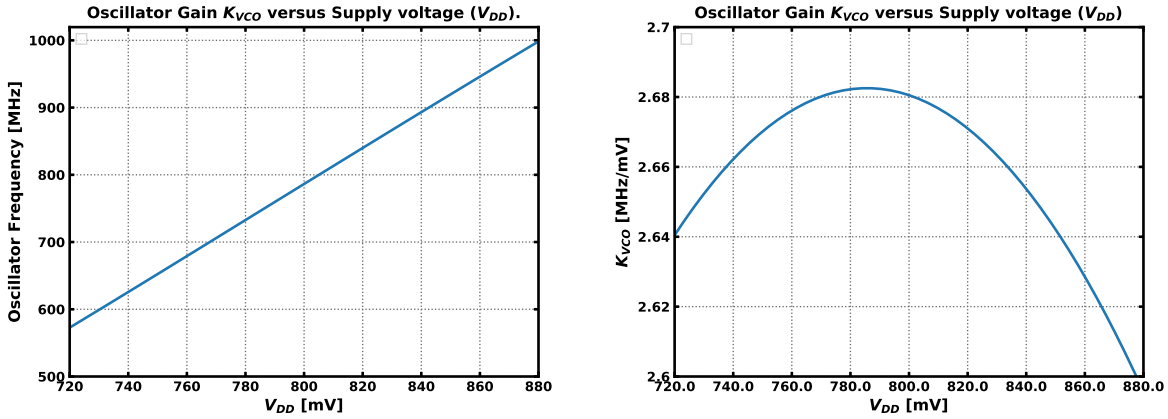
The oscillator tuning was characterized by sweeping the supply voltage, and the medium and fine backgate tuning range voltages. Results for tuning gain at nominal biasing (V_{DD} = 0.81, 0.405V backgate bias) are provided in table 10, which have been used in the loop filter design. It should be noted that the supply tuning has extremely high gain, 328 %/V, in comparison to the 0.677 %/V and 4.5 %/V observed in the medium and fine ranges, suggesting good granularity is achieved with the implemented tuning scheme. Results for frequency versus supply voltage and VCO gain versus supply voltage are in figure 64a and 64b. Results for frequency versus the medium tuning range and VCO gain versus the medium tuning are in figure 65a and 65b.

[4]Up to 100 MHz

Finally, results for frequency versus the fine tuning range and VCO gain versus the fine tuning are in figure 66a and 66b. The fine tuning range demonstrates good linearity, with $K_{VCO} \in$ [5.35, 5.60] kHz/mV for the full biasing range. The high linearity implies the closed loop characteristics of the PLL should be consistent across the different bias settings. The medium tuning range exhibits a sublinear characteristic, decreasing in frequency gain with increased bias, however this should be insignificant as the medium tuning setting should be static in steady state.

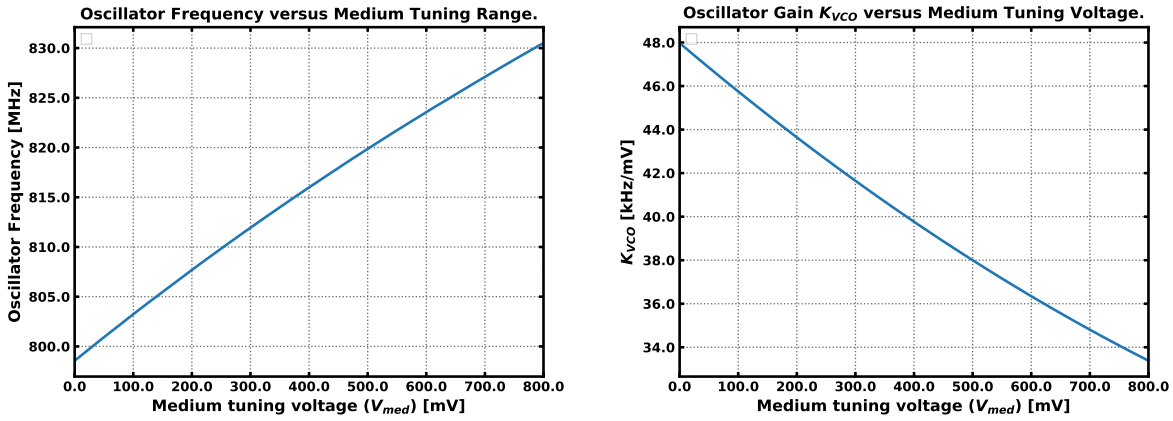
Mode	VCO Gain ($K_{VCO,fine}$)	Units	Normalized gain	Units
Supply tuning	2.677	MHz/mV	328	%/V
Medium tuning	39.76	kHz/mV	4.50	%/V
Fine tuning	5.529	kHz/mV	0.677	%/V

Table 10: Extracted VCO gain values.



(a) **(b)**

Figure 64: Supply voltage versus ($\pm$ 10% from 0.8V) **(a)** Oscillation Frequency, **(b)** VCO gain.



(a) **(b)**

Figure 65: Medium tuning range versus **(a)** Oscillation Frequency, **(b)** VCO gain.

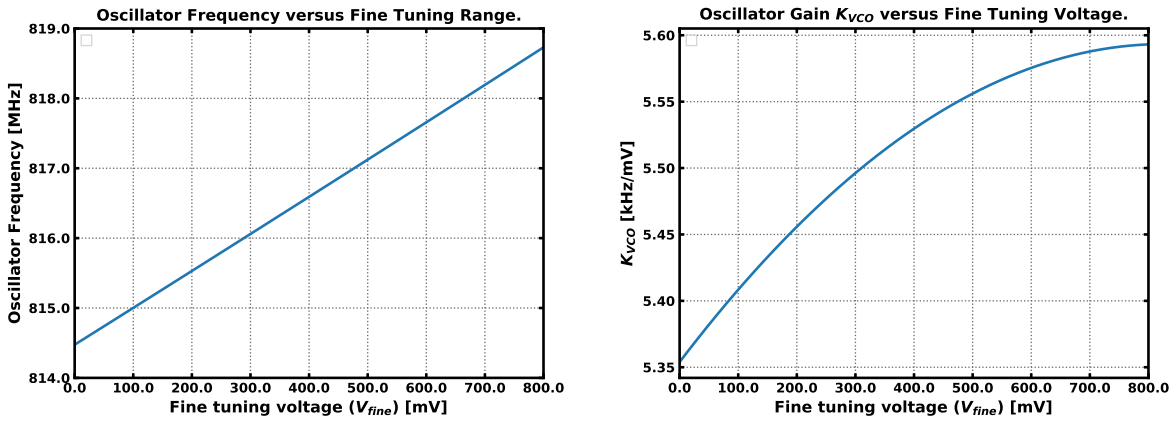


Figure 66: Fine tuning range versus **(a)** Oscillation Frequency, **(b)** VCO gain.

9.4.3 VCO Monte Carlo Simulation

To characterize the effect of process variation on the implemented oscillator, a Monte Carlo simulation of process variation and mismatch was run to extract a distribution for oscillator frequency (in figure 67a) and fine tuning K_{VCO} (in figure 67b). Nominal core biasing of V_{DD} = 0.81V was used, with 200 simulation samples. The resulting extracted values for RMS variance of the oscillator are in table 11, showing 4.5 % and 4.67 % RMS variation from the mean expected for the frequency and K_{VCO} respectively. The frequency variation should be correctable via implementation of frequency calibration, and the K_{VCO} variation is small and should not have a major impact on the closed loop PLL dynamics.

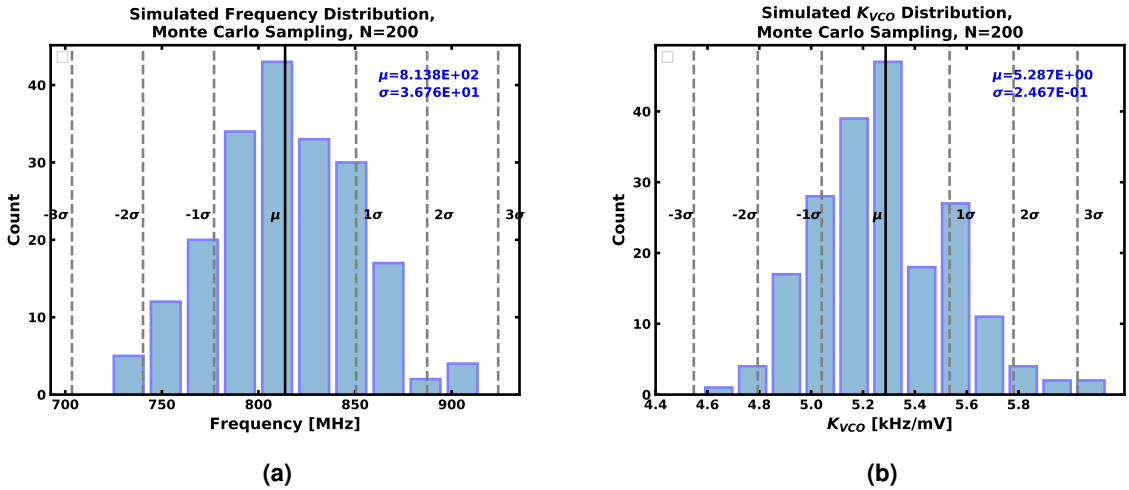


Figure 67: **(a)** Variation of oscillator frequency from Monte-Carlo variation/mismatch simulation, **(b)** Variation of VCO fine tuning gain from Monte-Carlo variation/mismatch simulation.

Parameter	RMS Variance	Units
Frequency	36.762 / 4.50	MHz / %
$K_{VCO,\ fine}$	0.2467 / 4.67	MHz / %

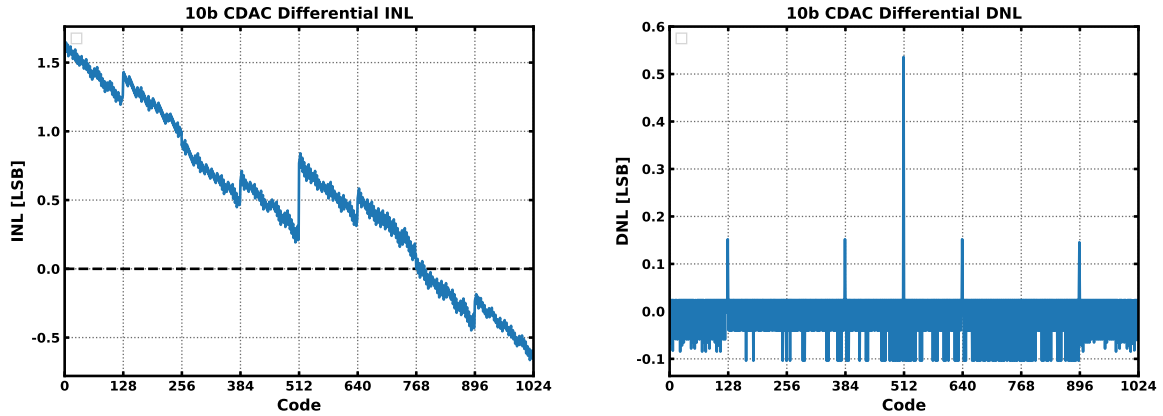
Table 11: Ring oscillator Monte Carlo simulation extracted values.

9.5 Oscillator Digitization

Results for implementation of the DACs which digitize the VCO and the corresponding DCO gains of the digitized VCO are in this section.

9.5.1 10b CDAC

The implemented 10b differential CDAC was simulated with an input code sweep in order to extract results for integral nonlinearity (figure 68a) and differential nonlinearity (figure 68b). A total gain error of approximately 2 LSB is seen across the input code range, with a maximum differential nonlinearity of 0.54 LSB. This implies high accuracy of the implemented CDAC, with no missing codes.

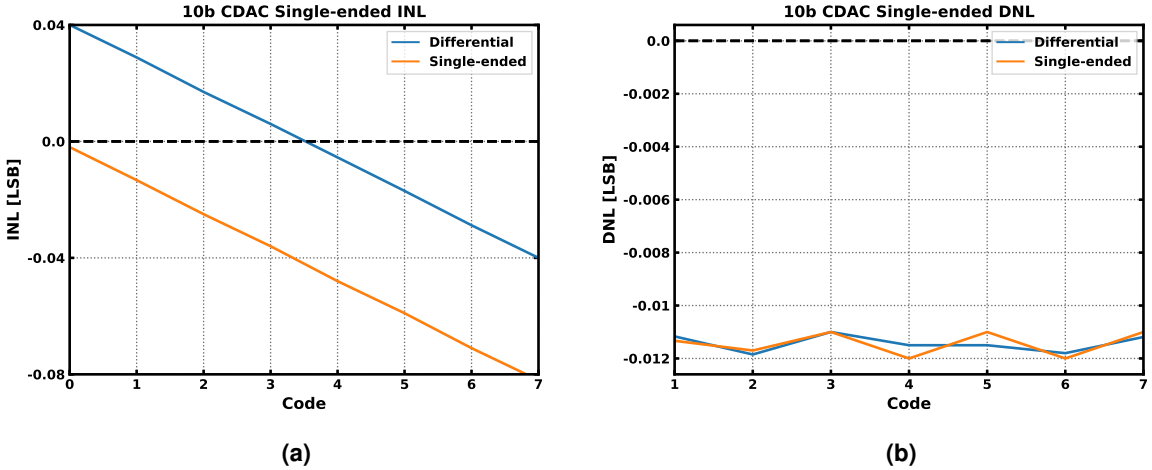


(a) **(b)**

Figure 68: Differential 10b CDAC **(a)** Integral Nonlinearity, **(b)** Differential Nonlinearity.

9.5.2 3b CDAC

The implemented 3b differential CDAC was simulated with an input code sweep in order to extract results for integral nonlinearity (figure 69a) and differential nonlinearity (figure 69b). A total gain error of 0.08 LSB is seen across the input code range, with a maximum differential nonlinearity of 0.012 LSB, implying high accuracy and no missing codes.



(a) (b)

Figure 69: Differential 3b CDAC **(a)** Integral Nonlinearity, **(b)** Differential Nonlinearity.

9.5.3 DCO Gain

Applying the expected LSB magnitude for the implemented DACs to the extracted VCO gains of table 10 yields the DCO gain values for the medium and fine ranges of the final implemented DCO in table 12.

Parameter	Value	Units
$K_{DCO,\,fine}$	4.2 ± 0.53[5]	KHz/LSB
$K_{DCO,\,med}$	2.00	MHz/LSB

Table 12: DCO Gain values from final VCO gain and DAC results.

[5] With $\pm 3\sigma$ of process variation coverage.

9.6 Bang-bang Phase Detector

Simulation of the implemented bang-bang phase detector to extract its jitter characteristics have been performed, to result in the output expectation versus input timing differential plot of figure 70a, and the jitter probability distribution plot of figure 70b. The final RMS jitter value of the implemented detector is in table 13. This value, 1.342 ps RMS, is small compared to the oscillation cycle period of 1225.5 ps, and results in a low impact to the PLL noise.

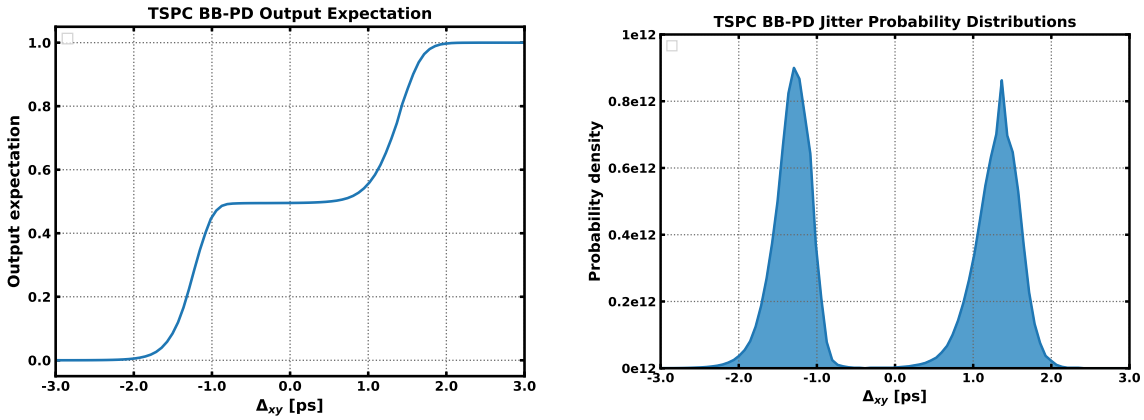


Figure 70: BBPD extracted jitter **(a)** Cumulative Distribution Function, **(b)** Probability Distribution Function.

Parameter	Value	Units
RMS Jitter	1.342 [6]	ps

Table 13: BBPD jitter extracted values.

[6] With noise simulated up to 20 GHz

9.7 Loop Filter

Utilizing the extracted design values of the PLL for oscillator phase noise, DCO gain, and phase detector jitter, the optimization theories of sections 6.4 and 6.5.1 have been applied to calculate optimal loop filter parameters, whose results are given in table 14 (undigitized) and table 15 (digitized).

9.7.1 Optimized Filter Parameters

Parameter	Value	Unit
K	1.2008153×12^{13}	
K_i	3.8686562×10^{7}	
K_p	2.2328113×10^{1}	
f_z	2.7575807×10^{5}	Hz
b_0	24.746023×10^{1}	
b_1	-22.328113×10^{1}	
Estimated bandwidth	1.369080	MHz
Estimated RMS jitter	13.5851	ps

Table 14: PLL parameters determined from filter design and optimization process for minimum phase noise with BBPD.

9.7.2 Digital Filter Implementation Parameters

Parameter	Value	Value (digital)	Value Error
Sign bits	1		
Integer bits	5		
Fractional bits	8		
Total dataword bits	14		
b_0	$2.474609375 \times 10^{1}$	`0b01100010111111`	$+6.9880465 \times 10^{-5}$
b_1	-2.2328125×10^{1}	`0b10100110101100`	$-1.1305756 \times 10^{-5}$

Table 15: Loop filter digitized coefficients.

9.8 Logic

Results for the synthesis and place and route of the loop filter logic are provided here. The logic count of the implemented design is in table 16, and the expected power consumption are in figure 17.

Component	Count	Area [μm^2]	Area (% total)
Sequential (DFF)	39	57.1	31.9
Inverter	29	3.86	2.2
Logic Gates	265	117.9	65.9
Total	333	178.9	100

Table 16: Synthesized logic counts.

Voltage	Corner	Temperature [C]	Power [μW]
0.59	SS	40	2.33
0.59	TT	40	2.51
0.65	TT	25	12.1

Table 17: Power consumption.

10 Discussion

In this discussion, the performance of the implemented design will first be analyzed via comparison to a theoretically calculated jitter limit, and then will be compared to current state of art. Small area and low power PLLs are considered for reference. Later, identified areas of improvement within the presented design are discussed.

10.1 Performance Limit for Ring Oscillator BBPD PLLs with PI-Controllers

In the case of a perfect ring oscillator PLL, all components would be noiseless and consume minimum possible energy. For an ADPLL, the consideration of power can be divided between logic and the oscillator. In the case of logic, the theoretical energy limit for switching of a logical level of a gate equates to $E_s = \ln(2)k_BT$, [35]. With a reference frequency of f_{ref}, and N digital nodes, the minimum possible power expenditure from digital components of PLL is in equation 170. This assumes the worst case scenario where all gates switch every cycle.

$$P_{min,digital} = N f_{ref} \ln(2) k_B T \tag{170}$$

At 300 K, the design considered in this work, having a logic complexity of N = 333 (based on the logic syntesis data in table 16), and f_{ref} = 16 MHz, yields a *theoretical* minimum logic power consumption of 22 pW, practically zero. Infact, it is found *theoretically* that the one can operate 242 thousand gates at 1 GHz and consume only 1 μW of power. Following these findings, and considering total PLL operating power on the order of 100 μW, it is asserted here that the theoretical power limit for digital components of an ADPLL is practically zero. In the case of a ring oscillator, however, power may not be scaled to zero as with logic. This is due to the fundamental relationship between oscillator power and phase noise, as discussed in section 3.5.4. Therefore, it is now asserted that an optimal ADPLL will expend all of its power in its oscillator. Analyzing the case presented in this work of a BBPD and PI-controller based PLL, it was determined that the expected value of total phase noise is in equation 113. Using the theoretical limit of ring oscillator phase noise in equation 47, the result of equation 171 provides the minimum achievable PI-controller BBPD PLL phase noise.

$$\sigma^2_{\Phi_{n,opt}} = 74.79376 \cdot \frac{\mathcal{L}_{min}(f) f^2}{f_{ref}} = 74.79376 \cdot \frac{7.33 k_B T f^2_{osc}}{f_{ref} P_{DC}} \tag{171}$$

This result can be converted into RMS jitter, with $\sigma_{\Phi_n} = 2\pi f_{osc} \sigma_{j_t}$, yielding equation 172.

$$\sigma^2_{j_t} = 74.79376 \cdot \frac{7.33 k_B T}{(2\pi)^2 f_{ref} P_{DC}} \tag{172}$$

Using the FOM_{jitter} expression in equation 48, it is seen that the theoretical limit for PLL FOM of the PI-controller BBPD-PLL is in equation 173. Noting the dependence on reference frequency, with f_{ref} = 16 MHz at 300 K, this is -234.4 dB. Equation 174 provides the general expression for FOM_{jitter} limit provided an oscillator FOM_{pn} value. It should be noted that the only way to improve jitter FOM in the proposed architecture is to reduce temperature, increase the reference frequency, or improve oscillator phase noise FOM (that is, use a resonant oscillator with higher Q, for example a LC oscillator).

$$\text{FOM}_{\text{jitter,min}} = 10\log_{10}\left(\frac{\sigma_{t_j}^2}{(1\text{ s})^2}\cdot\frac{P_{DC}}{1\text{ mW}}\right) = 10\log_{10}\left(74.79376\cdot\frac{7.33\times10^3 k_B T}{(2\pi)^2 f_{ref}}\right) \tag{173}$$

$$\text{FOM}_{\text{jitter,min}} = \text{FOM}_{pn} + 10\log_{10}\left(\frac{74.79376}{(2\pi)^2 f_{ref}}\right) \tag{174}$$

10.2 State of Art

In order to form a comparison to the current state of art for ultra low power PLLs, a wide search of literature was undertaken, and data from relevant PLL designs were collected into table 18. Specific criteria for this search were power consumption below 1 mW, publication within 2 years of this work, similar oscillation frequency, and preference to ring oscillator designs implementing integer-N architectures. Filtering in this manner has resulted in a curated selection of 5 highly comparable designs to the one of this work.

Analyzing FOM_{jitter}, this work is on the lower end of being state of art, achieving -225 dB, where the observed range was [-236.8,-226.1] dB for the selected works. Using the theoretical limit for FOM_{jitter} in this topology derived in section 10.1, the best achievable value of FOM_{jitter} possible with this work using a ring oscillator is -234.4 dB (at 300K and f_{ref} = 16 MHz). Adding a penalty for consuming power in non-oscillator components (22.3 μW of the 95 μW power consumption) results in a 1.2 dB reduction from the optimal jitter FOM. Furthermore, the obtained oscillator phase noise FOM of -160.4 dB, adds an additional penalty of 4.8 dB versus the theoretically obtainable -165.2 dB. Thus the realistic best case result in this design including the penalties is therefore -228.4 dB, which explains the positioning of this work on the low end of FOM_{jitter} versus comparable designs. In equation 174, oscillator FOM is seen to be improved with increasing reference frequency. In this work, however, a higher reference frequency was not an option, as this design was constrained with a 32 MHz reference frequency, and this must be divided to 16 MHz to achieve an integer ratio to the target RF frequency of 2448 MHz. If it were possible to increase the reference frequency, for example to 200 MHz as in Xiang'20 [36], the theoretical FOM_{jitter} then is extended to -245.4 dB, or -239.4 dB penalized, bringing the FOM to be highly competitive with the other works. As a general statement, the FOM_{jitter} of this work is necessarily limited by the design constraints imposed on the PLL.

This work comes out ahead of existing designs in terms of total power consumption, where sub-100μW is achieved, a feat that was not paralleled by any of the surveyed works. In the application area of this work to duty cycled wake up receivers, fast locking and ultra low power consumption are of primary interest in terms of PLL performance. While the other surveyed designs obtain better phase noise performance than this work with simultaneously higher power consumption, this design has been optimized to have sufficiently good phase noise for the target application while preferring reduction in power over improving phase noise. Furthermore, the architectural choices of this work have been implemented to favor fast locking, on the order of 664 ns, compared to the other design which make no mention of locking performance, require long lock times, in upwards of 120μs (1200 cycles at 10 MHz) in the case of Liu'19, or have prohibitively high power with 682 μW in Xiang'20 to obtain a 200 ns locktime. It is therefore ascertained that this work meets the needs of the end use for wake up receivers better than the surveyed literature, providing merit to the design beyond the pure phase noise performance results.

In terms of oscillator performance, this design shows improvements again in power versus others, utilizing only 72.2 μW. The next closest work in oscillator power is that by Liu'19 [6]. That design uses an LC VCO with a SSB phase noise of -107 dBc/Hz at 1 MHz for a 2.46 GHz frequency, yielding an oscillator FOM of -184.5 dB. The oscillator is only a single stage differential LC oscillator, consuming 107 μW. Practically, the PLL of this work is required to generate quadrature signals, so the non-quadrature 107 μW of that work should be doubled, i.e. to 214 μW, to estimate power consumption for quadrature phase generation. A new oscillator FOM of -181.5 is achieved, which is 21.1 dB improved over the -160.4 dB achieved in this work. It is not expected that the remaining works are substantially better than this work in terms of oscillator performance, due to them being ring oscillator based and constrained with the same theoretical limit of -165.2 dB for FOM phase noise at 300 K. Based purely on oscillator phase noise values, and the prediction for PI-controller BBPD-PLL FOM$_{jitter}$ in equation 174, the LC-based PLL should be expected to achieve *at least* 21.1 dB better FOM$_{jitter}$ than this work. However, this is not completely observed, Liu only reports -236.8 dB FOM$_{jitter}$, an improvement of 11.8 dB over this work. This discrepancy is probably due to the FLL architecture used in that work. It appears that the oscillator core from Liu's work, coupled with the PLL topology of this work, would yield a FOM$_{jitter}$ of -248.0 dB, substantially better than that demonstrated in either work. It is a question, perhaps for future work, to determine if an LC oscillator core can be used satisfactorily with the topology of this work for the needs of wake up receivers. Issues cropping up related to the LC oscillator may prove challenging due to non-instantaneous startup, and inability to reset oscillator phase to be clock synchronous instantly, which may overall lead to locking instability with the BBPD-PLL.

In regards to implementation area, this work is highly competitive to current state of art design, only beat in area by 1% by a fractional-N PLL built in 5nm technology by Liu'20 [7]. This should be expected due to substantially smaller devices and metal pitch in 5nm versus the 22nm

in this work. The LC based design by Liu'19 achieved an area 49x of this work, which was limited by integration area needed by the resonant LC circuit to have sufficiently high-Q. The analog designs also came close in area. The design implemented by Zhang'19 [5] in 40 nm technology achieved only 2.39x greater area than this work.

Concerning analog versus digital implementation, the two analog ring-oscillator PLL designs (Zhang'19 [5] and Xiang'20 [36]) are comparable in terms of FOM, however, power is not seen to scale as low as this work. Both designs also employ higher reference frequencies than here, being 100 MHz [5] and 200 MHz [36], which is expected to help reduce phase noise contribution from the oscillator significantly, as much higher loop bandwidths can be used, bringing down the in-band phase noise level. The analog designs discussed here are both phase-frequency detector (PFD) and charge pump (CP) based, which exhibit linear dynamics [26], in comparison to the BBPD design of this work that is inherently nonlinear due to its detector characteristics. As seen in this work, BBPD designs can exhibit undesirable emergent behaviors, potentially leading to cyclostationary phase trajectories and increased phase noise contributions if not properly designed. This hazard can be mitigated with linearized designs, for example employing a PFD-CP architecture. It is expected, though, that analog implementations will introduce different non-idealities into the PLL, namely extra analog noise into the loop, which may negate any advantages. It is possible to implement a PFD-PLL with a digital CP loop filter to remove these noise sources, as Palaniappan'18 [37] does. In that work, a comparable FOM to this work of -226.1 dB was seen, albeit at a lower output frequency of circa 400 MHz. According to [14], the PFD-CP approach is not necessarily better, as in practice, equal performance in terms of total jitter is achievable with BBPD and charge pump designs *if* properly optimized. Furthermore, implementation complexity is higher for a PFD, nominally requiring two D flip flops and an AND gate [26], whereas a BBPD is as simple as a single D flip flop. Thus, when scaling for minimum power, lower power should be achievable with a BBPD as it is simpler. Overall, it does not appear that either analog implementation or CP-PFD designs pose any significant advantages to this work in the ultra low power regime when considering the design of a sub-100 μW PLL. Rather, digital implementation is perhaps more favorable due to lower sensitivity to PVT variation.

Two of the reviewed papers presented interesting comparison figures for (a) PLL jitter FOM versus power consumption, in figure 71a, and (b), jitter FOM versus implementation area, in figure 71b. The works that the figures were published in are from 2019 and 2020 respectively. With the PLL of this work having a power consumption of sub-100 μW, a FOM_{jitter} of -225 dB, and area of 0.00365 mm^2, it is seen that this design lands off the chart, beyond the suggested FOM trend line in power versus FOM, and lands in a comparable position with other recent design in terms of FOM versus area. Based on this comparison, it is concluded that this work is boundary pushing in terms of power consumption, and is also state of art in area of implementation.

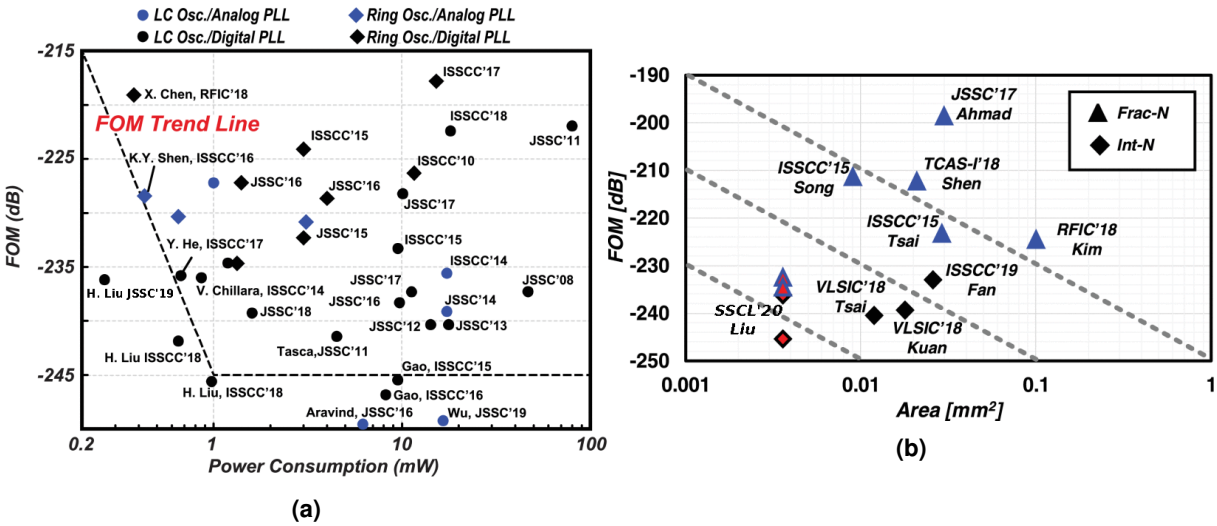


Figure 71: (a) FOM_{jitter} versus power modified from [6] (JSSC 2019), **(b)** FOM_{jitter} versus area modified from [7] (SSCL 2020).

Parameter	This Work	JSSC'19 Liu [6]	NORCHIP'18 Palaniappan [37]	SSCL'20 Liu [7]	2019 Zhang [5]	CICC'20 Xiang [36]
Analog/Digital	Digital	Digital	Digital	Digital	Analog	Analog
Int-N/Frac-N	Int-N	Frac-N	Int-N	Int-N	Int-N	Int-N
Architecture	BB-PLL[7]	FLL + ODZ[8]	Digital CP-PLL[9]	IL-PLL[10]	CP-PLL	CP-PLL
Process	22nm	65nm	40nm	5nm	40nm	22nm
Osc. Type	RO	LC	RO	RO	RO	RO
Detector	BBPD	ODZ	PFD[11]	Sampling	PFD	PFD
Area [mm^2]	0.00365	0.25	0.0186	0.0036	0.00873	0.015
Power [μW]	95	265	270.5	440	170	682
f_{ref} [MHz]	16	10	-	40	100	200
f_{osc} [GHz]	0.816	2.1-3.1	330-470	1.0	1.6	3.2
Osc. Stages (N_{stg})	6	1	8	-	3	-
$f_{osc} \times N_{stg}$ [GHz]	4.896	2.1-3.1	2640-3760	-	4.8	-
Osc. Power [μW]	72.2	107	-	398	-	225
Jitter [ps_{RMS}]	18.4	2.8	9.53	2.34	8.3	2.3
$\text{FOM}_{\text{jitter}}$ **[dB]**	-225.0	-236.8	-226.1	-236.2	-229.3	-234.3
Lock-time [μs]	0.664	$\leq$ 120	-	-	-	0.2

Table 18: State of art comparison of PLLs.

[7] BBPD PLL
[8] Out of deadzone detector
[9] Charge Pump PLL
[10] Injection-locked PLL
[11] Phase-frequency detector

10.3 Radio System Performance

For the specified radio system in which this PLL has been designed to enable, a requirement of $\leq$ 20.56 ps RMS integrated jitter was defined to ensure satisfactory bit error rate performance. In this work, the implemented design meets this requirement, with an observed RMS jitter of 18.4 ps (see table 8). Furthermore, the power requirement of $\leq$ 100 μW is obtained, with 95 μW of power consumption realized. Finally, the implemented PLL enables IQ sampling at 2.448 GHz through oversampling at the 1/3 subharmonic (816 MHz), satisfying the last major requirement for the PLL design to enable radio operation at 2.448 GHz. Therefore, the implemented PLL design of this work has been found to satisfy the original design requirements.

10.4 Areas of Improvement

10.4.1 Coarse Frequency Calibration

Currently, no frequency calibration scheme is implemented in the design of this work. This work primarily focused on achieving sub-100μW power consumption under steady state conditions, so it was decided that implementation of a calibration scheme was out of the project scope. For a design implemented in physical hardware, however, calibration will be important to handle effects of process, voltage and temperature variation on the oscillator characteristics. In section 7.3.4, it was observed that ring oscillators exhibit high frequency tuning gain with supply tuning, seeing on the order of 328% frequency change per volt of applied bias in the design of this work (see table 10). To combat large potential large variations in nominal oscillator frequency, it is therefore suggested to implement coarse frequency calibration using supply based tuning. Such a change would require implementation of a digitally tunable voltage regulator for the oscillator core, with tight regulation of supply voltage. Requirement of tight regulation of the supply is paramount due to the high frequency gain of the oscillator with supply tuning (2.577 MHz/mV). Design of such a regulator within the PLL power requirements is possibly a daunting endeavor, and has again been considered outside of the current scope of this work, but is a possible future area for improvement.

10.4.2 Subharmonic Oscillator

The usage of a 1/3 subharmonic oscillator as in this work is possibly undesirable in some regards for application to radio receiver design. This design choice pushes additional circuit complexity into the receiver circuitry, which must be designed to achieve full rate sampling by edge combining the 12 oscillator phases resulting from the 6-stage, 1/3 sub-harmonic oscillator. It is therefore probable that topological improvements for achieving full frequency operation of this

PLL design for radio applications is an attainable area of improvement.

10.4.3 Ignored Flicker Noise

In this work, only oscillator noise components with -20 db/decade slope were considered in the PLL loop filter optimization theory, in order to simplify the derivations. The -20 db/decade noise components were specifically paid attention to due to being a fundamental component of ring oscillator phase noise [22]. In Leeson's model for phase noise (section 3.5.2), it is seen that flicker noise can result in a -30 dB/decade phase noise region for low frequencies, being mainly influenced by device characteristics. It has been found through phase noise simulation of the implemented ring oscillator that the flicker noise region is infact a substantial noise component in this design, with a 2 MHz flicker noise corner as seen in figure 63. This has an impact of reducing oscillator FOM for low frequencies, as seen in table 9. It is therefore expected that the optimization result from the introduced loop filter design theory is suboptimal for the PLL implemented in this work. This non-ideality likely explains the discrepancy in the transistor-level PLL simulation results for RMS jitter being higher than that expected by theory, where 18.4 ps was observed versus a prediction of 13.59 ps. In the interest of optimizing PLL performance, it is therefore suggested as a future area of improvement to extend the derivations of this work to include flicker noise components.

10.4.4 CDAC Switching Noise

It has been observed in the implemented CDACs that transient spikes occur in the DAC output during changing of the input code, as demonstrated in figure 72. This is a result of varying RC constants of the different switch and capacitor combinations. The small RC constant switch and capacitor combinations will settle very fast, causing an initial rising/falling portion of a spike to be seen in the DCO output. The larger capacitor and switch combinations will settle delayed in time, causing the spike to subside and the output to settle to the desired value. The DAC spikes, while short in duration, are expected to have a contribution to increasing phase noise of the oscillator, perhaps explaining part the excess jitter observed in the transistor level PLL simulation versus theory. An area of improvement in future is to reduce this spiking, through more careful design of the switch and capacitor combinations.

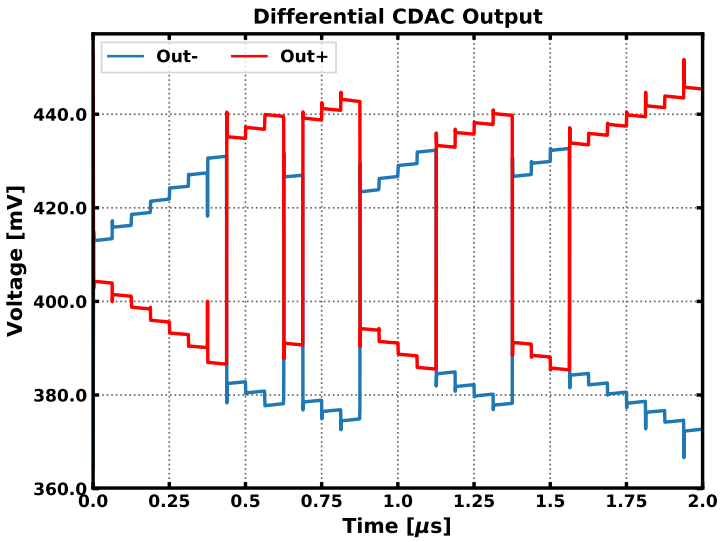


Figure 72: Noise spikes in DAC output during switching.

11 Conclusion

In this work, an ultra-low power phase locked loop of novel architecture was implemented to achieve ultra-low power operation for the needs of wake up receiver applications, with state of art power (95 μW) and area (0.00365 mm^2). The proposed architecture successfully implemented power saving simplifications, including dividerless operation, an all-digital loop filter, and a novel DCO design. The DCO architecture introduced a new pseudo-differential delay cell based voltage controlled ring oscillator topology, operating on backgate connections to implement both frequency tuning and differential operation. This ring oscillator topology exploits characteristics of FD-SOI, which enabled highly linear oscillator gain with rail-to-rail control voltages. The oscillator topology design was shown to operate effectively coupled with a capacitive DAC, resulting in a low energy, low complexity oscillator with fine control of frequency. Theory regarding the design and operation of such oscillators was introduced. Furthermore, theory for filter optimization of PI-controller BBPD-PLLs was derived, and a theoretical result for the best case jitter and jitter FOM for such a topology was derived. Specifically, it was determined that PI-controller BBPD-PLL jitter is proportional directly to oscillator phase noise FOM, and inversely proportional to reference frequency. In the case of implementation with ring oscillators operating at a fixed temperature, the fundamental limit for jitter is inversely proportional to reference frequency, leading to the finding that the only way to improve PI-controller BBPD-PLL phase noise and jitter is to increase the reference frequency used.

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A Verilog

A.1 Loop Filter and Reset Logic

```
module lf
(
  input in, clk, rst, set_out, lf_en,
  input signed [13:0] b0, b1,
  input [12:0] init_out,
  output reg vco_rst, dac_rst,
  output [12:0] lf_out, lf_out_n
);
  reg last, wait_cycle1, wait_cycle2;
  reg signed [23:0] accum_reg;  // Output accumulator
  wire signed [13:0] p0, p1;    // PI filter products
  wire signed [23:0] sum;       // Accumulator sum
  reg [12:0] lf_rounded;        // Rounded integer portion
                                // of accumulator for output

  // Muxes - Implements PI filter multipliers with a BBPD
  assign p0 = in ? b0 : ~b0 + 1;
  assign p1 = last ? b1 : ~b1 + 1;

  // Accumulator sum
  assign sum = p0 + p1 + accum_reg;

  // Accumulator fractional part msb for output rounding decision
  assign frac_msb = sum[7];

  // set outputs OR'd with DAC reset as needed by CDACs
  assign lf_out = lf_rounded|{13{dac_rst}};
  assign lf_out_n = (~lf_rounded)|{13{dac_rst}};

  always @ (posedge clk) begin
    if (rst) begin  // RST cycle 1: DCO+DAC RST
      dac_rst <= 1;   // Assert DCO/DAC rst synchronously
      vco_rst <= 1;
    end
    else if ((!rst)&&(dac_rst)) begin
      dac_rst <= 0;   // RST Cycle 2: de-assert dac_rst,
      wait_cycle1 <= 1;
    end
    else if (wait_cycle1) begin
      vco_rst <= 0;     // RST cycle 3: Wait 1 cycle
      wait_cycle1 <= 0; // before BBPD sampling, no lf update
```

```
42        wait_cycle2 <= 1;
43      end
44      else if (wait_cycle2) begin
45        wait_cycle2 <= 0; // RST cycle 4: Wait 1 cycle
46        last <= in;       // Record initial BBPD sample, no lf update
47      end
48      else if (lf_en) begin   // Normal operation
49        last <= in;
50        accum_reg <= sum;
51        lf_rounded <= frac_msb ? sum[20:8] + 1 : sum[20:8]; //output rounding
52      end
53      if (set_out) begin  // Set output if set_out asserted
54        accum_reg[23:21] <= {3{1'b0}};
55        accum_reg[20:8] <= init_out[12:0];
56        accum_reg[7:0] <= {8{1'b0}};
57        lf_rounded <= init_out[12:0];
58      end
59    end
60
61  endmodule
```

Listing 1: Loop filter hardware description.

B Layout

B.1 Full Layout

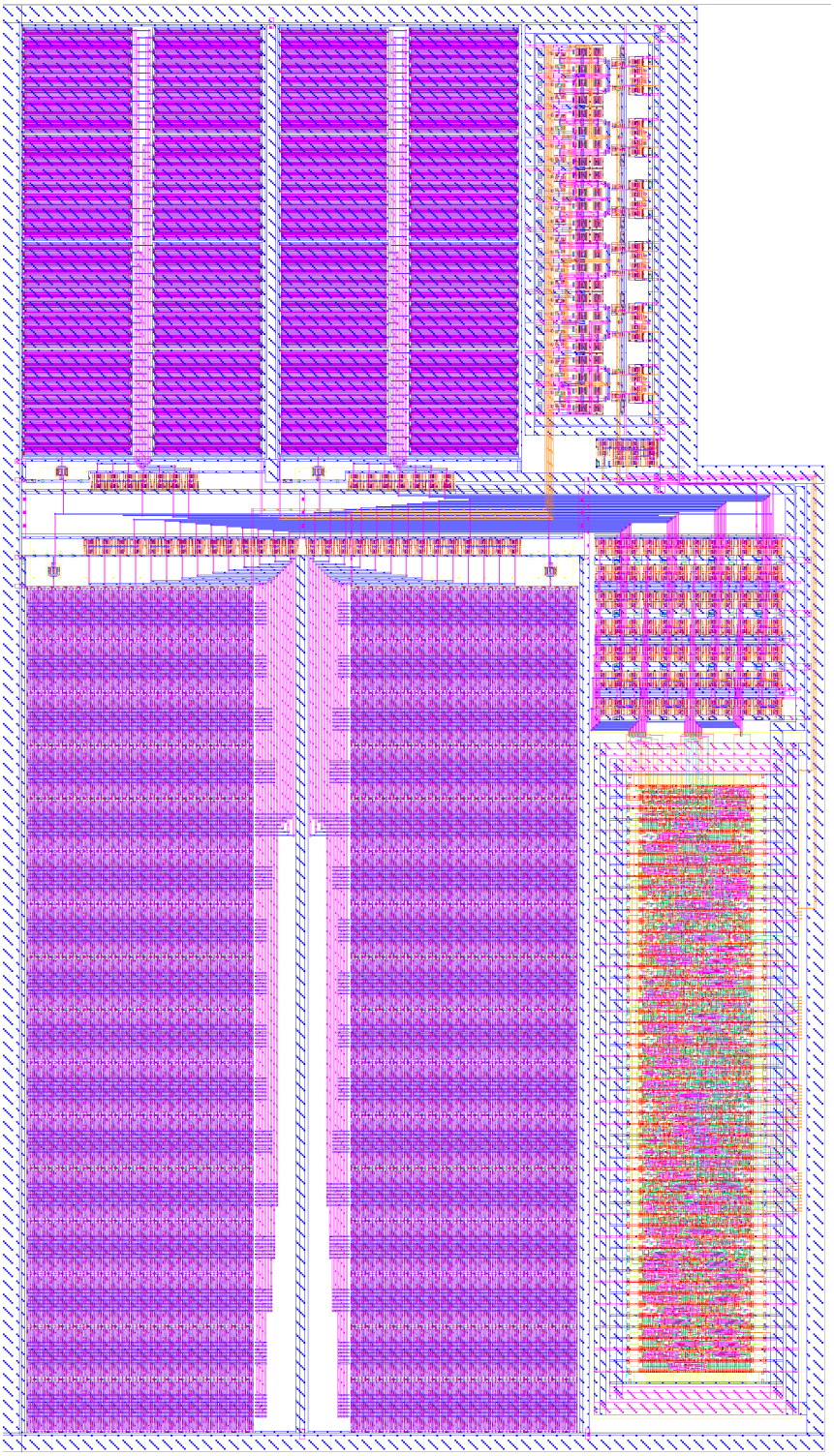


Figure 73: Full PLL Layout.

B.2 Ring Oscillator

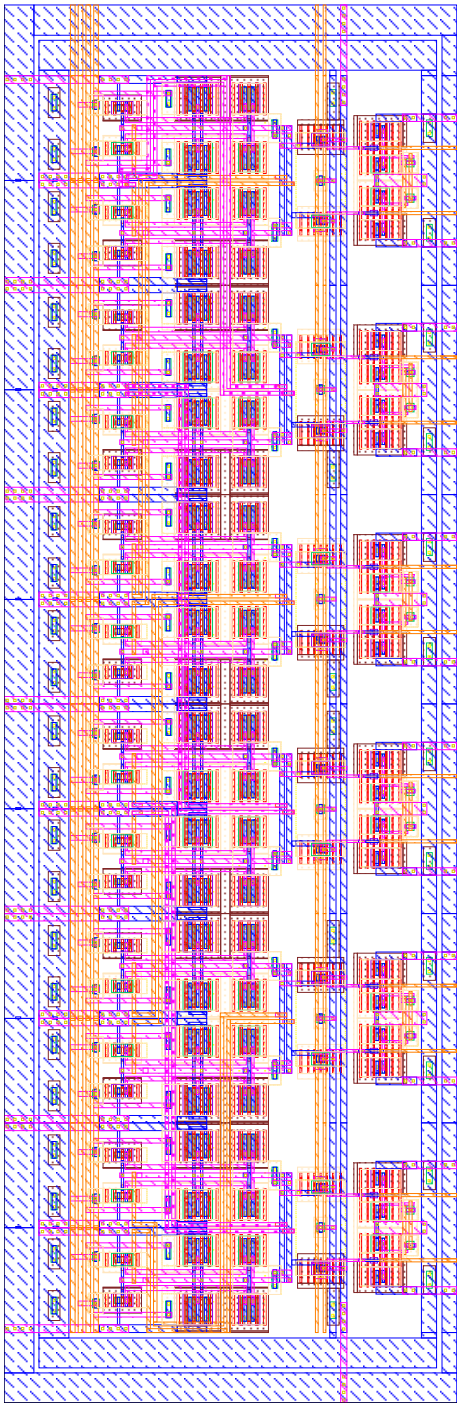


Figure 74: Full six stage oscillator layout with capacitor tuning bank, reset switches, and output buffer.

B.2.1 Pseudodifferential Inverter Delay Cell

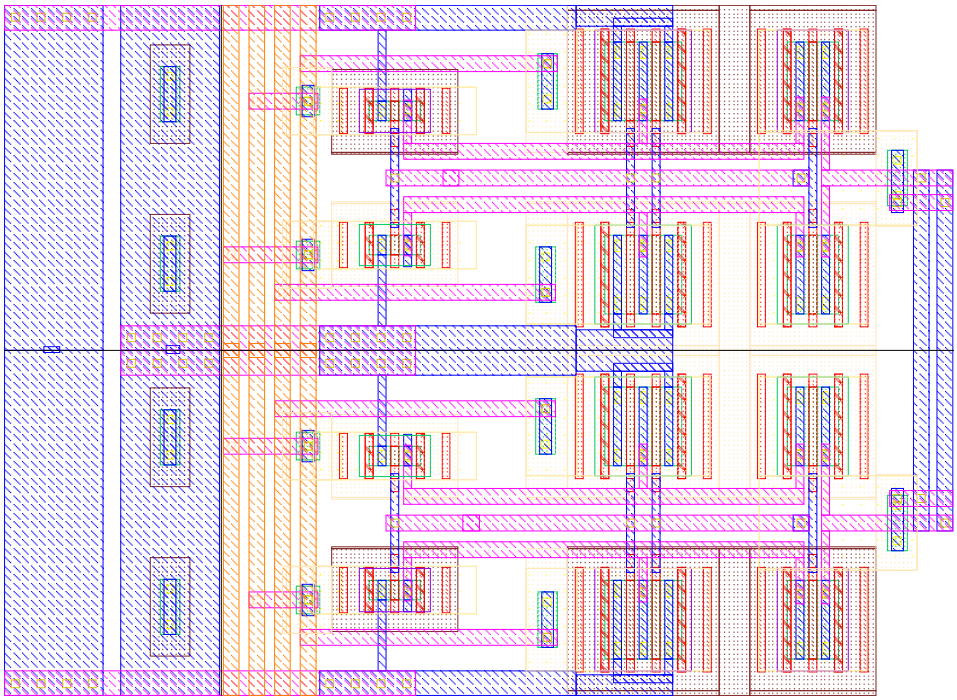


Figure 75: Unit delay stage pseudodifferential inverter.

B.2.2 Reset Switches

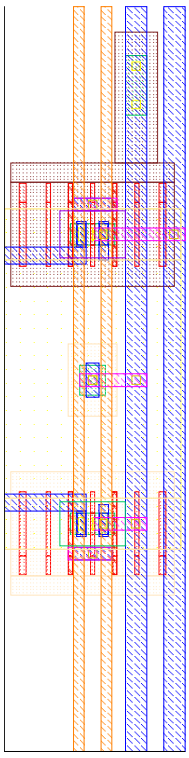


Figure 76: Oscillator reset switches.

B.2.3 Output Buffer

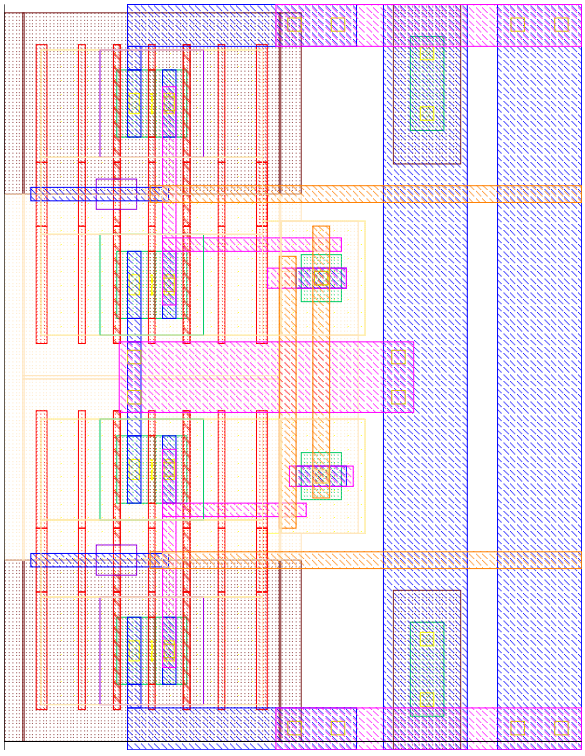


Figure 77: Pseudodifferential inverter buffer cell.

B.3 10b CDAC

B.3.1 Full CDAC Layout

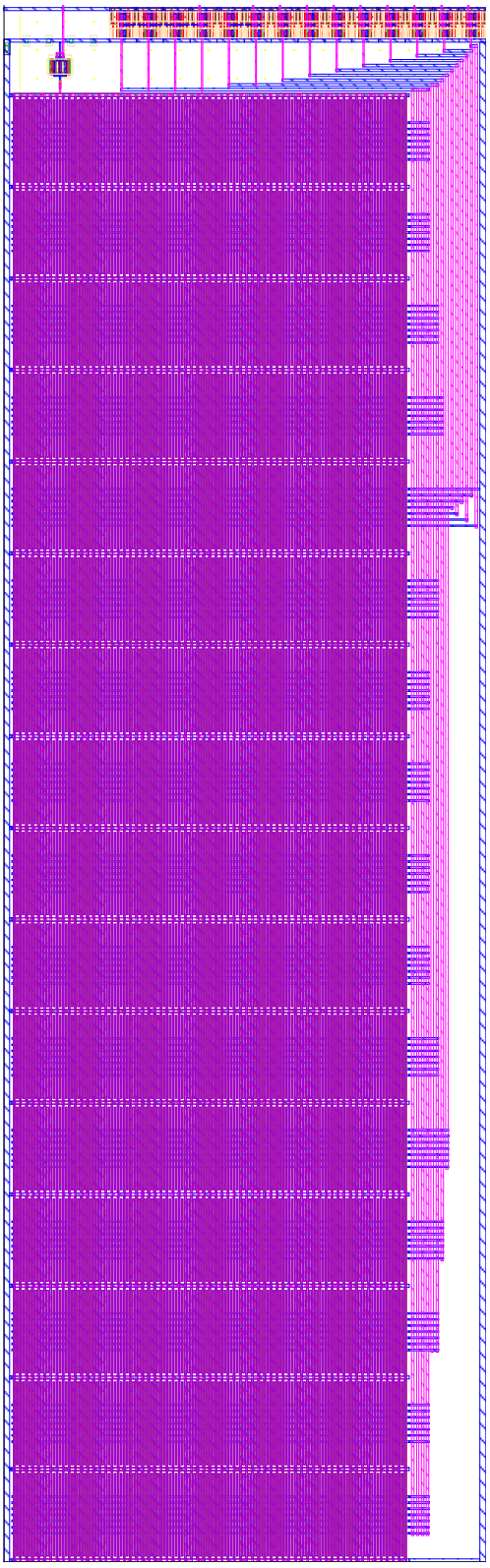


Figure 78: 10 bit CDAC layout.

B.3.2 64 Unit Capacitor Sub-bank

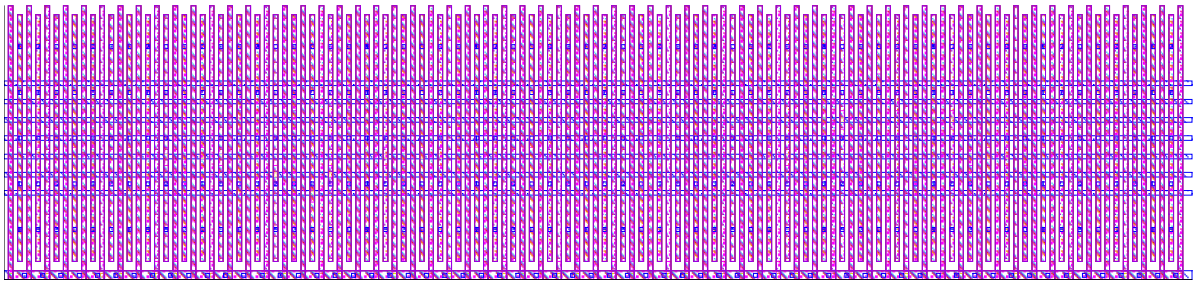


Figure 79: 64 unit capacitor bank.

B.4 CDAC Capacitor Switch

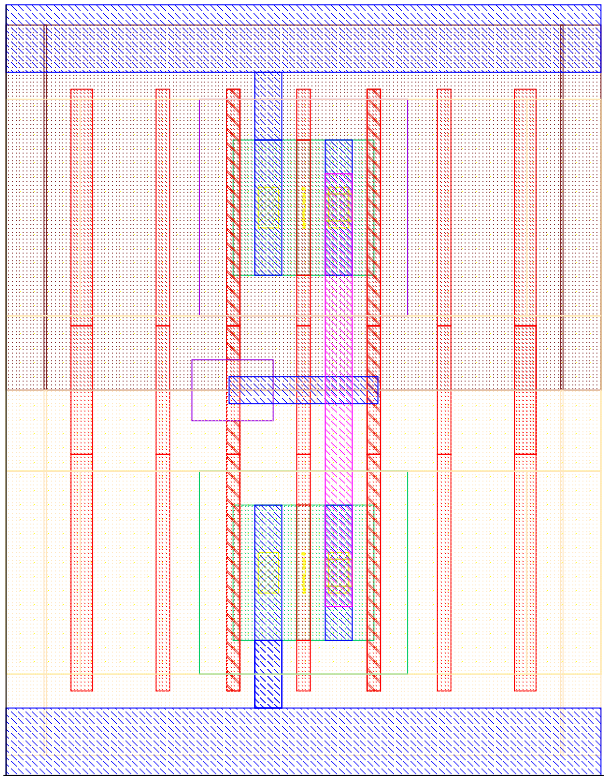


Figure 80: CDAC capacitor switch.

B.5 3b CDAC

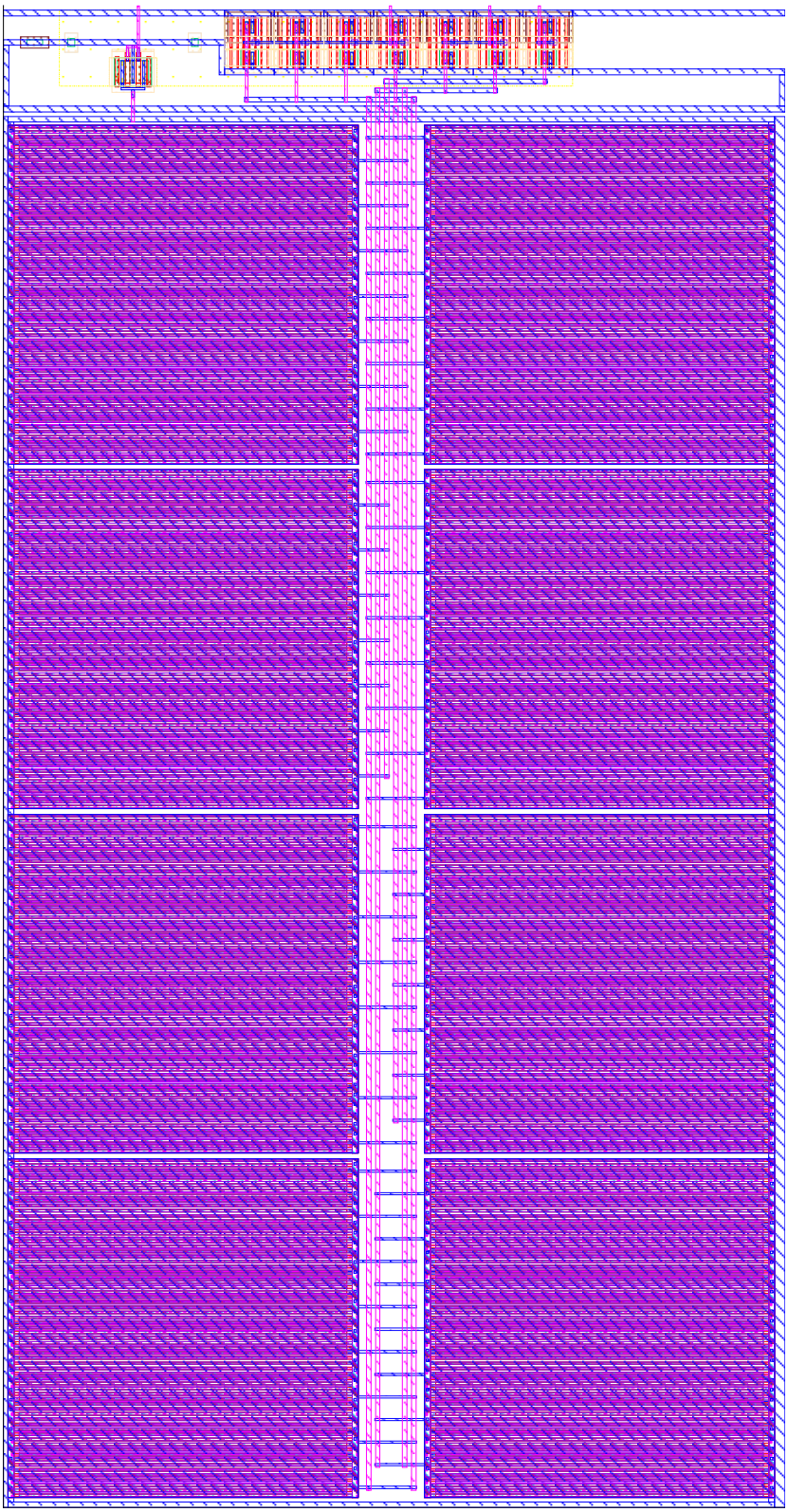


Figure 81: 3 bit CDAC layout.

B.6 BBPD

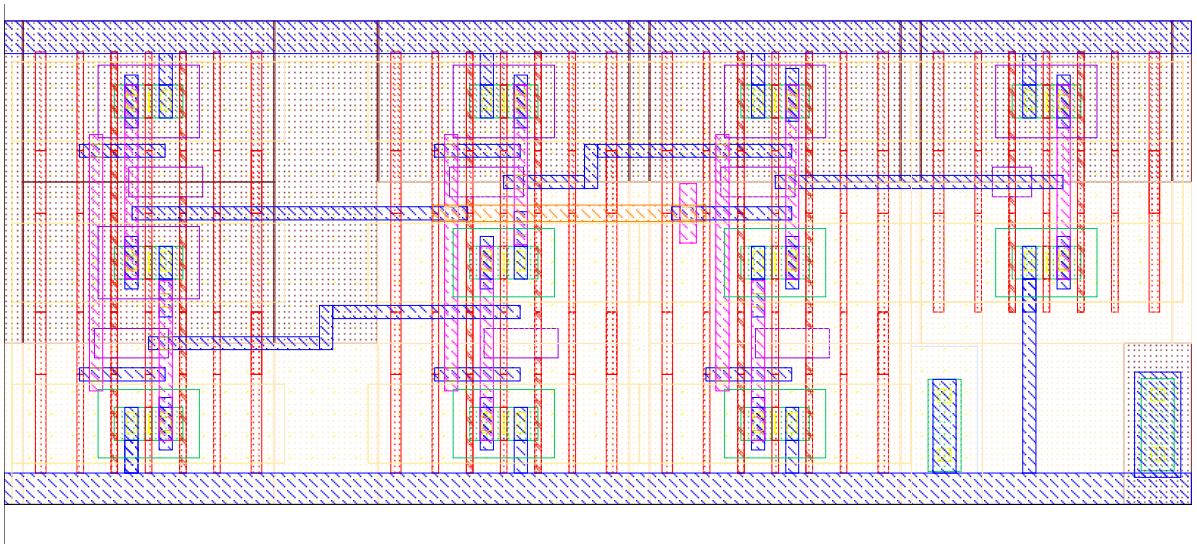


Figure 82: Single ended bang-bang phase detector.

B.7 Level Shifter

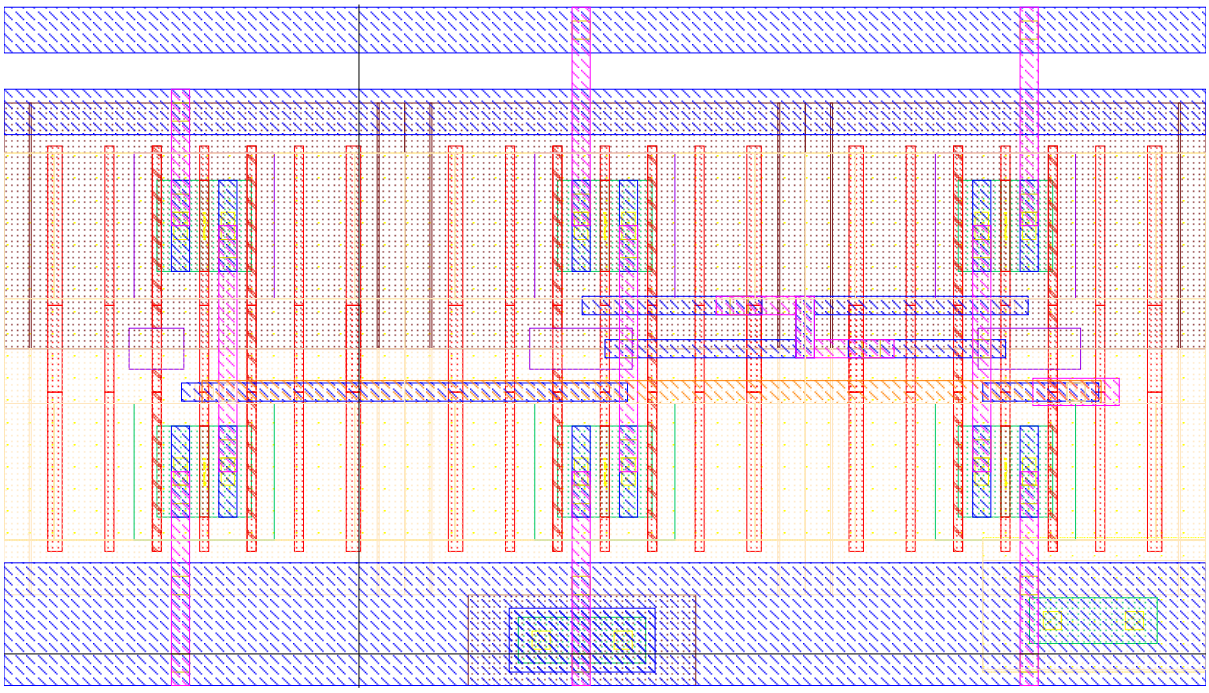


Figure 83: Low to high voltage domain level shifter.

B.8 Loop Filter Logic

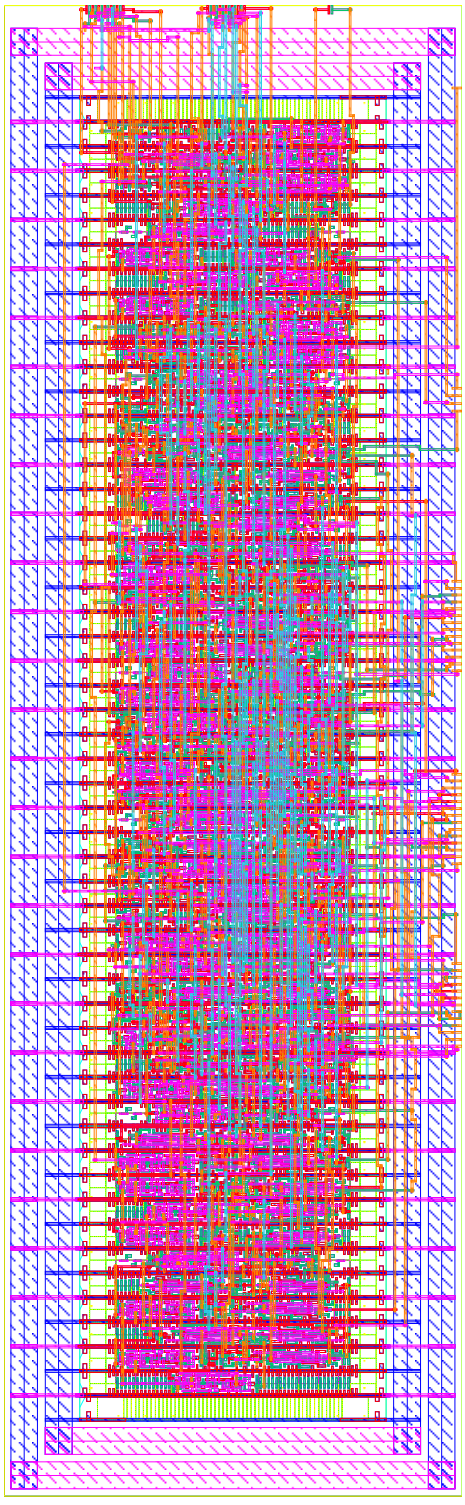
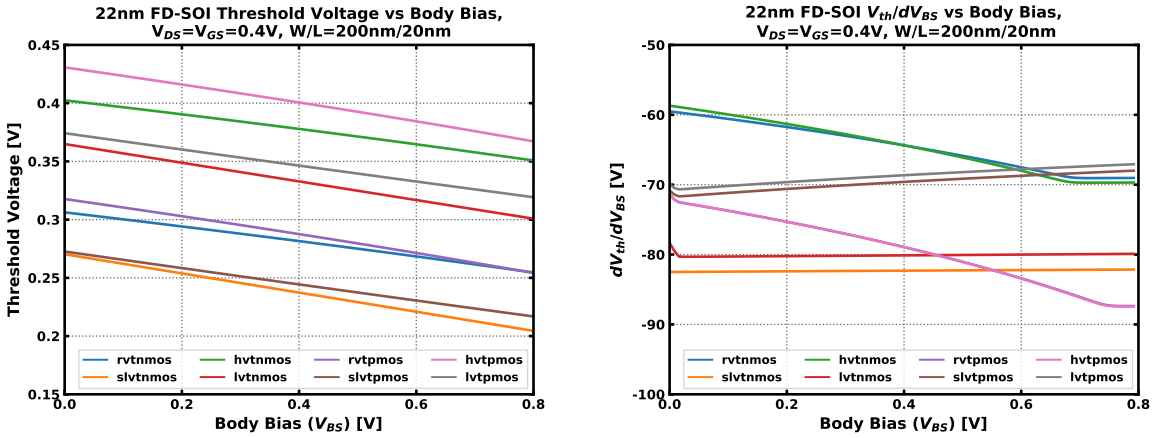


Figure 84: Place and route generated loop filter logic for PLL.

C Extracted FD-SOI Device Parameters

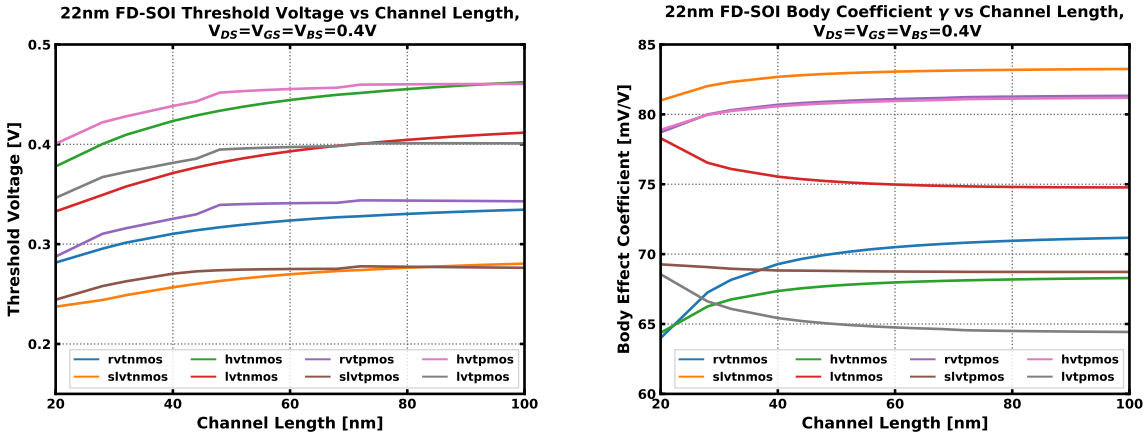
To analyze the body effect with FD-SOI backgates of the 22nm process technology used in this work, SPICE simulations to extract the body effect coefficient γ and threshold voltage V_{TH} for different channel lengths and bias conditions have been performed. Parameters for threshold voltage, and transconductances g_m and g_{mb} have been extracted using DC operating point simulations. Noting the relation from equation 12, where $g_{mb} = \gamma g_m$, γ can be deduced from operating point g_m and g_{mb} values. Figures 85a and 85b show the extracted threshold voltage versus backgate bias and the slope of that relationship. Figures 86a and 86b show the extracted threshold voltage and body effect coefficient versus channel length. Furthermore, table 19 provides a selection of extracted N-channel device parameters, and table 20 provides extracted P-channel devices parameters.

It is observed that the threshold voltage slopes of figure 85 are not perfectly linear, but for the simplified analytical purposes of this work, they can be approximated as linear. The P-channel devices in the technology of this work show a high degree of linearity, whereas the N-channel devices show variation in slope as in figure 85b. It is also observed that the threshold voltage and body effect coefficient vary as channel lengths approach zero, but flatten out for longer device length. A final note is there is substantial variation of γ and V_{TH} between device types, so prudent care must be taken in the oscillator for selection of devices and their sizing.



(a) **(b)**

Figure 85: (a) 22nm FD-SOI process threshold voltage versus body bias, **(b)** Rate of change of threshold voltage versus body bias.



(a) **(b)**

Figure 86: (a) 22nm FD-SOI process extracted threshold voltage versus channel length, **(b)** Extracted body effect coefficient.

Device	L [nm]	W [nm]	V_{th} [mV]	γ [mV/V]
rvtnmos	20	100	306.3	59.14
rvtnmos	100	500	376.4	65.4
slvtnmos	20	100	270.3	81.38
slvtnmos	100	500	326.7	83.23
hvtnmos	20	100	402.4	58.85
hvtnmos	100	500	513.5	61.96
lvtnmos	20	100	364.9	77.72
lvtnmos	100	500	466.3	74.85

Table 19: 22nm FD-SOI process NMOS device threshold voltage and body effect coefficient extraction.

Device	L [nm]	W [nm]	V_{th} [mV]	γ [mV/V]
rvtpmos	20	100	317.7	71.51
rvtpmos	100	500	366.8	74.32
slvtpmos	20	100	272.6	71.09
slvtpmos	100	500	294.4	70.79
hvtpmos	20	100	430.7	71.28
hvtpmos	100	500	488.4	74.23
lvtpmos	20	100	374.2	69.93
lvtpmos	100	500	422.8	66.43

Table 20: 22nm FD-SOI process PMOS device threshold voltage and body effect coefficient extraction.

D Optimal Selection of Backgate-Coupled Pseudodifferential Inverter Devices

To implement inverters with common backgate wells supporting positive voltage biasing, devices that are over N-wells must be used in the 22nm FD-SOI process utilized in this work. Accordingly, these devices are RVTPMOS, HVTPMOS, SLVTNMOS, LVTNMOS. The devices should be relatively matched in terms of threshold voltage and body effect coefficient. Referencing the extracted device parameters in appendix C (tables 19 and 20), HVTPMOS is not considered here due to its high threshold voltage, being greater than $V_{DD}/2$ for $V_{DD} = 0.8$. Thus, an optimization for ratio of inverter W_P/W_N for the circuit shown in figure 87 was performed. This circuit is used to determine the common mode level V_M of a common-backgate inverter achieved through self-biasing. This level is expected to be the output crossing level of a backgate-coupled pseudodifferential inverter fabricated with the same devices as the test circuit. This level should be ideally at $V_{DD}/2$, thus the optimization simulation run determined the optimal W_P/W_N required in order to achieve $V_M = V_{DD}/2$. This optimization was run for inverters of RVTPMOS + LVTNMOS devices, and RVTPMOS + SLVTNMOS devices. The result of this optimization is in figure 88. It is seen that for RVTPMOS + SLVTNMOS, large W_P/W_N ratios are required, on the order of 5 or greater. In the RVTPMOS + LVTNMOS combination, a near unity ratio is achieved, with $W_P/W_N \in [0.8, 1.5]$ for $L \in [20, 100]$ nm. It is of interest to keep device sizes similar to reduce total device capacitance, so the selection of RVTPMOS + LVTNMOS devices in the 22 nm FD-SOI process of this work has been determined to be the optimal device combination for backgate-coupled pseudodifferential inverter implementation. These devices also possess close backgate coefficients, for LVTNMOS $\gamma \in$ [77.72, 74.85] mV/V and for RVTPMOS $\gamma \in$ [71.51, 74.32] mV/V, for $L \in [20, 100]$ nm.

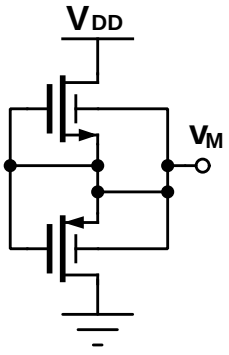
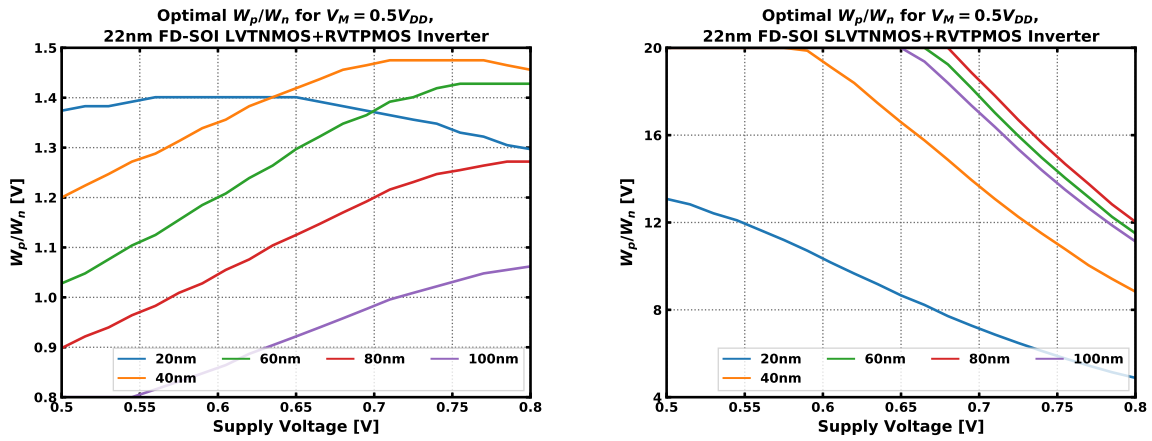


Figure 87: Circuit to extract self-biased common mode level.



(a) **(b)**

Figure 88: (a) Optimal width ratio of RVTPMOS/LVTNMOS, **(b)** Optimal width ratio of RVTPMOS/SLVTNMOS.