Master's thesis

NTNU
Norwegian University of Science and Technology
Faculty of Information Technology and Electrical Engineering
Department of Electronic Systems

Simen Føreland

# Design of an efficient and linear 10W GaN PA with harmonic tuning at input and output.

Master's thesis in Electronic Systems Design
Supervisor: Morten Olavsbråten
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# Abstract

Striving for high efficiency has historically been a driving force in power amplifier design. Many high efficiency power amplifier designs employ compression of the output signal in order to achieve greater efficiency. Increasing the efficiency usually comes at the cost of poor linearity performance when the transistor is driven into compression.

In this thesis a linearization technique based on input network impedance tuning is explored. A 10 W GaN HEMT is utilized to design an amplifier based on the highly efficient class $F^{-1}$ at 2.4 GHz. The amplifier achieves high efficiency through compression, at the expense of linearity. Separate input networks are tuned and constructed to enhance the linearity by attenuation of intermodulation products.

The linearization technique reaches an improvement in $IMD_3$ products of 3.4-, 4.55- , 4.5 dB for output powers 32-, 35 and 38 dBm respectively.

Varying degrees of linearity enhancement are attained through frequencies 2.3-2.5 GHz, given sufficient output power is generated.

# Sammendrag

Strebing etter høy effektivitet har historisk sett vært en drivkraft i effekforsterkerdesign. Mange effektforsterkere med høy effektivitet benytter kompressjon av utgangssignalet for å øke effektiviteten. Økning i effektivitet følger ofte med seg en reduksjon i lineæritet når transistoren er drevet i kompressjon.

I denne oppgaven er en lineæriseringsteknikk basert på endring av inngangsnettverksimpedansen utforsket. En 10 W GaN HEMT er benyttet for å designe en forsterker basert på den høyt effektive klasse $F^{-1}$ forsterkeren ved 2.4 GHz. Forsterkeren oppnår høy effektivitet gjennom kompressjon, på kostnad av lineæritet. Separate inngansnettverk er tunet og konstruert for å oppnå forbedring i lineæritet ved å redusere intermodulasjonsprodukter.

Lineæriseringsteknikken oppnår forbedring i tredjeordens intermodulasjonsprodukt, $IMD_3$, på 3.4-, 4.55- og 4.5 dB for henholdsvis utgangseffekt på 32-, 35 og 38 dBm.

Varierende forbedring av lineæritet er observert gjennom frekvensbåndet 2.3-2.5 GHz, ved tilstrekkelig generert utganseffekt.

# Preface

This master thesis is submitted to the Department of Electronics Systems at the Norwegian University of Science and Technology (NTNU) in Trondheim, Norway.

I would like to thank my supervisor Morten Olavsbråten. His spirit and technical input has been a great contributor and driving force throughout the process of completing this thesis.

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# Abbreviations

| | |
|---|---|
| **RF** | Radio Frequency |
| **PA** | Power Amplifier |
| **BW** | Bandwidth |
| **PAE** | Power Added Efficiency |
| **IMD** | Intermodulation Distortion |
| **PAPR** | Peak-to-Average Power Ratio |
| **ADS** | Advanced Design Systems |
| **OPBO** | Output Power Back-Off |
| **GaN** | Gallium Nitride |
| **HEMT** | High-Electron-Mobility Transistor |
| **HI** | Harmonic Injection |
| **QAM** | Quadrature Amplitude Modulation |
| **ACPR** | Adjacent Channel Power Ratio |
| **DUT** | Device Under Test |
| **ET** | Envelope Tracking |

# Chapter 1

# Introduction

The goal in this thesis is to look at a specific technique to increase linearity and possibly efficiency in an RF power amplifier. While there are several active techniques in order to increase linearity the focus in this thesis will be a passive technique. No additional power will be injected into the circuit and the performance of the amplifier is increased by passive RF network design. Further techniques which does involve actively injecting power into the circuit could be used in conjunction to this technique down the line, in order to increase the overall performance of the amplifier.

Increasing linearity in a power amplifier is traditionally done by the use of digital solutions like digital predistortion, envelope tracking, feed forward and harmonic injection [6]. The latter will have close similarities to the technique presented in this thesis. Harmonic injection uses the fact that non-linear components may be cancelled by injection of an identical signal but with opposite phase. Actively injecting a second harmonic at the drain of a transistor in counter-phase could reduce the harmonic components which are inevitably created by a transistor in compression. This can be applied for all kinds of unwanted signals at the output to achieve great linearity in the output signal.

The main issue with harmonic injection as means of linearization is that it requires a separate signal processing circuit in order to calculate and generate the signals which are to be injected. While the outcome is improved linearity, the problem is shifted to the efficiency of the amplifier. This is a trade-off, and it is hard to realize a scenario which achieves both.

High linearity in power amplifiers is required when applying real signals with complex modulation schemes. High Peak-to-average power ratios require high dynamic range in power amplifiers, and ideally high linearity for all levels of output power. If a power amplifiers linearity is high in for instance 6 dB back off it is not implied that the amplifier performs the same in saturation, or vice versa.

## 1.1 overview

High efficiency is important in power amplifier technology because it is the driving factor for power consumption, i.e. battery life. A power amplifier is usually driven into saturation to increase efficiency, but this will usually lead to higher levels of distortion. Filtering techniques and other active techniques like digital pre-distortion[6] and harmonic injection[6, 5] focuses on reducing this generated noise which may leak into adjacent radio channels.

The focus of this thesis can be summarized as as distorting the signal at the input in order to achieve an overall gain in linearity and/or efficiency at the output of the transistor.

Because the linearity is not achieved by linear operation, such as the standard class A amplifier, there is no need to have a perfectly linear device. Other modes of operation will therefore be considered in order to achieve efficiency, such as the class F amplifier.

Design specifications for the amplifier to be designed through this thesis is summarized in Table 1.1.

Table 1.1: Amplifier specifications

| **Parameter** | **Goal** |
|---|---|
| Fundamental frequency | 2.4 GHz |
| Smallsignal BW | 200 MHz |
| Small signal gain | $> 14$ dB |
| Ripple in band | $<$ 1dB |
| S11 | $< -10$ dB |
| Saturated output power | 41 dBm |
| Efficiency | maximize |
| Linearity | maximize |

# Chapter 2

# Theory and background

## 2.1 S-parameters

In order to describe RF networks scattering matrices are often used which represent the network in terms of incident-, reflected- and transmitted waves. A scattering matrix can be used to describe RF networks with any number of ports and is shown in Equation 2.1.

$$\begin{bmatrix} V_1^- \\ V_2^- \\ \vdots \\ V_N^- \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} & \dots & S_{1N} \\ S_{21} & S_{22} & & \vdots \\ \vdots & & & \\ S_{N1} & \dots & & S_{NN} \end{bmatrix} \begin{bmatrix} V_1^+ \\ V_2^+ \\ \vdots \\ V_N^+ \end{bmatrix} \tag{2.1}$$

$V_m^-$ is the amplitude of the reflected voltage wave from port m, while $V_m^+$ is the incident voltage wave on port m. The scattering matrix elements are referred to as S-parameters and are defined as the ratio between reflected and incident voltage wave, as shown in Equation 2.2

$$S_{ij} = \left.\frac{V_i^-}{V_j^+}\right|_{V_k^+ for\, k \neq 0} \tag{2.2}$$

The generalized S-parameter in Equation 2.2 explains that $S_{ij}$ is the relation between reflected wave $V_i^-$ from port $i$ when providing port $j$ with an incident wave of $V_j^+$. In other words port $i$ is the responding port when exciting port $j$.

The following scattering matrix is typically used to describe a two port network:

$$\begin{bmatrix} V_1^- \\ V_2^- \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} V_1^+ \\ V_2^+ \end{bmatrix} \tag{2.3}$$

Input return loss or insertion loss is defined by Equation 2.4.

$$RL_{in} = -20log_{10}(|S_{11}|)\,[dB] \tag{2.4}$$

Output return loss is given by Equation 2.5.

$$RL_{out} = -20log_{10}(|S_{22}|)\,[dB] \tag{2.5}$$

Small signal gain is defined by Equation 2.6

$$|G| = S_{21}\,[dB] \tag{2.6}$$

Reverse gain is defined by Equation 2.7

$$G_{rev} = S_{12}\,[dB] \tag{2.7}$$

## 2.2 PA design

A general schematic of a power amplifier topology is illustrated in Figure 2.1. This section will provide information regarding matching-, bias-, and stability networks in power amplifier applications.

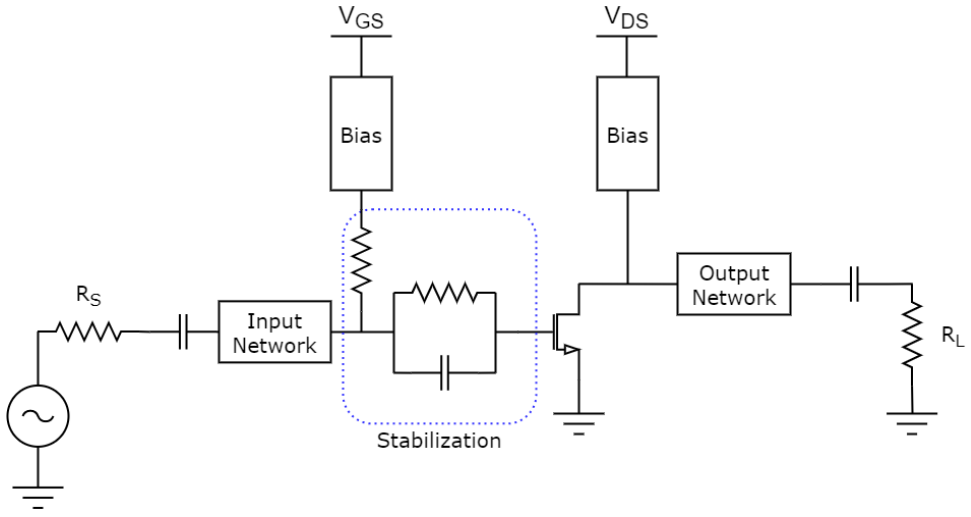



Figure 2.1: General schematic of a power amplifier circuit.

### 2.2.1 Matching networks

Matching networks are typically distributed in power amplifier topologies to ensure performance of specific design parameters. When the resistance of a load is matched exactly to the resistance of the source maximum power transfer is possible as the reflection coefficient $\Gamma$ is set to 0. A complex source impedance can be matched by providing the source with a load with the conjugated impedance value, effectively cancelling the reactance and creating a resistive match [7]. Matching to meet other criteria such as efficiency and output power is possible, and is defined by transistor parameters.

### 2.2.2 Bias networks

Biasing networks exist to prevent RF power from leaking into DC power supplies. This is both to protect the DC power supply and to ensure that RF power is delivered to the load. An ideal biasing network serves as an open circuit impedance for all frequencies above DC, while serving as a short circuit for DC where $f = 0Hz$. Several decoupling capacitors are usually connected in the bias to ground, to serve as a short circuit for any stray RF signals.

### 2.2.3 Stability

Unconditional stability is usually a design criterion in RF power amplifier design, where the networks needs to meet conditions where the reflection coefficients $|\Gamma_{in}|$ and $\Gamma_{out}$ are less than 1 for all load impedances. These conditions are met by default in any passive networks, however in active devices feedback at certain frequencies may cause oscillation [7]. Equation 2.8 provides a figure of merit of the stability based on S-parameters, where $\Delta = S_{11}S_{22} - S_{12}S_{21}$

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22} - \Delta S_{11}^*| + |S_{12}S_{21}|} > 1 \tag{2.8}$$

In order to provide unconditional stability to an amplifier circuit stability networks are often added. Such a network introduces loss at frequencies which may be problematic, and reduces the reflection coefficient below 1 which is required for unconditional stability. In RFPAs the most common occurrence of oscillations are at relatively low frequencies [6].

## 2.3 PA classes

Many classes of operation in regards to a power amplifiers may be defined by its conduction angle, $\alpha$. The conduction angle is defined as the angle of which a device conducts current through one full period (360 °or $2\pi$) [6]. The most basic amplifier classes ranging from A to C are defined by their conduction angle as shown in Table 2.1.

Table 2.1: Amplifier classes based on conduction angle $\alpha$

| **Amplifier class** | **Conduction angle** $\alpha$ |
|---|---|
| A | $\alpha = 2\pi$ |
| AB | $\pi < \alpha < 2\pi$ |
| B | $\alpha = \pi$ |
| C | $0 < \alpha < \pi$ |

Setting up a transistor to work in a specific type of operation requires a set bias at the input and output of the transistor. A class A amplifier conducts current through the whole RF cycle, i.e. $\alpha = 2\pi = 360°$ as shown in Table 2.1. Class A amplifiers operate in the linear region where the output signal will ideally be a pure representation of the input only scaled in amplitude. Changing the bias to lower the conduction angle results in other modes of operation as represented in Table 2.1. For a power amplifier to operate efficiently a resistive load is presented to the device which minimizes overlap between voltage and current wave forms, and therefore dissipated power. Increasing the efficiency comes at the expense of lowering the linearity, as

harmonic tones are generated through clipping of the output waveform. Figure 2.2 shows an illustration of the conduction angle of the different classes from A to C. Lowering the gate bias below pinch off results in clipping of wave forms and reduced conduction angle.

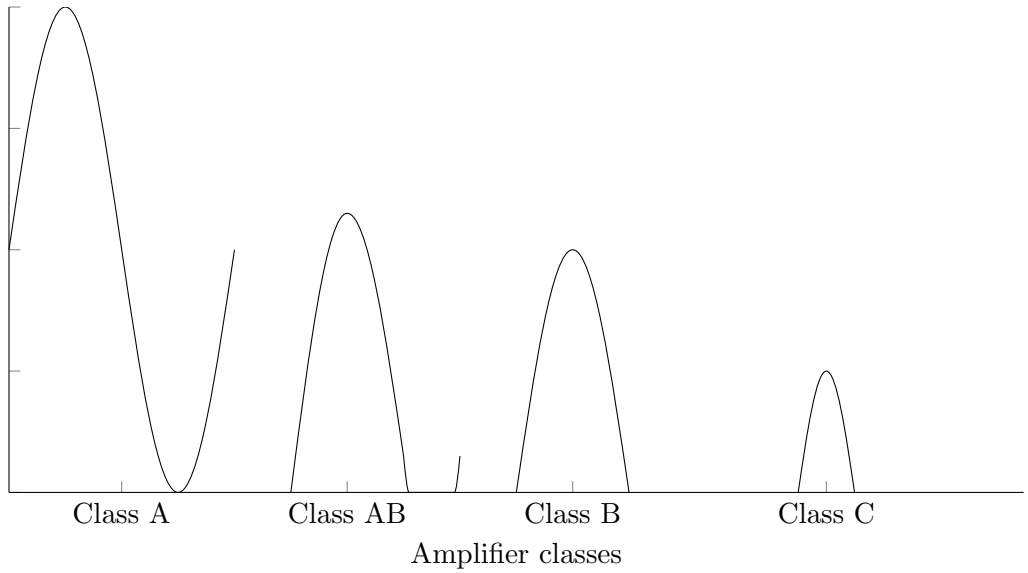



Figure 2.2: Illustration of amplifier classes based on conduction angle $\alpha$. Conduction angles correspond to Table

## 2.4 Efficiency

The efficiency of an amplifier is a metric that relates fundamental output power to the DC power delivered to the transistor. Two different forms of efficiency are commonly used which are drain efficiency ($\eta_D$) and power added efficiency (PAE). Power added efficiency is more descriptive and usually preferred as it includes the power in the input signal and therefore the gain of the amplifier. Both metrics are usually represented in percentage, and definitions are shown below.

$$\eta_D = \frac{P_{out}(f_o)}{P_{DC}} \tag{2.9}$$

$$PAE = \frac{P_{out}(f_o) - P_{in}(f_o)}{P_{DC}} = (1 - \frac{1}{G})\eta_D \tag{2.10}$$

## 2.5 Class F and inverse class F

A class F amplifier utilizes waveform shaping to create a square voltage waveform and half rectified current waveform at the output. This specific case of waveform shaping is done to minimize the overlap between positive current- and voltage curves within the transistor, effectively reducing dissipated power. The waveform shaping is done through presenting the appropriate impedance termination for harmonic frequencies at the output. In the case of class F a short circuit termination is presented to the even harmonic frequencies, and an open circuit for the odd harmonic frequencies. Inverse class F or class $F^{-1}$ is the inverse of class F, where the perceived

terminations are reversed. Another important result from squaring the voltage waveform is that the fundamental amplitude may increase, subsequently achieving higher output power [6].

To create an ideal class F amplifier sufficient power has to be attributed to the different harmonics to produce an ideal square wave. In theory a square wave is formed of an infinite amount of odd harmonic sinusoids with specific magnitudes as the orders increase. For practical class F implementations it is common to consider harmonics up to the third or fifth order, since harmonics of higher order contribute less to the waveform shaping. In a real life implementation the perfect impedance can not be achieved for several multiples of the fundamental frequency. This is primarily contributed to the permittivity of the materials used, which are frequency dependant. Figure 2.3 shows basic configuration of a class F topology. An LC network reflects third harmonic back to the transistor while a resonant tank provides a short circuit for all frequency other than the fundamental.

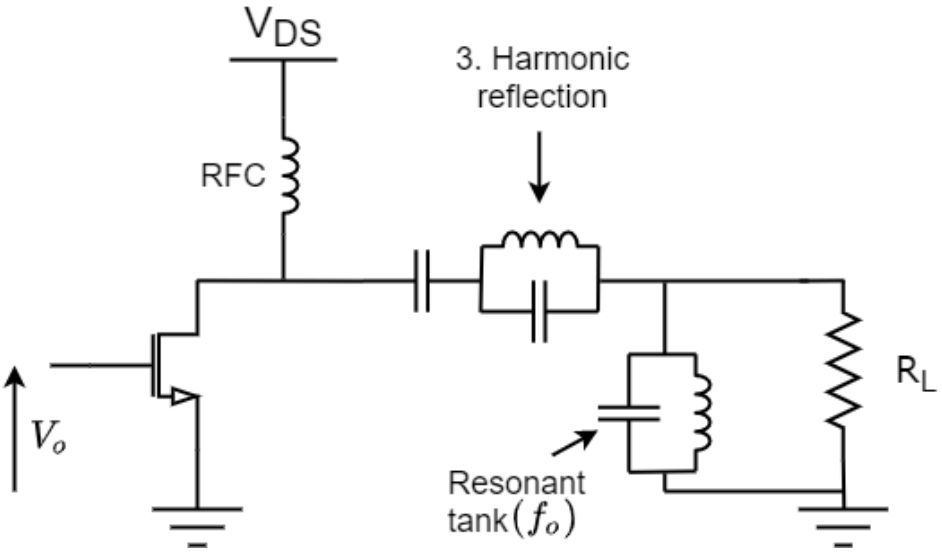



Figure 2.3: Basic configuration of class F amplifier topology [9].

Creating proper terminations for harmonic frequencies needs to be accommodated with exact magnitudes of the harmonic tones. In order to generate harmonics the class F amplifier is driven into saturation, and harmonics are generated through gain compression. Class F amplifiers are typically developed from class B or deep class AB amplifiers [6].

The ideal efficiency of a class F amplifier range from 50% such as the class A, to 100% as the number of harmonics increases [6] .

## 2.6 Linearity

An RF power amplifier has the task of boosting an input signal through delivered DC power. Total input and output power has to obey energy conservation, which implies output power is limited by the provided DC power. Because of this limitation compression occurs at high input signal level, i.e. the gain is reduced and non-linear amplification is the result.

An amplifier can be described by a non-linear device with a given gain. The output of this amplifier can further be modelled by a Taylor series where the output signal is a product of the

input signal as shown in Equation 2.11[7, p. 511-519].

$$v_o = a_0 + a_1 v_i + a_2 v_i^2 + a_3 v_i^3 + ..., \tag{2.11}$$

The terms of Equation 2.11 usually represents a combination of different effects in the non-linear device. Examples range from gain harmonic generation, compression, intermodulation, spectral regrowth and others [7, p. 511].

By applying Equation 2.11 to a sinusoid containing a single frequency the resulting output is shown in Equation 2.12, only containing up to third order terms.

$$v_o = (a_0 + \frac{1}{2}a_2 v_0^2) + (a_1 V_0^2 + \frac{3}{4}a_3 V_0^3)cos\omega_0 t + \frac{1}{2}a_2 V_0^2 cos2\omega_0 t + \frac{1}{4}a_3 V_0^3 cos3\omega_0 t + ..., \tag{2.12}$$

Equation 2.12 states that a single frequency input results in an output signal containing multiple frequencies. For an input containing $f_0$ the output will in general consist of harmonics of the fundamental frequency $nf_0$, where $n = 0, 1, 2, ...$ For an amplifier this property leads to distortion and signal loss in the $f_0$ tone. Harmonic components are generally increased when entering the saturation region of the transistor.

## 2.7 Intermodulation

When considering more useful signals this issue of linearity becomes more complex when multiple closely spaced frequencies are applied. An input signal on the form $v_i = V_0(cos\omega_1 t + cos\omega_2 t)$ will result in intermodulation products of frequency $m\omega_1 + n\omega 2$ where $m, n = 0, \pm 1, \pm 2, \pm 3, ....$ A typical output spectrum from a two tone input signal is shown in Figure 2.4[7, p. 515].

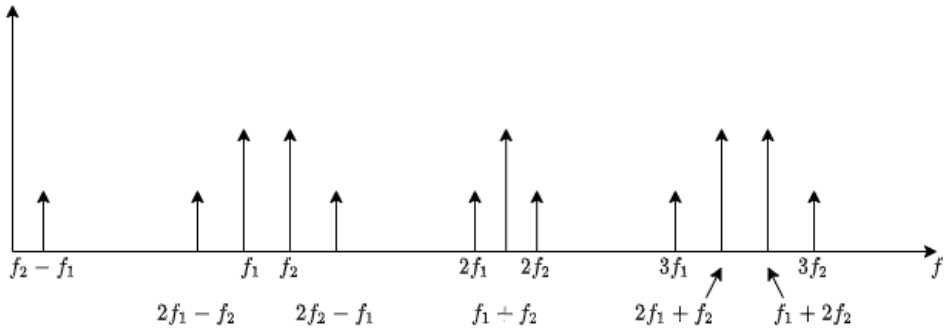



Figure 2.4: Output spectrum of second- and third order intermodulation products if $f_2 > f_1$ [7, p. 515].

Equation 2.13 shows the same Taylor series expansion as Equation 2.11 with a two tone input signal. The voltage increase at the input results in second harmonic voltages increasing by $V_0^2$ and third harmonic voltages by $V_0^3$ respectively. The implications of Equation 2.13 is that the harmonic products will become more dominant with higher input power.

$$v_o = a_0 + a_1 v_0^2(cos\omega_1 t + cos\omega_2 t) + a_2 V_0^2(cos\omega_1 t + cos\omega_2 t)^2 + a_3 V_0^3(cos\omega_1 t + cos\omega_2 t)^3 + ... \tag{2.13}$$

## 2.8 Load Pull

A power amplifiers output power, gain, linearity and efficiency performance is attributed to the dynamic loadline of the transistor. The dynamic load line is defined by the impedance perceived at the output of the active device.

Load pull measurements are used in order to measure the performance of an active device given a specified load impedance. By tuning the impedance the performance of the active device can be measured at different load impedances for different frequencies. Load pull measurements are commonly used in RFPA design in order to find optimal load impedance values.

## 2.9 Peak-to-average power ratio

Peak-to-average power ratio is a metric which provides a relation between the maximum instantaneous power and average power required to transmit various RF signals. PAPR is useful for analyzing RF signals which are not of constant amplitude, which is the case in most modulation schemes where data rate is important.

The effect of PAPR on a power amplifier is that it provides additional requirements on the PA. Efficiency and linearity are non-linear effects which vary depending on the power level presented to the PA. As such the performance of a PA varies depending on the level of output power back-off (OPBO).

# Chapter 3

# Design methodology

In this section the design procedure for creating a PA output network and three separate input networks is explained. The input network revisions are referred to as Rev 1, 2.0 and 2.1. Software used for circuit design and simulations is Keysight ADS (Advanced Design System). The transistor used in the design is CG2H40010F from Wolfspeed/Cree.

## 3.1 Design Considerations

The main goal of this thesis is to explore a technique for linearity enhancement in non-linear efficient power amplifiers by input tuning. In order to have a high impact on linearity an inverse class F amplifier topology is deployed as the main building block because of its inherent nonlinear nature. With this topology more harmonic distortion is generated and harmonic tuning of the input is applied in order to reduce the overall effect of the distortion. The inverse class F amplifier is chosen over the classic class F amplifier because of documented performance increase in comparison to class F [3] . The design goal is to match the characteristics of a class $F^{-1}$ amplifier, not necessarily create a class $F^{-1}$ by definition.

In order to design a class F amplifier the transistor needs to operate within deep saturation. Typically class AB is set as the biasing condition when constructing a class F or inverse class F amplifier section 2.5. In output power backoff (OPBO) the transistor will approach class AB performance, because the harmonic components creating class $F/F^{-1}$ operation are no longer generated. Operating the amplifier in OPBO may reduce the overall impact of the linearization technique as the unwanted components are smaller in back off. While the linearization effect should reach its maximum in deep saturation, the main results are gathered around 6 dB backoff. The decision to accumulate results around 6 dB backoff is made because it is a common level for PAPR in modulated signals, and lessen constraints of the PA.

Specifications for the PA is shown in Table 3.1. Pout, gain, efficiency and linearity are important parameters. A bandwidth of 200 MHz is set as a goal in the design procedure but is not crucial to explore the linearization technique. The bandwidth of the technique will however be an interesting result in itself.

Table 3.1: Design specifications for the amplifier design.

| Parameter | Goal |
|---|---|
| Fundamental frequency | 2.4 GHz |
| Smallsignal BW | 200 MHz |
| Small signal gain | $> 14$ dB |
| Ripple in band | $< 1$dB |
| S11 | $< -10$ dB |
| Saturated output power | $> 41$ dBm |
| Efficiency | maximize |
| Linearity | maximize |

The output network is designed with maximum power added efficiency as the main goal, while maintaning 41 dBm output power. Three separate input networks are designed with three separate mind sets. The first network is designed to achieve high gain and an overall efficient topology. The second network is designed to increase linearity while maintaining the gain. The last network is designed to maximize linearity at the expense of gain while still maintaining over 15 dB power gain before saturation.

## 3.2 Linearization technique principle

Striving for efficiency and linearity has historically been a driving force for RF power amplifier design. Many different topologies have been developed such as Doherty in order to increase efficiency and linearity. Examples are Doherty topology, envelope tracking and pre-distortion [6]. Down to its core the basic principle is using non-linear properties of a transistor to reduce non-linear components at the output of the amplifier by input tuning.

Figure 3.1 illustrates the implementation of the technique on a power amplifier with corresponding spectrums. For illustration purposes a two tone signal is shown at the input of the device. The two tone signal is amplified by the transistor, which produces harmonic tones according to Equation 2.13 (Signal amplitudes are not to scale). For simplicity the illustration only contains second harmonic intermodulation products, but in reality there will be theoretically an infinite amount. Only up to third order will be considered while designing the networks, as the magnitude of IMD products falls off dramatically with harmonic order.

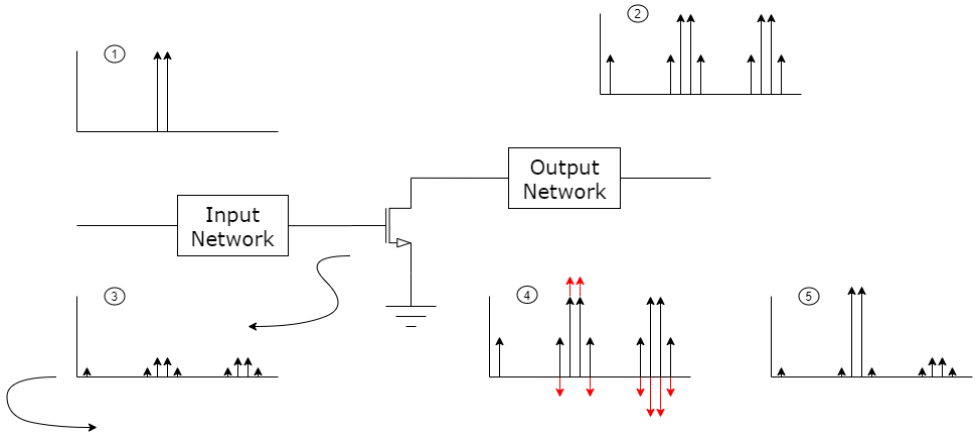



Figure 3.1: Working principle of the proposed technique (amplitudes not to scale).

In the illustration of Figure 3.1 input spectrum 1 is fed to the input of the amplifier. Non-linear properties in the transistor produces output spectrum 2. Some proportion of this output spectrum is leaked out on the gate side of the transistor. At this point the total input spectrum is a combination of 1 and 3. The non-linear components are reflected back at the transistor while the phase of second and third harmonic is altered by the input network. Spectrum 4 shows an ideal scenario where the intermodulation products from spectrum 2 and spectrum 3 are summed in counter phase. Given that the products are in counterphase and of similar amplitude the total output spectrum is shown in spectrum 5 of Figure 3.1, and the result is a more linear amplifier. An ideal scenario is one where the IMD products are completely eliminated, however in practice a reduction of a few decibels is more feasible.

### 3.2.1 Challenges

A transistor will usually be tuned to work within a specified bandwidth, where the second and third harmonics will be located far outside said bandwidth. Amplification of harmonic content is thus reduced compared to the fundamental frequency ($f_0$). Power leaking out from the transistor on the gate side will be of relatively small magnitude, as it is created by a small portion of the fundamental tone. Furthermore full elimination would only work at one discrete frequency at a singular input power considering ideal circumstances. Because of these constraints the goal is not to eliminate harmonics, but rather reducing the power of IMD products through harmonic phase tuning.

Bandwidth limitations may be a severely limiting factor. A given bandwidth at the fundamental frequency $BW_{f0}$ will correspond to $2 \cdot BW_{f0}$ and $3 \cdot BW_{f0}$ for the second and third harmonic respectively. Matching the optimal impedance within all specified frequency ranges increases the complexity dramatically.

Because the intermodulation products are used as a tool to eliminate IMD products, there is also a concern with the dynamic range of the technique. The exact amount of harmonics required may be generated at a specific output power, but in output power backoff (OPBO) the components may change in amplitude and phase thus decreasing the linearization effect. Signals with high PAPR highlight this issue.

A concern was raised regarding the additional delay introduced because of the physical length the signal needs to travel by reflection, after which it is summed at the output. Because a real RF signal is not sampled until it approaches a steady state this is not an issue.

The main reason this technique may be of interest is that it can potentially increase the linearity of a power amplifier with no external circuitry added to the amplifier. While digital solutions for increased linearity are widely used, they have one fundamental flaw. In order to increase the linearity power has to be added in the form of processing power and external signal generators. The only drawback of this passive technique is adding complexity to the circuitry. No additional power requirement means the overall efficiency is not degraded, while linearity may increase. Another drawback is that the technique may not work very well throughout large dynamic ranges and bandwidths.

## 3.3 Similar techniques

Harmonic injection employs a similar strategy with one important distinction, additional power is injected into the circuit. A harmonic injection power amplifier (HIPA) is usually constructed by two separate PAs in parallel. The main PA provides fundamental power, while the auxiliary PA injects harmonic power to the output of the main PA [4, 2]. HI is thus an active technique for waveform shaping. By injecting a signal at the drain side of the main amplifier it is possible to emulate any desired load impedance seen by the transistor, thereby tuning the load. An example is creating a virtual harmonic short circuit termination which may be problematic because of gain compression. Figure 3.2 illustrates a topology which may be used to create a HIPA.

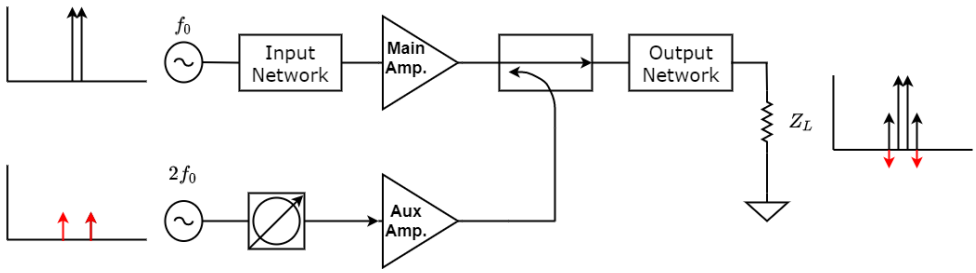



Figure 3.2: Example topology used for harmonic injection in order to reduce $IMD_3$ and increase efficiency [5]

The class F amplifier is an amplifier topology which already benefits from waveform shaping. By terminating odd harmonics with an open circuit and even harmonics with a short circuit 100% efficiency is possible to achieve in theory. In reality reflecting harmonics with the perfect amplitude and phase proves difficult, and is usually done up to the third or fifth harmonic in practice. By utilizing HI it is possible to inject odd harmonics to create the desired class F characteristics by injection instead of tuning the harmonic output terminations. Several studies have been done on harmonic injection, and main PA PAE increases are well documented [**boulder**, 4, 5, 11, 2].

This principle can work the same way with linearity, where a signal can be injected in order to emulate the appropriate impedance to increase linearity. Studies show that active harmonic injection on input to reduce $IMD_3$ is achievable [1].

## 3.4 Substrate

Initially Rogers 3006 is chosen for the design. Rogers 3006 has low dielectric loss tangent of 0.002 and a high permittivity of 6.15. Low loss will directly contribute to the efficiency, which is important to maintain especially in power amplifiers. Having a high permittivity facilitates more compact designs, as the wavelengths are reduced. Compact design may again contribute to lower loss, as the signal path is shorter. Due to shut down on campus related to Covid-19 the design later had to be reworked to FR4. FR4 is chosen to minimize the fabrication time as it is a widely used substrate. With a permittivity of 4.4 all components have to be tweaked slightly to match the new permittivity, and dimensions are increased. FR4 introduces a higher dielectric loss tangent of 0.02 which corresponds to slightly more loss in the circuit.

## 3.5 Biasing of the transistor

Determining the bias conditions of the transistor is done through sweeping the parameters $V_{GS}$ and $V_{DS}$. The resulting I-V characteristics allows choosing a proper biasing condition to meet certain requirements. As this design is initially based on a class F amplifier, the transistor is biased to meet class AB characteristics.

Setting the bias voltages $V_{DS} = 28V$ and $V_{GS} = -2.8V$ produces the bias current $I_{DS} = 105mA$ and achieves deep class AB biasing conditions.

## 3.6 Stability

A power amplifier should in general be designed to meet requirements of unconditional stability as mentioned in section 2.2, to prevent oscillations from occuring. Loss is introduced to the circuit to counteract oscillations which in essence are defined as negative resistance.

A stabilization component is added on the gate side of the transistor through a parallel network of a capacitor and resistor creating a high pass network as shown in Figure 3.3. The resistor provides loss at lower frequencies when the capacitor acts as an open circuit. A small capacitor is added in parallel in order to minimize loss at higher frequencies. Stabilization components are tuned until unconditional stability is achieved through simulations.

An additional 10 Ohm resistor is added in the gate biasing network to provide further stability.

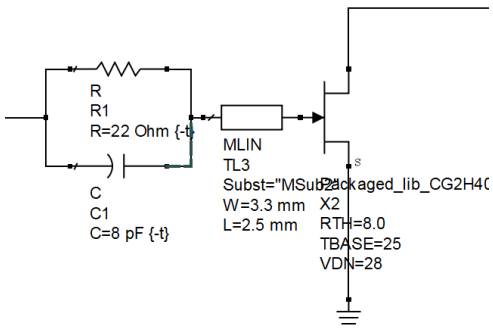



Figure 3.3: Working principle of the presented technique (amplitudes not to scale).

## 3.7 Biasing networks

Introducing real components in the biasing networks will have an impact on the performance of the amplifier. Biasing networks are generated early in the design process, and will act as parts of the input- and output networks.

As harmonics of the fundamental frequency are to be utilized further the goal for the bias network is to act as an open circuit for all harmonic frequencies.

The bias networks are shown in Appendix A and **??** in the design. The same biasing network is

used on gate and drain side of the transistor, with an exception of an additional microstrip line on the gate side to meet dimension requirements.

## 3.8 Output network

A load pull analysis is performed in order to find optimal reflection coefficients or target impedances for the output network. This design approach allows the network to be generated by S-parameters, as the process is made passive in its entirety. The main benefit of creating a passive problem is that simulations can be performed at a much higher rate. A sensitivity analysis is performed in order to set target impedance goals, as perfect match may be hard to achieve in practice.

In order to create a compact design the network is made as simple as possible. A simple design will reduce chances for large discrepancies between simulations and the physical circuit by minimizing the amount of variables.

### 3.8.1 Load pull

To achieve inverse class F operation the output network needs to accommodate proper impedance terminations for harmonic frequencies. Even harmonics should experience a short circuit, while odd harmonics experience an open circuit. In practical design these conditions are hard to achieve, and compromises must be done. Ideally all harmonics up to $\infty$ should be considered, however in practical design going higher than the third or fifth harmonic usually does more harm than good.

The target impedance of the output network is generated through a load pull analysis. Load pull analysis' are performed in ADS through a component created by Morten Olavsbråten that allows an impedance of a specified frequency to be set independently. Optimal load impedance for the transistor can therefore be found for all frequencies, and be used to create a network with said load impedance. Figure 3.4 shows the ADS implementation of the procedure. Input power is set to 27 dBm to ensure that the transistor operates within deep saturation (3 dB compression). By sweeping the reflection coefficients for fundamental and harmonic frequencies up to third order optimal loads are found. The main goal through this procedure is to maximize the PAE with the given input power of 27 dBm, while keeping the fundamental output power above 41 dBm. To further maximize the PAE an optimization procedure is done in ADS. The load pull analysis is performed with ideal components and a microstrip line of characteristic impedance 50Ω for the fundamental frequency. Because the transmission line is tuned to 50Ω it has minimal impact on the fundamental output power, and is later used to adjust the dimensions of the total circuit.

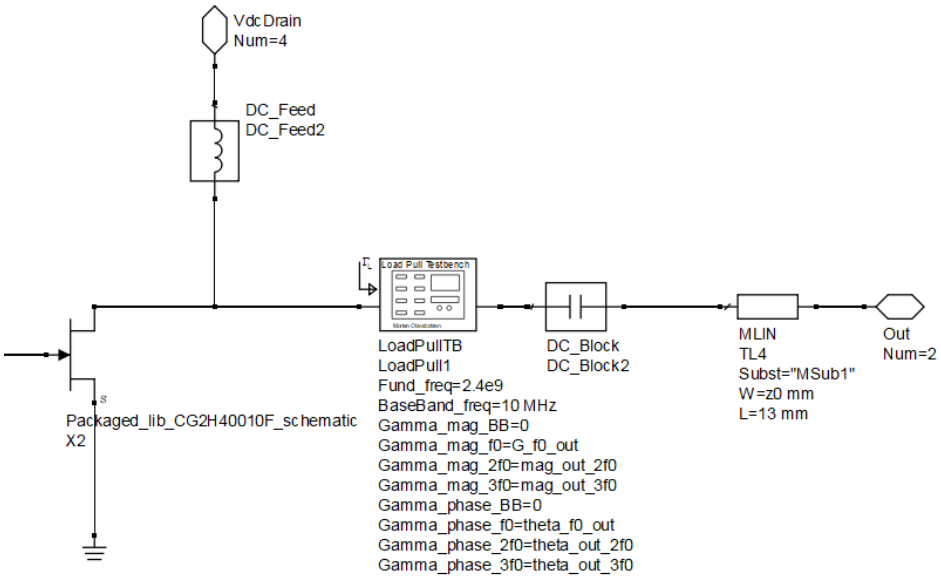



Figure 3.4: ADS setup of the initial load pull procedure.

### 3.8.2 Sensitivity Analysis

To achieve an optimal output network all impedances within the passband have to match those of the optimal load. For this design that means perfect impedance match within $2.4\,GHz$ or $f_0 \pm 100MHz$, $2f_0 \pm 200\,MHz$ and $3f_0 \pm 300MHz$. Achieving perfect match for all frequencies is simply not possible in practical design. A sensitivity analysis is deployed in order to find suitable impedance values which degrades the performance a minimal amount with respect to efficiency and output power. The sensitivity analysis procedure is based on paper by Morten Olavsbråten Et al [10]. Figure 3.5 shows how changing impedance values impacts the PAE and/or output power. From Figure 3.5 it is concluded that the fundamental and second harmonic impedance are of most importance. Mapping the sensitivity in this fashion makes it possible to set target impedances which remain within a limited area throughout the fundamental and harmonic passbands.

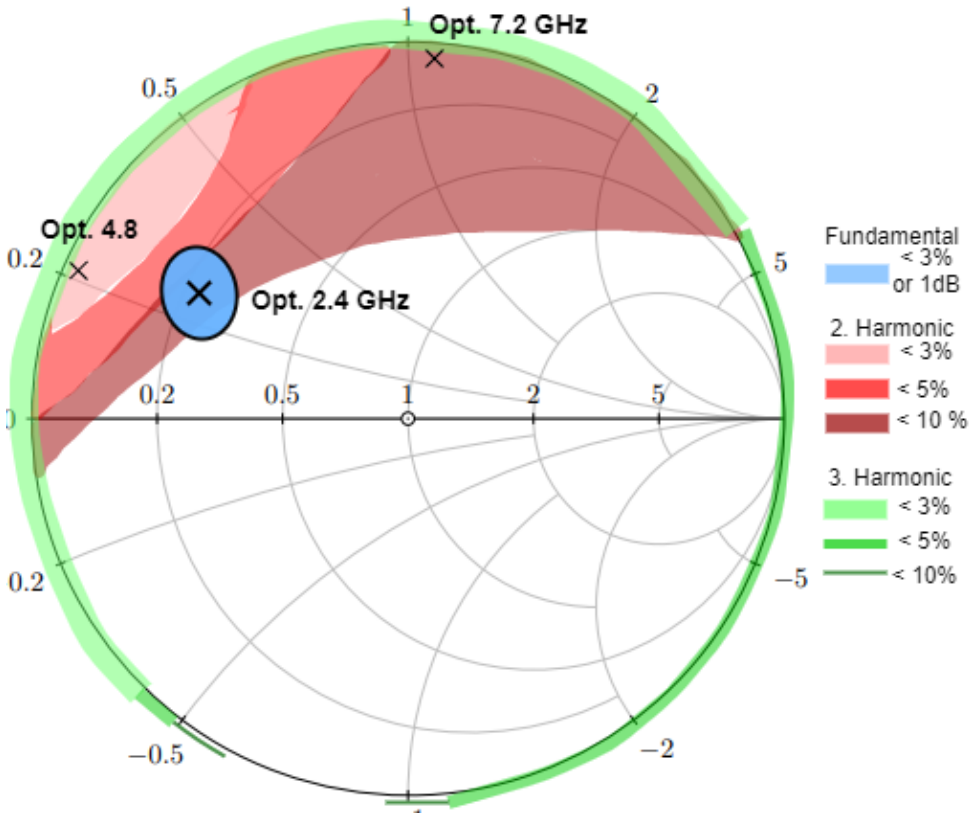



Figure 3.5: Output network sensititivy analysis. Fundamental tone represented by blue, second harmonic by red and third harmonic by green.

The contour for the fundamental frequency covers all impedances where output power is not degraded further than 1dB, or where PAE is not degraded more than 3 percent. Optimal impedance for the fundamental frequency is plotted with regards to PAE and output power. Second and third harmonic contours show the impedance range where a degradation of PAE does not exceed 3, 5 and 10 percent limits respectively. Adjusting the magnitude of the third harmonic is neglected as the magnitude will approach unity. An identical procedure is performed for the edges of the passband for fudamental, second and third harmonic.

An interesting observation is that the optimal impedances are located relatively close to each other. The Foster theorem states that the reactance of a two port network will increase with frequency [8]. A practical implication of the foster theorem is that multiple loops around the smith chart may be required to realize the network, as the reactance increases with frequency.

Another thing to note is the tolerance for the harmonics. As harmonic products increase the less relevance they have on the total output spectrum. This is in line with the theory of class F amplifiers, where the fundamental products have a progressively smaller impact. Optimizing for the third harmonic is therefore not prioritised, since sweeping the phase throughout the smith chart degrades the PAE marginally compared to the fundamental and second harmonic.

### 3.8.3 Optimal load impedance

The circuit performance is deemed sufficient when $82.5\%\, PAE$ is achieved with ideal components, and the output power level exceeds $41.5\, dBm$.

Waveforms on the drain side of the transistor is shown in Figure 3.6 and shows tendencies towards the inverse class F characteristics, although far from ideal. These reflection coefficients are the results found by ADS when maximizing for efficiency while maintaning a minimal output power of 41 dBm.

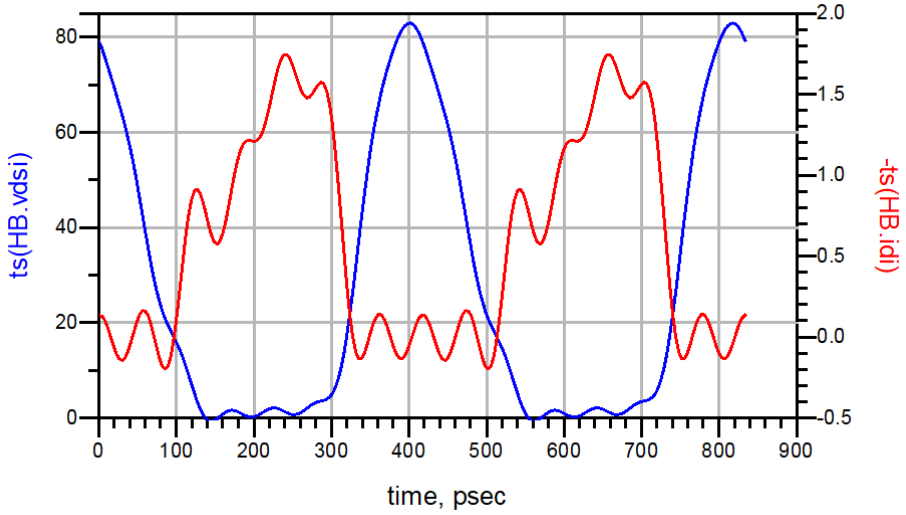



Figure 3.6: Voltage and current waveforms on drain side of transistor. Voltage (V) represented in blue, and current (A) represented in red.

### 3.8.4 Synthesizing output network

By extracting the S-parameters of the load pull component as seen in Figure 3.7 they can be used to create a physical output network. By using this approach the output design process becomes entirely passive. An output network can therefore be synthesized by matching the load pull components S-parameters at all frequencies.

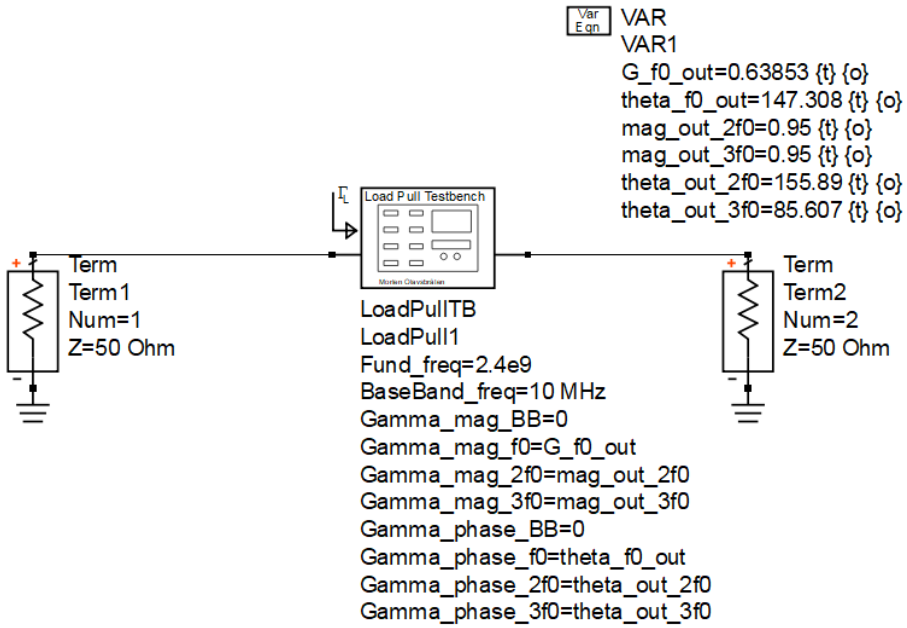



Figure 3.7: Testbench for extracting load pull S-parameters.

Running an S-parameter simulation of the circuit in Figure 3.7 generates the S-parameters illustrated in Figure 3.8. By using the sensitivity analysis results goals can be set in order to match a real output network as close to the ideal scenario. Maintaining the fundamental impedance within the contour of Figure 3.5 is given a high priority. In ADS this is done by letting the vector difference between $S_{11}$ or $S_{22}$ from the two scenarios be as close to 0 as possible ($S_{11} = S_{22}$ in passive networks, i.e. a reciprocal network), with higher priority in the center of the passband.

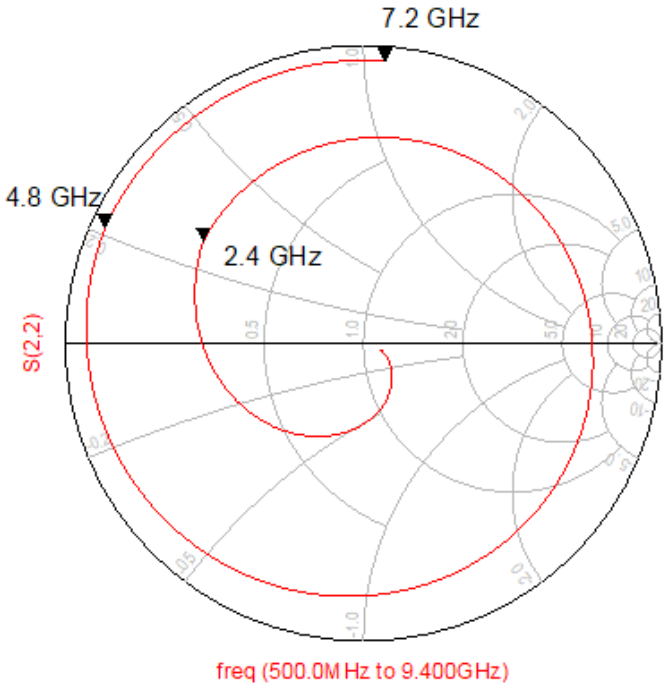



Figure 3.8: $S_22$ of the ideal output network. The network is passive and therefore reciprocal so that $S_{11} = S_{22}$.

An output network is synthesized by trying to mimic the performance of the load pull component as seen in Figure 3.8. As few components as possible is used for the output network, and the biasing network is included. The resulting network can be seen in Figure 3.9.

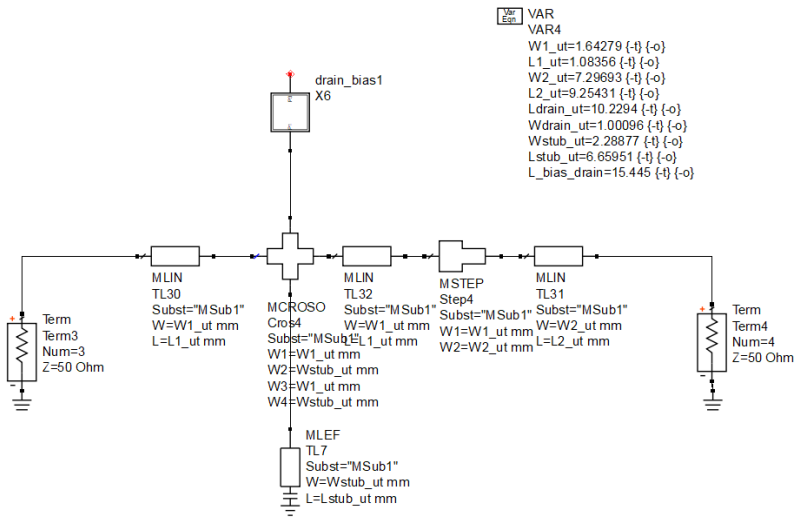



Figure 3.9: Real synthesized output network.

Placing the synthesized network at the output of the transistor yields a worse performance than predicted. An optimization sequence is performed in order to regain the desired PAE and output power performance. Figure 3.10 shows the $S_{22}$ of the completed output network after optimization. Comparing the results to the sensitivity analysis the fundamental and third

harmonic are within reasonable distance to the optimal values. However the second harmonic has drifted into an area which should result in 10% PAE degradation based on the sensitivity analysis. This is not the case, likely due to changes in the fundamental- and third harmonic impedance.

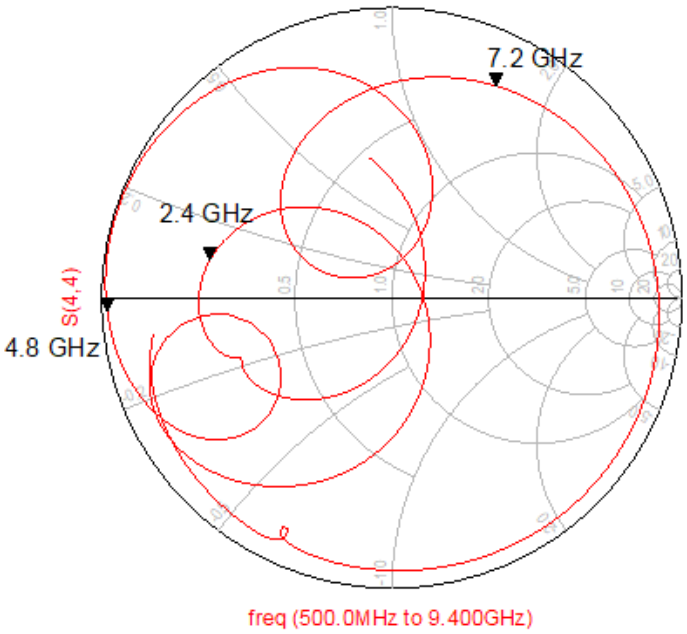



Figure 3.10: $S_{22}$ of the synthesized output network.

Tabell for å sammenlikne ideel performance vs reell, eller kurver?

### 3.8.5 Optimizing output network for efficiency

Designing the output network for optimal PAE is an ambiguous term. It is not specified at which output level the PAE should be optimized. A reasonable assumption would be to optimize the efficiency with regard to the peak output power, while another reasonable approach is optimizing for average output power.

16 bit QAM is briefly analyzed in order to justify the optimization parameters. Considering a 16 QAM signal there are 3 different states of different amplitudes. There are 4 symbols associated with the lowest discrete voltage, 8 with the medium voltage level and 4 with the highest voltage level, as can be seen in Figure 3.11. With no regard to the probability of the different symbols appearing, the sum of all probable vectors are $4\sqrt{1^2+1^2}+8\sqrt{3^2+1^2}+4\sqrt{3^2+3^2}$. Taking the power into account eliminates the square roots, which leads to the remaining sum $4\cdot(1^2+1^2)+8\cdot(3^2+1^2)+4\cdot(3^2+3^2)=160$.

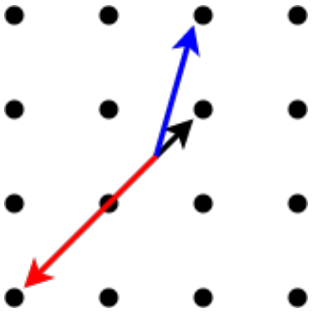


Figure 3.11: Possible vectors of a 16 bit QAM signal.

Figure 3.12 shows the resulting power distribution, where the mid and high states are clearly dominant. It is therefore considered reasonable to optimize toward either peak output power or average output power (at about 6 dB OPBO). Optimizing towards a point in between peak and average output power will likely yield an even better result with regards to efficiency, but is deemed unnecessary as it would be outside the scope of the thesis. For this design efficiency is maximized with an input power of 27 dBm which corresponds to close to peak output power.

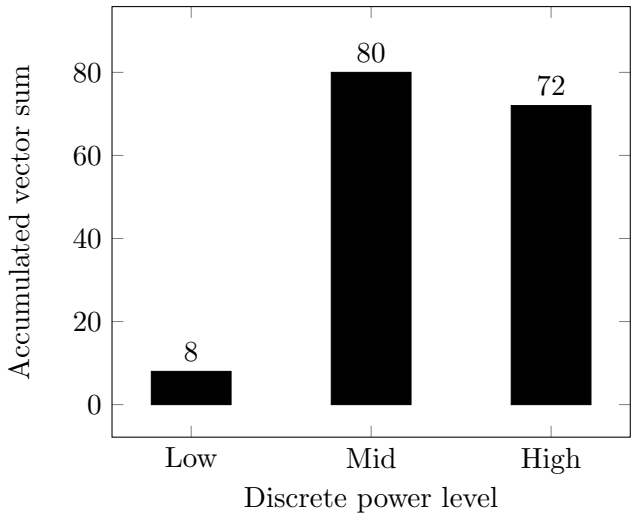



Figure 3.12: Power distribution in 16 bit QAM with equal probablility between all symbols.

## 3.9 Input Network - Revision 1.0

The main focus of this thesis is to look at the input network and utilize it for further linearization and/or increase in efficiency. Because the gain is essential in achieving a high PAE the initial input network is designed to yield a high gain. Matching the input to 50 Ω is nominal in order to achieve high gain. A simple conjugate match is therefore constructed for the input network, where the transistor impedance will be transformed to 50 ohms when looking at the input of the circuit. The input network is kept as simple and compact as possible, with a single stub as seen in Appendix B. No further considerations are made for the first revision of the input network, as this will be the reference design where maximum gain is emphasized. The bias network is the same as for the drain side of the transistor.

Figure 3.13 shows the return loss of the complete circuit containing both input and output networks with regards to output power. The return loss is fairly constant until the transistor

is driven into saturation, where an even better match is achieved. Maximum output power is achieved at 2.4 GHz and approaches 41.6 dBm with a peak efficiency of 76%.

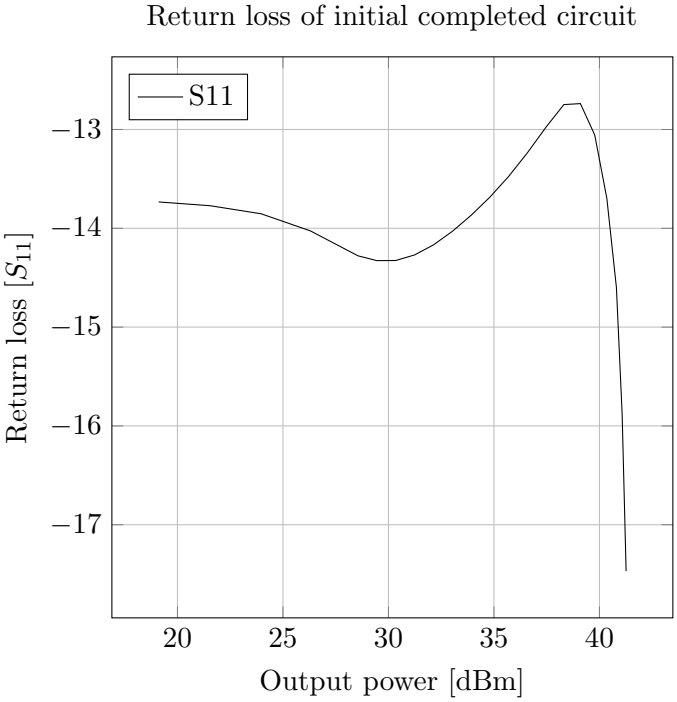



Figure 3.13: Return loss $S_{11}$ of completed initial circuit.

## 3.10 Input network iterations

The primary idea with further revisions is to utilize the harmonic tones generated by the transistor, which will leak out both at the input and output. These harmonic tones will then be reflected back at and fed through the transistor. Through careful tuning these tones could end up cancelling the harmonic products at the output, ideally resulting in a more linear amplifier. Another plausible outcome is adding power to the main tone, which could lead to an increase in efficiency. In order to achieve the above mentioned features the impedances of the input network needs to be tuned accordingly.

The following chapters will explain the design procedure in order to find the optimal source impedances to grant linearity improvements.

## 3.11 Input tuning - Revisions 2.0 and 2.1

In order to look at how phase tuning at the input affects the amplifier design two additional input networks are designed. Initially only one additional input network was planned, where the input phase tuning affecting linearity is analyzed. During the design procedure it is discovered that by introducing loss in the fundamental frequency the linearity could be further increased with the same output power level. Two revisions are planned where the first revision tries to maintain the magnitude of the fundamental reflection coefficients, $|\Gamma_{f0}|$, while only tuning $\Gamma_{2f0}$ and $\Gamma_{3f0}$. Rev 2.1 is free to change the fundamental impedance as long as 15 dB gain is achieved

with 35 dBm output power (roughly 6 dB OPBO). Output parameters to maintain while tuning for linearity are summarized in Table 3.2.

Table 3.2: Minimum amplifier specifications while tuning for linearity.

| **Parameter** | **Goal** |
|---|---|
| Gain @ 35 dBm $P_{out}$ | $>$ 15 dB |
| PAE @ 35 dBm $P_{out}$ | Maximize |
| Linearity | Maximize |

Stability circuits and biasing networks are duplicated across all input networks to minimize discrepancies due to changing components or layout.

Design of input networks with enhanced linearity (Rev 2.0 and Rev 2.1) is achieved by source pull analysis similar to the output procedure. By sweeping the second and third harmonic magnitude and phase the optimal impedance can be found with respect to linearity. In order to compare the improvements a weighted function is created which serves as a optimization parameter $P_{SumWeight}$. The parameter consist of the summed power in third order intermodulation products relative to the carrier tone at $6\,dB \pm 3\,dB$ backoff (32, 35 and 38 dBm $P_{out}$) in Watts. Samples in 9, 6 and 3 dB backoff are given weights of 1, 20 and 2 respectively. This circumvents the issue of severely dominant samples at high output power while emphasizing $P_{Avg}$ at around $35\,dBm$. Samples in deeper saturation are still relevant as the issue of linearity becomes more problematic with higher input power because of saturation. $P_{SumWeight}$ is defined below in Equation 3.1.

$$P_{SumWeight} = \frac{1}{23}(P_{3IMD(32dBm)} + 20 \cdot P_{3IMD(35dBm)} + 2 \cdot P_{3IMD(38dBm)}) \tag{3.1}$$

Revision 2.0 looks at how only changing the phase of fundamental and harmonic frequencies affects the amplifier output linearity. In ADS the source pull component allows all other parameters to be kept constant while adjusting the phase of specific frequencies independently. Optimal parameters are found by utilizing the weighted optimization parameter $P_{Sum,Weight}$. The source pull results can further be utilized to synthesize a real network by generating a network with the same S-parameters as already performed with the output network.

A two tone test is setup in order to observe the performance of the amplifier with regards to linearity. Figure 3.14 shows how the linearity is affected while changing $\Gamma$ of the input network. Simulated linearity of Rev 2.0 (black) may be compared to with the initial coefficients (red) for comparison. Another intermediate set of coefficients is plotted (blue) where the fundamental magnitude and phase is kept constant.

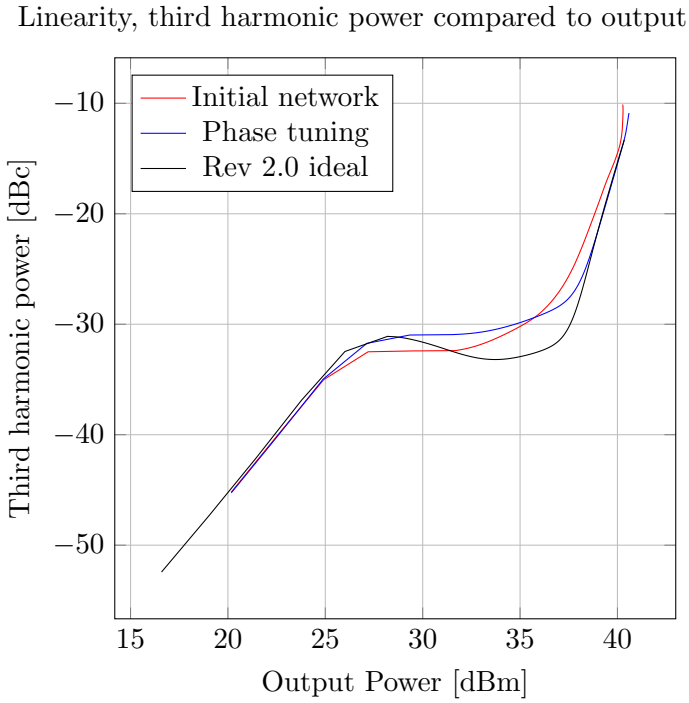



Figure 3.14: Linearity improvements from phase tuning
Linearity improvements from phase tuning. The initial network is represented in red, the blue graph is generated through only changing phase on 2. and 3. harmonic reflection coefficients, while the last black graph represents impedance tuning in fundamental, 2. and 3. harmonic.

Table 3.3 shows the corresponding reflection coefficients of the input network in order to produce Figure 3.14.

Table 3.3: Optimal reflection coefficients for linearity.

| **Frequency** | $\Gamma_{Init}$ | $\Gamma_{Rev2}$ |
|---|---|---|
| $2.4\,GHz$ | $0.836\angle -169.08$ | $0.836\angle -141.5$ |
| $4.8\,GHz$ | $0.871\angle 128.73$ | $0.837\angle -90.3$ |
| $7.2\,GHz$ | $0.95\angle 67.98$ | $0.905\angle 80.4$ |

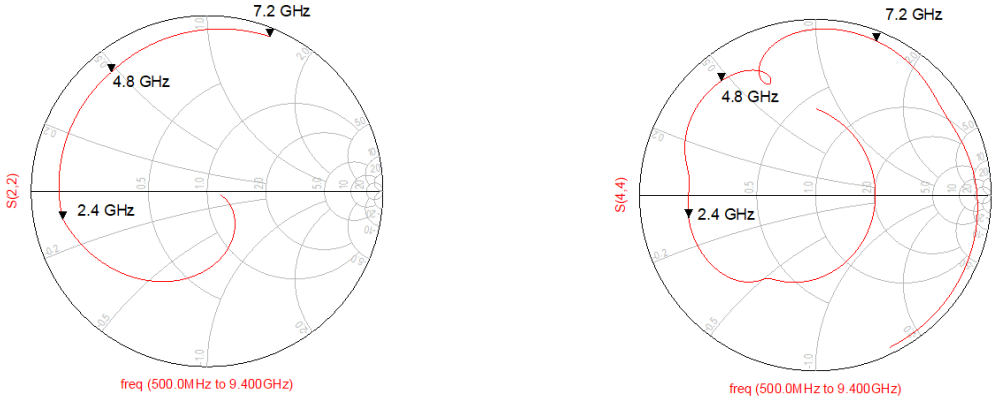
From observing Figure 3.14 only changing the phase of second and third harmonics has an impact on the linearity, but only slight. After surpassing 35 dBm output power there is a clear improvement in linearity compared to no tuning. While the improvement is not astounding this could yield a higher dynamic range for the device. Slight tuning of the fundamental phase has a much larger impact on linearity than only tuning phase. A dip is created around the average output power of 35 dBm, and the linearity is enhanced substantially when higher output power is generated.

A third revision (rev 2.1) is designed where the magnitude of $\Gamma_f 0$ is also changed, as simulation results indicated large impact on linearity by increasing the return loss. The design procedure is done with the same source pull method with $P_{Sum,Weight}$ as the main optimization parameter.

Changing the magnitude of $\Gamma_{f0}$ lowers the gain of the transistor by transforming the input impedance away from $50\Omega$ and lowering $S_{11}$. Lowering $S_{11}$ should have an impact on distortion compression and therefore 3IMD, as the device will enter saturation at a higher input level.

### 3.11.1 Synthesizing the input networks

A similar procedure is carried out when synthesizing the input networks as is done with the output network. S-parameters are extracted from the ideal reflection coefficients and a real network is synthesized and placed in the circuit at the location of the source pull component. Figure 3.15 shows S-parameters of both ideal source pull component and the synthesized network from the initial design. This procedure is duplicated for revisions 2.0 and 2.1.




(a) $S_{22}$ generated from source pull

(b) $S_{22}$ of real synthesized network

Figure 3.15: Comparison of $S_{22}$ by ideal source pull component and real input matching network.

Perfect match is hard to achieve, and introducing loops are necessary in order to match the optimal impedance for the third harmonic.

Total schematics are included in **??**.

## 3.12 Initial layout

Complete layout of the output network and initial input network is shown in Figure 3.16. The substrate used for the first layout is Rogers 3006, and the manufacturing process is done at NTNU Gløshaugen. Manufacturing of the initial layout is done right before lockdown due to Covid-19.

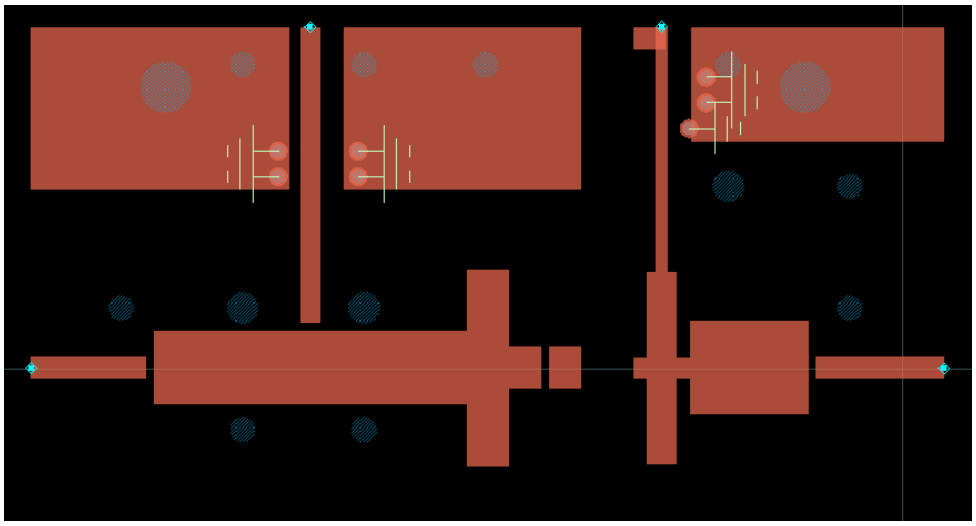


Figure 3.16: Layout of input and output network in Rogers 3006

## 3.13 Revised layout

Because of the outbreak of Covid-19 revisions could not be manufactured with Rogers 3006. A rework of the initial input network had to be created by using FR4 instead of Rogers 3006. Figure 3.17 is the result of all three input networks on the same substrate. The output network from Figure 3.16 in Rogers 3006 is still used, as input and output networks were separated in the manufacturing process.

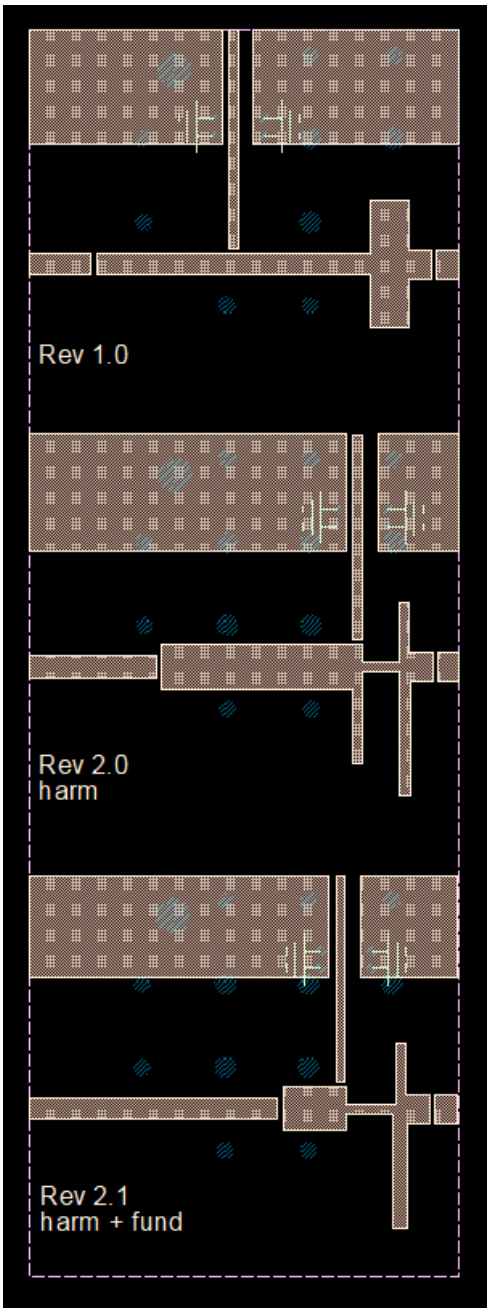



Figure 3.17: Triple layout of input networks on same substrate

# Chapter 4

# Simulation results

In this section the simulation performance of the three circuits will be presented. The metrics PAE, linearity and gain will create a reference for measurements on the physical circuits. The same output network is used for all measurements.

## 4.1 Small signal gain - $S_{21}$

The small signal gain is presented in Figure 4.1.

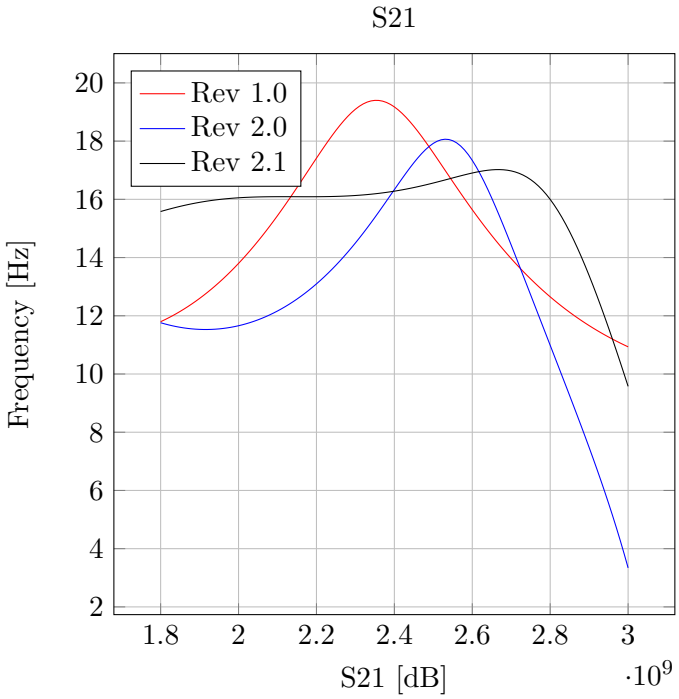



Figure 4.1: Simulated small signal gain - $S_{21}$.

The goal of 200 MHz bandwidth is barely achieved for Rev 1.0, although at center frequency

2.35 GHz. Revisions 2.0 has its center frequency drifted to 2.53 GHz with a smaller bandwidth.

Revision 2.1 as drifted even further away from the target center frequency with a peak at 2.67 GHz. An interesting observation is the flat gain achieved in revision 2.1, which corresponds to a $< 1dB$ ripple bandwidth of 820 MHz.

S-parameters were not emphasized when optimizing towards linearity, which explain the drift in center frequency.

## 4.2 One tone simulation results

Presented one tone simulations are performed with 27 dBm input at 2.4 GHz.

### 4.2.1 Pout

The simulated output power curves are similar for the three cases, however revisions 1 shows higher output power before compression at the same input levels, which can be attributed to gain.

Simulated output power of all completed circuits in FR4

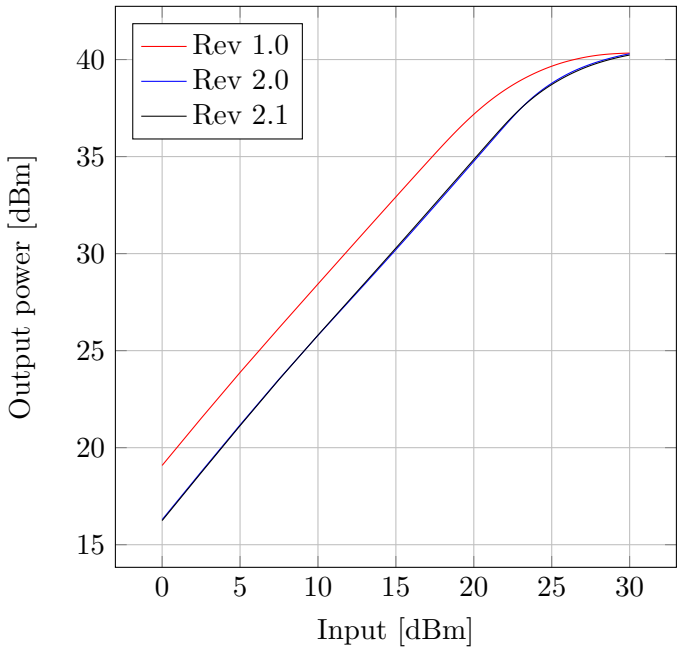



Figure 4.2: Simulated Output power

### 4.2.2 Gain

The subsequent revisions have a large drop in gain which is observed in Figure 4.3. When designing these the goal was to have revision 2 with close to the same gain as revision 1.

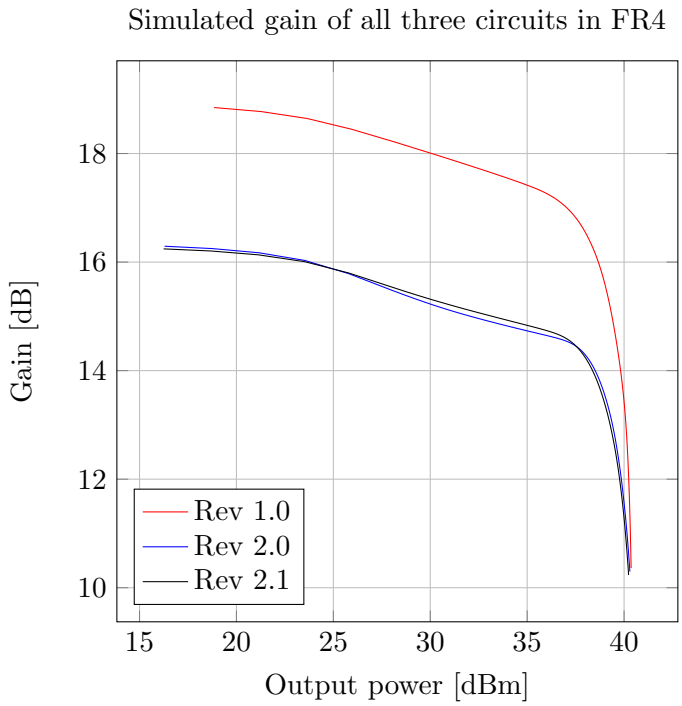



Figure 4.3: Gain of all completed circuits in FR4

### 4.2.3 PAE

The power added efficiency is very similar for all circuits, and approaches 70 % peak efficiency. Revisions 2.0 and 2.1 achieve slightly higher PAE than the revision 1.0. The similarities between the designs are likely caused by having similar goals when optimizing.

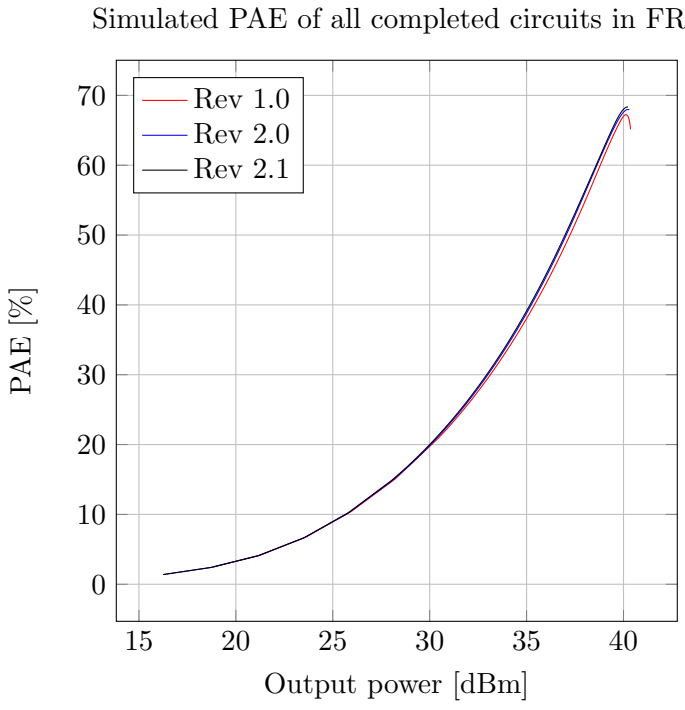



Figure 4.4: PAE of all completed circuits in FR4.

## 4.3 Two tone simulation - Linearity

Later revisions with an emphasis on linearity is clearly shown in Figure 4.5, where a dip is created centered around 35 dBm output power.

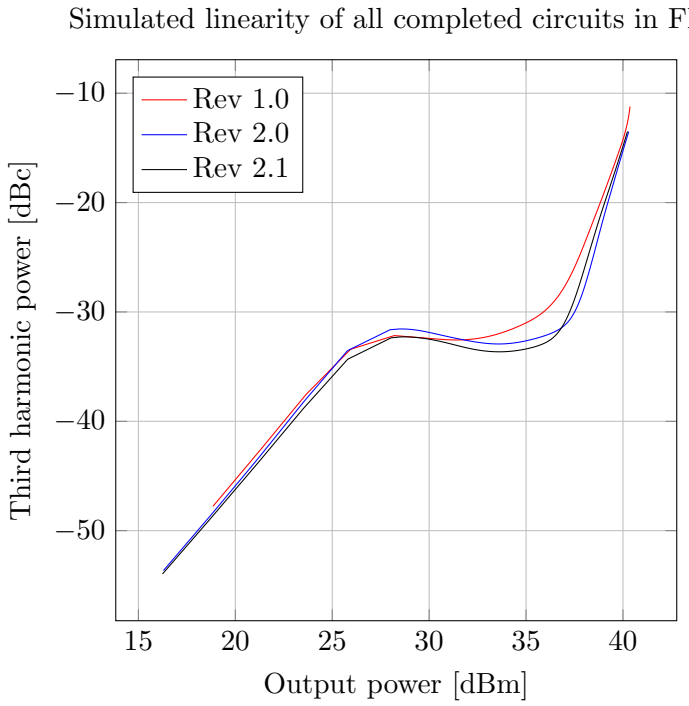



Figure 4.5: Power in third harmonic [dBc]

## 4.4 Simulation results improvements

Performances of all three input network revisions are summarized in Table 4.1. All results are measured with 41 dBm fundamental output power.

Linearity performances from the two tone tests are shown in Table 4.2. The metric used to indicate linearity is power in third order intermodulation products relative to the fundamental power in dBc at various output power levels.

Table 4.1: Simulated one tone performance for frequencies 2.3-2.5 GHz in increments of 50 MHz. 41 dBm is not achieved at 2.5 GHz for revision 1.0.

| **Freq.** | $P_{out}$ | **PAE** | **Gain** |
|---|---|---|---|
| Rev 1.0 @2.3 $GHz$ | 41.00 dBm | 62.68 % | 16.00 dB |
| Rev 2.0 @2.3 $GHz$ | 41.00 dBm | 62.77 % | 11.05 dB |
| Rev 2.1 @2.3 $GHz$ | 41.00 dBm | 63.20 % | 12.90 dB |
| Rev 1.0 @2.35 $GHz$ | 41.02 dBm | 68.58 % | 16.02 dB |
| Rev 2.0 @2.35 $GHz$ | 41.00 dBm | 70.30 % | 12.00 dB |
| Rev 2.1 @2.35 $GHz$ | 41.00 dBm | 69.69 % | 13.25 dB |
| Rev 1.0 @2.4 $GHz$ | 41.01 dBm | 74.18 % | 15.31 dB |
| Rev 2.0 @2.4 $GHz$ | 41.01 dBm | 73.51 % | 13.21 dB |
| Rev 2.1 @2.4 $GHz$ | 41.00 dBm | 74.93 % | 13.00 dB |
| Rev 1.0 @2.45 $GHz$ | 41.00 dBm | 76.17 % | 12.2 dB |
| Rev 2.0 @2.45 $GHz$ | 41.00 dBm | 76.65 % | 12.21 dB |
| Rev 2.1 @2.45 $GHz$ | 41.00 dBm | 75.53 % | 10.90 dB |
| Rev 1.0 @2.5 $GHz$ | - dBm | - % | - dB |
| Rev 2.0 @2.5 $GHz$ | 41.00 dBm | 72.02 % | 10.50 dB |
| Rev 2.1 @2.5 $GHz$ | 41.00 dBm | 73.01 % | 9.40 dB |

Table 4.2: Simulated linearity performance for frequencies 2.3-2.5 GHz in increments of 50 MHz.

| **Freq.** | **I/C** $IMD_{3(32_{dBm})}$ | **I/C** $IMD_{3(35_{dBm})}$ | **I/C** $IMD_{3(38_{dBm})}$ |
|---|---|---|---|
| Rev 1.0 @2.3 $GHz$ | -35.30 dBc | -34.08 dBc | -26.95 dBc |
| Rev 2.0 @2.3 $GHz$ | -31.98 dBc | -36.54 dBc | -24.67 dBc |
| Rev 2.1 @2.3 $GHz$ | -33.74 dBc | -34.84 dBc | -26.19 dBc |
| Rev 1.0 @2.35 $GHz$ | -34.00 dBc | -32.22 dBc | -25.64 dBc |
| Rev 2.0 @2.35 $GHz$ | -34.57 dBc | -35.37 dBc | -25.77 dBc |
| Rev 2.1 @2.35 $GHz$ | -33.96 dBc | -34.61 dBc | -26.67 dBc |
| Rev 1.0 @2.4 $GHz$ | -32.68 dBc | -30.47 dBc | -23.49 dBc |
| Rev 2.0 @2.4 $GHz$ | -32.31 dBc | -32.05 dBc | -26.89 dBc |
| Rev 2.1 @2.4 $GHz$ | -33.39 dBc | -33.29 dBc | -25.76 dBc |
| Rev 1.0 @2.45 $GHz$ | -31.56 dBc | -29.00 dBc | -20.14 dBc |
| Rev 2.0 @2.45 $GHz$ | -30.65 dBc | -29.45 dBc | -21.70 dBc |
| Rev 2.1 @2.45 $GHz$ | -31.49 dBc | -30.51 dBc | -21.21 dBc |
| Rev 1.0 @2.5 $GHz$ | -31.00 dBc | -28.57 dBc | -18.90 dBc |
| Rev 2.0 @2.5 $GHz$ | -30.50 dBc | -29.13 dBc | -19.88 dBc |
| Rev 2.1 @2.5 $GHz$ | -31.01 dBc | -30.14 dBc | -20.02 dBc |

# Chapter 5

# Measurements

Due to Covid-19 restrictions measurements had to be performed by Morten Olavsbråten because of access to instruments and laboratories.

Two measurements were done in order to characterise the performance of the different input networks. A one tone test is performed to measure the output power, which is used to define gain and PAE for the networks. Two-tone tests are performed in order to generate intermodulation and test the linearity performance.

The measurements are performed with a spectrum analyser for one and two tone tests. A driver amplifier amplifies the signal before it enters the DUT. A circulator is used to prevent any damage to the signal generator and/or driver amplifier. A portion of the signal is fed to the spectrum analyzer through a directional coupler before the majority of the power is terminated in a 50Ω RF load. Figure 5.1 shows a block schematic of the measurement setup.

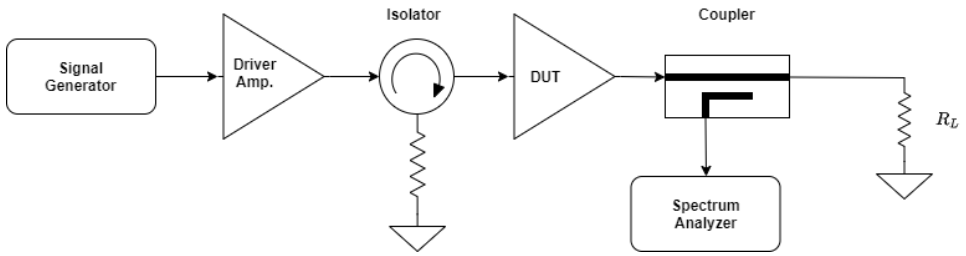



Figure 5.1: Block schematic of measurement setup.

Calibration procedures are performed in order to isolate the performance from the DUT. A driver amplifier is used in order to raise the signal to a proper level before passing through the DUT, which may have an impact on linearity measurements. As the same setup is used for all measurements this uncertainty is ignored.

Mounting of the transistor is done with a 3-D printed mounting bracket. The bracket allows for quick mounting and dismounting of the transistor. The same transistor can therefore be used in all measurements with no desoldering, to reduce the amount of sources of error. Because the input networks and output network are designed on separate substrates the output can stay stationary, while the input is changed for each measurement.

Figure 5.2 shows the measurement procedure during a two tone test.

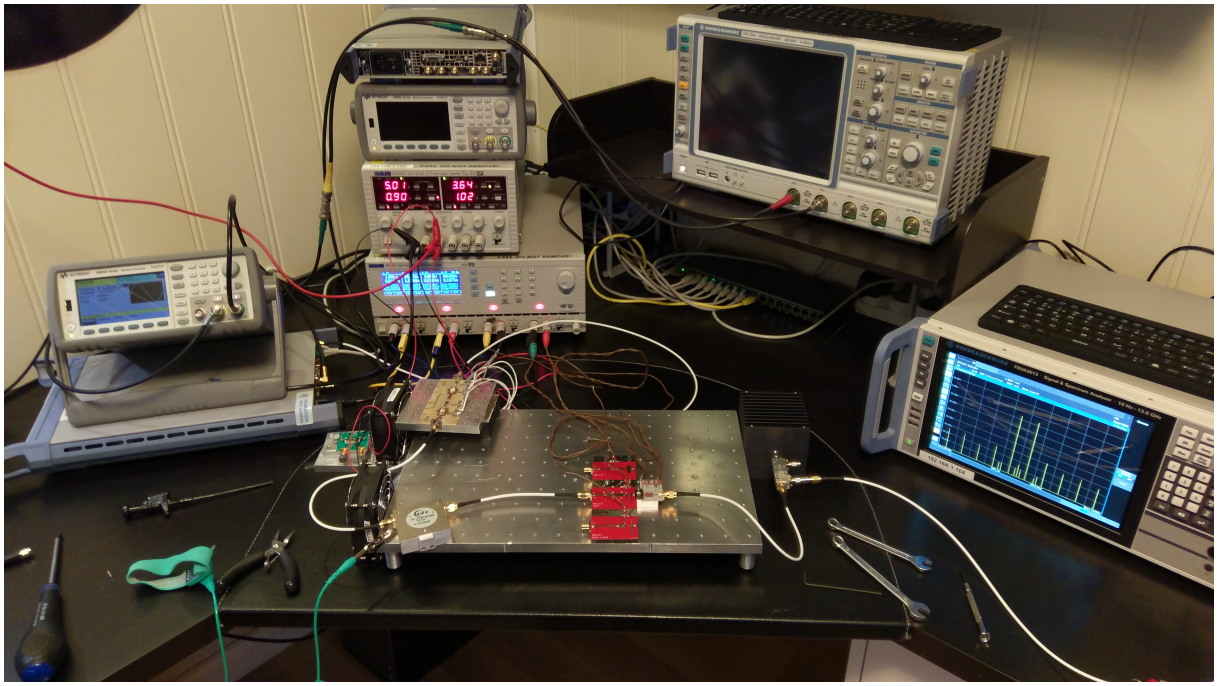


Figure 5.2: Measurement setup during a two tone test.

Instruments and components used for the measurements are summarized below in Table 5.1.

Table 5.1: Components and instruments used for one tone and two tone measurements.

| **Instrument/Component** | **Manufacturer** | **Model** |
|---|---|---|
| Signal Generator | Rohde & Schwarz | SGS100A |
| Waveform Generator | KEYSIGHT | 33600A |
| Spectrum Analyzer | Rohde & Schwarz | FSVA3013 |
| Power Supply | TTi | MX100QP |
| Isolator | uiy | UIYBCI5049B |

# Chapter 6

# Results

The measured results are prestented in this chapter, for one- and two tone tests. Results are only presented for one frequency, 2.35 GHz as the results indicates good performance for this frequency. Appendix contains more measurements for other frequencies.

## 6.1 One tone measurements

### 6.1.1 Output power

Figure 6.1 shows the output power generated with the different input network revisions. Revision 2.0 has a slightly higher output power before saturation, while the other two networks are very similar in performance. Deeper in saturation these plots should converge, as the saturated output power is defined by the transistor.

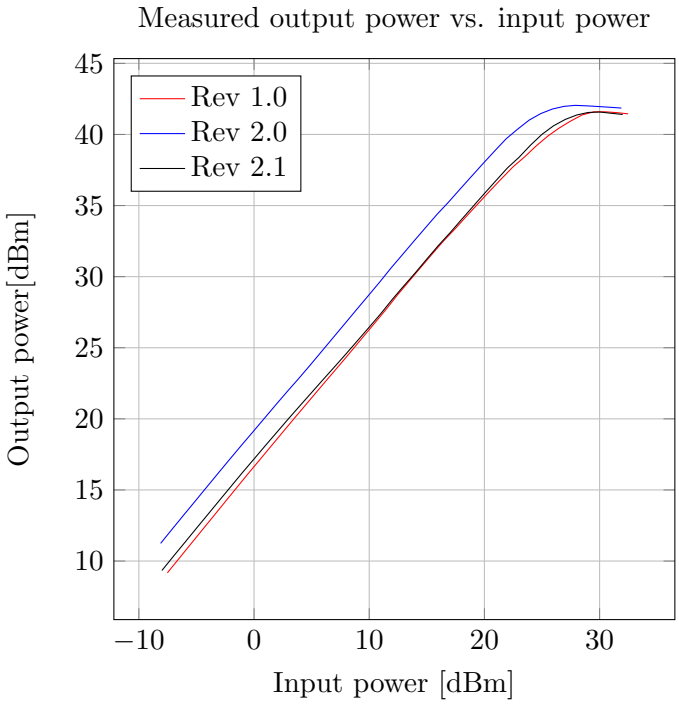



Figure 6.1: Measured output power of all input network revisions.
Measured output power of all input network revisions.

### 6.1.2 Efficiency

Efficiency is measured in PAE, which includes the gain of the device. Power added efficiency is a highly sought after metric in power amplifiers, as it directly translates to power consumption. Again revision 2.0 is favored in comparison to the other two.

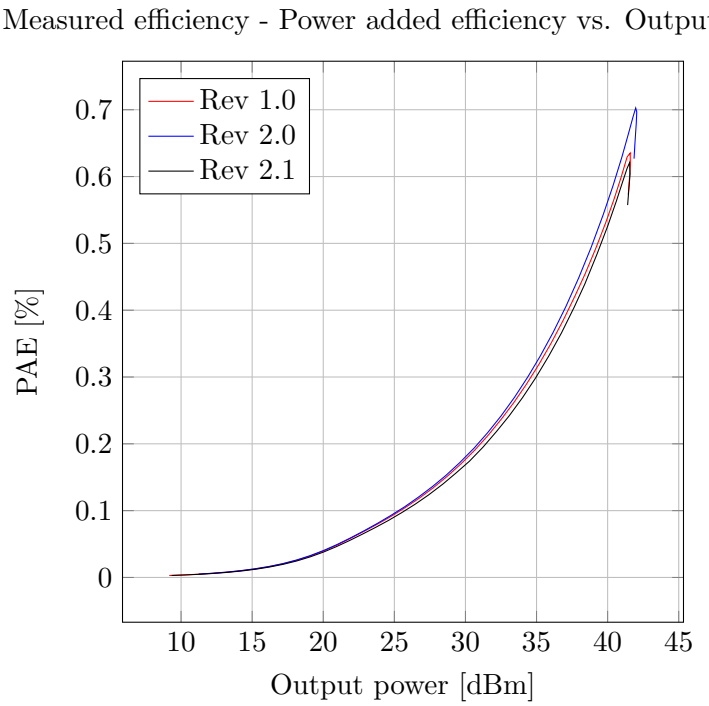



Figure 6.2: Measured power added efficiency performance of all input network revisions.
Measured power added efficiency performance of all input network revisions.

### 6.1.3 Gain

The gain variations with the three different input networks is plotted in Figure 6.3. Revision 2.0 is superior to the other two in gain, which explains the increase in output power before saturation in Figure 6.1.

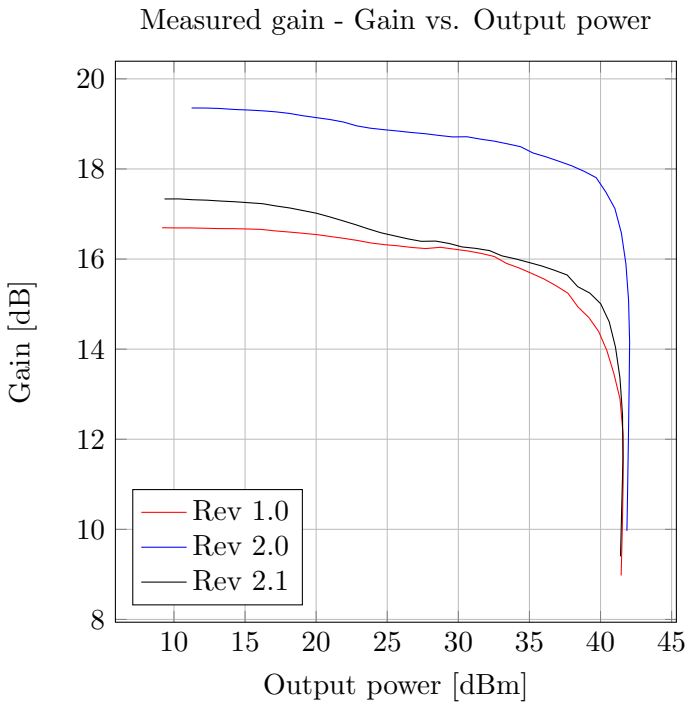



Figure 6.3: Measured gain performance of all input network revisions.
Measured gain performance of all input network revisions.

### 6.1.4 Linearity

The presented results consists of the total summed power in $IMD_3$ products of high and low tones ($f_0\pm$ Tone spacing) in relation to total output power in the fundamental. Additional plots are added in APPENDIX.

Results from the two tone test to measure linearity is shown in Figure 6.4. Between 5-15 dBm output power the measured signal seems to be dominated by noise. This is likely due to the noise floor of the instrument, resulting from the resolution bandwidth of the spectrum analyzer. The linearity shows tendencies of improvement in cases of high output power with input revisions 2.0 and 2.1. Revision 2.1 is superior in terms of linearity as the $IMD_3$ products show a 3 dB increase at 35 dBm output power. While the improvements are relatively small, these results are only a factor of more complex input networks. The linearity at lower output power is increased with the linearization networks, however linearity is more of an issue when approaching saturation.

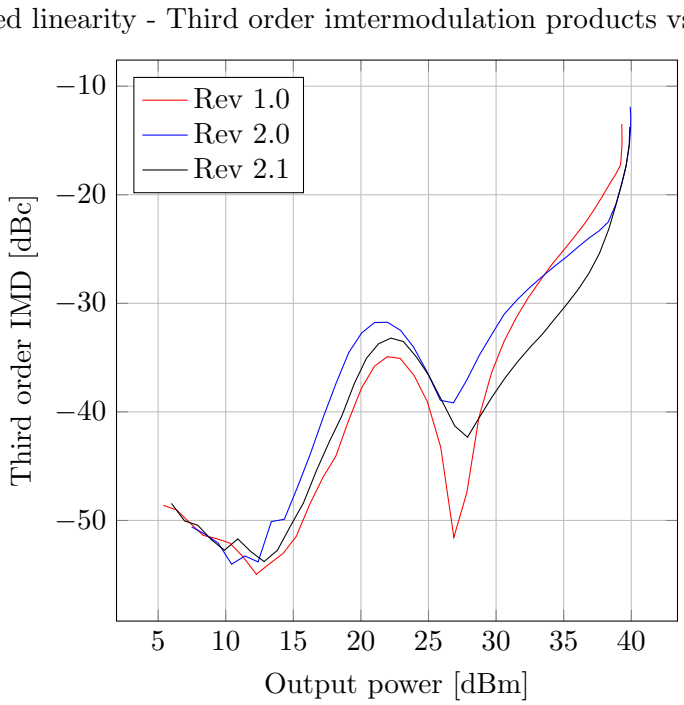



Figure 6.4: Measured linearity performance of all input network revisions.
Measured linearity performance of all input network revisions. The graphs represent the average power in high and low tones which correspond to $2.35\,GHz \pm 5+, MHz$.

Table 6.1 contains the power in $IMD_3$ products related to total output power. High and low tones are summed together. The measurements are done in descrete signal levels, so the data in Table 6.1 is approximated.

Table 6.1: Measured linearity performance for frequencies 2.3-2.5 GHz in increments of 50 MHz. Out of bound measurements are indicated by OOB

| **Freq.** | **I/C** $IMD_{3(32_{dBm})}$ | **I/C** $IMD_{3(35_{dBm})}$ | **I/C** $IMD_{3(38_{dBm})}$ |
|---|---|---|---|
| Rev 1.0 @2.3 $GHz$ | -30.45 dBc | -25.40 dBc | -20.75 dBc |
| Rev 2.0 @2.3 $GHz$ | -28.40 dBc | -25.55 dBc | -22.40 dBc |
| Rev 2.1 @2.3 $GHz$ | -32.75 dBc | -29.10 dBc | -23.65 dBc |
| Rev 1.0 @2.35 $GHz$ | -30.00 dBc | -24.65 dBc | -19.05 dBc |
| Rev 2.0 @2.35 $GHz$ | -28.40 dBc | -24.95 dBc | -21.80 dBc |
| Rev 2.1 @2.35 $GHz$ | -33.40 dBc | -29.20 dBc | -23.55 dBc |
| Rev 1.0 @2.4 $GHz$ | -30.35 dBc | -24.20 dBc | -17.9 dBc |
| Rev 2.0 @2.4 $GHz$ | -28.05 dBc | -24.00 dBc | -20.35 dBc |
| Rev 2.1 @2.4 $GHz$ | -32.90 dBc | -28.10 dBc | -22.55 dBc |
| Rev 1.0 @2.45 $GHz$ | -29.05 dBc | -23.10 dBc | -15.4 dBc |
| Rev 2.0 @2.45 $GHz$ | -28.00 dBc | -23.75 dBc | -17.60 dBc |
| Rev 2.1 @2.45 $GHz$ | -32.05 dBc | -27.05 dBc | -18.90 dBc |
| Rev 1.0 @2.5 $GHz$ | -27.10 dBc | -21.40 dBc | OOB |
| Rev 2.0 @2.5 $GHz$ | -27.95 dBc | -22.65 dBc | OOB |
| Rev 2.1 @2.5 $GHz$ | -31.10 dBc | -25.90 dBc | -15.95 dBc |

# Chapter 7

# Discussion

This chapter goes through the results presented in chapter 4 and chapter 6.

## 7.1 Input network performances

When designing the input networks there was no large emphasis on maintaining center frequency and bandwidth. As a result the simulated S-parameters have drifted away from the initial center frequency of 2.4 GHz. This effect is even worse in revision 2.0 and 2.1 where reducing the $IMD_3$ products is utilized as the main parameter for optimization. Higher gain and PAE could likely be achieved if the center frequency was maintained. In regards to linearity improvement this could have a result on the bandwidth of the technique.

From the plots in chapter 6 it is evident that output power, PAE and gain is superior for revision 2.0. The primary factor which may contribute to the increased performance compared to the others is the gain of the device. An increased gain will contribute to a higher output power given the transistor is not fully saturated. Higher output power and gain leads to higher PAE as indicated in chapter 2. The higher gain is likely attributed to a better match (lower $S_{11}$, which implies more power is delivered to the device. This should however not result in a higher saturated output power. Differences in output power is attributed to the fact that total saturation is not achieved.

## 7.2 Linearity results

From the results presented in Figure 6.4 the input tuning has a clear impact on reducing the $IMD_3$ products. As predicted in chapter 3 the linearity enhancement should have a greater impact with high levels of saturation, as harmonics of higher amplitude are generated by the non-linearities in the transistor. At lower output power the networks designed to increase linearity does the opposite. Finding optimal source impedance for improving linearity is done while the transistor operates within compression. Therefore the enhancement on linearity is not complied for lower output power. The technique is based on using the generated harmonics for tuning purposes, deteriorating the linearity in high OPBO is therefore not unreasonable.

Appendix C and Table 6.1 also indicates reasonable performance within a large bandwidth. Measured $IMD_3$ in Revision 2.1 is lower than the reference design rev 1.0 in all cases between 2.3 and 2.5 GHz. Although the best results are at 2.35 GHz.

The simulated results in regards to linearity shows a smaller improvement than the real measurements. The transistor model may not be able to predict the non-linear effects of the transistor.

## 7.3 Comparison of measurements and simulations

The dip in third harmonic $IMD_3$ products appear at different output power in simulations and measurements. There is however consistency in all linearity measurements as this dip appears at roughly the same output power in all measurement cases. The transistor model is likely the cause of this as it may not be able to predict the output signal entirely.

## 7.4 Future work

#### Linearity Measurements

Due to time constraints and Covid-19 interference the linearity performance is not tested with real input signals. The circuits should undergo more linearity testing in order to see how the linearity enhancement performs with real signals. Measurements of ACPR and Error vector magnitude are of great relevance, and should be the next step to better understand the results. Based on linearity results signals which employ modulation schemes with large PAPR would likely see less improvement from this technique.

#### Characterizing bandwidth

Little emphasis is put on determining the bandwidth of this technique, however Table 6.1 indicates linearity enhancement through 2.3-2.5 GHz. Initially in the design procedure this technique was predicted to be very bandwidth restricted. However achieving improvements through more than 200 MHz bandwidth suggests similar techniques can improve linearity through wider bandwidths.

### Optimizing towards linearity

Only the input network is tuned to accommodate a linearity increase in this thesis. Optimizing towards linearity for the whole amplifier circuit could reach the same results, and should be investigated further. Certain output terminations may attribute to a larger improvement in linearity by changing the magnitude of reflected power at the output network.

### Combination with other techniques

As the presented linearization technique is highly dependant on the transistor operating in compression (as is evident from Figure 6.4) other techniques could be of interest in combination with the input tuning. Especially envelope tracking could further increase the overall performance. Envelope tracking is a technique which dynamically adjusts the bias of an amplifier based on the input signal. Adjusting the bias dynamically allows the transistor to reach compression through a large dynamic range which generally increases efficiency. As the result of ET is a transistor that always operates within compression regions the input tuning for linearity could increase linearity within a larger dynamic range.

# Chapter 8

# Conclusion

In this thesis a passive linearization technique based on tuning of the input impedance has been explored on a 10 W GaN HEMT.

A highly efficient 2.4 GHz non-linear amplifier has been designed in ADS through load pull analysis. An initial input network is designed to accentuate the gain of the amplifier. Revisions of the input network has been constructed in order to enhance linearity, with reduction in $IMD_3$ as the main parameter.

With an input signal of frequency 2.35 GHz the linearity enhancing input network provides an improvement in $IMD_3$ of 3.4-, 4.55- , 4.5 dB for output powers 32-, 35 and 38 dBm respectively. Varying degrees of improvement are observed for all input signals of frequencies 2.3-2.5 GHz while the fundamental output power exceeds 32 dBm. Minimal impact is made on the PAE while linearity is enhanced.

The measured results indicate that linearity enhancement is possible by passive tuning of the input network, within a sufficient bandwidth. This particular method has the highest impact on linearity when the transistor is operating within compression regions.

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# Appendices

# Appendix A

# Biasing networks

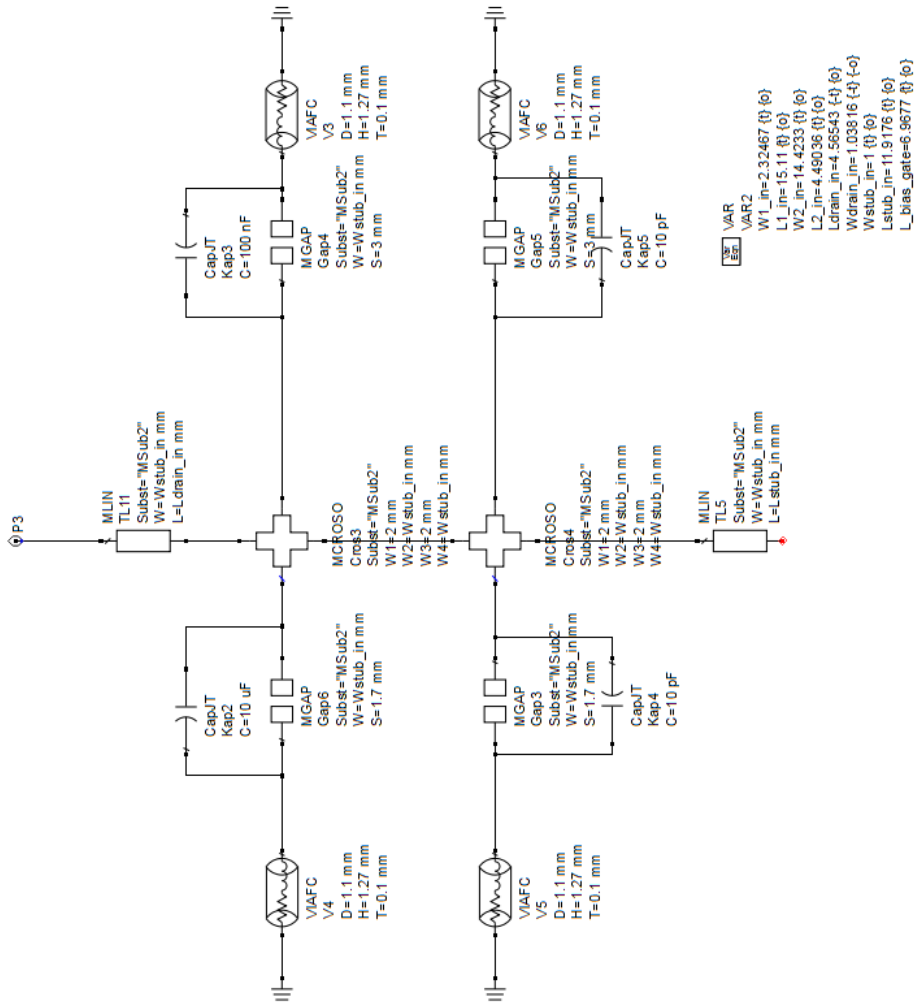



Figure A.1: ADS schematic of input biasing network.

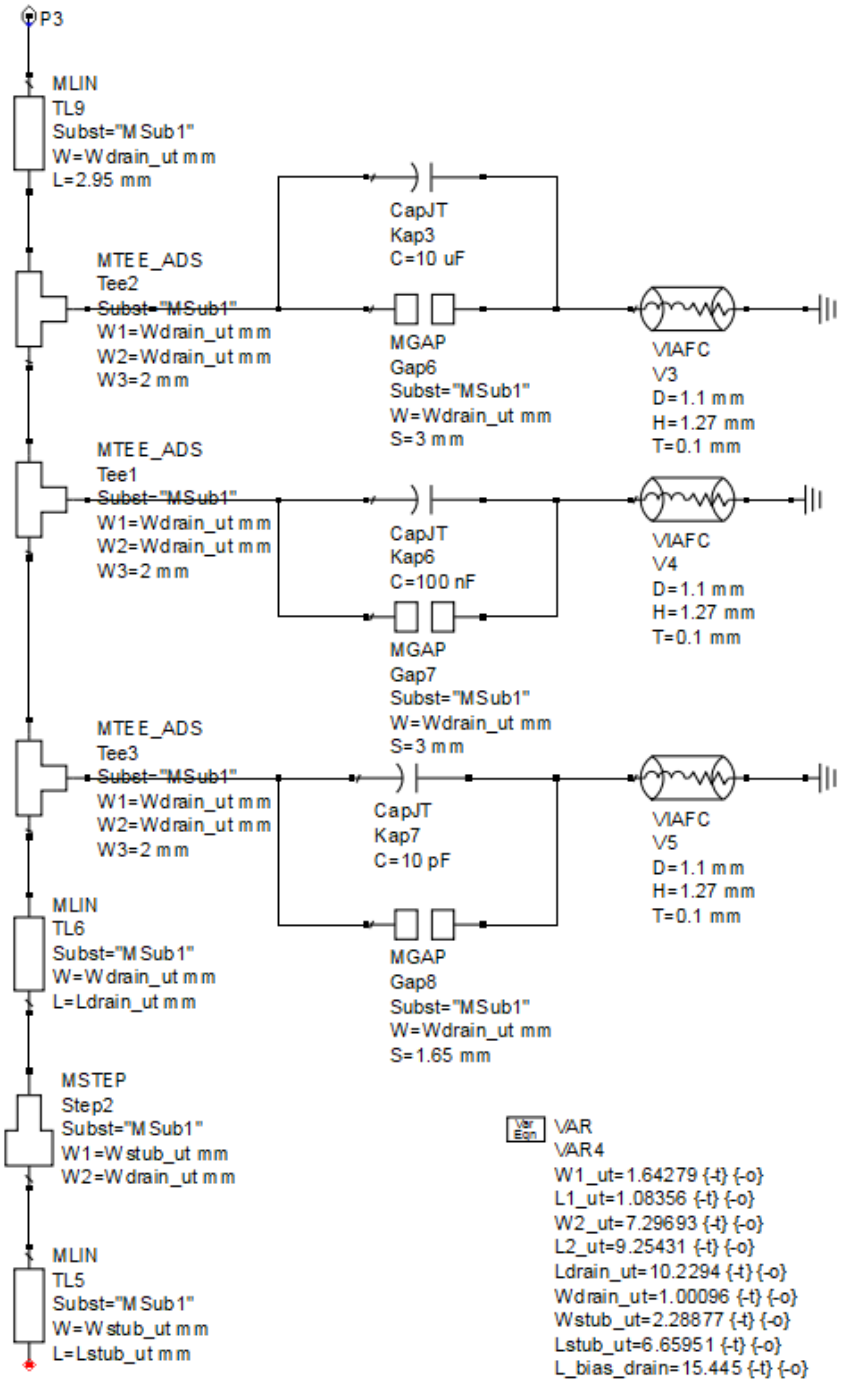



Figure A.2: ADS schematic of biasing network

# Appendix B

# Total circuit

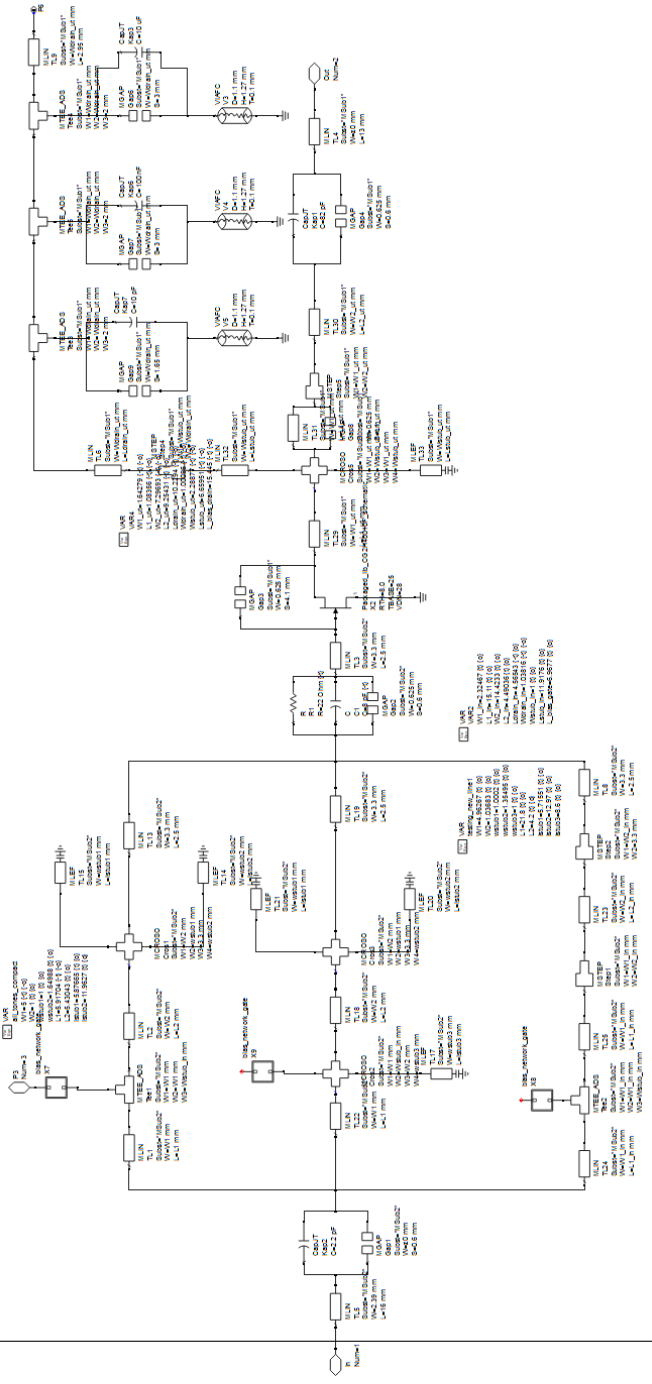




Figure B.1: Complete ADS schematic. Input revisions 1.0, 2.0 and 2.1 from right to left.

# Appendix C

# Linearity measurements 2.35-2.45 GHz

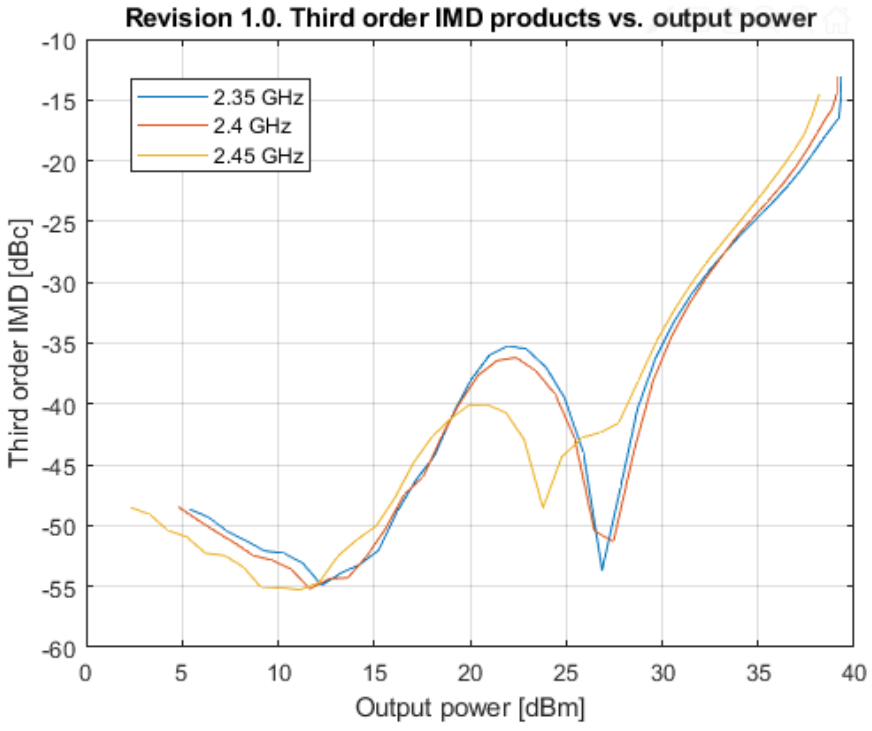



Figure C.1: Linearity measurements from 2.35-2.45 GHz on rev 1.0.

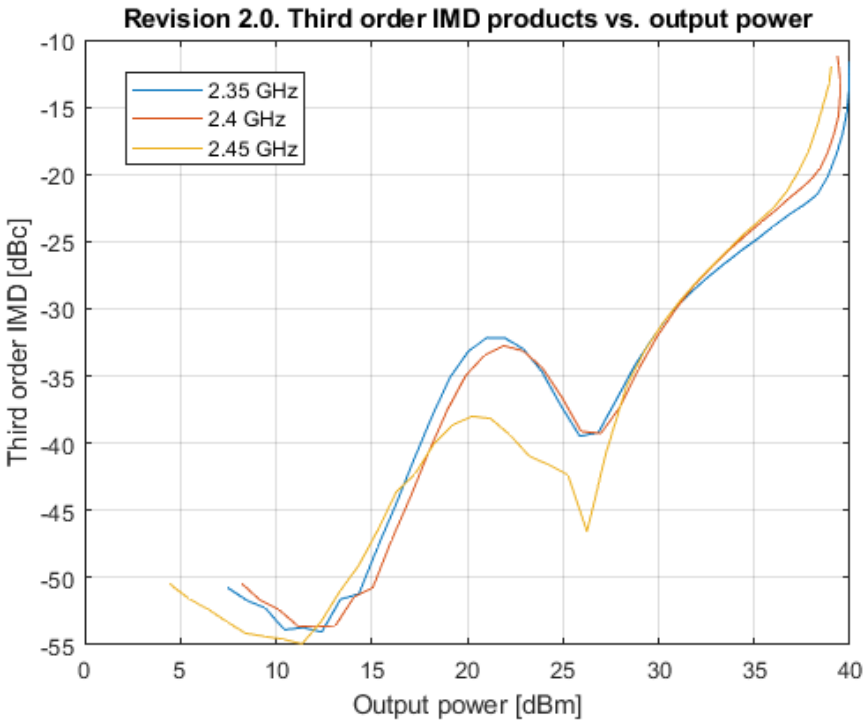



Figure C.2: Linearity measurements from 2.35-2.45 GHz on rev 2.0

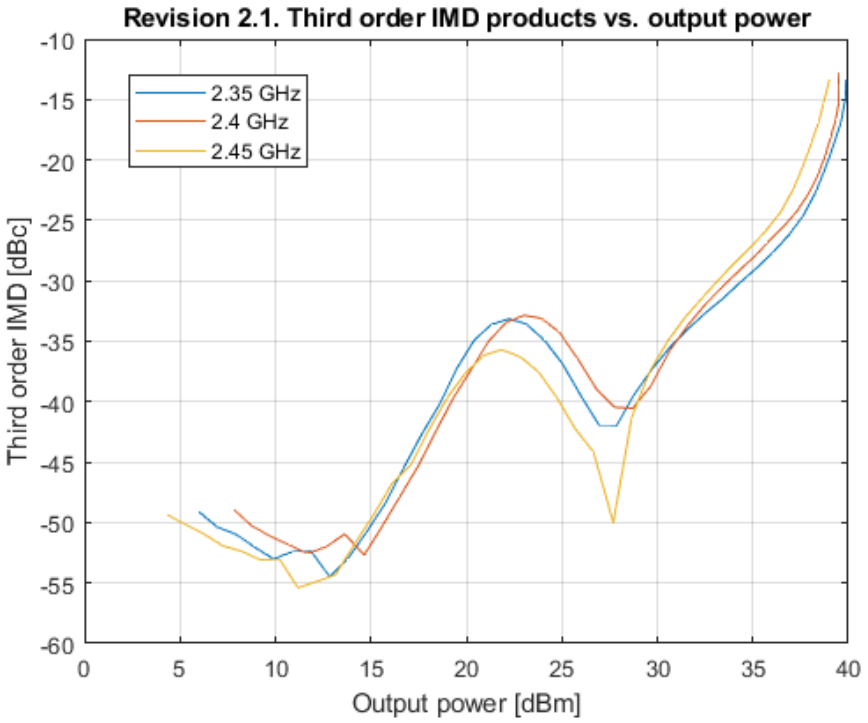
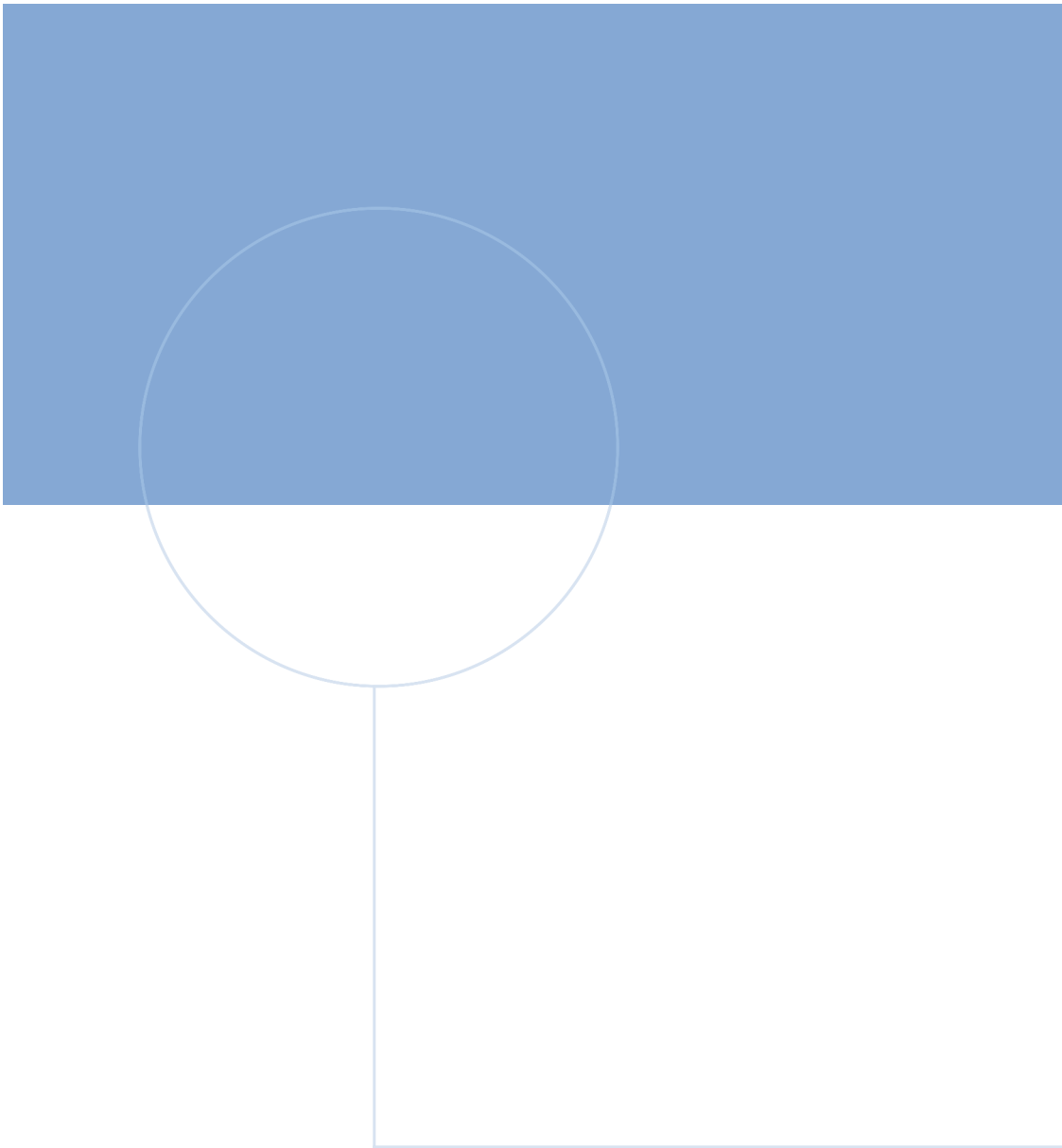



Figure C.3: Linearity measurements from 2.35-2.45 GHz on rev 2.1.



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