A Low-power High-gain Inverter Stacking Amplifier with Rail-to-Rail Output

Erwin H. T. Shad[1], Tania Moeinfard[2] , Marta Molinas[1], Trond Ytterdal[3]

***Abstract*—In this article, a rail-to-rail low-power amplifier is presented based on stacking inverter-based amplifiers. The output voltages of each inverter-based amplifier are converted to a current and then mirrored to the output so that a rail-to-rail output is achieved. Besides, extensive simulations have been carried out to show the effect of drain-source voltage on the intrinsic gain of a transistor. Based on these simulations, a minimum supply voltage is chosen to achieve high open-loop gain and low closed-loop gain error. All the simulations are carried out in a commercially available 0.18 µm CMOS technology. The proposed amplifier achieves 88 dB open-loop gain. It is exploited in a capacitively-coupled amplifier structure. The closed-loop gain is 40 dB in the bandwidth of 0.1 Hz to 10 kHz when the power consumption is 0.54 µW at a 1.2 V supply voltage. The total input-referred noise is 4.7 $\mu\mathrm{V_{rms}}$ in the whole bandwidth. The proposed neural amplifier achieved 0.02 SEF in the bandwidth from 200 Hz to 10 kHz. The proposed amplifier achieved a rail-to-rail output swing while the SEF is among the best reported SEF in the literature. Besides, to show the robustness of the proposed structure in the presence of process and mismatch variation, 500 Monte Carlo simulations are carried out. The PSRR and CMRR mean values are 89 dB and 68 dB, respectively. Finally, the proposed neural amplifier area consumption is 0.03 $\mathrm{mm^2}$ without pads.**

***Index Terms*—Inverter-based, current-reuse, neural amplifier, low power, low noise, rail-to-rail**

I. Introduction

The maximum required supply voltage decreased over the past decades by progress in technologies [1]. Besides, lower power consumption applications ensure higher battery life and smaller battery [2]. Consequently, the intrinsic gain of transistors decreases in smaller technologies which limits the open-loop gain of amplifiers [3].

A significant amount of power is usually dedicated to the first stage amplifier just to minimize the total input-referred noise [4], [5]. Minimizing the total input-referred noise becomes more challenging in implantable high-density neural applications where the total power consumption is constraint due to the side effects of high heat on body tissues [6].

In order to minimize the thermal noise, usually, the input transistors of amplifiers are biased in weak-inversion to maximize g_m/I_D [7]. As the required noise floor decreases, higher power is required. In order to increase the input transconductance without increasing current, inverter-based or current reuse structure is proposed [8]. Furthermore, stacking and orthogonal inverter-based amplifiers have been suggested in many applications to increase the g_m more than before [9], [10]. Although it has been widely used in biomedical applications [11]–[13], they still require a second stage to boost the output swing [9].

In order to have better comparison between amplifiers, noise efficiency factor (NEF) [14] , Power efficiency factor (PEF) [15] and then system efficiency factor (SEF) [16] are proposed as Eq. 1, 2 and 3, respectively. Besides, the output dynamic range can be calculated as Eq. 4. Therefore, in order to design an amplifier with very low SEF, the proposed amplifier should have not only low noise and low power but also high swing.

$$NEF = V_{ni,rms}\sqrt{\frac{2I_{tot}}{\pi V_T 4kTBW}} \tag{1}$$

$$PEF = NEF^2.V_{DD} \tag{2}$$

$$SEF = PEF/DR_{out} \tag{3}$$

$$DR_{out} = 10\log\frac{V_{amp,max}^2}{2.A^2.V_{ni,rms}^2} \tag{4}$$

where $V_{ni,rms}$ is the total equivalent input-referred noise in the amplifier's bandwidth, BW is the amplifier's -3 dB bandwidth, v_t refers to the thermal voltage, V_{DD} is the supply voltage, I_{tot} is the total current drawn from the power supply, $V_{amp,max}$ is the maximum swing at the amplifier output and A is the amplifier voltage gain.

A high swing current reuse amplifier was presented in [17]. In this structure, the input transconductance is equal to $2g_m$. Although this amplifier achieved low NEF as well as high swing, the minimum supply voltage is limited by $2(V_{GS} + V_{DS})$. Therefore, it requires a very high supply voltage like any other conventional inverter-based amplifier.

In this article, first, it has been shown how limited drain-source voltage will affect the intrinsic gain. This problem is severe in cascoding and stacking structures with limited supply voltage. Then, a new structure based on stacking inverter-based amplifier is proposed which will have high gain and rail-to-rail output swing. In the simulation result section, the proposed structure is used in a capacitively-coupled amplifier (CCA) structure to show its performance as a neural amplifier. Finally,

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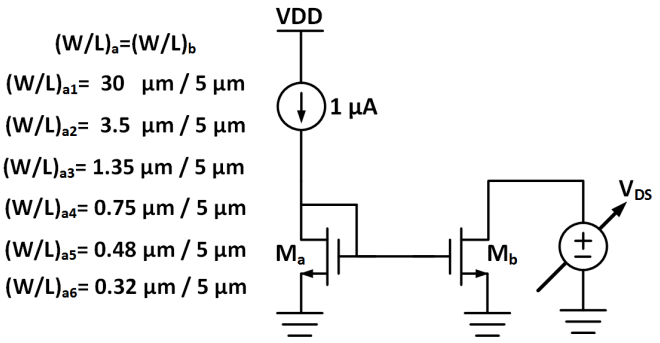

Fig. 1. The test circuit to see how drain-source voltage will effect intrinsic gain, g_m and r_{ds}.

it is compared as a neural amplifier with the state-of-the-art amplifiers.

II. The Effect of Drain-source on Intrinsic Gain

Generally, the voltage gain of an amplifier is proportional to the transistors intrinsic gain. The intrinsic gain of a transistor can be defined as equation 5. Simplified equation of g_m and in strong inversion (SI) and subthreshold (ST) can be shown by Eq. 6 and 7. Also, the output impedance of a single transistor is as Eq. 8 where I_D is the drain current of the transistor, W and L are the transistor's width and length, C_{ox} is the gate oxide capacitance per unit area, μ is the mobility of charge (electron or hole), n is the non-ideality factor and λ is channel-length modulation coefficient [18].

$$Intrinsic\ gain = g_m r_{ds} \tag{5}$$

$$g_{m,SI} = \sqrt{\frac{2I_D \mu C_{ox} \frac{W}{L}}{1 + \lambda V_{DS}}} \tag{6}$$

$$g_{m,ST} = \frac{I_D}{n v_t} \tag{7}$$

$$r_{ds} = \frac{1}{\lambda I_D} \tag{8}$$

To see the effect of drain-source voltage on a transistor intrinsic gain, a test circuit as it is depicted in Fig 1 is used. The dependency of intrinsic gain to V_{DS} is depicted Fig. 2 for the NMOS transistor in a commercially available 0.18 µm CMOS technology for different W/L. V_{dsat} is defined as Eq. 9 where V_{TH} is the threshold voltage of the transistor and V_{GS} is the gate-source voltage. Different V_{dsat} represents different operational regions also.

$$V_{dsat} \approx V_{GS} - V_{TH} \tag{9}$$

In order to see which parameter is affecting intrinsic gain, g_m and r_{ds} versus V_{DS} are separately simulated as it is shown in Fig. 3 and 4. According to these simulations, it can be seen that for high V_{DS}, the variation of g_m is negligible although this dependency increases as the transistor go from strong

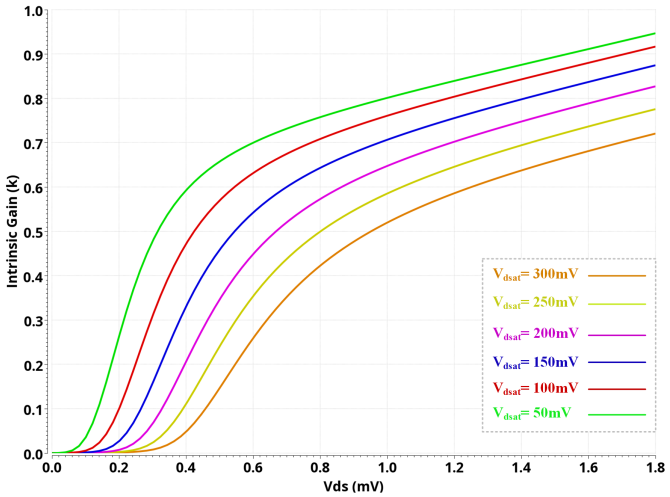

Fig. 2. Dependency of intrinsic gain to drain-source voltage for different $\mathrm{V_{dsat}}$.

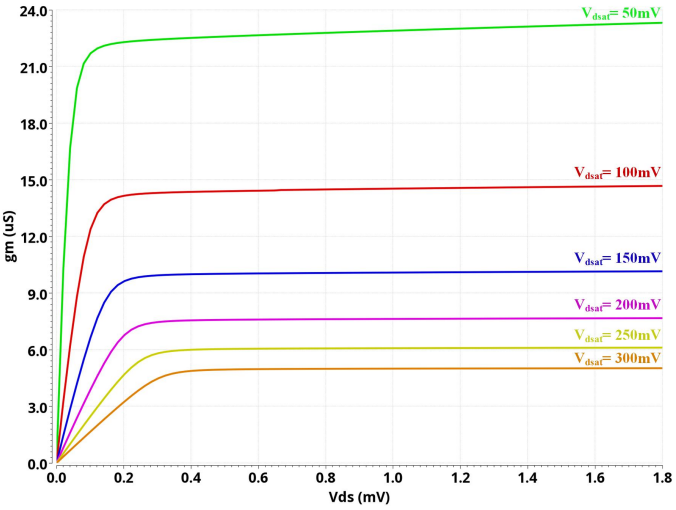

Fig. 3. g_m dependency to drain-source voltage for different $\mathrm{V_{dsat}}$.

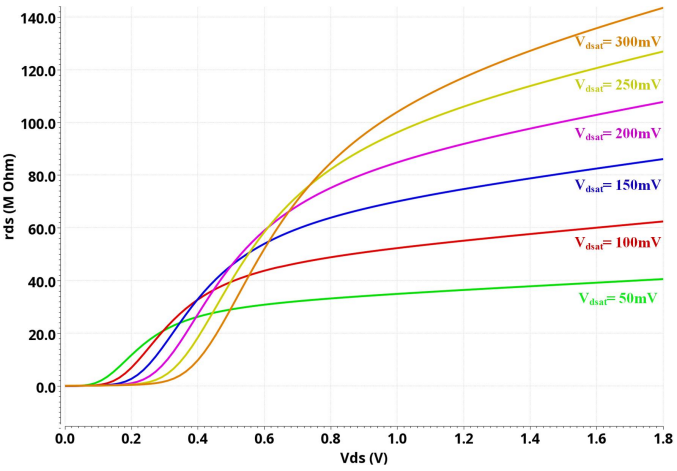

Fig. 4. r_{ds} dependency to drain-source voltage for different $\mathrm{V_{dsat}}$.

TABLE I
VARIATION OF INTRINSIC GAIN, g_m AND r_{ds} VERSUS DRAIN-SOURCE VOLTAGE FOR DIFFERENT V_{dsat}

Vds,sat= 50mV										
V_{ds} (mV)	50	100	150	**200**	250	300	350	400	450	500
r_{ds} $(M\Omega)$	0.2	1.6	5.8	**12**	17	21	24	26	28	29
g_m (μS)	18.1	21.6	22.1	**22.3**	22.3	22.4	22.5	22.5	22.5	22.6
$g_m r_{ds}$	3.62	34.6	128.2	**267.6**	379.1	470.4	540	585	630	655.4
Vds,sat= 100mV										
V_{ds} (mV)	50	100	150	200	**250**	300	350	400	450	500
r_{ds} $(M\Omega)$	0.1	0.5	2.3	7	**14**	21	28	32	36	39
g_m (μS)	7.4	12.3	13.6	14.2	**14.3**	14.3	14.3	14.4	14.4	14.4
$g_m r_{ds}$	0.74	6.15	31.28	99.4	**200.2**	300.3	400.4	460.8	518.4	561.6
Vds,sat= 150mV										
V_{ds} (mV)	50	100	150	200	250	**300**	350	400	450	500
r_{ds} $(M\Omega)$	0.1	0.3	0.7	2.7	7.9	**15.8**	24	33	40	45
g_m (μS)	3.5	6.6	8.8	9.6	9.8	**9.9**	10	10	10	10
$g_m r_{ds}$	0.35	1.98	6.16	25.92	77.42	**156.42**	240	330	400	450
Vds,sat= 200mV										
V_{ds} (mV)	50	100	150	200	250	300	**350**	400	450	500
r_{ds} $(M\Omega)$	0.1	0.2	0.4	1	3.5	9	**18**	27	37	46
g_m (μS)	2	3.8	5.5	6.7	7.3	7.4	**7.5**	7.5	7.5	7.6
$g_m r_{ds}$	0.2	0.76	2.2	6.7	25.55	66.6	**135**	202.5	277.5	349.6

inversion to weak or sub-threshold region. Therefore, unlike Eq. 5-8, it has been shown through simulation in Fig. 4 that the dependency of r_{ds} versus V_{DS} is more severe and complex. Unlike the behaviour of g_m, the variation of r_{ds} versus V_{DS} decreases as the transistor goes from strong-inversion to sub-threshold region.

For lower V_{DS}, these variations for intrinsic gain, g_m and r_{ds} are abrupter. In table I, these variations have been reported up to 500 mV. It has been shown by increasing the V_{DS} the variation for all parameter decreases. The variation of g_m is not severe for V_{DS} higher than V_{dsat}. Though in sub-threshold and weak inversion, as it gets near to V_{dsat}, the variation becomes greater.

Interestingly, if V_{DS} increased 50 mV, the intrinsic gain will be multiplied by a factor larger than 2, until V_{DS} is 150 mV above V_{dsat} regardless of operation region of the transistors. These values are shown with a bold font in the table. Therefore, high V_{DS} is necessary to achieve high r_{ds} and intrinsic gain.

III. PROPOSED STRUCTURE

In [9], a new stacking structure was shown to increase the input transconductance as well as minimizing the required supply voltage. Although they achieved a very low NEF, stacking led to limited low output swing. Besides, stacking leads to limited drain-source voltage for each transistor. Although their structure has an intrinsic gain square gain, as it is shown in the table I, the limited gain drain-source voltage might bring very low open-loop gain and consequently high gain error in closed-loop gain. In [17], a structure for inverter-based amplifiers is shown to increase output swing with approximately same power consumption as conventional inverter-based amplifiers.

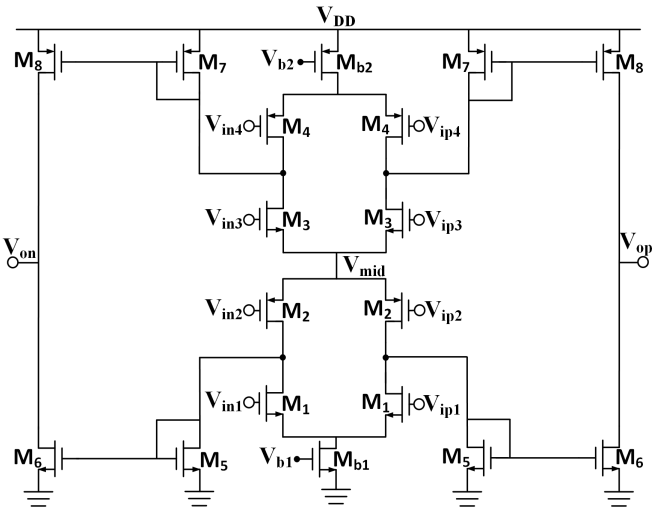

Fig. 5. Proposed high-swing stacked inverter-based amplifier.

A new structure with less noise and rail-to-rail output swing is proposed in this article by combining these two techniques which are shown in Fig 5. M5 and M7 are connected so that they make a low impedance path for the AC signal to the output branch. This leads to generating a low impedance node at the output of the inverter-based amplifiers. As long as, the current that flows in M_{5-8} is relatively less than tail currents, the effect of these M_{5-8} will be negligible on total power consumption.

In this structure unlike conventional inverter-based amplifier, inputs are detached from each other. This helps to minimize the required supply voltage. Input transistors are biased in the sub-threshold region to achieve highest g_m/I_D. V_{dsat} is approximately 50 mV in this case and the variation of g_m is relatively high near to this value. Besides, to generate a low impedance path by M5 and M7, r_{ds1-5} should be sufficiently large. Furthermore, tail transistors should be in strong inversion to increase the robustness of circuit in the presence of process and mismatch variation, therefore, a large proportion of supply voltage should be allocated to tail transistors. By considering all of these effects, according to I a 1.2 supply voltage is used for this structure.

The gain of the proposed structure is equal to Eq. 10 where the input transconductance can be calculated as Eq. 11. This gain is proportional to the transconductance of the input transistors and the output impedance. This is different from the intrinsic gain of a single transistor. Therefore, a high gain can be achieved with much freedom. In this structure, most of the current flows through input transistors to generate large transconductance and a small proportion of input current will flow to the output branch to provide large output impedance. Therefore, the gain should be extremely larger than the intrinsic gain of any transistor in this structure.

$$A = g_{m,in}(r_{ds6} \parallel r_{ds8}) \approx 2g_{m1}r_{ds6} \tag{10}$$

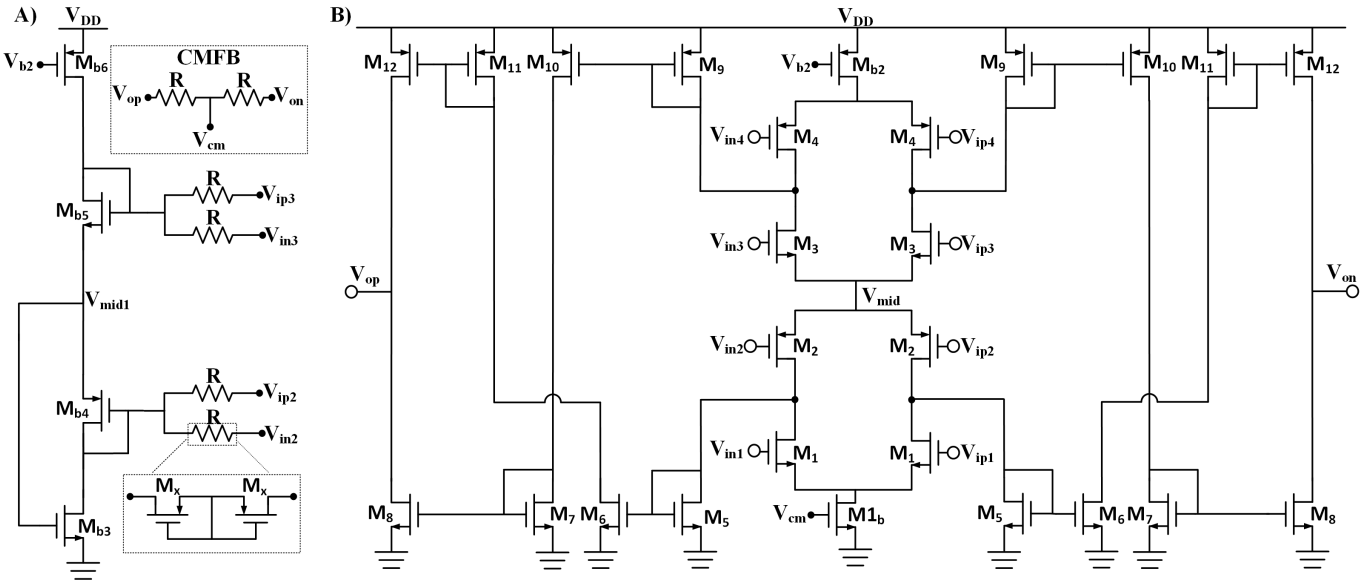

Fig. 6. A) the biasing circuit and common-mode feedback B) The modified proposed structure to utilize passive common-mode feedback.

$$g_{m,in} = g_{m1} + g_{m2} + g_{m3} + g_{m4} \tag{11}$$

The input-referred noise is approximately equal to Eq. 12. High proportion current is flowing through input transistors in comparision with the M_{5-8}. Besides, the input transistors are biased in weak inversion and M_{5-8} are in strong inversion. Therefore, the input referred-noise can be approximated to the Eq. 13.

$$v_{ni}^2) = \frac{16kT}{3g_{m,in}}(1 + \frac{g_{m5}}{g_{m,in}} + \frac{g_{m6}}{g_{m,in}} + \frac{g_{m7}}{g_{m,in}} + \frac{g_{m8}}{g_{m,in}}) \tag{12}$$

$$v_{ni}^2 \approx \frac{4kT}{3g_{m1}} \tag{13}$$

M_1 and M_4 biasing is simple but M_2 and M_3 require specific biasing technique. A biasing technique based on what is proposed in [9] is exploited as it is depicted in Fig. 6A. In order to make the structure adaptable with passive common-mode feedback, a couple of transistors are added to provide a negative common-mode feedback to set the output DC voltages on the desired voltage. The final circuit is drawn in Fig. 6B. The width and L of M_{5-12} are same so that the additional circuit will not affect gain or bandwidth. Therefore, the noise and gain equation is almost the same as the proposed structure in Fig 5.

The open-loop gain and input-referred noise of the proposed structure has been shown in Fig. 7. The proposed structure achieved 88 dB gain at low frequencies, and the noise floor is 43 nV/sqrtHz. This high gain is achieved by exploiting 250 nA for tail current and 25 nA for output branches. This leads to relatively high input transconductance and very high output impedance.

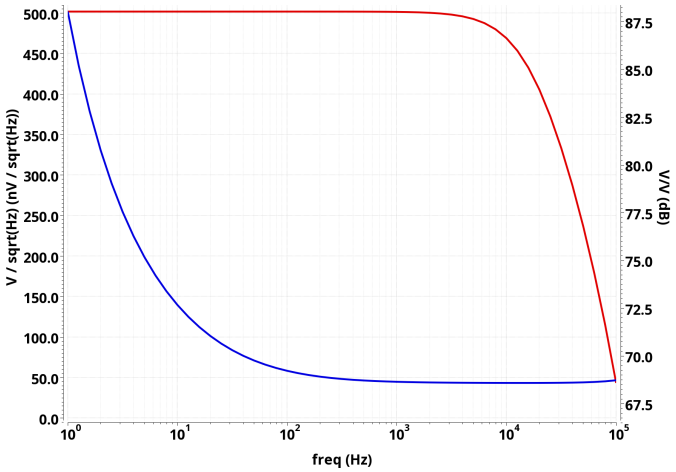

Fig. 7. The open-loop gain (red line) and input-referred noise (blue line) of the modified proposed structure.

IV. Simulation Results for the Closed-Loop Neural Amplifier

The proposed structure is used as a core amplifier in the structure in Fig. 8. In this structure, C_{in} and C_f are 10 pF and 100 fF, respectively. The input capacitors detached the DC of input source from the inputs. R_f generates a DC path from input to output to minimize the offset, and it determines the lower cut-off frequency with C_f. This resistor is also implemented by pseudo-resistors. The layout of the closed-loop amplifier is shown in Fig. 9. The proposed structure consumes 0.03 mm^2 area. In order to minimize flicker noise, the input transistors are chosen quite larger than the rest transistors.

The closed-loop gain and noise have been shown in Fig. 10. The lower cut-off frequency is less than 0.1 Hz and the

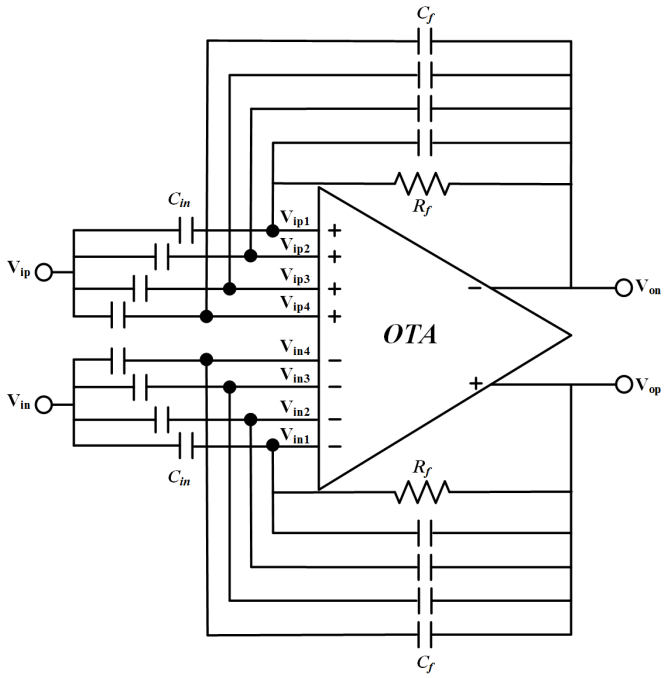

Fig. 8. Capacitively-coupled amplifier with the proposed structure as its core.

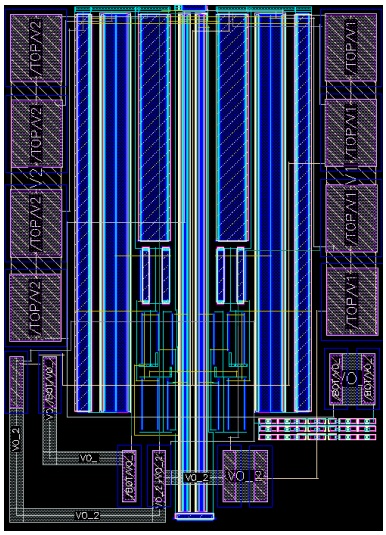

Fig. 9. The layout of the proposed neural amplifier without biasing circuit and pads (150 µm× 206 µm).

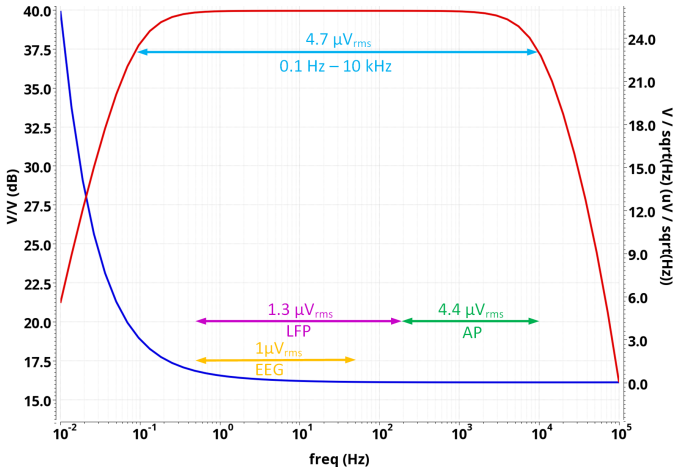

Fig. 10. Gain and noise of the capacitively-coupled amplifier.

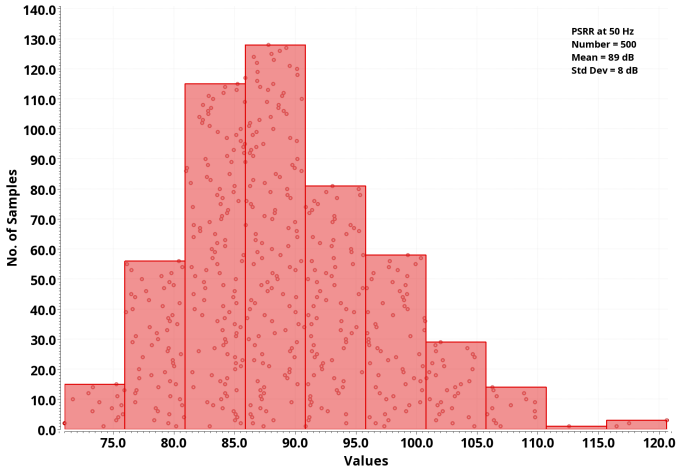

Fig. 11. The PSRR of the capacitvely-coupled amplifier.

higher cut-off frequency is 10 kHz for 1.2 pF capacitive load. The midband gain is 39.96 dB. Total input-referred noise at different bandwidth is reported in the figure. EEG (electroencephalography) bandwidth represents the bandwidth from 0.5 to 50 Hz, and LFP (local field potential) bandwidth represents bandwidth from 0.5 to 200 Hz. Besides, AP (action potential) bandwidth is from 200 Hz to 10 kHz.

In order to show the robustness of the proposed structure, 500 Monte Carlo simulations have been carried out for process and mismatch variations. These simulations are depicted in Fig. 11 and 12, respectively. The mean values for CMRR and PSRR are 65 dB and 89 dB, respectively. The differential gain mean value is 39.96 dB with 6.4 mdB standard deviation. This low gain error is achieved due to utilizing high gain core amplifier. Besides, the minimum and maximum differential gain is 39.95 dB and 39.99 dB, respectively.

In table II, the proposed capacitively-coupled amplifier is compared with the state-of-the-art amplifiers. In [16] and [19], they have utilized dual supply voltage. Therefore, they need dc-dc converter which increases complexity, area, and power consumption. The PEF of [19] by considering the power consumption of dc-dc converter is 1.8. Although in the bandwidth of [19] the dominant noise might be flicker noise, they used chopping technique to remove flicker noise. Therefore, comparing them with the rest of the articles is fair. The SEF of the proposed amplifier is in the range of the best SEF while the output swing is higher than the rest single supply voltage amplifiers. Besides, due to the high open-loop gain, the proposed closed-loop amplifier achieved a very low gain error.

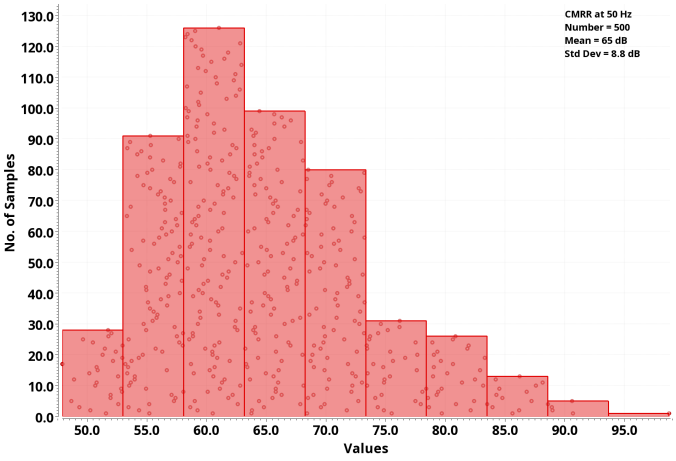

Fig. 12. The CMRR of the capacitvely-coupled amplifier.

TABLE II
COMPARISON THE PROPOSED RAIL-TO-RAIL AMPLIFIER WITH THE STATE-OF-THE-ART CAPACITIVELY-COUPLED NEURAL AMPLIFIERS

Specs	[9]	[17]	[16]	[19]	This Work
Technology (nm)	180	180	180	180	180
Supply Voltage (V)	1	1.2	0.45/0.9	0.2/0.8	1.2
Power (μW)	0.25	1.28	0.73	0.79	0.54
Gain (dB)	25.6	39.93	52	57.8	39.96
Bandwidth (Hz)	250-10k	0.6-5k	0.25-10K	0.5-0.67	200-10 k
CMRR (dB)	84	86	73	85	68
PSRR (dB)	76	-	80	80	89
IR Noise (μV_{rms})	5.6	3	3.2	0.94	4.4
NEF	1.07	1.68	1.57	2.1	1.15
PEF	1.15	3.4	1.12	1.6	1.59
SEF	0.02	0.05	0.02	0.3	0.02
Swing (V)	0.4	1	0.7	0.4	1
Area (mm^2)	0.29	0.03	0.25*	1	0.03
Sim./Meas.	Meas.	Sim.	Meas.	Meas.	Post Layout Sim.

*Approximate value

V. CONCLUSION

In this article, the dependency of intrinsic gain, transconductance and drain-source impedance of a single transistor was investigated in a commercially available 0.18 μm CMOS technology. Although transconductance variation is negligible for high drain-source voltage, these changes are dramatic near to the drain-source saturation voltage. The dependency of drain-source impedance to drain-source voltage is more severe than transconductance. Based on the simulation for the different operational region (from subthreshold to strong inversion), regardless of the operational region, the intrinsic gain increases by a factor larger than 2 until the drain-source voltage gets to 150 mV above the saturation voltage. In the proposed structure, the gain is defined by input transconductance and output impedance. Therefore, it is not limited to the intrinsic gain of any transistor and can be designed with more freedom. In this way, 88 dB gain is achieved without cascading output transistors. Therefore, the closed-loop gain is relatively low. Finally, the proposed structure achieved a rail-to-rail output while its SEF is same as the state-of-the-art single supply voltage amplifiers.

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