High voltage insulation design of coreless, planar PCB transformers for multi-MHz power supplies

Ole Christian Spro, *Student Member, IEEE,* Frank Mauseth, *Member, IEEE,*
Dimosthenis Peftitsis, *Senior Member, IEEE,*

***Abstract*—This paper investigates the insulation design for printed, planar, coreless, and high-frequency transformers with high isolation-voltage. By using finite element analysis on 2D axial-symmetry, the transformer circuit parameters and electric field distribution are modelled and estimated. Several transformers are designed for an operating frequency of 6.78 MHz. The high frequency, coreless design allows for using thicker insulation material while ensuring a high transformer efficiency. The inclusion of the coupling capacitance in the design optimisation results in several design solutions with the same figure of merit, but with different footprint and isolation voltages. Moreover, high electric fields are identified around the sharp edges of the PCB windings. Finally, the electrical and isolation performance is verified experimentally. The measured electrical properties are close to the simulated values, validating the chosen model. Breakdown tests demonstrate the feasibility of isolation voltage levels up to several tens of kilovolts. The majority of breakdowns occurs at the outer edge of the PCB winding that was identified as a high-field area. Additionally, a concept for grading the electric field of PCB windings is also proposed. Based on the results, the design aspects are discussed in detail for planar, high-frequency isolation transformers with medium-voltage isolation level.**

***Keywords*—Resonant power conversion, Transformers, Design methodology, Dielectric breakdown, Insulation,**

I. Introduction

High-frequency, isolated power electronic converters are key components that are used in a vast variety of industrial, residential and e-mobility applications. Isolation between the input and output stages of such converters is achieved by using high-frequency transformers. Based on the power ratings, operating constraints, and the targeted optimization objectives, frequencies exceeding a few MHz might also be utilized. In an industrial perspective, using planar transformers made with printed circuit boards (PCB) allows the transformer to be manufactured with higher parameter accuracy and precision compared to winded structures. On the other hand, such transformers are restricted to lower inductance values for the same component area which necessitates higher operating frequencies. The introduction and constant development of wide band gap semiconductors, ie. SiC and GaN components, makes high operating frequency into the MHz range increasingly feasible. Similarly, the research and development of wireless power transfer can be extended to design of isolated auxiliary power supplies without magnetic cores.

High frequency, planar PCB-transformers have been investigated in the literature with either a magnetic core [1]–[5] or as coreless designs [2], [6]–[15]. The design and optimisation of the transformer is often investigated in terms of winding structure to reduce losses and/or intra-winding capacitance [1]–[3], [6], [7], [10]–[12], [16]. In recent works on planar PCB transformers, the minimisation of the coupling capacitance over the insulation barrier in the transformer (see Fig. 1a) has been the target of optimisations on auxiliary power supplies that energizes gate drivers [4], [5], [15], [17]–[21]. The power requirement for the published auxiliary power supplies, and hence also for the transformer, is in the range of 2–200 W. In a power supply, the coupling capacitor constitutes a path for noise current that is generated during switching events with high dv/dt [22], [23]. Therefore, minimising the coupling capacitance will minimise the circulating current and, hence, reduce any related EMI issues.

Although the input and output voltage of isolated auxiliary power supplies for gate drivers is usually limited to a few tens of volts, the transformer requires a coordinated insulation system for the target isolation voltage. For medium voltage converters, the operating voltage ranges from 1–35 $\mathrm{kV_{RMS}}$. For a target isolation voltage up to a few kilovolts, the PCB itself is used as a solid insulation material in the transformer [9], [13], [16], [18]. Alternatively, air can be used as insulation medium in a wireless power transfer setup [15], [20], [24], [25]. However, the drawback is that this design approach necessitates larger clearances, especially at high isolation voltages i.e. 50 mm for a operating voltage of 35 $\mathrm{kV_{RMS}}$ [24]. To obtain more compact transformers, solid or liquid insulation should be used instead. Examples of planar transformers with PCB windings with isolation voltages of 5 kV or more are found in the literature using polypropylene [26], [27], polysterimide [4], [5], polyimide [19], or polytetraflouorethylene (PTFE) [5], as insulation material. The thickness of the insulation material is reported to be in the range of 1 to 1.6 mm. For coreless isolation transformers, the auxiliary power supply is often operating at multi-megahertz frequency [8], [19]–[21]. However, detailed investigations into the electric field distribution are not reported earlier for coreless PCB planar transformers.

Due to the high operating frequency and relatively large leakage inductance of the transformer, the majority of the

O.C. Spro, F. Mauseth and D. Peftitsis are with the Department of Electric Power Engineering, Norwegian University of Science and Technology, Trondheim, Norway. Corresponding author: olechristian.spro@ntnu.no

The authors acknowledges the funds received through the Norwegian Research Council grant 243711.

This paper has supplementary downloadable material available at http://ieeexplore.ieee.org, provided by the authors. This includes a data set with results and a code example to reproduce the FEA simulation presented in the manuscript. The total file size is 17 kB.

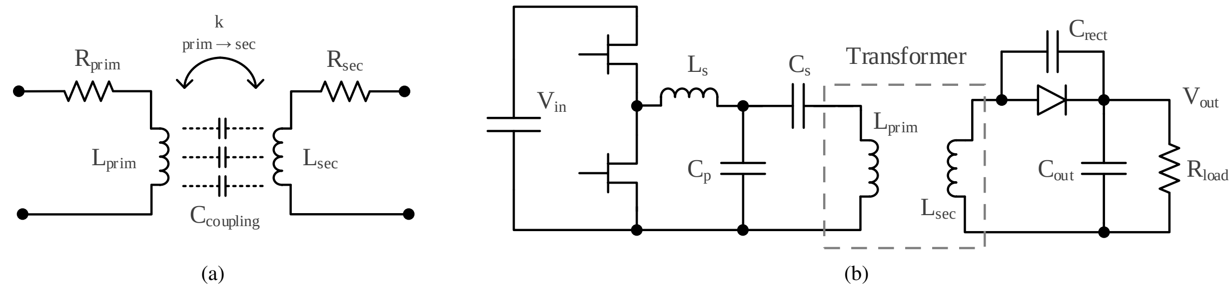


Fig. 1. Schematic diagram of a) the circuit model of the transformer and b) the topology for the auxiliary power supply that incorporates the loosely coupled transformer.

auxiliary power supplies uses resonant converter topologies to transfer power. The resonant topology in this work is shown in Fig. 1b [21]. Due to the high isolation voltage and sensitivity to coupling capacitance, the converter is operated in open-loop. While the input and output voltage is limited to approximately 48 V and below, the transformer's isolation level is targeted for use in medium-voltage converters.

In this work, the design of planar, coreless transformers for high-frequency and high isolation-voltage is investigated in terms of circuit and dielectric performance by both simulation and experimental work. The scope of the work includes demonstrating an efficient way of manufacturing a medium-voltage isolation transformer using PCB coils, limited to a single combination of insulating materials and short-term testing. The transformer circuit parameters and electric field distribution are identified from finite element analysis with 2D axial-symmetry. The operating frequency is set to 6.78 MHz, which allows coreless design to use thicker insulation material while upholding the transformer efficiency. A resonant converter system capable of utilising such a transformer and operating at the high frequency was recently demonstrated in [21]. From the design space, a total of ten transformer designs are prototyped. The electrical and isolation performance of the transformers is verified experimentally. The resulting breakdown voltages and placement for all designs are reported with sample sizes of 10. As an additional contribution, this work investigates concepts for grading the electric field of PCB windings that are suitable for the design of coreless, high-frequency transformers with high isolation voltage. The rest of the paper is structured as follows: Section II defines the transformer modelling and the design goals of the paper. Then, the simulation procedures and results are presented in Section III. Experimental validation is presented and discussed in Section IV before the design guidelines are stated in Section V. Finally, the conclusions are drawn in Section V.

II. TRANSFORMER MODELLING

The windings of the planar transformer are printed as spiral windings on a PCB. If a single turn is used, the coil consists of a helical winding. As a result, the geometry of the transformer can be described as a axial-symmetric cross-section that is illustrated in Fig. 2a. For all parameters, *prim* and *sec* indicate the primary and secondary side, respectively. The set of parameters consist of the number of winding layers ($Layers_x$), the number of turns on each layer (N_x), the width and the height of the copper track, (w_{cu}) and (h_{cu}), the distance between tracks ($w_{clearance}$), and the radius from the centre to the inner winding (r_x). The number of turns per winding layer on the PCBs are set equal. Furthermore, the height of the dielectric material placed between the primary and secondary side of the transformer is defined as $h_{dielectric}$. While Fig. 2a shows a transformer with primary and secondary sides made up of single layer PCBs, alternatively, the windings on either side of the transformer can be made as multi-layer PCBs. The geometry of double layer and four layer PCBs are shown in Fig. 2b. For single and two-layer PCBs, the definition of the board height includes the copper layers. When producing a higher number of layers, there are different methods of building the PCB stack. Figure 2b shows a common stack for four-layer PCBs. The two centre-layers are produced on a core as for a double-layer PCB and the additional layering is done by adding sheets of prepreg and copper. The consequence of the production method is that there are added degrees of freedom for PCBs of four or more layers. In this work, all PCBs are designed to have the same total height, i.e. h_{pcb} = 1 mm, and the internal layer heights are adjusted accordingly.

Unless a helical singe-turn coil is chosen, the coil windings are aligned – as in the model – or staggered depending on where the cross-section is made. This is illustrated in Fig. 3, where an example is given of a 2-layer 3-turn coil. In the horizontal cross-section (dotted line) the tracks appear aligned. For the remaining cross-sections, the degree of misalignment will increase, until maximum misalignment is reached. As will be shown later in the paper, the comparison between the simulated and measured values has shown small errors. Hence, the model is sufficient, at least for the size and geometry of coils investigated in this work.

A. Circuit parameters

A lumped circuit parameter model is used to describe the circuit performance of transformer as previously shown in Fig. 1a, where the primary and secondary sides consist of the self inductances (L_x) in series with an equivalent resistance of the winding (R_x). The lack of a magnetic core and the non-magnetic behaviour of the FR4 material of the PCB limits the loss factors to the winding losses. Due to the frequency dependence of the winding losses, the equivalent series-resistance is only valid for a single frequency. Additionally,

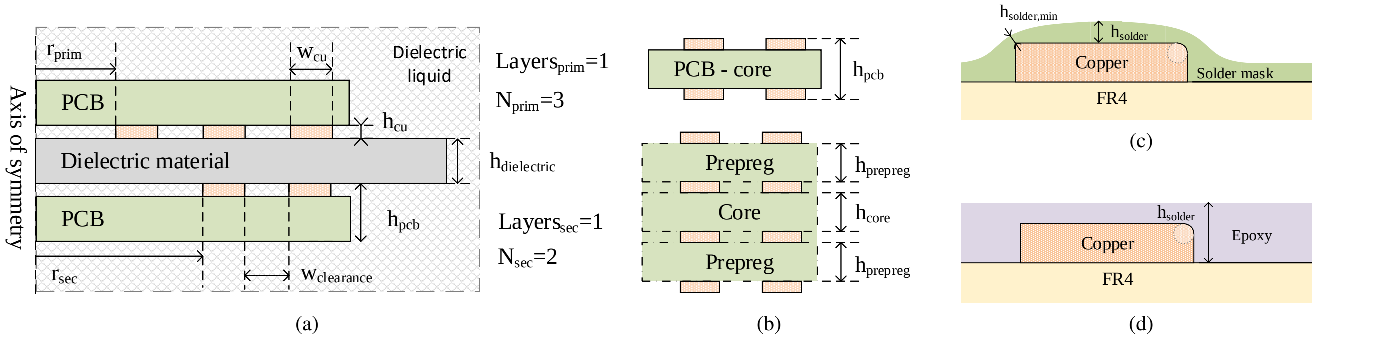


Fig. 2. a) Axial-symmetric geometry of the transformer. b) Cross-section of 2-layer PCBs and 4-layer PCBs showing the stack build-up of multi-layered PCBs. c) Typical geometry of solder mask layer. d) Geometry of applied epoxy layer for layer thicknesses of 50 and 100 µm.

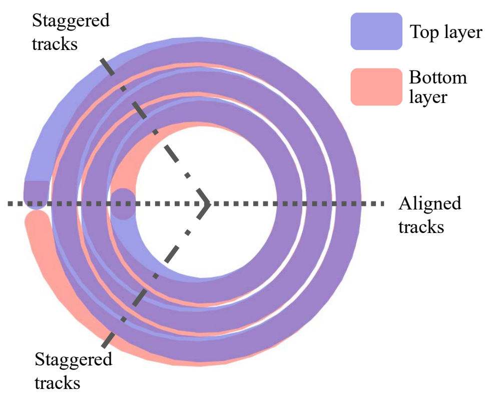


Fig. 3. Illustration on how the 2D model is a simplification of the transformer when using multi-layered spiral windings. The example shows a two-layered three-turn coil.

the transformer is characterised by a coupling factor, k, and a coupling capacitance, $C_{coupling}$, between the primary and secondary sides. Several combinations of parameters will be able to satisfy a given inductance value. Transformer designs across different number of layers, turns and dielectric height can be compared using a figure of merit (FOM) used for coupled inductors [28]:

$$FOM = k\sqrt{Q_{prim}Q_{sec}} = k\omega\sqrt{\frac{L_{prim}L_{sec}}{R_{prim}R_{sec}}} \quad (1)$$

where k is the coupling factor, ω is the angular frequency, and Q_x, L_x, and R_x represent the quality factor, inductance and resistance. The FOM is a direct measure for the transformer efficiency in a wireless power transfer system [28]. For a target inductance value, the transformer efficiency is improved by lowering the track resistance and increasing the coupling factor. To maximise the coupling factor, the primary and secondary side coils are made equal [29]. Furthermore, it can be shown that the track resistance increases with increasing turns number [16]. Although the minimum resistance is obtained for a single turn, this design might not be the optimal choice [30]. To understand this, the transformer coupling capacitance is approximated as a plate capacitor:

$$C = \frac{\epsilon_0\epsilon_r S}{d} \quad (2)$$

where the plate area, S, is proportional to the area of the spiral windings, the gap distance, d, is approximately equal to the thickness of the dielectric material, and the permittivity, $\epsilon_0\epsilon_r$, is given by the properties of the dielectric material. Having a single turn results in a high effective area, S. To keep the capacitance below the capacitance target, the gap distance is increased with a resulting decrease in the transformer coupling factor, k, and, hence, a reduction of the transformer FOM. Consequently, the optimal design is no longer trivial. The geometry of the windings and the choice of the dielectric material will affect the final coupling capacitance value. Although the coupling capacitance is a distributed parameter, as indicated in Fig. 1a, a lumped parameter capacitor is sufficient for modelling the coupling capacitance up until the self-resonance frequency of the coil.

B. *Dielectric parameters*

The transformer is also characterised by a withstand voltage that is governed by the dielectric material and geometry. The ideal dielectric material is non-magnetic, has a low permittivity and can sustain high electric fields. Assuming a uniform electric field distribution, the insulation voltage of the transformer will depend on the material thickness, $h_{dielectric}$, and the maximum field the material can sustain, E_{max}, without breakdown:

$$V_{breakdown} \leq E_{max} \cdot h_{dielectric} \quad (3)$$

Yet, the field in a practical geometry is rarely perfectly uniform, especially for sharp-edged geometry like PCBs. Hence, the actual breakdown will be lower than the maximum value as indicated by the inequality in (3). Furthermore, the transformer should be submerged in a dielectric liquid or potted in a gel to avoid flashovers. In this work, PTFE is used as the solid insulation-barrier and Midel 7131 is used as the dielectric liquid. In addition to being non-magnetic, their dielectric constants are relatively low. The dielectric constants for FR4, PTFE and Midel 7131 are 4.4, 2.0 and 3.15, respectively [31]–[33].

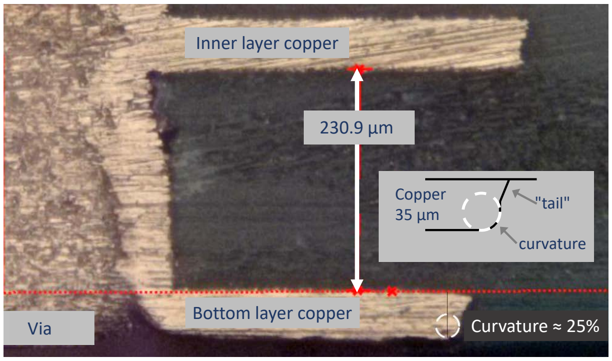


Fig. 4. Cross-section of a PCB production batch showing a part of a via, the bottom copper layer and an inner layer.

For the electric field simulations, exact modelling of the transformer is challenging if the goal is to obtain electric field values in absolute terms. This is due to the natural variation in PCB manufacturing in addition to the challenges related to curvature and mesh-size dependent electric field in FEA simulation. Regarding the latter, it has been shown that the simulated electric field close to sharp edges is dependent on the mesh size of the FEA [34]. With a variable edge curvature, it becomes difficult to establish the exact relation between simulated and actual peak electric field. In this work, the simulations are used to compare transformer designs relatively while the final breakdown voltage is tested experimentally. Consequently, simulations are limited to electro-static simulations with a simplified geometry. Figs. 2c and 2d show the geometry of the solder mask and epoxy layer if these are included in the electric field simulation. The solder mask layer's task is to protect the PCB from several external hazards as well as insulating the copper tracks from each other. As will be seen, this layer can have a large impact on the peak electric fields occurring close to the PCB windings. Furthermore, the corners of the copper tracks are rounded as seen in Fig. 2c, where the edge is replaced with an arc with a given radius. In this work, the radius is set to 20% of the copper height. This represents an average of the observed curvature of the prototype production batches. An example cross-section is shown Fig. 4, where the bottom layer edge shows a curvature of approximately 25 % of the copper height. Rounding of the corners is only applied to the critical points where high field is observed. The copper tail was not included in the modelling as it was found not to substantially change the results of the electric field simulations.

III. Simulation results

To investigate the trade-offs in the design of a high-frequency transformer with high isolation voltage, the transformer geometry is varied as specified in Table I. Using finite element analysis, the geometry is tuned to obtain the target inductance and capacitance values. The simulations are carried out using *FEMM*, a free software for solving 2D problems using finite element analysis (FEA) [35], and the code developed for this work has been made available [36]. The inductance

TABLE I. PCB and winding parameters for the different design cases.

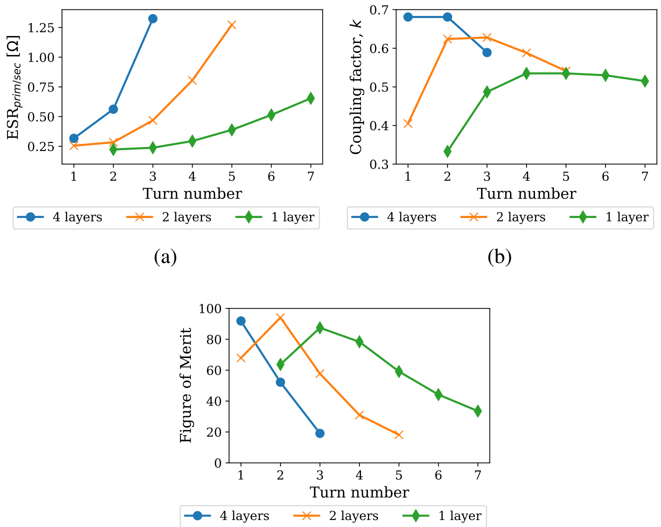
Number of layers	Range of windings *prim/sec*	Height PCB core / prepreg
1	from 2 to 5	1.0 mm / -
2	from 1 to 5	1.0 mm / -
4	from 1 to 3	0.75 mm / 0.08 mm

Copper height	Copper width	Track clearance	Target inductance	Target capacitance	Operating frequency
35 µm	3.0 mm	0.5 mm	1.0 µH	10 pF	6.78 MHz

target of 1 µH is set as reasonable values for the application [3], [11], [19], [21]. For the coupling capacitance, there is no consensus in the literature on the maximum allowable value. Rather, the goal is to keep the coupling capacitance as low as practically possible. The maximum allowable capacitance in a system depends on several factors including dv/dt and ground impedance [22], [23]. In this work, the coupling capacitance is set to a target of 10 pF, however, the design method presented here is also valid for other design targets. The capacitance goal is suitable for transformers in auxiliary power supplies for modules in a multilevel-type converter [21].

The self and mutual inductances, as well as the equivalent series resistance (ESR), are calculated in three consecutive simulations with current flowing in only the primary circuit, only in the secondary circuit, and in both sides, respectively. Moreover, the coupling capacitance is calculated from the charge stored on the secondary side conductors when applying a voltage potential between the primary and secondary side. For one iteration, the simulation time is shorter than 10 seconds. The design flow for each transformer design is as follows. Firstly, the inner radius is adjusted to obtain the target inductance value. Secondly, the height of the insulation material is dimensioned to obtain the target coupling capacitance. Since the inductance and capacitance values are slightly cross-coupled through the geometry, these two first steps are iterated until the inductance and capacitance are found to be within $\pm 1\%$ of the target value. When the inner radius and height are set, the electric field simulations are investigated in further detail to study the magnitude and position of the peak electric field.

The resulting ESR, coupling factor and FOM using the simulation tool are shown in Fig. 5. Figure 5a shows the ESR of each winding. As expected, the lowest turns numbers result in the lowest ESR. Similarly, a lower number of layers also decreases the resistance. Figure 5b shows the coupling factor of the transformers. A higher number of layers results in a higher coupling factor. This is due to the low height of the dielectric for transformers made with multi-layer windings, since multiple layers give the same inductance but with a lower effective area between the primary and secondary side. In this situation, the 4-layer designs exhibits the highest ESR and the highest coupling factor, both of which affect the transformer performance. To compare the transformer efficiency, the FOM of all transformer designs are shown in Fig. 5c. It is observed that multiple designs can obtain a similar FOM, and the 2 and 4-layer designs obtain the highest FOM values of 94 and 92,



(a) (b) (c)

Fig. 5. FEA simulation results of a) equivalent series resistance (ESR) of either primary or secondary coil and b) the coupling between the two coils. c) shows the resulting FOM.

respectively. For the 1-layer design, a maximum FOM of 87 is obtained.

Although important, the efficiency is not the only performance parameter of a transformer. For the application targeted in this work, the dielectric height will be important as this is related to the transformer isolation voltage. Furthermore, the outer winding radius of the transformer is used as an indicator of power density. The three parameters, namely the FOM, the height of the dielectric material and the outer radius of the windings, are shown in Fig. 6. For a low number of turns and layers, the effective area between the coils becomes high as the radius needed to achieve 1 µH becomes large (Fig. 6c). As a result, the dielectric height is increased substantially as seen in Fig. 6b, e.g. 19 mm for the 1-layer 2-turn coil compared to approximately 1 mm thickness for coils made on 4-layer PCBs. In terms of maximum transformer efficiency, the FOM matrix in Fig. 6a shows a diagonal trend. As indicated by the colouring, approximately the same FOM can be obtained across different number of layers and turns. On one hand, 4-layer coils obtain the smallest size due to the low surface between the two transformer sides. On the other hand, 1-layer coils can likely sustain higher isolation voltages due to the increased thickness of the dielectric. Hence, the optimal design choice will depend on the application requirements. From the design space identified in simulations, five designs with similar FOM and outer radius are selected for prototyping and experimental validations. Two of the five prototypes (#2 and #4) are the designs with the highest identified FOM. The remaining three prototypes (#1, #3, and #5) have similar FOM in the range of 50 across 1, 2 and 4-layer designs with a range in footprint size that is both smaller and larger than the design with highest FOM. These designs are presented and compared in Table II.

TABLE II. COMPARISON OF THE DESIGNS CHOSEN FOR PROTOTYPING.

Prototype	#1	#2	#3	#4	#5
Layers	1	2	2	4	4
Turns	5	2	3	1	2
FOM	59	94	58	92	52
Dielectric height	6.5 mm	3.1 mm	2.6 mm	1.3 mm	1.0 mm
Outer radius	28.4 mm	24.3 mm	19.2 mm	19.2 mm	12.2 mm
$V_{50kV/mm}$	27 kV	24 kV	24 kV	16 kV	16 kV

A. Challenges in the dielectric design

In high-voltage dielectric design, sharp edges and corners are avoided due to the electric field amplification in such areas [37]. The copper tracks on the PCB will naturally have sharp edges due to the fabrication process. While the edges of adjacent tracks will shield each other, the field amplification is high at the outermost and the innermost edge as indicated by the red boxes in Fig. 7a. Since the winding has a spiral shape, the innermost edge will also be partially shielded depending on the inner radius of the winding. Consequently, the outer edge is the most exposed, although, the difference between the inner and outer edge field can be quite small. Figure 7b shows an example view of how the peak field is high at the corner of a track edge. Although the average electric field in the dielectric is lower than 20 kV/mm (green-yellow), the field at the corner reaches as high as 50 kV/mm (red-purple). This high field area stretches out into the dielectric liquid and into the dielectric material. Consequently, it is hypothesised that the breakdown voltage of the transformer will be limited by the field in these corner areas. To investigate the relationship between the breakdown voltage and the insulation thickness, the maximum allowable electric field strength is set to 50 kV/mm, approximately the dielectric strength of both PTFE and Midel 7131 [5], [38]. The RMS voltages are reported in the final row of Table II. It is observed that the allowable voltage level increases with dielectric height. Yet, the voltage increase for an increase insulation thickness becomes smaller with dielectric height, i.e. 8 kV increase from 1 to 3 mm thickness versus 3 kV increase from 3 to 6 mm thickness. This is a result of the non-linear relationship between the geometry-amplified electric field and the distance between the coil windings.

B. Field grading methods

As a part of this work, methods for addressing the field amplification around the winding edges are investigated. Prototype #4 from Table II is chosen to perform these investigations since it is 4-layered, and it has a high FOM. Additionally, the helical four-layer single-turn design leads to less discrepancy between the prototype and the simplified model used in simulation due to via connections and winding layout. To compare the effect of different designs on the electric field, the peak electric field is recorded at the same location on the rim of the outer and inner corners. For all simulations, the voltage

(a)

Turns \ PCB Layers	1	2	4
1	-	68	92
2	64	94	52
3	87	58	19
4	78	31	-
5	59	18	-

(b)

Turns \ PCB Layers	1	2	4
1	-	10.6	1.3
2	19	3.1	1.0
3	9.0	2.6	1.1
4	7.0	2.6	-
5	6.5	2.8	-

(c)

Turns \ PCB Layers	1	2	4
1	-	52.9	19.2
2	59.2	24.3	12.2
3	38.4	19.2	12.2
4	31.2	18.2	-
5	28.4	18.6	-

Fig. 6. Main parameters of the design space used for the evaluation of best individuals. a) Figure of merit, b) height of dielectric material in mm, and c) winding outer radius in mm.

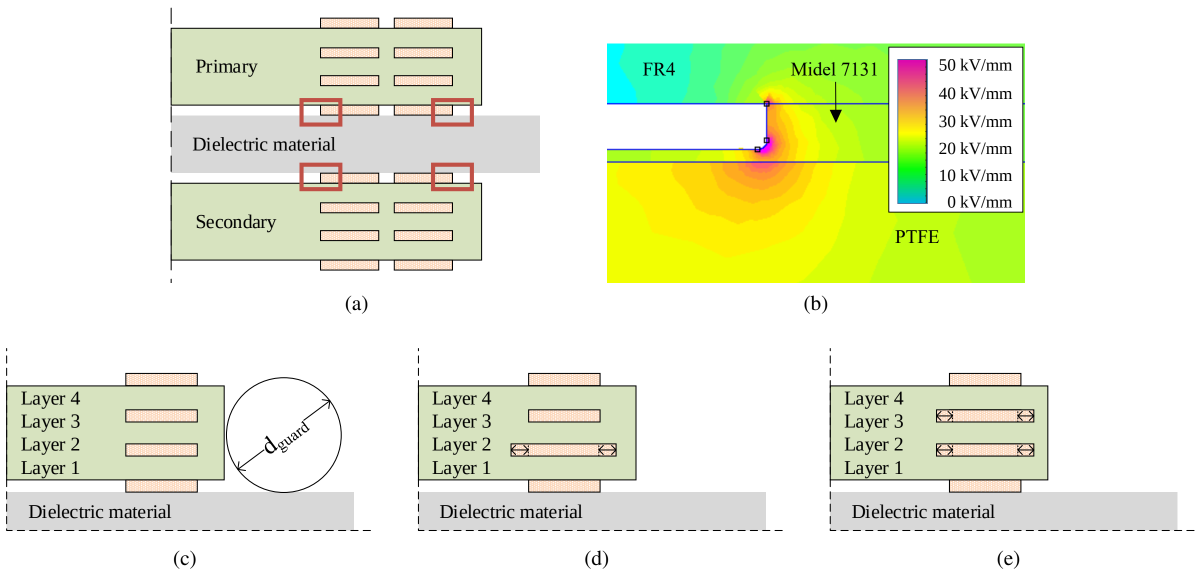


Fig. 7. Dielectric design a) problem areas and b) an example of the field amplification in the corner of the outer winding. Investigated field grading methods include c) adding a guard ring around the edge of the PCB, or by elongation of copper width of d) one or e) two inner layers.

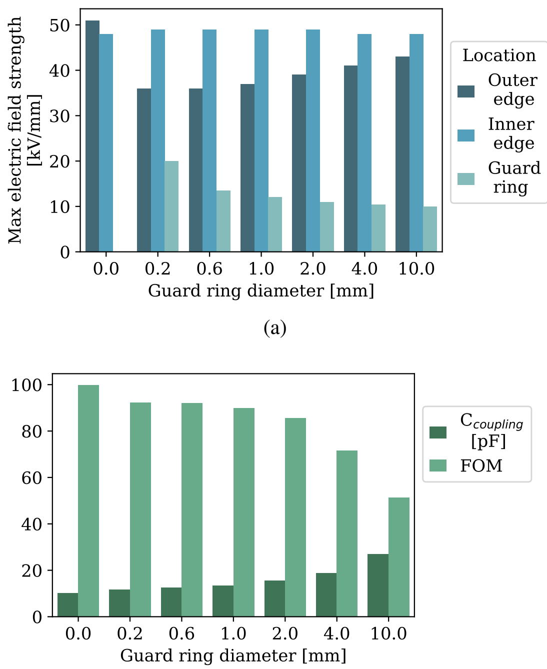
between the primary and secondary side is kept constant at 16 kV.

Measures for addressing the issue of high electric field can be categorised in two main categories: geometry field-grading or permittivity field-grading. Increasing the distance between conductors and rounding conductors are typical field grading methods that uses the geometry to decrease peak fields. Permittivity field-grading uses the material constants of the different components to push the electric field away from critical areas. In this work, the following field-grading methods are investigated:

1) Adding guard rings along the PCB edge (geometry)
2) Increasing track width of inner layers (geometry)
3) Changing the type of epoxy and geometry for the solder mask layer (permittivity)

Methods 1 and 2 are shown in Fig. 7c, 7d and 7e while Fig. 2c and 2d show the geometry of method 3 where a layer of solder mask or epoxy is deposited on the PCB surface that faces the insulation material.

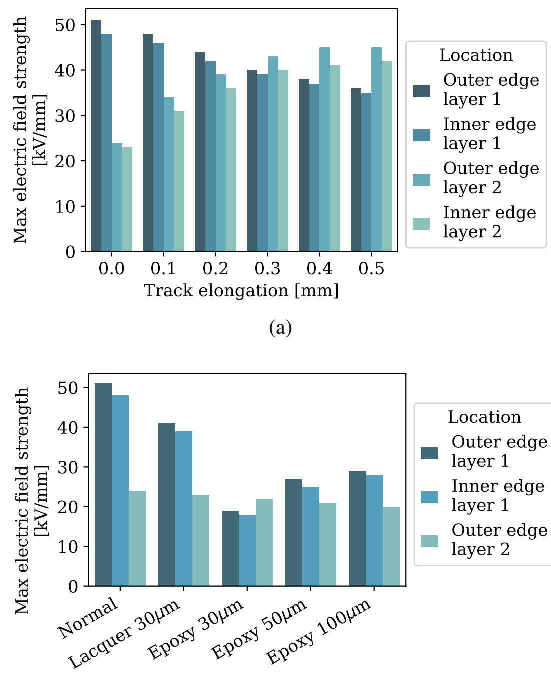
Adding guard rings is a common way in high-voltage engineering to grade the electric field in problematic areas [39]. The guard ring cross section is circular with a given diameter, d_{guard}, and is placed outside the PCB edge. Due to limitations imposed by PCB manufacturers, there is a minimum distance between the copper track edge and the PCB edge distance. Consequently, there is a slight separation between the two. The copper-to-PCB edge is set to 0.5 mm. The guard ring diameter is varied from 0.2 to 10 mm and the resulting peak field is given in Fig. 8a. It is observed that the field on the outer edge is lower with a guard ring. Hence, the guard ring provides shielding of the copper track edge, but naturally only on the outer corner. For small diameters, the guard ring can be placed close to the copper track and efficiently shield the high field. However, small diameter ring will also experience higher local field strength as seen by the value *guard ring* in Fig. 8a. This



(a)

(b)

Fig. 8. Transformer characteristics found through simulation for varying guard ring diameter: a) Maximum field strength of inner and outer corner. b) Coupling capacitance and figure of merit.



(a)

(b)

Fig. 9. Maximum field strength of different winding edges found through simulation for different designs: a) Elongation of the track on layer 2. b) Different coating types and geometry over the copper track compared to bare-copper windings.

can be countered by increasing the guard ring diameter. Yet, due to the larger cross-section of the guard ring, it is now moved further away from the copper corner, and the effective shielding diminishes. Moreover, a shielding technique is also needed on the inner winding for the isolation voltage to be increased.

Additionally, the guard ring is subjected to the magnetic field produced by the transformer windings. Despite having guard rings as open circuits, the transformer losses are increased due to eddy currents in the surface of the copper guard ring. Figure 8b reports the decrease in transformer FOM with increasing guard ring diameter. A guard ring material with higher resistivity would lead to lower eddy-currents and likely lead to a smaller decay of the transformer efficiency. Moreover, Fig. 8b also shows the coupling capacitance of the transformer. From the smallest diameter and upwards to largest guard ring, the capacitance increases from approximately 12 pF up to 27 pF. Since the guard rings increase the effective surface area of the coils in (2), the coupling capacitance increases.

If the windings are printed on multilayer PCBs, then the PCB geometry can be used for field shaping. The track width of each individual layer can be manipulated to change the peak electric field. As indicated in Fig. 7d, the width of the copper track on the inner layer (layer 2) can be increased to partly shape the field around the edge of outer layer. Figure 9a shows how the peak electric field can be shifted from the outermost layer (layer 1) to the next layer (layer 2) by increasing the track width of layer 2. However, increasing the width too far will only move the problem from one layer to another. The dielectric strength of FR4 is quoted lower (30 kV/mm [9]) compared to the used insulation material (PTFE).

Figure 9a shows that a elongation of 0.1 mm in our case violates the FR4 limit. Yet, if the width of layer 3 is also increased by 0.1 mm (ref. Fig. 7e), the field on layer 2 inside the FR4 material is within the limit. The advantage of this technique is that it is easy to implement and the change in electrical parameters (resistance, coupling and coupling capacitance) is negligible when elongating the inner layer tracks. However, the effect on the peak field is limited, i.e. elongation of both layers by 0.1 mm decreases the field on the layer 2 edge from 33 to 30 kV/mm while the layer 3 edge field is increased close to the material limit. Additionally, the FR4 material is known to have variations in dielectric performance based on the variations in manufacturing, making it a less reliable choice for insulation.

Until now, all simulations have been performed while excluding the solder mask layer – with its characteristic green colour – that is normally applied to PCBs. Two types of coatings are added to the simulation with variable geometry and thickness. Figure 2c shows the typical geometry of the solder mask over a copper track. Due to the layer thickness and the viscosity of the solder mask lacquer, the thickness over the copper edges ($h_{solder,min}$) will be lower than on top of copper and FR4 surfaces (h_{solder}). In this work, the solder layer height is set to 30 µm with a minimum value of 10 µm over the copper edges and the dielectric constant is set to 4, However, the thickness and material properties are given by the PCB manufacturer and can vary significantly between manufacturers. The maximum field values are shown in Fig. 9b (*Lacquer 30μm*). Adding the solder mask layer to the simulation shows a decrease in the peak electric field of about 20%. Further expanding on this idea, the solder mask lacquer can be exchanged for an epoxy with a higher dielectric constant. The relative permittivity of the epoxy is set to 9. Additionally, the geometry of this epoxy layer is varied between that of the solder mask (*Epoxy 30μm*) and a box layer (ref. Fig. 2d) with thicknesses of 50 and 100 μm (*Epoxy 50μm* and *Epoxy 100μm*, respectively). Four observations are made from Fig. 9b. Firstly, high permittivity epoxy substantially lowers the peak electric field occurring at the corner. Secondly, the electric fields are reduced both at the outer and the inner corner. Thirdly, increasing the thickness of the coating does not decrease the peak field. Lastly, the coating has minimal effect on the field of the layer 2 corner. This is in contrast to employing a guard ring. Thus, using a coating layer to shape the high-field region does not exclude the need to limit the high field occurring on adjacent layers. Changing the normal solder mask to a high permittivity epoxy is found to decrease the field in the outer corners by over 60% compared to bare-copper windings. The high dielectric constant of the epoxy layer would increase the coupling capacitance. However, the increased height between coils due to the additional coating thickness largely compensates this increase. As long as the coating layers are non-magnetic, the electrical parameters stay almost unchanged as simulations show a maximum parameter variation of ±2 %.

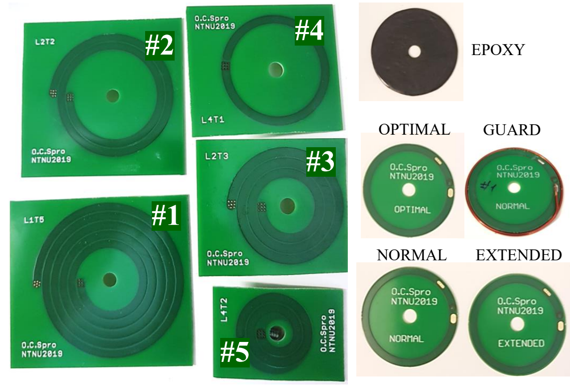
IV. Experimental validations

The experimental validations performed in this work have two objectives. Firstly, the accuracy of the simulation using a simplified FEA model is investigated. This is achieved by characterising prototypes in terms of electrical parameters and comparing them to the simulated values. Secondly, it is of interest to quantify the breakdown voltage of the investigated transformer designs. Due to the uncertainty in actual PCB geometry, it is necessary to experimentally establish the breakdown voltage. In addition, weak points in the design can be identified by using destructive breakdown tests.

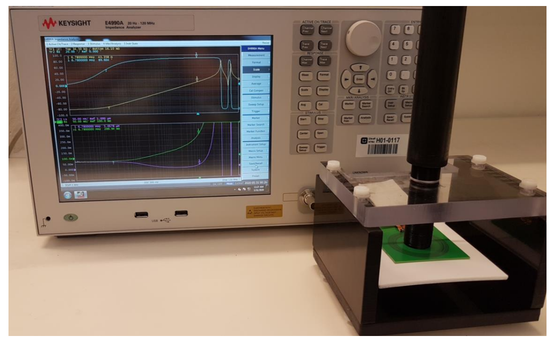
A. Transformer parameter characterisation

The five designs listed in Table II were printed on 4-layer PCBs and photos of the prototypes are shown in Fig. 10a. Two identical windings are used as primary and secondary coils. In addition, five different variations of prototype #4 (4-layered single-turn) are produced for evaluating the effect of field grading methods on the breakdown voltage. The five variation of #4 are as follows:

NORMAL — Normal layout, equal to L4T1 (4 layers, 1 turn).
GUARD — Normal layout with an outer guard ring with a diameter of 1.1 mm (Fig. 7c).
EXTENDED — Normal layout with 0.5 mm elongation of the winding on layer 2 (Fig. 7d).



(a)



(b)

Fig. 10. a) Photo of the ten transformer designs used in the experimental validation. On the left, the designs from Table II are labeled and the five variations of field-grading are shown on the right. b) Photo of the laboratory test setup for impedance measurement of the transformer using a fixture.

OPTIMAL — Normal layout with 0.1 mm elongation of the windings on layer 2 and 3 (Fig. 7e).
EPOXY — Normal layout produced without solder mask and covered with an epoxy with a relative permittivity, ϵ_r, higher than 9 (Fig. 2d).

These five variations of #4 are milled out of the PCB with a 0.3 mm distance from copper track to the PCB edge. Since no field grading technique is applied to the *NORM* variation, this serves as a base case. Consequently, all tests of field grading methods are compared within the same PCB production batch.

All prototypes are characterised by placing two identical coils together in a fixture along with the dielectric material. An impedance analyser (Keysight E4990A) is used to perform the measurements (Fig. 10b). At the time of testing, PTFE was available in thicknesses of 1, 3, and 6 mm. These were used to construct the 4, 2 and 1 layer transformers, respectively. These material heights are very close to the values identified in simulation.

Five impedance measurements were done per transformer over the frequency range of 1 kHz to 120 MHz, which is the upper frequency limit of the test equipment. Both primary and secondary side are measured twice while the opposite side is either short-circuited or is kept in open circuit. These measurements are used to characterise the inductance, resistance and

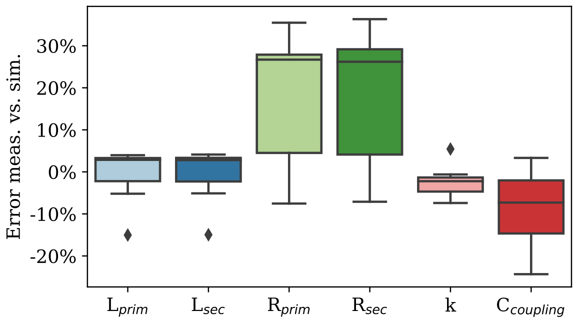


Fig. 11. Relative error of electrical parameters between simulation and measurement for all ten transformer designs.

coupling parameters of the transformer [30]. The capacitance between the primary and secondary side is measured while the terminals on both the primary and secondary side are shorted. This measurement method is used to characterise the coupling capacitance as described in [40]. For all values, the error between the measured and the simulated value are calculated as

$$err = \frac{X_{meas} - X_{sim}}{X_{sim}} \tag{4}$$

where X corresponds to the parameter in question. Table III summarises the measured and simulated primary side inductance for all ten design variations, along with the error value. It is observed that the inductance is within $\pm 4\%$ of the simulated value for most of the prototypes. Table IV shows the measured coupling capacitances which are all lower than 10 pF. To get an overview of how accurately the simplified simulation model reproduces the actual transformer performance, the variation in inductance, resistance, coupling factor and capacitance for all ten designs are summarised in Fig. 11. In the figure, the boxes show the span of quartile 1-3, the whiskers show minimum and maximum values and the line indicates the median value. Markers show outliers within the population. The outliers in inductance are related to L4T2, which is the most compact of all designs. Since the simplified geometry modelled in FEMM does not take via connections and actual spiral windings into consideration, the model is expected to be increasingly inaccurate for increasing transformer density and number of winding layers. Still, the transformer parameters are close to the simulation values, overall. As previously stated, the majority of the inductance values are within 4% error, with the L4T2 design being an outlier with an error of -15%. The coupling factor for all transformers is within $\pm 7\%$ of the simulated value, which again shows a good correlation between simulations and measurements. The coupling capacitance values have a higher error in percentage, with most of the transformers measuring between 0 and -15% of the simulated value. Apart from measurement error and coil misalignment, an increased insulation thickness would also decrease the coupling capacitance. Since the measured PFTE thicknesses are equal or slightly larger than the simulated thicknesses, this exclusively negative trend is deemed reasonable. For the ESR, although it shows large variations compared to the simulated value (-8 to +36%) this is within the measurement error band of the impedance analyser at 6.78 MHz. In conclusion, the simulated component results can be reproduced experimentally with a sufficiently good accuracy. Although, additional errors are expected for compact winding structures and multi-layer transformer designs.

B. Breakdown voltage tests

There are two types of tests available for establishing the maximum operating voltage of the insulation. These are the breakdown voltage tests and partial discharge (PD) inception and extinction voltage tests. In the breakdown voltage testing, the voltage over the insulation barrier is increased until a breakdown occurs in the insulation. Published standards for target operating voltage state the necessary breakdown voltage performance, e.g. IEC 60071. In contrast, PD measurements are non-destructive. The applied voltage is increased until PD is detected. Subsequently, the voltage is lowered until PD activity stops again. These voltage levels, known as the PD inception and extinction voltages, directly indicate the operating voltage of the transformer for long lifetime. However, repeated breakdown tests give additional information on the design weakness by studying the location and the mechanism of the breakdown.

Step-up breakdown voltage test was chosen to evaluate the design variations and concepts. A standard test using 50 Hz ac voltage is applied between the primary and the secondary side of the transformer. The voltage was increased in steps of 1 kV followed by a waiting period of 1 minute for each step. Ten samples of each design or more are tested due to the stochastic nature of device breakdown. This is in accordance with IEC 60060 procedure for a class 3 withstand voltage test. However, in a switch-mode power converter, the actual voltage transients are expected to be trapezoidal. Consequently, the likelihood of partial discharges increases and, in turn, deterioration of the insulation material at lower voltage levels is anticipated [37]. Nevertheless, as specified in IEC 60664, the selected test is accepted as long as the operating frequency is equal or lower than 30 kHz. For medium voltage converters, this frequency limit can be considered in the higher range of switching frequency. The breakdown test was in part chosen to be able to identify the weak points in the design where a breakdown is most likely to happen.

Figure 12 shows the details of the high voltage test setup. Breakdown tests are performed for the five different prototypes given in Table II as well as the five design variations of prototype #4 for testing field grading methods. Figure 12b shows a photo of one sample of the L4T1 design after breakdown, where black spots are visible on the outer edge of the copper track. The average and standard deviation in recorded breakdown voltages are presented in Table V. Visualisation of the breakdown voltages are shown in Fig. 13a and 13b.

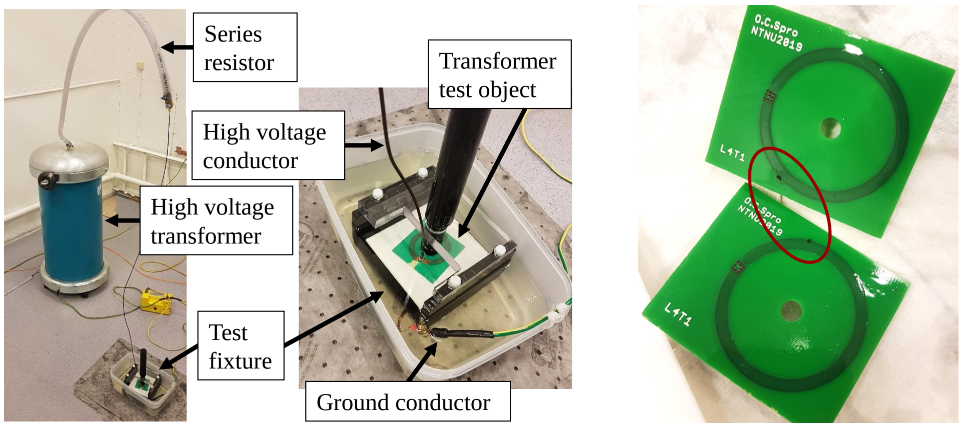
Figure 13a shows that the breakdown voltage follows the thickness of the insulation material, with average breakdown voltages for 1, 3, and 6 mm thicknesses of 37, 48, and 73 kV, respectively. It should be noted that the tests of *L1T5* were stopped at 80 kV due to the voltage limitation of the test

TABLE III. COMPARISON OF SIMULATED AND MEASURED SELF-INDUCTANCE OF THE PRIMARY SIDE COIL FOR ALL TEN DESIGNS.

	L4T1	L4T2	L2T2	L2T3	L1T5	NORM	EXT	OPT	GUARD	EPOXY
$L_{prim,sim}$ [μH]	0.980	0.987	1.036	1.051	1.014	0.989	0.949	0.979	0.980	0.989
$L_{prim,meas}$ [μH]	1.011	0.839	0.982	1.013	1.033	1.020	0.981	1.015	1.005	1.028
err	3.1%	-15.0%	-5.2%	-3.6%	2.1%	3.1%	3.3%	2.6%	2.6%	4.0%

TABLE IV. MEASURED VALUES OF THE COUPLING CAPACITANCE OF ALL TEN DESIGN VARIATIONS.

	L1T5	L2T2	L2T3	L4T1	L4T2	NORM	EXT	OPT	GUARD	EPOXY
$C_{coupling}$ [pF]	8.14	7.70	6.70	9.86	8.71	7.98	8.85	7.95	8.68	7.95



(a) (b)

Fig. 12. Photos of a) the test setup for the breakdown test using a step-up transformer. The transformer prototypes are placed in a fixture and housed in a container filled with Midel 7131. c) Photo of the breakdown (black spots) on the outer edge of design L4T1 sample 6.

setup and, as such, the actual breakdown voltage of this design is higher. Following the standard test voltages given in IEC 60071, the transformers are above the test voltage levels for standard insulation levels in the medium voltage range of 12, 17.5 and 24 kV, respectively. This shows that the transformer concept is relevant as a component in auxiliary power supplies for medium voltage converters. However, further testing would be necessary to prove and qualify the transformers for long-term operation at these voltage levels. Insulation lifetime testing could include PD measurements and more breakdown tests at lower voltage levels to obtain a lifetime curve (expected time to breakdown at a given voltage).

In Fig. 13b, the comparison is made between different field grading techniques where *NORM* serves as the benchmark. Although the difference in breakdown voltage between the designs is limited, it follows the expected trend. *EXT* and *OPT* use the PCB geometry to shield edges of the outermost winding, yet, the achievable reduction in peak field is limited and this results in higher electric fields within the FR4 material. While the track elongation of *EXT* was made rather large, the difference between the cross-section of *OPT* and *NORM* is minimal. As such, *EXT* is likely to have a lower breakdown voltage while *OPT* should be very similar to *NORM*. Adding guard rings should decrease the peak field at the outer edges. *GUARD* is observed to have a slightly higher tendency than *NORM*. *EPOXY* samples have a higher breakdown voltage and lower deviation, indicating that the epoxy layer is improving the electric field distribution in the transformer.

For all breakdown events, the breakdown point was registered and categorised. The number of breakdown points is aggregated for all transformers and presented in Fig. 13c. The categories, 'Outer edge' and 'Inner edge', refer to the edge of the conductors which are indicated as a problematic area in the simulations (Fig. 7a). As can be seen, the majority of the breakdowns happened on the outer edge of the PCB windings. This validates the peak electric fields area found in simulation. 'Middle track' accounts for all breakdowns that are not close to the edge or somewhere on the inner tracks. This group consists of approximately 1/3 of the breakdowns. Possible reasons for breakdown in this area are the variation in fabrication of the PCBs, defects in the insulation material, and other possible high-field regions in the spiral structure that is not captured by the 2D transformer model. The final category, 'GR to GR', are the breakdowns that occurred where the arc crossed from guard ring (GR) to guard ring from the primary to the secondary sides. Hence, for the *GUARD* samples, a new breakdown path was introduced and shows the sensitivity of guard ring implementation of this design.

C. Discussion of experimental results

The results of the electrical characterisation show that the simplified model is accurate for the transformers in the investigated range, with an exception for the most compact PCB transformer design (L4T2). Low variation between simulation and final prototypes is critical as any variation in the parame-

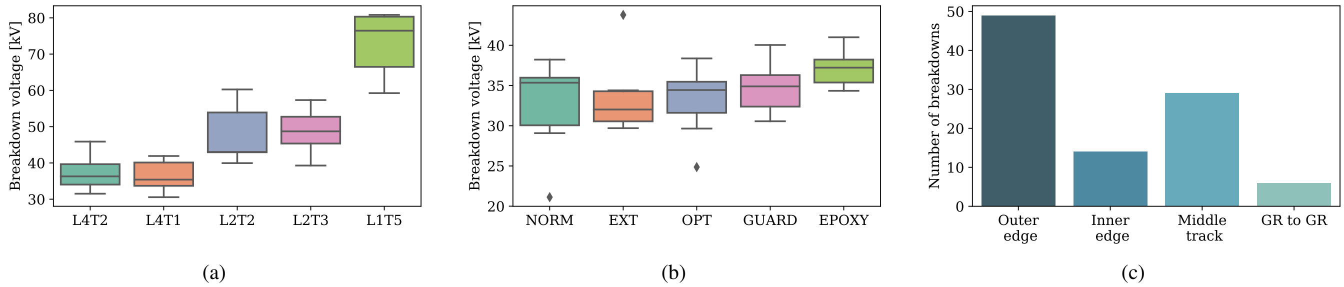


Fig. 13. Experimental breakdown voltages of the different designs. a) Five prototypes with varying turn layers and turns. b) Five variations of prototype #4 with different field grading method. c) Aggregated distribution of breakdown point for all tested designs.

TABLE V. MEAN BREAKDOWN VOLTAGE AND STANDARD DEVIATION FOR ALL TEN TRANSFORMER DESIGNS.

	L4T1	L4T2	L2T3	L2T2	L1T5
mean [kV_{RMS}]	36.7	37.3	47.8	48.7	73.3
std [kV_{RMS}]	3.88	4.58	7.77	6.33	8.16
	NORM	EXT	OPT	GUARD	EPOXY
mean [kV_{RMS}]	32.8	33.1	33.6	34.9	37.0
std [kV_{RMS}]	5.09	4.17	4.14	3.28	2.11

ters will affect the performance of the resonant converter that employs such a transformer.

The breakdown location of the tested transformers correlates well with the the simulations that showed peak electric fields occurring at the outer winding edge. An important finding from the electric field simulation is the influence of the solder mask layer on the insulation properties of the transformer. Hence, this layer cannot be disregarded when designing planar transformers using PCB printed windings. However, the simulation can only be used as a qualitative investigation since the model cannot be an exact replica of the prototypes due to variations that occur both in the manufacturing processes and for the material quality of PCBs. Hence, the withstand voltage is identified experimentally.

The transformer design space identified in simulations and the experimental breakdown voltages for different insulation thicknesses show that the optimal number of layers and the turns number of a planar transformer with PCB windings depend on three parameters; the targeted self-inductance, coupling capacitance and isolation voltage. The converter shown in Fig. 1b can incorporate all of the presented transformer prototypes to serve as a auxiliary power supply with an isolation voltage mainly depending on the insulation thickness. Moreover, the low coupling capacitance of the transformer limits the possible operating challenges of the medium-voltage converter due to EMI issues caused by high dv/dt.

In this work, a set of design parameters were kept constant to limit the scope of the investigations, e.g. equal turns number for primary and secondary side in addition to keeping the winding width and clearance constant between all designs. Further optimisation of the transformer efficiency is likely possible by freeing these design variables. Moreover, the insulation system is not limited to the chosen materials presented in the paper.

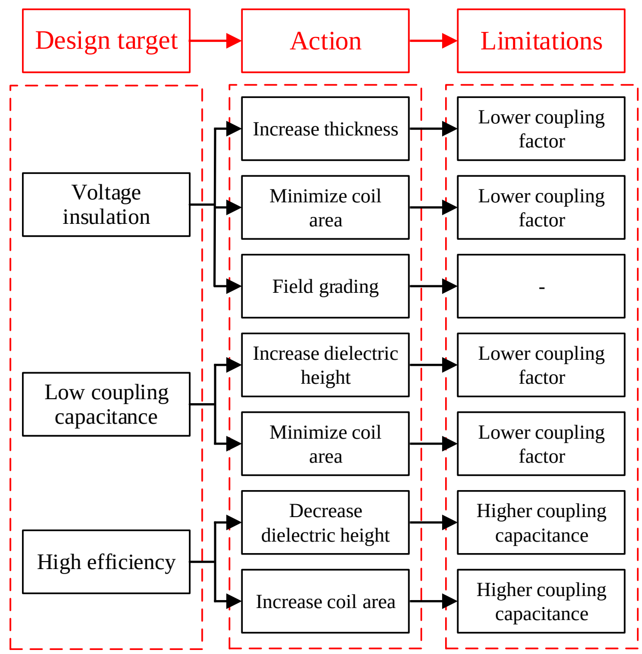


Fig. 14. Overview of the goals, actions and limitations given in the design guidelines.

The lifetime of the insulation is dependent on both surface area and volume of the insulation system, which can affect the final design. These aspects are the target of future work.

V. Summary of Design Aspects

This section presents a summary of all the design aspects that have been discussed in the previous sections. These can be used as guidelines for designing high-frequency and high voltage isolation transformers considering various design and optimisation directions. Achieving a transformer with the target inductance, coupling capacitance and isolation voltage is an iterative process due to the cross-coupling of these characteristics to the geometry parameters. The optimisation of the power converter circuit and the transformer design could be performed holistically. Due to the relatively low computational load of 2D FEA simulations, this is considered feasible for practical design processes [21]. The presented design actions and their subsequent consequences directs the reader towards a design of an isolation transformer that maximises the transformer efficiency while upholding the restrictions for coupling capacitance and isolation voltage performance. For the sake of flexibility, the guidelines are divided into two categories, namely insulation design and circuit considerations, whereas within each category the impact of the various design parameters on the transformer design are discussed. Figure 14 gives an overview of the design guidelines where design actions and resulting limitations are defined for the bullet points. Among the presented guidelines, a few of them are inversely correlated. Hence, the reader is left to select the topics of the highest priority for their target application and design. For example, the target for the coupling capacitance serves as an upper limit since lowering the coupling capacitance leads to better EMI immunity. However, as a general rule, lowering the capacitance will also negatively affect the transformer efficiency.

A. Insulation design considerations

The following guidelines aid the designer for the initial design. However, the withstand voltage capability for the intended application must be verified experimentally for several reasons. Firstly, PCB manufacture gives a natural variation in edge curvature which is challenging to model and simulate accurately. Moreover, the geometry of spiral windings is not fully accounted for in the 2D FEA simulation model. In contrast, helical windings (single turn) are more consistent with the 2D model. Furthermore, the PD inception voltage has been shown to depend on the dv/dt of the voltage over the isolation barrier [37]. Hence, testing of the insulation should also be performed with switching waveforms with dv/dt values close to those ones experienced in the practical application. Measuring the inception voltage of partial discharges can be performed in addition to destructive short-term withstand voltage tests for determining the withstand voltage level.

- Insulation material thickness

As discussed in this paper, the required thickness of the insulation material exhibits a non-linear relation with regards to the isolation voltage requirement. This stems from the peak electric field occurring in the copper edges. As shown by simulations and experiments, this means that the average electric field decreases with increasing thickness. Furthermore, dielectric design theory states that the likelihood of breakdown is correlated with the surface and the volume of the insulation system, i.e. thicker and larger area of material increases the chance of breakdown [39]. The withstand voltage is maximised if field-grading techniques are employed rather than only increasing the insulation thickness. If PFTE is used as the solid insulation, the experimental results on the anticipated breakdown voltage that is presented in this paper can be used as a basis for the initial design. For other insulation materials, similar and relevant studies are listed in Section I. However, due to the natural variance of PCB characteristics caused by the fabrication process, testing of the breakdown, regardless of the insulation material utilised, should be performed experimentally.

- Coil size area

As noted previously, the likelihood of breakdown is correlated with the volume of the insulation material. Hence, to decrease the possibility for a breakdown to occur, the coil area should also be minimised. This also results in low coupling capacitance, but negatively affects the efficiency due to lower coupling coefficient.

- Equal coil sizes on primary and secondary sides

The areas of the coil windings on the primary and secondary sides should have an equal size, if the maximum efficiency and withstand voltage of the transformer are targeted. Different sizes of the windings could be introduced to further decrease $C_{coupling}$; however, this is achieved at a cost of higher electric fields around the edges of the smaller winding [19]. This has a negative impact on the insulation properties of the transformer since the withstand voltage is defined by the peak electric field occurring in the transformer design. Same size coils also result in the highest coupling factor, which is beneficial for maximising the transformer efficiency.

- Choice of insulation materials.

The choice of materials is not limited to the ones presented in this paper. The reader is referred to Section I that lists examples of published designs that use other solid insulation materials. In addition, the interface material between the copper and the solid insulation is not limited to a liquid interface. Other materials that could be considered for the interface are silicone gel and dry-casting. Silicone gel has a relatively low dielectric constant and it is also used in other high-electric-field applications. Dry-cast transformers are maintenance-free, while humidity-control will have to be considered for liquids- and gels-based designs. In contrast, a solid insulator (dry-cast) is closer to a thermal insulator and would negatively affect the power capability of the transformer. In this regard, a liquid insulator is preferred to achieve a more efficient cooling of the transformer. For this work, the choice of the liquid was done in part in order to facilitate the practical aspects of performing the large number of breakdown tests necessary for fulfilling the testing standard.

- Field-grading techniques

The classical approach of adding a guard ring to control the electric field was not found to be efficient, since additional eddy-current losses are introduced. Using the inner layers of the PCB to alter the peak field was shown to be possible. Yet, the effectiveness is deemed limited as additional electric field stress is put on the FR4 material that is considered less reliable insulator. Among the presented field-grading techniques, adding a coating layer with a high dielectric constant appears to be the best performing solution. The simulation and experimental data reveal that the correct choice of solder mask or coating material can improve the dielectric performance of the transformer. While the medium-voltage insulation between the two PCBs is handled by the solid insulation, a coating with a high dielectric constant can decrease the peak field occurring at the edges. However, this coating layer will be exposed to high electric fields which must be taken into account during the design phase. In addition, the coating material should comply with the existing criteria for solder mask (IPC-SM-840). Epoxy, in general, exhibits characteristics and qualities that fit these requirements. Also, the pot life and viscosity might affect the choice of deposition method. Vacuumisation should be performed while depositing the coating layer to avoid any voids or air bubbles in the coating layer.

B. Circuit considerations

- Turns number

In this paper, the turns number on the primary and secondary sides is equal due to the converter optimisation on a specific use case [21]. The optimal turns ratio may be different depending on the input and output voltages of each use case. Still, from the dielectric point-of-view, the coil sizes should be equal to avoid field amplification. For a fixed coil size area and track clearance, and with changing turns number, the turn width is adjusted accordingly. An example exploration of the design space for the L2T3 design is performed in simulation and shown in Table VI. In general, an increased turns number results in higher resistance and slightly increased coupling factor. A different approach to changing the turns number is by increasing the number of winding layers, e.g. combining a 2-layer winding on the primary and a 4-layer winding on the secondary side. Table VI shows that changing the turns number in this manner results in minor changes of the coupling factor, while the coupling capacitance stays essentially unchanged. Additionally, the copper area of the windings is made equal or even larger, which reduces losses. For high turns numbers, the self-resonance frequency of the coil should be investigated to make sure that the coil can operate at the target operating frequency of the power converter.

TABLE VI. RESULTING CHANGE IN TRANSFORMER PARAMETERS WHEN CHANGING THE TURNS NUMBER OF THE SECONDARY SIDE FOR THE L2T3 DESIGN.

$Layer_{sec}$	N_{sec}	w_{cu}	L_{self}	k	$C_{coupling}$	R_{ESR}
		mm	μH	-	pF	m
2	3	3	0.995	0.572	7.73	461
2	4	2.125	1.814	0.574	7.73	825
2	5	1.6	2.887	0.576	7.72	1309
4	3	3	3.995	0.573	7.74	1478
4	2	4.75	1.699	0.569	7.75	596

- Power capability

The power capability of a transformer is given by the thermal limitation, i.e. a maximum given temperature rise. Since there is no magnetic material, the only loss contribution is caused in the windings. Although not demonstrated in this paper, the 2D model is suitable for investigating the power limits of the design by combining circuit and thermal simulations. The thermal conductivity of the insulation materials are normally poor while copper is a good thermal conductor. Hence, the thermal sink is likely to be the external connections to the transformer. As discussed above, the choice of interface material between the copper and the solid insulator can affect the thermal performance.

- High efficiency

As shown in the paper, high coupling factor and low track resistance leads to higher transformer efficiency for a given inductance. If the coupling capacitance is below the upper limit, the coupling factor can be increased by increasing the coil area by changing the inner radius and the turns number. Decreasing the track resistance is achieved by widening the copper track or reducing the number of winding layers. However, increasing the copper height to reduce losses is a costly alternative and should be evaluated according to the skin depth that corresponds to the operating frequency of the converter. Hollowness of the winding [10] has been shown to affect coil losses. Additionally, the PCB stack-up can slightly alter the losses from skin effects. Exploring these design spaces is feasible by using optimisation algorithms and 2D FEA simulations [21].

- Low coupling capacitance

In order to achieve a design with low coupling capacitance, the straightforward way is to minimise the coil area and the distance between them. However, these actions tend to counter the transformer efficiency. To minimise the coil area, the number of turn-layers should be increased, while minimising the inner radius and the number of turns. Alternatively, the secondary coil are can be made smaller than the primary coil [19]. However, as discussed in Section V-A, this leads to an increased peak electric field on the secondary side winding and lower coupling factor.

Moreover, an insulation material with low dielectric constant, e.g. PFTE, should be used. The low dielectric constant of air is used as the argument of using it as the insulation medium [15]. In addition, the separation distance between primary and secondary side becomes large due to the low dielectric strength of air. Consequentially, the coupling capacitance becomes low; however the compactness of the transformer is lost.

VI. CONCLUSION

This paper has presented a design methodology for coreless printed planar transformers operating at multi-megahertz frequencies and with an isolation voltage in the medium-voltage range. The electrical and dielectric performance of the designed transformers has been validated by both simulations and experiments. For the investigation, the transformer design space is set as 1 μH self-inductance with a coupling capacitance of 10 pF. To summarise, low coupling capacitance can be obtained for several combinations of PCB layers and turns with approximately equal transformer efficiency. The highest figure-of-merits of 92 or 94 are obtained with 2-layer 2-turn or 4-layer 1-turn winding designs. For similar values of figure-of-merit, the resulting isolation voltage is different due to different thickness of the insulation material. Based on the experimental validation, the mean breakdown voltages were found to be 37, 48, and 73 kV for PTFE thicknesses of 1, 3 and 6 mm, respectively. Despite having different breakdown voltages, the transformers' similar FOM indicates that the converter efficiency should be similar. Even though the coupling factor is lower for higher PTFE thicknesses, the winding ESR is lower which allows for power transfer with the same or similar efficiency. Moreover, the 2D model of the transformer is shown to be sufficiently accurate while having a short calculation time. As a result, the designer can practically map a large design space.

For the dielectric design, the sharp edges of the PCB's copper tracks were found to amplify the electric field around the copper edge and, consequently, limit the isolation voltage of the transformer. Several methods for field shaping of planar PCB transformers have been presented and analysed. The most promising method is changing the solder mask epoxy for an epoxy with a higher relative permittivity (permittivity field-shaping). In contrast, the classical field-shaping approach of adding a guard ring only marginally increases the breakdown voltage while lowering the transformer efficiency and increases the coupling capacitance between the primary and the secondary side.

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Ole Christian Spro was born in Høvik, Norway in 1986. He received his M.Sc. and PhD degree in electrical power engineering from the Norwegian University of Science and Technology, Trondheim, Norway, in 2013 and 2020, respectively. Curretly, as well as in the period 2013-2016, he works at SINTEF Energy Research, Trondheim, as a researcher. His research interests include design of high frequency power converters, modelling and use of wide bandgap semiconductor devices, and reliability of power semiconductor devices.

Frank Mauseth received his M.Sc. degree in Electrical Engineering from Delft University of Technology, The Netherlands, in 2001. Since then he has been with the Norwegian University of Science and Technology (NTNU) in Trondheim, Norway, where he received his Ph.D. degree in 2007 and is now an Associate Professor. His main fields of interest are high voltage insulation materials and systems, measurement methods and testing. He is also active in the IEEE DEIS TC "HVDC Cable Systems".

Dimosthenis Peftitsis (Senior Member, IEEE) is Associate Professor of Power Electronics in the Department of Electrical Power Engineering at the Norwegian University of Science and Technology (NTNU) in Trondheim, Norway where he has been a faculty member since May 2016. Born in Kavala, Greece, he received his Diploma degree (Hons.) in electrical and computer engineering from Democritus University of Thrace (Xanthi, Greece) in 2008. In his final year of studies, he spent six months in ABB Corporate Research, Västerås, Sweden, writing his thesis. He completed his Ph.D. degree at the KTH Royal Institute of Technology (Stockholm, Sweden) in 2013. Dimosthenis was a Postdoctoral Researcher involved in the research on SiC converters at the Department of Electrical Energy Conversion, KTH Royal Institute of Technology (2013/14). He also worked as a Postdoctoral Fellow at the Lab for High Power Electronics Systems, ETH Zurich, where he was involved in dc-breakers for multiterminal HVDC systems (2014 to 2016). His research interests lie in the area of power converters design using WBG devices (e.g. SiC, GaN) including adaptive drive circuits, dc-breaker design for MV and HVDC systems, as well as reliability assessment and lifetime modelling of high-power semiconductor devices, including reliability of SiC power switches. He has published more than 60 journal and conference papers; he is the co-author of one book chapter and the presenter of 5 conference tutorials. Dimosthenis is a member of the Outstanding Academic Fellows Programme at NTNU, a member of the EPE International Scientific Committee and currently serves as the Chairman on the Norway IEEE joint Power Electronics Society/Industry Applications Society/Industrial Electronics Society Chapter.