High Input Impedance Capacitively-coupled Neural Amplifier and Its Boosting Principle

Erwin H. T. Shad[1], Kebria Naderi[2], Marta Molinas[1]

***Abstract*—This article proposes a technique for increasing the input impedance of conventional capacitively-coupled neural amplifiers based on careful examination of its analytical model. Following the precise derivation of the input impedance model, the effect of a negative capacitor is exploited as boosting principle to the input impedance of capacitively-coupled neural amplifiers. In order to implement this negative capacitor, some modifications were made to the conventional structure to make them suitable for capacitively-coupled neural amplifiers. The boosting factor which is calculated after these modifications exhibits frequency dependant parameters which offers further flexibility in the design and tuning. The proposed method to improve the input impedance is tested through simulation in a commercially available 0.18 µm CMOS technology. The robustness of the proposed structure is tested through Monte Carlo simulation in the presence of mismatch and process variation. Although the input impedance dropped with a factor of 2 during Monte Carlo simulations, the proposed method can still boost the input impedance by a factor of 100 at 100 Hz. While the proposed method might increase the area consumption, it maintains power efficiency property. When the proposed neural amplifier is compared to the state-of-the-art in terms of noise, power and input impedance, it shows relatively higher input impedance with negligible effect on input referred noise and power consumption which makes this structure suitable for low-power applications.**

***Index Terms*—High input impedance, input impedance analysis, neural amplifier, low power, low noise**

I. Introduction

Neural signals have widely been used in order to diagnose diseases or disorders besides treatment, entertainment, BCI (brain to computer interfaces) and many other applications. In the first stage, they should be captured by a wet or dry electrode, then it should be amplified with an amplifier.

Based on the type of electrode, the minimum acceptable input impedance of the amplifiers is different. In order to minimize the attenuation and make the amplifier compatible with all types of electrodes, the amplifier should have very high input impedance. The electrode impedance can be up to 1 MΩ for dry-contact and non-contact electrodes are 1 GΩ at 1 Hz, respectively [1]. Dry electrodes is the term that is used for electrodes that can be used without conventional preparation such as gel or saline environment.

Chopping techniques is one of the most conventional techniques used to minimize the flicker noise for biomedical applications. Limited input impedance is the main problem in amplifying biomedical signals. In [2], a technique is proposed to boost the input impedance for chopper amplifiers. But it still suffers from limited input impedance and lack of detailed analysis about input impedance calculation and boosting factor. In addition positive feedback [3] and auxiliary path way [4] to boost the impedance of chopper amplifier was proposed. The initial value of the impedances are relatively low in chopping technique. Therefore, even after boosting, they are not suitable for high impedance electrodes.

In this article, conventional structures to amplify neural signals which have much higher input impedance than chopping techniques, is surveyed. After that, a detailed analysis on input impedance of conventional structure is carried out. In addition, a method to boost the input impedance of the amplifier is proposed. Furthermore, it's proven by equations and tested through simulations. Finally, the proposed amplifier is compared with the state-of-the-art in term of noise, power, area and input impedance.

II. Capacitively-coupled neural amplifier properties

Capacitively-coupled neural amplifier (CCNA) was proposed first in [5]. A fully differential structure based on conventional CCNA is shown Fig. 1. In this figure, C_p is the parasitic capacitance of the input transistors. This structure is chosen because of its lower systematic offset and higher dynamic range. CCNA has been widely used to amplify biomedical signals because of their nice properties such as tunability of lower cut off frequency, blocking DC offset and good NEF (noise efficiency factor), but its input impedance is limited [5], [6].

The total input-referred noise of the neural CCNA can be calculated by Eq. 1 where v_{ni} is the input-referred noise of the amplifier. In order to minimize the coefficient factor behind the v_{ni}, C_{in} should be much bigger than C_f and C_p. Besides, in order to minimize the flicker noise of the amplifier, the W and L of the input transistors should be relatively large. Furthermore, the mid-band gain of this structure will be defined by the value of C_{in}/C_f. Therefore, the value of C_{in} should be high enough to meet the requirement.

$$v_{ni,amp}^2 = (\frac{C_{in} + C_f + C_p}{C_{in}})^2 v_{ni}^2 \tag{1}$$

In order to calculate the input capacitance of the CCNA, a voltage source is put in one of the input nodes as it's shown in 2. In this shape, the input impedance before boosting is shown with Z_{in} and the boosted input impedance is shown by $Z_{in,B}$.

[1]Erwin Shad and Marta Molinas are with the Faculty of Information Technology and Electrical Engineering, Engineering Cybernetics, Norwegian University of Science and Technology (NTNU), Trondheim, Norway. Erwin.shad@ntnu.no

[2]Kebria Naderi is with the Faculty of Engineering, Electrical Engineering, Gauilan University, Rasht, Iran. Kebria.Naderi@gmail.com

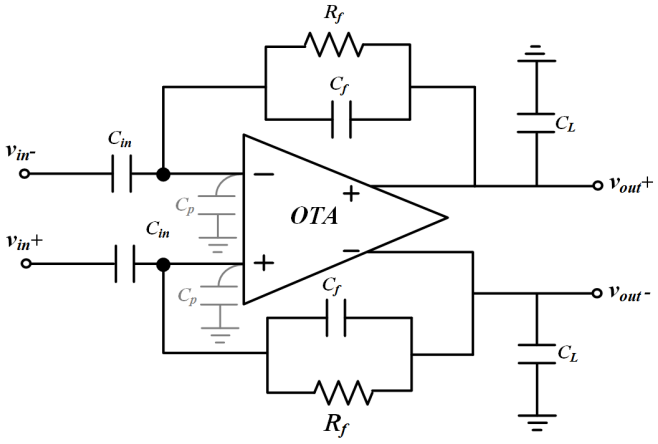

Fig. 1. A fully differential capacitively-coupled neural amplifier structure

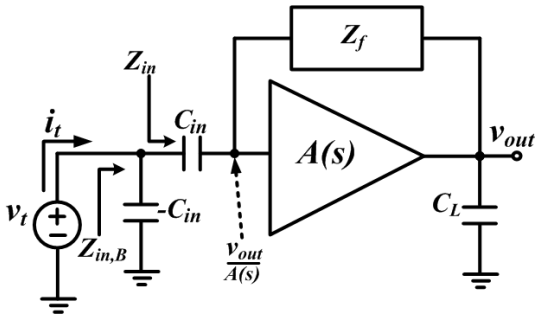

Fig. 2. Input impedance analysis

In order to simplify the model, it's assumed that the amplifier has one pole and the pole is in the output node. The open-loop transfer function can be calculated as Eq. 2 where ω_L is the higher cut-off frequency of the open-loop amplifier, R_L is the output resistance and A_0 is the DC gain of the open-loop amplifier.

$$A(s) = \frac{-A_0}{1 + \frac{s}{\omega_L}} \quad \text{and} \quad \omega_L = \frac{1}{R_L C_L} \tag{2}$$

By two KCLs, the input impedance will be calculated as Eq. 4 where Z_f is equal to Eq. 3. In order to calculate the input impedance of CCNA before boosting, $-C_{in}$ is eliminated from Fig. 2. In order to calculate accurately, the input node of the amplifier is not considered as a virtual ground. The reason behind this will be elaborated in this section.

$$Z_f = R_f \parallel \frac{1}{sC_f} = \frac{R_f}{1 + sC_f R_f} \tag{3}$$

$$Z_{in} = \frac{v_t}{i_t} = \frac{1}{sC_{in}} + \frac{Z_f}{1 - A(s)} \tag{4}$$

Because of the values of input capacitor and high open-loop gain and the value of Z_f, input capacitors is mostly dominant In the Eq. 4. Therefore, the input capacitor can be approximated to 5.

$$Z_{in} \approx \frac{1}{sC_{in}} \tag{5}$$

By adding the negative capacitor with the same value of input capacitor in parallel to the input impedance as it's shown Fig. 2, the boosted input impedance would be infinite with approximate input impedance value. Therefore, we need to go back to more accurate input impedance equation which was calculated in Eq. 4. The boosted input impedance will be according to:

$$Z_{in,B} = Z_{in} \parallel \frac{-1}{sC_{in}} \tag{6}$$

$$Z_{in,B} = \frac{\frac{1}{sC_{in}} + \frac{Z_f}{1-A(s)}\frac{-1}{sC_{in}}}{\frac{1}{sC_{in}} + \frac{Z_f}{1-A(s)} + \frac{-1}{sC_{in}}} \tag{7}$$

$$Z_{in,B} = -[1 + \frac{(1 - A(s))}{sC_{in}Z_f}]\frac{1}{sC_{in}} \tag{8}$$

In the bandwidth of capacitively-coupled neural amplifier, the open-loop gain is much larger than 1. Therefore, the Eq. 8 can be simplified to Eq. 9 and finally the boosting factor is according to Eq. 10.

$$Z_{in,B} \approx -\left[1 + \frac{A_0(1 + sC_f R_f)}{sC_{in}R_f(1 + sR_L C_L)}\right]\frac{1}{sC_{in}} \tag{9}$$

$$BF \approx 1 + \frac{A_0(1 + sC_f R_f)}{sC_{in}R_f(1 + sR_L C_L)} \tag{10}$$

The input impedance boosting factor shows that the impedance at very low frequency will be boosted by a higher factor and it reduces by increment in frequency. The value of input capacitor not only defines the input impedance before boosting, but also it affects the boosting factor itself. Noteworthy, at very high frequencies the proposed method will have the same impedance in comparison with input impedance before boosting since the boosting factor will reach to 1.

The Eq. 8 shows that the input impedance can be increased by increasing C_f which also defines lower cut-off frequency with R_f. Besides, it has an inverse relation to R_L an C_L of the open-loop amplifier which not only defines the higher cut-off frequency of the amplifier, but also it controls the closed-loop higher cut-off frequency.

III. Implementation of High Input Impedance Capacitively-Coupled Amplifier

In order to achieve low input-referred noise and high open-loop gain, a similar structure which was proposed in [7] is chosen. Since a single ended structure has an inherent systematical offset and limited output swing, it is modified to a fully differential structure as it's shown in Fig. 3. Besides, a common-mode feedback was implemented to set the output DC voltage.

The negative capacitor is implemented based on the cross-coupled structure as it is shown in Fig. 4. The total input impedance at the input nodes of cross-coupled structure can

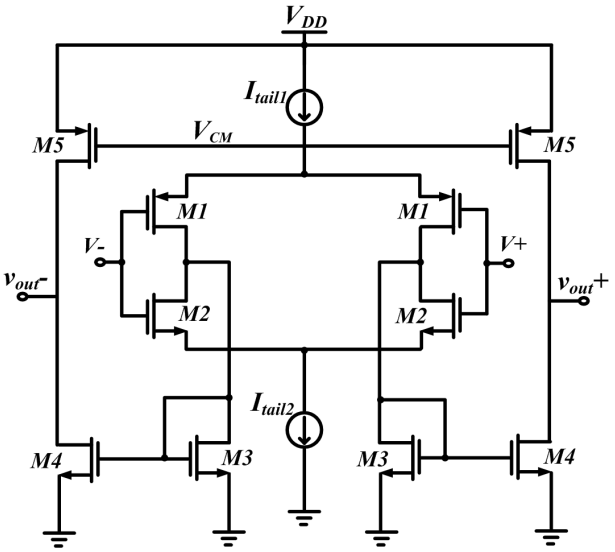

Fig. 3. The fully differential structure used as the amplifier

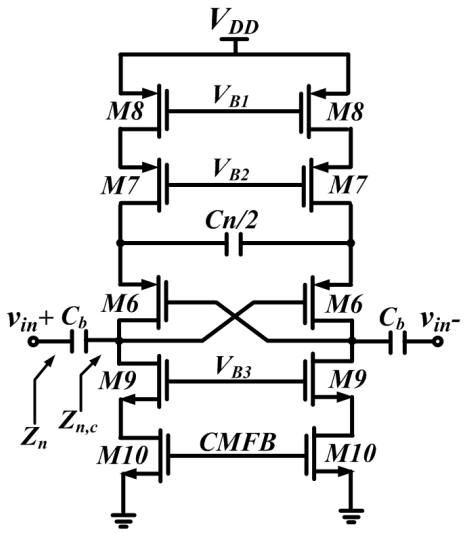

Fig. 4. Implementation of negative capacitor

be calculated as Eq. 11. The cascode structure is designed in order to make the C_n dominant at much lower frequency. Besides the lower bias current helps to increase the parallel resistor to capacitor which helps to make the capacitor dominant. Therefore, the proposed structure doesn't consume much power. In this design, the current in each branch is 40 nA. In the simulation, the $C_n/2$ is 3 pF to make it dominant in very low frequencies. By these considerations, the input impedance of the cross-coupled structure can be approximate to the Eq. 12.

$$Z_{n,c} = -\left(\frac{1}{g_{m6}} + \left(\frac{1}{sC_n} \parallel r_{o8} g_{m7} r_{o7}\right)\right) \parallel r_{o10} g_{m9} r_{o9} \quad (11)$$

$$Z_{n,c} \approx -\left(\frac{1}{g_{m6}} + \frac{1}{sC_n}\right) \quad (12)$$

It should be noted that C_b is mainly used to separate the DC bias of input nodes from the proposed negative capacitor. Besides, it helps to generate much larger negative capacitor. The total Z_{neg} and equivalent C_{neg} can be calculated as Eq. 14 and 15, respectively. Although the Z_{neg} has also a resistive part, it will not affect the input impedance boosting factor so much in comparision with ideal negative capacitor as it will be depicted in the simulation results section.

$$Z_{neg} = Z_b + Z_{n,c} \quad \text{and} \quad Z_b = \frac{1}{sC_b} \quad (13)$$

$$Z_{neg} \approx -\frac{1}{g_{m6}} + \frac{1}{s}\left(\frac{C_n - C_b}{C_b C_n}\right) \quad (14)$$

$$C_{neg} \approx \frac{C_n C_b}{C_n - C_b} \quad (15)$$

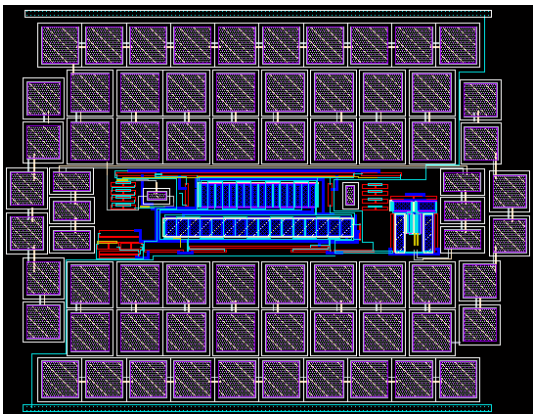

Fig. 5. The Layout of the high input impedance CCNA (226 µm x 296u µm)

IV. Simulation Results

The proposed amplifier is designed and simulated in a commercially available 0.18 µm CMOS technology. The layout of the circuit is depicted in Fig. 5. As it's shown, most of the area is occupied by capacitors. A 10 pF capacitor is used as the input capacitor. In order to generate a -10 pF capacitor at input nodes, C_b and $C_n/2$ are chosen 15 pF and 3 pF, respectively. By adding the boosting impedance circuit, the area consumption increased by a factor of 1.5.

Input impedance value versus frequency before and after boosting, with ideal negative capacitor and the implemented negative capacitor is shown in Fig. 6. It is shown in decibel in order to make it easier to see the boosting factor. The real part in Z_{neg}, which is the effect of $1/g_{m6}$, even helped to improve the boosting factor in our simulation. In this simulation, the input impedance boosted by a factor of 200 at 100 Hz and the input impedance itself is 68 GΩ at 100 Hz which is much higher than wet and dry electrode impedances.

In order to see the performance of this technique with respect to the existence of process variations and mismatch of

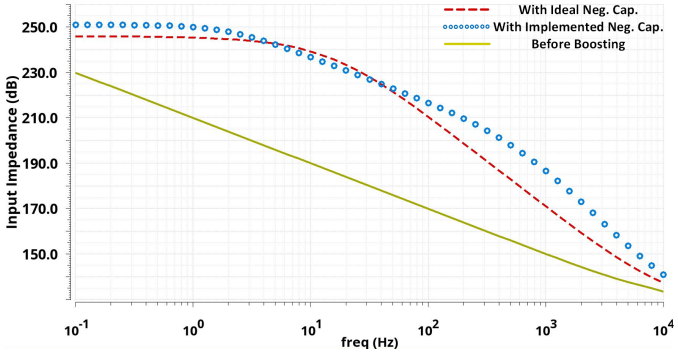

Fig. 6. The Input impedances of the CCNA before and after boosting

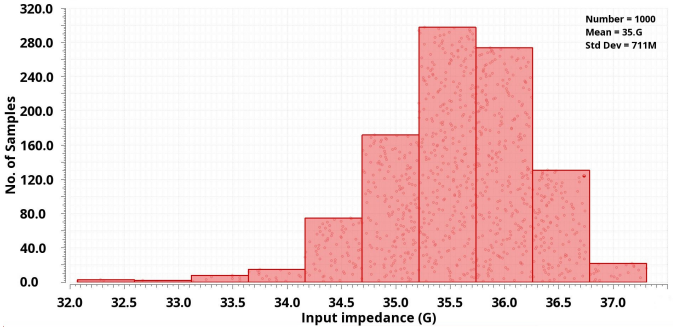

Fig. 7. The boosted Input impedance values of the CCNA for 1000 runs

the CCNA, 1000 runs for Monte Carlo simulation is carried out and the input impedance values at 100 Hz are depicted in Fig. 7. Although the mean-value of input impedance dropped by a factor of two, it is still 100 times higher than the impedance of amplifier before boosting. Even 35 GΩ input impedance of amplifier proves recording neural signals with negligible attenuation.

In order to compare this work with the state-of-the-art, NEF ($NEF = V_{ni,rms}\sqrt{\frac{2I_{tot}}{\pi U_T 4kTBW}}$) and power efficiency factor ($PEF = NEF^2.V_{DD}$) are chosen besides other parameters. As it's shown in the table I, the proposed structure has a very high input impedance. The impedances are reported at 100 Hz. In [8], they utilize buffer at the input nodes to increase the input impedance. This technique was at the cost of loosing NEF and PEF. In order to hold the noise level lower than a specific amount, their buffer should consume a high amount of power which leads to higher NEF and PEF. In [2], although they exploit the same technique, but it was used with chopping technique. Therefore, input impedance before boosting was much lower in the first place. Therefore, even after boosting, the input impedance is not comparable.

In this work, By cascoding transistors, the negative capacitors are used with conventional CCNA. In addition, its PEF is better due to utilization of power efficient amplifier and the nice properties of input impedance boosting technique. The effect of the proposed technique on power and noise are negligible. Therefore, this technique is suitable for low-power and low-noise structures.

TABLE I
COMPARISON THE PROPOSED HIGH INPUT IMPEDANCE AMPLIFIER WITH THE STATE-OF-THE-ART CAPACITIVELY-COUPLED NEURAL AMPLIFIERS

Specs	[8]	[4]	[3]	[2]	This Work
Technology (nm)	180	40	180	65	180
Supply Voltage (V)	1	1.2	1.8	1.2	1.2
Power (μW)	5.5	2.8	19.8	30	1.6
Gain (dB)	40-7	25.7	100	40	40
Bandwidth (Hz)	0.6-1k	1-5k	0.5-100	0.7-450	0.5-10 k
IR Noise (μV_{rms})	2.4	7.1	0.8	-	3.95
NEF	7	6.1	12.3	-	1.79
PEF	49	44.6	272	-	3.85
Input Impedance GΩ @ 100 Hz	6	1	0.05	0.3	35
Boosting Technique	Buffer	Aux-path	Positive feedback	Negative Cap.	Negative Cap.
Area (mm^2)	-	0.069	6.5	-	0.067
Sim./Meas.	Sim.	Meas.	Meas.	Sim.	Post Layout Sim.

V. CONCLUSION

In this article, a method to improve the input impedance of CCNAs is proposed. This method is proven by careful examination of the analytical model of the input impedance and subsequent simulation in a commercially available 0.18 μm CMOS technology. The input impedance boosting factor is defined by the insertion of a negative capacitor. It exhibits dependency on frequency in addition to being related to other parameters such as lower and higher cut-off frequency, open-loop gain and even input capacitor itself. Due to this flexibility, it will offer the designer more freedom to optimize the boosting factor. Finally, the proposed method is implemented and simulation results have shown a boosting factor of 100 at 100 Hz and even higher for lower frequency. The proposed structure achieved very low NEF, low PEF and very high input impedance, due to exploiting power and noise efficient amplifier and the input impedance boosting method.

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