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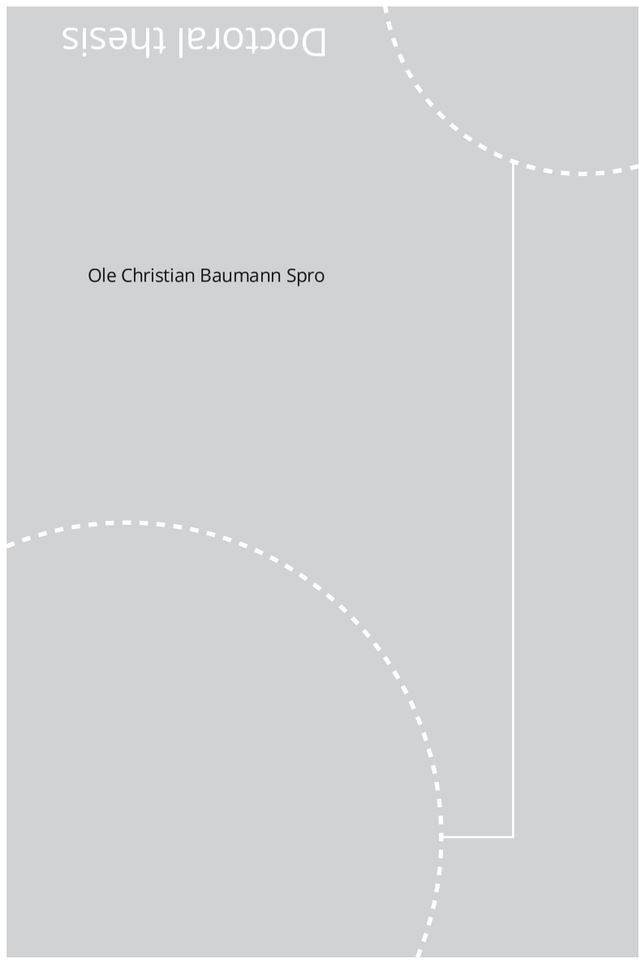
Ole Christian Baumann Spro

Design and optimisation of an auxiliary power supply with medium-voltage isolation using GaN HEMTs



ISBN 978-82-326-5046-0 (printed ver.)
ISBN 978-82-326-5047-7 (electronic ver.)
ISSN 1503-8181

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Thesis for the Degree of Philosophiae Doctor

Trondheim, November 2020

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Printed by NTNU Grafisk senter

Abstract

This PhD thesis shows that compact and efficient converter systems can be obtained by leveraging the inherent characteristics of GaN HEMT devices. In the targeted application of an auxiliary power supply with medium-voltage isolation, the design, optimisation and experimental validation of the auxiliary power supply demonstrate that the high frequency characteristics of GaN HEMTs allow for high-efficiency even at multi-megahertz frequencies. The high operating frequency enables the use of coreless planar transformers with solid insulation that is sandwiched with PCB windings, where the insulation thickness is significantly increased while upholding the converter efficiency compared to the literature. Additionally, the design methodology of the transformer is modified to include the coupling capacitance of the transformer. This capacitance constitutes a high-frequency noise path and must be minimised in order to avoid affecting the operation of the main converter.

In this PhD work, an auxiliary power supply is designed based on a resonant topology operating at 6.78 MHz. The design methodology results in a compact rectifier with inherent output voltage regulation. Simulation-based design methodologies for both the converter topology and the isolation transformer are presented, followed by experimental validation. For the converter, the optimisation process uses a genetic algorithm. Designs are evaluated through 2D finite element analysis and SPICE simulations. Four prototypes were made from the identified Pareto front. These prototypes were able to transfer from 11 to 16 W with a measured peak efficiency of 81% and the output voltage regulation is experimentally validated. However, there is a discrepancy in simulated and measured inverter losses despite the effort to model the additional loss factors of GaN HEMTs, namely dynamic on-state resistance and C_{oss}-losses. Thus, these losses represent a hindrance for improving the efficiency of converters operating at high frequency. Consequently, virtual prototyping, which is more time- and material-efficient than design by prototyping, also becomes more challenging.

Finally, the thesis presents a design methodology for a compact, printed, high-frequency isolation transformer with medium-voltage isolation that can be used in the previously presented resonant converter. The methodology takes the coupling capacitance of the transformer into account. Additionally, possible field-grading methods are investigated with permittivity field-grading showing the most promise for the application. Experimental breakdown tests are performed according to IEC standards. Using printed windings allows for producing windings with higher accuracy and higher precision. Characterisation of the transformers shows low variation in transformer parameters from the simulated values.

Acknowledgements

Looking back, I strongly believe that the support of our families builds the inner strength that we carry with us and can draw upon when needed. Their smiling eyes of love and expressions of how proud they are of our efforts stay with us for a lifetime.

My thoughts go, in particular, to my father, who passed away one early morning in August 2018 and thus did not get the chance to see me defend my PhD. Although unconsciously, my heritage weighed strongly on the path I have taken. Being the son of an engineer that graduated from NTH, Trondheim results in the likelihood that I would be one too. Not because he would try to influence my choice, but because of how he shared his own history and interests with my brother and me. The only exception was his ultimatum to both of us that we should go to high school and obtain our *examen artium* because "our heads were too good to go to waste". I guess he wasn't wrong.

If he was here for the occasion, he would also have gotten the chance to meet some of the people who helped me along the way and made this path possible. The availability and informal tone of professor Dimosthenis 'Dimos' Peftitsis made him a great support in many times. His technical interest and friendly nature has led us to have countless discussions, both technical and social, in the office as often as elsewhere. Also, I thank professors Ole-Morten Midtgård and Tore Undeland for believing in my capabilities and selecting me for this position. They have supported my initiatives and, at times, accepted my stubbornness. Moreover, the technical staff at the department have been most helpful through all of my experiments.

As my exchange experience, I got to spend three highly memorable months at G2Elab in Grenoble, France with professor Pierre Lefranc and his group. In contrast to the stereotypical view of researchers, Pierre looks more like a rock star, driving a motorcycle in his leather jacket to the office. But his dedication, attention to detail and presence in the moment make him an excellent collaboration partner and researcher. This stay marked a turn in my research and, consequentially, will likely follow the rest of my career. Additionally, the French *apero* is a great tool for improving work relations and quality of life in general.

During any PhD period, there are surely both good times and frustrating times. For the latter, missing results, short deadlines and experimental setups blowing up two weeks before the paper deadline were part of mine. For those frustrating times, it is crucial to be surrounded by people one can discuss with and vent to. Just remember to also share the good times with these same people. At times serving as unofficial supervisor and personal mentor, Gilbert Bergna-Diaz has been a great

support during the PhD years. Other colleagues at SINTEF Energy Research, particularly Giuseppe Guidi and Andrzej Holdyk, have also been a great support in both good and frustrating times. Also, what is any workplace without office mates ... and coffee breaks? I had the pleasure of sharing time with many, but above all, Subhadra Tiwari, Andreas Giannakis and Santiago Sanchez made it into a friendly and witty atmosphere.

And to Marième who supported me through all periods of this journey, with her love, her listening, and her constructive input. Also, taking more than her share on the home front, taking care of both me and Samuel. Samuel may not have put in any effort to accelerate my work, but I would not be without him. He adds a completely new dimension to life. His wonder, joy and curiosity about the world are traits to be desired by researchers. I will, to the extent of my capabilities, support and encourage him to observe and explore, while letting him form his own path... to engineering.

List of Abbreviations

2DEG	2-dimensional electron gas
CCM	Continuous-current mode
CMCD	Current-mode class D (inverter)
EMI	Electromagnetic interference
ESR	Equivalent series resistance
FEA	Finite element analysis
FFT	Fast Fourier transform
FHA	Fundamental harmonic approximation
FOM	Figure of merit
HEMT	High electron mobility transistor
IEC	International Electrotechnical Commission
ISM	Industrial, scientific, and medical (radio bands)
LVMOSFET	Low-voltage MOSFET
MOSFET	Metal oxide semiconductor field effect transistor
PCB	Printed circuit board
PFC	Power factor correction
PTFE	Polytetraflouorethylene – also known as Teflon^{TM}
SJ FET	Super-junction field effect transistor
WPT	Wireless power transfer
ZCS	Zero-current switching
ZDC	Zero-voltage-derivative switching
ZVS	Zero-voltage switching

Contents

Chapter 1

Introduction

1.1 Background

Based on the growing knowledge of the planet's biosphere and climate change, decarbonisation of the economy has become one of the major goals of global politics in the last few decades. This is achieved through the use of renewable energy sources, increased energy efficiency, and electrification of large societal sectors, e.g. transport and industry. Thre electrification and digitalisation of society is not possible without the use of power electronic converters. Moreover, the use of converters enables high-efficiency energy conversion, ensures grid stability, and controls power flow between sources and loads. High efficiency is achieved through the use of power electronic converters to optimise the operation point and switching loads on and off only when they are needed. Among the numerous technologies needed for this shift in society, medium-voltage grids, both DC and hybrid AC-DC grids, are considered to be an enabling technology for efficiency improvement in distribution grids, charging infrastructure, and industrial applications, as well as accelerating the integration of renewable energy sources and energy storage systems [1, 2, 3, 4, 6, 8, 9, 10, 12]. The most vital grid components in such grids are the power electronic converters.

Up until recently, state-of-the-art silicon-based converters have been the only alternative. However, Si devices have reached the theoretical limit of the material. Hence, to further increase efficiency and power density, new materials and device structures have to be explored. In this context, the manufacturers have been introducing new power semiconductor devices based on wide-bandgap materials, namely SiC and GaN. These materials exhibit characteristics that allow for improved performance compared to the Si counterparts, i.e. lower losses for the

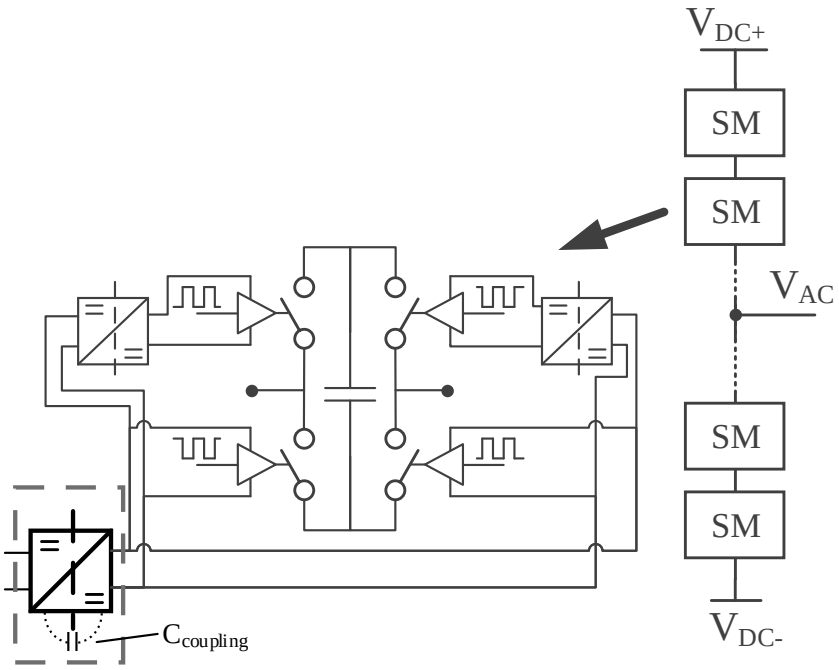

Figure 1.1: Phase.leg of a modular multilevel converter where a sub-module is fed by an auxiliary power supply connected to an external power source.

same rated voltage and current capability, improved performance at higher operating temperatures and higher power density due to the potential for increased switching frequency, albeit at a higher unit cost for the time being. In the last decade, GaN devices have shown increasing maturity and thus have been increasing their market share, going from around $8 million in 2017 to an estimated well above $50 million in 2020 [11]. The current device development indicates that SiC devices are targeting higher voltage and power levels while GaN devices cover lower voltage ranges, with an overlapping area at around 600 V [5, 11]. However, in terms of frequency, the roles are interchanged and GaN performs better at high frequencies. Current application areas for GaN devices are point-of-load converters, and power supplies for lidar and telecom, with expected near-future expansion to electric transport and wireless charging [11].

Modular multilevel converters (MMC) or series-connected switches in 2- or 3-level converters are feasible topologies for medium-voltage converters. Regardless of the topology, these converters need auxiliary converters to supply gate drivers, sensors and control circuitry for individual power electronic switches or for whole converter modules [7]. Figure 1.1 shows the phase-leg of an MMC where one sub-

module is energised by an auxiliary power supply. The coupling capacitance over the isolation barrier is a possible source for electromagnetic interference (EMI) issues for the medium-voltage converter. High operating frequency could benefit the transformer design of the auxiliary power supply by decreasing the coupling capacitance. From the voltage, power, and frequency levels, GaN components rise as suitable candidates for this application.

1.2 Research questions

This work is part of the research project HiPPE[1] that was funded by the Norwegian Research Council. The objective of this research project was to advance the field of power electronics using wide-bandgap devices. For the project, the primary objective was defined as:

> *"to develop ancillary electronics and passive components needed for the efficient use of wide-bandgap devices in power electronics converters, as well as to implement prototypes of new converters based on the new devices and the ancillary systems and components developed in this project, ideally both for SiC and GaN devices."*

In 2016, when the research questions were formulated, the technology and markets of GaN devices were different compared to today. Devices were only available from a few manufacturers with much smaller market share than today, and device reliability was largely unknown. A consequence of the high unit price was that other system costs had to be reduced or the system had to offer better performance than the state-of-the-art. Based on these aspects, the following research questions were formulated:

— Which application areas would benefit by exploiting the characteristics of GaN devices, resulting in increased performance over other semiconductor technologies?

— How can GaN devices be modelled so they can be used for design and optimisation processes?

— How should the topology and the other converter components, e.g. passives, be optimised to maximise the system benefits?

[1] **Hi**gh **P**erformance **P**ower **E**lectronics with Wide Bandgap Power Semiconductors for Industrial, Marine, Renewable Energy and Smart Grid Applications

1.2.1 Scope and limitations

This thesis aims to demonstrate that compact and efficient converter systems can be obtained by leveraging the GaN-device characteristics. The content covers the design, optimisation and experimental validation of an auxiliary power supply that consists of a dc-dc converter employing GaN HEMT devices and with a high-frequency isolation transformer that is rated for medium-voltage applications. As described in the presented background, auxiliary power supplies with high isolation voltage is an application that could potentially benefit from the inherent characteristics of GaN devices.

To successfully demonstrate the suitability of GaN devices for the targeted application, several objectives had to be set:

— Investigate a simulation model that can account for the behaviour of the GaN device dynamic on-state losses.

— Identify a circuit topology that is suitable for a low-power, high-frequency auxiliary power supply.

— Optimise the power supply based on SPICE simulation, followed by experimental validation.

— Design and optimise a compact transformer with medium-voltage isolation, followed by experimental validation.

The application use case is built around standard and expected voltage and power levels. For the input, the voltage is selected to be 48 V – a common dc-bus voltage level suitable for supplying auxiliary converter systems. Furthermore, the output voltage was set in the range of 20 to 25 V, which covers the expected drive voltages of the SiC MOSFETs that are used as the main switching component in the medium-voltage converter. Finally, the operating frequency is targeted to 6.78 MHz, the first available frequency in the ISM bands[2]. In many countries, emissions in these bands are allowed, which results in reduced EMI requirements for the design of the converter.

[2]Radio bands that are intended for **i**ndustrial, **s**cientific and **m**edical (ISM) purposes

1.2.2 Outline of the thesis

Chapter 1 introduces the thesis with a macro-view background and briefly presents the scope, outline and contributions of the thesis.

Chapter 2 presents an updated status of GaN device technology including historical, technological and application-oriented aspects.

Chapter 3 analyses and justifies the choice of topology for the targeted application. The topology is a combination among several presented resonant inverter and rectifier topologies.

Chapter 4 presents the design, optimisation and experimental validation of an auxiliary power supply operating at multi-megahertz frequency.

Chapter 5 presents the design methodology for high-frequency printed planar-transformer with high isolation voltage. Additionally, the results of high-voltage experimental breakdown testing and characterisation are presented.

Chapter 6 summarises and concludes the thesis and gives suggestions and directions for future work.

1.2.3 Research contributions

The contributions from this PhD thesis work are given in the beginning of each chapter. In summary, the main contributions of this PhD are:

— Demonstration of the feasibility of using simulation-based optimisation of a resonant converter employing GaN HEMTs.

— Design and demonstration of a class E rectifier that utilises the transformer self-inductance instead of the leakage inductance or an added discrete inductor which improves the power density.

— Design and experimental validation of a compact high-frequency transformer with high isolation voltage that uses PCB windings.

The scientific findings made during this PhD work have been published in two journal articles and four conference articles. These are listed in the ‘List of Publications’ found below. In addition, five other publications, with this author either as the first or second author, were published during the PhD period. These are listed under ‘Other Publications’.

List of Publications

[P1] Ole Christian Spro, Ole-Morten Midtgård, Tore Undeland and Giuseppe Guidi. 'Development of a Full Bridge GaN HEMT Converter for Inductive Power Transfer Application'. In: *2016 IEEE 4th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*. Nov. 2016, pp. 30–34. DOI: 10.1109/WiPDA.2016.7799905.

[P2] Ole Christian Spro, Supratim Basu, Ibrahim Abuishmais, Ole-Morten Midtgård and Tore Undeland. 'Driving of a GaN Enhancement Mode HEMT Transistor with Zener Diode Protection for High Efficiency and Low EMI'. In: *2017 19th European Conference on Power Electronics and Applications (EPE'17 ECCE Europe)*. Sept. 2017, pp. 1–10. DOI: 10.23919/EPE17ECCEEurope.2017.8099200.

[P3] Ole Christian Spro, Dimosthenis Peftitsis, Ole-Morten Midtgård and Tore Undeland. 'Modelling and Quantification of Power Losses Due to Dynamic On-State Resistance of GaN E-Mode HEMT'. In: *2017 IEEE 18th Workshop on Control and Modeling for Power Electronics (COMPEL)*. July 2017, pp. 1–6. DOI: 10.1109/COMPEL.2017.8013410.

[P4] Ole Christian Spro, Dimosthenis Peftitsis and Pierre Lefranc. 'High-Voltage and High-Frequency Design of Planar Transformer with Minimum Coupling Capacitance'. In: *2019 21st European Conference on Power Electronics and Applications (EPE '19 ECCE Europe)*. Sept. 2019, pp. 1–10. DOI: 10.23919/EPE.2019.8915570.

[P5] Ole Christian Spro et al. 'Optimized Design of Multi-MHz Frequency Isolated Auxiliary Power Supply for Gate Drivers in Medium Voltage Converters'. In: *IEEE Transactions on Power Electronics* 35.9 (Sept. 2020), pp. 9496–9511. ISSN: 1941-0107. DOI: 10.1109/TPEL.2020.2972977.

[P6] Ole Christian Spro, Frank Mauseth and Dimosthenis Peftitsis. 'Design of Coreless, Planar PCB Transformers with High Isolation Voltage for Multi-MHz Power Supplies'. In: *submitted for review* ().

Other Publications

[O1] Ole Christian Spro. 'Trådløs Kraftoverføring i Fremdig Elektrisk Transport'. In: *Teknisk Møte 2017 - Det Digitale Energiskiftet*. Trondheim, Norway: SINTEF Energi AS, Apr. 2017, pp. 79–87. ISBN: 978-82-594-3772-3.

[O2] Fredrik Göthner, Ole Christian Spro, Magnar Hernes and Dimosthenis Peftitsis. 'Challenges of SiC MOSFET Power Cycling Methodology'. In: *2018 20th European Conference on Power Electronics and Applications (EPE'18 ECCE Europe)*. Sept. 2018, P.1–P.8.

[O3] Ole Christian Spro et al. 'Driver Stage Implementation with Improved Turn-on and Turn-Off Delay for Wide Band Gap Devices'. In: *2018 20th European Conference on Power Electronics and Applications (EPE'18 ECCE Europe)*. Sept. 2018, P.1–P.10.

[O4] Håvard Lefdal Hove, Ole Christian Spro, Giuseppe Guidi and Dimosthenis Peftitsis. 'Improved SiC MOSFET SPICE Model to Avoid Convergence Errors'. In: *International Conference on Silcon Carbide and Related Materials 2019 (ICSCRM'2019)*. Kyoto, Japan, Nov. 2019.

[O5] Håvard Lefdal Hove, Ole Christian Spro, Dimosthenis Peftitsis, Giuseppe Guidi and Kjell Ljøkelsøy. 'Minimization of Dead Time Effect on Bridge Converter Output Voltage Quality by Use of Advanced Gate Drivers'. In: *2019 10th International Conference on Power Electronics and ECCE Asia (ICPE 2019 - ECCE Asia)*. May 2019, pp. 883–890.

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[12] Juergen K. Steinke, Philippe Maibach, Gabriel Ortiz, Francisco Canales and Peter Steimer. 'MVDC Applications and Technology'. In: *PCIM Europe 2019; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*. May 2019, pp. 1–8.

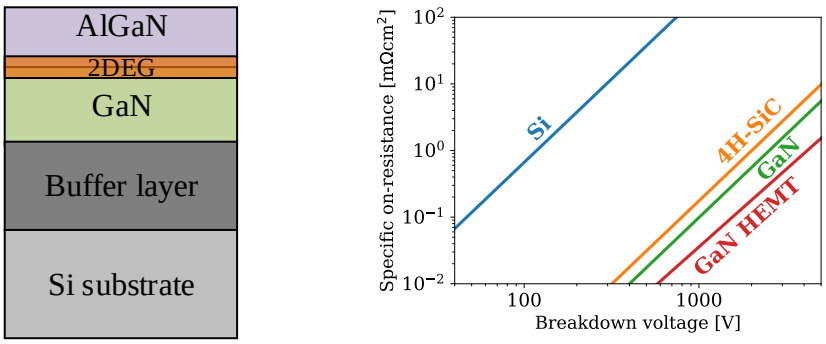
Chapter 2

Characteristics and application of GaN HEMT devices

This chapter presents the characteristics of GaN material and the GaN-based power device structure that is prominent today. An initial historical context is given to the development of the semiconductor field using GaN material. Subsequently, the characteristics of GaN power devices are detailed and compared to competing semiconductor technologies, namely SiC MOSFETs and Si super-junction (SJ) MOSFETs, in an effort to highlight the fundamental performance differences between these technologies. The final goal of the chapter is to identify relevant application areas and justify that the characteristics of the GaN power device enable crucial performance benefits, in particular for high-frequency applications.

Contributions

Contributions to the literature on the topic of this chapter have been made through publications [**P1**,**P2**,**P3**,**P5**]. In [**P1**] and [**P2**], the performance of GaN HEMTs is demonstrated in a wireless power transfer (WPT) application and a power factor correction (PFC) converter. While improvements in efficiency for the converters are shown, the system efficiency might only be marginally increased due to other dominating loss elements. Hence, the goal must be to find an application where the new GaN HEMT technology makes a large impact. In [**P5**], this is demonstrated for a high-frequency auxiliary power supply with high isolation voltage. However, as will be shown in this chapter, the GaN technology has new aspects that need to be modelled. In [**P3**], contributions were made to the discussion on measurements of one of these phenomena, namely the dynamic on-state resistance. In particular, measurement errors and SPICE modelling were discussed.



(a) (b)

Figure 2.1: a) Heteroepitaxial structure of a GaN HEMT, indicating the location of the 2DEG between the GaN and AlGaN layers (layer height is not shown to scale). b) Theoretical lower limit of specific on-resistance of vertical devices based on Si, SiC and GaN, and for the lateral GaN HEMT device.

2.1 GaN material and the HEMT device

The development of GaN for use in the semiconductor industry has primarily been driven by the desire to produce light emitting diodes (LEDs) using GaN as the main semiconductor material [9, 43]. GaN has a direct band gap that results in light emission in the near-UV spectrum. Furthermore, by making different alloys with AlN or InN, the band gap can be slightly adjusted. This has led to the development of highly efficient violet and blue LEDs. Such LEDs are in turn used for advancing more efficient technology for emitting white light, an achievement that was rewarded with the Nobel Prize in Physics in 2014 [53].

Additionally, the GaN material is suitable for making power devices in a structure known as the high electron-mobility transistor (HEMT). A HEMT does not rely on doping to obtain a highly conductive channel in the semiconductor material. Rather, a polarisation charge is established in the interface between two different material layers. Figure 2.1(a) shows the heteroepitaxial structure of a GaN HEMT made on a Si substrate [34]. In the GaN HEMT, this polarisation charge is formed between a GaN and an AlGaN layer. This interface layer of charge is referred to as a 2-dimensional electron gas (2DEG). To handle the mismatches in the material properties between Si and GaN, a buffer layer is grown on top of the substrate. Subsequently, the GaN and the AlGan layers are grown to establish the 2DEG. Finally, a transistor is made by adding a gate structure across this layer that can neutralise the polarisation charge in such a way that the device can be turned on and off. A consequence of this structure type is that it is only fabricated as a lateral

device. Vertical structures are preferred for power devices due to better current distribution and improved use of the chip area [6, 27, 1]. However, this could limit the voltage rating of such devices due to cost and fabrication yield. Several vertical GaN device structures are currently being explored: current-aperture vertical electron transistor (CAVET), trench MOSFET and vertical fin power FET [59]. The latter has shown promising performance [56, 59]. Nevertheless, most of the vertical device structures have to be grown on high-quality GaN substrates which are currently expensive and too small for large-scale power device fabrication [27]. Some researchers are circumventing this limitation by fabricating vertical GaN structures on Si substrates in an effort to cut component cost [27].

Reports in the literature in the late 1990s and in the 2000s indicate that a method for producing GaN devices on Si wafers was successfully implemented, which was the foundation for modern GaN-based power electronics [1, 22, 34]. Si wafers are significantly cheaper than wafers based on GaN, SiC or sapphire, and the available wafer size is much larger. Furthermore, existing fabrication infrastructure for Si can be reused for producing this new device [34]. Hence, it became conceivable that costs for GaN HEMT devices could be lowered sufficiently to enter the very price-competitive power electronics market. GaN devices were first available in the RF market where the high price could be leveraged by the device performance. These devices are usually made on SiC or sapphire substrates, although GaN-on-Si was also available [34]. EPC was one of the first companies to launch a GaN HEMT device for the power electronics market in 2009 and they were closely followed by many other companies in the start of the last decade. The market size for GaN power devices is still modest in comparison to the total market for power devices. In 2017, the total GaN market was estimated to be approximately $8M [14] while the SiC market was valued at $311M [48]. Yet, both markets are small compared to the total market size of $15.4B for power devices [48]. However, finding suitable markets for the introduction of a new technology is the key to its adoption among converter designers [38]. The current adoption rate of GaN is increasing and the market is predicted to increase between 55 and 93% annually in the period 2017-2023 [14].

Furthermore, the high channel mobility means that smaller devices can be made for a similar rating, which results in a smaller device area [1]. Typically, device technologies are compared using specific on-resistance and plotted for different breakdown voltages. This results in on-state values that are independent of chip area, and, hence, the conduction losses of different technologies can easily be compared. Figure 2.1(b) shows the lower theoretical limit in on-state resistance for vertical Si, SiC, and GaN devices, and a theoretical lower limit for the GaN HEMT device [1] (although there are small variations in these limits in the literature [18]).

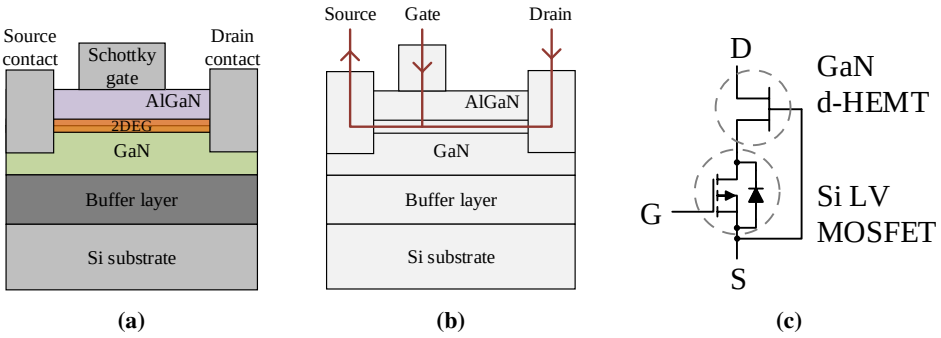


Figure 2.2: a) Semiconductor structure of the GaN HEMT with a Schottky gate contact. b) Diagram showing the current flow between the external contacts, highlighting that the device is lateral. c) Schematic diagram of GaN HEMT cascode configuration of a low-voltage Si MOSFET and a GaN d-HEMT.

This figure shows that GaN devices can achieve lower resistance than Si and SiC devices for the same rated breakdown voltage, and the GaN HEMT device can achieve even lower resistance due to its high channel mobility. However, while commercial SiC MOSFET devices are closing in on the theoretical value of specific on-resistance, modern GaN HEMT devices are further away from their theoretical potential, with very few reported GaN devices crossing the theoretical limit of 4H-SiC [6, 20, 59]. Thus, there is still considerable room for improvement for future GaN power devices.

2.1.1 Normally-on and normally-off device, and related gate structures

The GaN HEMT is inherently a normally-on, or depletion mode, device (d-HEMT) due to the formation of a 2DEG between the AlGaN and GaN layers. This entails that the device is in on-state with a zero gate-to-source voltage and requires a negative voltage to be turned off. In its simplest form, a Schottky contact can be made on top of the AlGaN layer to serve as the gate contact (shown in Fig 2.2(a)). When the device is turned on, the current flows in the device structure, as indicated in Fig. 2.2(b). As can be seen, the currents go through the 2DEG between the AlGaN and GaN layers. Notably, the currents do not go in the substrate since it is a lateral device. The 2DEG is turned off by applying a negative voltage on the gate contact relative to the source that closes the 2DEG channel under the gate contact. However, application engineers tend to avoid normally-on devices. The converter system must be designed so that it goes to a safe state in the case of a gate driver failure or a loss of power to the gate driver. This is perceived as easier when using a normally-off device despite demonstrations of driver circuits that can handle the start-up and loss-of-power conditions for normally-on switches [42].

As an example, a bridge converter using normally-on devices would short-circuit the dc-link capacitor in case of a fault, which is a highly undesirable situation. Accordingly, the GaN industry is currently focusing on manufacturing normally-off devices.

The GaN HEMT can be made normally-off by two main techniques. Either the HEMT is series-connected with a normally-off device in a cascode configuration, or a gate structure is implemented such that the device becomes an enhancement mode device (e-HEMT).

In the first technique, the d-HEMT is combined with a low-voltage MOSFET (LVMOSFET) to appear as a normally-off device (Fig. 2.2(c)). This is known as cascode configuration. The internal connection of the HEMT gate to the external source terminal leads to inherent negative driving of the GaN HEMT gate when the auxiliary MOSFET is off. When the LVMOSFET is on, the GaN HEMT sees a gate voltage close to zero or higher, and, hence, is turned on. When the LVMOSFET is off, the blocking voltage is seen as a negative gate voltage for the GaN HEMT which is then also turned off. However, the losses of the device are governed by the two devices in series. It has been shown that for high-voltage HEMTs, the added channel resistance of the LVMOSFET is relatively low, thus it becomes a feasible solution [34]. Consequentially, cascode devices are only seen commercially for devices rated for 600V. This device type has two main benefits. Firstly, the structure lowers the reverse conduction losses compared to normally-off devices. When a negative current goes through the device, the gate-source voltage of the d-HEMT equals the forward voltage drop of the LVMOSFET. This entails that the GaN HEMT sees a gate-source voltage greater than zero and is thus turned on. Secondly, existing driver circuitry and voltage levels can be used to drive the cascode device. However, the cascode device will have reverse recovery losses due to the body diode in the LVMOSFET. The LVMOSFET will also have higher gating losses than other GaN HEMT devices since the input capacitance and the driving voltage are higher. This, in turn, limits the cascode at a lower operating frequency compared to other GaN HEMT device types. Other negative aspects of cascode devices are added parasitic inductance of the on-chip bond wires connecting the series-devices [58], and reduced control of the switching speed.

The alternative technique to make the HEMT normally-off is to make an enhancement mode device (e-HEMT) [25, 46]. This entails that the semiconductor design is modified so that the charge of the 2DEG under the gate structure is depleted with zero gate-source voltage, effectively raising the threshold voltage above zero volts. To re-establish the 2DEG, a positive gate voltage must be applied that reintroduced the channel charge. In the literature, there are two main concepts that are followed.

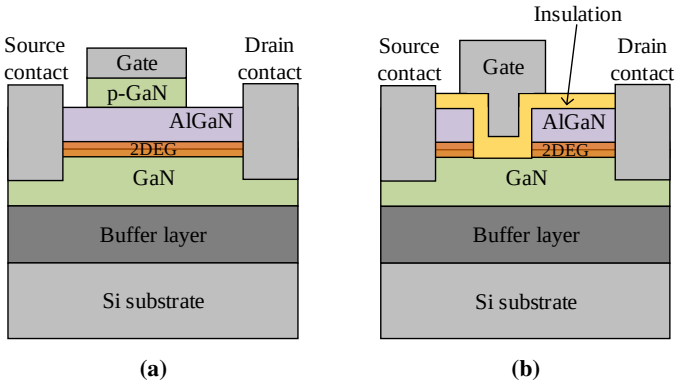


Figure 2.3: Semiconductor structure of different gate structures for normally-off GaN HEMT. a) p-GaN gate structure. b) Recess gate structure.

The first concept is p-GaN gate shown in Fig. 2.3(a) and the second is the recess gate structure shown in Fig. 2.3(b). Although there are more gate structure concepts, these are the most actively researched concepts. In addition, the p-GaN gate structure is the only structure used in commercial e-HEMT devices [46]. Furthermore, the reported specific on-resistance for e-HEMTs is lower than for d-HEMT devices [1].

In the p-GaN gate structure, a p-doped GaN layer is deposited on top of the AlGaN layer. In semiconductor terms, this leads to a shift in the valence band under the gate structure that brings the interface layer above the Fermi level. In other words, the holes of the p-GaN layer diffuse into the 2DEG and deplete the channel charge. Consequently, there is no forming of the 2DEG in that area. The lack of an insulation layer in this gate structure leads to strict gate voltage rating of these devices, usually in the range of 5 to 6 V. For higher voltage, the gate current increases drastically which can, in turn, lead to device overheating and failure.

In the recessed gate structure, the AlGaN layer is thinned sufficiently so that the valence band is above the Fermi level under the gate, and thus there is no polarisation charge and 2DEG. An undesired effect of this structure is the high gate leakage current. To counter the leakage current, an insulating layer is introduced and the gate contact is made on top of the insulating layer, making a metal-insulator-semiconductor HEMT (MISHEMT) device. In comparison with the p-GaN gate structure, the recess gate introduced several new steps in the manufacturing process and increased complexity of the design. Although the gate leakage current decreases and the voltage rating of the gate increases, the reported performance and additional reliability issues do not make this a commercially viable design to

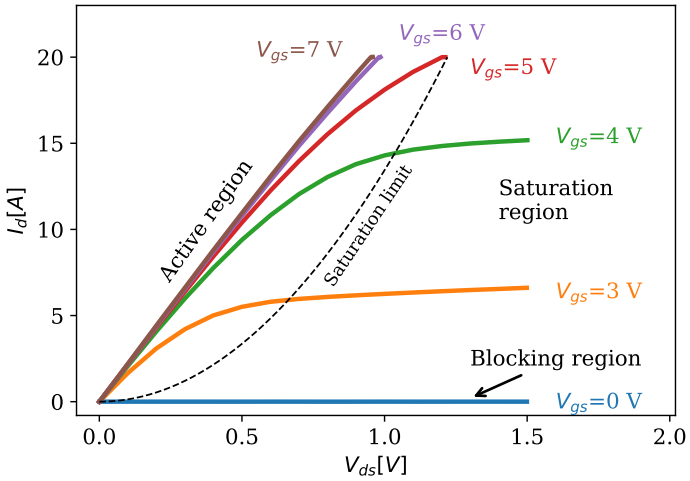


Figure 2.4: The different operating regions for forward voltages shown in a IV curve of a GaN HEMT (GS66508T).

date [46].

Despite the lack of insulated gate structures among the commercial devices, there is still a differentiation in the driving scheme between current-driven (Panasonic, Infineon) and voltage-driven (EPC, GaN Systems, etc) devices. Common for all devices is that they have low threshold voltages that result in strict requirements for the driving circuit [**P2**]. With low threshold voltage, the device becomes more prone to parasitic-turn on and more sensitive to noise. On the contrary, the gate terminal of cascode devices are connected to a low-voltage MOSFET, hence these devices have voltage-driven isolated gates with the same immunity to noise as Si devices (Transphorm). For most of the published work of the author, voltage-driven devices from GaN Systems have been used, in addition to devices from Texas Instruments with integrated drivers.

2.2 Circuit behaviour and device modelling

In this section, the static and dynamic behaviour of GaN HEMTs is presented in detail to identify the similarities and differences with other power devices. Firstly, the different conduction modes are investigated. Following this, the parasitic elements will be discussed. As will be seen, the standard small signal model of unipolar devices is suitable for modelling the circuit behaviour of GaN HEMTs. Yet, there are two supplementary loss aspects that are reported in the literature, which are not covered in conventional device modelling, namely dynamic on-state resistance and

Device	Manufacturer	Type	$V_{DS,max}$ [V]	$R_{DS,on}$ @25 °C mΩ	Relative $R_{DS,on}$ @150 °C	V_{SD} [V]
IPT60R065S7	Infineon	Si	600	100	2.35	0.82
C3M0065090J	Wolfspeed	SiC	900	65	1.38	4.8
IMZA65R072M1H	Infineon	SiC	650	72	1.31	4.0
SCTH35N65G2V-7	STM	SiC	650	55	1.31	4.5
SCT3060AL	Rohm	SiC	650	60	1.33	3.2
GS66506T	GaN Systems	GaN	650	67	2.61	3.0
IGT60R070D1	Infineon	GaN	600	55	2.18	2.2
PGA26E07BA	Panasonic	GaN	600	56	1.96	2.1
TP65H050WS	Transphorm	GaN	650	50	2.06	1.3

Table 2.1: Comparison of a selection of devices from competing technologies with similarly rated blocking voltage and nominal on-resistance. V_{SD} is given for a drain current in the range of −8 to −13 A.

output capacitor hysteresis losses. Subsequently, these loss aspects are covered in depth. As will be made clear, both of them scale with frequency and voltage, and they become prominent at high frequencies. The research trends and future outlook will also be discussed. Based on the device characteristics, the subchapter is concluded with suitable application areas where GaN HEMTs exhibit a clear advantage over other technologies.

2.2.1 Forward conduction and blocking region

The behaviour of the GaN HEMT is comparable to other unipolar devices such as n-type JFETs and MOSFETs. A voltage or a current signal is applied to the gate, which, in turn, controls the channel of the device. As shown in Fig. 2.4, the first quadrant behaviour can be divided into three regions: saturation, blocking and active. In the blocking region, the device has a small leakage current for drain-source voltages below the blocking capability of the device. In the saturation region, increasing the drain-source voltage does not lead to a substantial increase in the drain current, as expected. In the active region, approximate linear relationship between device current and voltage drop means that the device can be modelled as a resistor, R_{on}. The device on-resistance is often quoted in the datasheet for a given drain current and allows for fast comparison between devices. A selection of GaN HEMTs and competing technologies with similar on-resistance are provided in Table 2.1. A visible trend in the table data is that commercial GaN HEMTs have a high temperature coefficient (Relative $R_{ds,on}$@150 °C) compared with SiC

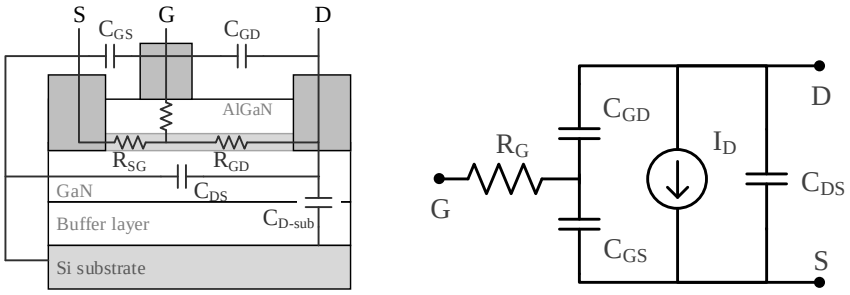


Figure 2.5: a) Diagram of the GaN HEMT diagram to highlight the parasitic elements. In particular, the distance between gate-drain is longer than for gate-source, making the channel resistance higher. b) Small signal model of GaN HEMT without any package parasitics.

MOSFETs. The increase in on-resistance from room temperature to 150 °C is in the range from 100 to 160% for the GaN HEMTs while only 30 to 40% for the SiC MOSFETs. Yet, the selected Si SJ FET has a comparable increase in on-resistance with temperature as the GaN HEMT. A consequence of the high temperature coefficient is that nominal operation will be at higher on-resistance than the quoted datasheet value, which, on the one hand, leads to higher conduction losses. On the other hand, a positive and high temperature coefficient makes such devices suitable for paralleling.

2.2.2 Reverse current conduction

The third quadrant operation for GaN HEMT is slightly different than for other unipolar devices. Since there is no doping in the HEMT structure, there is no body diode either. Yet, the HEMT can still conduct a current in the reverse direction. When the drain-gate voltage reaches the threshold voltage of the device, the device channel opens [25, 34]. The basis for the reverse conduction property of HEMTs lies in the symmetry of the structure. Since there is no doping, there is no difference between drain and source contacts with respect to the gate contact. This symmetry is transferred to the circuit diagram shown in Fig. 2.5(a). The only difference is the distance. Hence, the channel will start conducting if either V_{gs} or V_{dg} are higher than the threshold voltage [44]. The effective gate voltage, $V_{gs,eff}$, is expressed as:

$$V_{gs,eff} = V_{gs} - R_{gs} I_d \qquad \text{in forward conduction} \qquad (2.1)$$

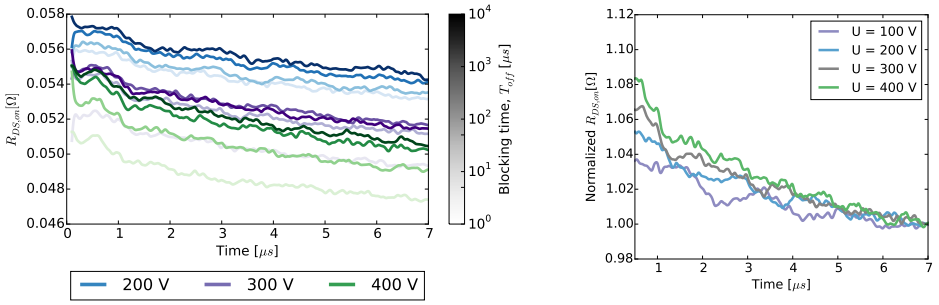
$$V_{gs,eff} = V_{ds} - V_{gs} - R_{gd} I_d \qquad \text{in reverse conduction} \qquad (2.2)$$

where R_{gs} and R_{gd} are the contact and channel resistance between source-gate and drain-gate, respectively. However, the transconductance will be lower in reverse conduction than in forward conduction [44]. As mentioned, the distance between drain and gate is longer than for source and gate, as illustrated in Fig. 2.5(a). With a given sheet resistance of the channel, the drain-gate resistance, R_{gd}, and, hence, the voltage drop, will be higher than for source-gate for the same current amplitude. This voltage drop leads to a decrease in the effective gate voltage, and thus the voltage drop over the device will be higher for the same current. Additionally, if the device is driven with a negative gate voltage during the off-state, $V_{gs,neg}$, this voltage is added to the device voltage drop.

As a circuit analogy, e-HEMT devices can be modelled as having a body diode with high forward voltage drop ($\geq$2 V + $V_{gs,neg}$ if looking to Table 2.1), and no reverse recovery charge. Nevertheless, if the device is turned on, the channel can conduct in the reverse direction with similar on-resistance as for the forward current direction.

2.2.3 Parasitic capacitances and small signal model

Due to the extent of the geometry, there are parasitic capacitances between the device terminals and the substrate, as indicated in Fig. 2.5(a). Since the parasitic elements and channel behaviour are similar to other power devices, the same small signal model can be used (ref Fig. 2.5(b)). The effect of the capacitors C_{gs}, C_{dg}, and C_{ds} on the device behaviour is, again, the same as for other unipolar devices; the drain current source depends on the gate-source voltage, and, during turn-on and turn-off, the gate-drain and drain-source capacitors are charged and discharged. However, since GaN HEMTs are lateral devices with an insulating layer (buffer layer) between the active region and the substrate, there are also parasitic capacitances between the device terminals and the substrate. Usually, the substrate is shorted to the source terminal, thus the source-substrate capacitor is not shown in Fig. 2.5(a). In contrast, the capacitor C_{d-sub} is not shorted and plays a role in the device losses that will be discussed in Section 2.2.5. However, it is of less importance for the switching behaviour. In total, the GaN HEMT can be modelled with the same small signal model as used for other unipolar devices; the three parasitic capacitances and the channel current determined from the device transfer function. However, some modifications must be made to account for third quadrant behaviour and the applied gate voltage. Additional parasitic inductance and resistance due to packaging can also be included in the modelling, yet this is standard procedure for all types of devices.



(a) **(b)**

Figure 2.6: Example waveforms of the development in the device resistance with time that show the effect of dynamic on-state resistance. Test object is a 55 mΩ GaN HEMT (GS66506T). a) Measured resistance in absolute terms from 200 ns to 7 µs for different dc-link voltages and blocking times [**P3**]. b) Comparing the relative change in resistance for the same blocking time of 50 µs, but with different dc-link voltages [**P3**].

2.2.4 Dynamic on-state resistance, $\mathrm{R_{DS,on}}$

An added characteristic of GaN HEMT devices compared to other power devices is that the on-state resistance is not a static parameter. Common to all power device types is that the on-state resistance depends on the junction temperature. In addition, the GaN HEMT on-resistance has a time dependency, and is thus dynamic in nature. The dynamic on-state resistance is also known in the literature as current collapse, or gate lag in the radio frequency domain. The dynamic behaviour contains several time constants which further complicate the phenomenon [23, 30]. The increase in resistance depends on many operating parameters, among which the most influential are off-state voltage, on- and off-times (frequency and duty cycle), junction temperature, and switching mode (hard- or soft-switching, HS/SS). Naturally, the influence of each parameter also varies among manufacturers. Figure 2.6 shows example waveforms of the time variation in the device resistance [**P3**]. After blocking the dc-link voltage for the indicated blocking time, the device is turned on and the resistance is measured from 200 ns to 7 µs. In Fig. 2.6(a), the resistance is shown in absolute value for varying blocking time and dc-link voltage. For reference, the datasheet resistance value is 55 mΩ. In Fig. 2.6(b), the relative change from start to end is plotted for the same blocking time. The current is kept constant at 10 A for all tests. The device resistance is observed to decrease over time.

The underlying mechanism of the current collapse is the trapping of charge in different parts of the HEMT structure; in interface layers around the gate or originat-

ing from traps in the buffer layer [5, 57, 65]. Early reports showed a substantially increased on-resistance in GaN HEMT devices. To address this issue, manufacturers worked on improving the surfaces in interface layers. Additionally, using field plates to shape the electric field around the gate terminal towards the drain terminal was shown to counter the current collapse. Later, injection of holes on the drain side using p-GaN has also been demonstrated to be an effective technique to decrease the impact of the issue [10, 26, 52] (see Fig 2.5(a)).

The literature contains many circuit suggestions for measuring the dynamic on-state resistance. A common limitation for the circuits is the time delay from when the device is switched on until the measurement can begin. In 2017, the author presented such a measuring circuit in [**P3**] with a time delay of approximately 200 ns and high measurement precision. Most circuits have had a limitation of 200 ns or more, and improvements are made continuously. The lowest reported time delay is approximately 10 ns [31]. This delay relates to how long it takes to discharge the capacitance of the blocking device and for any oscillations to settle. Hence, the delay time is constant and poses a limitation to the maximum frequency for which the on-resistance can be measured. An alternative is to measure the dc input power to a test circuit while accurately estimating other loss factors [13]. The remaining losses are attributed to the conduction losses of the device under test. Several works highlight the need to run measurement tests over several pulses since the first pulse in a double pulse test is not representative for the steady state behaviour. However, in pulsed operation or steady state, it becomes increasingly difficult to separate the dynamic resistance behaviour from static resistance.

Although there is an increasing number of papers on the subject, it is difficult to draw clear conclusions. As summarised in [65], variations in testing methodology and reporting technique lead to confusion. One particular aspect that creates confusion is that the reported dynamic resistance is relative to 25 °C. Since the static resistance of GaN HEMTs has a substantial temperature coefficient (ref Table 2.1), it becomes difficult to differentiate between the loss contribution of the dynamic resistance and the known static behaviour of the tested device. Thus, the reported increase in device resistance might be exaggerated. Despite the current state of reporting in literature, a summary of the effect of operational parameters most commonly found in the literature is given in Table 2.2 along with (non-exhaustive) examples.

Regarding the off-state voltage, the literature is almost unanimous in stating that higher voltage leads to increased on-resistance. However, the device-specific trends are not equal. Some devices increase resistance linearly with voltage while some hit a knee voltage after which the dynamic resistance decreases with voltage [32]. This could potentially be linked with the wafer production, as increased leakage

current at higher voltages leads to de-trapping in off-state [40, 57]. Moreover soft-switching can limit the significance of the off-state voltage on dynamic resistance [65].

In addition, the literature is unanimous in expressing that increased operating frequency leads to increased on-resistance. This is related to the difference in trapping and de-trapping time constant, where the latter is significantly larger than the former. Hence, increased frequency leads to less de-trapping and increased resistance. Using some examples of results, [32] shows that the resistance increases up to twice the nominal value at 1 MHz. At an operating frequency of 3 MHz, the on-resistance of GaN HEMT devices is reported in the range of 4 to 6 1 times the $R_{ds,on}$ at 25 °C depending on blocking voltage and junction temperature [13]. Similarly, an increased duty cycle will give more time for de-trapping and, hence, the resistance decreases [2, 3, 65].

As indicated in Table 2.2, the effect of temperature is not consistent across recent literature. Although increased junction temperature leads to higher static resistance, [37, 65] demonstrate that high temperature does not lead to increased dynamic resistance. Rather, it is shown that higher temperature leads to shorter de-trapping time and, consequentially, lower dynamic resistance compared to low temperature measurements. In contrast, [33] states the opposite, although this could be due to wafer quality (see difference in 'epi vendors' in [57]). A consequence of the negative temperature coefficient of the dynamic on-resistance is that the device is less prone to thermal runaway. Moreover, it has been shown that minimal trapping can be achieved by optimising the device production process [39].

In addition, the effect of hard-switching and soft-switching modes on the dynamic on-resistance has also been investigated. If operating in hard-switching mode, hot-electrons generally lead to more trapping of charge, thus the dynamic resistance is

Parameter	Effect on dynamic $R_{ds,on}$	Citation
Off-state voltage	Increase	[65, 12, 32, 4, 13, 29]
Frequency	Increase	[65, 29, 12, 32, 4]
Temperature	Depends	[65, 37, 33, 4]
Hard-switching	Depends	[65, 32]

Table 2.2: Overview of influence from different operational parameters on the dynamic on-resistance.

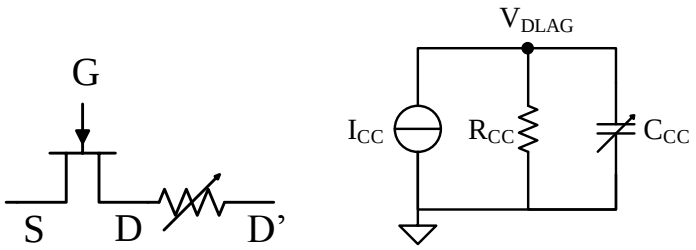


Figure 2.7: GaN HEMT model to model dynamic on-state resistance [**P3**]. The value of the resistance between D and D' depends on the voltage value, $VDLAG$.

more pronounced compared to the soft-switching mode [10, 65]. In contrast to this finding, the GaN HEMT structure with hole-injection at the drain contact [26] has been shown to have higher losses in soft-switching compared to hard-switching when subjected to high voltage during the off-state [32]. Consequentially, the choice of device manufacturer can be influenced by the intended application.

It is clear from the historic trends that manufacturers are finding ways to alleviate the problem. The industry is continuously demonstrating advances in device performance [24, 26]. Regardless of future improvements, the lack of dynamic on-resistance after microseconds of conduction shows that this effect is of lesser importance for converters operating with frequencies lower than 100 kHz. To date, there is no standard way of reporting dynamic on-state resistance even though some initial attempts have been made [12, 65].

Attempts have been made to include dynamic resistance in device models [41], [**P3**]. In [**P3**], an implementation of dynamic on-state resistance was demonstrated in a SPICE simulator software. The model, shown in Fig. 2.7, is used to change the resistance element of the active device with a time-dependent behaviour. The capacitance value is changed according to the operating point. Although shown with a single time constant, additional time constants could be added. However, the large amount of operational parameters that affect the on-state resistance make it difficult to suggest a global model. Furthermore, without a global model, it becomes challenging to include this dynamic effect in design tools such as SPICE simulators. Thus, for the time being, engineers in high-frequency applications will have to expect increased resistance and include margins during the design phase.

2.2.5 Output capacitor hysteresis losses, $\mathrm{C_{OSS}}$ losses

All power devices are characterised by a parasitic output capacitance between the power terminals, often referenced as C_{OSS} (small-signal output capacitance) taken

from the designation in device datasheets. When using a soft-switching technique such as zero-voltage switching (ZVS), external reactive components are used to discharge the capacitor before the device turns on. Thus, the turn-on losses are eliminated. However, it is reported that GaN HEMT devices experience losses even though the devices are not conducting a current through the channel but only experiencing charging and discharging of the output capacitor [50, 61, 63]. The loss mechanism appears as a hysteresis effect when charging and discharging the output capacitor, similar to Si super-junction devices [11, 47]. The implication of this effect is that soft-switching converters will experience additional losses despite the implementation of soft-switching techniques.

This hysteresis loss component has been shown to depend on $\mathrm{d}v/\mathrm{d}t$, device manufacturer and substrate biasing [61, 63]. Further investigations show that the losses stem from the current going through the parasitic capacitance between drain and substrate [16, 62]. The buffer layer, as for dynamic on-resistance, is identified as one of the perpetrators. More specifically, the trapping and de-trapping process leads to losses that are temperature dependent, with room temperature identified as the worst-case condition [62]. Moreover, losses occur as the drain-substrate current passes resistance of the buffer layer and the substrate resistance [62]. Although the details are scarce, it has been demonstrated that buffer layer optimisation can dramatically reduce C_{OSS} losses [16]. The continuous efforts demonstrated by researchers and manufacturers give reason to believe that this loss factor can be reduced for future commercial devices.

Since the loss scales with frequency and voltage, significant losses occur for converters operating at switching frequencies in the range of megahertz and above. Yet, for a given application, these losses can be taken into account at a design stage. In the literature, the losses are expressed as a percentage loss of the output capacitance energy per switching cycle [63]. In resonant converters, the frequency and switch voltage are not only known, but they are also mostly static in steady-state operation. Hence, the losses can be included in the design phase, and even in SPICE-based circuit optimisations, as demonstrated in [**P5**]. For completely static operation, the additional loss component can be estimated as:

$$\begin{aligned} P_{C_{OSS},} &= \%_{percycle} \cdot E_{oss} \cdot f \\ &= 0.5 \cdot \%_{percycle} \cdot C_{OSS} \cdot V_{ds}^2 \cdot f \end{aligned} \tag{2.3}$$

where $\%_{percycle}$ is the per cycle percentage loss of the E_{OSS} that can be approximated from C_{OSS}, the small signal capacitance, at the maximum switch voltage, V_{ds}. In SPICE, this loss can be included by using equation-based current sources.

If no actions are taken to model the additional losses, the discrepancy between the expected losses and the experimental results will be high. Examples from measurements in [**P5**] are shown in Fig. 2.8. The experimental inverter losses are estimated using a calibrated loss model with the measured inverter temperature as input. Figure 2.8(a) shows the inverter losses for the initial prototype that was used to tune the simulations. The grey shaded area shows the added C_{OSS} losses as estimated from Eq. 2.3. Consequently, the gap between the simulated and the experimental losses is decreased. For the converter optimisation, the C_{OSS} losses were added in the SPICE environment.

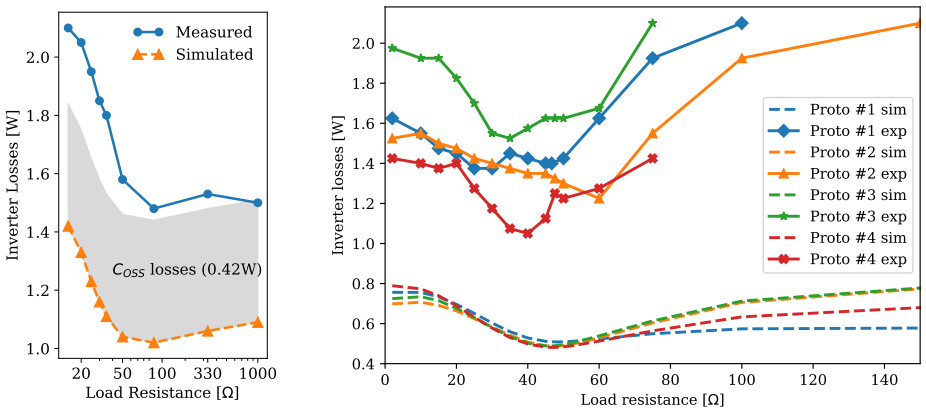
The comparisons between simulated losses and experimental losses for the four prototypes are shown in Fig. 2.8(b). Even though the added loss would decrease the gap, there are other challenges in estimating inverter losses. Firstly, the temperature coefficient and the dynamic behaviour of the on-state resistance will have to be accounted for. One approach to this challenge could be the common engineering practice of adding a margin, e.g. by multiplying the datasheet resistance with a safety factor to account for these additional losses in an early design phase. Secondly, a substantial loss contribution comes from parameter variation for both the active and the passive components. In case the variation results in a loss of soft-switching, the additional losses are considerable. This has been observed for several operating points of the four prototypes. The design engineer should therefore guide the design parameters towards more robust solutions. In [**P5**], this was done for the experiment where prototype #4 supplied power to four Cree SiC drivers (CRD-001). The series capacitance was increased slightly, and the length of the PWM signal adjusted so that soft-switching was ensured for the whole operating range. As a result, the converter operation was well within thermal limits.

2.3 Identification of application areas utilising the qualities of GaN HEMTs

Previously, this chapter has focused on the particularities of the GaN HEMT device, highlighting both the possibilities and the challenges. However, from an application point of view, it is of interest to compare GaN HEMTs to the other power device technologies on a common basis. Here, the loss components of the active device are used as a basis to highlight the application areas where GaN HEMT has a clear advantage. In general, the semiconductor losses can be divided into three parts:

$$P_{semiconductor} = P_{conduction} + P_{switching} + P_{gate} \tag{2.4}$$

The conduction losses, $P_{conduction}$, occur during the on-time of the device or dur-



(a) **(b)**

Figure 2.8: Visualisation of the difference in inverter losses between simulation and experimental results. a) Loss difference for the initial prototype used to tune the simulations [**P5**]. The grey area shows the approximated hysteresis losses of the output capacitance. b) Loss difference for the four prototypes of the Pareto front. Simulated values use the datasheet on-state resistance.

ing the freewheeling period. As has been shown, devices with similar ratings for on-state resistance are available in all technologies. Hence, the conduction losses in a given application are similar for various technologies. Therefore, to find a suitable application area for the GaN HEMT, simply stating that GaN HEMTs have low conduction losses is not adequate to differentiate them from the other technologies. Instead, a different loss aspect must be identified.

Switching losses

The switching losses in a converter are calculated as the integration sum of the volt-ampere area during turn-off and turn-on events:

$$P_{switching} = f_{sw}\left(\int^{t_{on}} V_{ds}I_d \ dt + \int^{t_{off}} V_{ds}I_d \ dt\right) \tag{2.5}$$

where f_{sw} is the converter switching frequency. Wide-bandgap devices have been praised for their capability of switching faster which in turn reduces the switching losses of a converter. Switching faster is also possible with Si technology. Yet, the gate driver circuit must be designed for higher currents due to the larger gate charge, Q_g, of Si devices (see comparison of Q_g in Table 2.3). Larger gate currents lead to stricter demands for the driver circuit, which are more likely to incur

Device	Type	Q_g [nC]	Q_{rr} [nC]	C_{OSS} [pF]	E_{OSS} [uJ]
IPT60R065S7	Si SJ	51.0	3900	32	40.7
C3M0065090J	SiC	27.4	245	60	8.0
IMZA65R072M1H	SiC	22.0	90	86	7.8
SCTH35N65G2V-7	SiC	66.0	85	125	10.0
SCT3060AL	SiC	58.0	55	55	9.0
GS66506T	GaN	4.4	0	49	5.3
IGT60R070D1	GaN	5.8	0	72	6.4
PGA26E07BA	GaN	5.0	0	71	7.5
TP65H050WS	GaN	16	125	130	15.2

Table 2.3: V_{SD} within a range of 8 to 13 A. C_{OSS} at 400 V except for Cree and SJ (600, 300V respectively).

gate oscillations and can require longer dead time[**O3**,**O5**]. Hence, wide-bandgap devices are easier to switch faster.

Although there are several circuit parameters that affect the switching losses, the stored output energy in the device capacitance influences switching losses directly. This energy is discharged in the device channel and leads to turn-on losses. The energy at the operating voltage across different device types can be evaluated and compared directly. Table 2.3 shows the small signal output capacitance, C_{OSS}, and the stored energy in this capacitor, E_{OSS} during turn-off. It is observed that, despite the C_{OSS} values being fairly similar for all devices, the stored energy differs between the various technologies. GaN e-HEMT devices have lower stored energy in the output capacitance and, therefore, have the best merit.

Reverse recovery loss and freewheeling time

An aspect that is included in the switching losses but is often discussed separately, is the reverse recovery loss of diodes. The recovery charge is the amount of charge that needs to be extracted from a diode's active region for the blocking capability to be reestablished after the diode has been conducting. During this time, the active device has to carry the load current and the reverse recovery current, resulting in additional losses in the device that is turning-on. A comparison in the reverse recovery charge of the different technologies is given in Table 2.3. Only qualitative comparisons should be performed since the test conditions stated in the datasheets vary considerably. The important differences are between the Si technology and wide-bandgap devices. It is observed that the body diodes of modern SiC MOS-

FET have small reverse recovery effects compared to Si power diodes [54]. The complete lack of recovery charge in the HEMT structure leads to even lower losses in hard-switching converters. This feature is also present in Schottky diodes. In contrast, the GaN cascode device (TP65H050WS) has a small reverse recovery charge due to the internal LVMOSFET, another feature that might limit the use of these devices at elevated frequencies.

However, GaN HEMTs have high reverse current conduction losses compared to Si power diodes or SiC Schottky diodes. Consequently, the converter efficiency is sensitive to the length of the freewheeling period, e.g. length of the dead time in a bridge converter. This component also scales with frequency, and, hence, there is a considerable interest in minimising the dead time, especially for converters operating in frequencies higher than 100 kHz [8, 15, 60].

Gate losses

The gate losses are approximated as:

$$\begin{aligned} P_{gate} &= f_{sw} \cdot Q_{gate} \cdot (V_{gs,pos} - V_{gs,neg}) \\ &= f_{sw} \cdot C_{ISS} \cdot (V_{gs,pos} - V_{gs,neg})^2 \end{aligned} \tag{2.6}$$

where Q_g is the gate charge, C_{ISS} is the small signal input capacitance, and $V_{g,pos}$ and $V_{g,neg}$ are the positive and negative gate driver voltages. From Eq. 2.6, it is clear that wide-bandgap devices offer lower losses for the same device rating. Firstly, the input capacitance of the devices is smaller for the same rated on-state resistance, e.g., from Table 2.3, Si SJ – 1932 pF, average for SiC devices – 907 pF, average for GaN devices – 327 pF. Despite GaN and SiC devices both having low input capacitance, the gate charge is the lowest for GaN devices. This is visible from the Q_g quoted in Table 2.3. The gate voltage needed to drive the GaN device is smaller than for both Si and SiC devices. Typical numbers for GaN HEMTs are around 5 V, while for SiC devices this increases to a range from 15 to 20 V if the nominal gate voltage from the datasheet is chosen. Hence, the total gate charge for GaN HEMTs becomes smaller. As a remedy, resonant driver structures can be used for high-frequency Si and SiC MOSFET based converters, but they come at the price of increased complexity [55]. For GaN HEMTs, the low gate losses allow for integration of the gate driver in the same package as the power device [21].

Effect of lower output capacitance with less non-linear behaviour

The magnitude and non-linearity of the device capacitance has a large impact on the switching behaviour and the converter design. These effects will be highlighted

here for both hard-switched and soft-switched converters. Table 2.4 shows a comparison between a GaN HEMT, a SiC MOSFET and a Si SJ FET in terms of magnitude and non-linearity of the output and reverse transfer capacitances. The C_{OSS} value at 400 V is similar for all devices, but the change in capacitance from zero voltage is somewhat different. Similar relations are seen for C_{RSS}. As has already been discussed, the energy stored in C_{OSS} affects switching losses, and wide-bandgap devices are favoured. Moreover, a large change in C_{RSS} will lead to a more 'snappy' voltage waveform during switching, which leads to EMI issues. For Si SJ FETs, some converter designers will add discrete, fixed capacitance in parallel to the device to minimise this effect.

For soft-switching applications, the switching losses are close to eliminated. Yet, there is still an advantage of GaN HEMT over Si counterparts (although a comparable performance with SiC MOSFETs). Since the output capacitance, C_{OSS}, and its stored energy, E_{OSS}, are lower, shorter dead-time or lower circulating current is needed for achieving zero-voltage switching. In the case of zero-current switching, lower energy is lost in each cycle. All of these have advantages for the converter performance, either in terms of efficiency and/or output voltage quality.

For resonant converters, the output capacitance can affect the possible design range. If the converter resonance frequency, ω, and the inductance, L, are given, the capacitance needed in a series resonance becomes:

$$C = \frac{1}{\omega^2 L} \tag{2.7}$$

In resonant converters, a discrete linear capacitor is most often placed in parallel with the capacitance of the active device. Consequentially, the capacitance, C, is the sum of the non-linear device capacitance and the linear capacitance of the external capacitor. Often, the design rules assume that the ratio between the linear and the non-linear capacitor is high, hence, the total capacitance can be considered linear [45, 49]. Therefore, lower device capacitance gives better linearity in such cases. Compared to vertical Si MOSFETs, wide-bandgap devices will have lower capacitance for the same on-state resistance. Si SJ FETs are not used in resonant converters due to their highly non-linear device capacitance.

On the contrary, if the device capacitance is higher than the capacitance calculated in Eq. 2.7, the design is not feasible. Many high-frequency designs require capacitances in the same order of magnitude as the device capacitance [45]. At the boundary case, only the device capacitance is used in the resonance tank [7, 51]. Then the non-linearity of the device capacitance influences the converter performance, e.g. power capability and resonant overvoltages.

Device	C_{OSS} @0V	C_{OSS} @400V	C_{RSS} @0V	C_{RSS} @400V
GS66506T	400 pF	49 pF	50 pF	1.5 pF
C3M0065090J	1100 pF	80 pF	100 pF	4 pF
IPT60R065S7	20 000 pF	32 pF	1100 pF	70 pF

Table 2.4: Caption

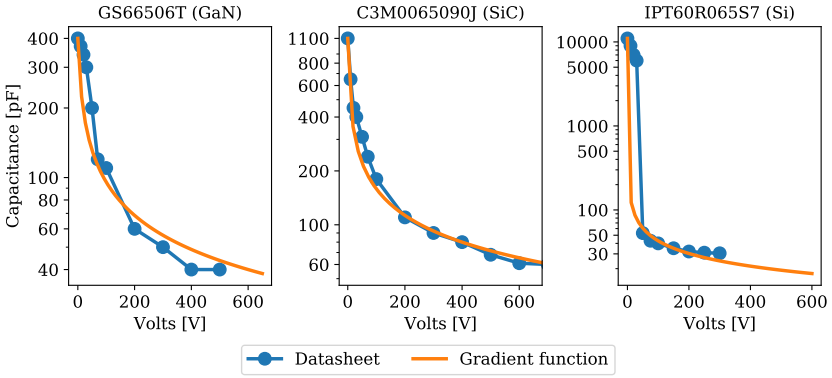


Figure 2.9: Modelling of non-linear capacitance and comparison to the datasheet values. a) GaN HEMT device (GS66506T). b) SiC MOSFET device (C3M0065090J). c) Si SJ FET device (IPT60R065S7)

To investigate the difference in the non-linear capacitance, three devices of different technologies are modelled, and the equivalent linear capacitance value is found. A common mathematical function for modelling the voltage-dependence of the junction capacitance for diodes is the gradient function [7]:

$$C(v) = \frac{C_0}{\sqrt{1 + \frac{v}{V_{bi}}}} \tag{2.8}$$

where C_0 is the initial capacitance value at zero volts and V_{bi} is the built-in potential of the pn-junction. The coefficients for each function are optimised for each of the three devices. The model output is compared to the datasheet capacitance, and the optimisation aims at minimising the error. For the error, a normalised root mean square deviation is used:

Device	C_0	V_{bi}
GaN	400 pF	6.06 V
SiC	1100 pF	2.33 V
Si SJ	11 015 pF	1.51 mV
Typ. Si values	–	0.5 to 0.9 V [51]

Table 2.5: Optimised parameters for fitting the gradient capacitor model to the datasheet values of each device.

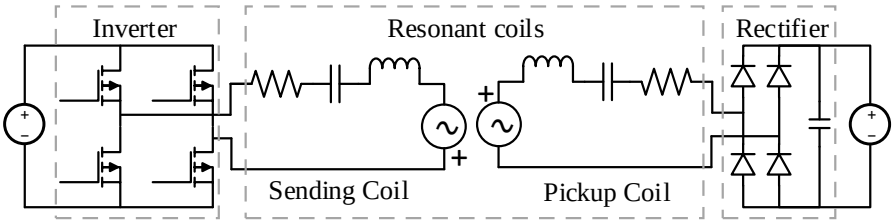


Figure 2.10: Schematic diagram of the wireless power transfer converter system, where the GaN HEMT replaced the Si MOSFETs in the full-bridge inverter on the sending side.

$$err = \sum_{i=1}^{N} \frac{\sqrt{(C_{datasheet,i} - C_{model,i})^2}}{C_{datasheet,i}} \tag{2.9}$$

where i indicates the index among the N points for which the capacitance was read from the datasheet. The parameters for the three devices are shown in Table 2.5. The extracted datasheet capacitance values and the model capacitances are shown in Fig. 2.9. For the GaN HEMT and the SiC MOSFET, the capacitance model corresponds well over a large operating area. The discrepancies are larger for the Si SJ FET due to its step-like behaviour of the output capacitance.

The value of V_{bi} indicates how non-linear the capacitance is. The higher the value, the more linear the capacitance is. From Table 2.5, it is observed that the GaN HEMT has the most linear device behaviour, with the two wide-bandgap devices having substantially higher values than the typical value for Si devices. This can lead to lower resonant overvoltages and more ideal converter performance [7, 51].

2.3.1 Hard-switching versus soft-switching applications

The author has demonstrated the GaN HEMT performance in both hard-switched and soft-switched modes in [**P1**]. The application system is shown in Fig. 2.10 and consists of a full-bridge inverter feeding a series-series compensated resonance circuit in a WPT application [17]. On the secondary side, the ac power is rectified by a full-bridge rectifier and fed to the dc-load. The nominal output power of the system is 580 W. The inverter operates in both soft-switched mode and hard-switched mode depending on the load and the coupling of the transformer coils. At nominal load the converter operates at 104 kHz. As the load power decreases, first the frequency is increased from 104 to 137 kHz. For the lowest loads, the inverter operates at maximum frequency and uses hard-switching to limit the sending power. For the test case in [**P1**], the inverter is soft-switching for loads higher than approximately 35%. In theory, soft-switching eliminates switching losses and conduction losses are the only remaining factor. Therefore, the experiment was designed to compare the technologies in hard-switched mode only, since the soft-switching performance will be dominated by the on-state resistance.

The recorded efficiency for both the Si- and GaN-based full-bridge inverters while operating in hard-switched mode up until the inverter is soft-switching, is shown in Fig. 2.11. Moreover, the theoretical inverter efficiency with only conduction losses is also indicated. In soft-switched mode, the Si-based converter performs better than the GaN HEMT due to its lower on-state resistance. In hard-switched mode, however, the GaN HEMT-based converter clearly outperforms the Si-based converter as expected, in particular since the gate resistances of the GaN HEMT inverter were optimised for fast switching. The effect of dead time and reverse conduction losses for GaN HEMTs was also investigated. A reduction in dead-time from 70 ns to almost zero gave an efficiency increase by 0.25 % at 20% load.

The key take-away points from this work is that low conduction losses can be obtained with other technologies, as previously discussed in this chapter. However, for the Si inverter, the large chip area needed leads to decreased performance when hard-switching is utilised. GaN power devices can therefore obtain both characteristics simultaneously, although the GaN HEMT inverter efficiency is more sensitive to the freewheeling time. Thus, the freewheeling time should be minimised to the full extent possible, in particular at elevated operating frequencies.

2.3.2 Drop-in replacement

A drop-in replacement suggests that the previous active device in an application is replaced by a GaN HEMT with similar ratings. Replacing Si IGBTs with GaN HEMT as a drop-in replacement for household appliances and electric vehicles is

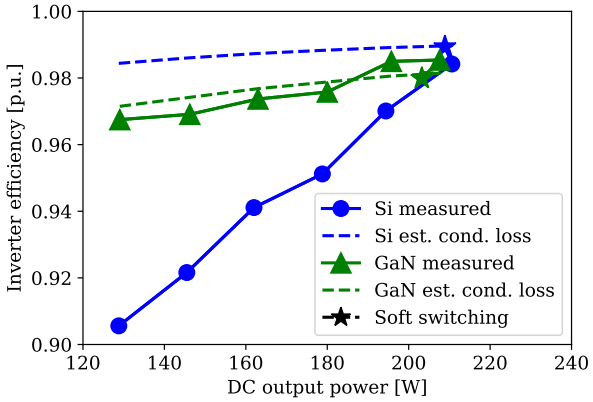


Figure 2.11: Efficiency comparison between full-bridge inverters based on Si MOSFETs and GaN HEMT from [**P1**].

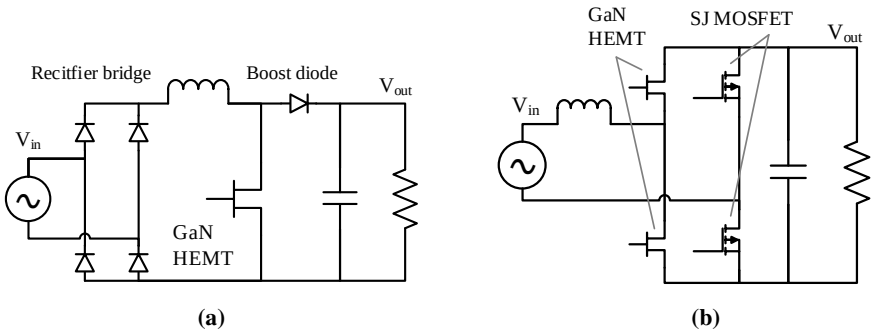


Figure 2.12: Schematic diagrams of two power factor correction (PFC) circuits. a) Continuous conduction mode boost PFC topology. b) Bridgeless totempole PFC topology.

such an example [28]. The switching frequency and circuit topologies are kept unchanged, and the performance is compared. As expected, the GaN HEMT exhibits a better performance at lower loads due to the lack of a pn-junction and reverse recovery losses. Furthermore, the dead-time is decreased and the increase in system efficiency enables operation without a heat sink. In contrast, the unit cost is quite different with $1 and $10 at the time of writing for an order of 1000 units.

A power factor correction (PFC) converter, based on the continuous conduction mode (CCM) Boost PFC topology (Fig. 2.12(a)), with a GaN HEMT drop-in replacement is reported in [**P2**]. A peak converter efficiency of almost 97.8% was achieved, which is in the upper range for this topology [38]. The efficiency across

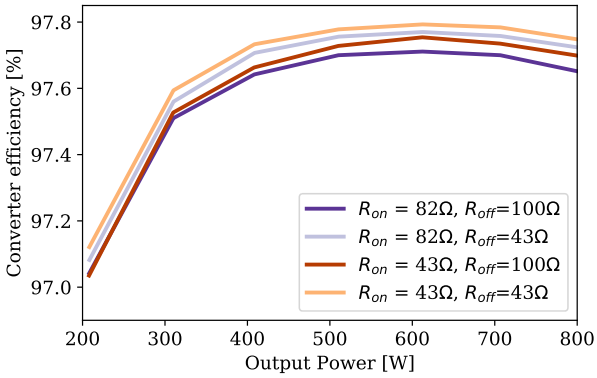


Figure 2.13: Measured efficiency for the GaN HEMT based PFC converter with changing gate resistors from [**P2**].

the whole operating range is shown in Fig. 2.13. When investigating the loss breakdown in a CCM Boost PFC, it is observed that only a small increase in converter efficiency is possible when using a GaN switching device [36, 66]. Given that the on-resistance of the active device is similar, the largest improvement comes from changing the boost diode from a Si power diode to a SiC Schottky diode. Adding that the switching frequency is relatively low (66 kHz), the lower switching losses using GaN HEMTs have a minor effect on the converter efficiency. The conduction losses can be decreased by using a GaN HEMT with lower on-state resistance; however, this will increase the converter cost. Moreover, the converter power density would only marginally increase if the switching frequency is kept constant. Hence, drop-in replacements such as those described above are not very attractive in an industrial setting for a new technology like GaN HEMTs.

2.3.3 Changing circuit topology

The more interesting application areas are those where the characteristics of the GaN HEMT device act as an enabling technology. That is to say, previous technology had inherent design and operation limitations hindering the system performance. For PFC converters, the GaN HEMT acts as an enabling technology due to the lack of reverse recovery. A new topology, the bridgeless totem-pole PFC topology seen in Fig. 2.12(b), becomes a promising contender in this application area [19, 35, 38] since the GaN HEMT replaces the input rectification diodes, the active switch, and the boost diode. Hence, the forward voltage drop of both the rectifier bridge diodes and the boost diode are removed. Additionally, the loss budget now allows for the switching frequency to be increased. Consequentially, the inductor, and possibly the filter size, decreases and the PFC converter can ob-

tain higher efficiency and higher power density.

2.3.4 High-frequency application

From the previous discussions of loss contributions and aspects of the GaN HEMT technology, frequency is a recurring parameter. All losses have been shown to scale with frequency. Conduction losses (R_{on}) and C_{OSS}-losses have been shown to increase with frequency while the lack of reverse recovery losses and low gate losses are benefits for GaN HEMTs. The advantages of using GaN HEMT devices in high-frequency applications can be summarised as follows:

1. Low driving losses
2. Low stored output charge
3. No reverse recovery charge

The needed gate charge compared to Si or SiC devices is lower, thus gate losses for GaN HEMTs will be approximately an order of magnitude lower at the same frequency. This is critical for the efficiency in low-power, high-frequency converters. Additionally, non-resonant gate drivers can be used, which are easier to design and implement.

The low output capacitance will benefit soft-switching converter topologies. Low $\mathrm{C_{OSS}}$ allows for better performance for most quasi-resonant converters. As previously discussed, devices for low output capacitance are beneficial to resonant converter design. The frequency range can be extended and more external capacitance can be added, resulting in a more linear behaviour. Additionally, for cases where only the device capacitance is used in the resonant tank, GaN HEMTs exhibit less non-linear capacitance behaviour. Subsequently, the resonant overvoltages are decreased and the converter power capability is closer to the ideal case.

An investigation into the suitable marked segments in high-frequency resonant inverters employing commercially available GaN HEMT, SiC MOSFET or Si SJ has been published in [64]. This study shows that currently available GaN HEMTs have lower losses in the high-frequency application area. The losses include the C_{OSS} losses; however, the on-resistance's frequency and temperature dependence are not take into account. Since C_{OSS} for GaN HEMTs scale with frequency, there exists a boundary where SiC MOSFET becomes the preferred choice. For a $V_{ds,max}$ of 600 V, this boundary is estimated to exist around 20 MHz for low current, increasing towards 50 MHz for load currents greater than 10 A. For lower drain voltages, the maximum frequency limit for GaN HEMTs increases. Yet, using SiC MOSFET at such elevated frequencies requires the use of resonant drivers

to limit the gate losses. Finally, it should be highlighted that the frequency limit is identified from evaluating losses in the active device including gate losses, but practical considerations are not accounted for.

2.4 Conclusion

Based on the background information regarding the fabrication method and theoretical performance limits, it is clear that GaN HEMT is part of the wide-bandgap semiconductor devices of the future. However, the current available devices have lower specific resistance than their theoretical limits and exhibit additional loss mechanism compared to other power device technologies. Dynamic on-state resistance and output capacitor hysteresis losses give significant loss contributions, especially at elevated operating frequencies. Until manufacturers are able to minimise these loss factors, GaN HEMTs in practical implementations are underperforming compared to their theoretical potential. Nevertheless, commercial GaN HEMT devices are already demonstrating good performance compared to the competing technologies, and the market size is increasing. However, due to the high cost of new technology, it is of interest to identify application areas where GaN HEMTs enable new applications or significantly increases the converter performance. From the investigation and discussion of the device characteristics, GaN HEMTs appear to have an advantage over competing technologies in high-frequency (higher than 100 kHz) and low-power applications (up to approximately 1 kW).

First of all, current GaN HEMT devices are limited commercially to 650 V, which in itself naturally limits the power range for the technology. In addition to improved converter efficiency, the low gate-driver losses open up the possibility of integrated gate drivers in the device package. Consequently, smaller converter footprints and improved power density are achieved. Moreover, the lack of a pn-junction and low output capacitance enables higher efficiency, particularly at lower converter loads. In addition, the lack of reverse recovery losses makes the GaN HEMT an attractive candidate in bridge circuits as long as the freewheeling time is limited.

For high-frequency applications, the low output capacitance, lack of reverse recovery losses and low gate-driver losses enable operation at higher frequencies for many applications. By using resonant converters and soft-switching techniques, the operating frequency is increased into the megahertz ranges, which in turn can decrease the size of passive components and reduce the converter footprint. WPT is such an application. A particularity of WPT systems is the loosely coupled transformer. By removing the magnetic core of the transformer, high frequency becomes increasingly important for the system efficiency and size. Using loosely coupled transformers could be expanded to other power supply applications.

One application in this category is auxiliary power supplies for power modules in medium-voltage converters, supplying power to the gate drivers, sensors and control circuits. The required medium-voltage isolation necessitates the use of a high-frequency transformer. If the frequency of the auxiliary power supply can be substantially increased, a loosely coupled transformer can be used without suffering large penalties in efficiency and power density. It is GaN HEMT technology that enables the power supply to simultaneously obtain high frequency and high efficiency. The potential of GaN HEMTs will be demonstrated by developing and experimentally validating a design and optimisation methodology for a dc-dc converter with high isolation voltage operating in the multi-megahertz frequency range. Subsequently, the following chapters are divided in order to highlight different parts of the development phase. Firstly, a suitable resonant converter structure for high-frequency operation of the auxiliary power supply is identified, followed by separate investigations and optimisation of the converter circuit and the isolation transformer.

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Chapter 3

Resonant circuit topologies for high-frequency application

This chapter discusses different circuit topologies for high-frequency applications based on the literature review. Additionally, simulation results of the investigation of the class E rectifier from [**P5**] are presented and discussed at the end of the chapter. In this context, high frequency refers to the multi-megahertz range. In particular, the ISM frequency bands[1] are targeted in research due to the allowed radio noise emissions in these bands. The lowest available band is at 6.78 MHz, with sequential bands available at 13.56, 27.12, and 40.68 MHz.

The investigated topologies are intended for a dc-dc converter topology, as shown in Fig. 3.1. It consists of an inverter, a loosely coupled transformer, and a rectifier, all designed for high-frequency operation. For frequencies into the multi-megahertz range, resonant converter topologies are used owing to low switching losses. The inverter and rectifier must be chosen based on their compatibility regarding the output source behaviour and the input source requirements. Moreover, the operating point of many resonant topologies is in-part defined by the load resistance. Hence, the converter operation is load dependent unless specific measures are taken in the topology selection and design phase, or by implementing a control scheme. Consequentially, the suitability of the inverter and rectifier with the load behaviour must be ensured.

All of the resonant circuit topologies discussed in this chapter are used in high-frequency applications due to the elimination of switching losses using soft-switching techniques. Zero-voltage switching (ZVS) can be achieved both at turn-on and

[1] ISM = Reserved frequency bands intended for **i**ndustrial, **s**cientific and **m**edical applications.

Figure 3.1: Block diagram of the converter structure, where the topic of the chapter, the inverter and rectifier, are highlighted.

at turn-off. For turn-on, the load, as seen from the inverter, must be inductive at the operating frequency such that the voltage of the output capacitance is discharged before the device turns on. For zero-voltage turn-off, the presence of a capacitor over the drain-source terminals leads to low voltage during the turn-off phase. Furthermore, zero-current switching (ZCS), sometimes termed zero-voltage-derivative switching (ZDS), can also be implemented to lower switching losses. Again, the reactive elements in the converter topology are used to shape the current at the switching instant. For the resonant rectifiers, it is of interest to design them with low di/dt when using power diodes with a *pn*-junction to reduce reverse-recovery losses. Moreover, resonant rectifiers aim at avoiding steps in the diode voltage during switching, but rather use the junction capacitance in resonance circuits so that the stored energy is used or circulated rather than dissipated or radiated. Additionally, avoiding step-like behaviour in the waveforms reduces the generated EMI of the converters.

Since the operating frequency is so high, circuit design focuses on topologies that are inherently self-regulating. In comparison, for lower frequency ranges, a control system can be designed to achieve soft-switching behaviour over a large operating range. When operating with frequencies in the ISM bands, control and sensor technology effectively limits such schemes.

Contributions

This chapter presents an evaluation and comparison of resonant topologies for a high-frequency application that can incorporate a loosely coupled transformer. In addition, the topology selection is aimed at reducing the component count such that a high power density solution is identified. For the identified rectifier topology, the improved design procedure is presented in [**P5**]. It is demonstrated that the rectifier can achieve higher efficiency, inherent voltage regulation and very low component count when designed with a resonance frequency higher than the operating frequency. Although each of these characteristics is separately indicated in the literature, they have not been investigated and demonstrated together, as in [**P5**]. Additional results of the investigation are presented in this chapter.

3.1 High-frequency resonant inverters

As candidates for high-frequency inverters, class D/DE, class E, class EF, and class Φ_2 inverters will be presented in this section. After the presentation, a comparison and a discussion on the suitability of the topologies for the application introduced in Chapter 1 using GaN HEMTs are presented.

3.1.1 Class D and class DE inverters

The class D inverter is a switching amplifier that can be implemented either as a half-bridge or a full-bridge circuit. For this work, only the half-bridge variant is considered. It consists of two series-coupled switches that are fed by a dc-voltage. The mid-point of the switches is the ac signal output terminal. As seen in Fig. 3.2, the half-bridge inverter is combined with a resonance tank of two or more elements to obtain soft-switching operation. One advantage of class D circuits is that they can operate over a wide load range [1]. That is to say, the soft-switching characteristic is not affected by the load resistance. Another advantage of class D inverters over the other topologies is the high switch utilisation. The maximum voltage over each switch is equal to the dc-link voltage. This leads to a higher output power compared to other amplifiers when using components rated for the same peak current and peak voltage [9].

However, large switching losses can be experienced when using class D inverters. Even if the impedance, as seen from the inverter, appears purely resistive, the output capacitance of the switches is discharged in every switching cycle. In turn, this leads to large losses at high frequency. By having a suitable dead time and having an inductive load seen from the inverter, ZVS can be obtained. This operation and circuit topology is referred to as the class DE inverter [13, 22]. During the dead-time interval, the output capacitances of the switches are charged and discharged as part of the resonance tank, hence, turn-on ZVS is obtained. With this augmentation, it has been analytically shown that the maximum frequency limit for the class DE half-bridge inverter is close to the class E inverter frequency limit [22].

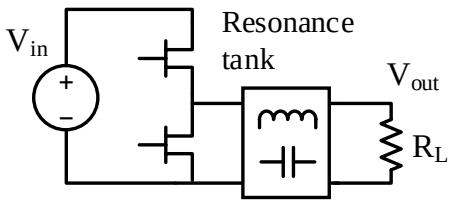

Figure 3.2: Schematic diagram of a class D half bridge amplifier.

Nevertheless, there are practical limits for this topology related to the inverter implementation. In hard-switching circuits, the required PWM resolution creates a challenge; however, this is not the main challenge. Rather, the timing requirements for the driver implementation are difficult to fulfil. Especially for the higher frequency bands, every nanosecond offset can influence the converter behaviour. Due to the varying potential of the ac-node in the half-bridge, the high side switch needs a floating driver supply and an isolated control signal. Implementing a signal-isolating circuit that also results in low mismatch between the low side and the high side signal becomes increasingly difficult with increasing dc-link voltage and operating frequency. As an example, there are several published examples of class DE inverters operating at 6.78 MHz with dc-link voltages of several hundred volts [16, 37]. In contrast, for converters operating at 13.56 MHz, the dc-link voltage is limited to less than 50 V [9, 35]. For higher frequencies, there exists a current-mode class D inverter (CMCD) topology which overcomes the above-mentioned challenges [38]. However, the CMCD converter has to sustain higher switch voltages such as the other inverter types discussed below.

Furthermore, considering that the class DE inverter has two active devices, and that additional circuitry is needed for the high-side gate driver, the cost and complexity of class DE inverters can become higher than for other inverter classes.

Resonant tanks

In contrast to the other resonant inverter topologies, the class DE inverter does not consist of reactive elements other than the switch output capacitance and any added parallel capacitance. For this reason, the topology must be combined with a resonant tank. Within the field of wireless power transfer, there are substantial research efforts made on resonant tank structures combined with half-bridge or full-bridge inverters. An inherent characteristic of a loosely coupled transformer is large leakage inductance, which in turn is often included in the resonant design in an effort to increase system efficiency.

The four possible combinations of series and parallel compensated primary and secondary sides have been studied in many works [15], from which the series-series (SS) and series-parallel (SP) topologies are the most popular. For most wireless power transfer (WPT) systems or for converters with loosely coupled transformers, the SS compensation is often combined with a full-bridge rectifier at the output. Yet, a full-bridge rectifier is expected to give a significant loss contribution in a low-power application, and, hence, is an undesirable choice in this work [21, 36]. Other rectifier choices might have other requirements, e.g. source type, than the SS topology can provide. Consequently, other resonant tank structures must be considered. One course of action is to add more reactive components

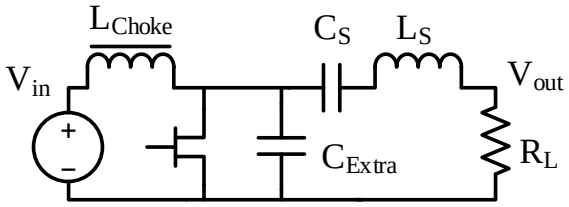

Figure 3.3: Schematic diagram of a class E inverter.

to the resonant tank to obtain more degrees of freedom in the converter design. The *LCC* and *LCL* topologies have also been studied for use in WPT applications [6, 8, 25]. Of the two, the *LCC* topology appears to be an attractive choice for high-frequency applications due to obtainable characteristics of soft-switching over a large load range and low sensitivity to change in rectifier reactance [27, 39]. Yet, due to the mutual dependency between the resonant tank and the rectifier behaviour, the choice of resonant tank must be made in conjunction with the relevant rectifier. The dependency originates from the required input source of the rectifier in addition to the need for an inductive load as seen from the inverter.

3.1.2 Class E inverter

The class E inverter is shown in Fig. 3.3 and consists of a single ground-referenced switch, one input choke inductor[2], and a series-tuned filter, C_S and L_S, connected towards the load, R_L. Owing to its soft-switching operation, it has been a popular topology for high-frequency dc-ac applications for several decades [17]. When operating at the optimum design point, the switch operates under ZVS and ZCS at turn-on (often noted as ZDS in the literature). As a result, it is able to deliver more power than other amplifier classes for the same input voltage [3]. Yet, this feature of the class E inverter comes with the drawback that the active switch is subject to a high voltage potential during operation, theoretically evaluated to approximately 3.6 times the input voltage (see V_{IN} in Fig. 3.3). Along with the high switch voltage, the class E inverter is also sensitive to load change due to the load resistance being a part of the dimensioning of the resonant tank. This means that small changes in load resistance, i.e. less than $\pm 25\%$, result in a loss of the soft-switching properties and the introduction of switching losses. The severity of the switching losses increases with the relative change in load resistance from the optimal value. At megahertz switching-frequency range, this greatly affects the converter efficiency.

[2]A choke inductor, or just choke, means that the inductance value is high so that the drawn current is largely a dc current.

There are several works that suggest possible remedies for the load sensitivity, three of which are mentioned here. The first approach is to include further design criteria, resulting in a new design method of the reactive components that leads to good load-independence performance at the price of higher maximum voltage and current amplitudes for the switch [2]. The second approach is to use additional components in the resonance tank so that the effect of load variation on soft-switching is avoided [33]. Similarly, the third possibility is to use the loosely coupled transformer in the design procedure, leading to a large operating area while the ZVS condition is upheld [4]. This is a highly relevant case for the application in question.

3.1.3 Class EF and Φ_2 inverter

The class EF inverter is shown in Fig. 3.4(a). It consists of the same components as the class E inverter plus an additional series-filter, C_P and L_P, placed in parallel with the switch. This additional filter is tuned at a multiple, n, of the operating frequency. The subscript n can be included in the inverter name to indicate this frequency, resulting in a naming convention for these inverters as *class EF*$_n$ [3]. Accordingly, this additional degree of freedom can be used to increase the inverter performance. In particular, converters with *n* equal to 2 or lower appear to give the highest power-output capability [2, 3]. Furthermore, the voltage stress of the switch can be lowered compared to the class E inverter. In the special case of $n = 2$, the second harmonic is highly damped and the EMI performance of the inverter output is improved [1]. Class EF inverters and rectifiers can be designed to be highly load-independent [2]. On the one hand, it is possible to design the class EF inverter to operate at approximately the same maximum frequency of class E inverters. On the other hand, this does not result in the global performance optimum. If a more preferential operating point for the class EF is chosen, the maximum operating frequency decreases below the class E. It has been demonstrated that the class EF converter can be more efficient than the class E counterpart, although this depends on two conditions; namely, that the input voltage has to be higher and that the active switch has to have a relatively high on-state resistance [3]. In the case of low on-state resistance of the active switch, the difference in efficiency between class E and class EF inverters is decreased.

The class Φ_2 inverter, shown in Fig. 3.4(b), is a special case of the class EF$_2$ inverter [3], where the input choke inductor is non-infinite and tuned to resonate with a part of the capacitance C_P [31, 32]. The result is an increase in the maximum operating frequency and lower voltage stress on the active switch. In the literature, this converter is often demonstrated operating at one of the ISM frequencies (6.78 MHz (2.2 kW) [7], 13.56 MHz (2.0 kW) [29], and 27.13 MHz (0.4 kW) [12]), but converters operating at even higher frequencies are also found

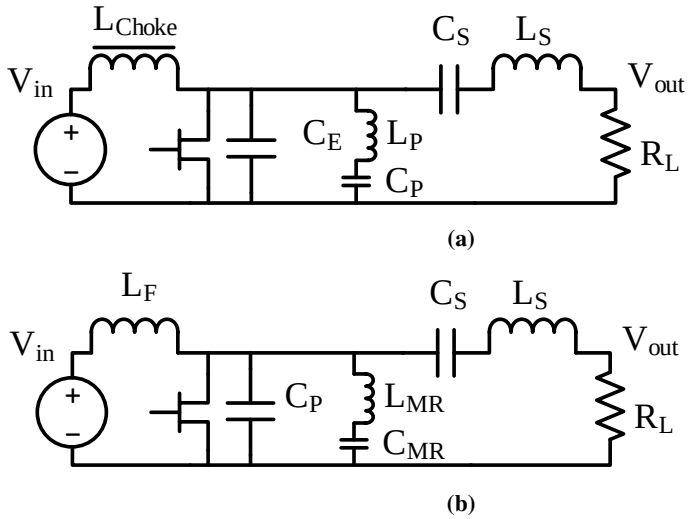

Figure 3.4: Schematic diagrams of a) the class EF and b) the class Φ_2 inverters. The biggest difference is that the Φ_2 inverter uses the input inductor as part of the impedance network. The naming convention of the Φ_2 inverter follows the initial publication [31].

(30.0 MHz (200 W) [32], 64 MHz (11 W) [11], and 85 MHz (10 W) [34]). Following the design guidelines for the inverter, the resulting switch voltage is approximately 2.3 times the input voltage, which is lower than for the class E inverter. Whereas following the original design method has the same sensitivity to load changes as for the classical class E inverter, the class Φ_2 inverter can also be designed to maintain ZVS for a large variation in load resistance [33].

For both class EF and class Φ_2 inverters, the main disadvantage is the added complexity in the added components and the required accuracy of tuning the resonance networks.

3.1.4 Comparison of inverter topologies

A comparison of the discussed inverter topologies is given in Table 3.1 with regards to voltage stress and component count. The maximum voltage stress the switch will have to sustain depends on the specific inverter topology if the input voltage is equal. Therefore, the availability of GaN devices and the magnitude of the maximum device voltage must be investigated. In summary, there is no technical limitation regarding the device availability. Single GaN devices are available from below 100 V and up to a maximum of 650 V. In contrast, half-bridge modules, are available up to a rated 100 V (e.g. from Texas Instruments and EPC). For the application in question, an input voltage of 48 V has been selected. Con-

Inverter	$\frac{V_{ds,max}}{V_{in}}$	no. of switches	no. of Ls / Cs	$\frac{R_{load}}{R_{opt}}$ range
Class DE (+LCC)	≈1	2	1 / 2	$0 \rightarrow \infty$
Class E	3.6	1*	2 / 2	$0.5 \rightarrow \infty$
Class EF	≤2.3	1*	3 / 3	$0 \rightarrow 2$
Class Φ_2	≈2.4	1*	3 / 3	$1 \rightarrow 10$

*ground referenced switch

Table 3.1: Comparison of switch voltage and power capability of suitable topologies for high-frequency converters.

sequently, a class DE inverter can be implemented using integrated half-bridge circuits. For the other inverter classes, the available single-switch devices have voltage ratings that allow for a safety margin despite a voltage stress of multiples of the input voltage. Furthermore, there is no identifiable cost difference that could tip the scale in any favour. Even though the class DE converter will need two active devices, it does not necessarily result in increased costs. The difference in cost between a half-bridge module and single switches, at the time of writing, is not large. An integrated half-bridge circuit is approximately $10, while a single 200 or 650 V switch with similar $R_{ds,on}$ are approximately $6 and $17, respectively. However, the price for a single-switch device is quoted excluding the gate driver, and it is not clear if different classes require the same rated on-state resistance to obtain similar efficiencies.

In addition to demonstrating high efficiency, the inverter should also handle a largely varying load. Typical for the application would be quiescent or minimum load when the dc-load is off and up to a maximum load. Most of the inverters discussed here are able to handle partial load variation with proper design, and a summary of the load variation capabilities is given in the last column of Table 3.1. Class DE with an LCC has been shown to handle large load variations [27]. Class E can be designed to handle load variation from 50% of optimal load resistance to open circuit load [2] and handle large variation when designed together with a loosely coupled transformer [4]. Class EF_2 has been demonstrated to handle load variation from short-circuit up to 200% of optimal load resistance [2]. The class Φ_2 inverter has also been demonstrated to handle large increases in load resistance [11, 33], although some solutions require additional components. In conclusion, all inverter types here have been demonstrated to handle load variations. In contrast to the others, the class EF inverter can handle short-circuit condition,

but not an increase in resistance towards open circuit. For a converter, resilience against short-circuit is a desirable trait, whereas, a low-load situation, modelled as high load resistance, is a more likely use case. The class EF inverter could still be chosen; however, an impedance inverter is required [18]. It must be mentioned that, at the time of the inverter investigation for the work in [**P5**], most of the literature on load-independent design for class E, EF, and Φ_2 inverters was not available.

In summary, neither cost nor load variation seem to substantially differentiate the discussed inverter types. Nevertheless, from Table 3.1, it is observed that the class DE inverter needs the lowest number of passive elements, and, hence, less tuning of resonance frequencies is required. Furthermore, the implementation is simplified since an integrated circuit (IC), containing the half-bridge circuit with drivers, is available in the voltage range of the application at the lowest ISM band of 6.78 MHz. However, the final choice of inverter has to be compatible with the rectifier circuit.

3.2 High-frequency resonant rectifiers

For all of the previously discussed inverter classes, an equivalent class resonant rectifier exists. Many of the characteristics of the inverters are present in the equivalent rectifier topology. In this section, class D/DE and class E rectifiers will be investigated in detail. Class EF and class Φ_2 rectifiers also exist. As for their inverter counterparts, they decrease the peak voltage stress of the diode by adding additional components. However, due to the low output voltage and the current diode technology, this feature is not of particular interest for the intended application. Hence, these two rectifiers are not discussed.

All rectifiers can be made into active rectifiers by exchanging the diode for an active switch, which could lower the conduction losses. However, this increases the design complexity. Therefore, for the low-power application, only diode rectifiers will be considered. Resonant rectifiers employing diodes can also be designed for low switching losses. Firstly, ZVS operation of diode rectifiers leads to lower losses and minimised EMI, since the diode capacitance energy is circulated in the circuit instead of being dissipated or radiated. Secondly, by decreasing di_d/dt at turn-off, reverse-recovery losses can be reduced.

3.2.1 Class DE rectifier

Class DE rectifiers, also referred to s class D rectifiers in the literature, consist of 2 or 4 diodes and exist in both current- and voltage-driven variations. Since the target application is low power, only solutions using two diodes will be discussed. Four topologies are shown in Fig. 3.5. In one half-period, power is transferred

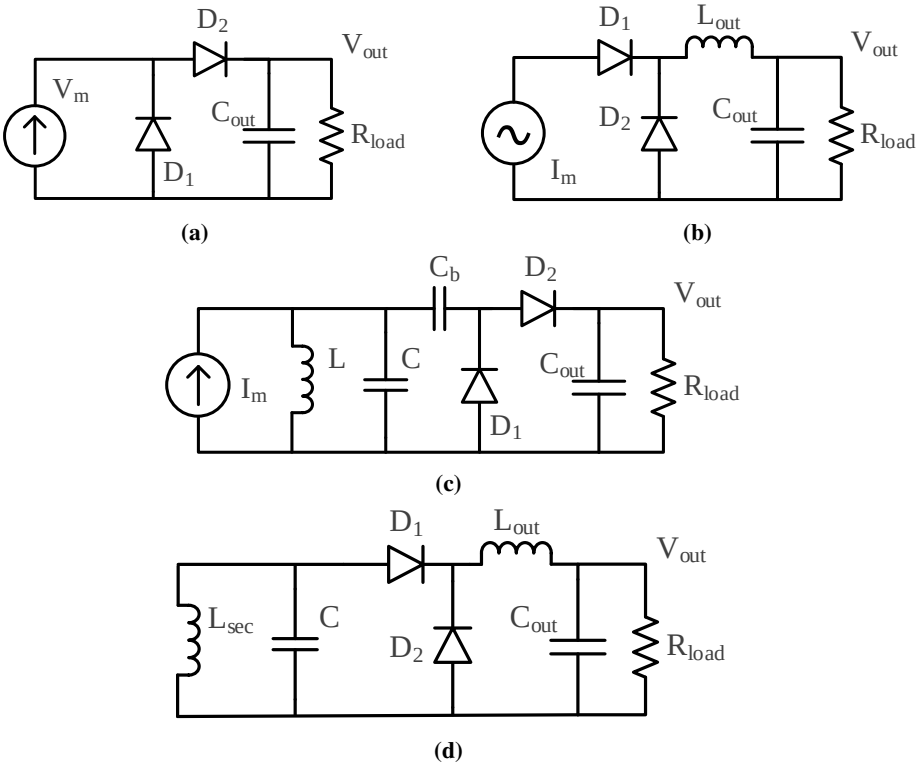

Figure 3.5: Schematic diagrams of three class DE rectifier topologies: a) current-driven rectifier, b) voltage-driven rectifier, c) current-driven with resonance tank, and d) voltage-driven with resonance tank. In d), the input source is included in the secondary side coil (L_{sec}) of the transformer.

to the output through one of the diodes, while the input current is freewheeled in the other diode during the second half-period. The current-driven rectifiers will have a voltage stress equal to the output voltage, while the voltage-driven rectifier will experience a current stress equal to the output current [26]. In addition to its simplicity, the input impedance of this class rectifier is mainly resistive if the diode impedance is small compared to the resonant tank capacitor [21].

Figure 3.5(a) shows the current-driven rectifier. The sinusoidal input source will be subjected to a square signal with a dc-component and amplitude equal to half of the output voltage. When the sinusoidal input-current changes polarity, the diode capacitances will be charged and discharged until the opposite diode is conducting [10]. No other components are needed in this topology. However, the performance was observed to be affected due to the inherent diode junction-capacitance in-

crease at lower output voltages. Hence, for high-frequency applications, it would be preferential with topologies that incorporate the diode capacitance in the resonance tank [21]. Figure 3.5(b) shows the voltage-driven counterpart, where the sinusoidal voltage source supplies a square wave current. The output dc-current is maintained by the output filter consisting of L_{out} and C_{out}. In contrast to most other class D converters, the voltage stress on the diodes in this topology will be higher than unity [26]. Moreover, this topology has an additional filter-inductor compared to the current-driven rectifier, thus making it less attractive.

However, these rectifier circuits must be combined with a suitable resonance tank at the input in the application converter. In this way, the diode capacitance can be incorporated in the discrete capacitance of the resonance tank. An example of the current-driven rectifier is seen in Fig. 3.5(c). The parallel resonance tank, L and C, is added between the input source and the rectifier. The two additional capacitors, C_b and C_{out}, are sufficiently large not to impact the operation at the switching frequency. Thus, the junction capacitance of the diodes can effectively be combined with the parallel capacitor, C, to form the resonance circuit [28]. The unity voltage stress on the diodes makes this topology highly relevant for high-voltage rectification [28]. However, it requires additional components since the transformer secondary side cannot directly be used as the resonance-tank inductor. In comparison, this is possible for the voltage-driven rectifier, as shown in Fig. 3.5(d). The secondary side of the loosely coupled transformer, L_{sec}, is used as the input source directly. Simultaneously, the diode capacitances can be incorporated into the resonance capacitor. Nonetheless, this topology also requires an additional inductor for the output filter.

3.2.2 Class E rectifier

Class E rectifiers are found in several configurations that have been extensively analysed several decades ago [17], mainly for resonant power converter applications. Their popularity has increased within the last decade primarily due to the development of WPT converters operating in the multi-megahertz range. Several class E rectifiers have been investigated for use in wireless power transfer operating at ISM band frequencies [20, 24]. Four classical variations of the class E low dv/dt rectifier plus one newer addition are shown in Fig. 3.6. The difference between the topologies is the arrangement of L, C, and the diode, as well as the required input source behaviour. Consequently, their performance changes in terms of input impedance, transfer function, and load variation behaviour [20]. Similar for all topology variants is that the voltage stress on the diode is 3.6 times the output voltage at resonance, just as for the class E inverter, which is a disadvantage of this topology. Similarly, the diode current stress will also be higher than the output current. Furthermore, the input reactance will change with load, which, in turn, is

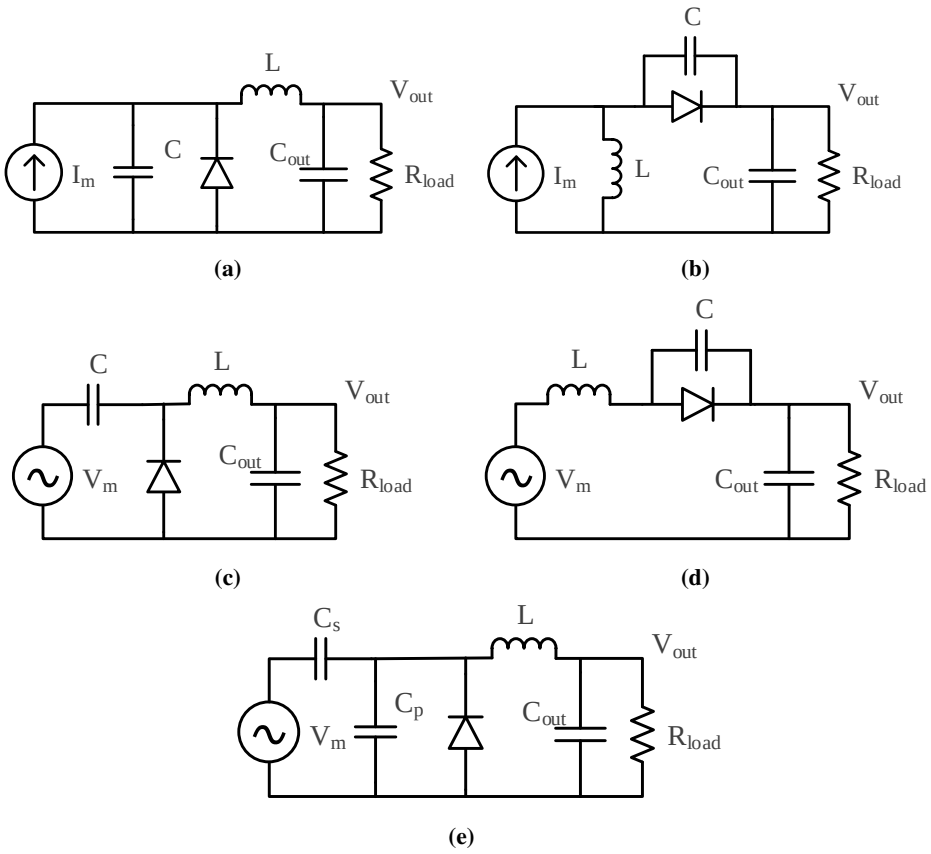

Figure 3.6: Overview of class E low dv/dt rectifier topologies. The junction capacitance of the diode is not shown explicitly.

a challenge for the design of the high-frequency converter.

Figure 3.6 shows five variations of the class E rectifier:

a) The current-driven, parallel-capacitor class E rectifier [20].

b) The current-driven, parallel-inductor class E rectifier [24].

c) The voltage-driven, series-capacitor class E rectifier [20].

d) The voltage-driven, series-inductor class E rectifier [17, 20].

e) The hybrid parallel-capacitor class E rectifier [20], which is an evolved version of c), where the input capacitor is split into two capacitors so that the diode junction capacitance could be incorporated into the resonance tank.

Topology	# diodes	# inductances	# capacitors**	$V_{d,max}/V_o$
Class D c	2	1	2	≈1
Class D d	2	1	2	>3 [26]
Class E a	1	1*	1	3.6
Class E b	1	1	1	3.6
Class E d	1	1 (0)	1	3.6
Class E e	1	1*	2	3.6

*Inductor to minimise current ripple in the output current.

**Output capacitor is not counted as it is required for all rectifiers.

Table 3.2: Component count for the presented resonant rectifier topologies.

Rectifiers **a** and **b** are current driven, meaning that they expect a sinusoidal current input. Similarly, rectifiers **c**, **d**, and **e** require a sinusoidal voltage input. All variations of the class E rectifier consist of a single diode. Furthermore, the diode is in parallel with a capacitor that effectively incorporates it in the resonance tank. Accordingly, they can be designed to have low switching losses. The disadvantage of the structure, as for the class E inverter, is that the diode will have to be dimensioned for higher voltage and current stress relative to the output voltage and current. For variation **c**, since the diode's junction capacitance is not included in the resonance circuit of the class E **c** rectifier, it is not considered any further.

3.2.3 Comparison and discussion of rectifier topologies

In regards to the evaluation of the inverters, the rectifiers will be compared based on diode voltage stress, component count, and load-variation behaviour. The quantifiable rectifier aspects are listed in Table 3.2.

To evaluate the consequence of the diode's maximum voltage stress in different topologies, a survey of the relevant diode technology is needed. The available technology choices for high-frequency rectifier diodes are Si Schottky diodes, SiC Schottky diodes and GaN HEMTs. None of these technologies exhibit reverse recovery losses. Although GaN HEMTs have many desirable characteristics, they are avoided in rectification due to the high reverse conduction losses. While Si Schottky diodes are limited to a rated blocking voltage of up 100 V, SiC Schottky diodes are currently available from 650 to 1700 V. Hence, the use of Si Schottky diodes is not feasible in all resonant rectifiers, even at low output voltages, due to the required voltage rating of the diode. For the parasitic capacitance, SiC

diodes should theoretically have lower capacitance for the same rating as the Si counterpart. However, due to the difference in ratings, the Si and SiC diodes have comparable capacitance values. Yet, whereas the Si Schottky diodes have lower forward voltage drop than SiC counterparts, the drawback of Si diodes is the high leakage current, in particular at elevated temperatures. As an example, the maximum leakage currents of a 100 V Si Schottky diode (B3100) and a 650 V SiC Schottky diode (STPSC4H065) are 20 mA@100 °C and 170 µA@150 °C, respectively, at the maximum blocking voltage. In summary, if Si Schottky diodes can be used then efficiency could potentially be increased. However, the difference in using a SiC Schottky diode is small, which would also give a substantial voltage margin to the design. The cost difference between the two technologies, with a current rating of 3 to 4 A, is approximately $0.5 versus $1.5 at the time of writing.

A small advantage of class E rectifiers is observed when comparing the component count shown in Table 3.2. Although each topology will need an inductor, inductors in variation **a** and **e** are part of the output filter and will see lower ac current peaks [20]. This can reduce magnetic losses if magnetic cores are used in the implementation. However, this might also entail that the inductance value should be high to ensure that the output current is approximately constant. Another element to consider is the inclusion of the transformer in the resonance tank of the rectifier. In particular, if the transformer inductance is made as a part of the rectifier, the implementation needs one less inductor. In this regard, there is an opportunity to integrate rectifier variation **d** (series-L class E rectifier) and the transformer. This aspect of the series-L class E rectifier is often misunderstood, namely that it is assumed that the series inductance must be implemented as a discrete inductor in addition to the inductance on the transformer secondary side [20]. As shown in [**P5**], the transformer secondary side can be used as both the voltage source input and the series-inductance on the rectifier side. Thus, the rectifier component count reduces to a diode and a capacitor. An additional advantage is that any stray inductance becomes a part of the series-inductor. Consequently, the rectifier solution does not need additional passive components and the anticipated power density is increased. A simplified efficiency evaluation between class DE and class E rectifiers was carried out in [30]. In summary, current-driven class DE shows higher efficiency at low loads while the series-L class E rectifier has higher efficiency at high loads. It is also pointed out that the lack of switching losses for class E rectifiers make them most suitable for high-frequency applications.

An additional interest in the use of class E rectifiers was raised from the observation of Kkelis et al. that "... *for a constant current in the receiving coil, both the hybrid and the current-driven rectifier achieve inherent output voltage regulation in the order of 3% and 8% of the nominal value, respectively, for a variable dc*

load range from 100% to 10%." [20, p. 8322]. The investigated class E rectifiers (Fig. 3.6(b) and 3.6(e)) exhibit inherent voltage regulation, a highly desirable feature for a power supply application, for A_r greater than 1.6. Since only two of five variations of the class E rectifier were investigated, selection of the other class E rectifiers would necessitate additional investigations on whether this property is present for similar design and operating conditions.

In conclusion, the literature overview presented in this chapter points out that both class DE and class E rectifiers can perform well at frequencies in the ISM band. However, there is no clear advantage for either topology in terms of cost and there is no apparent technical limitation. Yet, regarding the number of passive components, the series-L class E, shown in Fig. 3.6(d), has the lowest component count of all the compared topologies. Since this rectifier can use the self-inductance of the transformer secondary side, the power density is expected to be higher. Nonetheless, using class E rectifier imposes different challenges. In addition to the increased stress on the active component, the change in input reactance of class E rectifiers with load variation must be handled by the complete converter solution. Despite of this disadvantage, this topology is selected for further investigation for use in the intended application. Supplementary investigation of this topology was therefore carried out and is presented below.

3.3 Series-L class E rectifier

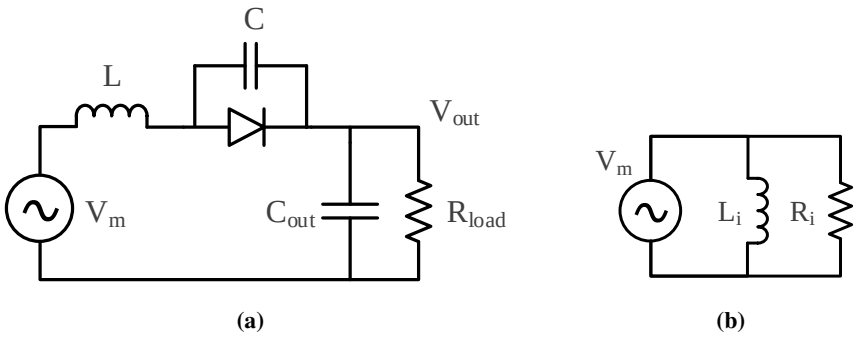

Figure 3.7: Schematic diagrams of a) the investigated rectifier for the application, and b) the equivalent diagram [17].

This section highlights the findings in [**P5**] regarding the rectifier topology and presents new information regarding the trade-offs present in the design space. The rectifier schematic is reiterated in Fig. 3.7(a) together with the equivalent model for the rectifier input impedance in Fig. 3.7(b).

Regarding the dimensioning of the series-L class E rectifier, an important obser-

vation was made in [20]. This rectifier type is stated to have inherent voltage regulation when designed with a resonance frequency higher than the operating frequency. From this statement, two advantages can be envisioned. Firstly, inherent voltage regulation is, in itself, a desired characteristic of a power supply, since this simplifies the converter design by operating in open loop. Secondly, designing for higher resonance frequency results in a decreased size of the passive components. In the literature, these aspects have not been investigated, most likely due to the abovementioned misunderstanding of the series-L class E rectifier. Using the transformer secondary as the rectifier inductor has been demonstrated in [23], although only the leakage inductance was used. Additionally, the rectifier was tuned to the operating frequency. Both of these aspects increase the required size of the transformer and the rectifier.

Based on the previous discussion, a knowledge gap exists regarding how this rectifier performs if dimensioned above resonance using the transformer secondary side as inductor. As has been shown in [**P5**], this solution is highly viable for power supply applications. For the analysis of the rectifier, the initial point is to define the relation between resonance and operating frequencies:

$$A_r = \frac{\omega_r}{\omega_0} \tag{3.1}$$

where A_r is defined as the ratio between the rectifier resonance frequency, ω_r and the operating frequency, ω_0 [20]. When A_r equals 1, the resonance frequency of the rectifier is equal to the operating frequency. Similarly, A_r increases when the rectifier is designed for a higher frequency and operation is below the resonance. For the investigations below, the range of A_r is focused on 1.5 to 2.0 since the dc-output behaves like a voltage source for $A_r > 1.5$. To dimension the passive components of the rectifier, the following equations are used:

$$L = \frac{R_{L,min}}{A_r \omega_0 Q} \tag{3.2}$$

$$C = \frac{1}{A_r^2 \omega_0^2 L} \tag{3.3}$$

where $R_{L,min}$ is the load resistance at maximum load, and Q is the loaded quality factor when the duty cycle of the diode equals 50% [17, 20], which constitutes the operating point with the highest power-output capability. In contrast, keeping L constant for varying A_r will not give any operational benefits outside of the resonance frequency [5]. In this work, the Q-value for 50% duty cycle has been found through SPICE simulations of the rectifier shown in Fig. 3.7(a) for the A_r range of interest. The resulting Q values are listed in Table 3.3.

A_r	1.0	1.1	1.2	1.3	1.4	1.5	1.6	1.7	1.8	1.9	2.0
Q	0.39	0.46	0.54	0.63	0.74	0.85	1.03	1.24	1.56	2.05	2.867

Table 3.3: Q values corresponding to a 50% duty cycle at nominal power with varying resonance frequency.

A previous work on this rectifier has used fundamental harmonic approximation (FHA) to obtain analytical expressions for the rectifier behaviour with variation in resonance frequency and load [20]. However, there are concerns about using FHA due to the existence of substantial current harmonics in the circuit when designing with a resonance frequency higher than the operating frequency. There are two primary contributions to the generation of harmonics. Firstly, as A_r increases towards two, any second harmonic current will be amplified due to the low impedance of the series-resonance. Secondly, the class E rectifiers are half-wave rectifiers, and thus generate second harmonic signals. For these reasons, numerical simulations are used in this work. In the simulations, the input source is modelled as an ideal voltage source, the passive components are lossless, and the diode is modelled as a resistor with R_{ON} =50 mΩ and R_{OFF}=10 MΩ. This way of modelling has two main effects. Firstly, with lossless components, the simulation results obtained are closer to the theoretical potential and the results become more general. Secondly, the lack of diode capacitance gathers all the capacitance in the parallel capacitance and disregards the diode's non-linear capacitance. This can affect the actual converter performance if the capacitance value is in the same order of magnitude as the diode capacitance, as discussed in Section 2.3.

A use case is investigated to show how the component values and rectifier performance changes with design frequency. At a rated load of 10 W, the minimum output voltage is set to 20 V, hence the minimum load resistance, $R_{L,min}$ equals 40 Ω. Using Eqs. 3.1, 3.2, and 3.3, the rectifier components are calculated for varying resonance frequencies. The resulting component values for the capacitor and inductor are shown in Fig. 3.8. It is observed that the inductance value drops by approximately an order of magnitude (from 2.41 µH to 0.164 µH) when increasing A_r from 1.0 to 2.0. Although the required capacitance increases, the effect on the implementation is softer since the converter density and losses are less affected by increasing capacitance. Moreover, the voltage gain, known as the voltage transfer function, M_V, greatly influences the converter design and is defined as:

$$M_V = \frac{V_{out}}{V_m} \tag{3.4}$$

The voltage gain describes the relation between the rectifier input source amp-

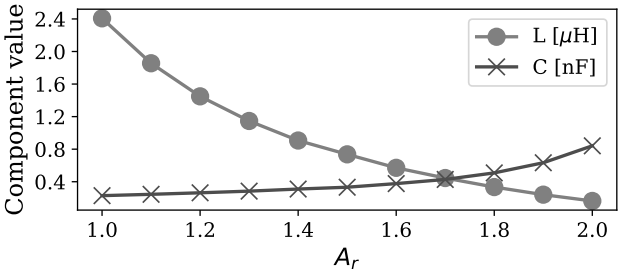

Figure 3.8: Passive component values for increasing design resonance frequency.

litude, V_m, and the rectified output voltage, V_{out} [20]. In the following step, the rectifier performance is investigated with a varying dc-load as A_r changes ($\mathrm{R_L}$ = 40 to 3000 Ω). The rectifier performance is evaluated in terms of the following parameters:

1. voltage transfer function, M_V, ref Eq. 3.4.
2. any variation in output voltage.
3. the relative magnitude of second harmonic of the current.
4. change in input reactance, L_i, ref Fig. 3.7(b).
5. peak current through the diode, $I_{d,max}$.
6. peak reverse voltage over the diode, $V_{d,min}$.

The input source modelled as $v_m = \hat{V}_m sin(\omega_0 t)$ and the amplitude is kept constant for all designs. The results of the investigation are shown in Fig. 3.9.

In Fig. 3.9(a) the voltage transfer function is shown. It is observed that A_r = 1.5 gives the highest voltage gain. Although not shown, all of the designs have higher voltage gain than design at resonance. For $A_r = 1.0$, the voltage gain, M_V, equals 0.2605 [14]). This value increases with A_r up to the peak at $A_r = 1.5$ and then decreases again. At $A_r = 2.0$, the voltage gain is around 0.83, which is approximately the same voltage gain as for $A_r = 1.4$. A higher voltage transfer function can initially be assumed to lead to higher efficiency in the discussed application, since the circulating current on the transformer primary side can be decreased. An additional observation in Fig. 3.9(a) is that the curve for $A_r = 1.5$ shows an increase in output power for the first steps in the load resistance before attaining the same shape as the other designs. This stems from the fact that the rectifier is changing

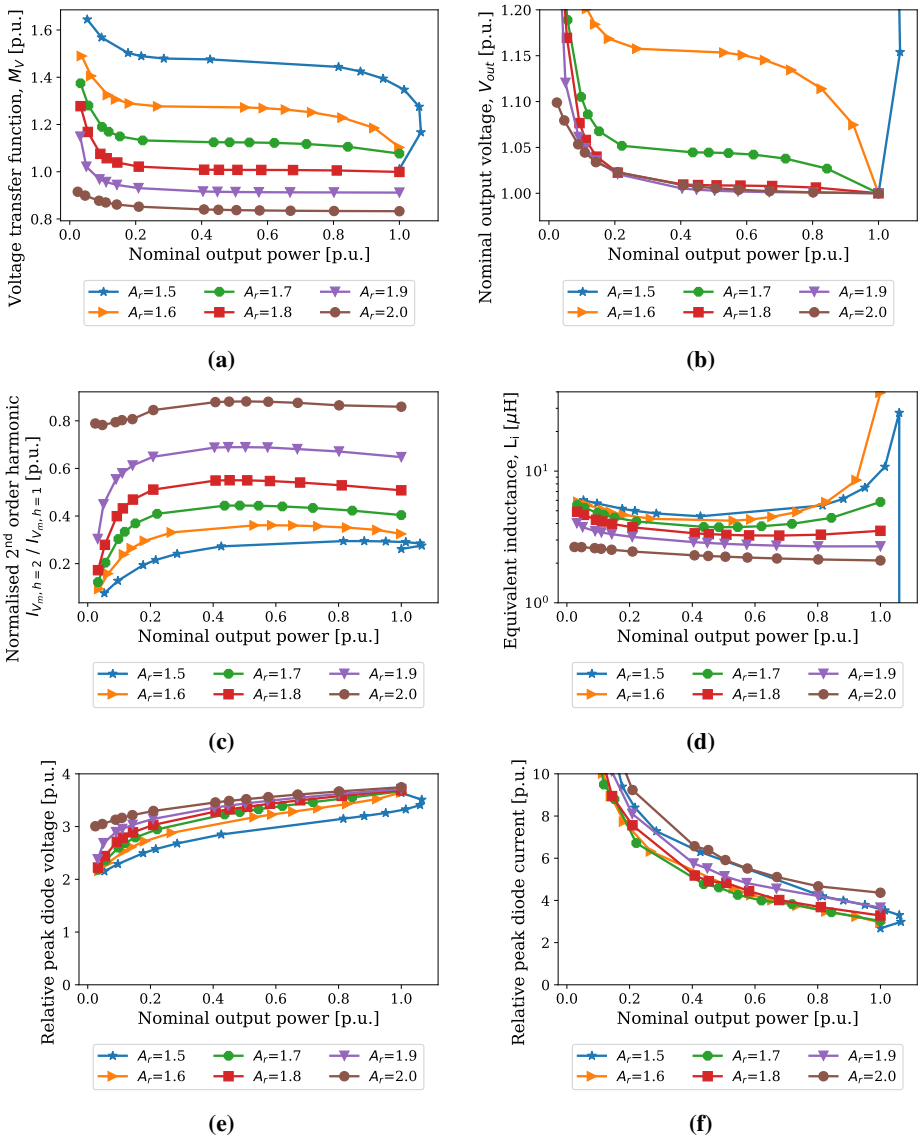

Figure 3.9: Results from SPICE simulations of the rectifier circuit assuming ideal components. The a) voltage transfer function [**P5**], b) output voltage variation [**P5**] and c) relative second harmonic in the current [**P5**] are plotted as a function of output power. d) peak voltage stress for the diode e) peak current stress for the diode and f) equivalent inductor seen from the input source as a function of output power.

from a constant current output to a constant voltage output. This source behavioural change is observed for all designs, although the inception points are different. In summary, if the rectifier is designed in accordance with the literature and for A_r equal or lower than 1.5, the rectifier output behaves like a constant current source with lower voltage gain. For the majority of applications, a constant output voltage is preferred. Hence, the voltage gain curve shows an improved design space above 1.5.

To investigate the change in output voltage with changing load, the input voltage is adjusted for all designs so that they have the same output voltage at nominal load (V_{out} = 1.0 p.u.). Then, the change in output voltage is observed as the load resistance increases. This is shown in Fig. 3.9(b). It is observed that for A_r equal or higher than 1.8, the output voltage changes less than 10% down to approximately 10% load, which is similar to the performance of commercial low power dc-dc converters operated in open loop. Hence, the design space for higher A_r is again more interesting for the power supply application.

Figure 3.9(c) shows the relative size of the second harmonic of the current, $\frac{I_{L,h=2}}{I_{L,h=1}}$. An increasing amplitude from approximately 20% and up to above 80% of the fundamental component is observed for increasing A_r. An increased second harmonic is expected since the peak gain of the resonance tank approaches the second harmonic and a half-wave rectifier inherently generates a second harmonic component. The conclusion is that the FHA method for resonant converters will lose accuracy for the design cases discussed here. This is an argument for using numerical methods instead, e.g. a SPICE-based design, as presented in the publication [**P5**].

In the following step, the magnitude and development of the input reactance are investigated. The input inductor, L_i is defined in the equivalent circuit of the rectifier, shown in Fig. 3.7(b). In a wireless power transfer converter, the reactance should be compensated by other passive components to limit the VA rating of the inverter. Using FFT, the fundamental components are extracted from the simulations and the equivalent input inductor, L_i, is plotted in Fig. 3.9(d). Similarly as for the output voltage, a smaller change in input reactance is observed for higher A_r. At the same time, the magnitude generally decreases over the whole load range which increases the source rms current. Thus a design trade-off emerges. On the one hand, increasing A_r to 1.8 or above leads to lower variation in the rectifier parameters, yet this comes at a price of a sub-maximum voltage gain and higher rms current. On the other hand, at medium A_r, the converter can likely obtain a higher peak efficiency but will exhibit larger output voltage variation and variation in input reactance over the operating range. This could be the preferred choice for

converters operating mostly at nominal load or, possibly, for cascaded converters where the following converter controls the output voltage.

As for other class E converters, the semiconductor device will have to sustain higher voltage and current stress compared to the output values. The relative stress is defined as:

$$\text{voltage stress} = \frac{|V_{d,min}|}{V_{out}} \tag{3.5}$$

$$\text{current stress} = \frac{I_{d,max}}{I_{out}} \tag{3.6}$$

where $I_{d,max}$ is the peak current, and $V_{d,min}$ is the peak blocking voltage, for the diode during one period. These values will influence the choice of the diode for the rectifier implementation and not the output values. Figures 3.9(e) and 3.9(f) show the voltage and current stress for varying resonance frequency. For increasing A_r, the voltage stress increases from 3.64 to 3.75 at nominal load, which is very close to the theoretical value for $A_r = 1.0$ of 3.6 [14]. However, in the same design range, the current stress is increased. For A_r from 1.5 to 2.0, the current stress increases from 2.68 to 4.36 compared to the theoretical value of 2.78 at $A_r = 1.0$ [14]. For all designs, the voltage stress decreases towards 2 as the load resistance increases. At the same time, the current stress increases towards infinity; however, the actual peak current decreases. Hence, only the current stress at nominal load is taken into account for dimensioning the rectifier diode.

In summary, the series-L class E rectifier shows promising characteristics for a power supply application when designed with a resonance frequency higher than the operating frequency. However, there clearly exists a design trade-off when approaching $A_r = 2.0$. Thus, the exact design should be evaluated simultaneously with the rest of the converter to find a global maximum. Additionally, the FHA should be avoided since there is considerable level of other harmonics present during operation.

3.4 Complete converter topology

Firstly, the presence of a loosely coupled transformer in the converter structure is necessitated by the application and the chosen design strategy for a high isolation-voltage transformer. For the choice of the complete converter topology, it has already been established that a resonant converter structure will be used due to the transformer and the high operation frequency. For the remainder of the converter, the discussion starts with the rectifier topology. As shown in the previous section, the series-L class E rectifier exhibits promising characteristics in terms of output voltage regulation, low component count and high expected power density.

Notably, the lack of discrete inductors is an advantage. Additionally, the topology consists of a single diode, hence lower losses are expected for the targeted low-power application.

For the choice of inverter side, the investigation of the series-L class E rectifier revealed that output voltage regulation was achieved for high A_r. However, the simulation was performed using an ideal voltage source as input. Although there are several ways of providing such an input, the choice fell on an LCC resonant tank, which was briefly discussed in Section 3.1.1. As described in [27], the LCC resonant tank can deliver an approximately constant current in the transformer primary side, while simultaneously handling some variation in reactance from the secondary side. These two characteristics are complementary to the need and behaviour of the rectifier. The constant primary side current gives a constant voltage source behaviour on the transformer secondary side in series with the self-inductance. Moreover, the switching current of the inverter can be tuned by resonant tank design, namely by changing the value of C_s. The rectifier has been shown to vary its input reactance with varying load, which is partly absorbed by the resonant tank. Therefore, the LCC resonant tank appears to be a promising candidate. This aspect of reactive power balance is important for the converter operation. If the reactive power requirement of the circuit is not met by the resonant tank, then the inverter will have to supply it. This has two negative consequences. Firstly, the active devices have to be dimensioned for higher current stress. Secondly, higher losses are expected due to high reverse conduction voltage drop of GaN HEMTs.

Although a full-bridge inverter was used in [27], the resonant tank can be combined with a half-bridge inverter since any dc-voltage will be blocked from the transformer by the capacitor C_s. A half-bridge inverter is suitable considering the available GaN HEMT devices and their voltage rating. In addition, using an integrated half-bridge solution allows for a small converter footprint. The complete converter structure is shown in Fig. 3.10. This combination of a class DE inverter and a class E rectifier has been previously identified in the literature, although without a loosely coupled transformer [19]. However, the resonance frequency is tuned to the operating frequency and frequency modulation must be implemented to regulate the output voltage with load variation. As such, the proposed solution will give a simpler converter structure with the operational benefit of inherent voltage regulation.

To demonstrate the benefits and challenges of the topology, simulation results with a simplified converter circuit are demonstrated. The simplified circuit is shown in Fig. 3.11(a). The inverter output is modelled as a trapezoidal voltage source with 50% duty cycle and 10 ns rise and fall times. Additionally, the rectifier is simplified to its reflected impedance in series with the primary side winding,

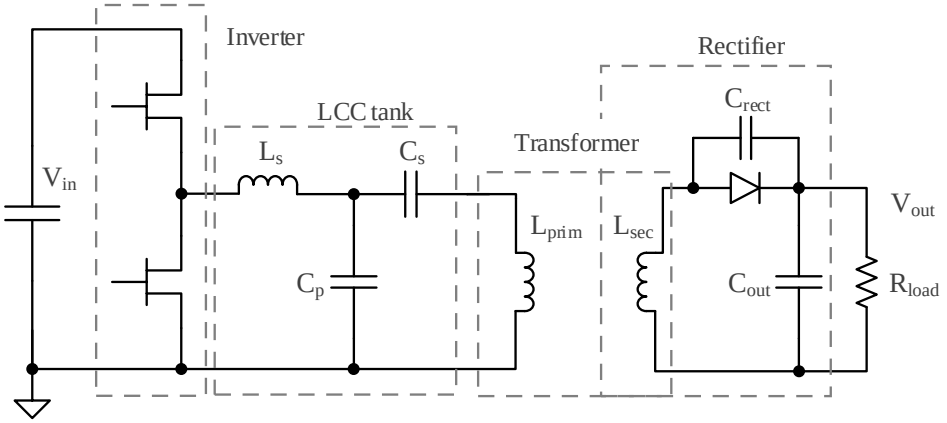

Figure 3.10: Schematic diagram of the complete converter structure: class DE inverter, LCC resonance tank, loosely coupled transformer and the series-L class E rectifier.

$Z_{load} = R_{load} + j\omega L_{load}$. For the remaining passive components, the component values were calculated according to the design method in [**P5**] with the dimensioning values stated in Table 3.4. To simulate a varying load, R_{load} is varied to obtain an output power range of 5 to 100 W. This range, and other values, are selected to produce characteristic waveforms for the topology. The waveforms are shown in Fig. 3.11(b). The half-bridge inverter gives a trapezoidal output due to the ZVS operation. If the load power increases, the in-phase part of the inverter current is observed to increase as well. Yet, regardless of the load, the current at the switching instant is approximately unchanged. This is true if the load reactance stays unchanged. Steady-state values for the circulating current and the instantaneous switching current are shown in Fig. 3.11(c). For varying load, the circulating current is observed to stay unchanged, as was derived in [**P5**]. The expression for the switching current is given as [**P5**]:

$$I_{inv,sw} = \frac{2V_{in}}{\pi Z_c}\left(\frac{L_{prim}}{L_s} - \frac{C_p}{C_s} + \frac{X_{load}}{Z_c} - \frac{\pi^2}{8}\right) \tag{3.7}$$

where $Z_c = \sqrt{\frac{L_s}{C_p}}$. Since the load resistor does not appear in the equation, the switching current should be unaffected by load variation. The instantaneous switching current is shown in Fig. 3.11(c) and is observed to stay approximately unchanged, although slightly lower than anticipated. However, the load reactance is present in Eq. (3.7). A linear increase and decrease in load reactance, from zero to 50 nH ($\pm 10\%$ L_{prim}), in correlation with the load resistance is also shown in

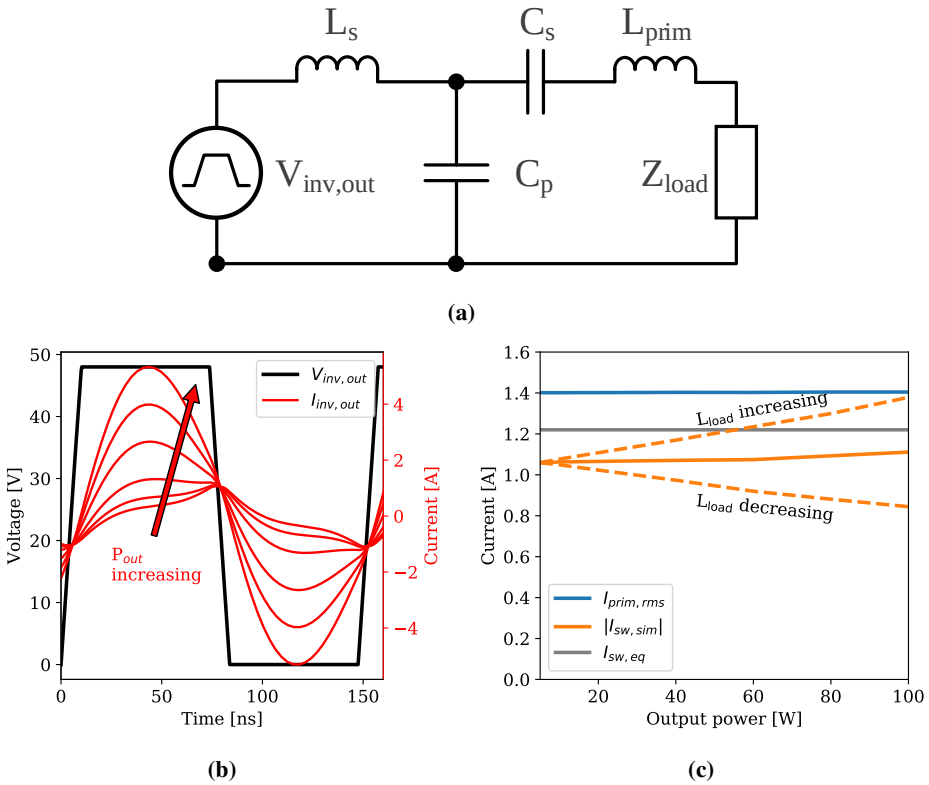

Figure 3.11: a) Schematic diagram of the simplified simulation circuit for investigating the inverter and LCC resonant tank. b) Time-domain waveforms of the inverter output voltage and current. c) Steady-state current values for the circulating current, I_{prim}, the instantaneous switching current derived from equations and simulated.

Fig. 3.11(c). From this observation, it is clear that any change in load reactance has to be handled by the inverter. This is handled by either dimensioning the dead-time in the operating point with the lowest switching current or by implementing an adaptive control scheme for the dead-time. Moreover, Eq. (3.7) shows that Z_c is an important factor for the relative change in switching current with changing L_{load}. On the one hand, high Z_c gives higher immunity, while on the other hand, it results in a lower circulating current. Therefore, low power and highly coupled circuits should be less prone to changes in load reactance. Nevertheless, the range in output power equals a change in load resistance from 5 to 50 Ω, which shows how this topology, in contrast to other class inverters, is insensitive to change in load resistance.

f_0	V_{in}	$\hat{\mathrm{I}}_{\mathrm{prim}}$	$\mathrm{C_s}$	$\mathrm{L_{prim}}$
6.78 MHz	48 V	2.0 A	2.0 nF	500 nH

Table 3.4: Values of the simplified circuit shown in Fig. 3.11(a).

3.5 Conclusion

In this chapter, resonant inverter and rectifier topologies have been investigated and compared. Resonant type topologies are selected due to their soft-switching property that leads to high performance at high operating frequencies. For the application in question, the available wide-bandgap devices are well within the expected resonant voltage levels, and hence, they do not pose strict limitations on the choice of topology or the implementation. Hence, more complex designs, i.e. class EF inverters and rectifiers, are avoided since they require more components.

From the discussion, the converter combination with the lowest component count and best suitability is found to be a class DE inverter with an LCC resonant tank and a series-L class E rectifier. The LCC resonance tank has been found to able to retain the soft-switching conditions for the inverter despite large variations in the load resistance, and some variation in the load reactance. Moreover, the series-L class E rectifier shows promising characteristics for a power supply application when designed with a resonance frequency higher than the operating frequency since inherent load regulation was observed (Fig. 3.9). Additionally, high power density can be achieved due to the merging of the rectifier and transformer secondary side coil. The remaining step is to combine the different topologies together and optimise the complete converter structure. In the following chapter, the converter structure is optimised within the scope of the targeted application. Chapter 5 investigates the details of the magnetic and dielectric properties of the high-voltage isolation, high-frequency transformer.

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Chapter 4

Auxiliary power supply with high isolation voltage

This chapter presents the optimisation of the identified circuit topology in the target application of an auxiliary power supply with high isolation voltage. Firstly, a more in-depth discussion of the application background is presented along with an overview of the existing literature. After introducing the optimisation algorithm, the optimisation results are discussed thoroughly to identify trends in the design space. Four prototypes were built and tested to verify the simulation and optimisation results. Additionally, the performance of one of these prototypes is fully demonstrated by supplying power to four commercial gate drivers as would be the case in an actual application. Finally, concluding remarks are made regarding the demonstrated performance and the challenges for the topology and the design process.

Contributions

The main novelty of this work lies in using GaN HEMTs to obtain a compact and coreless transformer design operating at multi-megahertz frequencies. This brings benefits for the system design, hence further developing the capabilities of auxiliary power supplies in terms of isolation voltage, compactness and efficiency. The content of this chapter summarises the work presented in [**P5**] and provides complementary information. For the published work, the contributions can be specified as following:

— Identifying and developing a suitable converter topology for a low-power auxiliary supply (previous chapter) that enables the increase in the solid in-

sulation thickness while keeping high efficiency and a small footprint.

— The holistic design becomes important as the coupling capacitance (transformer size) makes the transformer design and the converter design interdependent. This work demonstrates the feasibility of using a virtual prototyping tool for the design of the converter topology and using it to explore new design spaces. The experimental performance is demonstrated while supplying various types of loads, e.g. commercial gate drivers, sensors and control circuits.

— In this work, the class E rectifier is designed to be very compact compared to the state-of-the-art rectifiers presented in the literature. In the literature, a common misconception is that the series-inductor of the rectifier must be in series with the transformer as a discrete inductor. Alternatively, the literature does not exploit the benefits of designing the rectifier resonance above the operating frequency. In this work, both aspects are incorporated in the design process.

4.1 Background

The overview of the application that was first introduced in Chapter 1 is provided in Figure 4.1 . An auxiliary power supply supplies power to the gate drivers and auxiliary other loads in modules employed in medium-voltage modularised converters, or in switching valves consisting of series-connected switches in two-level converters (not shown here). These auxiliary power supplies must fulfil several criteria. Firstly, the power supply has to be able to **handle load variations** from 0 to 100 %, and similarly, the output voltage has to be within the allowed range for that same load variation. These criteria are common for all power supplies. Secondly, the **highest efficiency** possible should be sought. High efficiency leads to lower operating cost and lower cooling requirements. A consequence of the latter is increased power density. In addition, the insulation barrier naturally has to be able to **withstand the high voltage potential** between the primary and secondary sides. However, the auxiliary power supply has an additional design restriction related to the **EMI performance** of the system. The transformer is characterised by a parasitic capacitance between the two coils, $C_{coupling}$, that is shown in Fig. 4.1. This capacitance constitutes a path for noise currents. In particular, this noise current can be high during switching events in the medium-voltage converters due to the high dv/dt of the mid-nodes in the bridge modules. The capacitor current is defined as $i_c = C\frac{dv}{dt}$, and, as a result, a minimised $C_{coupling}$ gives higher system immunity to noise.

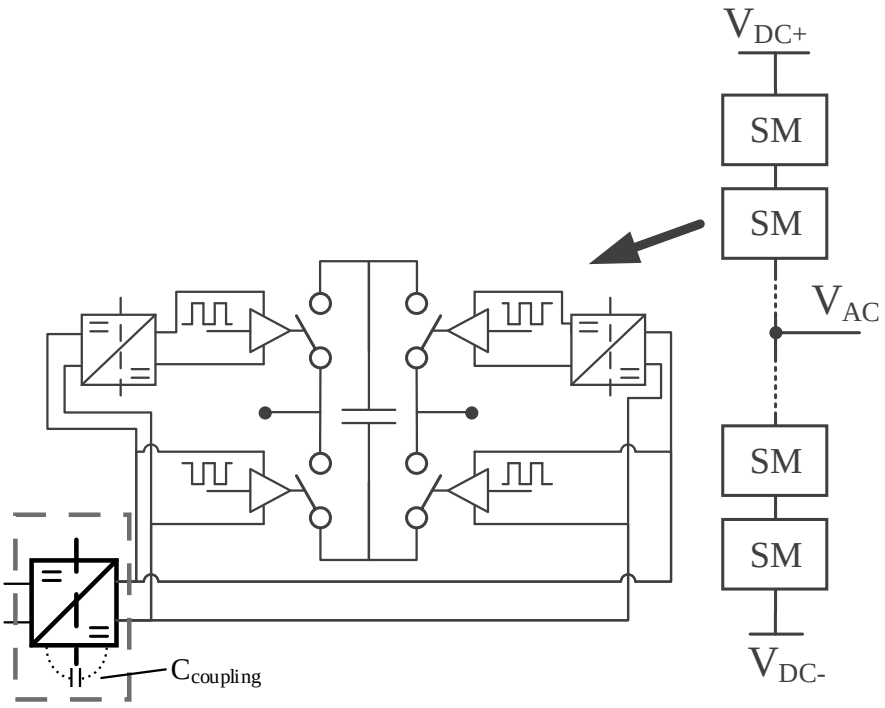


Figure 4.1: A simplified diagram of the target application for the auxiliary power supply (red box). Power is supplied to the gate drivers (and other loads) to one module in a medium-voltage, modularised converter.

Previous work on auxiliary power supplies for medium-voltage converters are reported in several publications. These publications are sorted in Table 4.1 according to whether the transformer is designed with a magnetic core [1, 2, 3, 7, 8, 9, 11, 13, 14], or if the design is coreless, either with [5, 10, 16, 20] or without a shielding ferrite [19, 17, 12]. For the coreless solutions, the publications are further sorted between planar or radial type transformer design. The power range is from 2 to 250 W, which covers the power requirement for a gate driver of a single IGBT or SiC MOSFET [2, 12, 14], and up to a full converter module [16, 19]. Common for most of the transformers for higher isolation voltages is a low coupling factor, usually due to the presence of a large air gap. In the field of wireless power transfer (WPT), loosely coupled transformer coils are an inherent feature. Since the distance between the coupled coils is large, the coupling factor of the transformer is low. Despite the low coupling factor, WPT systems can successfully transfer power at good efficiencies using resonance systems. Consequently, applying concepts from WPT to the auxiliary power supply can enable higher isolation voltages

while keeping high efficiency.

The transformer can be designed with air as the insulation material. This path has been explored in the literature (ref. [10, 12, 16, 17, 20] in Table 4.1). The drawback is that the size of the coils and the clearance between them have to be large. Hence, the power density of the implementation decreases, and the size of the auxiliary power supply can become larger than the driver circuit for low-power equipment [14]. The required clearance distance can be identified in IEC 60664-1 standard on insulation coordination for equipment connected to a low-voltage supply system. Due to the relatively small diameter of the transformer windings compared to the air gap of such a transformer, the electric field distribution is classified as *inhomogeneous*. This entails that the geometry has relatively sharp corners and field amplification is likely to occur in these areas. As a result, the required clearance between the primary and secondary side is increased. The clearance distance is plotted in Fig. 4.2.

As an alternative, potting or solid insulation can be used to establish the isolation barrier between the coupled coils. Examples from the literature and from this work are also indicated in Fig 4.2. In general, solid insulation and potting materials can sustain higher electrical fields without breakdown. Hence, the transformer solution becomes more compact, which increases the coupling factor and the power density. Figure 4.2 demonstrates how the clearance – and thus the density – is decreased when changing the insulation from air to solid insulation. It should be noted that the examples of transformers with solid insulation cannot be compared directly based only on the figure, since there are other criteria that are not accounted for, e.g. coupling capacitance, ease of manufacturing, and price.

In the literature, there is a small number of publications that employ solid insulation or potting in coreless transformer systems [12, 14, 15, 19] which have all been published in the last 2-4 years. [**P5**, **P6**] are the first publications to use

	Single load	Multiple loads	Planar	Radial
Core	[2, 11, 3, 14, 9]	[13, 1, 7, 8]		
Coreless	[20, 19, 16, 17, 12]	[10, 5]	[16, 10, 17, 12, 19, 5]	[20]

Table 4.1: Categorisation of literature concerning auxiliary power supplies for medium-voltage converters.

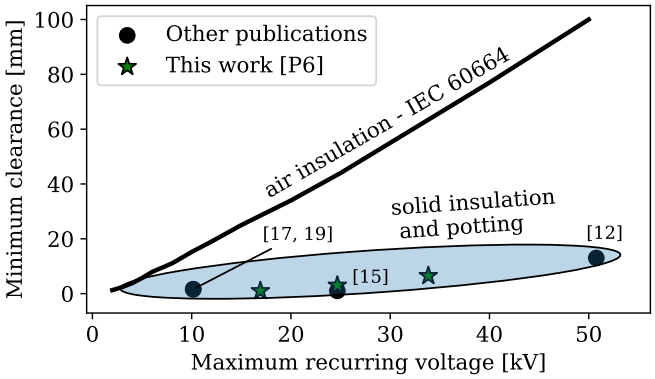


Figure 4.2: The required clearance between the primary and secondary side of the transformer using either air as insulation medium, or if solid insulation or potting materials are used.

GaN HEMTs in a solid insulation scheme. Furthermore, the operating frequency is also the highest reported for the application. [**P5**] shows the converter design aspects and is presented in this chapter. The details of the insulating properties of the loosely coupled transformer are covered in [**P4**, **P6**], and are presented in Chapter 5. The insulation concept of interest for this work was selected from Am et al. [2]. Here, the transformer air gap is filled with a non-magnetic insulation material. However, it is reported that any increase in air gap, which in turn increases the isolation voltage, substantially decreases the efficiency. Therefore, if the isolation voltage is to be increased, the circuit should be redesigned as to improve the efficiency.

4.2 Design aspects of the converter

The main drivers for the converter design start with the transformer. An equivalent circuit representation is shown in Fig. 4.3(a). The transformer is modelled by its self-inductances and the coupling between primary and secondary side. Additionally, the included parasitic elements are the transformer losses, modelled by an equivalent series resistance (ESR), and the coupling capacitance between the primary and secondary windings. In this work, the transformer is realised as a planar transformer type where each coil is constructed as spiral tracks on a PCB. Figure 4.3(b) shows the 2D cross-section with axial symmetry that represents this transformer geometry. In [**P5**], the degrees of freedom of the transformer are limited to track width, w_{cu}, inner radius to the first turn , r, and number of winding turns, N. This limitation was enforced due to practical considerations. In particular, the dielectric height and material were fixed to 1.5 mm FR4 so that the

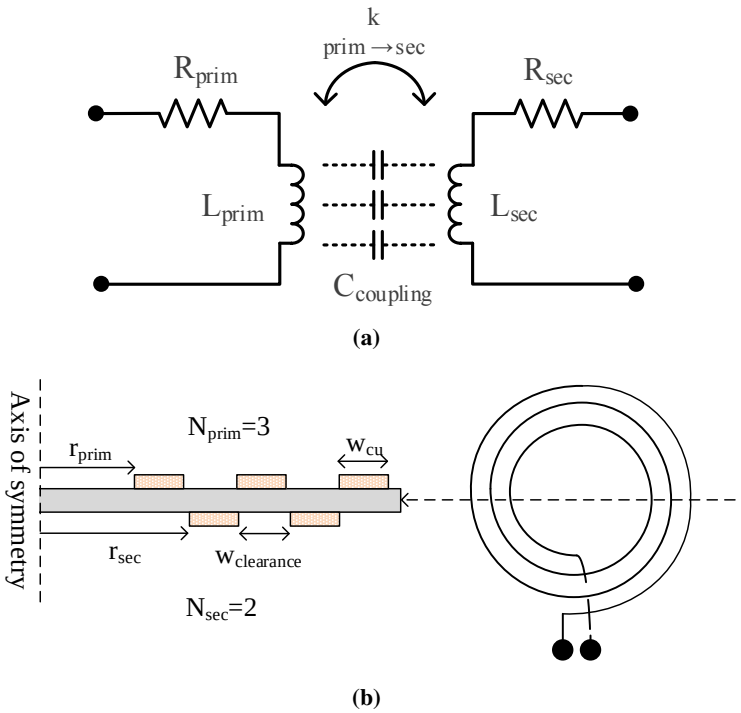


Figure 4.3: a) Schematic equivalent diagram of the isolation transformer [**P4**]. b) Illustration of the cross-section view of two spiral windings that make up the transformer primary and secondary sides [**P5**].

transformer primary and secondary windings could be produced on the same PCB. As a result, each winding is limited to a single layer. In [**P4**,**P6**], additional degrees of freedom are included such as dielectric height and number of turn layers. Additionally, the dielectric material was changed to Teflon to allow for higher withstand voltages and lower coupling capacitance. These aspects are covered in the following chapter.

As discussed in [4], the transformer efficiency is proportional to the relationship

$$\eta_{transformer} \propto k\sqrt{Q_{prim}Q_{sec}} \approx k\omega\frac{L}{R_L} \tag{4.1}$$

where k is the coupling factor, and Q_{prim} and Q_{sec} are the quality factors of the two coupled coils. If the two coils are identical, the quality factors are equal and the efficiency scales with the coupling factor, frequency, and self-inductance, $L = L_{prim} = L_{sec}$. In contrast, the efficiency inversely scales with the coil resistance, R_L. Furthermore, the parasitic capacitance, $C_{coupling}$ can be imagined as a plate

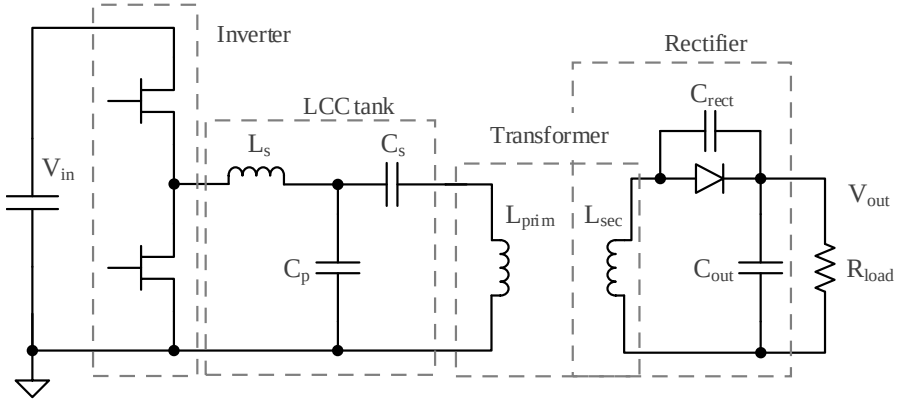


Figure 4.4: Schematic diagram of the converter topology.

capacitor, where the capacitance scales with area and inversely scales with distance between plates. Consequently, the coil area should be minimised and the distance increased. However, this negatively affects coupling factor and the $\frac{L}{R_L}$ ratio and, as a result, the efficiency decreases. In conclusion, the transformer design constitutes an optimisation problem.

On investigation of Eq. 4.1, it is observed that the transformer efficiency increases with frequency, ω. This is due to the lack of magnetic material which in turn eliminates the core losses. Yet, the transformer winding losses increase with frequency due to the skin effect which increases R_L. However, the increase in R_L with frequency is slower than ω and higher transformer efficiency is achieved at higher frequency. Together with lower passive component values at higher frequency, this forms the background for choosing the target operating frequency of 6.78 MHz. An additional benefit of operating at an ISM band is that the EMI requirements for the converter are lower as emissions in these bands are allowed. This is an important aspect since the lack of a magnetic core in the transformer might result in emissions that otherwise would not be tolerated. At the same time, many loss factors of the GaN HEMT are frequency dependent, as discussed in Chapter 2. Consequently, the frequency should be limited due to inverter losses. Hence, the lowest of the ISM frequency bands, i.e. 6.78 MHz, was chosen as operating frequency.

4.2.1 Output voltage regulation

The high operating frequency and the high isolation voltage barrier impose challenges in designing a closed loop control of the converter, which is, hence, avoided. Rather, the power supply is operated in open loop and should feature inherent out-

put voltage regulation. This was found to be reported for a class E rectifier which was covered in the previous chapter. Furthermore, a promising converter topology was identified that could incorporate this rectifier and its characteristics. Minimising the variation in output voltage with varying load was not included in the optimisation process. The main reason was that adding simulation steps to map the converter behaviour for several load resistances would require considerably longer simulation times. The optimisation algorithm should have as few steps as possible as part of the evaluation to ensure sufficiently short run times. In addition, it can be risky to add limitations to the optimisation problems, since limitations can introduce unintended effects on the result. Rather, the optimisation was assessed against design and operating constraints. Consequentially, load variation was investigated after the optimisation step.

The auxiliary power supply has to ensure that the output voltage is within the required output voltage variation constraint. A common dc-bus voltage of 48 V as input was selected. The output voltage was targeted to be between 20 to 25 V at nominal load. Hence, the voltage gain of the converter must be tuned accordingly. Since the voltage usually decreases with load, the output voltage was specified at maximum load. Traditionally, the voltage gain of a converter is tuned by changing the winding numbers of the transformer. In resonant converters, the input-to-output gain is a function of several converter parameters. For the converter topology in question (Fig. 4.4), the voltage gain can be defined as:

$$G_{dc-dc} = G_{inv} \cdot G_{lcc} \cdot G_{transformer} \cdot G_{rect} \tag{4.2}$$

hence, the total converter gain is the product of the inverter gain, G_{inv}, resonant tank gain, G_{lcc}, transformer gain, $G_{transformer}$, and the rectifier gain, G_{rect}. Resonant converter topologies are often investigated analytically using FHA. Here, only the fundamental frequency is investigated, which enables the simplification of the circuit to a single lumped parameter model. Most of these gains can be approximated using FHA. However, there are challenges in using analytical expressions. Firstly, they assume that only the fundamental component is present in the system, which is true only if the resonance circuit is tuned close to the operating frequency. Secondly, the rectifier and resonant tank gains change with the rectifier load. As for any complex system, highly optimising one part of the system can negatively affect another part. Therefore, it is of great interest to solve the optimisation problem holistically.

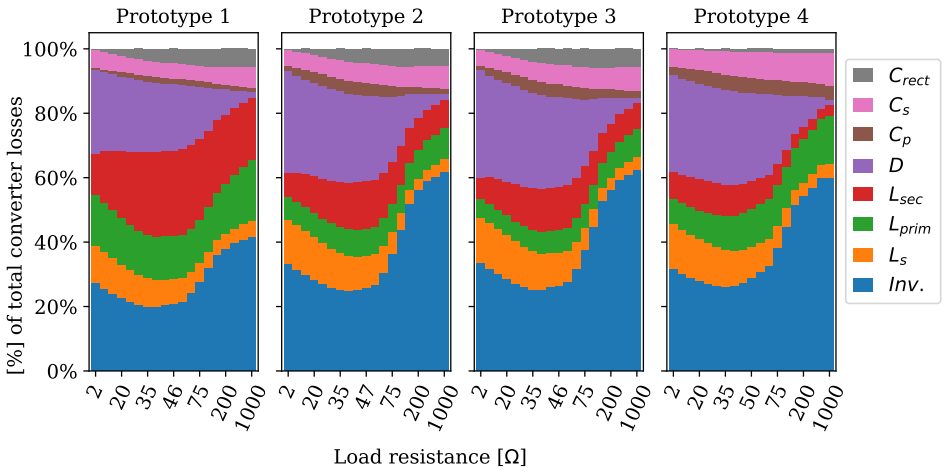


Figure 4.5: Simulated loss distribution of different converter components over a large variation in load for the four prototypes that were presented in [**P5**].

4.2.2 Efficiency

When operating at multi-megahertz frequencies, the inverter and the rectifier should exhibit soft-switching to allow for much higher efficiencies. This is an important criterion for choosing resonant converter topologies. Yet, as discussed in Chapter 2, there are additional loss factors for GaN HEMTs operating at high frequency. While dynamic on-state resistance was established knowledge at the time the work was started, the hysteresis effect of the output capacitance of GaN HEMTs had not been investigated thoroughly. Therefore, this relatively large loss factor of the inverter, despite soft-switching, was not expected. For near-future high-frequency applications considering GaN HEMTs, an additional design step for choosing the GaN device is advised. Since the hysteresis losses are decreased with chip area, it is likely that a smaller chip with slightly higher conduction losses will give lower total losses [21]. A particular aspect of the experimental results is that the chosen inverter is an integrated half-bridge module (TI LMG5200). On the one hand, integrated solutions decrease the device footprint which allows for high power density. On the other hand, the internal structure is unavailable and optimisation of the power circuit is not possible. It should also be noted that the IC was operated outside the frequency range given in the datasheet for which the device is characterised (f_{sw} = 6.78 MHz > 5 MHz). Other loss factors concerning the converter structure can be summarised into equivalent series resistances of the passive components.

To demonstrate an example of the relative contribution of each loss factor, the rel-

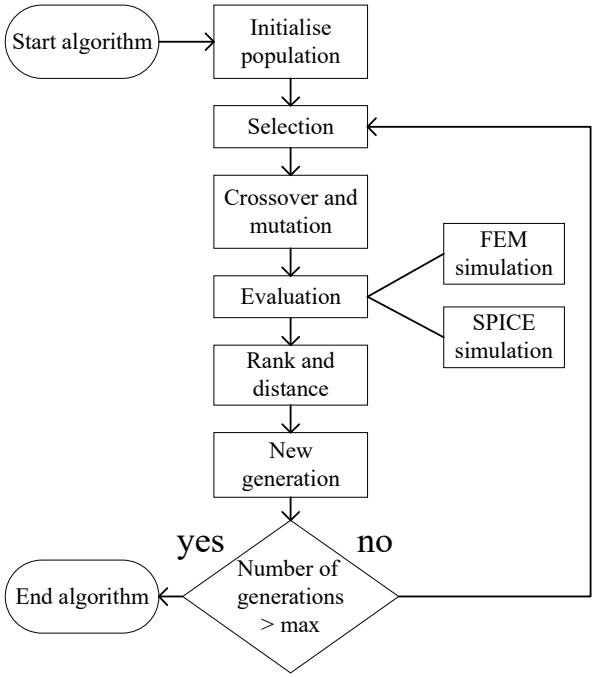


Figure 4.6: Flow chart for the genetic algorithm [**P5**].

ative loss distribution, found in simulation, of the four prototypes presented in [**P5**] is shown in Fig. 4.5. These four prototypes are further discussed in Section 4.4. The figure shows the development in the relative size of loss components over a large load variation (2 to 1000 Ω). The dominant loss factors are observed to be the inverter, the diode, the inductive components (L_s, L_{prim}, and L_{sec}) and the series capacitor, C_s. One important difference between the four prototypes is the copper cross-section of the transformer windings, with increasing cross-section area from prototypes 1 to 3. Prototypes 3 and 4 have approximately the same cross-section area. Subsequently, the relative loss of the transformer (red and green) is observed to decrease with increasing cross-section.

4.3 Optimisation of the converter

In [**P5**], design equations for the converter topology were developed for operation at the resonance frequency of the rectifier. Yet, it is hypothesised that the desired converter behaviour lies outside the validity of these equations. As such, an accurate model of the converter for a larger operating area is required. For this purpose, SPICE modelling of the circuit was developed. Since there is a lack of general

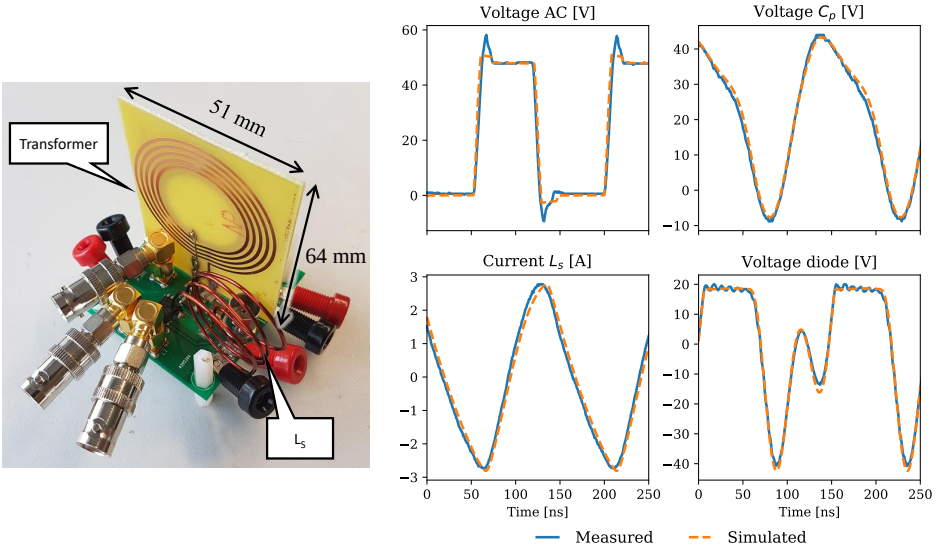
design equations for the converter topology outside resonance, the dimensioning of the passive components should be set through the optimisation problem. By allowing each passive component to be set individually, the optimisation algorithm is unrestricted in exploring the trade-offs within the transformer design, converter efficiency, and the resonance frequency. In summary, the optimisation algorithm must find the transformer geometry and passive component values that ensure the desired output voltage and simultaneously operate at high efficiency with the smallest possible transformer size.

A genetic algorithm was selected to perform the optimisation of the converter. In particular, the NSGA-II algorithm[1] was selected due to its suitability to the multi-objective optimisation problem [6]. A flow chart for the steps in the algorithm is shown in Fig. 4.6. For the evaluation of each individual, the lumped electrical parameters of the transformer are extracted using a finite element analysis software[2]. Hence, the transformer self-inductance, mutual inductance and the estimated series equivalent resistance of the transformer coils are taken into account by the optimisation algorithm through finite element analysis of the transformer cross section. The series resistance of the discrete inductor in the *LCC* circuit is not optimised and is left for future work. To include the copper losses of this inductor, the quality factor of the coil was set to 150. Moreover, the capacitor selection was limited to a single widely available technology (C0G material category) and simplified resistance modelling was implemented (R_{EST}=100 mΩ). Alternative capacitor technology has the potential to further decrease the converter losses and improve the efficiency. For the semiconductor components, dedicated SPICE models were used to model the losses.

In the following step, a SPICE simulation is run with all component parameters to find the steady-state converter efficiency. A first attempt at verifying the converter performance experimentally was conducted by constructing an initial prototype [**P5**], which is shown in Fig. 4.7(a). Figure 4.7(b) shows a comparison in time-domain between four measured and simulated signals. Naturally, only one operating point of the converter is shown, but the comparison for other operating points is similar. A good correlation is observed between the signals. Thus, the SPICE simulation model is largely validated. Yet, some discrepancies are also seen. Of these, the most notable is the difference in the reverse voltage drop during the freewheeling period, where the measured peak is twice as high, but only for a short period. Nevertheless, some additional losses are usually expected compared to a simulation model, and the model is thus used further. A production process was also established for accurately reproducing the transformer coils based on the

[1] **N**on-dominated **s**orting **g**enetic **a**lgorithm.

[2] *FEMM* - Finite Element Method Magnetics. A free software available on www.femm.info.



(a) (b)

Figure 4.7: a) Photo of the initial prototype. The green PCB is populated with the converter components [**P5**]. b) Time domain comparison for the inverter output (top left), LCC voltage (top right), current in L_s (bottom left), and the voltage on the transformer secondary side (bottom right).

simulated geometry. Consequentially, converter simulation results are representative for the expected experimental performance, although with some additional losses, e.g. small simulation discrepancies and higher inverter losses due to the additional loss factors covered in Chapter 2 [**P5**].

4.3.1 Genetic algorithm

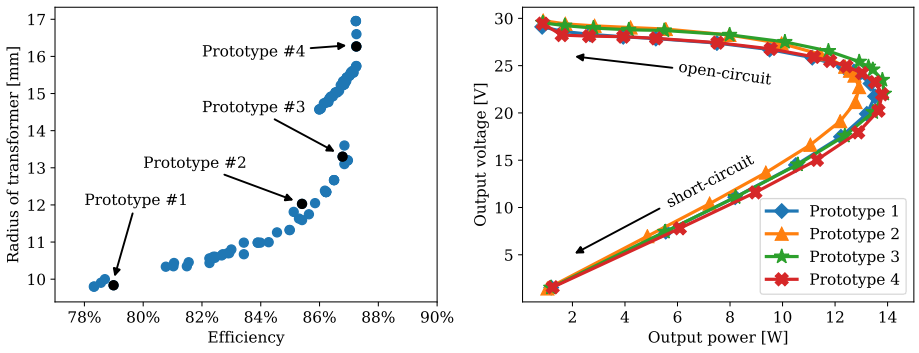
The genetic algorithm is one of several evolutionary optimisation algorithms that mimics a behaviour or structure that is found in nature. The evolution of populations can be described as the passing of genes from parents onto children, and the fitness of the new individuals to their surroundings impacts their chance to pass on their own genes. This process is most known through Charles Darwin's theory of evolution. As such, the genetic algorithm recreates this process by encoding the variables of the optimisation problem into genes. The genes from a pair of parents are recombined ('crossover' in Fig. 4.6) to a new individual, i.e. a child. Additionally, random mutation of genes, as is present in nature, are incorporated ('mutation' in Fig. 4.6). Different parents are selected to make children until a new generation is made ('selection' in Fig. 4.6). Each individual is evaluated through

a fitness function ('evaluation' in Fig. 4.6), and the fittest individuals are allowed to pass on their genes to the next generation. This follows the common expression from evolutionary theory of *survival of the fittest*. Genetic algorithms can be applied to many practical problems and give viable solutions in shorter time frames compared to evaluating all possible combinations of values for all design variables. Furthermore, genetic algorithms can simultaneously handle optimisation of multiple variables and variable types with multiple fitness functions [6]. The critique of genetic algorithms, and heuristic algorithms in general, is that the global optimum solution is not guaranteed. Yet, using alternative optimisation algorithms on analytical expressions may give a false optimal, as the underlying expressions are derived using assumptions, approximations and simplifications.

For the converter structure, there are many degrees of freedom, and the rectifier is highly non-linear. Hence, using SPICE simulations to evaluate the circuit performance is considered to give good precision, assuming that the device models are sufficiently accurate. In particular since the capacitance values of the converter were expected to be in the same order of magnitude as the device capacitances. Furthermore, due to the low calculation cost of the finite element analysis (FEA) for the simplified transformer geometry, both SPICE and FEA simulations can be combined with a genetic algorithm to explore the design space. By combining the evaluation of different converter aspects in this fashion, a holistically optimised converter structure can be obtained. The genome of the genetic algorithm contains the converter passive component values and the transformer geometrical parameters. Moreover, two fitness functions were defined for the genetic algorithm. Firstly, the efficiency of the dc-dc converter is maximised. Secondly, the transformer radius, and hence size, should be minimised. For the latter function, this objective has two effects. The most obvious effect is that the algorithm will seek to uphold converter density by decreasing the transformer size. However, the additional effect of smaller transformer radius is that the coupling capacitance between the primary and secondary sides also decreases. In [**P5**], the transformer geometry has a fixed distance between the primary and secondary windings. Additionally, the windings are limited to a single layer. Therefore, the transformer size becomes proportional to the coupling capacitance. Thus, minimising the transformer size allows for minimisation of the coupling capacitance without having to explicitly calculate it. More degrees of freedom for the transformer design are investigated in [**P4**,**P6**].

4.3.2 Simulation results

In [**P5**], a population of 100 individuals was randomly initialised, and the algorithm evolved over 125 generations. The last generation is shown in Fig. 4.8(a), demonstrating the identified Pareto front in the design trade-off between efficiency



(a) **(b)**

Figure 4.8: a) The last generation of the genetic algorithm showing the cross-section where efficiency and transformer size becomes a trade-off [**P5**]. The realised prototypes are marked explicitly. b) The relationship between output power and output voltage for the four individuals selected for prototyping. The load resistance goes from 2 to 1000 Ω, which replicates the range of short-circuit to open circuit condition.

and transformer size. From this last generation, four individuals were chosen for prototyping and experimental validation. The characteristics of the four individuals and the population average are given in Table 4.2. These characteristics are winding number, relative frequency of the series resonance, $\omega_1 = \frac{1}{2\pi\sqrt{L_s C_p}}$, the relative frequency of the rectifier resonance, $\omega_{sec} = \frac{1}{2\pi\sqrt{L_{sec} C_{rect}}}$, and the transformer coupling factor, k.

The four individuals are listed in order of increasing converter efficiency and size. It is observed from Table 4.2 that the efficiency follows the size and the coupling factor of the transformer. The size increase from prototypes 1 to 3 is due to increasing track width. While the track widths of prototypes 3 and 4 are similar, the higher inner radius of prototype 4 increases the size and the coupling factor. These aspects result in increased transformer efficiency. Furthermore, the coupling capacitance also increases with the transformer size. For all individuals, the winding number was identical at four turns for both primary and secondary turns. The equal turn number for the two sides is an expected result since the coupling factor is maximised when the two coils are of equal size [18] which positively affects the transformer efficiency (Eq. 4.1).

Since the optimisation algorithm is left to run without design restrictions, it is able to explore design spaces that are unbiased by common design conceptions. A design restriction would be to use a design equation, e.g. when L is set, calculate

	Winding number	$\frac{\omega_1}{\omega_0}$	$\frac{\omega_{sec}}{\omega_0} = A_r$	k	η_{dc-dc}
Average	4:4	1.07	1.54	0.64	85.3%
Prototype #1		1.28	1.27	0.57	79.0%
Prototype #2		1.02	1.34	0.64	85.4%
Prototype #3		1.01	1.34	0.68	86.8%
Prototype #4		1.00	2.04	0.71	87.3%

Table 4.2: Selection of design characteristics from the average of the whole generation and the prototype individuals.

C to obtain a given resonance frequency. The lack of such a design restriction has an inherent safety feature regarding the optimised result. If the common design rules are in fact the optimal solution, the algorithm should end up in that design space area. However, if it is not a good design rule, the algorithm can find a design area that increases the performance as defined by the fitness functions. Looking to the optimisation results, the average series-resonance frequency, ω_1, is found to be 1.07 which is close to the operating frequency for all devices. This is in line with the analytical design approach. In contrast, the relative rectifier resonance frequency in Table 4.2, ω_{sec}, indicates that a rectifier design at resonance frequency is less favourable [**P5**]. This was also hypothesised from the investigation of the rectifier as presented in the previous chapter. The average relative frequency of A_r =1.54 is approximately equal to the design point with the highest voltage gain found in the same investigation. Prototypes 1–3 have similar rectifier resonance frequency while prototype #4 has a resonance frequency of approximately twice the operating frequency. The relationship between output power and output voltage is plotted for the four individuals in Fig. 4.8(b). Interestingly, from the resonance frequencies of prototypes 1–3, a current source output would be expected. Yet, a constant output voltage characteristic is observed. This indicates a limitation in converter investigations with ideal input sources and the use of FHA. Rather, it is important to investigate the full converter structure, preferably including harmonics.

4.4 Experimental results

Prototypes of the four individuals were constructed to validate the simulated behaviour to the experimental performance. For each component, the component value was measured and compared with the value found by the optimisation algorithm. Both the measured value and the error are shown in Table 4.3, where the compon-

	Experimental value (error %)							
Prototype	#1		#2		#3		#4	
L_s [nH]	468	(1%)	501	(1%)	502	(2%)	469	(2%)
L_{prim} [nH]	395	(3%)	392	(5%)	388	(6%)	561	(4%)
L_{sec} [nH]	395	(4%)	380	(6%)	377	(6%)	573	(5%)
coupling	0.57	(1%)	0.64	(-1%)	0.68	(<1%)	0.71	(-1%)
C_p [pF]	724	(<1%)	1036	(<1%)	1075	(4%)	1170	(3%)
C_s [pF]	1347	(<1%)	1379	(-1%)	1376	(-1%)	1199	(-1%)
C_{rect} [pF]	859	(2%)	808	(<1%)	813	(1%)	232	(-1%)
$C_{coupling}$ (sim / exp) [pF]	4.5 / 7.6		8.1 / 11.8		10.7 / 14.8		13.8 / 18.3	

Table 4.3: Comparison of component values between simulation and the experimental setup [**P5**].

ent name refers to the schematic diagram of the converter shown in Fig. 4.4. Since the capacitors were chosen based on their measured value, they have small deviations from the simulated values. The transformer inductance shows the largest offset up to 6%. In contrast, the coupling factors have very small errors.

Moreover, the static characteristics of the converters were investigated. The output load was varied by changing the load resistor and the resulting change in output voltage, output current and efficiency can be seen in Figs. 4.9(a) and 4.9(b). A significant difference in efficiency is observed, where the experimental versus simulated efficiencies at full load for prototypes 1–4 are 71.0/79.0%, 79.3/85.4%, 80.3/86.8%, and 81.0/87.3%. This difference in efficiency is partly ascribed to the additional losses in the GaN half-bridge. Comparing the simulated losses to the experimental losses shows an underestimation, as shown in Fig. 4.10. As discussed earlier, part of this gap between measured and simulated losses is due to the hysteresis losses. These are added as a constant factor of 0.42 W in the simulation. However, the gap from simulation up to the measured losses is higher than this. Another loss aspect of the inverter that was observed to be different was the reverse conduction losses. The reverse conduction voltage drop was observed to be both higher in amplitude and longer in duration than in simulation, hence increasing the losses. However, other effects, such as dynamic on-state resistance, have not been quantified due to difficulties in doing so as discussed in Chapter 2. Another loss aspect that affects the simulation accuracy is the equivalent series resistances of all the passive components, in particular the inductances. The quality factor of

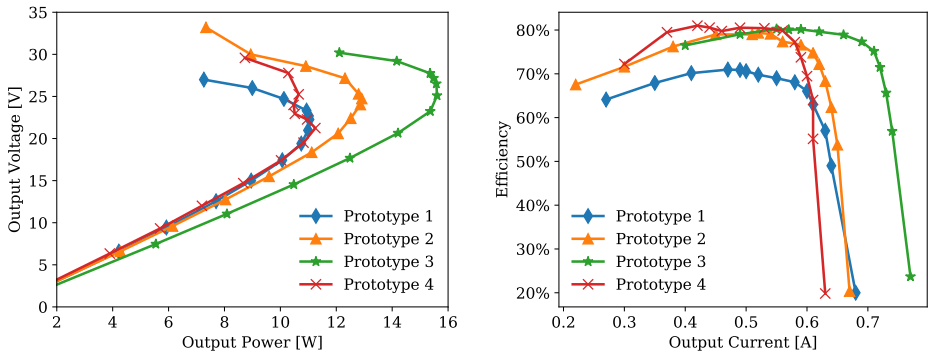


Figure 4.9: Experimental results from the four prototypes [**P5**]. a) Output voltage variation as a function of output power. b) Efficiency as a function of output current [**P5**].

a commercial air core inductor at 6.78 MHz is found to be 70[3], which is around half of the value of 150 used in simulations. For the transformer coils, although the inductance can be measured with good accuracy, it is challenging to verify the simulated series resistance at the operating frequency.

All converters could handle the short-circuit condition without reaching the thermal limit of the inverter. The short-circuit operation is identified in Fig. 4.9(a) as the output voltage tends towards zero in the nose curves. In contrast, a loss of soft-switching was observed for all of the prototypes as the load resistance increased towards open-circuit. As a result, the switching losses increase drastically and the inverter IC quickly reaches its thermal limit. Hence, the nose curves stop for increasing output voltages. Two factors contribute to this operational characteristic. Firstly, there are discrepancies between the simulation model and the real circuit, e.g. actual device capacitance, that contribute to the mismatch. Secondly, and more importantly, the optimisation algorithm maximises the performance in a single operating point. As a result, soft-switching for other operating points is not guaranteed. However, it was observed that the soft-switching range could be expanded by slightly increasing C_s, leading to higher average converting efficiency over a larger operating range.

To further demonstrate the feasibility of the converter structure, an additional experiment was performed with prototype #4. This prototype was chosen since it has demonstrated high efficiency and lower inverter losses over the tested load range, as seen in Figs. 4.9(b) and 4.10, respectively. Additionally, lower output

[3]Coilcraft 2929SQ-501, https://www.coilcraft.com/1515sq.cfm

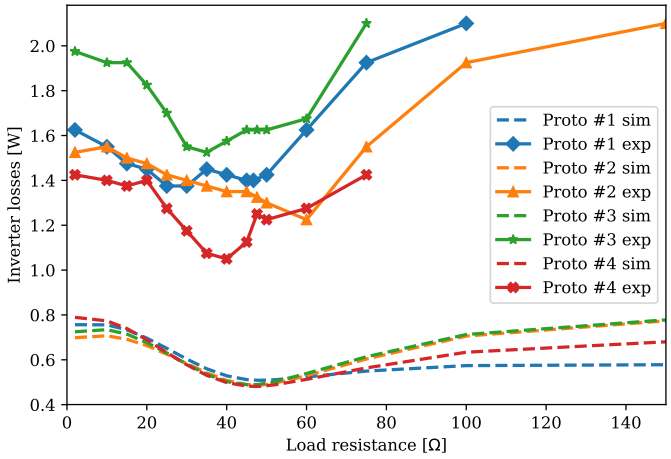


Figure 4.10: Comparison between simulated and measured inverter losses for the four prototypes.

voltage variation was expected due to the high A_r factor. Before carrying out the experiment, the capacitor C_s was increased compared to the optimised value to expand the soft-switching operating range of the converter. The output of the converter was loaded with four commercial gate drivers and a static minimal load (Fig.4.11(a)). This setup is the same as for the intended application previously shown in Fig. 4.1, where the auxiliary power supply feeds the four gate drivers in a full-bridge converter module. To demonstrate the output voltage variation of prototype 4 with changing load, the switching frequency of the four gate drivers is varied from 0 to 20 kHz. The resulting load line is shown in Fig. 4.11(b). From this figure, it is observed that the output voltage only slightly changes over most of the operating range, with less than 10% decrease up to 9 W of output power. As shown in Fig. 4.11(c), the measured dc-dc efficiency was higher than 80% for output powers of 6.5 W and above with a peak efficiency of 81.4%.

4.5 Conclusion

This chapter has discussed and investigated the criteria and performance of an auxiliary power supply for a medium-voltage converter module using a resonant converter topology with a medium-voltage isolation transformer. There are three main criteria in the design, namely **high efficiency**, **output voltage regulation** and **low coupling capacitance**. A genetic algorithm was used to optimise the converter design based on efficiency and size, of which the latter influences the coupling capacitance. By investigating the performance of the optimised designs, the hypotheses on the rectifier design discussed in the previous chapter were verified.

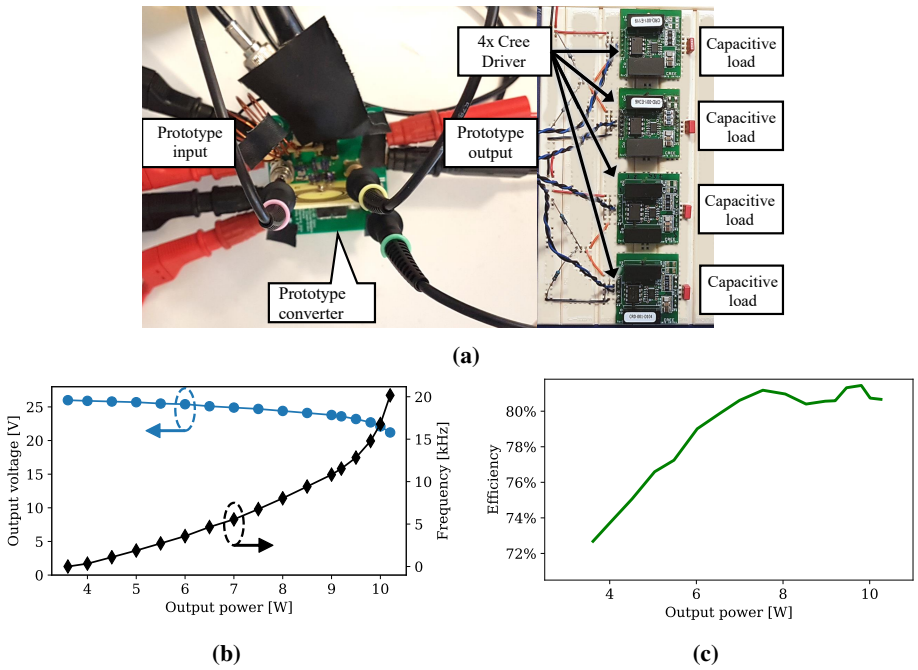


Figure 4.11: a) Photo of prototype 4 and the load on the output consisting of four Cree SiC MOSFET drivers (CRD-001) [**P5**]. b) The load line of prototype #4 while powering four Cree SiC MOSFET drivers with capacitive loads, where the output power varies with the driver switching frequency [**P5**]. c) Dc-dc efficiency of prototype 4 while supplying the gate-driver load.

Four designs from the optimisation results were selected for prototyping. The four prototypes are primarily distinguished by the transformer size, where the efficiency increases with transformer size. While other aspects of prototypes 1–3 are similar, the resonance frequency of prototype 4 is twice the operating frequency. Despite the efforts made in establishing accurate models of the converter components, a significant difference in converter efficiency between simulation and measurements was observed. From these results, it is clear that the challenges in modelling losses for GaN HEMTs negatively affect the design procedure. Subsequently, the optimisation procedure is similarly affected. The lack of modelling accuracy gives an erroneous simulation result. Consequently, this inaccuracy introduces an uncertainty for the designer since the simulated losses are not representative of the experimental performance. To further improve the design, the designer is left to explore changes experimentally, which is both more time- and resource-consuming. At the same time, a successful demonstration of prototype 4 supplying four commercial gate drivers shows the feasibility of the proposed solution. Both the output

voltage regulation and the maximum output power fulfil the application criteria. Simultaneously, the converter demonstrates an efficiency above 80% over a large operating range.

Moreover, the optimisation results demonstrate a contradiction regarding the use of such algorithms. On the one hand, if all parameters are unconstrained, the algorithm can explore design spaces that were not previously evident to the designer. After the optimisation results were ready, detailed investigations of the class E rectifier were performed to validate the basis for designing the resonance frequency higher than the operating frequency. From those investigations it was made obvious that the voltage gain is the highest at $A_r = 1.5$ and that a high voltage gain is beneficial for the converter efficiency. On the other hand, it is preferential to possess analytical knowledge on the system to guide the optimisation algorithm. Notably, high voltage gain gives better efficiency or smaller size. However, for the system operation it is beneficial to sacrifice some voltage gain in order to obtain lower output voltage fluctuation with load. By increasing A_r even further, the output voltage exhibits a lower variation for varying load, as seen for prototype #4. This is a desired behaviour of a power supply operated in open loop. Consequently, the first runs with genetic algorithms should likely be left free to explore the design space. Conversely, later runs should add design restrictions, e.g. $A_r > 1.5$, to find optimised individuals in the design space recognised as a better global optimum by the designer. Although such restrictions could be added to the objective functions early on, this would possibly add considerable calculation burdens and the optimisation time is greatly increased. It is considered less risky to perform multiple runs with shorter run times than the opposite case, since a failed simulation setup will result in a greater loss of time.

Although effort should be put into optimising the converter efficiency and operation as a whole, it is more important to focus on the design and optimisation of the high-voltage transformer. From a system perspective, the isolation transformer is the most crucial component in the converter. It is paramount that the isolation properties of the transformer are upheld to ensure the safety and operation of the medium-voltage converter. Similarly, a high coupling capacitance can negatively impact the system reliability due to noise currents, which also makes it a crucial design aspect. In contrast, the efficiency of the auxiliary converter is of less importance, since these losses will only marginally affect the efficiency of the medium-voltage converter. Therefore, the transformer design, including additional degrees of freedom, is investigated in detail in the following chapter.

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Chapter 5

Printed planar transformer design for high-voltage isolation

In this chapter, a design methodology is presented for planar, printed transformer with isolation voltages well into the medium-voltage range. The transformer is assembled by sandwiching solid insulation between two planar PCB coils. Among all the design characteristics of the transformer, the most crucial ones are the breakdown voltage, governed by the peak electric fields, and the coupling capacitance between the primary and secondary sides, which is a parasitic element appearing over the isolation barrier, as indicated in Fig. 5.1. Furthermore, low variation in self-inductance and coupling factor is also of importance since they affect the converter operation and efficiency. A design space is mapped for a target self-inductance of 1 µH and a coupling capacitance of 10 pF. The inductance value is suitable for an auxiliary power supply operating at the set frequency of 6.78 MHz. In addition, challenges, and potential solutions, related to electric field amplification are investigated in detail using finite element analysis. The electrical parameters and breakdown voltage of ten different transformer designs are verified experimentally. This chapter presents a summary of articles [**P4**, **P6**].

Contributions

Although several previous works have investigated the design and optimisation of planar transformers, a knowledge gap exists regarding the effect of adding the coupling capacitance to the design problem. The author's work shows that several combinations of winding layers and turns can obtain the same self-inductance and coupling capacitance with similar operating efficiency. The difference lies in the thickness of the insulation layer which affects the breakdown voltage of the

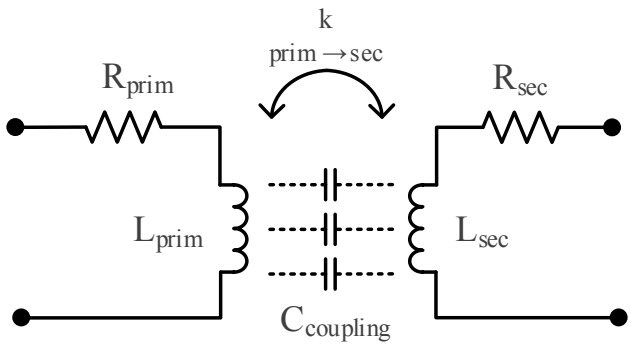


Figure 5.1: Schematic diagram of the transformer [**P4**].

transformer [**P4**, **P6**].

The peak electric field occurring in such a transformer is also investigated in [**P6**]. Although sharp edges are known to amplify the electric field, there has been little work that documents the conditions for such transformers. Two-dimensional FEA simulations show why the outer and inner edges of the PCB winding are the most critical regions. Moreover, different field-grading techniques are investigated and evaluated based on their effectiveness and manufacturing effort. It is indicated that permittivity field-grading is the most suitable approach for such transformers. From the identified design space, a total of ten transformer designs are verified experimentally. The resulting breakdown voltages and placement for all designs are reported with sample sizes of 10, which constitutes a significant amount of data to evaluate the feasibility of compact transformers using solid insulation material. The breakdown voltage level indicates that the isolation level is into the range of several tens of kilovolts, which is suitable for auxiliary power supplies in medium-voltage converters.

5.1 Background

For operation in the auxiliary power supply, the transformer can be represented as a lumped parameter model that is shown in Fig. 5.1, consisting of self-inductance, a resistive element, coupling factor and coupling capacitance. The optimisation results shown in the previous chapter used a simplified coil design and a fixed distance between the coils. Measured coupling capacitance and efficiency demonstrated the correlation between transformer size, converter efficiency and coupling capacitance [**P5**]. Prototype #4 has the largest footprint, highest efficiency and good output voltage regulation. However, it also has the highest coupling capacitance of 18.3 pF, which is high compared to the capacitances reported in the

literature. Further optimisation of the transformer is achievable if more degrees of freedom are added to the transformer design procedure. In particular, the insulation material can be substituted for a material with a lower dielectric constant [**P5**], and the number of winding layers and the distance between the coils can be adjusted [**P4**, **P6**]. In the field of wireless power transfer, many investigations have been made on coil optimisation. In summary, coils with a single turn have lower resistance than multi-turn coils [15], and equal size primary and secondary coils with no misalignment have the highest coupling factor [16]. A conclusion that could be drawn is that single-turn coils offer the best performance. However, none of these investigations take the coupling capacitance into account at the same time. [**P4**] shows that a range of different variations in turn-number and turn-layers can give the same transformer efficiency, although with different sizes and distance between coils.

The choice of insulation material also influences the possible breakdown voltage of the transformer. Materials that can sustain higher electric fields will allow for higher operational voltages. As an example, exchanging FR4 with polytetraflouorethylene (PTFE) can theoretically more than double the allowable voltage [**P5**]. Alternatively, the increased allowable electric field can be exploited to produce more compact designs with higher power density. The latter will positively affect efficiency due to the increased coupling factor of the coils. Examples of planar transformers with PCB windings with isolation voltages of 5 kV or more are found in the literature using polypropylene [8, 9], polysterimide [2, 12], polyimide [10], or PTFE (also known as Teflon) [12] as insulation material. The thickness of the insulation material is reported to be in the range of 1 to 1.6 mm. For coreless isolation transformers, the auxiliary power supply is often operating at multi-megahertz frequency [10, 11, 14, **P5**]. However, no detailed investigations into the electric field distribution are reported earlier for coreless PCB planar transformers.

In this work, the design of planar, coreless transformers for high frequency and high isolation voltage is investigated in terms of electric and dielectric performance by both simulation and experimental work. The transformer circuit parameters and electric field distribution are identified from finite element analysis with 2D axial symmetry. The operating frequency is set to 6.78 MHz, which allows a coreless design to use thicker insulation material while upholding the transformer efficiency. As an additional contribution, this work investigates concepts for grading the electric field of PCB windings that are suitable for the design of coreless, high-frequency transformers with high isolation voltage.

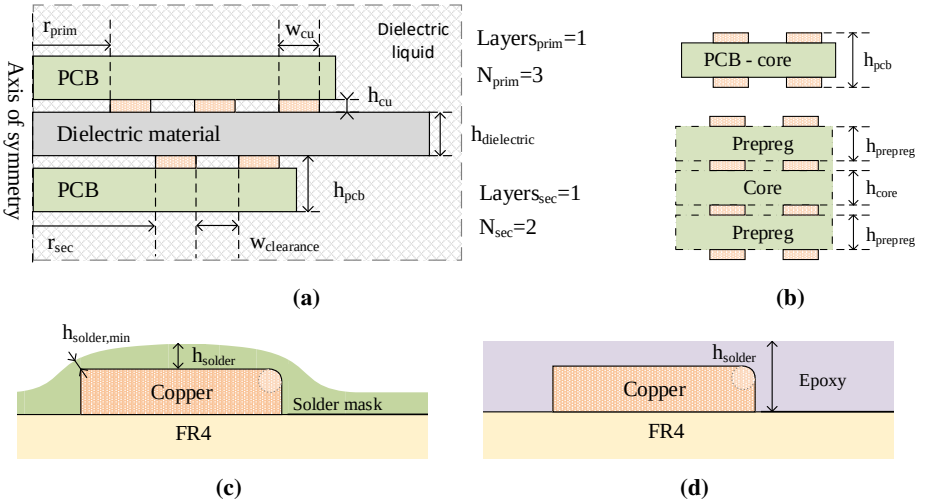


Figure 5.2: a) Axial-symmetric geometry of the transformer [**P4**]. b) Cross-section of 2-layer PCBs and 4-layer PCBs showing the stack build-up of multi-layered PCBs [**P4**]. c) Typical geometry of solder mask layer [**P6**]. d) Geometry of applied epoxy layer for layer thicknesses of 50 and 100 µm [**P6**].

5.2 Modelling of the transformer

The windings of the planar transformer are printed as spiral windings on a PCB. As a result, the geometry of the transformer can be described as an axial-symmetric cross-section that is illustrated in Fig. 5.2(a) [**P6**]. For all parameters, *prim* and *sec* indicate the primary and secondary side, respectively. The set of parameters consists of the number of winding layers ($Layers_x$), the number of turns on each layer (N_x), the width and the height of the copper track (w_{cu} and h_{cu}), the distance between tracks ($w_{clearance}$), and the radius from the centre to the inner winding (r_x). For simplicity, the number of turns per winding layer on the PCBs are set equal. Furthermore, the height of the dielectric material placed between the primary and secondary side of the transformer is defined as $h_{dielectric}$. While Fig. 5.2(a) shows a transformer with primary and secondary sides made up of single-layer PCBs, alternatively, the windings on either side of the transformer can be made as multi-layer PCBs. The geometry of double-layer and four-layer PCBs is shown in Fig. 5.2(b), which adds additional degrees of freedom.

A lumped circuit parameter model is used to describe the circuit performance of the transformer, as previously shown in Fig. 5.1, where the primary and secondary sides consist of the self inductances (L_{prim}, L_{sec}) in series with an equivalent series-resistance (ESR) of the winding ($R_{ESR,prim}$, $R_{ESR,sec}$). The lack of a mag-

netic core and the non-magnetic behaviour of the FR4 material of the PCB limits the loss factors to the winding losses. Due to the frequency dependence of the winding losses, the ESR is only valid for a single frequency. Additionally, the transformer is characterised by a coupling factor, *k*, and a coupling capacitance, $C_{coupling}$, between the primary and secondary sides. Several combinations of geometry parameters will be able to satisfy a given inductance value. Transformer designs across different numbers of layers, turns and dielectric height can be compared using a figure of merit (FOM) used for coupled inductors [4]:

$$FOM = k\sqrt{Q_{prim}Q_{sec}} = k\omega\sqrt{\frac{L_{prim}L_{sec}}{R_{prim}R_{sec}}} \tag{5.1}$$

where k is the coupling factor, ω is the angular frequency, and Q_x, L_x, and R_x represent the quality factor, inductance and resistance [**P4**]. The FOM is a direct measure for the transformer efficiency in a wireless power transfer system [4]. For a target inductance value, the transformer efficiency is improved by lowering the track resistance and increasing the coupling factor. To maximise the coupling factor, the primary and secondary side coils are made equal [16]. Furthermore, it can be shown that the track resistance increases with increasing turn number [15]; however, this design might not be the optimal choice [**P4**]. To understand this, the transformer coupling capacitance is approximated as a plate capacitor:

$$C = \frac{\epsilon_0\epsilon_r S}{d} \tag{5.2}$$

where the plate area, *S*, is proportional to the area of the spiral windings, the gap distance, *d*, is approximately equal to the thickness of the dielectric material, and the permittivity, $\epsilon_0\epsilon_r$, is given by the properties of the dielectric material. Having a single winding turn results in a high effective area, *S*. To keep the capacitance below the capacitance target value, the gap distance is increased, with a resulting decrease in the transformer coupling factor, *k*, and, hence, a reduction of the transformer FOM. Consequently, the optimal design is no longer trivial. The geometry of the windings and the choice of the dielectric material will affect the final coupling capacitance value.

5.3 Mapping of the design space

Using an FEA software, the performances of several transformer designs were mapped within the range of parameters listed in Table 5.1. The geometry variables are adjusted to obtain the target self-inductance and coupling capacitance for the operating frequency of 6.78 MHz. Three of the design variables are fixed, namely

Number of layers	Range of windings *prim/sec*	Height PCB core	Height prepreg
1	from 2 to 5	1.0 mm	-
2	from 1 to 5	1.0 mm	-
4	from 1 to 3	0.75 mm	0.08 mm

Copper height	Copper width	Track clearance	Target inductance	Target capacitance	Operating frequency
35 µm	3.0 mm	0.5 mm	1.0 µH	10 pF	6.78 MHz

Table 5.1: PCB and winding parameters for the different design cases [**P6**].

copper height, width, and track clearance, to simplify the comparison between the number of layers and turns. The resulting FOM, insulation thickness and transformer outer radius are reported in Fig. 5.3 [**P4**]. The darker colouring indicates the desired result, i.e. higher number for FOM (high efficiency), lower height for insulation thickness (compactness), and smaller outer radius (compactness).

A diagonal trend is observed in the FOM matrix in Fig. 5.3(a). As indicated by the colouring, approximately the same FOM can be obtained across different numbers of layers and turns. For a low number of turns and layers, the effective area between the coils becomes high as the radius needed to achieve 1 µH becomes large (Fig. 5.3(c)). As a result, the dielectric height is increased substantially, as seen in Fig. 5.3(b), e.g. 19 mm for the 1-layer 2-turn coil compared to approximately 1 mm thickness for coils made on four-layer PCBs. On the one hand, four-layer coils obtain the smallest size due to the low surface between the two transformer sides. On the other hand, single-layer coils can likely sustain higher isolation voltages due to the increased height of the dielectric needed to fulfil the coupling capacitance constraint. Hence, the optimal design choice will depend on the design and operating constraints of the converter.

From the design space identified in simulations, five designs with similar FOM and outer radius have been selected for prototyping and experimental validations [**P4**]. Two of the five prototypes (#2 and #4) are the designs with the highest identified FOM. The remaining three prototypes (#1, #3, and #5) have similar FOM in the range of 50 across one-, two- and four-layer designs with a range in footprint size that is both smaller and larger than the design with highest FOM. These designs are presented and compared in Table 5.2.

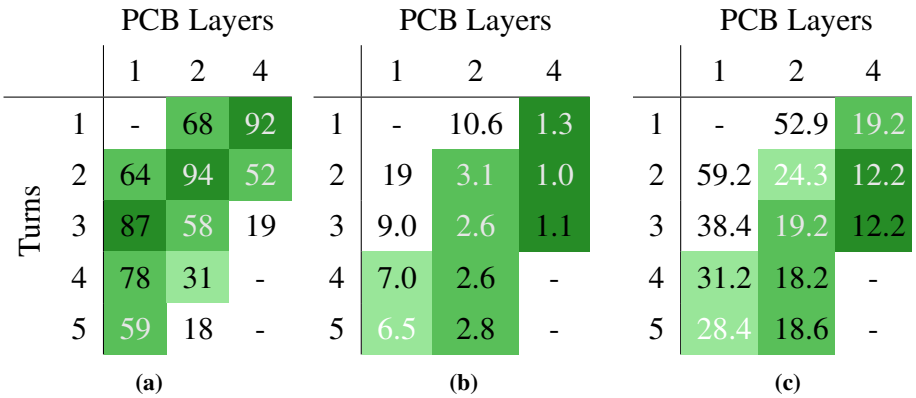


Figure 5.3: Main parameters of the design space used for the evaluation of best individuals. The individuals chosen for prototyping are shown in white text. a) Figure of merit. b) Height of insulation material in mm. c) Outer radius of winding in mm.

Prototype	#1	#2	#3	#4	#5
Layers	1	2	2	4	4
Turns	5	2	3	1	2
Label	*L1T5*	*L2T2*	*L2T3*	*L4T1*	*L4T2*

Table 5.2: The designs chosen for prototyping and associated number and label used in [**P4**, **P6**] and this thesis.

5.4 Investigations of dielectric simulations

With the transformer geometries chosen based on the previous analysis, the transformers were investigated in terms of electric field distribution and peak electric field. The main challenge when using PCBs in high-voltage circuits is the square cross-section of the tracks, which are potential areas where electric field amplification can occur. However, establishing the exact electric field values around the copper edges by simulation is challenging. Firstly, the exact geometry of the corner will depend on the manufacturing technique, in particular the solder mask layer and the copper cross-section. Secondly, 2D FEA simulators are unable to handle simulations of square corners [3]. While the results of a square cross-section in magnetic simulations are less affected by the mesh in the corner regions, the electric field simulations are sensitive to choice of mesh size and geometry in corners and triple points. The edges of the PCB copper track can be rounded in an effort to avoid this issue. However, it is shown that the resulting peak electric field

Proto-type	#1	#2	#3	#4	#5
$V_{50kV/mm}$	27 kV	24 kV	24 kV	16 kV	16 kV
$h_{dielectric}$	6 mm	3 mm	3 mm	1 mm	1 mm
E_{avg}	4.5 kV/mm	8 kV/mm	8 kV/mm	16 kV/mm	16 kV/mm

Table 5.3: Comparison of voltage and average electric field for different designs and insulation thicknesses based on FEA simulations.

is inversely proportional to the corner radius [3]:

$$E_{max} \propto \frac{1}{r^{\frac{1}{3}}} \tag{5.3}$$

Hence, the peak field reported from simulations would depend on the chosen corner geometry. Consequently, the accuracy of the peak field values from simulation can be questionable. As a result, the absolute value of the field is here of lesser interest for the investigations. Rather, the field values are used to identify the high-field regions and to compare different designs against each other. For the identified high-field regions, the track corner edge is rounded with a radius of 20% of the copper height.

Figure 5.4(a) shows the identified areas that experience the highest electric field. Since the geometry is symmetrical over the dielectric material, the areas with high field will be the same and only the primary side is investigated. The example layout in Fig. 5.4(a) summarises all the aspects related to high field areas. Firstly, any adjacent layer away from the dielectric material is shielded by the initial layer. Thus, the field here is lower. Similarly, the corners between tracks provide reciprocal shielding, and the field here is lower as long as the track clearance is low. Hence, the most critical areas are the outer and inner edges of the windings that are closest to the insulation material. An example view of the electrical field is shown in Fig. 5.4(b). It is observed how the electric field becomes high around the corner – which is submerged in the dielectric liquid – and extends into the insulation material. At the same time, the average electric field in the insulation material is much lower. Considering that the insulation material is characterised by a maximum allowable electric field, the field amplification in these corners will be the limiting factor in the insulation design.

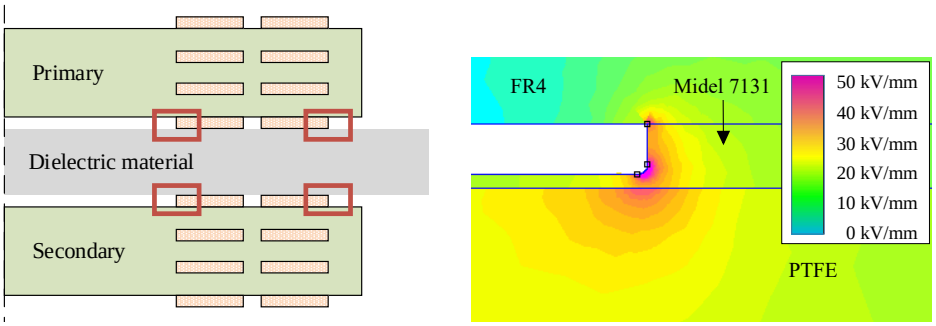


Figure 5.4: a) Diagram indicating the identified areas where the peak electric fields occur [P6]. b) Example view from FEA simulation result of the electric field around the outer edge of the copper track [P6].

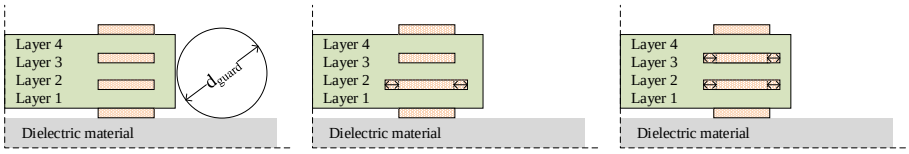
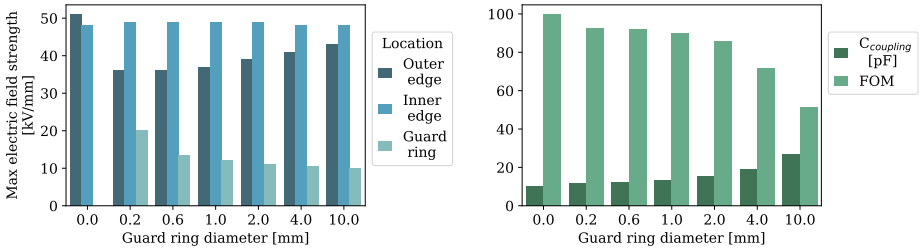


Figure 5.5: Investigated field grading methods include: a) adding a guard ring around the edge of the PCB and elongation of the copper width of b) one or c) two inner-layers of the PCB [**P6**].

5.4.1 Impact of insulation thickness

To investigate the relationship between breakdown voltage and the insulation thickness, the maximum allowable electric field strength is set to 50 kV/mm, approximately the dielectric strength of both PTFE and Midel 7131 [7, 12]. The applied voltage between primary and secondary sides is reported in Table 5.3. It is observed that the allowable voltage level increases with dielectric height. Yet, the voltage increase for an increase insulation thickness becomes smaller with dielectric height, i.e. 8 kV increase from 1 to 3 mm thickness versus 3 kV increase from 3 to 6 mm thickness. An alternative way of highlighting the same issue is by looking at the average electric field, which is decreasing with increasing insulation thickness. This is a consequence of the non-linear relationship between the geometry-amplified electric field and the distance between the coil windings. As a result, there is a less efficient use of the insulation material.



(a) **(b)**

Figure 5.6: Transformer characteristics found through simulation for varying guard ring diameter [**P6**]: a) Maximum field strength of inner and outer corner. b) Coupling capacitance and figure of merit.

5.4.2 Field-grading techniques

To decrease the peak field occurring in the transformer, field-grading techniques are investigated for the discussed application. Measures for addressing the issue of high electric field can be categorised into two main categories: *geometry field grading* or *permittivity field grading*. Increasing the distance between conductors and rounding the conductor cross-section are typical field-grading methods that uses the geometry to decrease peak fields. Permittivity field grading uses the material constants of the different components to push the electric field away from critical areas. Through simulations, the following field-grading methods are investigated:

1. Adding guard rings along the PCB edge (geometry field grading)
2. Increasing track width of inner layers (geometry field grading)
3. Changing the type of epoxy and geometry for the solder mask layer (permittivity field grading)

Geometry field grading

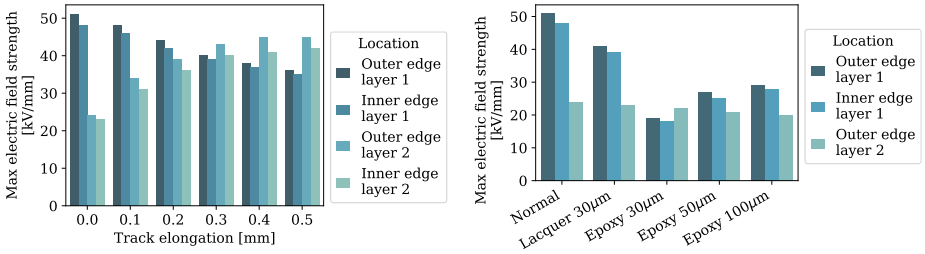
Method 1 is shown in Fig. 5.5(a), where the guard ring cross-section is circular with a given diameter, d_{guard}, and is placed outside the PCB edge. The resulting peak field while varying the guard ring diameter from 0.2 to 10 mm, is given in Fig. 5.6(a). It is observed that the guard ring provides shielding of the copper track edge, but naturally only on the outer corner. For small diameters, the guard ring can be placed close to the copper track and efficiently shield the high field. However, a small diameter ring will also experience higher local field strength, as

seen by the value *guard ring* in Fig. 5.6(a). This can be countered by increasing the guard ring diameter. Yet, due to the larger cross-section of the guard ring, it is now moved further away from the copper corner, and the effective shielding diminishes. Moreover, a shielding technique is also needed on the inner winding for the isolation voltage to be increased. Additionally, Fig. 5.6(b) shows how the guard ring decreases the transformer FOM due to eddy current losses and increases the transformer's coupling capacitance. In conclusion, there are several challenges with using guard rings as a field-grading method for this transformer.

Figures 5.5(b) and 5.5(c) show possible implementations of method 2, where the width of tracks is changed on one or several inner layers. If the windings are printed on multilayer PCBs, then the PCB geometry can be used for field grading. The track width of each individual layer can be manipulated to change the peak electric field. As indicated in Fig. 5.5(b), the width of the copper track on the inner layer (layer 2) can be increased to partly shape the field around the edge of outer layer. Figure 5.7(a) shows how the peak electric field can be shifted from the outermost layer (layer 1) to the next layer (layer 2) by increasing the track width of layer 2. However, increasing the width too far will only move the problem from one layer to another. The dielectric strength of FR4 is quoted lower (30 kV/mm [6]) compared to the used insulation material (PTFE). Figure 5.7(a) shows that an elongation of 0.1 mm in this case violates the FR4 breakdown limit. Yet, if the width of layer 3 is also increased by 0.1 mm (ref. Fig. 5.5(c)), the field on layer 2 inside the FR4 material is within the limit. The advantage of this technique is that it is easy to implement and the change in electrical parameters (resistance, coupling and coupling capacitance) is negligible when elongating the inner layer tracks. However, the reduction in the occurring peak field is limited. Additionally, the FR4 material is known to have variations in performance based on the variations in manufacturing, making it a less reliable choice for insulation.

Permittivity field grading

Method 3 consists of either changing the type of material that covers the copper track surface, or changing both the material type and its geometry. Up until this point, all simulations have been performed while excluding the solder mask layer – with its characteristic green colour – that is normally applied to the surfaces of the PCB. Two types of coatings are added to the simulation with variable geometry and thickness. Figure 5.2(c) shows the typical geometry of the solder mask over a copper track. Due to the layer thickness and the viscosity of the solder mask lacquer, the thickness over the copper edges ($h_{solder,min}$) will be lower than on top of copper and FR4 surfaces (h_{solder}). In [**P6**], the solder layer height is set to 30 µm with a minimum value of 10 µm over the copper edges and the dielectric constant is set to 4. However, the thickness and material properties are given by the PCB



(a) **(b)**

Figure 5.7: Maximum field strength of different winding edges found through simulation for different designs [**P6**]: a) Elongation of the track on layer 2. b) Different coating types and geometry over the copper track compared to bare-copper windings.

manufacturer and can vary significantly between manufacturers. The maximum field values are shown in Fig. 5.7(b) (*Lacquer 30µm*). Adding the solder mask layer to the simulation shows a decrease in the peak electric field of about 20%.

Further expanding on this idea, the solder mask lacquer can be exchanged for an epoxy with a higher dielectric constant. The relative permittivity of the epoxy is set to 9. Additionally, the geometry of this epoxy layer is varied between that of the solder mask (*Epoxy 30µm*) and a box layer (ref. Fig. 5.2(d)) with thicknesses of 50 and 100 µm (*Epoxy 50µm* and *Epoxy 100µm*, respectively). Four observations are made from Fig. 5.7(b) [**P6**]. Firstly, high permittivity epoxy substantially lowers the peak electric field occurring at the corner. Secondly, the electric fields are reduced both at the outer and the inner corners. Thirdly, increasing the thickness of the coating does not decrease the peak field. Lastly, the coating has minimal effect on the field of the layer 2 corner. This is in contrast to employing a guard ring. Thus, using a coating layer to shape the high-field region does not exclude the need to limit the high field occurring on adjacent layers. Changing the normal solder mask to a high permittivity epoxy is found to decrease the field in the outer corners by over 60% compared to bare-copper windings. As long as the coating layers are non-magnetic, the electrical parameters stay essentially unchanged [**P6**].

5.4.3 Transformer prototypes

As previously discussed, only the relative values of electric field are used from the dielectric simulations. Thus, experimental testing is also needed for evaluating the field-grading techniques. In addition to the previous five designs for prototyping (#1–#5), five more prototype designs were made in an effort to validate the dielectric simulations. All five designs are based on prototype #4 from Table 5.2 and are as follows:

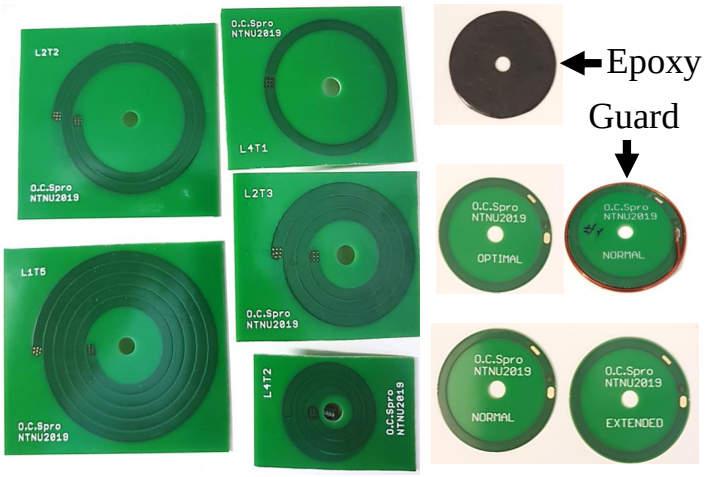


Figure 5.8: Photo of the ten transformer designs used in the experimental validation. On the left, the five designs from Table 5.2 are labelled and the five variations of field grading are shown on the right [**P6**].

NORMAL Normal layout, equal to #4 / L4T1 (4 layers, 1 turn) with 1 mm PTFE. Acts as a reference design.

GUARD Normal layout with an outer guard ring with a diameter of 1.1 mm made with enamelled copper wire, referring to Fig. 5.5(a).

EXTENDED Normal layout with 0.5 mm elongation of the winding on layer 2, referring to Fig. 5.5(b).

OPTIMAL Normal layout with 0.1 mm elongation of the windings on layer 2 and 3, referring to Fig. 5.5(c).

EPOXY Normal layout produced without solder mask and covered with an epoxy with a relative permittivity, ϵ_r, higher than 9, referring to Fig. 5.2(d).

Figure 5.8 shows one sample of each of the ten designs: prototypes #1–5 discussed earlier in the chapter and the five variations in field-grading technique discussed here. In contrast to designs #1–5, all variations are milled from the PCB, so that they are fabricated as similarly as possible. This milling step is a criteria for the *GUARD* design. *NORMAL* has no applied field-grading technique and is used as a control sample. *EXTENDED* design transfers the insulation stress from the insulation material to the FR4 material since the inner layer edge is prominently

(a) **(b)**

Figure 5.9: Photos of the EPOXY samples: a) before applying the epoxy layer and b) after the epoxy was applied.

extended. The elongation of the tracks in *OPTIMAL* also puts more stress on the FR4 material, however, the elongation of the second inner layer was done to balance the field stress inside the PCB structure.

The *EPOXY* samples were fabricated by hand starting from PCBs with the same design as *NORMAL*, but without the solder mask layer. Since the field-grading tests were considered to be an initial proof of concept, the samples were produced by hand. The samples are seen in Figs. 5.9(a) and 5.9(b). From investigations of the production steps, it is assumed that the deposited epoxy layer is slightly uneven with a thickness in the range of 50 to 100 µm. Judging from the simulation results, it is expected that this production process is sufficient to produce experimental results that verify or refute the concept.

5.5 Electrical characterisation

To experimentally validate the electrical characteristics, all ten designs, i.e. #1–5 plus the five variations of #4, were characterised using an impedance analyser (Keysight E4990A). Two identical PCBs were placed together in a fixture with a PTFE disc in between. The PCB prototypes and the characterisation setup are seen in Fig. 5.8 and 5.10.

For all values, the error between the measured and the simulated value is calculated as:

$$err = \frac{X_{meas} - X_{sim}}{X_{sim}} \tag{5.4}$$

where X corresponds to the parameter in question. The error in inductance, ESR, coupling factor and coupling capacitance for all ten designs are summarised in Fig. 5.11. In this figure, the boxes show the span of quartiles 1–3, the whiskers

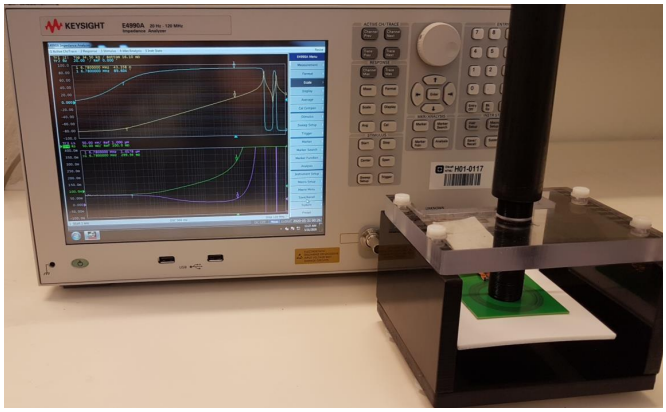


Figure 5.10: Photo of the laboratory test setup for impedance measurement of the transformer using a fixture [**P6**].

show minimum and maximum values and the line indicates the median value. Markers show outliers within the population. The outliers in inductance are related to *L4T2*, which is the most compact of all designs. Since the simplified FEA geometry model does not take via connections and actual spiral windings into consideration, the model is expected to be increasingly inaccurate for increasing transformer density and number of winding layers. Still, overall, the transformer parameters are close to the simulation values. The majority of the inductance values is observed to be within $\pm 4\%$ of the simulated values, with the *L4T2* design being an outlier with an error of -15%. It is not possible to establish the exact reason for this deviation. However, it is the hypothesis of the author that it is related to the inaccurate modelling of the inner track, the via connections and the spiral nature of the winding. The coupling factor for all transformers is within $\pm 7\%$ of the simulated value, which again shows a good correlation between simulations and measurements. The coupling capacitance values have a higher error in percentage, with most of the transformers measuring between 0 and -15% of the simulated value. For the ESR, although it shows large variations compared to the simulated value (-8 to +36%) these variations are within the measurement error band of the impedance analyser at 6.78 MHz.

In conclusion, the results of the electrical characterisation show that the simplified model is accurate for the transformers in the investigated range. The simulated components can be reproduced experimentally with a high level of accuracy. The exception is for the design *L4T2*, which indicates that the model has lower accuracy for compact PCB transformers, i.e. more winding layers, and small footprints. Nevertheless, additional errors are expected for compact winding structures and

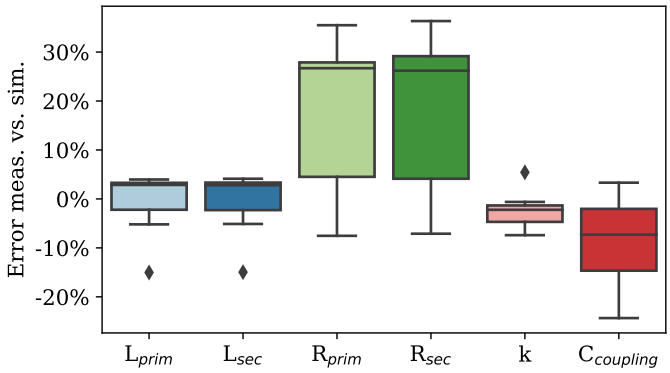


Figure 5.11: Relative error between the measured and simulated values of the transformer electrical parameters [**P6**].

Table 5.4: Mean breakdown voltage and standard deviation for all ten transformer designs [**P6**].

	L4T1	L4T2	L2T3	L2T2	L1T5
mean [kV_{RMS}]	36.7	37.3	47.8	48.7	73.3
std [kV_{RMS}]	3.88	4.58	7.77	6.33	8.16
	NORM	EXT	OPT	GUARD	EPOXY
mean [kV_{RMS}]	32.8	33.1	33.6	34.9	37.0
std [kV_{RMS}]	5.09	4.17	4.14	3.28	2.11

multi-layer transformer designs. Low variation between simulation and final prototypes is critical as any variation in the parameters will affect the performance of the resonant converter that employs such a transformer. Variation in the self-inductance and coupling factor will affect the efficiency and the output voltage of the auxiliary power supply described in the previous chapter. Consequentially, low variation is crucial for the modelling accuracy and the expected operation of the converter system.

5.6 Breakdown voltage results

The step-up breakdown voltage test was chosen to experimentally evaluate the design variations and concepts. A standard test with 50 Hz ac voltage is applied between the primary and the secondary side of the transformer. The voltage was increased in steps of 1 kV followed by a waiting period of 1 minute for each step.

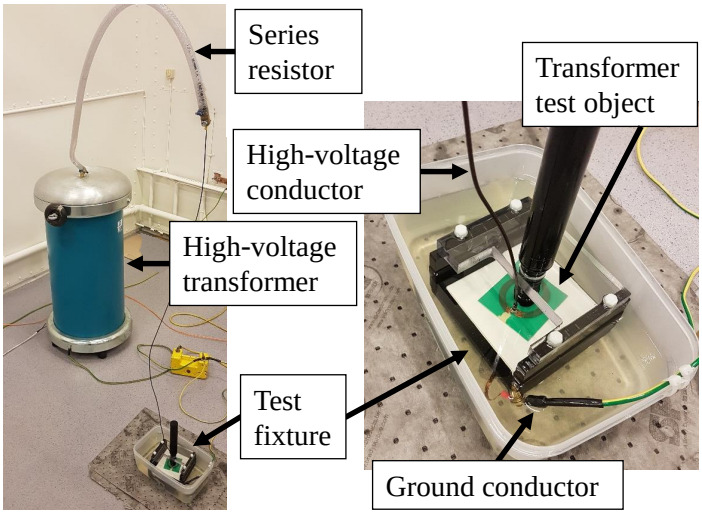


Figure 5.12: Photos of the test setup for the breakdown test using a step-up transformer. The transformer prototypes are placed in a fixture and housed in a container filled with Midel 7131 [**P6**].

	PTFE thickness		
	1 mm	3 mm	6 mm
Avg. breakdown voltage	37 kV	48 kV	73 kV
Avg. electric field	37 kV/mm	16 kV/mm	12 kV/mm

Table 5.5: Average breakdown voltages and electric field values versus insulation thickness.

Ten samples of each design are tested due to the stochastic nature of device breakdown. This is in accordance with IEC 60060 procedure for a class 3 withstand voltage test. However, in a switching converter, the actual voltage transients are expected to be trapezoidal. Consequently, the likelihood of partial discharges and breakdown at lower voltage levels increases [1]. Nevertheless, the selected test is accepted as long as the operating frequency is equal or lower than 30 kHz, as specified in IEC 60664. For medium-voltage, high-power converters, this frequency limit can be considered in the higher range of switching frequencies and the test is deemed appropriate for this work. Figure 5.12 shows the details of the high-voltage test setup.

Breakdown tests are performed for the five different prototypes given in Table 5.2

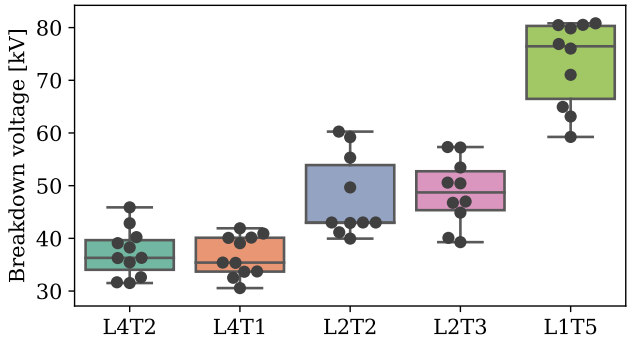


Figure 5.13: Breakdown voltages for designs listed in Table 5.2 [**P6**].

as well as the five design variations of prototype #4 for testing field-grading methods. Table 5.4 shows the average and standard deviation in the recorded breakdown voltages. Visualisation of the breakdown voltages for different designs are shown in Figs. 5.13 and 5.14. It should be noted that six tests of *L1T5* were stopped due to the voltage limitation of the test setup and, as such, the average breakdown voltage of this design can be assumed higher than stated.

The average breakdown voltages for 1, 3, and 6 mm thicknesses are summarised in Table 5.5. It is observed that the breakdown voltage increases with the increase in insulation thickness, i.e. 37, 48, and 73 kV, respectively. Following the standard test voltages given in IEC 60071, the transformers' breakdown voltages are above the test voltage levels for standard insulation levels in the medium-voltage range of 12, 17.5 and 24 kV_{RMS}, respectively. This shows that the transformer concept is suitable for auxiliary power supplies in medium-voltage converters. However, further testing would be necessary to qualify the transformers for long-term operation at these voltage levels. From Table 5.5, it is also observed that the average electric field decreases with increasing insulation thickness. This is the same trend as was identified in simulation. Compared to the simulated values in Table 5.3, the average experimental field values are higher. For the relative difference between the insulation thicknesses, the average field is lower for transformers with 3 mm and higher for transformers with 6 mm.

In Fig. 5.14, a comparison is made between different field-grading techniques applied to #4, where *NORMAL* serves as the benchmark. Although the difference in breakdown voltage between the designs is limited, it follows the expected trend. *EXTENDED* and *OPTIMAL* use the PCB geometry to shield edges of the outermost winding, yet the achievable reduction in peak field is limited and higher elec-

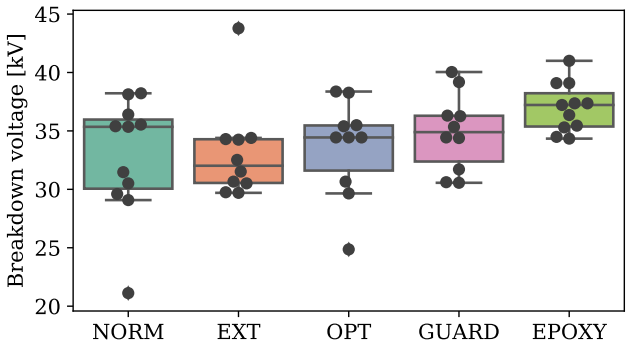


Figure 5.14: Breakdown voltages for the five designs of #4 with varying field-grading techniques [**P6**].

tric fields occur within the less reliable FR4 material. While the track elongation of *EXTENDED* was made rather large, the difference between the cross-section of *OPTIMAL* and *NORMAL* is minimal. As such, *EXTENDED* is likely to have a lower breakdown voltage while *OPTIMAL* should be very similar to *NORMAL*. Adding guard rings should decrease the peak field at the outer edges. *GUARD* is observed to have a slightly higher tendency in breakdown voltage than *NORMAL*. However, the chosen implementation of the guard ring leads to a new breakdown path, as will be discussed below. *EPOXY* samples have a higher breakdown voltage and lower deviation, indicating that the epoxy layer is improving the electric field distribution in the transformer.

For all breakdown events, the breakdown point was registered and categorised. Examples of transformers that fall under different categories are shown in Fig. 5.15. The categories, 'Outer edge' and 'Inner edge', refer to the edge of the conductors which are indicated as a problematic area in the simulations (Fig. 5.4(a)). 'Middle track' accounts for all breakdowns that are not close to the edge or somewhere on the inner tracks. In cases where breakdowns occurred from guard ring to guard ring, these were registered as 'GR to GR'.

In Fig. 5.16(a), the number of breakdown points is aggregated for all transformers. As can be seen, the majority of the breakdowns occurred on the outer edges of the PCB windings. This validates the peak electric fields area found in simulation. The "middle track" category is observed to contain a large proportion of the total population, consisting of approximately one-third of the breakdowns. The possible reasons for breakdowns in this area are the variations in fabrication of the PCBs, defects in the insulation material, and other possible high-field regions in the spiral structure that are not captured by the 2D transformer model. However, establishing

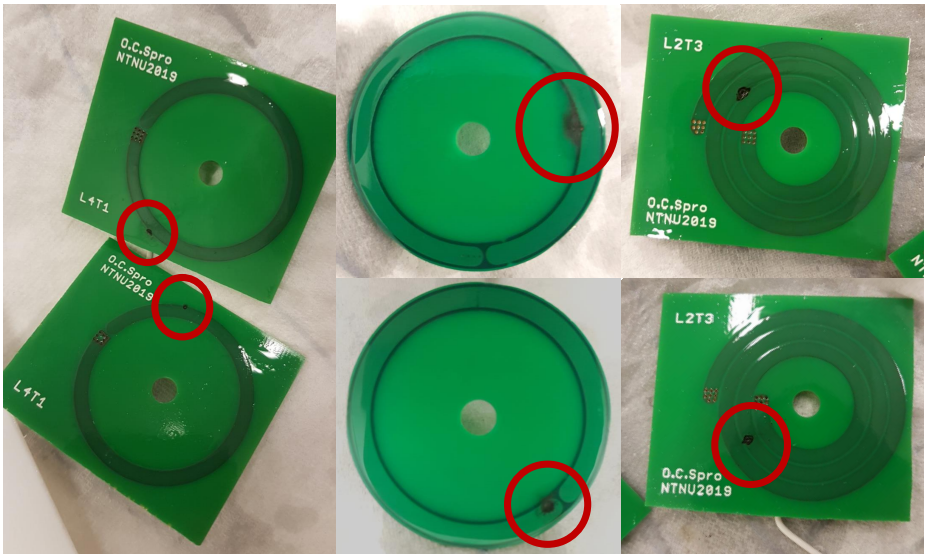


Figure 5.15: Examples of transformers after breakdown. From left: L4T1 sample 6 outer edge, EXT sample 3 inner edge, L2T3 sample 10 middle track.

the reason behind these breakdowns would necessitate new investigations. For the *GUARD* design, 6 samples had a breakdown path that includes the guard ring. Thus, a new breakdown path was introduced and shows the sensitivity of guard ring implementation of this design. An example of the breakdown of guard to guard ring is provided in Fig. 5.17. One example shows that the breakdown occurred on the outer side of the ring (left) while the other example shows a breakdown in a nook where the guard ring is bent (right).

To complement the discussions on breakdown point, Fig. 5.16(b) shows the breakdown point divided per design. It can be noted that designs *L1T5* and *GUARD* only have 4 samples. For *L1T5* it is due to the lack of breakdown during testing, as discussed previously. For the *GUARD* samples, the remaining samples fall under the category 'GR to GR' (ref. Fig. 5.16(a)) which is not plotted in Fig. 5.16(b). Consequently, their population sizes are smaller and are omitted from the discussion here. From Fig. 5.16(b), it is observed that the designs with 1 mm PTFE (*L4Tx*, *NORMAL*, *EXTENDED*, *OPTIMAL*, *EPOXY*) appear to have a larger spread in their breakdown point. In contrast, the majority of breakdowns for designs with a thicker PTFE layer (*L2Tx*) are at the outer edge. It is hypothesised that this is correlated with the average electric field in the PTFE has given by Table 5.5, making the high-field regions more critical for larger insulation thicknesses.

For the field-grading techniques, the decrease in breakdown voltage for *EXTEN-*

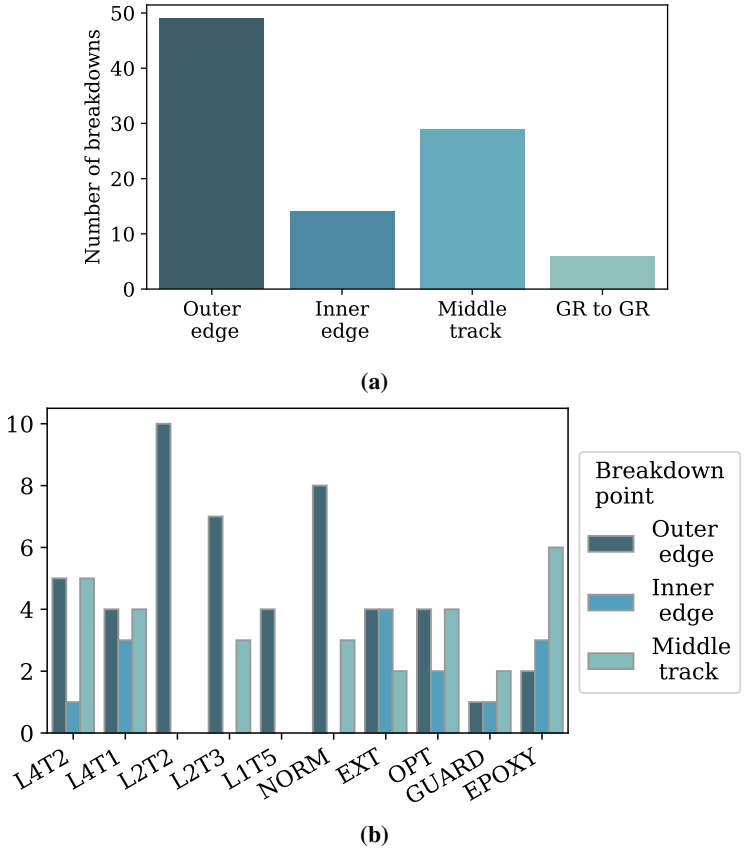


Figure 5.16: Number of breakdowns per defined breakdown point category. a) Aggregated data for all designs. b) Breakdown point per design for the three largest categories [**P6**].

DED and *OPTIMAL* designs indicate that using geometry-based shielding inside the PCB is not effective. As previously stated, the insulation properties of FR4 are worse than for the chosen insulation material since the dielectric strength is lower. This is suspected to be the reason for the decrease in breakdown voltage. In contrast, the breakdown voltage increased slightly for *GUARD* and *EPOXY*. However, the breakdown path changed, i.e. 'GR to GR' for *GUARD* and a shift towards 'Middle track' for *EPOXY*. This result can be interpreted as a successful implementation of the field-grading technique. Thus, the electric field on the outer edge is decreased and the breakdown occurs at the next design weakness. Nevertheless, the techniques could also be said to introduce new weaknesses by the same observations. Determining how to apply these techniques in an optimal way would require additional testing.

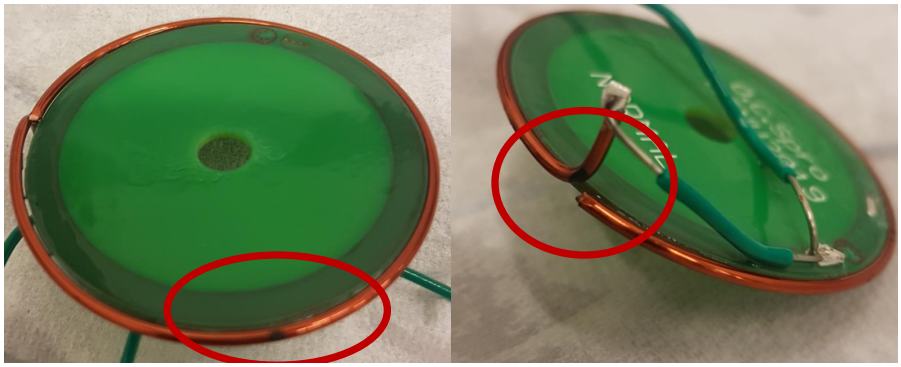


Figure 5.17: Examples of GUARD samples where the arc travelled from guard ring to guard ring. Left: breakdown on the outer side of the guard ring (sample 7). Right: breakdown starting from the separation in the guard ring itself (sample 6).

Based on these observations, some directions for future work are postulated. Firstly, testing of field-grading techniques should be performed with thicker insulation material. The data suggest that the outer edge breakdown is more prominent. Therefore it is hypothesised that field-grading techniques, if successful, would noticeably increase the breakdown voltage level. Future work should also include a design sample without solder mask to validate the effect of the solder mask layer that was identified in simulation. As previously mentioned, optimisation of the field-grading techniques would also be needed to demonstrate the practical performance gain by these techniques. In this regard, this work is conceptual and serves as a proof-of-concept.

5.7 Other design aspects

As stated in [**P4**,**P6**], equal transformer sides lead to a maximised coupling factor, thus resulting in higher efficiency. This design choice is consistently implemented in all the publications. Alternatively, minimisation of the coupling capacitance can be achieved by designing asymmetrical winding sizes of the transformer [10]. On the one hand, low coupling capacitance can be achieved despite the high power density of the transformer. On the other hand, the coupling factor, and thus the efficiency, decreases. In addition, the smaller sized winding will experience higher electric fields and, thus, limiting the isolation voltage level. These aspects can be observed in [10], but they are not discussed.

Moreover, the winding design could be expanded to incorporate other aspects that are found in the literature. The design could include the concept of varying winding width [5] and hollowness of the winding [13]. The former targets lowering

inter-winding capacitance if this is an issue for the application, while the latter can minimise the winding losses. The inter-winding capacitance forms a parallel resonance circuit with the transformer self-inductance. This can affect the converter performance if the resonance frequency is too close to the operating frequency, as the fundamental or switching harmonics can excite the resonance. Exploring the design spaces while including these concepts is feasible by using optimisation algorithms and 2D FEA simulations [**P5**]. Additionally, winding width and clearance were kept constant in this work at 3 and 0.5 mm, respectively. Further optimisation of the transformer efficiency is likely possible by freeing these design variables.

5.8 Conclusion

This chapter has presented the design methodology for high-frequency, printed planar transformers with isolation voltage in the medium-voltage range. The winding configuration with the highest efficiency is shown to be dependent on three aspects: self-inductance, coupling capacitance and isolation voltage level. For each layer and turn combination, the inductance target is achieved by changing the inner radius of the windings. Moreover, the coupling capacitance between the primary and secondary sides is reached by adjusting the insulation thickness. The required thickness depends on the effective surface area of the windings on the two sides. As shown experimentally, the insulation thickness greatly influences the breakdown voltage of the transformer.

The design methodology uses 2D FEA simulations to evaluate different transformer designs. Using a cross-section of the geometry results in low computation times. Consequently, the method can be used in practice to explore a large design space. Experimental characterisation of several prototypes shows that the method is sufficiently accurate for most geometries. The exception lies with the compact design, e.g. small inner radius, multiple layers, and several turns. In particular, the discrepancy is suspected to be due to an overestimation of the inductance of small-radius windings in simulation due to the actual spiral geometry of printed windings.

For the dielectric design, the sharp edges of the inner and outer PCB windings were found to amplify the electric field around the copper edge as expected. The consequence of the field amplification is a decrease in the achievable isolation voltage of the transformer. Several methods for the field grading of planar PCB transformers are investigated in simulation and experimentally. The most promising method is changing the solder mask epoxy for an epoxy with a higher relative permittivity (permittivity field grading). From experiments, this method exhibits the highest breakdown voltage, although only slightly higher than the reference.

Yet, the fabrication process can be easily industrialised and does not affect the transformer's electrical performance. In contrast, the classical field-grading approach of adding a guard ring only marginally increases the breakdown voltage while lowering the transformer efficiency and increases the coupling capacitance between the primary and the secondary sides.

In summary, the breakdown voltage level and compactness of the transformer prototypes demonstrate their feasibility for use in auxiliary power supplies for medium-voltage converters. The low variability in the transformer parameters renders them suitable for resonant converter topologies such as the one presented in the previous chapter. Additionally, the transformer can be produced with automated industrial processes, which is beneficial for minimising both parameter variability and cost. Furthermore, it is assumed that there is a room for further optimisation of the transformer's electric and dielectric performance. Still, the long-term performance of the concept requires additional testing.

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Chapter 6

Conclusions

This PhD thesis has modelled, optimised and validated the performance and isolation voltage increase of an auxiliary power supply by leveraging the inherent capabilities of GaN HEMTs. A simulation-based design methodology is presented and validated experimentally for both the converter topology and the isolation transformer.

GaN HEMT devices have shown great potential for performance improvements in the power electronics domain. Based on the characteristics of the semiconductor material and structure, the theoretical potential of GaN HEMTs allow for lower on-state losses compared to other unipolar devices made with both Si and SiC. Additionally, the device structure results in low capacitance values and eliminates the reverse recovery loss, which leads to advantages for converters operating at high switching frequencies. Due to a cap of 600 V voltage rating of currently available devices, relevant cases for using GaN HEMTs are limited to low-voltage applications.

The additional loss factors of GaN HEMTs, namely dynamic on-state resistance and C_{oss}-losses, have been shown to scale with frequency. Thus, these losses represent a hindrance for improving the efficiency of converters operating at multi-megahertz frequencies. The difficulties in accurate modelling of these losses present a challenge in designing converters by using simulation tools. Consequently, virtual prototyping, which is more time- and material-efficient than design by prototyping, also becomes challenging. Yet, it has been demonstrated that GaN HEMT can be utilised to improve the capabilities of auxiliary power supplies. The high switching frequency enables smaller transformer size while efficiency is upheld, with a measured dc-dc efficiency reaching over 80%. Since the device technology

is immature and device performance has continuously progressed, it is expected that future GaN devices will outperform the current generation. For the hysteresis losses, pre-design selection of devices based on expected operating voltage, current and frequency can be performed as shown in [8].

In the targeted application, an auxiliary power supply is energising the gate driver and other auxiliary loads of a converter module in a medium-voltage converter. The auxiliary power supply is realised using a resonant topology operating at 6.78 MHz. The topology consists of a GaN HEMT half-bridge inverter, an LCC resonant tank, an isolation transformer and a class E rectifier, operating with a 48 V input voltage, and a 20 to 25 V output voltage. During identification of a suitable topology for the targeted application, this thesis has developed a design methodology for a compact resonant class E rectifier topology. The design methodology incorporates the transformer inductance into the resonance circuit, limiting the additional resonant components to a single capacitor and a single diode. Additionally, by designing the resonance frequency to be higher than the operating frequency, i.e. 1.5 to 2 times higher, the converter efficiency can be increased and inherent output voltage regulation can be obtained. In this context, it has been shown that using FHA for the basis of the design equations must be critically evaluated. The assumption is that the fundamental frequency component dominates other harmonics, and this basis falters when the resonance circuit is no longer designed around the operating frequency.

For designing the converter, an optimisation process based on a genetic algorithm is used. The algorithm evaluates converter designs by first extracting transformer parameters by 2D finite element analysis simulation, and then evaluating circuit performance evaluation through SPICE simulations. Four prototypes were made from the identified Pareto front. These prototypes were able to transfer from 11 to 16 W with a measured peak efficiency from 71-81%, where the main difference between the prototypes is the transformer size and the resonance frequency of the rectifier. The output voltage regulation is experimentally validated, showing less than 9% voltage drop for a load change from 3 to 9 W.

The breakdown tests of isolation transformers using printed windings demonstrates the feasibility of operating well into the medium-voltage range. Using printed windings allows for higher accuracy and higher precision of transformer parameters, e.g. self-inductance and resistance. A design methodology was developed for identifying the combination of winding layers and turns that give the **highest transformer efficiency** for the **target isolation voltage** and **maximum coupling capacitance**. Since the 2D geometry is computationally inexpensive, the methodology allows for extensive mapping of the design space while taking all three aspects into consideration. Breakdown testing was performed according to IEC standards.

These same standards indicate that the transformer designs with 1, 3 and 6 mm PTFE insulation could provide isolation while operating at medium-voltage levels of 12, 17.5 and 24 $\mathrm{kV_{rms}}$. However, additional testing would be needed to assess the long-term isolation capability. The majority of the breakdown locations are consistent with the high electric field regions identified through FEA simulations. Due to the sharp edges, the critical area is along the inner and outer track edges of the winding closest to the insulation material. Investigations have been made into possible field-grading techniques that could be applied in the application, from which permittivity field grading shows the most promise. Application of an epoxy with high dielectric constant instead of the PCB solder mask minimises the peak field occurring on these edges almost without affecting the magnetic properties of the transformer.

6.1 Future work

The future work is primarily targeted to the topology and transformer aspects. It is believed that the performance enhancement of GaN HEMT converters is principally dependent on manufacturers' ability to eliminate the additional loss factors of the semiconductor device – dynamic on-state resistance and hysteresis losses. However, for the practising engineer, a framework for taking the losses into account in the design phase would be useful for designers. This includes device selection for minimisation of hysteresis losses [8] and reporting of dynamic on-state resistance for various operating parameters [9]. Without any information on the influence of design and operating parameters, the designer is left to execute the mission by 'trial and error' prototyping.

For the field of auxiliary and gate driver power supply design for medium-voltage converters, a framework for deciding the upper boundary of allowable coupling capacitance over the isolation barrier would be of value. This could also be extended to converters switching at high dv/dt. As present, there does not seem to be a consensus. Such a work could build on existing studies, e.g. [5, 7].

Using the developed design methodology, the class E with series-inductance shows great potential in terms of low component count and inherent output voltage regulation. However, a direct benchmark of different rectifier solutions has not been performed. This could be of interest to practising engineers. Furthermore, the concept of designing the resonance outside the operating frequency can be applied to other topologies and other applications. There are existing works that explore this concept [1, 3, 4]; however, the concept should be treated without the use FHA and preferably include non-ideal source characteristics.

Regarding the insulation testing of the transformer concept, the following direc-

tions and aspects are recommended:

— Accelerated lifetime testing of the insulation should be performed to assess the long-term effect of high electric field around the sharp edges of the PCBs. The standard step-up test uses 1-minutes test periods. Instead of recording the breakdown voltage, the time-to-failure should be recorded while the transformer is subjected to constant high voltage potential. These data can be used to produce an Arrhenius plot to give estimated breakdown voltage for a desired lifetime, e.g. 20 years for an industrial product.

— Permittivity field grading shows potential from both experimental breakdown results and from manufacturing aspects. Hence, simulation and experimental work to find optimal *EPOXY* design should be approached in a more systematic manner. Firstly, ideal epoxy geometries could be identified through simulation, with inspiration drawn from adjacent problems in the field, e.g. dielectric design of substrates for medium-voltage semiconductor modules [2, 6]. Secondly, the production of the samples should be industrialised. Alternatively, a manual work process must be established that allows for higher precision in the layer and deposition of epoxy over the transformer.

— Field-grading techniques should be tested at higher voltage levels. From Table 5.5, it is observed that transformers with thicker insulation have lower average electric field and thus have larger potential for increased breakdown voltage of the transformer. Additionally, the breakdown point was observed to be more frequent at the outer edge of the winding. For this reason, the effectiveness of the field-grading technique should be more visible in the data for higher insulation thicknesses.

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