




An Anti-Islanding Protection for VSM Inverters in Distributed Generation

MOHAMMAD AMIN ¹ (Senior Member, IEEE), QING-CHANG ZHONG ² (Fellow, IEEE),
AND ZIJUN LYU ² (Student Member, IEEE)

¹ Department of Electric Power Engineering, Norwegian University of Science and Technology, Trondheim 7491, Norway

² Department of Electrical and Computer Engineering, Illinois Institute of Technology, Chicago, IL 60616 USA

CORRESPONDING AUTHOR: MOHAMMAD AMIN (e-mail: mohammad.amin@ntnu.no).

ABSTRACT Virtual synchronous machine (VSM) technology is an attractive control method for an inverter-based distributed generation (DG) due to having the voltage, and frequency support functionality. Embedding an anti-islanding protection (AIP) scheme with a high accuracy is a requirement for DG inverters due to the safety concern of the personnel, and hazardous operation. This paper presents a novel hybrid AIP scheme for VSM inverters for integration of DG sources into the grid. The main advantage of this AIP scheme is that the proposed scheme can be embedded into the control of the DG inverters without a need of additional part in the hardware of the inverter, and any change in the controller. A detailed modeling of its implementation with the inverter control is presented, and the performance of the AIP scheme is verified by simulations, and experiments. It is shown that the AIP scheme detects the islanding condition successfully, and isolates the inverter from the grid after it experiences an islanding condition.

INDEX TERMS Anti-islanding protection scheme, distributed generation, inverter, pv integration, robust droop controller.

I. INTRODUCTION

Over the past decades, renewable energy based distributed generations (DG) are increasing significantly due to the commitment of integration more environment-friendly energy resources. The DGs are connected via power electronics inverters. The virtual synchronous machine (VSM) becomes an attractive solution for controlling these inverters [1]–[4]. The VSM ensures the load sharing naturally in the same way as the conventional synchronous generator (SG) does [5]. Moreover, the VSM control for DG inverters can operate in the grid-connected mode as well as an islanded mode [6]. The operation mode of DG inverters depends upon the state of the main grid. When DG inverters experience an islanding condition (grid absent), they should be disconnected from the rest of the grid in order to avoid personal injury and hazardous operation, and may operate in the islanded mode to supply a local load. The method for detecting and responding to the islanding condition is called anti-islanding protection (AIP) scheme. A proper AIP scheme should be included either in the control of the DG inverters or in the system so that islanding conditions can be detected and the inverters can be

disconnected from the rest of the grid in time. It is a desirable feature of the AIP scheme that it should detect the islanding condition accurately and isolate the inverters from the grid as soon as possible when the inverters experience an islanding condition. According to the IEEE Standards 1457, the inverters should be disconnected within 2 s after it experiences an islanding condition [7]. Therefore, embedding an AIP with a high accuracy and less detection time is a requirement for DG inverters. There are many AIP schemes employed in the existing system [8]–[20]. The main challenges in these are the accurate detection of the islanding condition and easy implementation of the AIP scheme.

The AIP schemes can be divided into main three categories; communication-based, passive and active AIP schemes. The communication based AIP schemes detect accurately and response quickly in the islanding condition, however, this method suffers from high cost, complicated hardware, and dependence on the communication coverage of their installed location [8], [9]. The passive AIP scheme is mainly realized by employing the over-voltage/under-voltage and over-frequency/under-frequency. The passive AIP method is simple

and easy to implement, and does not have an impact on the system operation. However, they have a large non-detection zone and suffer from malfunctioning when the local loads are equal to the power supplied by the inverters [10]. In order to overcome these limitations of the passive AIP methods, the fuzzy logic, artificial neural network, decision trees have been realized. These different techniques give an accurate detection of the islanding condition, however, these schemes become more complicated and difficult in hardware realization [21]. Different active AIP schemes have been proposed in the literature such as correlation-based AIP scheme using current magnitude disturbance [22], harmonic injection method [23], grid impedance estimation method [24]. In these active AIP methods, a small disturbance is injected into the point of common coupling (PCC) to monitor the continuous change in the system parameters. The active AIP methods have a better detection accuracy compared to the passive AIP methods. The main concern of this type of AIP schemes is that these injections may impact the quality of the power supply and introduce the instability problem as well as they require additional devices to inject the disturbance signal [11], [25].

Researches have also been conducted by combining different AIP schemes to achieve a better performance. An AIP scheme based on the combination of a reactive power versus frequency droop and rate of change of frequency is presented in [26]. The scheme is designed so that the reactive power injection is of the minor scale during normal operating conditions. An apparent power-based AIP scheme has been presented in [27] where the detection is based on determining the wavelet packet transform of high-frequency sub-bands present in the d–q-axis components of instantaneous 3-phase apparent powers. This scheme considers an islanding condition if the system creates a non-periodic and non-stationary high frequency component in the apparent power waveform. The active and reactive power variation based AIP scheme is mainly the active method [10], [11], [17], [28]–[30]. In these methods, the active and/or reactive power is injected with a certain frequency into the grid. An example of such an active AIP scheme presented in [28] where the AIP method is based on 40 Hz sinusoidal reactive power injection and used a double- second order generalized integrator topology for computation of harmonic amplitude. The islanding condition is also detected based on the change of the active/reactive power variation in addition to the voltage and/or frequency variation [10], [11]. These methods work well, however, the main concern about these methods is that in an electrical island operation where the voltage and the frequency variation is much higher compared to the grid-connected operation, it causes the inverter to trip. If more inverters are connected in parallel, false trips and stability problems can be experienced. Moreover, the accuracy depends on the selection of the calibration gain K_v and K_f . It is important to execute a correct calibration of K_v to avoid overcurrent. A power line carrier based AIP scheme has been presented in [31]. This AIP scheme mainly relies on transfer trips from upstream substations through communication media, which are expensive and

time-consuming because of the infrastructure. This scheme has been improved by measuring local data only, in which the controller requires a phase-locked loop (PLL) for calculating the firing angle for the thyristor [32]. However, these schemes become more complicated and require additional devices for successful implementation.

The main contribution of this paper is presenting a novel hybrid AIP scheme for the DG inverters. The advantages of this AIP scheme to the existing solutions [8]–[20] are:

- Its easy implementation without a need for any additional sensor and power devices in DG inverters;
- The AIP scheme is a combination of both active and passive AIP method and does not rely on a communication network;
- The complicated disturbance injection method has been avoided, consequently, the risk of triggering instability and power quality issues has been eliminated;
- The AIP scheme overcomes the malfunctioning when the local loads are equal to the power supplied by the DG inverter;
- The requirements for frequency and phase measurements have been removed.

The AIP scheme detects the islanding condition based on the system parameters such as the active power, the reactive power, and the voltage magnitude mismatches. The AIP scheme detects the islanding condition for all possible operation scenarios and disconnects the inverter from the main grid after it experiences an islanding condition. A detailed operating principle with the analytical modeling of the proposed AIP scheme is presented. Time domain simulations and the experimental results are presented to validate the performance of the proposed AIP scheme for different scenarios such as giving a command signal for changing the reference power of the inverter, initiating an islanding for a case when the local load is equal to the reference power of the inverter, connecting a heavy load, and introducing a grid fault.

The rest of the paper is organized in the following. Section II describes the detailed analytical modeling and operation principle of the proposed AIP scheme. Section III presents the performance of the AIP scheme validated through simulation. Experimental results is presented in section IV. Finally, section V concludes this work.

II. ANALYTICAL MODELING AND OPERATION PRINCIPLE OF THE PROPOSED AIP SCHEME

The proposed hybrid AIP method is based on the detection of active power, reactive power and voltage mismatch, which is shown to be an alternative to the impedance variation measurement technique. The analytical modeling and its implementation presented in the following section.

A. ANALYTICAL MODELING OF THE AIP IMPLEMENTATION

Fig. 1 shows a DG inverter and its VSM controller in a general form. The inverter sends the active power, P and the reactive power, Q to the grid according to its set power P_{set} and Q_{set} . It is important to note that in this work, the inverter current

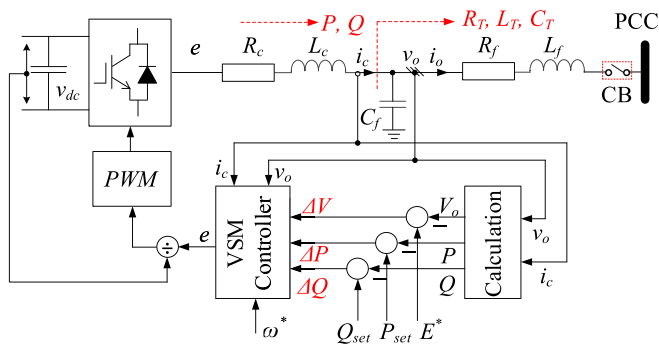


FIGURE 1. A general form of a VSM-based DG inverter and its controller.

is used to calculate the active and reactive power as shown in Fig. 1. The power of the inverter can be given by

$$P = P_{set} = \frac{V_o^2}{R_T} \quad (1)$$

$$Q = Q_{set} = V_o^2 \left(\frac{1}{2\pi f_1 L_T} - 2\pi f_1 C_T \right) \quad (2)$$

where V_o is the capacitor voltage magnitude, f_1 is the fundamental frequency, R_T , L_T and C_T are the equivalent resistance, inductance and capacitance respectively. If there are multiple DG sources connected to the PCC, (1) and (2) are still valid since each of DG source has its own equivalent R_T , L_T and C_T .

In the grid-connected mode, the grid mainly regulates the voltage and frequency, and the DG inverters transfer power to the grid based on its reference power, P_{set} and Q_{set} . However, in the islanded mode, the DG inverters take part in the voltage and frequency regulation and send power P and Q based on the connected local load, i.e., equivalent R_T , L_T and C_T . Since the inverters do not send the power according to its P_{set} and Q_{set} in the islanding condition, there is a power mismatch between the set power and actual power. This power mismatch can be given by

$$\Delta P = P_{set} - P \quad (3)$$

$$\Delta Q = Q_{set} - Q. \quad (4)$$

Eqns. (1) and (2) indicate that the power mismatch from the grid-connected mode to an islanding condition results from a change of V_o , f , and connected load, i.e., R_T , L_T and C_T . From (1) and (2), the power mismatch can be given by

$$\Delta P = \frac{2V_o}{R_T} \Delta V_o - \frac{V_o^2}{R_T^2} \Delta R_T. \quad (5)$$

$$\Delta Q = 2V_o \left(\frac{1}{2\pi f_1 L_T} - 2\pi f_1 C_T \right) \Delta V_o - \frac{V_o^2}{2\pi f_1 L_T^2} \Delta L_T - 2\pi f_1 V_o^2 \Delta C_T - V_o^2 \left(\frac{1}{2\pi f_1^2 L_T} + 2\pi C_T \right) \Delta f. \quad (6)$$

The Delta symbol Δ is used to represent a variation of the parameters from the grid-connected operation to an islanding condition, for example, the equivalent resistance is R_T in the grid-connected operation when in an islanding condition, it is $R_T + \Delta R_T$.

Both the grid-connected mode and the islanded mode, the voltage and frequency are regulated by controlling the generation of the active and reactive power, therefore, ΔV_o and Δf can be disregarded in (5) and (6). Thus, the power mismatches can be expressed as

$$\Delta P = -\frac{V_o^2}{R_T^2} \Delta R_T \quad (7)$$

$$\Delta Q = -\frac{V_o^2}{2\pi f_1 L_T^2} \Delta L_T - 2\pi f_1 V_o^2 \Delta C_T. \quad (8)$$

Detection of an islanding condition by monitoring the grid impedance variation is a very effective active AIP technique [19], [24]. The impedance variation is obtained by a perturbation method where a harmonic current ($i_{h,i}$) or voltage ($v_{h,i}$) signal is injected at the PCC, and the impedance is obtained from responses of the corresponding harmonic voltage ($v_{h,r}$) or current ($i_{h,r}$) with respect to injected signal as

$$Z_h = v_{h,r}/i_{h,i} = v_{h,i}/i_{h,r}. \quad (9)$$

The main concern is this method requires additional devices to inject the perturbation signal and more computational effort is needed in real-time impedance calculation.

Eqns. (7) and (8) indicate that the power mismatch is proportional to the grid impedance variation. As shown in Fig. 1, ΔP and ΔQ , which is equivalent to the impedance variation, can be obtained directly from the controller without injection of a disturbance signal. If the inverter is connected to the grid, P and Q follow P_{set} and Q_{set} . Hence, the power mismatch in (7) and (8) is zero, which meaning $\Delta R_T = \Delta L_T = \Delta C_T = 0$ in (7) and (8). However, during the change of operation condition from grid-connected mode to an islanding condition, ΔR_T , ΔL_T and ΔC_T will not be zero [24], resulting in a mismatch in the active power and reactive power.

The inverter usually operates under close to the unity power factor and the reactive power Q_{set} is usually set to zero when the inverter is connected to the grid. However, in an islanding condition, the inverter supplies or absorbs the reactive power depending on the connected L_T and C_T . For example, an unloaded transmission line connected to the inverter in the islanding condition generates the reactive power while an unloaded transformer absorbs the reactive power. The inverter maintains the voltage and frequency at the reference set point by absorbing or generating the reactive power and the active power. Therefore, there must be a mismatch between the set reactive power Q_{set} and the supplied reactive power Q from the inverter in an islanding condition. The reactive power mismatch is considered to be the first criterion for detecting an islanding condition. In the islanding condition, the reactive power mismatch ΔQ exceeds a threshold limit, Q_L with a

typical value of 0.1 pu, i.e., (10) is satisfied.

$$|\Delta Q| \geq Q_L \quad (10)$$

The second condition is about the mismatch of the active power. If the active power mismatch ΔP exceeds a threshold limit, P_L with a typical value of 0.1 pu, i.e., (11) is satisfied in the islanding condition.

$$|\Delta P| \geq P_L \quad (11)$$

The DG inverter supplies or absorbs the power to regulate the voltage and frequency in an island operation. If the inverter output current reaches its limit, it can no longer increase its power to maintain the voltage as a result, the voltage magnitude will tend to exceed from its operating range 0.95-1.05 pu. The voltage mismatch defined by

$$\Delta V = E^* - V_o \quad (12)$$

where E^* is the rated voltage, may exceed from the standard operating range. In severe cases, a voltage instability/collapse may occur. Hence, in addition to the power mismatch, the voltage mismatch has been considered as another condition for the AIP scheme if ΔV exceeds the threshold limit V_L , i.e., (13) is satisfied.

$$|\Delta V| \geq V_L, \quad (13)$$

The logic in the AIP scheme is set in such a way that if the condition in (10) is satisfied and together with at least one of the conditions from (11) and (13), the AIP scheme assumes the situation as an islanding condition.

B. CRITICAL CASE SCENARIO

The critical case is defined for the case when the inverter power becomes equal to the local load power in an islanding condition. Based on the discussion in the previous subsection, the AIP scheme proposed is based on the monitoring of the system parameters mismatch, therefore, it is a passive AIP scheme. Though the passive method is easy implementation, the challenge is: it cannot detect an islanding condition when the local load power, P_{load} is equal to P_{set} , i.e., $P_{set} = P = P_{load}$. Under this condition, the second criterion in (11) will not be fulfilled in an islanding condition since

$$|\Delta P| = |P_{set} - P_{load}| \approx 0 \leq P_L. \quad (14)$$

The inverter regulates the voltage in an islanding condition, therefore, the voltage stays within the limit, thus, (13) will not be satisfied as well. Since in addition to (10) at least one of the conditions from (11) and (13) need to be satisfied in the proposed AIP scheme, this method may fail to detect an islanding condition when $P_{set} = P_{load}$. In order to avoid this failure, the AIP scheme is altered to an active AIP scheme when only (10) is satisfied. An active power injection is applied in order to avoid a potential instability problem. The AIP scheme sends a command signal to the inverter for changing the active power set point. A step reduction of reference power, ΔP_{set} is applied, for which new power set point becomes $(P_{set} - \Delta P_{set})$.

Hence, the new power mismatch can be given by

$$\Delta P = (P_{set} - \Delta P_{set}) - P_{load} = -\Delta P_{set}. \quad (15)$$

ΔP_{set} should be higher than threshold limit. The active power mismatch in (11) is forced to exceed the threshold limit by giving the command for changing the active power reference of the inverter. If the inverter operates in the grid-connected mode, changing the active power reference will not lead to the threshold surpass since P will follow the power reference. Under an islanding condition, the inverter will supply the power equal to the local load power, and the inverter will not follow the command of the power reference change, ΔP_{set} . The command signal for changing the power reference from P_{set} to $P_{set} - \Delta P_{set}$ will force to have an active power mismatch equivalent $|\Delta P| = |\Delta P_{set}|$ and exceed the threshold limit. Hence, in addition to the reactive power mismatch condition of (10), the active power mismatch in (11) will be satisfied.

It can also be likely to happen in an islanding condition that the set reactive power is equal to the total connected reactive power load, i.e., $Q_{set} = Q = Q_{load}$. Under such critical case scenarios, to avoid the undetected condition, a step reduction of reference reactive power, ΔQ_{set} is applied, for which new reactive power set point becomes $(Q_{set} - \Delta Q_{set})$. Hence, the new reactive power mismatch can be given by $\Delta Q = (Q_{set} - \Delta Q_{set}) - Q_{load} = -\Delta Q_{set}$. ΔQ_{set} should be higher than threshold limit. The reactive power is forced to exceed the threshold limit by giving the command for changing the reactive power reference of the inverter. Hence, in addition to the active power mismatch condition in (11), the reactive power mismatch in (11) will be satisfied. Thus, the AIP scheme will detect an islanding condition.

C. AVOIDING A FAULT TRIGGERING

Many other cases such as a grid fault, voltage drop, frequency drop, different transient phenomena could cause a power and voltage mismatch for a short duration. The AIP should not send a false signal during those cases. In order to avoid a fault triggering during those cases, a time delay T_D with (10) and (11) is introduced. When the reactive power mismatch in (10) is satisfied for T_D time, and (11) and/or (13) are satisfied, the proposed AIP scheme considers the inverter in an islanding condition.

D. IMPLEMENTATION SUMMARY

Based on the mathematical modeling in the previous subsections, the AIP scheme can be presented through a flowchart as shown in Fig. 2 and can be implemented in a digital controller as shown in Fig. 3.

The reactive power mismatch exceeds the threshold limit Q_L for a delay time T_D . The delay time should be set according to the standard grid code requirement. In addition, the active power and/or voltage magnitude mismatch exceed their threshold limits P_L and V_L , then AIP scheme recognizes the situation as an islanding condition and the islanding detection

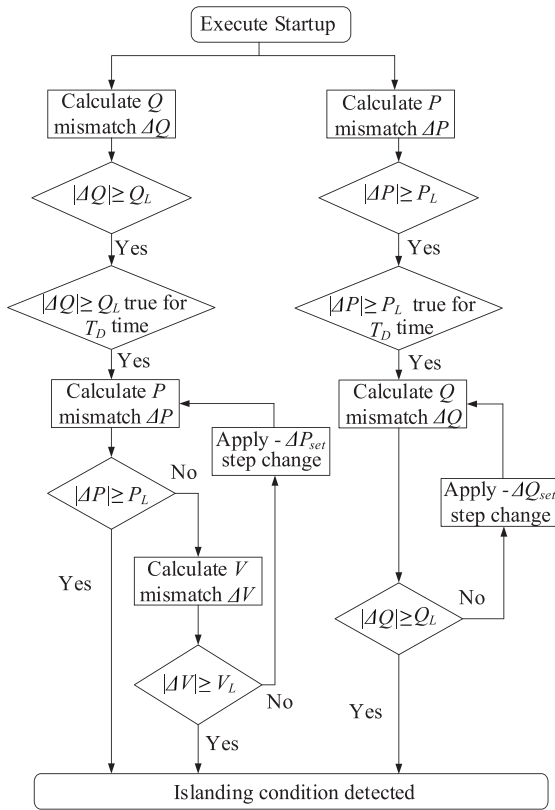


FIGURE 2. Flowchart of the proposed AIP scheme.

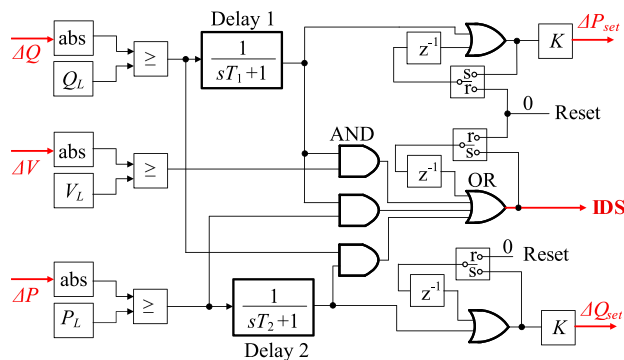


FIGURE 3. Control block diagram of the proposed AIP scheme.

signal (IDS) will be 1 (high) in in the logic circuit shown in Fig. 3.

The working procedure of the AIP scheme for the critical case scenarios is summarized in the following.

- If the reactive power mismatch exceeds the threshold limit Q_L for the duration of the delay time T_D but the active power or the voltage magnitude mismatch does not exceed the threshold limits, P_L and V_L , the AIP will send a command signal to change P_{set} and then re-calculate the ΔP . If the new power mismatch exceeds limit P_L , then AIP scheme recognizes the situation as an islanding condition.

TABLE 1. Parameters of the Investigated System

Parameters	Values
Rated apparent power, S_b	20 kVA
Rated grid voltage(L-L, RMS), V_o	208 V
Rated dc voltage, V_{dc}	500 V
Grid frequency, f	60 Hz
Inverter series inductance, L_c	1.4 mH
Inverter series resistance, R_c	0.1082 Ω
Filter capacitance, C_f	22 μ F
Filter inductance, L_f	0.2295 mH
Filter parasitic resistance, R_f	0.1082 Ω
Virtual resistance, R_v	1 Ω
Constant, K_e	5

- If the reactive power mismatch does not exceed the threshold limit Q_L for the duration of the delay time T_D but the active power mismatch exceeds the threshold limits, P_L for the duration of the delay time T_D , the AIP will send a command signal to change Q_{set} and then re-calculate the ΔQ . If the new power mismatch exceeds limit Q_L , then AIP scheme recognizes the situation as an islanding condition.

As can be seen in Fig. 3, it has three OR gates. Once the output of the OR gates becomes one (high), they hold it to high. When the inverters are reconnected to the grid after the grid is recovered, it is necessary to make the output low again. These reset blocks are used to make the output low again when the DG inverters are reconnected to the grid. When the proposed method is used, it needs to pay attention to selecting the current signal for calculating the inverter output power. As can be seen in fig. 1, it must be the inverter current, i_c which we used for calculating the active and reactive power. If the current i_o is used for calculating power, the method may not detect all islanding conditions, especially it may fail the detecting critical case scenario.

III. SIMULATION RESULTS OF THE AIP SCHEME

The AIP scheme has been implemented to a control of a DG inverter as shown in Fig. 4. The robust droop control (RDC) VSM proposed in [33] is used to control the DG inverter. Fig. 5 depicts the control stage of the RDC with embedded AIP scheme. As can be seen in Fig. 5, the required input signals ΔP , ΔQ , ΔV for implementing the AIP are readily available from the RDC controller. The RDC can be implemented in a single-phase as well as three-phase inverter without much modification in the control. Details about the mathematical modeling and operation of the RDC can be found in [33]. The control of the bidirectional $dc-dc$ converter with the energy storage is used to regulate the dc -bus voltage.

The system shown in Fig. 4 is implemented in MATLAB/Simulink in association with Sim Power System block set. The parameters of the system are given in Table 1. The value of the threshold parameters Q_L , P_L and V_L has been decided how conservative the detection method should perform. Here, the threshold limits are set to $Q_L = 0.1$ pu, $P_L = 0.1$ pu and $V_L = 0.1$ pu. The time delay T_D is set such that if

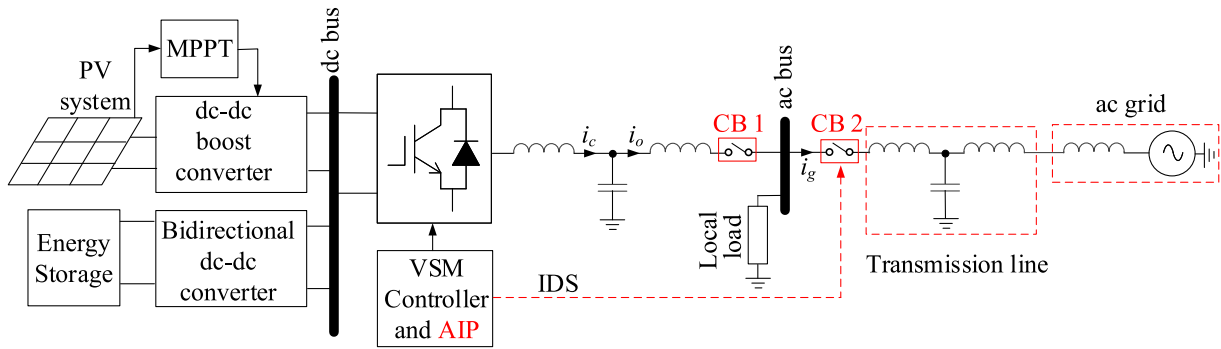


FIGURE 4. Integration of distributed generation sources through power electronics inverter.

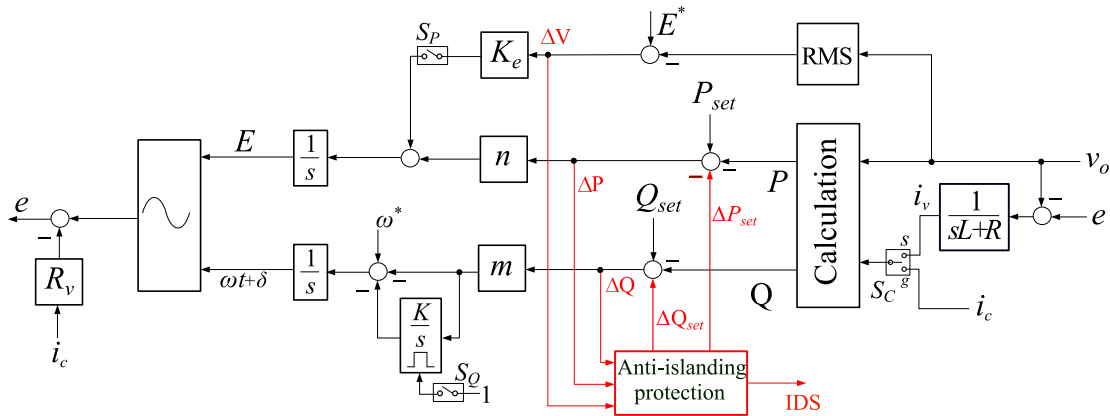


FIGURE 5. Embedded AIP scheme with the self-synchronized RDC.

the input to the transfer function is 1, the delay to reach the output 1 is 0.75 s. This means the AIP scheme detects an islanding condition in 0.75 s. Several simulations have been carried out for different scenarios to verify the effectiveness of the proposed AIP scheme. The simulation scenarios are divided into two categories, i) no false signal generated (subsection III-A and III-B) and ii) an IDS generated (subsection III-C) when an islanding occurs. The simulation scenarios are described in the following.

A. CHANGE OF THE POWER REFERENCE

The first simulation has been carried out for a normal operation with a command signal for changing P_{set} and Q_{set} . No islanding condition is initiated. The time domain responses are shown in Fig. 6(a). Initially, the inverter is operating in self-synchronization mode [33]. At 0.5 s, The grid connection circuit breaker (CB 1) has been closed and at the same time, the control mode of the VSM is changed from the self-synchronization mode to the droop-mode with $P_{set} = 0$ and $Q_{set} = 0$. The connection to the grid at 0.5 s is very smooth with a small transient. At 1 s, the real power and reactive power commands are set to $P_{set} = 15$ kW and $Q_{set} = 3$ kVar and the inverter quickly responded to the commands accurately. Another command is given at 3 s to change P_{set} from

15 kW to 10 kW. The inverter follows the given command smoothly. The IDS is 0 during this operation as shown in the bottom plot of Fig. 6(a), meaning an islanding condition is not occurred/detected.

B. A HIGH LOAD CONNECTION/DISCONNECTION AND A GRID FAULT

A load connection/disconnection and a fault have been simulated to investigate the performance of the AIP scheme.

A load change has been tested by connecting and disconnecting a 20-kW of a local load. Fig. 6(b) shows the simulation results for the case when the 20-kW load is connected to the grid at 2.5 s and disconnected at 4.0 s. During this load connection and disconnection, the inverter is acting according to its dynamic droop setting to support the grid. The IDS remains 0 and no islanding condition is detected.

Fig. 6(c) shows the simulation results for a three-phase to ground fault. The fault has been initiated at 2.5 s and cleared after 5 cycles. The power and voltage mismatch exceed the threshold limits during the fault, however, they are recovered when the fault is cleared. The IDS remains 0 and no islanding condition is detected. Hence, the AIP scheme does not generate a false signal during a grid fault.

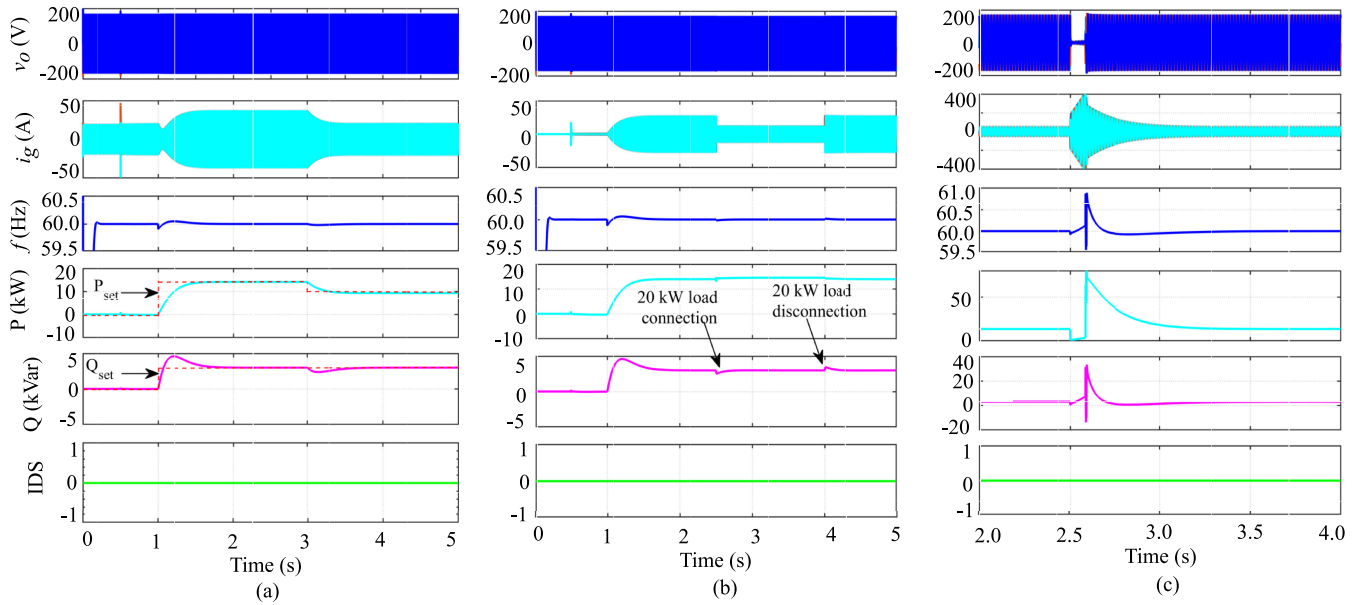


FIGURE 6. Performance of the AIP scheme: (a) Change of the Power Reference, (b) a load connection and disconnection and (c) a fault in the grid. The IDS is zero for these cases and no false signal is generated by the AIP scheme.

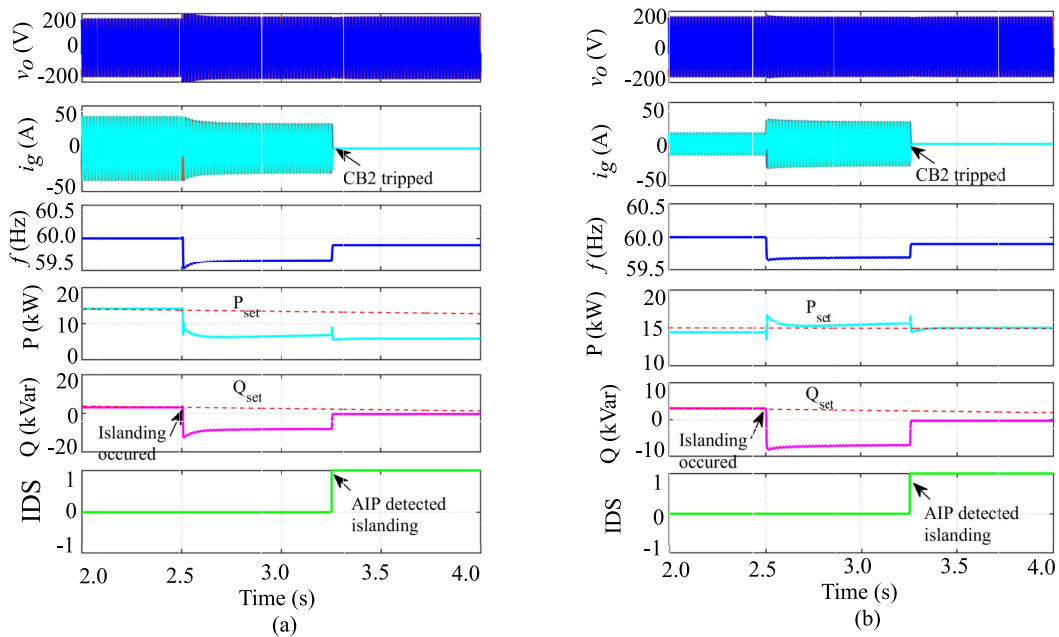


FIGURE 7. Performance of the AIP scheme: Islanding occurs when (a) the local load is smaller than P_{set} . $P_{set} = 15$ kW and $P_{load} = 5$ kW and (b) the local load is equal to P_{set} . $P_{set} = P_{load} = 15$ kW. The IDS becomes 1 for these cases and an islanding condition is detected.

C. ISLANDING OCCURRED AT DIFFERENT LOADING CONDITION OF THE LOCAL LOAD

These simulations have been carried out for different local load power while an islanding condition occurs. The first scenario is when the local load is less than the power send by the inverter. P_{set} and Q_{set} are 15 kW and 3 kVar, respectively.

The local load is 5 kW. The simulation results are shown in Fig. 7(a). Initially, the system operates in the grid-connected mode and the IDS is zero. At 2.5 s, an islanding condition occurs. As can be seen in the bottom plot of Fig. 7(a), the IDS becomes 1 at 3.25 s. The islanding condition is detected after 0.75 s of actual islanding occurred which is the specified time,

TABLE 2. Parameters of the Experimental System

Parameters	Values
Rated power, S_b	1200 VA
Rated grid voltage (L-L, RMS), V_o	208 V
Rated dc voltage, V_{dc}	400 V
Grid frequency, f	60 Hz
Filter inductance, L_c, L_f	2.2 mH
Filter capacitance, C_f	22 μ F

0.75 s set by the AIP designer. The system is designed such a way that when the IDS becomes 1, then CB 2 is opened to isolate the inverter from the rest of the grid. As can be seen, the current to the grid i_g becomes zero at 3.25 s since CB 2 is opened. After isolation at 3.25 s, the inverter operates in the stand-alone mode and supplies power to the local load.

Another simulation has been carried out for the case when the local load is equal to the power supplied by the inverter. The time domain responses are shown in Fig. 7(b). P_{set} and Q_{set} are 15 kW and 3 kVar. The local load is equal to P_{set} . In order to comply with IEEE 1547 Standard [7], in addition to a resistive load, the load network contains a 15-kVar capacitive and a 15-kVar inductive elements that cancel each other out. This creates a self-resonating island. Initially, the system is operating in the grid-connected mode, there is no violation of the threshold limit until 2.5 s. At 2.5 s, an islanding condition occurs. The reactive power mismatch $|\Delta Q|$ has exceeded the threshold limit Q_L when the active power mismatch $|\Delta P|$ and the voltage mismatch $|\Delta V|$ do not exceed the threshold limits P_L and V_L since $P_{set} = P_{load}$ and the inverter regulates the voltage. During the time from 2.5 s to 3.25 s, only the reactive power mismatch exceeds the limit Q_L . Since no violation occurs except the reactive power mismatch for 0.75 s duration, the AIP generates a command signal to change P_{set} for a step of $\Delta P_{set} = 0.125$ pu at 3.25 s. For this change of P_{set} , the active power mismatch $|\Delta P|$ exceeds the threshold limit P_L . Thus, (10), and (11) are satisfied. The IDS becomes 1 as shown in the bottom plot of Fig. 7(b). The islanding condition is detected. Hence, CB 2 operates to isolate the inverter from the rest of the grid. After isolation, the inverter operates in the islanding-mode and supplies stable power to the local load. The proposed AIP scheme works properly and can successfully detect the islanding condition.

IV. EXPERIMENTAL RESULTS

In order to further verify the performance of the proposed AIP scheme, experiments have been carried out in a single-phase small-scale setup of the system shown in Fig. 4. The inverter controller and the proposed AIP scheme has been implemented on a TMS320F28335 DSP with the sampling frequency of 10 kHz. The inverter parameters are given in Table 2. The bidirectional *dc-dc* converter regulates the *dc*-bus voltage and provides constant *dc* voltage, therefore, for simplification of the experimental setup, the PV and the energy storage are replaced by a programmable *dc* source. All the cases tested in the simulation are tested in the experiments

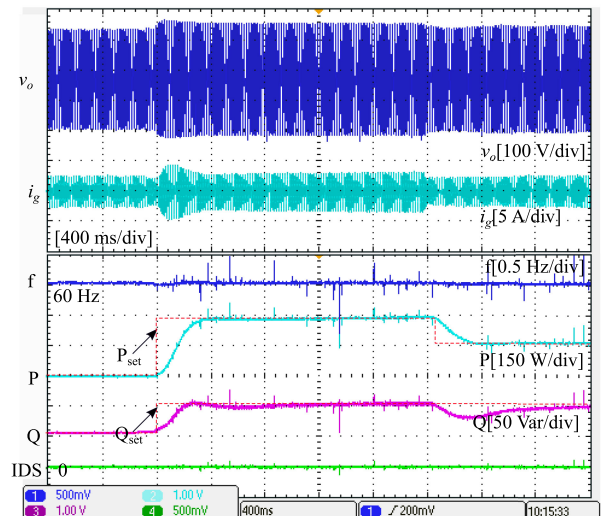


FIGURE 8. Performance of the AIP scheme in normal operation. i) The power references are set to 450 W and 50 Var at 0.80 s. ii) The active power reference is reset to 300 W at 2.8 s. The IDS is zero for this case and no false signal is generated by the proposed AIP scheme.

except the case of the ground fault due to safety concern in the Lab. The experimental scenarios are described in the following.

A. CHANGE OF THE POWER REFERENCE

The first experiment has been carried out for a normal operation and no islanding condition occurs. Command signals are given to change P_{set} in the grid-connected mode. Initially, the active power and the reactive power are set to $P_{set} = 0$ W and $Q_{set} = 0$ Var. The time domain responses are shown in Fig. 8. The real power command is set to $P_{set} = 300$ W at 0.8 s and the inverter quickly responded to the commands accurately. The inverter is exporting 300 W according to the dynamic setting. Another command signal is given to change P_{set} to 150 W. The inverter follows the given command smoothly. The IDS shown in the most bottom plot of Fig. 8 remains zero during the step change of P_{set} . The overall system performance is satisfactory and no false IDS is generated by the AIP scheme.

B. A LOAD CONNECTION/DISCONNECTION

This experiment has been carried to observe the performance of the proposed AIP scheme during a load connection and disconnection in the system. Fig. 9 shows the experimental result. As can be seen in Fig. 9(a), at 1.2 s, a 600-W local load has been connected to the system. A load disconnection event has been tested and is shown in Fig. 9(b). During this load connection/disconnection, the inverter is acting according to its dynamic droop setting to support the grid. However, the IDS remains zero and no false detection signal is generated.

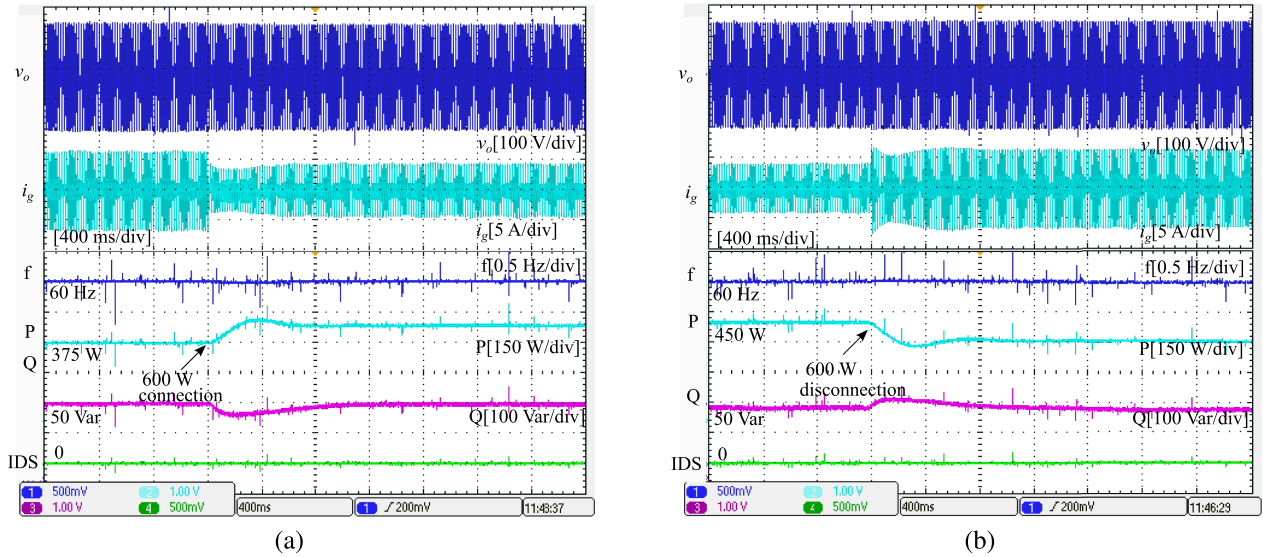


FIGURE 9. Experimental results: Performance of the AIP scheme, (a) a 600-W local load has been connected 1.2 s and (b) (a) the 600-W local load has been disconnected 1.2 s. The IDS is zero for this case and no false signal is generated by the proposed AIP scheme

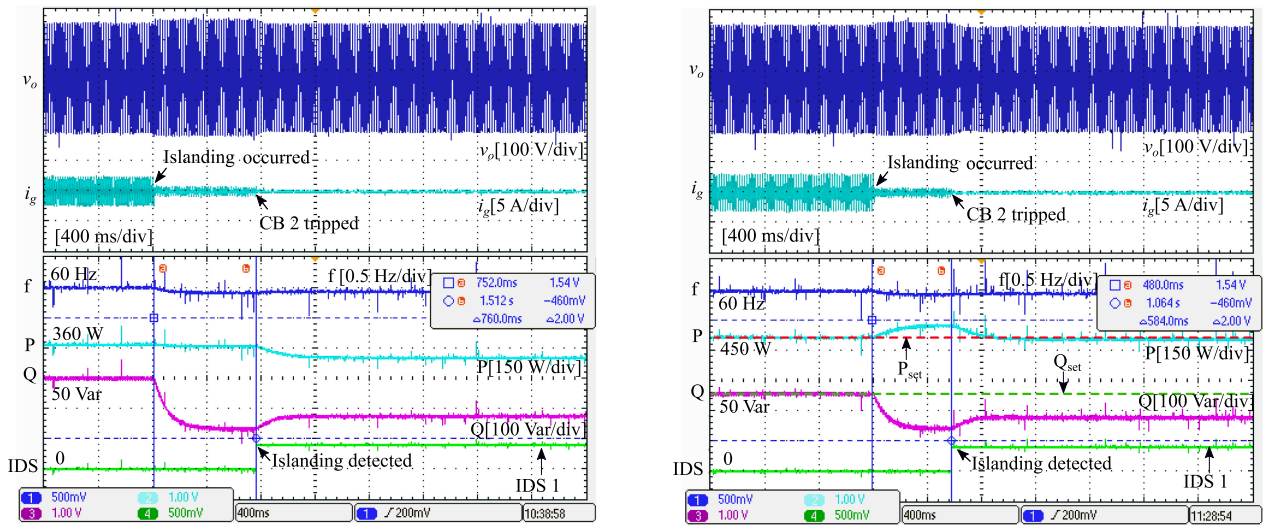


FIGURE 10. Islanding occurs when (a) the local load is smaller than P_{set} . $P_{set} = 450$ W and $P_{load} = 300$ W and (b) the local load is equal to P_{set} . $P_{set} = P_{load} = 450$ W. The IDS becomes 1 for these cases and an islanding condition is detected.

C. ISLANDING OCCURRED AT DIFFERENT LOADING CONDITION OF THE LOCAL LOAD

The first experiment has been carried for the case when the local load power is less than P_{set} of the inverter. The active and the reactive power are set to 450 W and 50 Var. The local load connected to the system is 300 W. Experimental results are shown in Fig. 10(a). The system is operating in the grid-connected mode and the IDS is zero. Though P_{set} is 450 W, the inverter is supplying this 360-W according to its droop setting in this experiments. At 0.8 s, an islanding occurs. As can be seen in the bottom plot of Fig. 10(a), the IDS becomes 1, meaning an islanding condition is detected. CB 2 is opened to

isolate the inverter from the main grid. After isolation from the grid, the inverter operates in the islanded mode and supplies power to the local load. The inverter maintains the ac bus frequency and voltage magnitude.

The next experiment has been carried out for the critical scenario when the local load is equal to the power supplied by the inverter. The experimental results are shown in Fig. 10(b). The active and reactive power are set to 450 W and 50 Var, respectively. The local load is also 450 W, i.e., $P_{set} = P_{load}$. Initially, the inverter is operating in the grid-connected mode. An islanding condition occurs at 1.2 s. The reactive power mismatch $|\Delta Q|$ has exceeded the limit Q_L when the active

power mismatch $|\Delta P|$ and the voltage mismatch $|\Delta V|$ do not exceed the threshold limits. During the delay time, only the reactive power mismatch $|\Delta Q|$ exceeds the threshold limit Q_L . The reactive power mismatch can exceed the threshold in the grid-connected mode as the VSM supports the grid by providing/consuming reactive power. Since no violation occurs except the reactive power threshold, in order to ensure it is islanding condition or not, the AIP generates a command signal to change P_{set} for a step of $\Delta P_{set} = 150$ W. If the inverter is in the grid-connected mode, the output power of the inverter will follow the new reference, however, in the islanded mode it cannot follow the reference. Here for this change of P_{set} , the active power mismatch $|\Delta P|$ exceeds the threshold limit of (11) due to the unbalanced power set point of the DG inverter and the local load. As can be seen in the bottom plot of Fig. 10(b), the IDS becomes 1 and an islanding condition is detected. CB 2 is opened to isolate the inverter from the rest of the grid. After isolation from the grid, the inverter operates in an islanded mode and supplies stable power to the local load.

V. CONCLUSION

This paper presents a novel hybrid AIP scheme for DG inverters. The implementation of the AIP scheme is based on the signal obtained from the DG inverter controller. The main advantage of this proposed AIP scheme is that it can be embedded into the control of inverters without a need of additional part in the hardware of the inverter and any change in the controller. The proposed AIP scheme does not rely on the communication network and is based on the local measurements. It detects the islanding condition based on continuous monitoring of the active power, the reactive power, and the voltage magnitude mismatch, which is shown to be an alternative to the impedance variation measurement technique. The complicated disturbance injection method in active method has been avoided, consequently, the risk of triggering instability and power quality issues has been eliminated as well as, it overcomes the malfunctioning of passive methods when the local load is equal to the power supplied by the inverter. The AIP scheme is tested under all possible islanding cases. Simulation and experimental results have verified the islanding detection function of the proposed AIP scheme.

ACKNOWLEDGMENT

The authors would like to acknowledge the open access publication support to the project "NTNU-Chinese Collaboration on Next Generation Power Electronics Converters for Renewable Energy (CoNeCt)" 309253 funded by the Research Council of Norway under the INTPART programme.

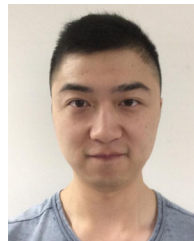
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QING-CHANG ZHONG (Fellow, IEEE) received the Ph.D. degree in control and power engineering from Imperial College London, London, U.K., in 2004 and the Ph.D. degree in control theory and engineering from Shanghai Jiao Tong University, Shanghai, China, in 2000. He is the Max McGraw Endowed Chair Professor in energy and power engineering with the Illinois Institute of Technology and the Founder and CEO of Syndem LLC, Chicago, USA. He is a fellow of IET, a Distinguished Lecturer of IEEE Power Electronics Society, IEEE Control Systems Society and IEEE Power and Energy Society, and the Vice-Chair of IFAC TC Power and Energy Systems. He served as an Associate Editor for the IEEE TAC/TIE/TPELS/TCST/Access/JESTPE. He proposed the synchronized and democratized (SYNDEM) grid architecture for the next-generation smart grid to unify the interaction of power system players with the grid for autonomous operation through the synchronization mechanism of synchronous machines, without relying on the communication network. His research interests focus on power electronics and advanced control systems theory, together with their seamless integration to address fundamental challenges in power and energy systems.



ZIJUN LYU (Student Member, IEEE) received the B.S. and M.Eng. degrees in electrical engineering from the Huazhong University of Science and Technology, Wuhan, China, in 2013 and 2015, respectively. He is currently working toward the Ph.D. degree with the Department of Electrical and Computer Engineering, Illinois Institute of Technology, Chicago, IL, USA. His research interests include renewable energy integrations, advanced control of power electronic converters and modular multilevel converters.



MOHAMMAD AMIN (Senior Member, IEEE) received the B.Sc. degree in electrical and electronic engineering from the Chittagong University of Engineering and Technology, Chittagong, Bangladesh, in 2008, the M.Sc. degree in electric power engineering from the Chalmers University of Technology, Gothenburg, Sweden, in 2011, and the Ph.D. degree in engineering cybernetics from the Norwegian University of Science and Technology, Trondheim, Norway, in 2017. From 2017 to 2019, he was a Senior Research Associate with

the Department of Electrical and Computer Engineering, Illinois Institute of Technology, Chicago, IL, USA. He is currently an Associate Professor with the Department of Electric Power Engineering, Norwegian University of Science and Technology. He was the recipient of the 2018 IEEE JESTPE First Prize Paper Award from IEEE Power Electronics Society. His research interests focus on power electronics application to power system, wind and solar energy integration, high voltage direct current (HVdc) transmission, microgrid, smart grids, and robust control theory for power electronics system.