A Fully Tunable Low-power Low-noise and High Swing EMG Amplifier with 8.26 PEF

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Abstract— In this paper, a low-noise low-power bio-potential amplifier for electromyogram (EMG) signals have designed and simulated in a commercially available 0.18 µm CMOS technology. In the first stage, a tunable band low-noise amplifier (TBLNA) is designed. In the second stage, a programmable gain amplifier (PGA) is utilized. Inside the TBLNA, by utilizing current splitting technique and current scaling technique in a current mirror operational transconductance amplifier (CM-OTA), a very good trade-off between power and noise is achieved. In addition, the second stage is designed to meet the maximum output swing. After post-layout simulation, the proposed amplifier has a variable gain between 40.2 dB to 57 dB while its high-pass and low-pass cutoff frequencies are 5-16 Hz and 1-1.75 kHz, respectively. Total input referred noise in the total bandwidth is 2.28 µV_{rms} and the total current consumption is 1.35 µA at a 1.4 V supply voltage. Therefore, the noise efficiency factor (NEF) is 2.43. By utilizing a rail-to-rail structure and a noise efficient design, the power efficiency factor (PEF) of the proposed structure is 8.26 which is relatively lower than state-of-the-art EMG amplifiers while its output swing is 1.2 V. The minimum value of the common mode rejection ratio (CMRR) and power supply rejection ratio (PSRR) are 70 dB and 73 dB, respectively. Finally, the total area consumption without pads is 0.07 mm².

Keywords— Bio-signal amplifier, EMG amplifier, low-noise, low power, PEF, high swing, input impedance

I. INTRODUCTION

Biomedical signal bandwidth ranges from few hundred miliherz (mHz) to few kilohertz (kHz) and their amplitude varies between few microvolts to few millivolts [1]. Due to their low amplitude, it is essential to amplify them in the first step. Therefore, a bio-potential amplifier is a necessary block in a biomedical signal acquisition application.

The power consumption plays a significant role in a biomedical amplifier designing. When the amplitude of input signals is relatively low, the designed circuit must have comparatively lower noise to amplify signals accurately. Dry electrodes have a high offset (about 200-300 mV) which can saturate the amplifier output. Therefore, it should be blocked. Besides, In order to have the minimum attenuation, the input impedance of the amplifier should be much larger than the electrode impedance. Furthermore, to suppress the unwanted common-mode signal for instance power-line noise, the proposed biomedical amplifier should have high CMRR and PSRR [2].

Due to the mismatch, process and temperature variation, a tunable bandwidth amplifier is required. Also, the amplitude of captured EMG signals is different according to the type of the electrode and its location. Thus, a tunable gain amplifier makes the amplifier compatible to all kind of electrodes [3].

A fully tunable amplifier was presented in [4] which could amplify different biomedical signals like neural, EEG,

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ECG and EMG. Although these systems can generally amplify different biomedical signals, they do not have a good NEF and PEF since they consume much power than a single-purpose circuit.

In this article, a fully tunable amplifier, for EMG recording with minimum stages in order to minimize the power consumption, is proposed. Besides, each stage is designed to have a rail-to-rail output swing in order to minimize the required V_{DD} . Furthermore, different low power and low noise techniques are used to reach a low NEF and PEF with rail-to-rail output swing.

In order to compare the performance of biomedical amplifiers, NEF and PEF are two important parameters. By decreasing V_{DD} , PEF can be reduced but it will be at the cost of limiting the output swing. In [5] CM-OTA is used which had a high output swing, but the total current consumption was high. Output transistors were biased in strong inversion (SI) in order to reduce the noise and cascode transistors were used in output branch to increase the open-loop gain. Consequently, this design led to the use of a high V_{DD} . Current scaling technique led to noise and power consumption in folded cascode topology [6], [7] at the cost of reduced effective transconductance (G_{meff}). In order to boost G_{meff} , a transistor is cascoded by the input transistor and a source degenerated current mirror is utilized [6]. Furthermore, a current splitting and source degeneration resistors are utilized in [7] to boost G_{meff} . In both structures, a high V_{DD} is required. Although these structures could achieve a good NEF, their PEFs are relatively high because of utilizing a high V_{DD} .

The CM-OTA with a parallel current source was introduced to increase the gain [8]. The final open-loop gain was approximately 60 dB which cause undesirable gain error for applications with 40 dB closed-loop gain. In this article, in order to have a relatively low NEF and PEF at the same time, this structure is optimized by current scaling for EMG signal acquisition with same noise and less current consumption.

II. FULLY TUNABLE EMG AMPLIFIER

The structure of a fully tunable amplifier which consists of a TBLNA and a PGA, is proposed in Fig. 1. This structure is optimized for EMG acquisition applications with a tunable bandwidth and gain. The TBLNA has a very low noise and the system bandwidth is controlled by this stage. The total gain is programmable by the second stage (PGA). Besides, second stage is designed to derive a 10 pF load capacitor. Because of the wide range of the signal amplitude, a high dynamic range and variable gain is required. The gain of the first stage has been fixed at 38 dB. The final combination of these two stages gives a programmable gain between 40.2 to 57 dB. In the proposed structure, the lower cut-off frequency can be tuned between 5-16 Hz and the higher cut-off frequency can be tuned between 1 kHz and 1.75 kHz.

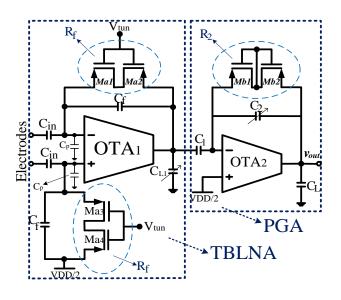


Figure1. Schematic of fully tunable EMG amplifier

A. TBLNA

The TBLNA topology is based on capacitively-coupled amplifiers (CCAs) which were introduced in [5]. The capacitive coupled structure is chosen in order to block the DC offset of electrodes. Mid-band gain, lower cut-off and higher cut-off frequencies are $G_1 = C_{in}/C_f$, $f_{L1} = 1/2\pi R_f C_f$ and $f_{H1} = G_{m1}/2\pi C_{L1}G_1$.

To reach the minimum gain, the C_{in} is chosen 8 pF and C_f is 0.1 pF. C_{in} and C_f are implemented by the only available MIMCAP (1fF/µm²) in the technology. Also, in order to minimize the noise effect of R_f [2]:

$$\frac{C_{L1}}{c_{in}} \ll \frac{2f_{H1}}{3f_{L1}}$$
 (1)

In designing EMG amplifier, the f_L is about few hertz. As a result, the noise contribution of R_f is negligible. Therefore, in this structure, the lower cut-off frequency is tuned by R_f . The R_f is implemented by a tunable pseudo resistor which can be controlled by V_{tune} . As long as Eq. (1) is satisfied, the dominant part of the input-referred noise of the TBLNA ($\overline{V_{nl,TBLNA}^2}$) is due to the input-referred noise of the OTA₁ ($\overline{V_{nl,OTA1}^2}$). By considering the parasitic capacitors and other capacitors, the total input-referred noise can be calculated according to [5]:

$$\overline{V_{n\iota,TBLNA}^2} = \frac{(c_{in} + c_f + c_p)^2}{c_{in}^2} \overline{V_{n\iota,0TA1}^2}$$
(2)

According to the equation above if C_{in} is comparatively higher than C_f and C_p , the total input-referred noise is the noise of the OTA₁. But, higher C_{in} leads to higher area consumption. In addition, this value will determine the input impedance. Decreasing input impedance leads to signal attenuation which is a crucial problem when the input signal amplitude is so small. Thus, in order to have a good tradeoff between noise, area consumption and input impedance the C_{in} is chosen 8pF. This value is the minimum in comparison with other works, which ensure an acceptable value for the input impedance. In order to reduce the area consumption, another stage is usually utilized to control the higher cut-off frequency for LFP amplifiers, which leads to higher power consumption. EMG signals usually have much higher bandwidth (up to 2 kHz). By eliminating additional stage, in the proposed structure, the higher cut-off frequency is tunable by the C_{LI} . This capacitor is implemented by three capacitors and two switches, and the gain value can be programmed in four steps. The design strategy was influenced by a tradeoff between power, area and complexity.

B. PGA

In the second stage, a conventional PGA [9] is utilized (Fig. 1). Although this structure has a low-frequency distortion, this distortion is negligible in the bandwidth of EMG amplifiers. The PGA gain can be set by the ratio between the input capacitor (C_1) and feedback capacitor (C_2). The feedback capacitor is programmable by two bits. The bandwidth of the whole system is controlled with the TBLNA. The lower cut-off frequency of the PGA ($1/2\pi R_2 C_2$) should be much smaller than the TBLNA. That is why, the R_2 is much bigger than R_f . R_2 is a fully balanced pseudo resistor. Besides, the bandwidth of PGA should be much bigger than first stage.

III. OTA DESIGN

The schematic of the OTA₁ with each branch current is depicted in Fig. 2. The current of output transistors are designed to be 1/16 of input transistors to minimize the input-referred noise. Each input transistor current (I_B) is 400 nA and the total current consumption is 2.125 I_B . Since the output current is very small, output impedance is relatively high. As a result, more than 85 dB open-loop gain is achieved. PMOS input transistor with large W and L are utilized to minimize the flicker noise. Also, M_1 and M_2 are biased in deep sub-threshold region to achieve highest g_m/I_D .

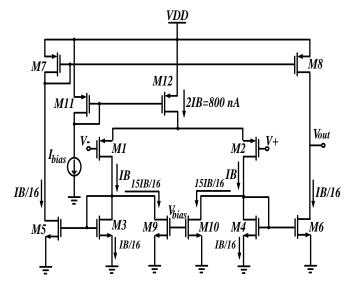


Figure 2. Schematic of the proposed OTA for TBLNA

TABLE I. OPERATING POINT FOR TRANSISTOR IN THE OTA1

Devices	$W/L(\mu m)$ $I_D(nA)$		$gm/I_{D}\left(V^{\text{-}1}\right)$	Operating region	
M _{1,2}	150/1	400	27.12	Sub-threshold	
M3-6	0.5/20	25	16.6	MI	
M7,8	2/20	25	16	MI	
M9,10	1.1/20	375	8.5	Near SI	

Output transistor noise contribution and $M_{3,4}$ can be minimized by decreasing their g_m/I_D at the cost of overdrive voltage which is not desirable in this design. Therefore $M_{3.8}$ are biased in moderate inversion (MI). Besides, in order to boost the current scaling accuracy, $M_{9,10}$ are biased just below the SI region. The transistors dimensions and their operating region are reported in TABLE I.

Since the proposed structure has a rail-to-rail swing, the same structure as it's shown in Fig. 2 with different dimension and bias is used in the second stage also. The second stage in terms of noise is much more relaxed thanks to the gain of the first stage, but in order to drive a 10 pF load and minimize the amplifier tracking error, a high G_{meff} is required. The maximum PGA gain is 10 and the highest cut-off frequency is 1.75 kHz. Therefore, according to equation (3) G_{meff2} should be bigger than 11 µS.

$$\frac{G_{meff2}}{2\pi \times 10p \times 10} >> 1.75 \, kHz \tag{3}$$

The current of each input transistor is designed 175 nA and the current scaling ratio is 1/7. Accordingly, the current of $M_{3,4}$ are 25 nA. In addition, each output branch consumes 75 nA. The total current consumption of the second stage is 500 nA. The dimension of transistors and region of operation are written in TABLE II. G_{meff2} is 13.6 µS in the designed amplifier.

IV. SIMULATION RESULTS

The proposed fully tunable EMG amplifier is designed in a commercially available 0.18 μ m CMOS Technology. The area consumption is 0.07 mm² without pads and the layout is shown in Fig. 3. Total current consumption is 1.35 μ A at a 1.4 V supply voltage. The mid-band gain of the first stage is 38 dB and total gain is programmable between 40.2 dB and 57 dB with four steps.

Devices W/L(µm)		ID(nA)	gm/I _D (V ⁻¹)	Operating region	
M1,2	60/1	175	27	Sub-threshold	
M3,4	0.5/20	25	16.9	MI	
M5,6	3(0.5/20)	75	16.9	MI	
M7,8	3/10	75	16.3	MI	
M9,10	3/20	150	16	MI	

TABLE II. OPERATING POINT FOR TRANSISTOR IN THE OTA2

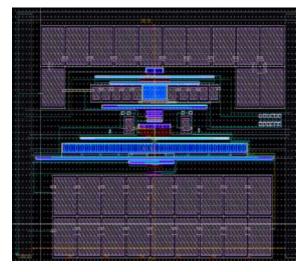


Figure 3. Layout of the EMG amplifier (192 μ m× 362 μ m)

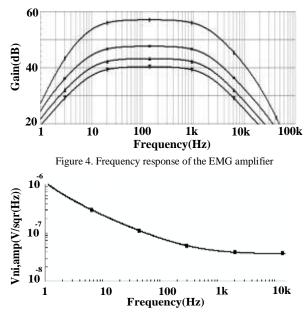


Figure 5. Input-referred noise spectra of the EMG amplifier

In Fig. 4, the output frequency response of the proposed amplifier with different gain is depicted. As the R_f value is variable with V_{tune} , the lower cut-off frequency is tunable from 5 to 16 Hz. Furthermore, higher cut-off frequency is variable with four steps between 1 kHz to 1.75 kHz. The total input-referred noise of the proposed EMG amplifier ($V_{ni,amp}$) is 2.28 μ V_{rms} in the amplifier bandwidth and the noise is shown in Fig. 5. NEF and PEF for the system are 2.43 and 8.26, respectively with 1.2 V_{p-p} output swing.

A Monte Carlo simulation has been carried out to predict the robustness of the proposed circuit under process and mismatch variation. The CMRR of the proposed amplifier is depicted in Fig. 6 for 100 runs under mismatch and process variation. The open-loop gain mean value of OTA₁ and OTA₂ are 85 dB and 79 dB, respectively. In addition, the CMRR and PSRR are higher than 70 dB and 73 dB, respectively. The proposed fully tunable amplifier is compared to the state-of-the-art amplifiers in the TABLE III. It should be noted that most of the area is consumed by the capacitor. That is exactly why, the area consumption in [4] is much less. Their MIMCAP density is 4 fF/µm².

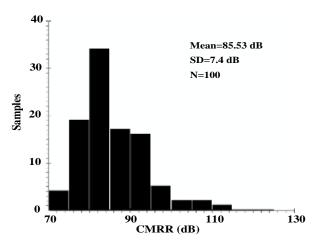


Figure 6. Mont Carlo simulation (100 runs) of CMRR at 50 Hz

Parameter	2011 [3]	2018 [10]	2017 [4]	2015[11]	This work
Technology	0.18 µm	0.18 µm	0.18 µm	0.18 µm	0.18 µm
Bio-signal-Type	Neural	Bio-potential	Multiple	EMG	EMG
Tunable Amplifier	Partial	NO	Full	Partial	Full
V _{DD} (V)	1.8	1.8	1.8	1.8	1.4
Output swing	1 V _{P-P}	1.4 V _{P-P}	N/A	N/A	1.2 V _{P-P}
Power (µW)	20.8	4.07	5.74	7.5	1.89
Gain (dB)	52.5 - 57.5	39.75	38 - 72	43 - 58	40.2 - 57
f _L (Hz)	4/300	0.3	0.5 - 300	0.65 - 3	5 - 16
f _H (Hz)	10 k	4.4 k	150 – 10 k	1 k	1k – 1.75k
V (V)	2.6	3.19	2.98	4	2.28
$V_{ni,amp} \left(\mu V_{rms} \right)$	(0.5 Hz - 50 kHz)	(1 Hz – 10 kHz)	(1 Hz – 4.5 kHz)	(4 Hz – 1 kHz)	(5 Hz – 1.75 kHz)
NEF	3.38	2.78	3.46 *	9.73	2.43
PEF	20.2	13.91	16.76 *	170	8.26
Max.signal (THD1%)	1 V (output)	14.86 mV _{p-p}	10 mV _{p-p}	N/A	10 mV _{p-p}
Cin	10 pF	15 pF	9.6 pF	9.6 pF	8 pF
CMRR (dB)	88	76	72	70	> 70
PSRR (dB)	85	77.6	81.7	80	>73
Area (mm ²)	0.061	0.058	0.0228	N/A	0.07
Sim./Meas.	Post layout sim.	Post layout sim.	Meas.	Meas.	Post layout sim.

TABAL III. BIO-SIGNAL AMPLIFIER PERFORMANCE COMPARISON

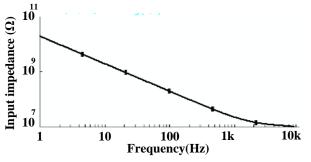


Figure 7. Input impedance of EMG amplifier

According to TABLE III, the proposed structure has the lowest PEF because of the rail-to-rail structure which lead to use a low V_{DD} while the structure is noise efficient. As it's shown to Fig. 7, the input impedance at 50 Hz is 40 M Ω . Since the input capacitor specifies the input impedance and it is less than state-of-the-art amplifiers, this structure has the highest input impedance.

V. CONCLUSION

In this article, a fully tunable amplifier for EMG signal acquisition is proposed. In order to minimize the power consumption, the proposed structure is utilizing the minimum number of stages. The gain is programmable between 40.2 and 57 dB and the bandwidth is adjustable. By utilizing current scaling technique in a suitable structure, the proposed amplifier has a lowest PEF in comparison with state-of-the-art with a high output swing. Finally, the Monte Carlo simulation proves the good performance of the amplifier under process and mismatch variation.

References

 $\begin{bmatrix} 1 \end{bmatrix} R. F. Yazicioglu, P. Merken, R. Puers and C. Van Hoof, "A 60 \ \mu W 60 \ nV/\sqrt{Hz} Readout Front-End for Portable Biopotential }$

Acquisition Systems," *IEEE J. Solid-State Circuits*, vol. 42, no. 5, pp. 1100-1110, May 2007.

- [2] R. R. Harrison, "The Design of Integrated Circuits to Observe Brain Activity," in *Proceedings of the IEEE*, vol. 96, no. 7, pp. 1203-1216, July 2008..
- [3] H. Rezaee-Dehsorkh, N. Ravanshad, R. Lotfi, K. Mafinezhad and A. M. Sodagar, "Analysis and Design of Tunable Amplifiers for Implantable Neural Recording Applications," in *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 1, no. 4, pp. 546-556, Dec. 2011.
- [4] H. Bhamra, J. Lynch, M. Ward and P. Irazoqui, "A Noise-Power-Area Optimized Biosensing Front End for Wireless Body Sensor Nodes and Medical Implantable Devices," in *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 25, no. 10, pp. 2917-2928, Oct. 2017.
- [5] R. R. Harrison and C. Charles, "A low-power low-noise CMOS amplifier for neural recording applications," *IEEE J. Solid-State Circuits*, vol. 38, no. 6, pp. 958–965, Jun. 2003.
- [6] W. Wattanapanitch, M. Fee, and R. Sarpeshkar, "An energyefficient micropower neural recording amplifier," *IEEE Trans. Biomed. Circuits Syst.*, vol. 1, no. 2, pp. 136–147, Jun. 2007.
- [7] C. Qian, J. Parramon, and E. Sanchez-Sinencio, "A micropower lownoise neural recording front-end circuit for epileptic seizure detection," *IEEE J.Solid-State Circuits*, vol. 46, no. 6, pp. 1392– 1405, Jun. 2011.
- [8] Libin Yao, M. Steyaert and W. Sansen, "A 0.8-V, 8-/spl mu/W, CMOS OTA with 50-dB gain and 1.2-MHz GBW in 18-pF load," ESSCIRC 2004 -29th European Solid-State Circuits Conference (IEEE Cat. No.03EX705), Estoril, Portugal, 2003, pp. 297-300.
- [9] X. Zou, X. Xu, L. Yao, and Y. Lian, "A 1-V 450-nW fully integrated programmable biomedical sensor interface chip," *IEEE J. Solid-State Circuits*, vol. 44, no. 4, pp. 1067–1077, Apr. 2009.
- [10] Sanjay, R., V. Senthil Rajan, and B. Venkataramani. "A low-power lownoise and high swing biopotential amplifier in 0.18 μm CMOS." Analog Integrated Circuits and Signal Processing 96, no. 3 565-576, 2018.
- [11] H. Bhamra *et al.*, "A 24 μW, batteryless, crystal-free, multimode synchronized SoC 'bionode' for wireless prosthesis control," IEEE J. Solid-State Circuits, vol. 50, no. 11, pp. 2714–2727, Nov. 2015.