A Power Efficient Low-noise and High Swing CMOS Amplifier for Neural Recording Applications

Kebria Naderi, Erwin Shad, Marta Molinas, Ali Heidari

***Abstract*— In this paper, a power efficient, low-noise and high swing capacitively-coupled amplifier (CCA) for neural recording applications is proposed. The use of current splitting technique and current scaling technique in a current mirror operational transconductance amplifier (CM-OTA) has lead to a very good trade-off between power and noise. The presented architecture is simple, without cascode transistor while it has more than 80 dB open-loop gain without extra power consumption. As a result, the proposed strucuture has a better power efficiency factor (PEF) and output swing in comparison with previous reported architectures is increased to the $2V_{ov}$ below the maximum supply voltage. In order to reduce flicker noise and achieve better trade-off between the power and noise, PMOS transistors with an optimum size have been utilized which operate in sub-threshold region. The amplifier is designed and simulated in a commercially available 0.18 µm CMOS technology. Monte Carlo simulations for process and mismatch have been carried out. The gain of the proposed amplifier is 39.22 dB in its bandwidth (3 Hz - 5 kHz). Total input-referred noise is 3.03 μV_{rms} over 1 Hz - 10 kHz. The power consumption of the amplifier is 2.98 µW at supply voltage of 1.4 V. The noise efficiency factor (NEF) and PEF are 2.4 and 8.06, respectively. The output swing is about 1.16 V. It means the proposed amplifier can tolerate up to 13.2 mV peak-to-peak input signal while its total harmonic distortion (THD) is less than 1%.**

***Index terms*— bio-signal amplifier, neural amplifier, low-noise, low power**

I. Introduction

Neural signals have wide range amplitude from a few tens of micro-volts to several milli-volts and their bandwidth range is from 10 - 200 Hz for local field potential (LFP) and 300 Hz - 5 kHz for action potential (AP) [1]. In this case, one of the significant blocks on neural recording system is a suitable amplifier for such a low frequency and amplitude signals.

The power consumption is a crucial parameter to design a neural amplifier. The amplitude of neural signals is low. Therefore, for clean signal acquisition, the amplifier must have sufficiently low input-referred noise. The electrode-tissue has DC offset voltage, and this must be blocked by on chip high pass filter. The designed structure must be small enough to be implantable. In addition, the amplifier should have a high CMRR and a PSRR to minimize interference from power line (50/60 HZ) and power supply [1]. Our purpose is to design a high-performance amplifier. Specially we focused on NEF and PEF improvement while we increase output swing. In this article, a current mirror OTA with parallel current source is optimized by current scaling technique for a neural amplifier. As a result, the proposed structure reaches a high output swing while it has less PEF in comparison with state-of-the-art neural amplifiers.

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II. Capacitively-coupled amplifier

The CCA architecture (Fig. 1) has been presented first in [2]. Neural signal is coupled with input capacitors (C_{in}) and therefore DC offset voltage caused by electrode tissue will be blocked. Due to eliminating DC level of the signal by filtration, the amplifier has rail-to-rail common mode input [3]. Combination of pseudo resistor (R_f) and feedback capacitor (C_f) define the low-frequency cutoff ($f_L = 1/2\pi R_f C_f$).

R_f has been implemented by two back-to-back PMOS transistors that results high resistance in a low space and added negligible noise and a small parasitic capacitor. Also, it has good linearity and it is possible to achieve more linearity if multiple pseudo resistor connects in series if it's desired. More linearity will be achieved since in series connection, a lower voltage drops across each R_f [4]. Higher R_f results in lower loading effect. Using the R_f also sets input and output common mode voltage on VDD/2. If the DC gain of the OTA is high enough, the midband gain of amplifier (A_M) will be set with ratio of input capacitor to feedback capacitor (C_{in}/C_f). This ratio is about 31.25dB which defines amplifier gain. High cutoff frequency is determined with dominant pole of OTA and bandwidth is approximately calculated by $f_H = G_m/2\pi C_L A_M$, where C_L is load capacitance and G_m is transconductance of OTA. The R_f contribution noise is minimized by satisfying equation (1) [1].

$$\frac{C_L}{C_{in}} \ll \frac{2f_H}{3f_L} \tag{1}$$

Thus, input-referred noise of the amplifier ($\overline{V_{ni,amp}^2}$) is given by:

$$\overline{V_{ni,amp}^2} = \frac{(C_{in}+C_f+C_p)^2}{C_{in}^2}\overline{V_{ni,OTA}^2} \tag{2}$$

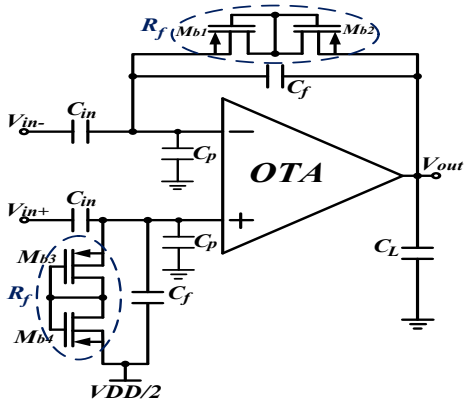

Figure1. Capacitively coupled neural amplifier

Where C_p is the OTA input parasitic capacitance and $\overline{V_{ni,OTA}^2}$ is the OTA input-referred noise. Therefore, in order to reduce $\overline{V_{ni,amp}^2}$, the OTA noise must be minimized. By increasing the C_{in}, $\overline{V_{ni,amp}^2}$ will be decrease in the cost of area consumption. On the other hand, with increasing the C_{in}, the input impedance has been lessened and the input signal will be attenuated. Also, with a fixed A_M, by increasing C_{in}, the CMRR will become higher. Therefore, there is a trade-off between these parameters.

III. LOW-POWER LOW NOISE AND HIGH SWING OTA DESIGN

A. OTA topology

Choosing an appropriate architecture is one of the most important part that should be considered. Folded cascode (FC) topology can have good open loop gain with one stage. Using current scaling technique in FC leads to a good tradeoff between noise and power [5]. By Using a large current scaling of 16:1 (input bias current: output branch current), the total current consumption got reduced and also, the noise effect of output branch transistors on input got decreased. But, utilizing this technique will lead to effective transconductance ($G_{m,eff}$) attenuation. In order to solve this problem, one cascode stage and source degeneration resistors have been utilized which increased area and voltage headroom. Additionally, in [6] recycling FC with current scaling technique for increasing $G_{m,eff}$ has been presented which was relatively noise efficient. However, in this structure, a large source degeneration resistor has been used which leads to a high voltage drop across it (about 600 mV). Although [5, 6] are the best reported designs according to trade-off between noise and power they have a large area consumption and a high supply voltage.

A current mirror OTA has wide output swing, although its open loop gain is low. The Cascode transistors are added to the output branch in order to increase the gain while the output swing is limited [2]. Since this topology totally consumes $2I_{tail}$, it is not power efficient.

The topology of CM-OTA with shunt current source was introduced first in [7] to enhance the DC gain and it was utilized in switched capacitor applications.Although this structure had rail-to-rail output swing, its gain was less than

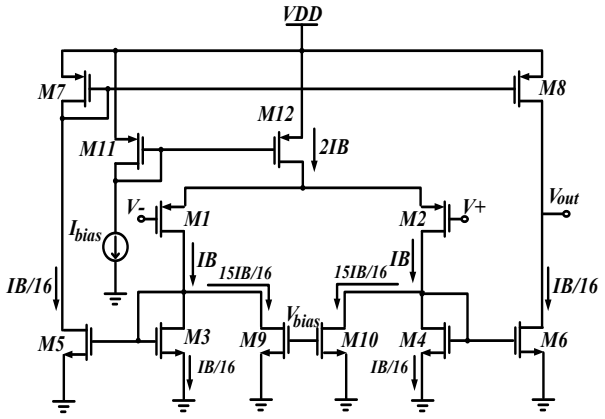

Fig.2 Schematic of the proposed OTA

TABLE I. OPERATING POINT FOR TRANS. IN THE OTA

Devices	W/L(μm)	I_D (nA)	gm/I_D (V^{-1})	Operating region
$M_{1,2}$	200/1	1000	25.9	Sub-threshold
M_{3-6}	1/20	62.6	15.9	MI
$M_{7,8}$	1/5.5	62.6	14.4	MI
$M_{9,10}$	3.75/20	937.4	10	Near SI

60 dB which might led to high gain error in many applications. In addition, this design is not power efficient.

In Fig. 2, the proposed modified CM-OTA and each branch current are shown. In this article, by utilizing the current scaling technique, the DC gain is enhanced more than 10 times with 1.4 times less power consumption and the same noise. Input transistors current I_B is set to 1uA. The small signal and large signal currents of M_1 and M_2 are split by bottom current source ($M_{9,10}$). Moreover, the small signal current goes through $M_{3,4}$ and it is mirrored to output. The $M_{9,10}$ are designed with $15I_B/16$ and only $I_B/16$ passes through $M_{3,4}$. Therefore, each output branch consumes only $I_B/16$. Current scaling of 16:1 ($I_{1,2}$:I_{3-8}) have been utilized to lessen the noise effect of M_{3-8} at the input. Besides, the total current consumption is decreased by this technique. Furthermore, due to the low current which goes through output branches, the output resistance is quite large. Accordingly, the low frequency gain is relatively high. Thus, the need for cascode transistor in order to boost DC gain is eliminated.

B. Optimum sizing of OTA

A flicker noise ($1/f$ noise) is the first concern in low-frequency and low-noise amplifiers. PMOS transistors have lower 1/f noise in comparison with NMOS transistors. Thus, PMOS differential pair is used at inputs. The flicker noise for each transistor in differential pair is given by

$$\overline{V_{fn}^2} = \frac{k_p}{c_{ox}^2.W_{1,2}.L_{1,2}} \times \frac{1}{f} \qquad (3)$$

where K_P is the flicker noise coefficient, C_{ox} is oxide capacitances per unit area, $L_{1,2}$ and $W_{1,2}$ are length and width of transistor. By enlarging ($L_{1,2} \times W_{1,2}$), the flicker noise decreases at the cost of bigger area consumption. Also, with increasing ($L_{1,2} \times W_{1,2}$), parasitic capacitor C_P will be increased.

Table II. PERFORMANCE COMPARISON WITH CAPACITIVELY COUPLED BIO-SIGNAL AMPLIFIER

Parameter	2007 [5]	2011 [6]	2011 [8]	2013 [9]	2018[10]	This work
Technology	0.5 µm	0.6 µm	0.18 µm	0.18 µm	0.18 µm	0.18 µm
V_{dd} (V)	2.8	2.8	1.8	1.8	1.8	1.4
Power (µW)	7.56	2.4	7.92	1.5	4.07	2.98
Gain (dB)	40.85	39.4	39.4	40.17	39.75	39.22
Bandwidth (Hz)	45 – 5.32 k	0.36 – 1.3 k	10 – 7.2 k	8 m – 1.68 k	0.3 – 4.4 k	3 – 5 k
$V_{ni,amp}$ (μV_{rms})	3.06	3.07	3.5	2.99	3.19	3.03
NEF	2.67	3.09	3.35	2.6	2.78	2.4
PEF	19.96	26.73	20.2	12.17	13.91	8.06
Max.signal (THD 1 %)	7.3 mV_{p-p}	10 mV_{p-p}	5.7 mV_{p-p}	5.9 mV_{p-p}	14.86 mV_{p-p}	13.2 mV_{p-p}
CMRR (dB)	66	66	70.1	70	76	> 70
PSRR (dB)	75	80	63.8	N/A	77.6	> 77
Area (mm^2)	0.16	0.13	0.065	N/A	0.058	0.046
Sim./Meas.	Meas.	Meas.	Meas.	Sim.	Post-layout Sim.	Post-layout Sim.

According to (2), the input-referred noise of overall circuit will be increased. However, till C_p is much smaller than C_{in}, this effect will be negligible. The total input-referred thermal noise can be approximately calculated by (4).

$$\overline{V_{ni,OTA}^2} \cong \frac{8kTc}{g_{m1,2}}\left(1+\frac{g_{m3,4}}{g_{m1,2}}+\frac{g_{m5,6}}{g_{m1,2}}+\frac{g_{m7,8}}{g_{m1,2}}+\frac{g_{m9,10}}{g_{m1,2}}\right) \quad (4)$$

Where k is Boltzmann's constant, T is the absolute temperature, g_{mi} is the transconductance of its transistor and c is approximately 2/3 though it varies slightly according to the biasing of the transistor. According to different operation regions of transistors, transconductance to drain current ratio (g_m/I_D) is different. $M_{1,2}$ are designed in sub-threshold region to maximize $g_{m1,2}$. In this case, the total input-referred noise decreases. Additionally, apart from reducing the noise, considering to small $V_{ov1,2}$, mismatch of differential pair is permissible. To attain maximum possible ratio of g_m/I_D (about 27 V^{-1}), the transistor can be designed in deep sub-threshold region but at the cost of increasing the dimensions of transistors and parasitic capacitors. $g_{m1,2}/I_{D1,2}$ ratio is optimized by setting it on 26 V^{-1}.

In order to reduce the noise effect of $M_3 – M_8$, the $g_{m3 – 8}$ must be significantly smaller than $g_{m1, 2}$. With designing M_3-M_8 in the SI region, the g_{m3-8} become minimum. But it costs of increasing the over drive voltage which leads to decrease the output swing. The $M_{3,4}$ and M_7 are diode connected and with reducing $g_{m3,4}$ and g_{m7}, their equivalent impedance seen by the gate of them will be increased. As a result, the non-dominating pole of the circuit becomes effective and it might reduce the phase margin (PM) significantly. In order to have a better balance between noise with phase margin and swing, M_{3-8} are designed in the moderate inversion (MI) region. Regarding the relatively high current of the M_9 and M_{10}, the contribution of them in input-referred noise is high. Therefore, $M_{9,10}$ are at the border of MI and SI region. By this low ratio of g_m/I_D, their effect on input-referred noise is reduced. In addition, the high value of the over drive voltage is the reason of increasing the accuracy of the current scaling. The table I illustrates the main transistors operating points.

IV. SIMULATION RESULTS

The proposed amplifier was designed and simulated in a commercially available 0.18 µm CMOS technology. The layout of the proposed amplifier is depicted in Fig. 3. The capacitors C_{in} and C_f are implemented by MIM capacitors. The proposed amplifier occupies 0.046 mm^2 (218 µm×215 µm) area and consumes 2.13 µA current from a 1.4 V supply. The simulated frequency response of neural amplifier is shown in the Fig. 4. The midband gain is 39.22 dB, -3 dB low and high cutoff frequencies are 3 Hz and 5 kHz for a load capacitance of 7 pF.

The input-referred noise is shown in Fig. 5. Simulations represent that the thermal noise floor is 26 nV/√Hz. The total input-referred noise of amplifier is 3.03 µV over 1Hz - 10 kHz. In order to compare amplifiers according to their noise, noise efficiency factor (NEF) is defined [11]

$$NEF = V_{ni,rms}\sqrt{\frac{2I_{tot}}{\pi V_T 4kTBW}} \quad (5)$$

Where $V_{ni,rms}$ is the input-referred rms noise, I_{tot} is the total supply current and BW is the amplifier bandwidth. The NEF is a significant criterion for representing the tradeoff between noise, bandwidth and current consumption.

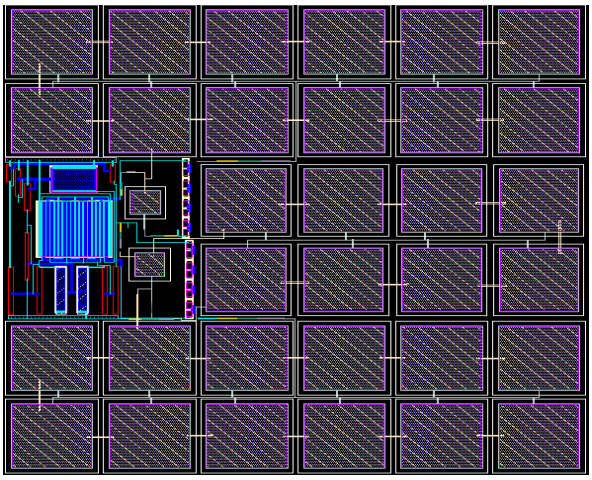

Figure 3. Layout of the amplifier with the size of (218 µm×215 µm)

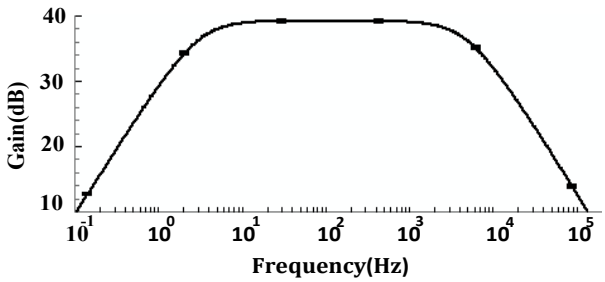

Figure 4. Frequency response of the amplifier

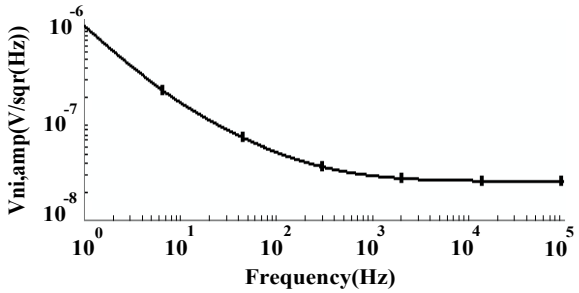

Figure 5. Input-referred noise spectra of the amplifier

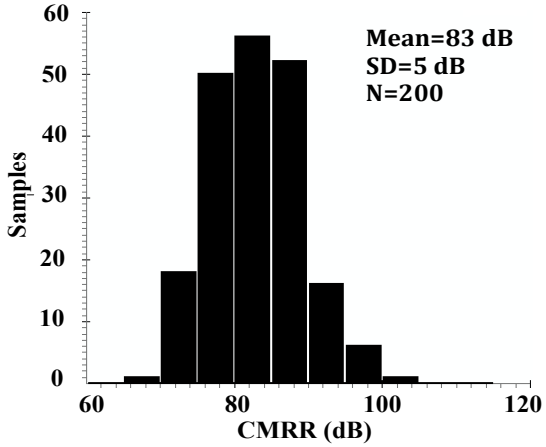

Figure 6. Mont Carlo simulation (200 runs) of CMRR at 50 Hz

However, it does not include V_{DD}. The PEF is another merit which adds supply voltage to noise efficiency factor, and it can be expressed as $NEF^2.V_{DD}$. In our design, $I_{tot}=2.125I_B$, $V_{DD}=1.4$ and input noise is 1.47 time of input noise of a differential pair in the sub-threshold region. In this regard, The NEF and PEF are 2.4 and 8.06, respectively.

The THD of the proposed amplifier stays below 1% with a maximum 13.2 mV_{p-p} input signal while the output signal swing is 1.16 $V_{p-p.}$ Also, the Monte Carlo simulation has been carried out to show the sensitivity of the circuit to the mismatches and process variations. Fig. 6 represents the CMRR of the amplifier for the process and mismatch simulation for 200 runs. It reveals that the amplifier CMRR is not too sensitive to process and mismatch. In addition, the mean values of open loop gain and close loop gain are 83.12 dB and 39.22 dB, respectively.

According to Monte Carlo simulation, CMRR and PSRR are in worst case, more than 77 and 70 at 50 Hz, respectively. In table II, the proposed amplifier is compared to the state-of-the-art capacitively-coupled biomedical amplifiers.

V. Conclusion

In this paper, a low-power, low-noise and high swing capacitively-coupled amplifier is proposed for biomedical application, especially neural recording. We have used several low-power and low-noise design techniques in a suitable structure to make an efficient trade-off. In this regard, the amplifier has a good NEF while it has a much better PEF and higher output swing with a same supply voltage. Finally, The Monte Carlo simulation showed the good performance of the circuit against mismatches and process variation.

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