A Low-power and Low-noise Multi-purpose Chopper Amplifier with High CMRR and PSRR

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***Abstract*— In this article, by choosing and optimizing suitable structure in each stage, we have designed a multi-purpose low noise chopper amplifier. The proposed neural chopper amplifier with high CMRR and PSRR is suitable for EEG, LFP and AP signals while it has a low NEF. In order to minimize the noise and increase the bandwidth, a single stage current reuse amplifier with pseudo-resistor common-mode feedback is chosen, while a simple fully differential amplifier is implemented at the second stage to provide high swing. A DC servo loop with an active RC integrator is designed to block the DC offset of electrodes and a positive feedback loop is used to increase the input impedance. Finally, an area and power-efficient ripple reduction technique and chopping spike filter are used in order to have a clear signal. The designed circuit is simulated in a commercially available $0.18\ \mu m$ CMOS technology. $3.7\ \mu A$ current is drawn from a $\pm 0.6V$ supply. The total bandwidth is from 50 mHz to 10 kHz while the total input-referred noise in this bandwidth is $2.9\ \mu V_{rms}$ and the mid-band gain is about 40 dB. The designed amplifier can tolerate up to 60 mV DC electrode offset and the amplifier's input impedance with positive feedback loop is $17\ M\Omega$ while the chopping frequency is 20 kHz. With the designed ripple reduction, there is just a negligible peak in the input-referred noise due to up-modulated noise at chopping frequency. In order to prove the performance of the designed circuit, 500 Monte Carlo analysis is done for process and mismatch. The mean value for CMRR and PSRR are 94 and 80 dB, respectively.**

***Index Term*— Instrumentation amplifier, High CMRR, Cross-coupled OTA, Current-reuse OTA.**

I. Introduction

The use of biomedical signals are not only in clinical purposes such as epilepsy and Parkinson's disease, but also in entertainment, sports and brain computer interfaces (BCIs). Due to the wide use of biomedical signals and their different characteristics, there is a great demand for amplifiers which can amplify all kind of biomedical signals. EEG, Local field potential (LFP) and Action potential (AP) are three kind of brain signals which have useful information in basic neuroscience research and therapy [1].

There is a trade-off between these three kind of signal. LFP and AP are invasive but they have better signal quality in comparison to EEG signals. The LFP and EEG have lower frequency while AP's frequency is relatively high. The differences are not limited by their frequency and the way they could be recorded is different. They even have different amplitude. Their amplitude, frequency and their recording method are reported in the Table I.

TABLE I
Overview on some neural signals and recording technique

Neural Signal	Amplitude (μV)	Frequency (Hz)	Recording method
EEG	0.5 -10	0.5 - 50	Non-invasive
LFP	10 - 1000	0.5 - 200	Invasive
AP	10 - 100	200 - 10000	Invasive

Since the electrode offset for EEG signals is much larger than the input signal amplitude, it can saturate the output. Therefore, the DC offset should be canceled. In addition, the input impedance of amplifier should be much higher than the electrode impedance. Finally, in order to reject common-mode signals like power line noise and other environmental noise which are relatively high in some cases, neural amplifiers should have high CMRR and PSRR.

Most of the article focuses on one type of signal in order to decrease power consumption or design simplification. In [2] a neural field potential amplifier with bandwidth from 50 mHz to 120 Hz was proposed. The total input-referred noise in the bandwidth from 50 mHz to 100 Hz is $0.95\ \mu V_{rms}$. In [3] and [4], they consume $14.8\ \mu W$ and $66.2\ \mu W$, respectively to reach to the bandwidth of 10 kHz and low noise.

In this article, by utilising chopping technique, the designed amplifier has low noise for EEG and LFP signals, and it has wide bandwidth and high swing due to first and second stage structure which made this amplifier suitable for AP signals. The first stage is a current reuse amplifier with a pseudo-resistor common-mode feedback which helped to increase the bandwidth and decrease the noise for a given bias current. In addition, a DC servo loop in order to block unwanted DC offset up to 60 mV is designed. The lower cut-off frequency is set on 50 mHz by utilizing two pseudo-resistors to make this such a low frequency achievable in an integrated circuit. The proposed chopper amplifier has a good NEF (noise efficiency factor), which shows the merit of the designed amplifier although it can be used for different neural signals.

II. System Overview

The structure of the proposed chopper amplifier is depicted in Fig. 1. The input signal is translated to higher frequency

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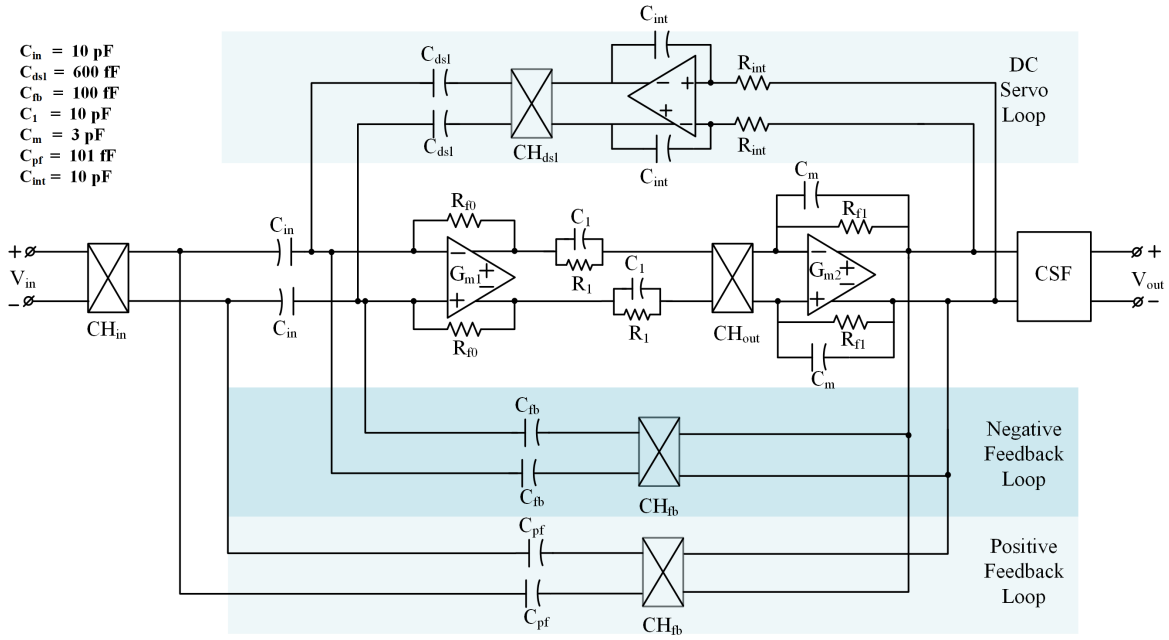

Fig. 1. Structure of designed chopper amplifier

by going through the CH_{in}. Afterwards, it will be amplified by the pre-amplifier and the second stage amplifier which are depicted with G_{m1} and G_{m2}. Meanwhile by passing through CH_{out}, the input signal is mixed down to its initial frequency while noise and offset are shifted to higher frequency. C_m and the output impedance of the first stage, make a low-pass filter to separate signal from up-modulated noise and offset. The effective capacitance for the low-pass is determined with C_m and the gain of the second stage. A negative feedback is used to set the gain on 40 dB. Therefore, since the C_{in} is 10 pF, the C_{fb} is 100 fF. The Positive feedback which consist of a chopper and two capacitors is designed to increase the input impedance. The DC servo loop effect is similar to a high-pass filter for the circuit. It consists of a simple integrator and a chopper and two capacitors which determine the tolerable offset. R_1 and C_1 are used to reduce the up-modulated noise and offset which cause ripple in the output signal. At the output, a chopping spike filter (CSF) is placed to eliminate spikes which are added to the signal from choppers. The R_{f0} and R_{f1} are implemented by pseudo-resistor to set the common-mode signal and make a better DC biased when there is a DC offset.

III. Pre-amplifier

Since the first stage plays a significant role in the total input-referred noise, a current reuse structure is chosen and is shown in Fig. 2 [5]. The input-referred noise can be calculated approximately as follows:

$$\overline{v_{ni}^2} = \frac{8kTc}{g_{m_1} + g_{m_2}} + \frac{2K_p}{W_1 L_1 f C_{ox}} + \frac{2K_n}{W_2 L_2 f C_{ox}} \quad (1)$$

In the above equation c is approximately $2/3$ though it varies slightly according to the biasing of the transistor, K_p and K_n are process-dependent constant, k is the Boltzmann constant and T is temperature in Kelvin. The input transistors are put in the sub-threshold region to increase $g_{m1,2}$ for a given current. The W and L are chosen large enough to have a negligible flicker noise after chopping. In addition, most of the power is consumed in this stage to minimize the thermal noise as well.

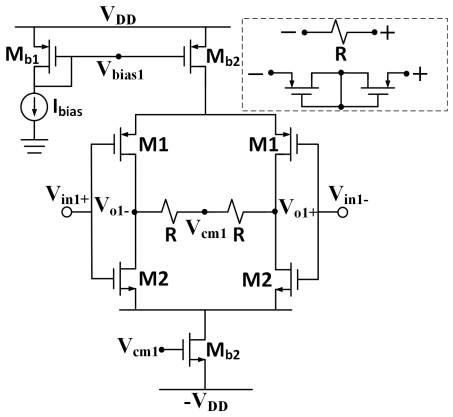

Fig. 2. Pre-amplifier with psuedo-resistor common-mode feedback

In order to reach the highest bandwidth and good DC bias, a common-mode feedback with two pseudo-resistors is applied to the circuit as it's represented.

IV. Second stage amplifier

The second stage consists of a simple differential amplifier with a common-mode feedback which are shown in Fig. 3. Although this stage has just a negligible effect on the noise, this stage will determine the output swing and upper cut-off

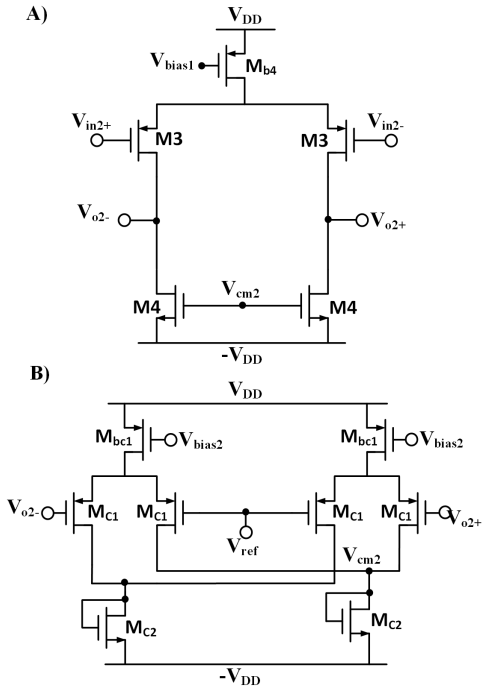

Fig. 3. A) The second stage amplifier B) the common-mode feedback

frequency. The minimum and maximum output voltage are equal to:

$$V_{O2,max} = V_{DD} - V_{DSAT,M_{bc1}} - V_{GS,M_{c1}} \tag{2}$$

$$V_{O2,min} = -V_{DD} + V_{DSAT,M_4} \tag{3}$$

In order to minimize the V_{GS} of M_{bc1}, it is put in the sub-threshold region. In order to reach the maximum swing, the voltage between $V_{O2,max}$ and $V_{O2,min}$ is chosen as a DC bias. Accordingly, maximum single-ended output swing is 700 mV peak to peak.

V. DC servo loop (DSL)

The DSL consist of an integrator, a chopper and two capacitors. The most important part is the integrator. A simple integrator which consists of an amplifier, a capacitor and a resistor is used in this design. It has a structure as used in [6]. The DSL loop determines the lower cut-off frequency and tolerable offset according to [7]:

$$f_{hp} = \frac{C_{dsl}}{C_{fb}} f_{0dsl} \tag{4}$$

$$V_{EO} = \frac{C_{dsl}}{C_{in}} V_{out,max} \tag{5}$$

In the above equation f_{0dsl} is the unity gain of the integrator which is controlled by the amplifier gain. The resistor and capacitor in the integrator, f_{hp} is the high-pass corner, which in this design is set on 50 mHz. In order to obtain such a low f_{hp}, we require a large RC. The designed capacitor is 10 pF while the resistors are pseudo-resistors

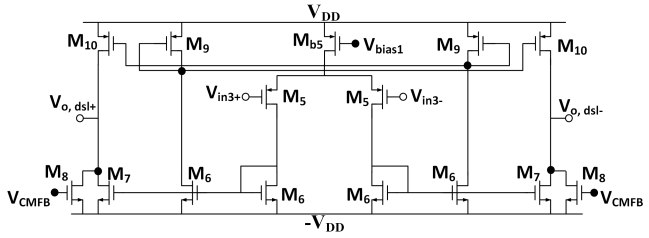

Fig. 4. The DSL amplifier with current mirror structure

to reduce the area consumption. Furthermore, V_{EO} is the maximum tolerable input offset voltage and $V_{out,max}$ is the maximum output swing of the integrator. That is why a current mirror amplifier as Fig. 4 is used to have the maximum output swing. In addition, C_{dsl} is 600 fF therefore according to Equation 5, tolerable offset is 60 mV.

VI. Chopping spike filter, positive feedback loop and Ripple reduction

In order to reach a high input impedance, a low power technique, which is used in [7], is applied to the circuit. In addition to minimize the ripple, which will be produced in the output due to up-modulated noise and offset, four series of pseudo-resistors in parallel with a 10 pF capacitor are placed after the first stage which is the main source of output ripple [8]. This resistor and capacitor are depicted as R_1 and C_1 in Fig. 1. A chopping spike filter is put at the end, in order to suppress the output spikes which are produced with choppers. In CSF there is another modulator which works with two times higher frequency than normal chopping frequency of circuit. When there is a spike in the output, the switches will disconnect the output path from output capacitor and it will help to smooth the output signal.

VII. Results

The designed capacitively-coupled chopper amplifier is simulated in a 180nm CMOS technology and its performance is tested with 500 Monte Carlo simulations for mismatch and process variations while the chopping frequency is 20 kHz. The designed amplifier has about 40 dB mid-band gain with 30 nV/sqrtHz noise floor. Without ripple reduction at chopping frequency, the noise was 300 nV/sqrtHz but with the ripple reduction it suppressed to 35 nV/sqrtHz and made a smooth noise spectral density as it's shown in Fig 5. The total power consumption with chopping spike filter is $4.4\ \mu W$. The chopping spike filter consumes about $1\ \mu W$. Total input-referred noise in the bandwidth of EEG, LFP and AP (as it's described in the table I) are $0.3, 0.44$ and $2\ \mu V_{rms}$, respectively.

The CMRR and PSRR mean values are 94 and 80 dB for 500 Monte Carlo simulations, respectively. The input impedance of the designed amplifier is 17 $M\Omega$ at 50 Hz. The transient output response to show the performance of CSF is depicted in Fig. 7. Finally, the designed chopper amplifier is compared with the state-of-the-art amplifiers in table II. There are different parameters to compare the amplifiers

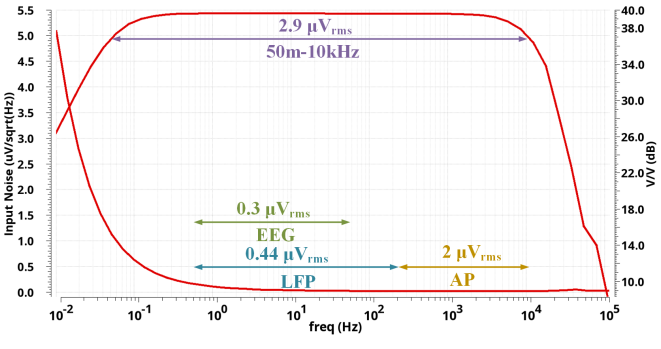

Fig. 5. The gain and noise versus frequency

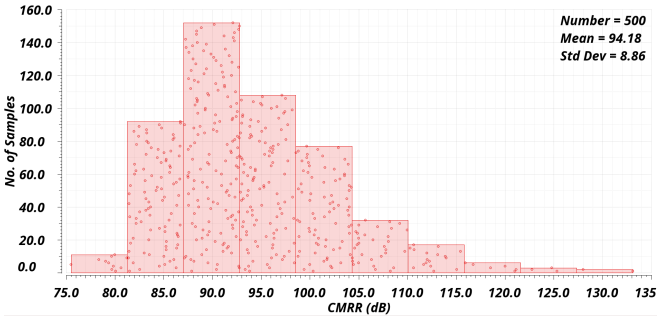

Fig. 6. 500 Monte Carlo simulation for CMRR

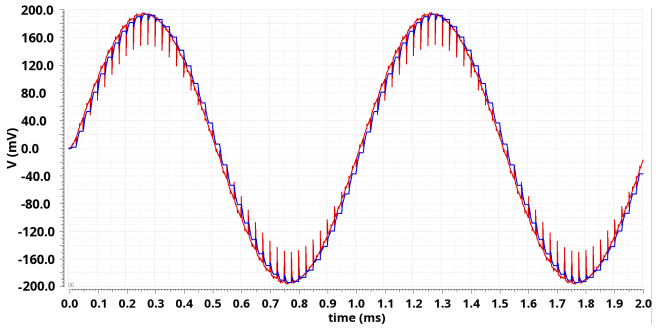

Fig. 7. Output transient response for 1 mV input signal, red line: without CSF, blue line: after CSF

TABLE II

PERFORMANCE SUMMARY AND COMPARISION

Specs	[1]	[2]	[9]	[10]	This Work
Tech. (nm)	40	800	65	180	180
Supply	1.2	1.8, 3.3	1	1	1.2
Current (μA)	1	1	3.28	0.25	3.7
Bandwidth (Hz)	1-5k	50m-120	1-8.2k	250-10k	50m-10k
Gain (dB)	26	41, 50	52.1	25.6	40
CMRR (dB)	-	100	80	84	94
PSRR (dB)	-	-	78	76	80
IR Noise (μV_{rms})	7	1.2	4.13	5.5	2.9
NEF	4.9	4.6, 5.4	3.19	1.07	2.2

merit. The defined NEF in [7] is used since it combines noise, bandwidth and current consumption together and represents a figure of merit for the designed amplifiers. As it's shown in the table II, the designed circuit has a good NEF while it can be used for EEG, LFP and AP signals. Although reference [10] has a better NEF, EEG and LFP signals are not in the bandwidth of it.

VIII. Conclusion

In this article, a multi-purpose chopper amplifier is presented. The proposed amplifier has wide bandwidth (50 mHz-10 kHz) and 2.9 μV_{rms} input-referred noise while it consumes 4.4 μW with chopping spike filter and DSL. Therefore, the designed amplifier has low NEF while it can be used for different purposes. The DSL is designed to block DC offset up to 60 mV. The input impedance of the designed amplifier at 50 Hz is boosted to 17 $M\Omega$ by a positive feedback loop. In addition, the performance of the designed circuit is tested with Monte Carlo simulation for mismatch and process variation. The CMRR and PSRR were 94 and 80 dB, respectively. Up-modulated offset and noise were suppressed with an area efficient ripple reduction techniques which leads to a smooth noise spectral density near the chopping frequency.

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