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Ida Marie Høiaas

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# SEMICONDUCTOR-GRAPHENE HYBRID STRUCTURES AND OPTOELECTRONIC DEVICES

Doctoral theses at NTNU, 2020:258

**NTNU**  
Norwegian University of Science and Technology  
Thesis for the Degree of  
Philosophiae Doctor  
Faculty of Information Technology and Electrical  
Engineering  
Department of Electronic Systems

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Norwegian University of  
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Thesis for the Degree of Philosophiae Doctor

Trondheim, September 2020

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# Abstract

In order to utilise the intriguing properties discovered in nanomaterials during the last decades, structures and devices that do exactly that have to be developed. Graphene, the carbon wondermaterial discovered in 2004, has baffled the scientific community with its endless possibilities for quantum physics experiments, as well as extreme properties for current conduction, transparency and heat dissipation. Semiconductor nanowires with their one-dimensionality have been able to solve some fundamental challenges in thin films, as they enable the integration of optically active semiconductors onto both conventional and new substrates. Together with a precise control of crystal design, this enables the integration of lasers, solar cells, photodetectors and light emitting diodes with different substrates not suitable for bulk growth. To take advantage of the possibilities offered by combining these two very different nanostructures, complex fabrication strategies, diligent and multifaceted characterisation work and extensive collaborations have to be employed to reach the end-goal of actual functional devices.

We have studied several approaches to enable the fabrication of graphene-semiconductor hybrid devices. The transfer of graphene with a metal protection layer has been studied in detail to try and realise molecular beam epitaxy-compatible chemical vapour deposited graphene for the direct growth of semiconductor nanowires. The growth of GaAs, GaAsSb and GaN nanowires on kish graphite has been investigated both with and without an oxide mask for position-controlled growth of the nanowires. A two-layer mask structure consisting of alumina and silicon oxide was found to give the best selectivity, while the oxygen plasma and subsequent hydrogen annealing treatment of graphite was found to increase the nucleation probability of nanowires.

To further increase the nucleation probability of GaAs and GaAsSb nanowires on chemical vapour deposited graphene, a thin film consisting of aluminium-induced crystallised Si was deposited. By varying the silicon surface oxide formation and optimising the nanowire growth, high-density vertical nanowires could be grown.

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Not only did the thin film of polycrystalline Si strongly increase the density of vertical nanowires, it was also discovered that the presence of graphene directly affected the crystallinity of the aluminium-induced crystallised Si, when compared with the same substrate without the graphene layer. The deposited Si had an increase in (111)-oriented grains with respect to the surface plane, which is beneficial for the growth of vertical GaAs nanowires, which also grow in the [111]-direction. The graphene is not damaged as aluminium-induced crystallisation of Si takes place at relatively low temperatures ( $< 577^{\circ}\text{C}$ ), and apparently adopts the strain present in the polycrystalline Si. An epitaxial model is suggested to explain the effect of graphene on Si crystallisation. A photodetector consisting of the graphene and aluminium-induced silicon was fabricated, but as of yet reliable operation could not be achieved.

The growth of GaN/AlGaN nanowires on bi- and single-layer graphene was studied and used for the fabrication of ultraviolet light emitting diodes using graphene as a transparent conductive electrode. The nitrogen plasma extensively damages graphene, but through the use of a special nucleation scheme using an AlN buffer layer the damage can be decreased and graphene can inject current through the photoactive nanowires. Emission in the UVA region (365 and 352 nm) was achieved, and the simultaneous use of graphene as growth substrate and transparent conductive electrode was demonstrated for the first time for any device.

Together, this work demonstrates the possibilities and potential platforms of certain semiconductor-graphene optoelectronic devices, possibly enabling the development of commercial technology in the future.

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Ida Marie Høiaas  
Trondheim, Norway  
June 2020

# List of abbreviations

1D	One-dimensional
2D	Two-dimensional
3D	Three-dimensional
AFM	Atomic Force Microscope
AIC	Aluminum-Induced Crystallisation
ALD	Atomic Layer Deposition
BLG	Bi-Layer Graphene
BSE	Backscattered Electron
CCD	Charge-Coupled Device
CMOS	Complementary Metal-Oxide-Semiconductor
CVD	Chemical Vapour Deposition
CW	Continuous Wave
EBL	Electron Beam Lithography
ED	Electrochemical Delamination
EDS	Energy-Dispersive X-ray Spectroscopy
EELS	Electron Energy Loss Spectroscopy
$E_g$	bandgap
EL	Electroluminescence Spectroscopy
EMCCD	Electron Multiplying Charge Coupled Device
EQE	External Quantum Efficiency
FWHM	Full Width at Half Maximum
HAADF	High-Angle Annular Dark-Field
IQE	Internal Quantum Efficiency
IV	Current-Voltage
LED	Light Emitting Diode
LEE	Light Extraction Efficiency
MBE	Molecular Beam Epitaxy

## CONTENTS

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MIC	Metal-Induced Crystallisation
NC	Nanocolumn
NW	Nanowire
OF	Optical Fiber
PA-MBE	Plasma Enhanced Molecular Beam Epitaxy
PD	Photodetector, Photodiode
PECVD	Plasma-Enhanced Chemical Vapour Deposition
PL	Photoluminescence Spectroscopy
PMMA	Poly(Methyl Methacrylate)
SAE	Selective Area Epitaxy
SAG	Selective Area Growth
SE	Secondary Electron
SEM	Scanning Electron Microscope
SLG	Single-Layer Graphene
STEM	Scanning Transmission Electron Microscope
TCE	Transparent Conductive Electrode
TEM	Transmission Electron Microscope
ToF-SIMS	Time-of-Flight Secondary Ion Mass Spectroscopy
UV	Ultraviolet
WPE	Wall Plug Efficiency
WZ	Wurtzite
XPS	X-ray Photoelectron Spectroscopy
XRD	X-ray Diffraction
ZB	Zinc Blende

# List of publications and presentations

## Journal publications included in this thesis

### Paper I

**Ida Marie Høiaas**, Dong-Chul Kim and Helge Weman. "Fabrication of Si(111) crystalline thin film on graphene by aluminum-induced crystallisation". *Applied Physics Letters* 108, 161906, 2016.

### Paper II

Dingding Ren\*, **Ida Marie Høiaas\***, Johannes Reinertsen, Dheeraj L. Dasa, A. Mazid Munshi, Dong-Chul Kim, Helge Weman and Bjørn-Ove Fimland. "Growth optimization for self-catalyzed GaAs nanowires on metal-induced crystallized amorphous substrate". *Journal of Vacuum Science and Technology B*, 34, 117, 2016.

### Paper III

Andreas Liudi Mulyo, Anjan Mukherjee\*, **Ida Marie Høiaas\***, Lyubomir Ahtapodov, Tron Arne Nilsen, Håvard Hem Toftevaag, Per Erik Vullum, Katsumi Kishino, Helge Weman and Bjørn-Ove Fimland. "Graphene as Transparent Conducting Substrate for The Fabrication of Flip-chip Ultraviolet Light-Emitting Diode Based on GaN/AlGaIn Nanocolumns". *To be submitted*, 2020.

## Paper IV

**Ida Marie Høiaas\***, Andreas Liudi Mulyo\*, Per Erik Vullum, Dong-Chul Kim, Lyubomir Ahtapodov, Bjørn-Ove Fimland, Katsumi Kishino and Helge Weman. "GaN/AlGa<sub>N</sub> nanocolumn UV LED using graphene as substrate and transparent electrode". *Nano Letters* 19, 1649-1658, 2019.

\*: Shared authorship

## Selected presentations (presenter underlined)

- Ida Marie Høiaas, Andreas Liudi Mulyo, Dong-Chul Kim, Bjørn-Ove Fimland, Katsumi Kishino and Helge Weman. "Using graphene as substrate and transparent electrode in an GaN/AlGa<sub>N</sub> nanocolumn flip-chip UV LED". Nanowire Week, Hamilton, Canada (June 11-15, 2018). [Oral presentation]
- Ida Marie Høiaas, Andreas Liudi Mulyo, Per Erik Vullum, Lyubomir Ahtapodov, Dong-Chul Kim, Bjørn-Ove Fimland, Katsumi Kishino and Helge Weman. "AlGa<sub>N</sub>/Ga<sub>N</sub> nanowire flip-chip UV LED using graphene as substrate and transparent electrode". Nano@NTNU, Trondheim, Norway (December 6-7, 2017). [Oral presentation]
- Andreas Liudi Mulyo, Ida Marie Høiaas, Mohana Krishnappa Rajpalke, Bjørn-Ove Fimland, Katsumi Kishino and Helge Weman. "Graphene as a substrate and bottom electrode for high density and vertically aligned Ga<sub>N</sub> nanocolumns". Nano@NTNU, Trondheim, Norway (December 6-7, 2017). [Oral presentation]
- Andreas Liudi Mulyo, Ida Marie Høiaas, Dong-Chul Kim, Bjørn-Ove Fimland, Katsumi Kishino and Helge Weman. "AlGa<sub>N</sub>/Ga<sub>N</sub> Nanocolumn Flip-Chip UV LEDs Grown on Graphene/Silica Glass". The 11th International Symposium on Semiconductor Light Emitting Devices, Michigan, USA (October 8-12, 2017). [Oral presentation]
- Ida Marie Høiaas, Dong-Chul Kim and Helge Weman. "Silicon-graphene heterostructure for optoelectronic devices". Nano Network Workshop, Trondheim, Norway (June 15-17, 2015). [Oral presentation]
- Ida Marie Høiaas, Andreas Liudi Mulyo, Per Erik Vullum, Lyubomir Ahtapodov, Dong-Chul Kim, Bjørn-Ove Fimland, Katsumi Kishino and Helge Weman.

- "GaN/AlGaN nanocolumn UV LED using graphene as substrate and transparent electrode". Int. Workshop on Nitride Semiconductors, Kanazawa, Japan (November 11-16, 2018). [Poster]
- Andreas Liudi Mulyo, Ida Marie Høiaas, Per Erik Vullum, Lyubomir Ahtapodov, Dong-Chul Kim, Bjørn-Ove Fimland, Katsumi Kishino and Helge Weman. "Growth and characterization of n-doped GaN nanocolumns grown on graphene using a thin AlN buffer layer". Int. Workshop on Nitride Semiconductors, Kanazawa, Japan (November 11-16, 2018). [Poster]
  - Ida Marie Høiaas, Andreas Liudi Mulyo, Dong-Chul Kim, Bjørn-Ove Fimland, Katsumi Kishino and Helge Weman. "Graphene as growth substrate and transparent electrode for flip-chip GaN/AlGaN nanocolumn UV-LEDs". Carbonhagen, Copenhagen, Denmark (August 2017). [Poster]
  - Ida Marie Høiaas, Dong-Chul Kim and Helge Weman. "Aluminum-induced crystallization of Si on graphene for optoelectronic devices". Carbonhagen, Copenhagen, Denmark (August 17-18, 2016). [Poster] **Award for best poster**
  - Ida Marie Høiaas, Dong-Chul Kim and Helge Weman. "Large-grained Si(111) crystalline thin film on graphene by aluminum-induced crystallization". Graphene, Genova, Italy (April 19-22, 2016). [Poster]
  - Ida Marie Høiaas, Dingding Ren, Dong-Chul Kim, Johannes Reinertsen, Bjørn-Ove Fimland and Helge Weman. "GaAs Nanowire Growth on [111]-oriented Silicon with sub-grain Thickness". MyFab and NorFab user meeting, Lund, Sweden (April 21-22, 2015). [Poster]
  - Ida Marie Høiaas, Dingding Ren, Dong-Chul Kim, Johannes Reinertsen, Bjørn-Ove Fimland and Helge Weman. "GaAs Nanowire Growth on [111]-oriented Silicon with sub-grain Thickness". Nano Network Workshop, Trondheim, Norway (June 15-17, 2015). [Poster]
  - Dingding Ren, Ida Marie Høiaas, Johannes Reinertsen, Dheeraj L. Dasa, A. Munshi Mazid, Junghwan Huh, Dong-Chul Kim, Bjørn-Ove Fimland and Helge Weman. "Growth optimization for self-catalyzed GaAs nanowires on metal induced crystallized amorphous substrate". 31st North American Conference on Molecular Beam Epitaxy, Mayan Riviera, Mexico (October 4-7, 2015). [Poster]

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Part I

Background



# Chapter 1

## Introduction

With electronic component feature sizes continuing to shrink [1], energy demands rising [2] and environmental pollution increasing [2], the need for better, smaller and more efficient electronic and optoelectronic devices and systems persist. To achieve this, two main paths can be chosen; either to incrementally improve existing technology or developing completely new materials and components. As existing industries are mainly devoted to the first path, science and academia are contributing in expanding, understanding and doing the preliminary development for the second path.

Nanotechnology entered the stage with a boom in the 1990s and 2000s, although many will claim that it has 'always' been researched, but within conventional scientific disciplines. Apart from being a buzzword, what changed during these last decades was that nanotechnology emerged as a truly interdisciplinary endeavour, combining and expanding knowledge from physics, chemistry, material technology, biology and many other fields. As a result thousands upon thousands of nanomaterials have been discovered and described, as an example only among two-dimensional materials the list of identified materials counted more than 800 in March 2017 [3], and newly developed nanoscopic techniques have led to an increased understanding of old and new materials alike. But after such a discovery, the first question to be asked by non-scientists is always the same: "What can you use it for?".

As many working within nanotechnology field are well aware of, there is a long way between characterising a material and making a functional device, like a diode, laser, transistor, actuator, solar cell or photocatalyst in water splitting to name a few. To achieve this, one must not only understand the material properties, but also possess the knowledge of controlled manipulation. The goal of this thesis has been

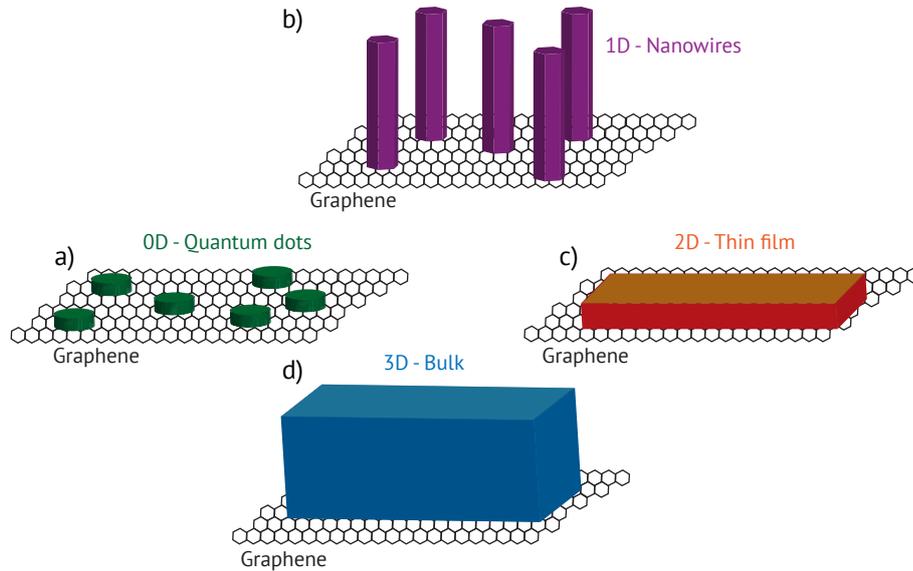


Figure 1.1: Different categories of nanostructured semiconductor-graphene hybrid structures.

to explore the semiconductor materials fabricated in our group, mainly nanowires, and fabricate optoelectronic devices based on hybrid structures of nanostructured semiconductors and graphene. The different categories of such hybrid structures are depicted in Figure 1.1, with the focus point of the thesis being on Parts (b) and (c), namely one-dimensional semiconductors/graphene and thin-film semiconductors/graphene. The definition of a nanomaterial is that one or more of the dimensions of the material is at most on the order of a few hundred nanometers. Also, that something is described as zero-, one- or two-dimensional typically means that quantum effects can be observed due to confinement in the tens of nanometer scale. The semiconductor nanowires that we work with are not proper 1D-materials, as they have diameters of a few hundred nanometers and thus are more appropriately termed quasi-1D structures.

Graphene is an interesting material in this context as it itself is a two-dimensional nanomaterial with extreme physical, optical and electronic properties. It is stable and has a high mechanical strength [4], it conducts electricity well because of its high mobility [5], and is transparent to all wavelengths of light [6]. Furthermore, it

has a hexagonal crystal lattice making epitaxial growth possible [7] and a tunable Fermi level [8]. All of these properties contribute to vast flexibility in optoelectronic device design.

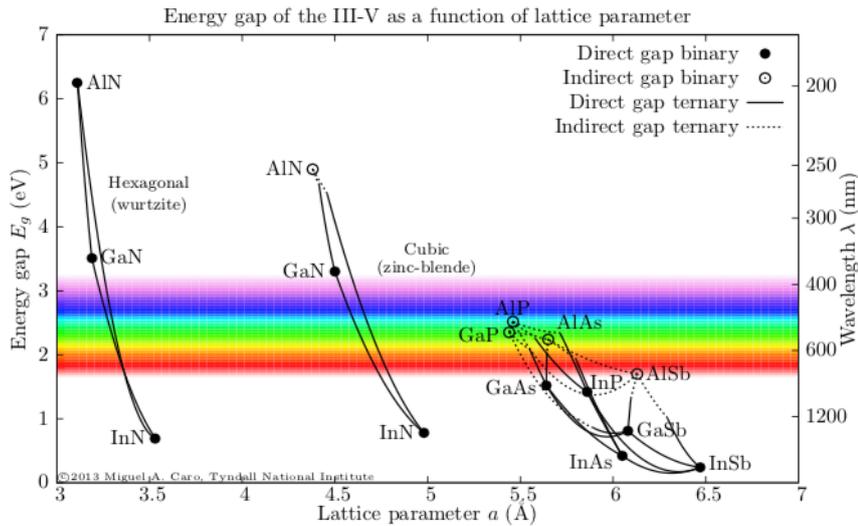


Figure 1.2: Lattice constants and bandgaps of III-V semiconductors commonly used in optoelectronics. Adapted from [9].

In conventional epitaxial growth, meaning the growth of a crystal on a crystalline substrate with an orientation determined by the substrate, the material combination possibilities are limited by lattice matching. Lattice mismatch means that a large discrepancy in the distance between atoms of the two layers leads to strain in the overlayer and consequently defects. Growing the overlayer in the form on nanowires allows the strain induced by lattice mismatch to relax through the surface, meaning that defect-free material can be grown even for lattice-mismatched systems. Several semiconductor nanowires have been grown on graphene, as described in more detail in Section 2.3.2, but in our group we have traditionally focused on III-V, including III-N, nanowire semiconductor growth and characterization, like GaAs [10–13], GaAsSb [14, 15], AlGaAs [16–18], GaN [19, 20] and AlGaN. The possibility of incorporating a third element in our semiconductor, like antimonide-incorporation in GaAs, enables tuning of the electronic properties and semiconductor bandgap, enabling a broader design and application range. This is especially true for the GaN-AlGaN system, as

## CHAPTER 1. INTRODUCTION

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shown in Figure 1.2, where the addition of Al to GaN means that the bandgap of the semiconductor can be tuned from violet at 365 nm for GaN to the deep UV-C region of 210 nm for AlN [21].

The results and ideas described by this thesis is part of the first work done on devices based on semiconductor-graphene hybrid structures in our group, and many methods and fabrication routes have been explored to achieve the final goal of optoelectronic devices. Some of these efforts have not led to publications but have been an important part of the thesis work, therefore some condensed results from this work have been included as part of the thesis.

## Chapter 2

# Background

This chapter is intended to provide a brief background to the topics described in Chapters 4-5, the papers and manuscript. For more detailed reading, the cited literature is advised.

### 2.1 Nanowires grown by molecular beam epitaxy

One-dimensional semiconductors, or nanowires, have been studied since the nineteen sixties [22], and there is still a very active field dedicated to this pursuit. Physical phenomena like extremely low thermal conductivity [23] and depression of melting point [24], has proven to be more accessible by looking at nanowires. Novel optical and electrical behaviour like a significant blue-shift of the absorption of Si [25] and extreme polarization anisotropy [26] has emerged compared with the bulk semiconductor. Finally, new device structures not previously possible in two-or three dimensional form has also been made possible, as the possibility to integrate active photonic components with CMOS platforms [27, 28]. This section aims to describe the growth and fundamental properties of semiconductor nanowires, and more specifically GaAs and GaN/AlGaN nanowires as these have been studied as part of this thesis.

Molecular beam epitaxy (MBE) can be used to grow high-purity crystalline materials with precise control of morphology, size, composition, phase and interfaces of the grown material. The base pressure of the chamber is in the order of  $10^{-10}$  Torr, meaning that the mean free path of the source gas molecules is longer than the source-substrate distance, and the gas molecules therefore do not interact with

each other. At NTNU, there are two MBE chambers, the Varian Gen II Modular system and Veeco GEN 930, where both are equipped for III-V growth, but the GEN 930 also has a nitrogen plasma source. During this thesis, both systems have been used to grow nanowires, as well as the EpiQuest RF-PAMBE system at Sophia University, Tokyo, Japan, for the AlGa<sub>N</sub> nanowire growth.

As nanowire growth by MBE is an epitaxial method, one requirement for growth is that the growth substrate is crystalline with a lattice constant similar to the material to be grown. Nanowires have the advantage over thin films that their large surface area allows them to relax strain more efficiently and thus be able to accommodate higher lattice mismatches than their thin film counterpart. A consequence of this is the possibility to grow nanowires on substrates unsuitable for thin film growth, and in this way open up for new material combinations. Our group showed in 2012 that GaAs nanowires can be grown directly on few-layer graphene, despite a large difference in lattice constants [29]. It is suggested that the semiconductor atoms bind to the surface of graphene with a quasi-van der Waals bond, which explains why such a large difference in lattice constant is possible without introducing defects in the nanowires.

### 2.1.1 III-V nanowire growth

MBE can be used to grow nanowires via the vapor-liquid-solid (VLS) method or vapor-solid (VS) method. III-V nanowires are normally grown by VLS, which requires the formation of a liquid catalyst droplet before any actual growth can occur. This droplet can be of a different material than the nanowire itself, for example Au, or by the group III-element, which is termed self-catalysed. Since 2009, most III-V nanowires grown at NTNU have been self-catalysed, using Ga as the catalyst droplet. Figure 2.1a) illustrates this growth method. After the Ga droplet has formed, As is supplied and incorporated by surface-diffusion of adatoms as well as direct impingement. Although all III-V semiconductors apart from nitrides are most stable in the cubic zinc-blende (ZB) crystal phase in bulk form, many can also form the hexagonal wurtzite (WZ) phase when grown in the form of nanowires [10,30–32], depending on the growth parameters employed.

### 2.1.2 III-N nanowire growth

What distinguishes nitride nanowire growth by MBE from the growth of other III-Vs, is the way the nitrogen atoms are supplied. Instead of using an effusion cell a nitrogen plasma source is used. This method is often coined plasma-assisted molecular beam epitaxy (PA-MBE). It is necessary to activate the nitrogen species

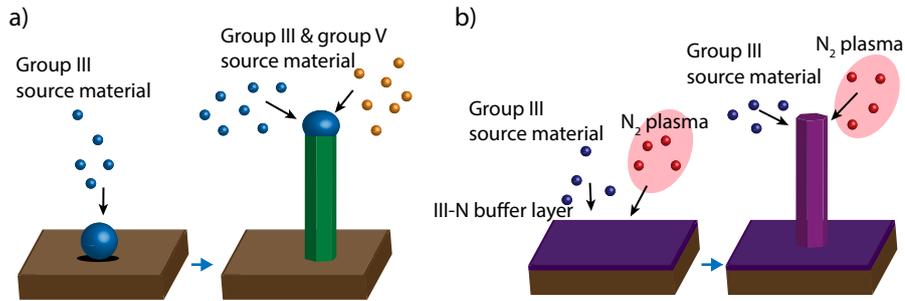


Figure 2.1: NW growth by the (a) VLS method for GaAs, and (b) VS method on graphene.

so that chemisorption can occur at the typical growth temperatures of 600-900°C. The dopants are still kept in standard effusion cells, in our case Si is used for n-doping and Mg is used for p-type doping. GaN and AlGaN do not need a catalyst droplet in order to form solid structures, and are grown by the VS method, as illustrated in Figure 2.1b). The WZ crystal phase is energetically favourable for the  $Al_xGa_{1-x}N$  system, and is therefore most commonly observed. As plasma in general is known to etch graphene and thus damaging it [33, 34], extra care must be taken when utilizing PA-MBE to grow nanowires on graphitic substrates [35].

## 2.2 Metal-induced crystallisation of Si

Amorphous silicon can be crystallised at low temperature by metal-induced crystallisation, utilising a metal catalyst as a diffusion path to crystallisation [36]. Aluminum-induced crystallisation (AIC) must be performed below the eutectic temperature between Al and Si of 577°C [37], and has been demonstrated at 150°C as the lowest temperature [38]. AIC is a so-called layer exchange mechanism, where two adjacent thin films of Al and Si exchange positions during the process, as depicted in Figure 2.2. The process starts by metal grains migrating through the Si layer, followed by diffusion of the semiconductor atoms through the metal [37] [39]. This leads to supersaturation, which is relieved through the nucleation and growth of polycrystalline Si [40]. A temperature field gradient due to energy release during crystallisation leads to a fractal formation of Si [41].

Crystallised Si as thin as 2.5 nm has been demonstrated by AIC [42], as well as films of several hundred nanometers [43]. The polycrystalline Si has been found

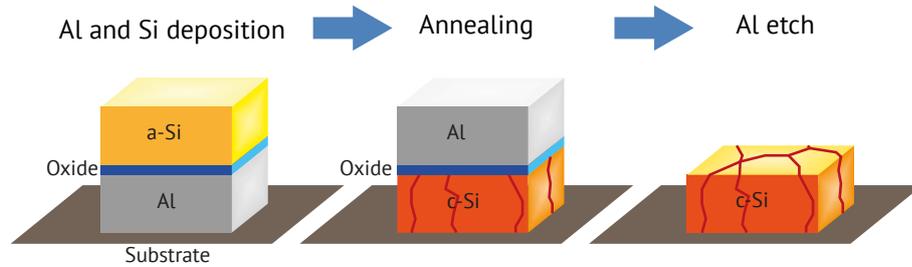


Figure 2.2: Schematic overview of the aluminum-induced crystallization of Si on graphene.

to be p-doped by Al [44]. The crystallisation duration is determined by a combination of factors, like temperature, thickness, and the presence of an interfacial oxide layer. This oxide layer can either be natively formed aluminum oxide or a deposited oxide. This oxide layer forms a semipermeable membrane which also affects the resulting out-of-plane orientation of the polycrystalline Si, with thicker oxides favoring [111]-orientation [45, 46]. The thickness of the Al and amorphous Si layers also affect the resulting orientation of the crystalline Si, with a change from predominantly [111]-orientation to [001]-orientation having been observed around 100 nm [45, 46]. Slower crystallisation leads to larger grains, and in general Si grains in the order of 10  $\mu\text{m}$  are commonly reported [47].

### 2.2.1 GaAs nanowire growth on AIC Si

There has previously been one report on the growth of GaAs nanowires on aluminum-induced crystallised Si, by Cohin et al [42]. By using glass substrates with different thicknesses of AIC Si, they showed that vertical nanowires could be grown by MBE on Si islands as thin as 2.5 nm. The nanowires were found to have a high crystal quality as attested by PL measurements, although twin defects during the initial growth stage led to a portion of the nanowires deviating from the vertical orientation.

## 2.3 Nanowire growth on graphene

Since it was first isolated and measured in 2004 [48], graphene has been regarded as a 'wondermaterial' due to its extreme properties in the form of mechanical stability, high electrical and thermal conductivity and light transparency [6]. Comprised of two overlapping triangular sublattices of carbon atoms, as shown in Figure 2.3(a), with sp<sup>2</sup>-hybridized orbitals, this two-dimensional material has enabled researchers to experimentally investigate physical phenomena like remote epitaxy [49, 50], spin-polarized currents [51] and superconductivity [52]. Due to its honeycomb lattice periodic potential, the behaviour of graphene charge carriers is better described as relativistic particles by the Dirac equation than the traditional Schrödinger equation. This allows scientists to directly probe quantum electrodynamics by measuring graphene's electronic properties [5, 53–57]. The light transparency surpasses that of conventional transparent conductive electrodes (TCEs), which is shown in Figure 2.3(b), especially in the ultraviolet region of the spectrum. The sheet resistance is comparable to conventional TCEs, but at a significantly lower electrode thickness as seen in Figure 2.3(c).

However, the two-dimensional nature of graphene also makes the integration of graphene with other materials challenging. To isolate a single layer of graphene, one must either mechanically exfoliate graphite [48] or transfer epitaxial [59, 60] or chemical vapor deposited (CVD) [61, 62] graphene from its metal catalyst. The first method leads to intrinsically pure graphene but with small flakes as a result [48], the second is a costly and difficult process [63], while the latter suffers from transfer contamination in the form of metal ions and organic residues [64, 65]. This is especially critical if one wishes to introduce the graphene to an ultra-clean MBE chamber, as all contamination is regarded as detrimental in such a system. Furthermore, a lack of dangling bonds makes graphene chemically inert, inhibiting the growth of foreign molecules and crystals. Both exfoliated graphite and CVD graphene has been used in the work described in this thesis. A promising route of CVD growth of graphene is the direct growth on the desired substrate [66–68], skipping the transfer process all together. However, such graphene still remains at a research-level and is not commercially available yet.

### 2.3.1 Graphene transfer

The conventional way of transferring CVD graphene involves covering the graphene with a sacrificial support layer, typically a polymer, and subsequently etching the Cu catalyst underneath graphene. This method leads to contamination with metal ions both from the Cu catalyst but also from the etchant solution which is typically

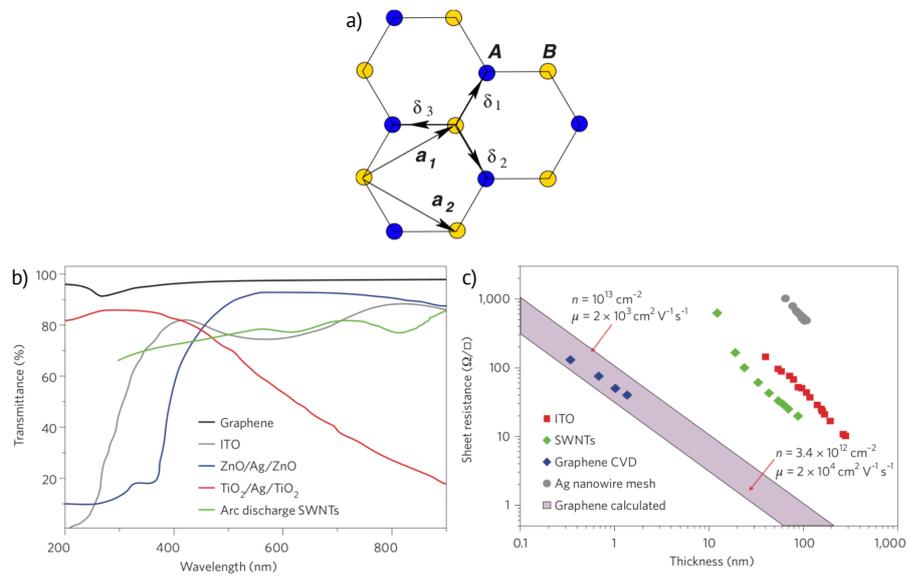
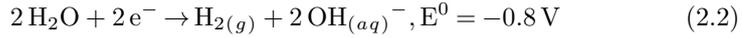
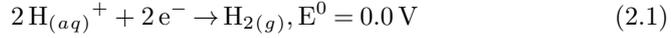


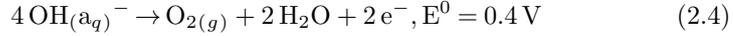
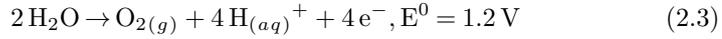
Figure 2.3: (a) Honeycomb crystal lattice of graphene with lattice unit vectors  $\mathbf{a}_1$  and  $\mathbf{a}_2$  and nearest neighbour vectors  $\delta_1$ ,  $\delta_2$  and  $\delta_3$ . The two different atomi groups A and B indicate the two triangular sublattices. (b) The transmission spectrum of common TCEs in the ultraviolet to NIR region. (c) Sheet resistance of common TCEs and the theoretically calculated limits of a graphene TCE with a carrier concentration of  $n = 3.4 \times 10^{12} \text{ cm}^{-2}$  and mobility of  $\mu = 2 \times 10^4 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ . (a) adapted from [58], (b) and (c) adapted from [6].

iron chloride ( $\text{FeCl}_3$ ) [69]. Through our collaboration with Sejong University Seoul, Korea, we have had access to graphene grown on a Pt catalyst instead of Cu, which is compatible with the MBE system.

A less contaminating transfer method, which also has the advantage of re-using the metal catalyst, is electrochemical delamination [70–72]. This method involves placing the graphene/metal catalyst piece in an electrolyte dissolved in  $\text{H}_2\text{O}$ , and consequently using it as one of two electrodes that pass current. Depending on the configuration, the sample can be used either as the anode or the cathode. If it is used as the cathode, hydrogen ( $\text{H}_2$ ) gas will evolve and delaminate the graphene, according to the following half-reactions:



If used as the cathode, oxygen gas ( $\text{O}_2$ ) will evolve and delaminate the graphene, following these reactions:



The mechanism responsible for the delamination has been debated. Earlier studies claim that gas evolution and consequently bubble formation mechanically delaminates the graphene [70], while more recent studies suggest that ion intercalation is the main driving force for graphene release from the metal catalyst [71].

The most commonly used electrolyte, sodium hydroxide ( $\text{NaOH}$ ), is known to cause cathodic corrosion to Pt [73], but it is unknown how this affects the graphene delamination when using it as the electrochemical electrolyte.

### 2.3.2 Growing semiconductor nanowires on graphene

The first hybrid structure of semiconductor nanowires grown on a graphitic substrate was demonstrated in 2009 by ZnO nanowires grown on few-layer graphene by Kim et al. [74]. After this, InAs nanowires were demonstrated in 2011 [75], and later several other semiconductor nanowires like Si [76], GaAs [29, 77], InP [78], GaP [77], InAs/InGaAs/InAsSb [77, 79–82] and GaN [20, 83–89] have followed suit. Because graphene is chemically inert, typically, the nanowire growth must be divided in a nucleation and growth step to achieve what is termed quasi-van der Waals-epitaxy

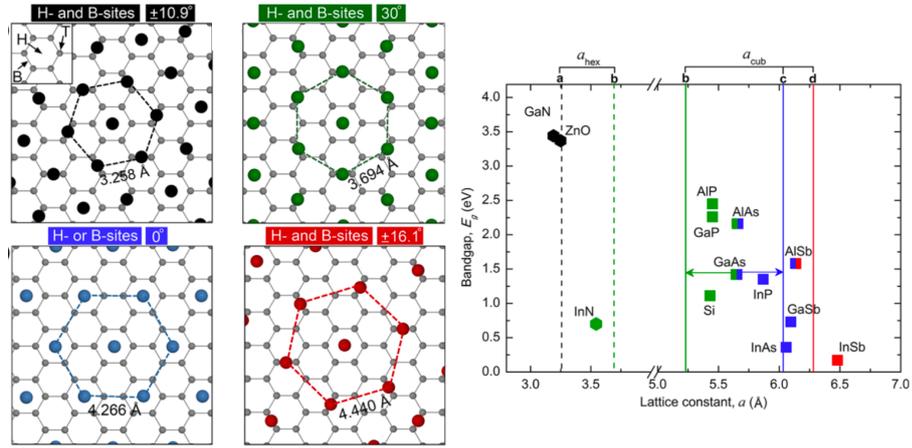


Figure 2.4: Potential atomic arrangements of semiconductor atoms on a graphene lattice, with the semiconductor atoms in the (111)-plane for cubic crystals and (0001)-plane for hexagonal crystals. Three possible sites are identified; H-, B- and T-sites. The potential arrangements shown in black, green, blue and red in the small panels are indicated as vertical lines of the same color in the lattice constant vs. band energy panel. The lattice constants of common semiconductors are shown as well to give some sense of the lattice mismatch that would result from the different arrangements. Adapted from [29].

[29,90], which means that the bond strength is stronger than van der Waals forces but weaker than a covalent bond.

There is not full agreement on the cause of the epitaxial relationship between semiconductor nanowires and graphene. Munshi et al. claim that GaAs nanowires grow epitaxially on graphene with the zincblende GaAs lattice rotated  $0^\circ$  or  $30^\circ$ , leading to a mismatch of 6.3% or 8.2% [29]. This is due to the preferential adsorption of atoms on H(hollow)-, B(brigde)- or H-and B- sites as seen in Figure 2.4. Likewise, GaN nanowires with a wurtzite crystal structure grow with the GaN lattice rotated  $\pm 10.9^\circ$  relative to the graphene lattice and a lattice mismatch of 2.1% according to Munshi et al. [29]. But according to Kumaresan et al., the lattice mismatch is 3.1% as they claim the first layer of either Ga- or N-atoms grow on T(top)- or B-sites in a supercell as shown in Figure 2.5 [87]. This theory is supported by Fernández-Garrido et al., whom found the epitaxial relationship between

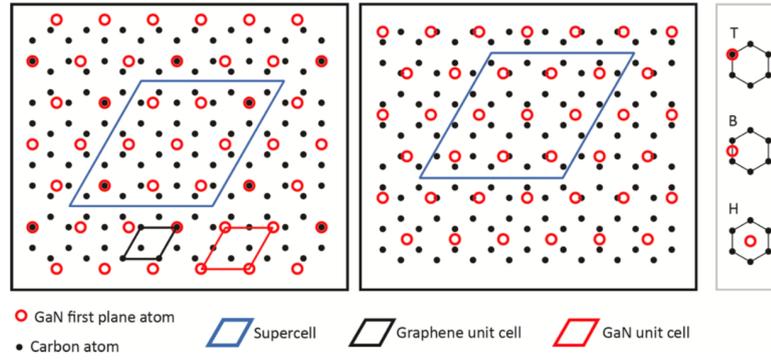


Figure 2.5: Potential atomic arrangements of the first layer of a GaN NW grown on graphene, where the blue rhomboid is the cell of coincidence between the GaN and graphene lattice. The two possible arrangements were found by placing GaN atoms on the H- and T-sites or B-sites of graphene. Adapted from [87].

GaN nanowires grown on epitaxial multilayer graphene on SiC by XRD. Here, the  $[1\bar{1}00]$ -direction of GaN was parallel to the SiC substrate  $[1\bar{1}00]$ -direction, which in turn is perpendicular to the graphene zigzag edges [91]. It is because of the efficient strain relaxation of the nanowires that such large lattice mismatches do not inhibit crystal growth, as they would for the thin film form of the semiconductors.

However, this is the case when a non-polar substrate is used underneath graphene. When a polar substrate is instead used, one has observed what has come to be known as 'remote epitaxy' [49] [50]. This means that the semiconductor atoms on top of graphene are affected by the potential field of the covalently bonded substrate material, and thus may adopt the atomic configuration of the substrate. Depending on the strength of the potential field, polar substrates can induce remote epitaxy through one, two or three monolayers of graphene [50]. Single-crystal semiconductor thin films have been demonstrated by remote epitaxy in MOCVD [49, 50] and MBE systems [50]. Recently, two-dimensional hexagonal boron-nitride (h-BN) has been used as a growth substrate to decouple the substrate effects from the GaN-based nanowire growth [92].

The reactive nitrogen plasma used for GaN/AlN growth by MBE has been shown to be damaging to graphene [93], as well as introducing dopants in the form of substitutional N [94]. Thus, measures must be employed to protect the graphene if one wishes to preserve its electronic properties after growth. One such measure

is the growth of a protecting AlN buffer layer [20, 84], as AlN nucleates faster on graphene than GaN due to the higher adsorption energy of Al adatoms.

## 2.4 Hybrid semiconductor-graphene devices

The research on carbon-semiconductor contacts started in the early 1900s, with the Ralph Hartsough at the University of Kansas formed a point contact between C and Si [95]. Some research on graphite-Si and amorphous C-Si junctions was conducted in the 1960s and 1970s [96, 97], but it was not until controlled synthesis of carbon allotropes was achieved in the 1990s that this field really evolved. Graphene has been used as the main or one of several components in a variety of electronic and optoelectronic devices. Transistors [48], solar cells [98], photodetectors [99], spintronics [100], LEDs [101] and lasers [102] are examples of device categories. In this chapter I will limit the discussion to the theory and examples directly related to the fabricated structures and devices.

### 2.4.1 Graphene-Si photodetectors

The difference in electron affinity between graphene and Si results in a Schottky barrier where the barrier height depends on the doping of both components. The junction is sensitive to illumination in broadband wavelengths when operated as a photocurrent device and also sensitive to weak signals when operated as a photovoltaic device [103, 104]. Taking advantage of graphene's transparency to light, photoexcitation can take place in Si while graphene functions as the carrier collector, exemplified in Figure 2.6(a). Due to a non-ideal interface, An et al. hypothesised that native oxide on Si leads to pinning of the Si energy bands to surface states, limiting carrier collection around zero bias [103]. Crystalline Si produced by AIC is intrinsically p-doped, and the expected Schottky junction with graphene is shown in Figure 2.6(b). The work function of intrinsic graphene is 4.5 eV, and CVD graphene is normally found to be lightly p-doped, increasing the work function [105]. Barrier heights of graphene/n-Si and graphene/p-Si have been found to be 0.8 eV [103] and 0.48 eV [105], respectively.

Most demonstrated graphene-Si photodetectors use exfoliated or CVD graphene transferred to crystalline Si, as first demonstrated by Li et al. in 2010 [106]. As described previously, this inevitably leads to native oxide forming on the Si surface and affecting the junction properties. In contrast, there are no examples of photodetectors fabricated by Si deposited on graphene. Initial material characterisation have been made, like the physical vapor deposition of Si on graphene for

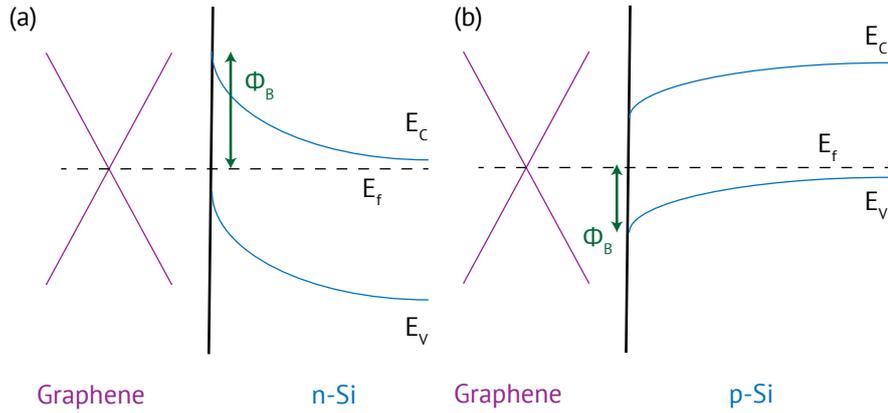


Figure 2.6: Band diagrams of (a) graphene/n-Si and (b) graphene/p-Si, under zero bias and no illumination.  $E_c$  and  $E_v$  denotes the conduction and valence band of Si,  $E_f$  refers to the Fermi level, and  $\phi_B$  denotes the Schottky barrier height.

crystalline thin films by Lupina et al. [107] and their subsequent work on amorphous Si deposited by plasma-enhanced CVD [108]. This work resulted in the fabrication of a graphene/n-doped amorphous Si diode device in 2017 [109]. Here, the barrier height was found to be lower than previous reports of such structures, at 0.49 eV, and this was attributed to the lack of Fermi-level pinning due to an oxide-free interface between graphene and Si.

A graphene-Si photodetector can work in different modes, which in turn allows tailored optical wavelength detection. If the incoming photons have an energy higher than the semiconductor bandgap, electron-hole pairs are mostly generated in the depletion layer of the semiconductor and their energies correspond to the semiconductor bandgap. If the incoming photons have an energy lower than the semiconductor bandgap but higher than the Schottky barrier between graphene and Si, electron-hole pairs can be generated in graphene, and this latter mode can be used for infrared photodetection [110].

### 2.4.2 III-Nitride based nanowire-graphene ultraviolet light emitting diodes

The most prominent advantages of a III-N nanowire LED over a conventional thin-film LED are the elimination of thick buffer layers due to efficient lattice relaxation [111], potential light guiding [112] and abrupt heterostructures [113]. Furthermore, efficient p-doping, which is one of the largest challenges for AlGaN LEDs, can be more efficient in nanowires due to the higher surface solubility of Mg [114]. A record-breaking nanowire LED grown with pure AlN on Si was demonstrated in 2014 by Zhao et al. [21], reaching an internal quantum efficiency of 80% at an emission wavelength of 210 nm.

Ultraviolet light emitting diodes (UV LEDs) based on GaN/AlGaN nanowires have been demonstrated both by RF-MBE [115] [116] and MOCVD [117], and on different substrates. However, although Ren et al. claim to have grown a full LED device structure by MOCVD, they do not show IV or EL data to support their claim [117]. The most common substrates are GaN [118], sapphire [119, 120] and Si [21, 113, 121–127], but recently more unconventional substrates like diamond [128] and metal films [129, 130] have also been used. A GaN-based LED grown on a two-dimensional material substrate was demonstrated by Zhao et al in 2017 [131], and consisted of a InGaN/GaN blue and yellow LED emitting at 635 nm.

The first III-nitride based LED grown on graphene was demonstrated by Chung et al. in 2014, where they grew GaN microrods with InGaN quantum wells resulting in an emission peak at 439 nm [132]. In this case the whole structure was delaminated from the SiO<sub>2</sub>/Si substrate and the graphene was not used as a transparent electrode. As discussed in chapter 2.3 and shown in Figure 2.3 (b), the high transparency of graphene in the ultraviolet region of the electromagnetic spectrum makes it ideally suited as a transparent electrode for optoelectronic devices operating in this region. It has therefore been used as a transparent electrode for thin-film [133–135] and nanowire [136] III-nitride-based UV LEDs, also functioning as a current spreading layer.

## Chapter 3

# Experimental methods

This chapter describes the experimental methods most central to this thesis.

### 3.1 X-ray diffraction spectroscopy

X-rays of light have wavelengths similar to to the interatomic spacing of crystalline materials, and x-ray diffraction (XRD) is therefore commonly used to gain information on the lattice spacing of a material. The basis for the technique is the relationship between the scattering of a coherent light wave from a crystalline solid and the spacing of atomic planes of that solid. The relationship when constructive interference is achieved is described by Bragg's law [137], where  $n$  is an integer,  $\lambda$  is the wavelength of the incident light wave,  $d$  is the lattice spacing of the crystal, and  $\theta$  is the angle between the incident light wave and the crystal surface plane:

$$n\lambda = 2d \sin(\theta) \quad (3.1)$$

Constructive interference is shown in Figure 3.1. The lattice spacing  $d$  of a cubic crystal is related to the lattice parameter  $a$  through the relationship

$$d = \frac{a}{\sqrt{h^2 + k^2 + l^2}} \quad (3.2)$$

where  $h$ ,  $k$  and  $l$  are miller indices.  $d$  thus depends on the orientation of the crystal.

By scanning a detector across a range of angles, the angle(s) of constructive interference can be determined, and as the light source wavelength is known the

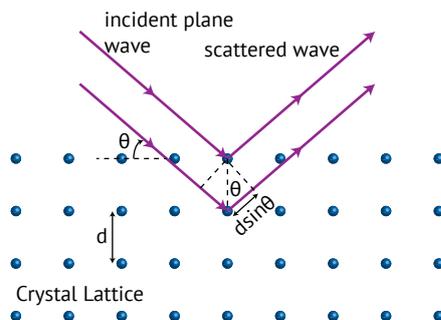


Figure 3.1: Constructive interference of coherent light by scattering in a crystal lattice, also known as Bragg's law.

lattice spacing can be determined. These scans are typically done as  $2\theta/\omega$  scans, where  $\omega$  is the aligned angle of the crystal plane [138].  $2\theta/\omega$  scans have been used in this thesis to determine the presence and orientation of Si crystallised by the AIC method. XRD is a macroscopic technique, revealing information of an area across the sample determined by the cross-section of the incoming light wave, typically a few  $mm^2$ .

The XRD system at NTNU is a D8 HRXRD system equipped with a copper filament ( $\lambda = 1.5406 \text{ \AA}$ ) yielding an unfiltered intensity of 170 000 000 cps (counts per second). The generator is normally set to 40 kV and 40 mA, using a pre-warming step of 30 min before starting scans.  $\omega$  is found by doing three consecutive z- and rocking curve-scans on the sample surface with increased accuracy [139].

## 3.2 Raman spectroscopy

When light interacts with molecules and crystals, in the form of a vapour, liquid or solid, vibrational modes in the molecules or phonons in a crystal can absorb some of the energy of the light. The inelastically scattered light therefore has a slightly lower energy than the incident one, and this is known as a Stoke-shift, while the scattering is termed Raman scattering [140]. Different molecules and crystals have distinct energy shifts, making it possible to identify them by doing such measurements. This is the basis for Raman spectroscopy, where a laser beam is focused on sample material and the energy shift of the scattered light is recorded. The elastically scattered light (Rayleigh scattering) is filtered out. If the laser beam

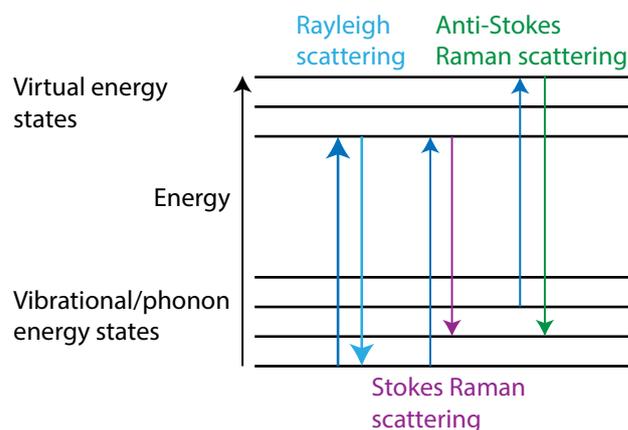


Figure 3.2: Raman spectroscopy takes advantage of Raman scattering, where the molecule or crystal is put in a virtual energy state before emitting inelastically scattered light.

can be focused into a small spot, it is termed micro-Raman spectroscopy.

The vibrational modes and phonons are closely related to the type of binding occurring in the material, making it possible to identify different isomers, phases, defects and strain in the material tested. When the laser beam excites the sample, the molecule or crystal adopts a virtual energy state, before a photon is re-radiated or what we term scattered. If the scattering is inelastic meaning the emitted photon has a different energy than the excitation photon, the molecule or crystal is left in a different vibrational state as seen in Figure 3.2. If the re-radiated light has a lower energy than the incident we call it Stokes Raman scattering, and if the light has a higher energy it is called anti-Stokes Raman scattering. The intensity of Stokes Raman scattering is normally higher than that of anti-Stokes scattering, and is therefore commonly used for spectroscopy.

The unit used in Raman spectroscopy is normally wavenumber( $\text{cm}^{-1}$ ) and not wavelength, as this is linearly related with energy and makes the Raman shift independent of incident laser beam wavelength. The Raman system at NTNU consists of a confocal micro-Raman Renishaw InVia Reflex Spectrometer system with lasers for VIS excitation (532 nm, 100 mW) and NIR excitation (785 nm, 300 mW). It has a spectral resolution below  $1 \text{ cm}^{-1}$  and a TE cooled CCD detector. The smallest laser spot size achievable is  $1.5 \mu\text{m}$ , and the smallest step size of the stage is 100

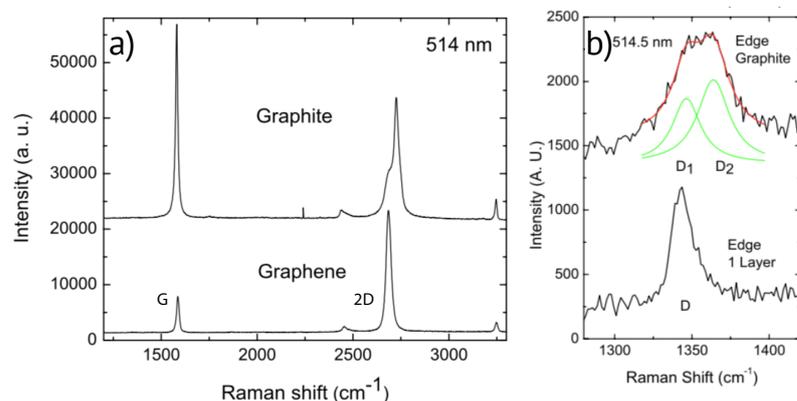


Figure 3.3: Raman spectroscopy of graphite and a single graphene layer, showing (a) the G- and 2D-peaks and (b) the D-peak near the edge of the sample where disorder is introduced [143].

nm.

### 3.2.1 Raman spectroscopy of graphene

The Raman spectrum of graphene has a few very distinct features, as shown in figure 3.3. The G band at  $1582\text{ cm}^{-1}$ , the G', or 2D, band at  $2700\text{ cm}^{-1}$  and the disorder-induced D band at  $1350\text{ cm}^{-1}$ , assuming a laser excitation wavelength of  $514\text{ nm}$  [141]. The G band is the only band arising from a normal first order Raman scattering event, and is associated with the iTO and LO phonon modes at the Brillouin zone center. The G' and D bands are both from second-order processes, associated with two iTO phonons near the K point for the G' band, and one iTO phonon plus one defect for the D band. A fourth band, D', located at  $1620\text{ cm}^{-1}$  can also appear for samples with induced disorders. The D and G' bands both exhibit dispersive behaviour, meaning that their position in the Raman spectrum changes with laser excitation energy. The frequency of the D band changes with  $50\text{ cm}^{-1}/\text{eV}$  while the frequency of the G' band changes with  $100\text{ cm}^{-1}/\text{eV}$  [141, 142].

The position, width and shape of the G' band, as well as the ratio of the G to G' band, can be used to determine the number of graphene layers. Figure 3.4 shows the different G' peaks measured for graphene with one, two, three or four layers with ordered stacking. When the stacking is not ordered, the G' peak does

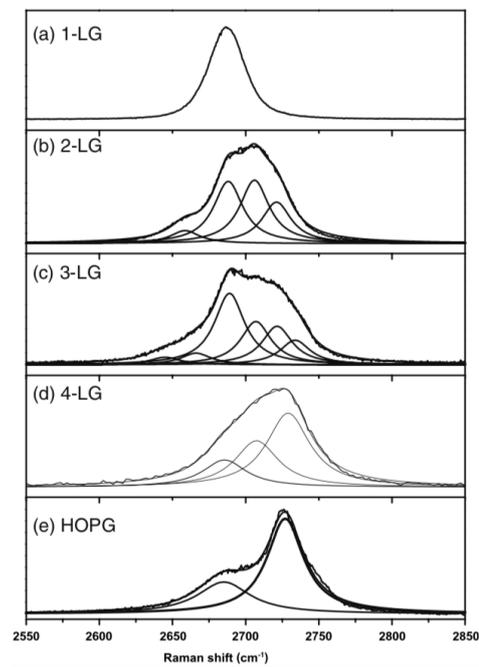


Figure 3.4: Raman spectroscopy of the G' (2D) peak shows the dependency on the number of graphene layers. This is shown for (a) monolayer graphene, (b) bilayer graphene, (c) three layers of graphene, (d) four layers of graphene and (e) turbostratic graphite. Figure from [141].

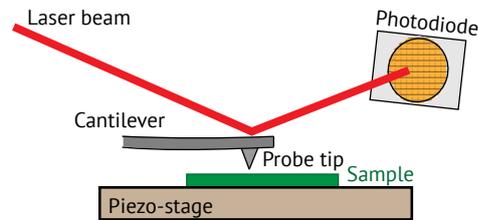


Figure 3.5: Basic principles of an atomic force microscope.

not change its appearance to such a large extent, and the ratio  $I_G/I_{G'}$  can be used to indicate the number of layers as well [144]. The positions of the G and G' peaks indicates the amount of strain and doping present in the graphene [145], and these two mechanisms can be decoupled by the analysis method developed by Lee et al [146], where they show that the two mechanisms can be revealed by distinct linear relationships between  $\Delta\omega_G$  and  $\Delta\omega_{G'}$ .

### 3.3 Atomic force microscopy

Imaging structures on the nanoscale can be quite challenging. A technique that has proven successful at this is atomic force microscopy (AFM), where a very fine probe is scanned on or close to the surface of the sample, recording the atomic forces between the probe and sample. As the equipment and software used to perform AFM has matured, tapping-mode has taken over for the original contact scanning mode [147]. As shown in Figure 3.5, this means that the cantilever with the probe tip is oscillating at a resonance frequency, trying to keep a constant amplitude and thus a constant distance from the sample surface. When the height difference changes, the amplitude becomes smaller or larger, and this change is recorded by a laser beam that is reflected off the backside of the probe. The laser beam is reflected onto a photodiode which records the change in amplitude and the software converts this to a force and then to a height measurement. The sample is scanned underneath the probe tip by a piezo-electric xyz-stage.

The AFM system at NTNU is a Veeco Multimode V AFM with Nanoscope software.

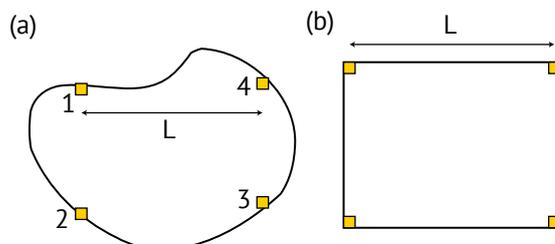


Figure 3.6: Typical van der Pauw measurement, for a sample of (a) arbitrary shape and (b) rectangular shape. Metal electrodes are indicated in yellow, and  $L$  is the distance between contacts.

### 3.4 Electrical characterisation

Electrical characterisation methods have been used to probe the electronic properties of the materials investigated in this thesis. While Raman spectroscopy can be used to evaluate the defect density in graphene, van der Pauw measurements can be used to reveal the effect of these defects on the conductivity of the graphene sheet. The most characteristic trait of a pn-junction is its rectifying effect on carrier transport, and therefore current-voltage (I-V) measurements are commonly used to evaluate these junctions.

#### 3.4.1 Van der Pauw method

To accurately determine the resistivity of a sample by the van der Pauw method [148], the sample has to fulfil the following requirements: the sample must be much thinner than it is wide, continuous, homogeneous, and the contact pads/electrodes must be placed on the perimeter of the sample and be at least one order of magnitude smaller than the total area to be measured. Four probes are used to perform the measurement, and a typical setup is shown in figure 3.6.

A dimensional-less quantity called the sheet resistance with the unit ohms/square ( $\Omega/\square$ ) is directly measured via the van der Pauw method, and if one also knows the thickness of the sample the resistivity can be calculated as well. The sheet resistance is found by numerically solving equation 3.3, where  $R_{12,34}$  is the resistance found by dividing the current measured between electrodes 1 and 2 with the voltage applied across electrodes 3 and 4. The precision can be further improved by measuring the reciprocal values ( $R_{34,12}$  and  $R_{41,23}$ ) and both polarities.

$$e^{-\pi R_{12,34}/R_S} + e^{-\pi R_{23,41}/R_S} = 1 \quad (3.3)$$

The resistivity  $\rho$  is given by  $\rho = R_S * t$  where  $t$  is the thickness of the sample. Van der Pauw measurements at NTNU were performed with a Lakeshore Hall Effect Measurement System.

### 3.4.2 I-V measurements

Current-voltage measurements can be used to characterise the junction properties and system losses of semiconductor interfaces, including rectifying junctions termed diodes. A typical IV curve for a diode is shown in Figure 3.7 and important regions are indicated. When biased in reverse, a small amount of current still flows through the diode, termed the leakage current, which is normally considered as negligible. However, alternative current paths and poor junction design can increase this entity. If the diode is biased at a strong reverse bias, it reaches its breakdown voltage and becomes conductive. The forward current divided by the reverse leakage current at a given voltage yields the diode on-off ratio, which is a figure of merit and is most often desired to be as high as possible. The turn-on voltage,  $V_f$ , from the IV-graph of the diode does not have a precise definition, but commonly an interpolation of the linear region of the forward current is used, and the intersection with the voltage axis is chosen as the "on" voltage [149]. The bandgap of the material influences the turn-on voltage, without there being a strict relationship. But in general, materials with higher band gaps have higher turn-on voltages, with the extreme case of 210 nm AlN LEDs having a turn-on voltage of around 6-8 V [21]. The slope of the linear region of the forward current can be approximated to the series resistance of the system, and is composed of resistance from the semiconductor and resistance from the contacts to the semiconductor.

The forward IV characteristics of AlGaN UV LEDs can be modelled with a three-diode circuit, as deep level trap states are expected to contribute to the current leakage beneath the turn-on voltage [150].

The IV measurements presented in this thesis were done with a Keithley 2636A sourcemeter connected to a Cascade probe station by triaxial connections. The 2636A sourcemeter enables measurements in the picoampere range at an accuracy of <0.15%.

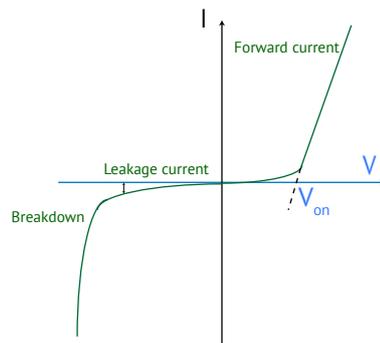


Figure 3.7: Typical IV sweep measurement of a diode, where important regions have been indicated.

## 3.5 Electron microscopy

An important tool for the precise measurement and characterisation of nanostructures is electron microscopy. The dimensions, morphology and yield of nanowires is measured by scanning electron microscopy (SEM), while more detailed features, crystal structure, defects and elemental composition is characterised by Transmission Electron Microscopy (TEM).

### 3.5.1 Scanning electron microscopy

In SEM, the sample is placed in a vacuum chamber, where a high voltage focused electron beam is used to image the sample surface. The electron beam is generated by a filament, and most newer SEMs have a field emission cathode as the filament. When the beam hits the sample, a number of processes occur that can be utilised for imaging. These processes are shown in Figure 3.8(a) and (b), and are all based on different energy transfer mechanisms. In SEM, the electrons emitted through the top surface can be collected and used to form an image of the sample. If the incident electron collides directly with an atom in the sample, the incident electron can be scattered  $180^\circ$  backwards, and this is termed backscattered electrons. The amount of backscattered electrons (BSE) scales directly with the atomic number of the sample  $Z$ , and can therefore be used to distinguish areas with different elements. If the incident electron passes near one of the atoms in the sample, it can transfer some of its energy to one of the lower energy electrons in the sample atom, ionizing

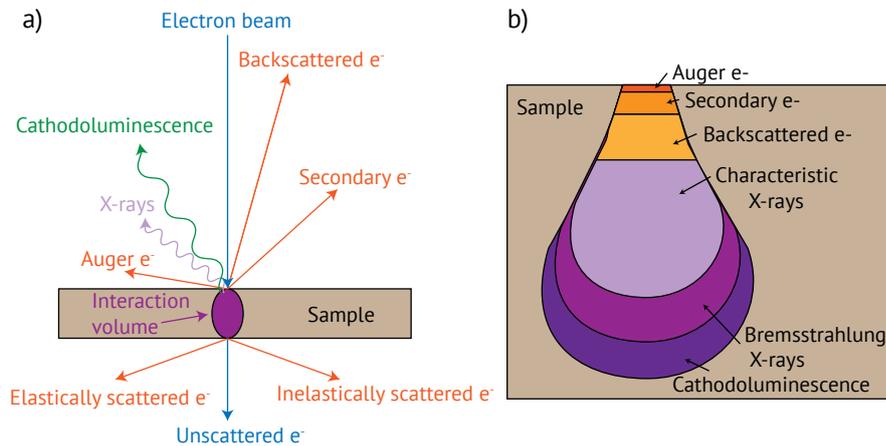


Figure 3.8: When a high energy electron interacts with a sample, (a) different energy transfer mechanisms can occur in the form of emitted electrons or photons. (b) The interaction volume of the different mechanisms.

it. This electron can then escape the sample, but as it has a low energy ( $< 50$  eV) only electrons from the surface of the sample can escape as secondary electrons (SE). These electrons are collected to image the surface of the sample. When the lower energy level in the atom that now has a missing electron is filled by one of the higher energy electrons, the surplus energy can be lost in the form of Auger electrons. The Auger electrons have energies characteristic to the element they escaped from, and can give compositional information on the sample. An image of the sample is formed by scanning the electron beam across the sample and collecting the electron signal [151].

The electrons that escape the sample can be collected by detectors either positioned at an angle to the sample surface (SE signal) or perpendicular to the sample surface (BSE signal). The electrons are accelerated towards a scintillator or semiconductor detector, connected to a photomultiplier which outputs a two-dimensional intensity distribution that can be recorded as an image.

### 3.5.2 Transmission electron microscopy

If the sample is thin enough and the incident electron beam electrons energetic enough, some of the electrons will be transmitted through the sample, or lamella,

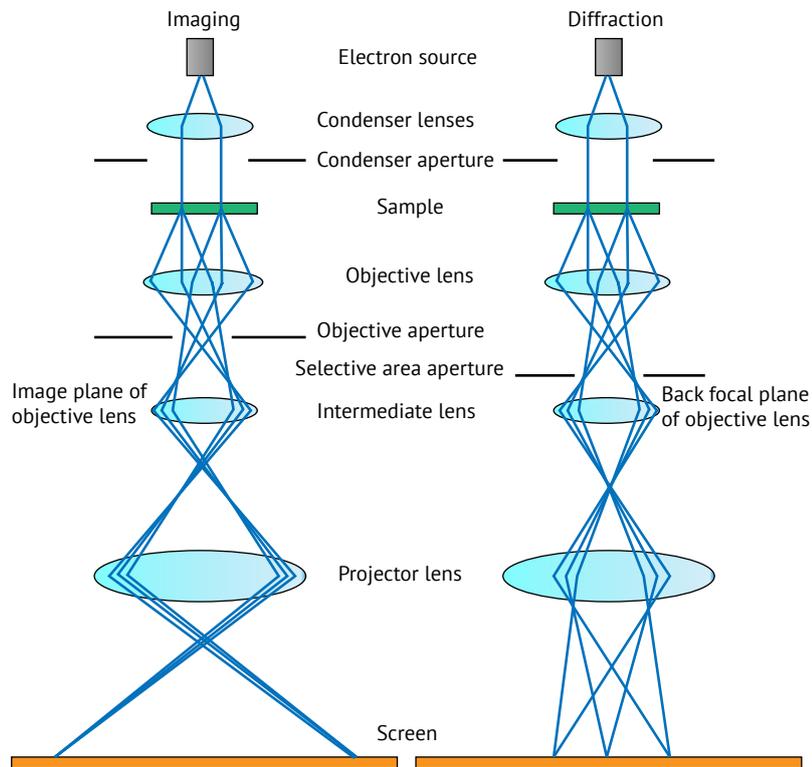


Figure 3.9: Two main operation modes of transmission electron microscopy; imaging mode and diffraction mode.

as shown schematically in Figure 3.8(a). A contrast can be detected through varying intensity of the transmitted electron beam due to thickness or absorption variations in the sample. For higher resolution images one has to take into account the wave-nature of electrons, and the image analysis becomes more complicated. There are two main operation modes in a TEM; imaging mode and diffraction mode, as shown schematically in Figure 3.9. Diffraction mode is achieved by placing the back focal plane of the objective lens on the imaging screen. For a sample consisting of a single crystal, the diffraction pattern is a series of dots, while a polycrystalline or amorphous sample will show a series of rings. The reason for diffraction is that the atom columns in the sample act as a diffraction grating for the incident electrons when oriented in certain directions, and the electrons will therefore scatter to particular angles. The diffraction pattern gives the atomic plane distances in reciprocal space, and can therefore be used to calculate the lattice spacing in the sample material and thus identify the different components as well as crystal orientation, phase and material strain [152].

The techniques discussed thus far have been based on the detection of the main beam and low-angle scattered electrons, while the electrons scattered to higher angles can also yield information about the sample. The amount of scattering depends on the atomic number of the sample elements, as heavier atoms will diverge the incident electron more. This is taken advantage of in high-angle annular dark field TEM (HAADFTEM), where the main beam is blocked while the high-angle scattered electrons are collected and used to form an image with contrast dependent on element composition. There are several other functionalities available in the TEMs used at NTNU, like scanning TEM (STEM), electron energy loss spectroscopy (EELS) and energy-dispersive x-ray spectroscopy (EDS). EELS uses the energy difference in inelastically scattered electrons to identify element composition while EDS uses the characteristic x-rays escaping the sample.

## 3.6 Optical characterisation

The optical properties of the semiconductor nanowires described in this thesis have been probed with two main techniques; optically pumped photoluminescence spectroscopy (PL) and electrically biased electroluminescence spectroscopy (EL).

### 3.6.1 Photoluminescence spectroscopy

When a crystal or molecule is excited by an optical pump, typically a laser beam, electrons are excited to a higher energy level after the absorption of a photon. When

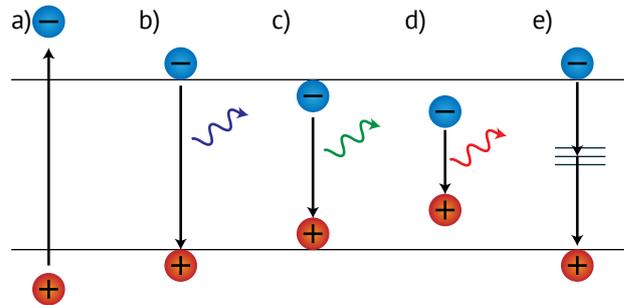


Figure 3.10: Different recombination routes for excited electrons and holes. (a) Excitation of an electron from the valence to the conduction band. (b) Relaxation to the band edge and band-to-band recombination. (c) Free exciton recombination. (d) Bound exciton recombination. (e) Deep-levels within the band gap suppress radiative recombination.

the crystal or molecule relaxes again, light is emitted as the electrons transition from a higher to a lower energy level through a recombination process. The emitted light can be collected and used to understand the electronic structure of the investigated sample. These are the very basic principles behind  $\mu$ - and macro-photoluminescence spectroscopy ( $\mu$ - and macro-PL), which is an important technique to investigate the electronic and crystal structure of nanowires [16].

When the electrons in a semiconductor are excited from the valence band to the conduction band by a laser with an energy higher than the band gap ( $E_g$ ) (Figure 3.10(a)), the electron undergoes thermal relaxation, which is the loss of energy to phonons, until it reaches the edge of the conduction band. From here, it undergoes a recombination process where it recombines with a hole in the valence band, and depending on the crystal structure, crystal quality and temperature, the recombination process can take different routes. At higher temperatures, band-to-band recombination normally dominates, as shown in Figure 3.10(b). As the temperature decreases, excitons become more prominent. An exciton is a quasi-particle consisting of an electron-hole pair. The free exciton has a higher emission energy than a bound exciton as seen in Figures 3.10 (c) and (d), where the latter is the case of an exciton binding to an acceptor (p-doping) or donor (n-doping) site. If the semiconductor has defects as the example in Figure 3.10(e), deep levels within the band gap can lead to non-radiative recombination of an electron and hole [153].

The setup used at NTNU is shown in Figure 3.11, where a Nd:YVO Spectra

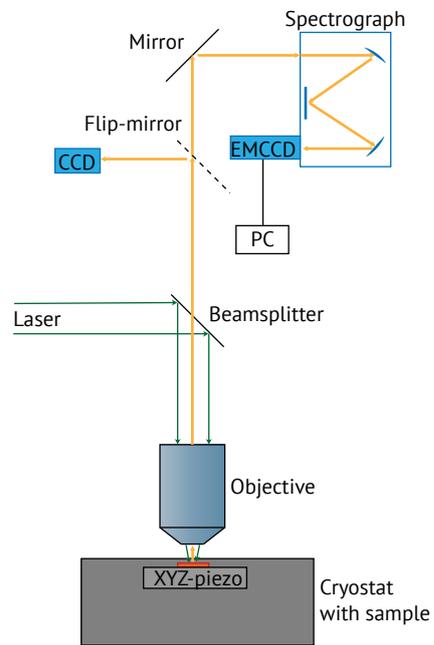


Figure 3.11: Schematic of setup used for photoluminescence measurements.

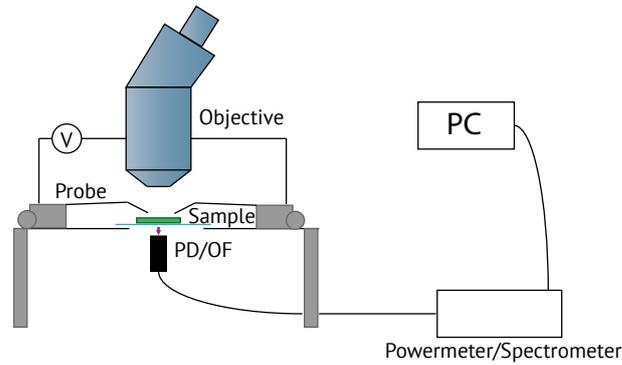


Figure 3.12: Schematic of setup used for electroluminescence measurements.

physics Millennia excitation source operating at 532 nm or a Kimmon Koha He-Cd laser operating at 325 nm is used to excite the sample with a continuous wave (CW) or pulsed laser beam, after being focused by a microscope objective. The sample is placed on a XYZ piezo stage which together with a flippable mirror that can direct the reflected signal to a charge coupled device (CCD) camera allows for precise excitation spot control. The piezo stage is positioned inside a cryostat, that by the use of liquid He can reach a temperature of 10K, so that temperature-dependant measurements can be performed. The signal is dispersed in by a spectrometer and the  $\mu$ - or macro-PL spectrum is detected by an electron multiplying CCD (EMCCD) for the CW measurements.

### 3.6.2 Electroluminescence spectroscopy

In EL, IV measurements are combined with either a photodiode or a spectrometer, to gain information on light emission due to radiative recombination of electrons and holes under current injection. In order to carry out the measurement, the sample must be processed so that electrical contacts can be made to both sides of the semiconductor or heterostructure p-n junction, and the semiconductor material must be conductive, which is normally achieved by doping it with acceptor or donor impurities. The setup used to measure the electroluminescence of AlGaIn/GaN nanowires in Paper III is shown in Figure 3.12. The sample is placed on a UV-transparent glass-slide, and two micromanipulators are used to place the probe tips on the contact metal pads of the sample. An optical microscope is used to position the probes correctly. A bias is applied between the two probes, and high-energy

electrons are fed into the semiconductor sample material to recombine with holes traveling the opposite way. To measure the optical emission power, a photodiode (PD) is used, and light of all wavelengths is collected and the intensity is recorded as optical power with the unit of Watts. A spectrometer with an optical fiber (OF) is used to collect the spectrum of the light emission, where a diffraction grating is used to separate the wavelength components of the incident light and a slit selects one component at the time so the intensity can be recorded at the detector, typically a charge-coupled device (CCD).

### 3.7 Electrical and optical characterization of LEDs

The two techniques described in chapters 3.4.2 and 3.6.2 can be combined to extract important information on the performance of LEDs. Some of the information is related to the material quality of the device, and some to the device design. The most important parameters to determine are related to the conversion of electrical energy to light energy as well as the extraction of the energy and are [154]:

- Internal Quantum Efficiency (IQE)
- Light Extraction Efficiency (LEE)
- External Quantum Efficiency (EQE)
- Wall Plug Efficiency (WPE)

The IQE is a measure of the number of emitted photons compared to the number of injected electrons to the active region of the LED, and can be calculated as the injection efficiency ( $\eta_{inj}$ ) multiplied by the radiative recombination efficiency ( $\eta_{rad}$ ):

$$IQE = \eta_{inj} * \eta_{rad} \quad (3.4)$$

$\eta_{rad}$  is the fraction of all electron-hole pairs that recombine radiatively in the active region of the device and can be expressed as the ratio of the radiative recombination ratio over the sum of the radiative and non-radiative recombination rates  $r_r$  and  $r_{nr}$ :

$$\eta_{rad} = \frac{r_r}{r_r + r_{nr}} \quad (3.5)$$

### 3.7. Electrical and optical characterization of LEDs

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The non-radiative recombination rate can be described as the sum of Shockley-Read-Hall (SRH) recombination and Auger recombination, where the SRH recombination is strongly influenced by the defect density of the material while the Auger recombination is material-specific [154].

The IQE can also be measured by temperature and excitation power-dependent photoluminescence spectroscopy (sect 3.6.1). The EQE of the LED can be directly measured from the comparison of optical power output with current injection, and depends on the emitted photon energy  $h\omega$ :

$$EQE = \frac{e * P_{out}}{I * h\omega} \quad (3.6)$$

The LEE is a measure of the ability of the emitted photons to escape the LED structure and be detected by the spectrometer. Re-absorption in different layers either by lower bandgap material or defects, internal reflections and metal-contact absorption all contribute to lowering the LEE, reducing the efficiency of the LED. The EQE is related to the internal quantum efficiency and light extraction efficiency by the relationship

$$EQE = IQE * LEE \quad (3.7)$$

The EQE is independent of the energy of the injected electrons, so in order to consider the full energy balance equation, the wall plug efficiency must be calculated via the equation

$$WPE = \frac{P_{out}}{I * V} = EQE * \frac{h\omega}{e * V} \quad (3.8)$$



## Part II

# Unpublished results



## Chapter 4

# Clean graphene transfer

One of the main obstacles preventing the integration of graphene with semiconductor materials is the lack of clean, large-scale graphene sheets. Here, clean means graphene without metallic and organic residues from the transfer process used to move the graphene sheet to an insulating substrate. Exfoliated graphite is per this definition clean, but is challenging to work with as it yields small flakes ( $<100 \mu\text{m}$ ) with arbitrary shape and position. Over the course of this thesis, several processes have been tested to try and achieve CVD graphene clean enough to be used as a substrate for NW growth by MBE. There are three major challenges that each has to be solved to achieve a clean transfer:

- Metallic residues from the etching of metal growth catalyst.
- Impurities introduced through transfer wet processes, e.g. Fe ions from etching process and alkali ions from electrolyte.
- Organic residues from polymer support layer used during transfer.

### 4.1 Metallic residues on graphene

The first item is partially solved by using a Pt metal catalyst instead of traditional Cu, as Pt is compatible with the MBE environment and less mobile than Cu. Our Korean collaborators have developed a CVD process for producing large-area single-layer graphene grown on a Pt catalyst [155], and this graphene has been used by us for the transfer process development. Furthermore, the amount of metallic residues

can be reduced by using an electrochemical transfer instead of the etching of the metal catalyst [69]. Several techniques can be used to evaluate the contamination, and in this project Time-of-Flight Secondary Ion Mass Spectroscopy (ToF-SIMS) and X-ray Photoelectron Spectroscopy (XPS) were used [156]. ToF-SIMS is a very sensitive spectroscopy technique, where an ion beam is used to sputter the top surface layer of the sample, and the ejected ions are accelerated by an electric field and collected by a detector that resolves their speed and thus mass. XPS utilises an x-ray beam to excite electrons in the surface of the sample, which emit light when they relax. The energy of the emitted light depends on the electronic configuration of the molecule or crystal, and is very sensitive to the immediate environment of the electron. This trait is used to measure the state of the surface atoms. ToF-SIMS can detect concentrations of ions down to  $10^{12}$  atoms/cm<sup>3</sup>, much lower than XPS, but cannot be used to separate e.g. different allotropes of carbon, which is why XPS is commonly used to measure the amount of organic residues on graphene while ToF-SIMS can be used to measure metallic residues.

We compared the metallic residues of common contamination metals for samples grown either on Cu or Pt substrates and processed with different transfer techniques. All of the graphene sheets were transferred to standard 300 nm SiO<sub>2</sub>/Si substrates so that the ratios of metal ions to Si ions could be quantitatively compared. The results are summarised in Figure 4.1. The results show, amongst other things, that graphene grown on Cu foil at NTNU and transferred by electrochemical delamination has less metal contamination than commercially purchased graphene from GrapheneA transferred by wet etching. Furthermore, both graphene grown on Pt at NTNU and Sejong University has less Cu contamination than the commercially purchased graphene from GrapheneA, which is grown using a Cu catalyst.

Using a sacrificial layer of Au during graphene transfer has been demonstrated by Lee et al. [157], but as Au is not CMOS-compatible we used In as a sacrificial layer. It has also been shown that a thin layer of Ti can be used to clean graphene [158].

## 4.2 Alkali ion contamination from electrolyte

The standard electrolyte used for electrochemical delamination (ED), which is described in more detail in Section 2.3.1, is sodium hydroxide (NaOH) [70]. However, the alkali Na ions could be a contamination source if the graphene has to be CMOS-compatible in later processes. The same goes for Ka ions. For these reasons, we tested graphene transfer with two different types of electrolyte; citric acid (C<sub>6</sub>H<sub>8</sub>O<sub>7</sub>) and ammonia solution (NH<sub>4</sub>OH). A concentration of 0.25 M for the citric acid and 5% for the ammonia solution was used. C<sub>6</sub>H<sub>8</sub>O<sub>7</sub> worked well as an electrolyte at

## 4.2. Alkali ion contamination from electrolyte

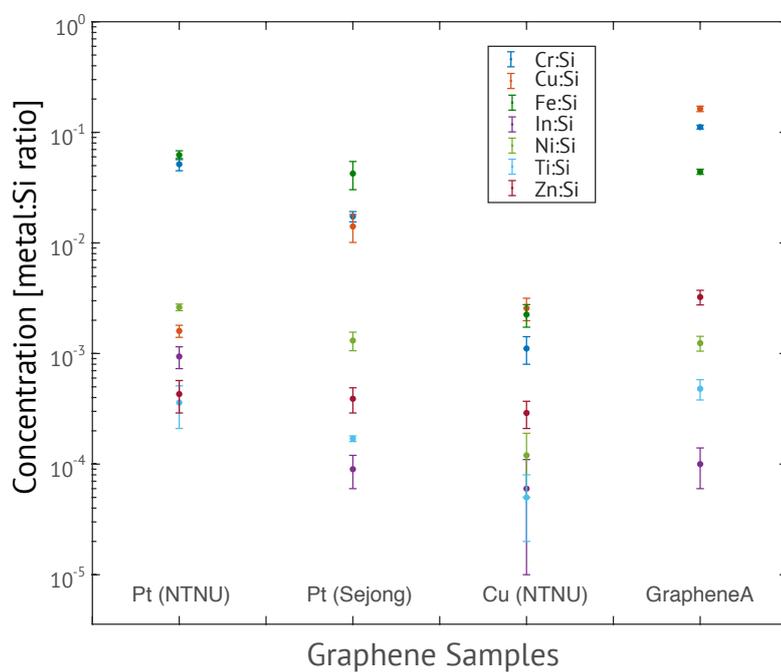


Figure 4.1: ToF-SIMS measurements showing the ratio of sputtered metal to Si ions for graphene grown on Pt at NTNU, graphene grown on Pt at Sejong University, graphene grown on Cu at NTNU and commercially purchased graphene from GrapheneA.

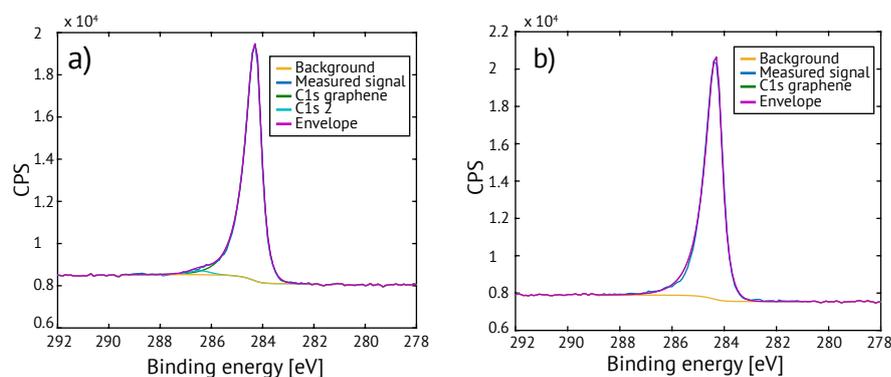


Figure 4.2: XPS C1s spectrum from pristine graphene grown on Pt (a) before and (b) after annealing at 300°C.

one occasion, where the graphene was completely delaminated from the Pt substrate. However, the experiment could not be repeated at later occasions. When  $\text{NH}_4\text{OH}$  was used as the electrolyte, complete delamination could consistently be achieved under a bias of  $\sim 4.5$  V and  $\sim 1$  mA, albeit slower than ED with NaOH, with transfer times ranging from 30 to 60 minutes. This is consistent with other reports [72, 159], where the ion intercalation of  $\text{Na}^+$  is found to be faster than the ion intercalation of  $\text{NH}_4^+$ .

### 4.3 Organic residues on graphene

By organic residues, we mean carbonic molecules which are remnants from the polymer used to support the graphene layer during transfer. Such a support is used both for wet etching transfer and electrochemical delamination. After transfer, the polymer film is dissolved in acetone, and optionally the sample can be annealed in a hydrogen-rich atmosphere to 'burn' away the polymer residues further. As ToF-SIMS does not separate between carbon from the polymer and carbon from graphene, XPS and AFM is used to evaluate the amount of organic residues after transfer. Figure 4.2 shows the XPS spectra of a graphene sheet still attached to the Pt catalyst, showing only one single asymmetric peak with a FWHM of 0.5417 eV after 1 hour annealing at 300°C in vacuum. Figure 4.2a) shows the XPS spectrum of the transfer polymer we use, poly(methyl methacrylate) (PMMA). Using these

### 4.3. Organic residues on graphene

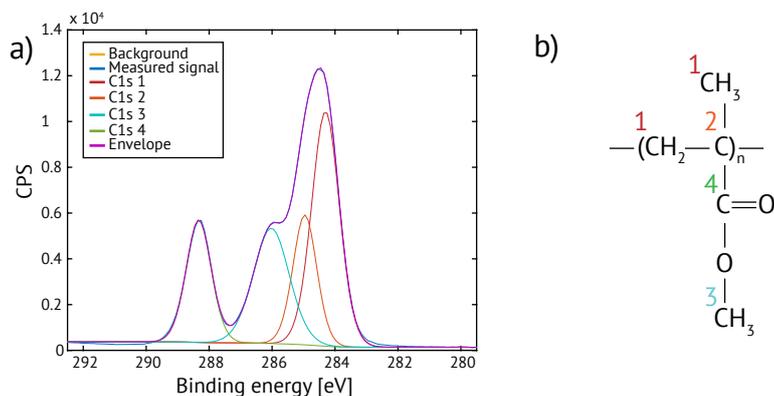


Figure 4.3: (a) XPS C1s spectrum from PMMA, fitted with the four peaks corresponding to the various carbon-hydrogen-oxygen bonds shown in (b) [160].

four peaks, which correspond to the bonds indicated in Figure 4.2b), together with the single graphene peak, the XPS spectrum of samples with PMMA residues can be fitted correctly.

Figure 4.4 shows a graphene layer transferred from Pt to SiO<sub>2</sub> by electrochemical delamination, with PMMA as the polymer support layer, before and after annealing at 600°C in vacuum for one hour. The PMMA signal is weaker after annealing, but still present, in contrast to the pristine graphene sample shown in Figure 4.2. In order to reduce these residues we attempted to cover the graphene with a thin layer of 15 nm In that was deposited before transfer, so that PMMA was never in direct contact with graphene. After the PMMA was dissolved in acetone, the sample underwent O<sub>2</sub> plasma ashing to remove PMMA, the In was etched by hydrochloric acid (HCl) and measured by XPS. These results are shown in Figure 4.5, and it appears that the annealing step at 600°C in vacuum for one hour almost completely removed the PMMA residues. This is in contrast to the sample transferred without In shown in Figure 4.4.

The organic residue concentration was also investigated with AFM for the samples shown in Figures 4.4 and 4.5, which yields qualitative results as only small areas on the sample can be analysed. The results are shown in Figure 4.6, where the sample transferred with In has many wrinkles, as well as less particles than the sample transferred without In. This is a further indication that the use of a sacrificial metal layer during transfer can lead to less carbonic residues.

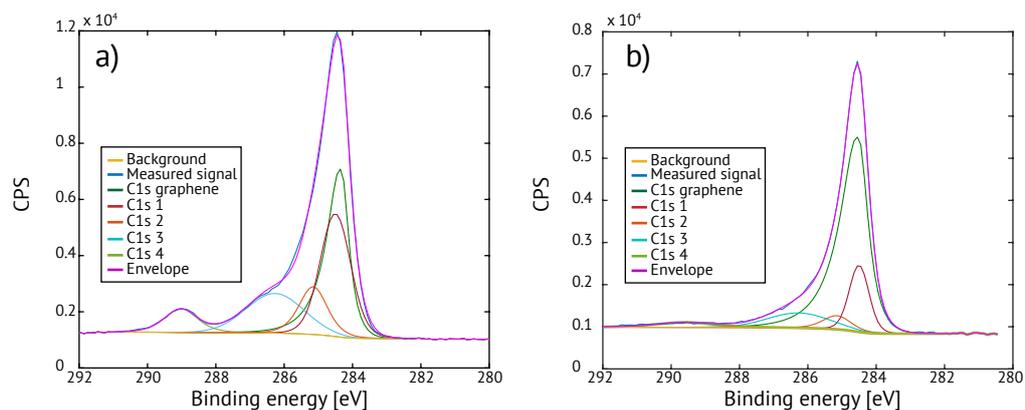


Figure 4.4: XPS C1s spectrum from graphene grown on Pt and transferred with electrochemical delamination (a) before and (b) after annealing in vacuum at 600°C for one hour.

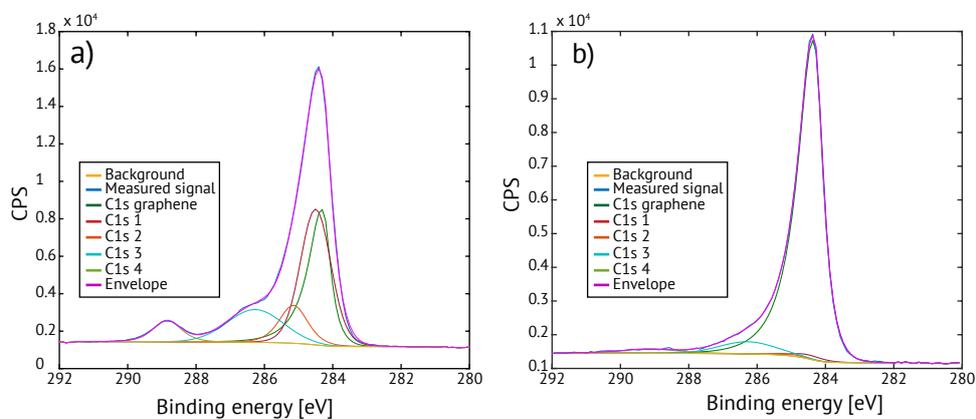


Figure 4.5: XPS C1s spectrum from graphene grown on Pt, covered with In and transferred with electrochemical delamination (a) before and (b) after annealing in vacuum at 600°C for one hour.

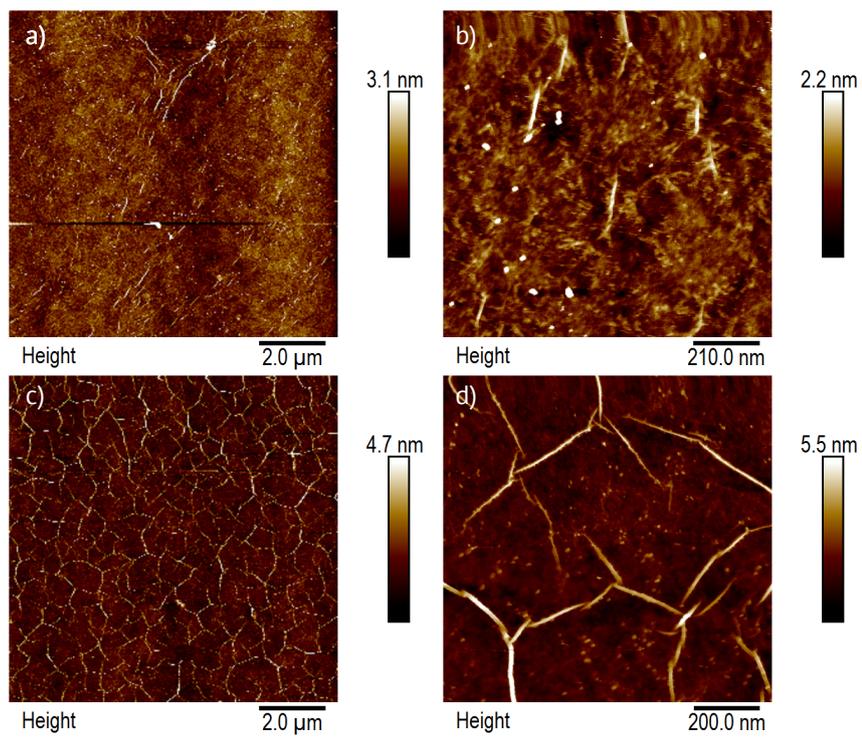


Figure 4.6: AFM scans of a graphene sample transferred (a,b) without In and (c,d) with In.

## 4.4 Challenges with the In sacrificial layer method

Although the In sacrificial method has been shown usable with graphene transfer from Pt substrates, we also experienced a number of challenges. The greatest challenge was the reliance on non-commercial graphene, as the graphene growth was continuously optimised, leading to large variations between samples. As the graphene was grown on thin sputtered Pt films on either SiO<sub>2</sub>, sapphire or fused silica, if the Pt film is too thin or the temperature under growth too high, the Pt will deform, leaving the substrate exposed. This leads to amorphous carbon regions that are not possible to delaminate. Reproducibility was also a considerable challenge due to the large variations between graphene samples. Removal of In could possibly damage graphene, or leave metal residues. Evaporation of In under vacuum was therefore tested, in contrast to the wet etching with HCl, but this led to damage of the graphene sheet. We still believe this transfer method has some merit, but reliable access to homogeneous graphene grown on Pt must first be ensured.

## Chapter 5

# Graphene-nanowire device processing and preliminary results

### 5.1 Graphene-nanowire device processing

Depending on what type of graphene is used, and what kind of device is developed, a range of techniques are utilised in the processing. The general steps in device processing are substrate preparation, mask deposition and patterning, semiconductor growth, device area definition and contact deposition, as shown in Figure 5.1. Characterization must be done as part of all processing steps to ensure a high degree of control of the process.

#### 5.1.1 Substrate preparation

There are three main substrates used during this thesis:

- Commercially purchased CVD graphene transferred onto fused silica
- CVD graphene transferred from Cu or Pt to SiO<sub>2</sub>/Si
- Exfoliated kish graphite transferred to Si or SiO<sub>2</sub>/Si

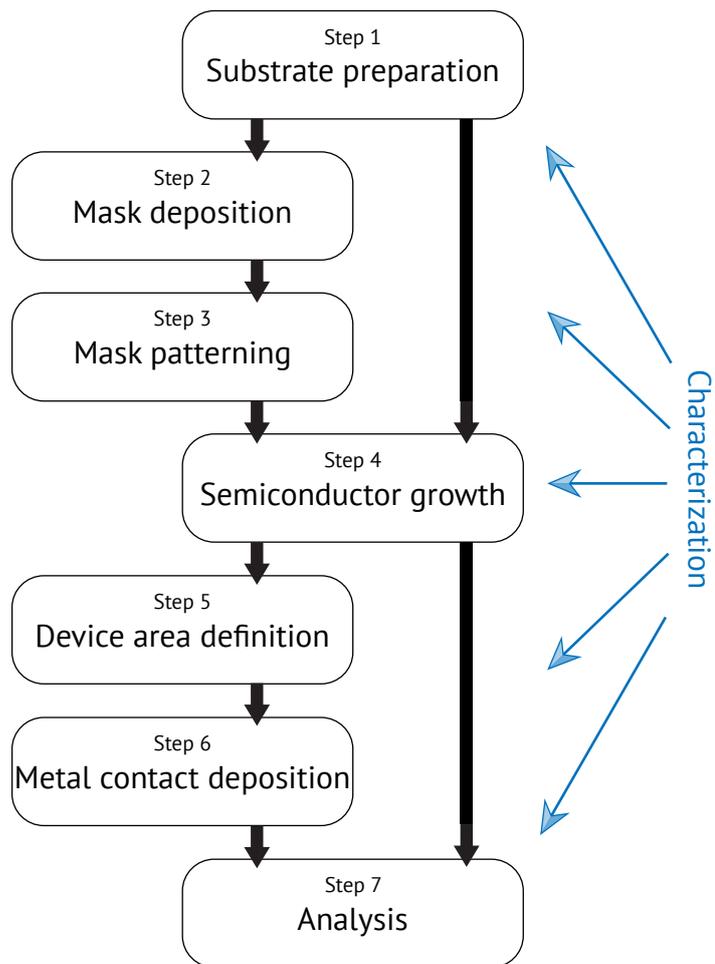


Figure 5.1: Schematic of processing steps.

For transferred graphene, the target substrate is first thoroughly cleaned in acetone, with or without sonication, and rinsed in IPA before drying with nitrogen gas. The transfer process for CVD graphene is described in section 2.3.1. If using exfoliated graphite, a small piece of kish graphite is exfoliated by repeated detachment with blue tape, before transferring to the target substrate with manual pressure. If there are no other requirements, the preferred target substrate is 300 nm thermally grown  $\text{SiO}_2$  on Si, as it has optical contrast even for single-layer graphene.

### 5.1.2 Mask deposition

For selective area growth (SAG) of nanowires, an oxide hard mask is deposited and patterned to achieve growth only on desired areas. An optimized oxide structure of  $\text{Al}_2\text{O}_3$  and  $\text{SiO}_2$  has previously been developed in our group, as this ensures the best adhesion between the oxide and graphene as well as good control over the etching profile. The  $\text{Al}_2\text{O}_3$  is deposited by Atomic Layer Deposition (ALD), a process developed and performed at Aalto University, and the  $\text{SiO}_2$  by Plasma-Enhanced Chemical Vapor Deposition (PECVD). An oxide mask of ALD and electron-beam evaporated  $\text{SiO}_2$  was also investigated, but found less successful in terms of adhesion and etching profile control.

### 5.1.3 Mask patterning

The patterning can either be done by photolithography or electron-beam lithography (EBL). Both methods require the use of a photo- or electronsensitive resist spin-coated on top of the sample. If larger areas are the target, photolithography either by a mask aligner (Karl Süss MA6), direct exposure by optical microscope or maskless aligner (Heidelberg MLA150) is used to pattern the resist. If smaller areas are the target, most typically small (50-150 nm diameter) holes for the growth of separated single nanowires, EBL is used. After the lithography step, the oxide mask is etched by buffered oxide etch, diluted to give the desired etch rate.

### 5.1.4 Semiconductor growth

The semiconductor structure is grown by MBE for III-V nanowires or by AIC for Si thin films, as described in sections 2.1 and 2.2.

### 5.1.5 Device area definition and metal contact deposition

The active area of the device, for example the aperture of an LED, is isolated by photolithography as described for mask patterning in section 5.1.3. To ensure electrical insulation, we have used the Shipley S1800 series photoresist to isolate the nanowire/thin film area, and then performed a subsequent baking of the resist at high T ( 180°C with ramping) to harden it into an isolating mask. Open areas must also be defined for the graphene bottom contact. Contact areas are defined in an additional photolithography step. Metal contacts are deposited either by sputtering or electron-beam evaporation of the metals suitable for the semiconductor material of the device. We have typically used Al for Si devices, Ni/Au for p-doped GaN and Au for the graphene electrode.

### 5.1.6 Analysis

The final devices can be measured and analysed by electrical and optical methods, described in sections 3.4 and 3.6.

## 5.2 Mask patterning for GaAs and GaN nanowire growth on graphitic substrates

Self-catalyzed GaAs semiconductor nanowires have proven difficult to grow on graphene and graphitic substrates, due to the lack of dangling bonds on the surface as described in Section 2.3.2. If the growth recipe used for NW growth on other substrates is used with graphene, typically a very low nucleation probability of nanowires is the result. To enhance the nucleation density of nanowires, we have employed three main approaches:

- Two-step temperature growth protocol, as described by Munshi et al [29].
- Activation of the graphene surface by oxygen plasma ashing and hydrogenation through hydrogen annealing.
- The growth of a short GaAsSb NW stem.

These approaches improved the yield of GaAs nanowires on exfoliated kish graphite flakes on a SiO<sub>2</sub> substrate, as seen in Figure 5.2, where (a) shows NW growth without any of the approaches listed above, and (b) is with these approaches. However, to be able to make a device of the graphite-NW heterostructure, we worked on optimising the NW growth on kish graphite with an oxide mask.

## 5.2. Mask patterning for GaAs and GaN nanowire growth on graphitic substrates

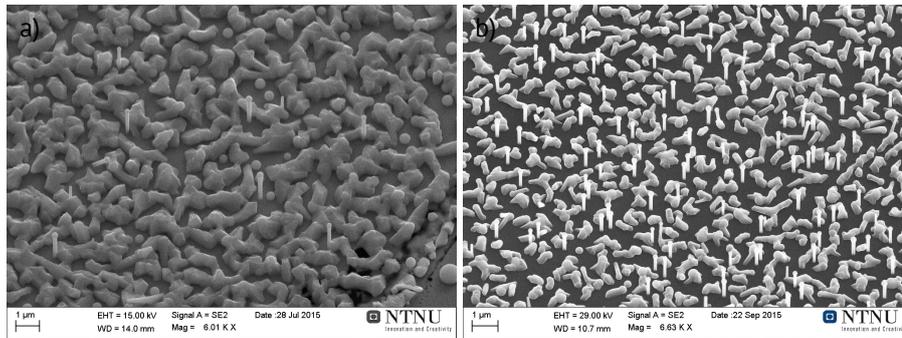


Figure 5.2: SEM images of (a) GaAs NWs grown on kish graphite, and (b) GaAs NWs with a short GaAsSb NW stem grown on surface treated kish graphite.

Different oxides were tested for mask patterning and nanowire growth on kish graphite. It was found that alumina ( $\text{Al}_2\text{O}_3$ ) had a better adhesion to the graphene surface than silica ( $\text{SiO}_2$ ), and thus a smaller chance of delaminating due to the elevated temperatures used during nanowire growth. However, GaAs nanowires have a higher nucleation probability on  $\text{Al}_2\text{O}_3$  than  $\text{SiO}_2$ , and therefore a two-layer mask was used, consisting of 30 nm  $\text{Al}_2\text{O}_3$  deposited by ALD at Aalto University, and 30 nm  $\text{SiO}_2$  deposited by PECVD at NTNU. The oxide mask was patterned by e-beam lithography (EBL), to produce holes with a diameter of 50-100 nm. A technique called one-shot exposure was utilised, which means that instead of scanning a small electron beam across the hole area, the beam is dwelling in the center of the hole for a prolonged period of time. This means that the dwell time of the beam decides the size of the hole pattern. This technique saves time and allows for bigger areas of the sample to be patterned. The best results achieved for GaAs nanowires with a GaAsSb NW stem on  $\text{Al}_2\text{O}_3/\text{SiO}_2$  oxide mask on kish graphite substrates are shown in Figure 5.3.

A high selectivity between the graphene surface and oxide mask was achieved, but at the cost of the yield of nanowires, meaning the number of nanowires occupying a hole divided by the total number of holes. Another challenge was a varying thickness of the oxide mask, as the kish graphite flakes have a varying number of graphene layers, leading to a thicker mask on some flakes and thinner on others. This in turn affects the size of the hole, as a thicker mask will have a smaller hole as compared with a thinner region, since this depends on the etching time of the mask. The size of the hole dictates whether zero, one, two or several nanowires will

## CHAPTER 5. GRAPHENE-NANOWIRE DEVICE PROCESSING AND PRELIMINARY RESULTS

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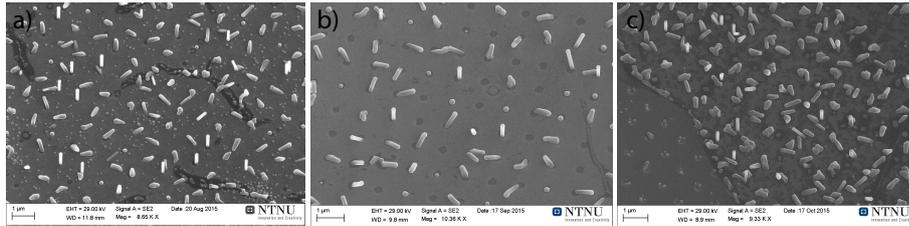


Figure 5.3: SEM images of GaAs nanowires grown with a GaAsSb stem by selective area growth on kish graphite flakes covered with an  $\text{Al}_2\text{O}_3/\text{SiO}_2$  oxide mask. The mask has been patterned with circular holes to allow for nanowire growth on the kish graphite surface. The three images are from three different growth runs with modified growth conditions.

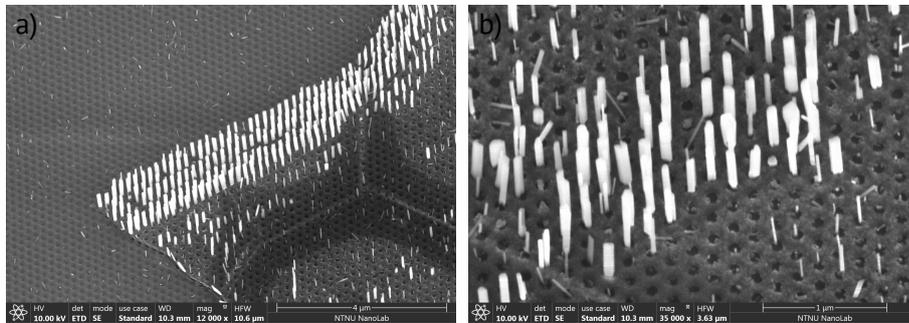


Figure 5.4: SEM images of GaN NW growth on kish graphite flakes covered by a patterned oxide mask. (a) shows an edge of a kish graphite flake and (b) the middle part of a kish graphite flake.

nucleate in the hole, as seen in Figure 5.3(c).

Preliminary tests on growth of GaN NWs on a patterned  $\text{Al}_2\text{O}_3/\text{SiO}_2$  oxide mask on kish graphite flakes showed that catalyst-free GaN NWs nucleate more readily on the graphene surface without any surface treatment, but only on some regions of the flakes. In addition to not having to form a liquid Ga droplet, we believe that GaN nucleates more easily than GaAs because of the nitrogen plasma damaging the graphene lattice and thus activating potential nucleation sites. SEM images of GaN NW growth on patterned kish graphite are shown in Figure 5.4, showing close to 100% yield in some regions of the graphite flake while other regions do not have any NW growth.

### 5.3 Graphene-AIC Si photodetector

After discovering the enhancement of Si crystallisation by AIC on graphene compared to amorphous substrates, we attempted to fabricate a photodetector based on the graphene and p-doped Si junction. It would be interesting to compare the junction properties with more conventional photodetectors using transferred graphene on Si, as there is a possibility that Fermi level pinning could be avoided by using a clean interface. Several fabrication schemes were tested, and two of the photodetector designs are shown in Figure 5.5, where a small-contact scheme is shown in panel (a), and a scheme with a thin layer of amorphous Si on top of crystallised Si is shown in panel (b).

Al was chosen as the contact metal to p-doped Si to ensure an ohmic contact. Electrical measurements were carried out on a sample fabricated as Figure 5.5(a), with 100 nm thick Al and Si layers, and a 5  $\mu\text{m}$  large contact between p-Si and Al. A typical IV curve is plotted in Figure 5.6, showing a higher current under reverse bias, which is to be expected of this type of device [104, 105]. However, when repeating the IV sweep, the device would break down and adopt a short-circuit behaviour. This inhibited comparison between IV-curves taken under light and dark conditions, and no photocurrent could be measured.

In an effort to make the device more robust, a 100 nm thick amorphous Si layer was deposited by PECVD at 180°C on top of crystallised Si, as shown in Figure 5.5(b). However, the amorphous Si layer was found to introduce stress in the system, causing the complete structure to release from the substrate between graphene and  $\text{SiO}_2$ . As discussed in our paper in chapter I, the adhesive forces are stronger between the crystallised Si and graphene than between graphene and the substrate [161], causing delamination and an intact graphene sheet. A method that could avoid this would be to pattern the amorphous Si into smaller regions and

CHAPTER 5. GRAPHENE-NANOWIRE DEVICE PROCESSING AND PRELIMINARY RESULTS

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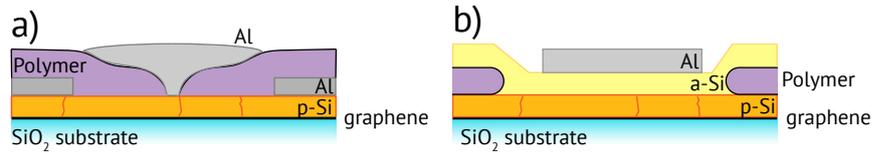


Figure 5.5: Fabrication of graphene-Si photodetector, with (a) a small Al contact to crystallised Si, and (b) a thin layer of amorphous Si deposited on top of crystallised Si.

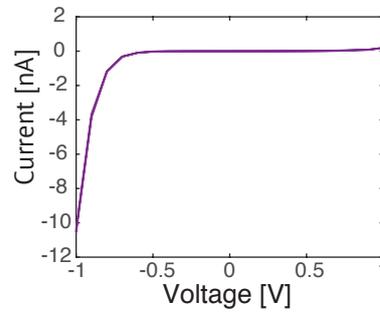


Figure 5.6: IV curve of graphene/p-Si photodetector fabricated by AIC.

thus release some of the stress laterally, but such a solution is challenging as both an elevated temperature at low pressure and plasma is used during amorphous Si deposition.

## Part III

# Papers and concluding remarks



## Chapter 6

# Summary of papers

In this thesis, optoelectronic devices comprised of heterostructures of semiconductors and graphene have been investigated, with a focus on method development and material characterisation. The results of this work is presented in three papers and one manuscript, in addition a collection of unpublished results are included in Part II. The fabrication and characterization of a gr-Si heterostructure and photodetector based on metal-induced crystallisation of Si is described in Paper I and section 5.3 of Chapter 5. The underlying research on achieving MBE-compatible graphene growth substrates is described in Chapter 4, while efforts to improve the nucleation density of GaAs, GaAsSb and GaN nanowires are presented in Paper 2 and Chapter 5. Finally, the growth, fabrication and characterisation of UV-LEDs based on GaN/AlGaN nanowires grown on single- and double-layer graphene is presented in Manuscript III and Paper IV.

### **Paper I**

In "Fabrication of Si(111) crystalline thin film on graphene by aluminum-induced crystallisation" a graphene-Si heterostructure is fabricated through the aluminum-induced crystallisation of amorphous Si directly on graphene. The heterostructure is characterized by XRD,  $\mu$ -Raman Spectroscopy and AFM, and an increase of crystallisation is found in the Si crystallised on graphene compared with the amorphous reference sample. An epitaxial model is proposed based on these findings.

In this paper, the study was designed and planned by I. Høiaas and D.-C. Kim. I. Høiaas performed all experimental work and characterization, while D.-C. Kim performed the theoretical calculations. H. Weman supervised the work. I. Høiaas drafted the manuscript, and all authors contributed to the discussions of its content.

### **Paper II**

In "Growth optimization for self-catalyzed GaAs nanowires on metal-induced crystallized amorphous substrate" the inclusion of a thin polycrystalline Si(111) film on an amorphous substrate is used to increase the nucleation density of GaAs and GaAsSb nanowires. The nanowire density is found to depend on the Si and native oxide thickness. Incorporating Sb during nanowire growth is also found to improve the nanowire density. Optical measurements verify the high quality of the nanowires, which is comparable to nanowires grown on bulk monocrystalline Si(111).

The idea and study was designed by D. Ren and I. Høiaas, supervised by D.-C. Kim, H. Weman and B.- O. Fimland. I. Høiaas prepared the metal-induced crystallization of Si substrates, D. Ren performed the substrate annealing and nanowire MBE growth in discussion with I. Høiaas, M. Munshi and D. Dheeraj. J. Reinertsen performed the photoluminescence measurements and data analysis. D. Ren drafted the manuscript together with I. Høiaas. All authors contributed to the discussion of results and preparations of the manuscript.

### **Manuscript III**

In "Graphene as Transparent Conducting Substrate for The Fabrication of Flip-chip Ultraviolet Light-Emitting Diode Based on GaN/AlGaN Nanocolumns" a two-stage nucleation scheme is used for the successful growth of vertical GaN/AlGaN nanocolumns on single-layer graphene on fused silica. The materials are investigated by SEM, XRD, TEM and  $\mu$ -Raman spectroscopy. The structure is processed into an LED device, showing weak EL emission in the UV-A spectrum at 352 nm, indicating that the very thin GaN layer observed in the active region is the origin of the emission.

In this manuscript, A. Liudi Mulyo planned the experiments under the supervision of B.O. Fimland, H.Weman and K. Kishino. A. Liudi Mulyo performed the nanowire growth by MBE and SEM imaging. I.M. Høiaas and H. Hem Toftevaag performed Raman spectroscopy and mapping and analysed the data, in collaboration with A. Liudi Mulyo. I.M. Høiaas performed preliminary device fabrication and I-V measurements, while A. Mukherjee fabricated the final LED device together with H. Toftevaag and did I-V/EL measurements. T.A. Nilsen did XRD characterization, simulation and analysis. P.E. Vullum performed TEM/STEM/EDX/EELS imaging and spectroscopy. L. Ahtapodov performed the photoluminescence measurements and analysis. A. Liudi Mulyo drafted the manuscript. All authors contributed to the discussion of results and preparations of the manuscript.

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#### **Paper IV**

In "GaN/AlGaN Nanocolumn Ultraviolet Light-Emitting Diode Using Double-Layer Graphene as Substrate and Transparent Electrode" a functional nanowire LED is demonstrated using double-layer graphene as growth substrate and transparent electrode. The material quality of both graphene and nanowires is assessed using  $\mu$ -Raman Spectroscopy, PL and TEM, showing plasma-induced damage in the graphene and a high crystal quality for the nanowires. Luminescence under continuous electrical bias is measured, confirming light emission in the UV-A spectrum, at 365 nm. TEM and PL results suggest that emission is taking place in the thin p-GaN contact layer.

In this paper, I. Høiaas planned the study with A. Liudi Mulyo under the supervision of H.Weman, B.-O. Fimland and K. Kishino. I. Høiaas performed the experimental work related to device fabrication and characterization, while A. Liudi Mulyo performed the nanowire growth by MBE and SEM imaging. P.E. Vullum did the TEM/STEM/EDX/EELS imaging in discussion with I. Høiaas and A. Liudi Mulyo. L. Ahtapodov performed the photoluminescence measurements. I. Høiaas drafted the manuscript together with A. Liudi Mulyo. All authors contributed to the discussion of results and preparations of the manuscript.

CHAPTER 6. SUMMARY OF PAPERS

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## Chapter 7

# Outlook

The goal of much of the work comprised in this thesis has been to develop optoelectronic devices based on hybrid structures of nanomaterials, more specifically graphene and nanostructured semiconductors. It quickly became apparent that both the graphene substrate and semiconductor growth had to be optimised in order for graphene-nanowires and graphene-thin film optoelectronic devices to be achieved. The challenges we met and the efforts to solve them have been documented in three papers, one manuscript and two chapters with unpublished results. They create a basis for further work, and some recommendations for future experiments follow here.

More detailed characterisation of the interface between graphene and aluminum induced crystallised Si would be interesting, as the atomic bonds between the two materials could behave differently than what is observed for graphene transferred onto Si. Furthermore, theoretical calculations and atomistic simulations could be necessary to determine whether this is closer to a van der Waals-bond or something in between van der Waals and covalent bonds.

Comparing the behaviour of a graphene/AIC-Si photodetector with a conventional transferred graphene/Si junction photodetector would yield insight on the effect of Fermi-level pinning on said photodetector. As graphene is known to offer high-speed capabilities, a more flexible junction design could help improve the photodetector performance and also lead to new applications.

Better understanding of van der Waals and quasi-van der Waals epitaxy growth is needed to increase the nucleation yield of nanowires on graphene. In our work, we have shown that the fabrication of nucleation sites through plasma treatment of the graphene is a useful tool to achieve increased density, but inherent to this method

## CHAPTER 7. OUTLOOK

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is the destruction of graphene. If one wants to utilise the functional properties of graphene also after growth, a nondestructive strategy should be found, understood and employed in the future.

Although we have demonstrated a proof-of-concept graphene-NW UV LED, this is only the starting point. The different segments of the structure must be optimised step-by-step to reach efficiencies that can compete with commercial components. Also, the carrier dynamics and interface properties must be investigated closer, as increased understanding can lead to an improved design. Especially, the interface between the graphene and nucleation layer is interesting, as the potential barrier is determined by several factors such as graphene quality, doping of graphene and growth parameters.

The concept of remote epitaxy through two-dimensional materials has been explored for thin film growth [49,50], but it could be just as interesting for nanowires and other nanostructures with the first couple of articles published recently on this topic [162,163]. Being able to delaminate the whole structure gives full flexibility in device and electrode design, and could be the ultimate approach for the recycling of expensive substrates.

To conclude, there are several things needed to go from proof-of-concept structures and devices to a commercial device. Firstly, the commercial supply of graphene is steadily expanding, so contamination-free graphene should be available in a not too distant future. Secondly, the integration of graphene-based structures into production-level processes must be investigated and achieved. Issues with premature delamination of the devices due to the weak bonds between the substrate/graphene and graphene/semiconductor interfaces must be solved and the availability of high-quality and clean graphene must be improved. Thirdly, the nanostructured device must be optimised for packaging and serial production to be sold as a product. The gap between research and industrialisation is a challenge inherent to the nanotechnology community, which needs to be solved to ensure funding for the continuation of our research. There is great value residing in the expansion of knowledge and understanding of materials and phenomena, but to actually incorporate the developed knowledge in useful products would communicate the value to a broader audience and help develop our field further.

## Chapter 8

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## Chapter 9

# Scientific Publications and Manuscripts

CHAPTER 9. SCIENTIFIC PUBLICATIONS AND MANUSCRIPTS

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Paper I

Fabrication of Si(111)  
crystalline thin film on  
graphene by  
aluminum-induced  
crystallisation

I. M. Højaas, D.-C. Kim and H. Weman  
Published in Applied Physics Letters **108**, 161906 (2016)

PAPER I. FABRICATION OF SI(111) CRYSTALLINE THIN FILM ON  
GRAPHENE BY ALUMINUM-INDUCED CRYSTALLISATION

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## Fabrication of Si(111) crystalline thin film on graphene by aluminum-induced crystallization

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We report the fabrication of a Si(111) crystalline thin film on graphene by the aluminum-induced crystallization (AIC) process. The AIC process of Si(111) on graphene is shown to be enhanced compared to that on an amorphous SiO<sub>2</sub> substrate, resulting in a more homogeneous Si(111) thin film structure as revealed by X-ray diffraction and atomic force microscopy measurements. Raman measurements confirm that the graphene is intact throughout the process, retaining its characteristic phonon spectrum without any appearance of the D peak. A red-shift of Raman peaks, which is more pronounced for the 2D peak, is observed in graphene after the crystallization process. It is found to correlate with the red-shift of the Si Raman peak, suggesting an epitaxial relationship between graphene and the adsorbed AIC Si(111) film with both the graphene and Si under tensile strain. © 2016 Author(s). All article content, except where otherwise noted, is licensed under a Creative Commons Attribution (CC BY) license (<http://creativecommons.org/licenses/by/4.0/>). [<http://dx.doi.org/10.1063/1.4947101>]

One of the most interesting applications of graphene for future electronic and photonic devices is to integrate it with currently widely used Si and III-V semiconductors in such a way that the characteristic properties of both graphene and semiconductors are well retained and utilized for their high performance. Several pioneering examples can be mentioned, for example, graphene-Si junctions for triode barristors and solar cells,<sup>1,2</sup> and the epitaxial integration of III-V semiconductor nanowires with graphene as a substrate.<sup>3,4</sup>

On combining graphene with Si, most studies are focused on devices where commercially available crystalline Si substrates are used with transferred graphene on top. The opposite case, using graphene as a substrate and depositing Si on top of graphene, is rarely reported.<sup>5–7</sup> In fact, graphene is considered to be chemically inert due to its lack of dangling bonds, resulting in a low adsorption probability of foreign atoms and molecules. It has been found that graphene retains its high quality by direct deposition of Si<sup>7</sup> and its sheet resistance when covered with a thin Si capping layer after post-crystallization,<sup>5</sup> due to the reduced carrier mobility being compensated by an increase in carrier concentration. If the crystal quality of the Si layer can be improved, the conductance of the Si/graphene film may be further increased.

In this letter, we present a method that allows for a crystalline (111)-oriented Si thin film on graphene as a substrate by a crystallization process of Si termed metal-induced crystallization (MIC). Using Al as the metal (AIC), this process is known to give a high quality Si film with a large grain size.<sup>8</sup> By combining this with transparent and flexible graphene, it can be highly beneficial for low cost production of Si photovoltaic cells<sup>9,10</sup> and photodetectors<sup>11</sup> as well as for the epitaxial growth of III-V nanowire devices on graphene.<sup>12</sup> The latter

requires an (111)-orientation of the Si film, and the growth of vertical GaAs nanowires on a 10 nm thick crystallized Si(111) layer on SiO<sub>2</sub> has been demonstrated.<sup>13,14</sup>

MIC is a diffusion-driven process, where thin layers of metal and Si are deposited on top of each other before undergoing an annealing step at 150–500 °C.<sup>15,16</sup> Al and Ni form eutectics with Si and can be used as the metal catalyst.<sup>17,18</sup> The Si diffuses through the metal layer and rearranges as a crystalline film at the metal/substrate interface, making the Si and metal layers exchange positions. The coverage and orientation of the Si are determined by the thickness of the metal and Si layers as well as the annealing process. With Al as the metal layer, the process has been investigated to obtain crystallized Si films on arbitrary substrates<sup>19</sup> with either (001)- or (111)-orientation. Kurosawa *et al.* have summarized which parameters favor which orientation, concluding that longer Al oxidation time and thinner (<100 nm) Al layers result in (111)-oriented Si.<sup>20</sup>

The samples used in this study were of two types processed in parallel: commercial chemical vapor deposition (CVD) grown monolayer graphene transferred onto Si(001) substrates from Graphenea S.A. and thermal SiO<sub>2</sub> (300 nm)/Si(001) substrates, respectively. The purpose of the latter substrate is to check the overall MIC process with optimized process parameters, in comparison with the substrate with graphene. On these samples, we deposited 50 nm Al by e-beam evaporation at a rate of 1 Å/s and a pressure of ~10<sup>-8</sup> Torr. The samples were oxidized for 24 h in an ISO5 cleanroom atmosphere before depositing 50 nm amorphous Si (a-Si) by e-beam evaporation at a rate of 1 Å/s and a pressure of ~10<sup>-8</sup> Torr. All depositions were done at room temperature. The samples were annealed for 15 h at 500 °C in a nitrogen gas. This temperature was chosen to decrease the annealing time as much as possible while still staying well below the Al-Si eutectic temperature of 577 °C. After the layer exchange by annealing, the top layer of Al was removed by etching in a

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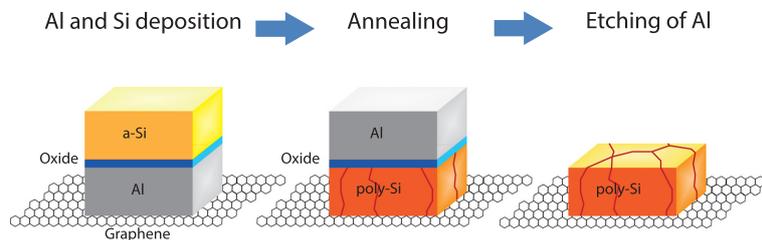


FIG. 1. Schematic showing the process steps of the Al-induced crystallization (AIC) process on graphene. An Al layer is first deposited and subsequently oxidized at room temperature for 24 h. Amorphous silicon (a-Si) is deposited on top of the stack, and the whole structure is annealed in a  $N_2$  atmosphere. The layers exchange positions as the Si atoms diffuse towards the substrate and rearrange as a polycrystalline Si film (poly-Si), and the top layer of Al can be etched away.

phosphoric acid mixture.<sup>21</sup> The overall process is shown in Figure 1. X-ray diffraction (XRD) measurements were done with a D8 HRXRD system, and the data shown here have been normalized to the Si(004) substrate peak intensity. Atomic force microscopy (AFM) images were acquired with a Veeco Multimode V system. The Raman spectra were collected by a Renishaw micro-Raman backscattering spectroscopy system using a 532 nm focused laser beam and 50 $\times$  objective lens. Raman maps were created by collecting spectra with a step size of 1  $\mu\text{m}$  from a 20  $\mu\text{m}$   $\times$  20  $\mu\text{m}$  area. Average peak positions and peak widths were calculated by averaging the values of 25 random spectra from the map.

It is worth to note that there is one major difference in our aluminum-induced crystallization (AIC) process compared to the conventional process. Most groups investigating the AIC process use sputtering for the Al layer deposition, which gives a preferable (111)-orientation of the Al grains.<sup>22</sup> However, the sputtering process involving a plasma with high-energy particles may damage the graphene layer, whereas e-beam evaporation provides a more gentle approach. In our experience, it is imperative to have a high vacuum during the e-beam Al deposition step. If the vacuum is too low ( $>10^{-7}$  Torr), the layer exchange between Si and Al is incomplete, resulting in poor Si(111) crystallization. We suspect this might be because the microstructure of Al is affected by the deposition pressure. Further investigations are needed to check this hypothesis.

The XRD data shown in Figure 2 were taken after e-beam deposition of Al and amorphous Si (top graph),

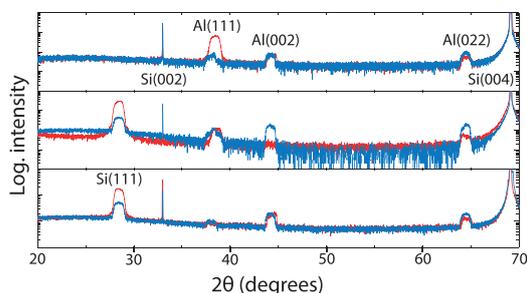


FIG. 2. XRD  $2\theta/\omega$  scans after deposition of Al and amorphous Si (top), after the Al-induced crystallization of Si (middle), and after the etching of Al (bottom). The red scans are from the graphene/Si(100) sample and the blue scans are from the  $\text{SiO}_2/\text{Si}(100)$  sample. The data have been normalized to the intensity of the substrate Si(004) peak. The Si(002) peak is also from the Si substrate.

after annealing (middle graph) and after etching of the top Al layer (bottom graph) on the graphene/Si(100) and  $\text{SiO}_2(300\text{nm})/\text{Si}(100)$  substrates. From Figure 2, it is observed that the as-deposited Al film is different for the two substrates. While all the Al(111)-, Al(002)-, and Al(022)-peaks show approximately the same intensity for the  $\text{SiO}_2$  sample, the Al(111) peak is about ten times as large as the other crystal orientations for the graphene sample. Furthermore, the Si(111) peak that appears after annealing is more than ten times larger than the Al(111) peak for the graphene sample, while it is only twice as large compared to the largest Al-peak for the  $\text{SiO}_2$ -sample. The data imply that the graphene directly affects the film formation of Al and consequently the AIC process. It should be mentioned here that the effect of the Si(100) substrate below graphene on the observed enhanced AIC process should be negligible. The Si(100) substrate was exposed to air before the graphene transfer so it is covered with a native amorphous oxide, similar to the  $\text{SiO}_2/\text{Si}(001)$  substrate. The prominent Al(111) peak may be explained in terms of an epitaxial relationship with graphene. The triangular lattice of the Al(111) plane matches well with the hexagonal lattice structure of graphene with a lattice mismatch of 0.8%, while the other (002) and (022) Al planes have a lattice mismatch of more than 10%.<sup>23</sup> The Al(002)- and Al(022) reflections can still be observed after etching, and we attribute this to local Al residues in some areas of the sample. These local residues could potentially be detrimental to device performance, and further improvement of the Al removal might be necessary.

Optical microscopy and AFM images of the two samples processed in parallel are shown in Figure 3. The appearance of the Si films differs both due to the color of the underlying substrate and their morphology after the AIC process. Dendrite structures are clearly visible in the images of the  $\text{SiO}_2$  sample, which are not observed on the graphene sample. The height profiles in the AFM images (Figs. 3(e) and 3(f)) show that there are two distinct layers present on the  $\text{SiO}_2$  sample which are not observed on the graphene sample. The dendrites seen in the optical images are islands with a height of about 30 nm on top of a 50 nm layer, which corresponds to the original Al thickness. The islands observed in Figures 3(a) and 3(c) are similar to what is observed for the crystallization process of Ge,<sup>24</sup> showing two distinct layers corresponding to the original thickness of Al and a-Si of 50 nm. Figure 3 indicates that the Si(111) film obtained by AIC on graphene is smoother than that obtained

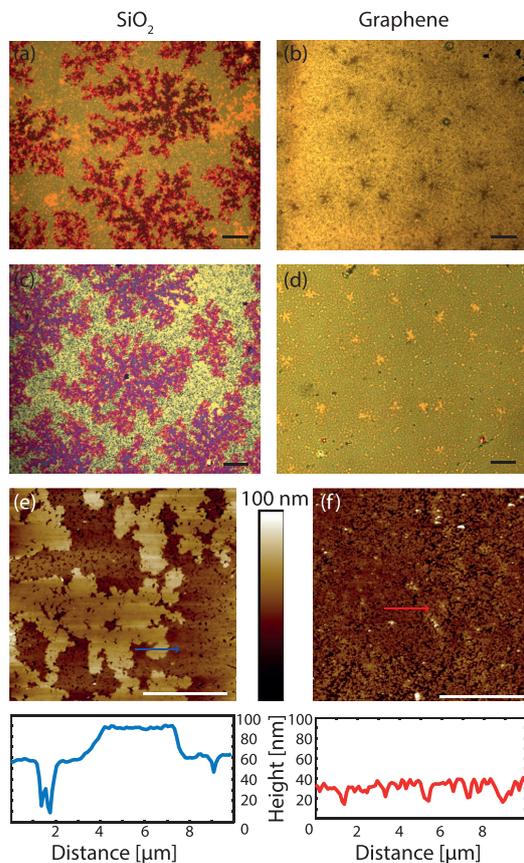


FIG. 3. Optical images show the SiO<sub>2</sub> sample (a) after the Al-induced crystallization process and (c) after subsequent Al etching, and the graphene sample (b) after the Al-induced crystallization and (d) after subsequent Al etching. AFM images of (e) the SiO<sub>2</sub> sample and (f) the graphene sample. AFM line scans from (e) and (f) (denoted by blue and red arrows, respectively) are shown in the bottom panels. All scale bars are 20 μm.

by AIC on SiO<sub>2</sub> with more homogeneity in thickness. Some local Al residues can be seen as bright spots in Figure 3(d).

It is already known that the substrate can influence the crystallization of Si. Toko *et al.* concluded that the type of substrate was important for the resulting Si-orientation, but could not determine the exact origin except for excluding the roughness of the substrate for being the reason.<sup>19</sup> They suggested that the difference in interfacial energy between Si and the substrate is the determining factor, but not in what form. The two samples used in this report for the AIC process: a graphene/Si(001) substrate and a SiO<sub>2</sub>/Si(001) substrate, respectively, were processed in parallel, so the difference observed in the crystallized Si film should be a direct effect of the substrate properties.

The AIC processed Al/Si layer on top of graphene can be easily exfoliated from the Si(100) substrates by using scotch tape as shown in Figure 4(a). This indicates that the interaction between the AIC processed Si layer and graphene gives stronger adhesion than the usual van der Waals interaction between graphene and the bottom Si(001) substrate, and

that the AIC process occurs on the graphene surface without any chemical interaction with the Si(100) substrate.

Figures 4(b)–4(e) show the Raman spectra and Raman mapping data of crystallized Si and graphene measured after exfoliation. The absence of the D peak at  $\sim 1320\text{ cm}^{-1}$  in the graphene spectra indicates that the AIC process does not damage the graphene, similar to other results from Si deposited on graphene devices.<sup>5,7</sup> Compared to the reference Si peak from a standard Si(100) substrate ( $520\text{ cm}^{-1}$ ) and graphene peaks from bare CVD graphene (G peak at  $1591\text{ cm}^{-1}$ , 2D peak at  $\sim 2684\text{ cm}^{-1}$ ) on Si substrates, the AIC processed Si and graphene show red-shifts of the Raman peaks. The Raman mapping reveals that the red-shifts of the Si and graphene Raman peaks are correlated; the regions experiencing the largest red-shift of the Si peak also experience the largest red-shift of the graphene peaks. The red-shift is more prominent for the 2D peak, which shifts up to  $\sim 24\text{ cm}^{-1}$ . This observation is opposite to previous results from e-beam crystallized Si on graphene, and Si-islands deposited on graphene where blue-shifts of both the G and 2D peaks were observed.<sup>5,6</sup>

A shift of the characteristic phonon modes of graphene indicates a change in doping and/or strain in the graphene layer. In a comprehensive study, Das *et al.* showed that field-effect doping of graphene leads to a blue-shift of the G peak and a red- or blue-shift of the 2D peak depending on the charge of the doping.<sup>25</sup> The simultaneous red-shift of the G and 2D peak indicates that tensile strain in graphene is the origin of the shift. The Al-induced crystallized Si has been known to be heavily p-doped by Al impurity atoms with values  $\sim 10^{18}$ – $10^{19}$  atoms/cm<sup>3</sup>.<sup>26–28</sup> This could give rise to p-doping in graphene. According to the correlation analysis of the G and 2D peak positions by Lee *et al.*, the effects of strain and doping can be separated. From the average values of the G and 2D peak positions in Table I of  $1584.5\text{ cm}^{-1}$  and  $2669.3\text{ cm}^{-1}$ , respectively, the graphene with the AIC processed Si(111) film has a tensile strain of  $\sim 0.25\%$  and a hole doping concentration of  $\sim 7 \times 10^{12}\text{ cm}^{-2}$ .<sup>29</sup>

The red-shift of the Si peak at  $520\text{ cm}^{-1}$  indicates that a tensile strain is present also in the crystallized Si(111) thin film. The correlation of the red-shift of the Si peak with that of the graphene peaks indicates some form of chemical bonding between the crystallized Si and graphene. We therefore next consider the possible adsorption sites of Si atoms in the (111) plane on graphene that would give rise to an epitaxial chemical binding. Theoretical calculations of the adsorption of a single Si adatom on three different graphene sites—H-sites: hollow sites above the centers of C hexagons, T-sites: sites on top of C atoms, and B-sites: bridge sites above the midpoints of C-C bonds—on graphene predict that the B-site is the most stable absorption site, followed by the T-site with a slight decrease of the adsorption energy of less than 0.1 eV. The H-site is the least favorable one with an adsorption energy difference of more than 0.4 eV.<sup>30,31</sup> However, for Si atoms in a (111) lattice plane which have one dangling bond, it is quite different. First-principles calculations show similar adsorption energy in all three site configurations.<sup>32</sup> Figure 5 shows possible arrangements of Si atoms in a (111)-plane above the hexagonal graphene lattice with the Si atoms at B-, T-, and H-sites. Figures 5(a) and 5(b) show the configuration when the center Si atom is adsorbed at the B- and T-site,

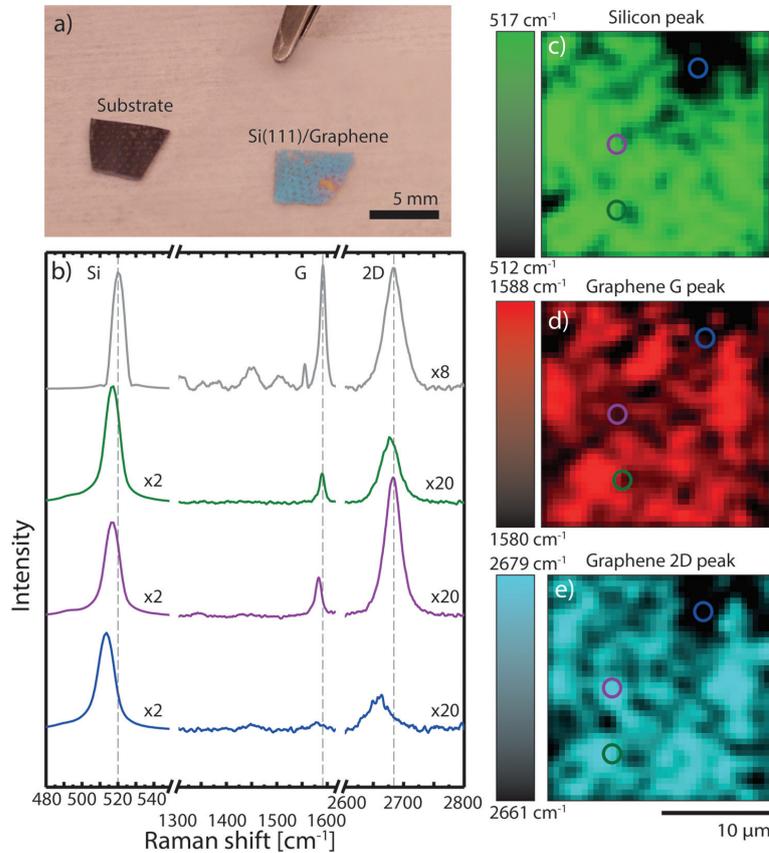


FIG. 4. (a) Photograph of the AIC processed Si(111)/graphene sample after exfoliation from the Si(001) substrate. (b) Raman spectra from the crystallized Si and graphene after the AIC process. Raman mapping images corresponding to (c) the position of the Si peak, (d) the graphene G peak, and (e) the graphene 2D peak. In (b), spectra from random locations denoted by circles in (c), (d), and (e) are shown together with a reference spectrum from pristine graphene on a Si(100) substrate (top). The peak positions of the reference spectrum are indicated with vertical dashed lines. The heights of the Si peaks and the graphene reference peaks have been normalized to fit the plot.

respectively, with a Si interatomic distance ( $a_{\text{Si-Si}}$ ) between the relaxed Si atoms (blue solid circles) of 3.840 Å. The green hexagon in Figure 5(a) represents a lattice-matched arrangement of atoms in a (111)-plane on graphene with an interatomic distance  $a = 3.694$  Å. The red hexagon in Figure 5(b) represents a lattice-matched arrangement of atoms in a (111)-plane on graphene with an interatomic distance  $a = 3.762$  Å. The same green and red hexagonal arrangements can also be obtained for the case when the center Si atom is adsorbed at the H-site (Fig. 5(c)). The lattice mismatch between (relaxed) Si(111) and graphene with the green and red hexagonal configurations is 3.95% and 2.07%, respectively. If conventional

TABLE I. Values for the mean frequency  $\bar{\nu}$  and full width at half maximum (FWHM) of Si and graphene main Raman peaks from the positions shown in the map in Figure 4 for graphene with crystallized Si(111) on top. Values from Si(001)/G are reference values obtained from CVD graphene transferred to a Si(001) substrate.

	$\bar{\nu}_{\text{Si}}$ ( $\text{cm}^{-1}$ )	$\text{FWHM}_{\text{Si}}$ ( $\text{cm}^{-1}$ )	$\bar{\nu}_{\text{G}}$ ( $\text{cm}^{-1}$ )	$\text{FWHM}_{\text{G}}$ ( $\text{cm}^{-1}$ )	$\bar{\nu}_{\text{2D}}$ ( $\text{cm}^{-1}$ )	$\text{FWHM}_{\text{2D}}$ ( $\text{cm}^{-1}$ )
Si(001)/G	520.3	7.4	1591.0	13.1	2683.6	36.2
Blue position	513.4	10.8	1579.8	27.5	2659.6	42.4
Purple position	516.7	9.7	1582.6	14.5	2682.3	31.6
Green position	516.9	9.6	1589.5	12.1	2677.7	36.9
Average	515.7	8.6	1584.5	14.4	2669.3	37.1

epitaxial growth of Si(111) on graphene is considered, graphene would be tensile strained while Si would be compressively strained as  $a$  is smaller than  $a_{\text{Si-Si}}$ . However, in the Raman data (Fig. 4) tensile strain in the AIC crystallized Si on graphene is observed. The MIC process itself is known to introduce stress in the Si film, and this stress can be either compressive or tensile depending on the process conditions.<sup>33,34</sup> It is worth to note here that we also observe a red-shift of the Si Raman peak of the AIC Si on SiO<sub>2</sub> in this study. Therefore, if one considers that the crystal structure of Si is (111)-oriented with tensile strain from the AIC process, it appears that graphene adapts to the tensile strained Si to meet the epitaxial relationship.

Theoretical calculations on the adsorption of single Si atoms or a (111) plane of Si atoms on graphene predict a strong chemisorption forming Si-C covalent bonds.<sup>30-32</sup> This will affect the electronic structure of graphene significantly, and even induce a large band gap in graphene.<sup>32</sup> In addition, there is disagreement to whether strain in graphene opens up a band-gap or not.<sup>35,36</sup> Since the Si/graphene interface in our samples is formed from the Si-Al interchange at an elevated temperature, Si(111) and graphene may form a clean junction, which is not possible if graphene is transferred on top of Si.

In summary, a heterostructure comprised of CVD graphene and crystallized Si(111) has been fabricated by an

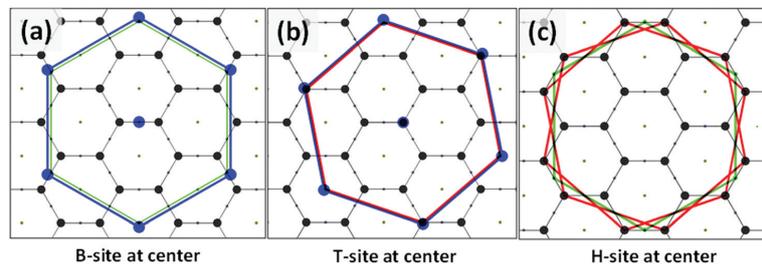


FIG. 5. Epitaxial arrangements of atoms in the (111) plane on top of the hexagonal graphene lattice. Large black solid circles denote the C atoms, which also correspond to the T-site configuration. B- and H-site configurations are denoted as small solid gray circles in the graphene lattice. In (a) and (b), the blue solid circles denote Si atoms with the blue hexagons indicating the (relaxed) Si atomic arrangement in the (111) plane with a Si-Si interatomic distance,  $a_{\text{Si-Si}}$ , of 3.840 Å. Three epitaxial configuration cases are shown: when the center Si atom is adsorbed at the (a) B-site, (b) T-site, and (c) H-site. The green hexagons in (a) and (c) represent lattice-matched arrangements of atoms in a Si(111) plane on graphene with an interatomic distance  $a = 3.694$  Å. The red hexagons in (b) and (c) represent lattice-matched arrangements of atoms in a Si(111) plane on graphene with  $a = 3.762$  Å. There are two possible lattice-matched arrangements for the red hexagonal configurations for the H-site at center case in (c).

AIC process. Improvement of crystallization and homogeneity of the Si(111) thin film has been observed with graphene compared to SiO<sub>2</sub> samples. Red-shifts in the Raman G and 2D peak positions indicate a tensile strain in the graphene. The red-shifts of the graphene Raman peaks correlate with a red-shift of the Si Raman peak, suggesting an epitaxial relationship with also the crystallized Si(111) under tensile strain. Theoretical modeling show that the adsorption of Si atoms in the (111) plane on graphene can be configured with a lattice mismatch of ~2%.

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PAPER I. FABRICATION OF SI(111) CRYSTALLINE THIN FILM ON  
GRAPHENE BY ALUMINUM-INDUCED CRYSTALLISATION

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## Paper II

# Growth optimization for self-catalyzed GaAs nanowires on metal-induced crystallized amorphous substrate

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PAPER II. GROWTH OPTMIZATION FOR SELF-CATALYZED GAAS  
NANOWIRES ON METAL-INDUCED CRYSTALLIZED AMORPHOUS  
SUBSTRATE

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## Growth optimization for self-catalyzed GaAs-based nanowires on metal-induced crystallized amorphous substrate

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The growth of monocrystalline semiconductor nanowires on arbitrary substrates via the metal-induced crystallization (MIC) process extends the possible combinations of substrates and epitaxial active materials. However, it is still difficult to accomplish high-density vertical nanowire growth on the MIC polycrystalline Si(111) substrate. Here, the authors report on the growth of self-catalyzed GaAs nanowires by molecular beam epitaxy on MIC polycrystalline Si(111) substrates with different surface oxide conditions. Forming the surface oxide by annealing the freshly hydrofluoric acid-etched MIC polycrystalline Si(111) substrate in an ambient atmosphere is found to be a key step to grow high-density GaAs nanowires. Moreover, the addition of Sb during nanowire growth improves the density of vertical nanowires. Photoluminescence measurements reveal a high optical quality of the GaAs nanowires, indicating that the nanowires grown on MIC polycrystalline Si(111) substrate may be used as building blocks for semiconductor nanowire optoelectronic devices on arbitrary substrates. © 2016 American Vacuum Society.

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### I. INTRODUCTION

One-dimensional nanowire structures attract great attention for heteroepitaxial growth, since elastic relaxation at the lateral free surfaces can accommodate strain due to lattice or thermal expansion mismatch between the substrate and epitaxial materials with nanoscale interfaces.<sup>1,2</sup> Therefore, materials with large lattice mismatch to the substrate can be epitaxially grown in the form of nanowires.<sup>3,4</sup> GaAs-based nanowires have been extensively studied recently due to their high carrier mobility, direct bandgap, and high optical quality, which in combination make them suitable for nano-optoelectronic devices, such as solar cells, photodetectors, and light-emitting diodes.<sup>5–9</sup> Tremendous efforts have been made lately to grow semiconductor nanowires, especially GaAs-based nanowires, on graphene or other two-dimensional (2D) materials.<sup>10–14</sup> However, the density of vertical nanowires on 2D materials is low compared to nanowire growth on, e.g., a Si substrate. Moreover, due to the lack of an epitaxial relation, it is very difficult to grow vertical nanowires on amorphous substrates, for example, indium tin oxide, which is used as transparent electrodes for optoelectronic devices.<sup>15,16</sup>

Recently, metal-induced crystallization (MIC) has been reported to be a promising strategy for forming polycrystalline Si on amorphous surfaces for the growth of vertical GaAs nanowires.<sup>17,18</sup> This strategy opens up new opportunities for nanowire growth on all types of substrates that can

be used for advanced optoelectronic applications. However, the density of vertical nanowires grown on MIC polycrystalline Si(111) is still low compared to the growth on, e.g., a monocrystalline Si(111) substrate, and thus requires further studies in detail.

In this work, we report on the growth optimization of self-catalyzed GaAs nanowires on MIC polycrystalline Si substrates. For this, a Si(111) surface orientation was first achieved using the MIC process on SiO<sub>2</sub> substrates. Then, GaAs nanowires were grown with different oxidation conditions on the MIC polycrystalline Si substrates. The formation of a thin oxide layer on top of the MIC polycrystalline Si substrate by thermal annealing was found to be a crucial step to improve the density of nanowires. Also, the vertical nanowire density was further improved by the addition of Sb during nanowire growth. In addition, we grew a radial AlGaAs shell around the GaAs nanowire core to passivate surface defect states. By performing micro-photoluminescence ( $\mu$ -PL) measurements on single GaAs/AlGaAs core-shell nanowires grown on MIC polycrystalline Si substrates, we observed that the nanowires exhibit a high optical response and is suitable for further development of high-density nanowire optoelectronic applications on arbitrary substrates.

### II. EXPERIMENT

The main steps involved in the MIC sample preparation are schematically shown in Fig. 1. The substrates used in this study were Si(001) wafers covered with 300 nm thick

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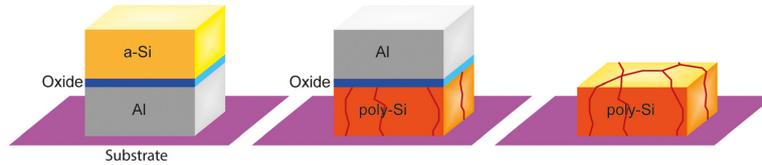


FIG. 1. (Color online) Schematic of MIC sample preparation. The thin films of Al and Si are deposited on the amorphous substrate by e-beam evaporation. The thin film stack is then annealed, making the thin film layers exchange position. After the annealing process, the top layer of Al, as well as the oxide, is removed by wet etching.

SiO<sub>2</sub>. The substrates were first cleaned with acetone and isopropanol before any depositions were done. Al was deposited at a rate of 1 Å/s by e-beam evaporation under a pressure of  $\sim 10^{-7}$  Torr. The substrates were subsequently oxidized for 24 h in an ambient atmosphere. Si was then deposited at a rate of 1 Å/s by e-beam evaporation at a pressure of  $\sim 10^{-7}$  Torr. Samples A–C had 10 nm Al and 10 nm Si while samples D–H had 50 nm Al and 30 nm Si. The Al/AlO<sub>x</sub>/Si thin film stack was then annealed in a furnace for 15 h at 500 °C in a flowing N<sub>2</sub> atmosphere. During the annealing process, the Al is transported to the surface by the layer-exchange diffusion process.<sup>19</sup> The Al was subsequently etched away during 45 min in a 25% HCl solution. The crystallinity of the MIC polycrystalline Si(111) substrate was characterized by high-resolution x-ray diffraction (XRD)  $2\theta/\omega$  scans, using a Bruker AXS D8 Discover x-ray diffractometer with half circle geometry, before and after the annealing process.

Eight MIC polycrystalline Si samples (samples A–H) were immersed in 5% hydrofluoric acid (HF) for 2 s to remove the SiO<sub>x</sub> on top of the MIC polycrystalline Si. After the HF treatment, samples A and D were kept in isopropanol and then directly loaded into the molecular beam epitaxy (MBE) system for nanowire growth. Samples B and E were kept in a flow bench for 8 days and samples C and F–H were annealed at 250 °C on a hotplate for 20 min in ambient atmosphere (room temperature  $\sim 20$  °C with humidity  $\sim 30\%$ ). The samples were In-bonded to a 2-in. Si(001) wafer before loading into the MBE system. A summary of the surface condition for each sample before loading into the MBE system is shown in Table I.

The nanowires were grown by a solid-source Varian Gen II Modular MBE system with standard effusion (Ga, Al) and valved cracker (As, Sb) cells. The major As and Sb species used in these experiments were As<sub>2</sub> and Sb<sub>2</sub>. For the axial and radial growth of the GaAs(Sb) nanowires, the temperatures of the Ga and Al sources were preset to achieve a nominal planar growth rate of 0.7 and 0.1 ML/s, respectively, on a GaAs(001) substrate (as measured by reflection high-energy

electron diffraction). The beam equivalent pressure for the As flux was  $3 \times 10^{-6}$  Torr. For sample H, where Sb was added to improve the vertical nanowire density, the Sb and As fluxes were  $4 \times 10^{-7}$  and  $2.5 \times 10^{-6}$  Torr, respectively. The substrate temperature was measured with a pyrometer (emissivity 0.62) and adjusted to 625 °C [a typical growth temperature for GaAs nanowires on monocrystalline Si(111)] for the nanowire growth on samples A–F and H. For sample G, the substrate temperature was adjusted to 640 °C to investigate the temperature influence on the nanowire growth on the MIC substrate. The nanowire growth was initiated by opening the shutters simultaneously for Ga and As (and Sb in case of sample H), and the growth duration was 10 min for GaAs and 15 min for GaAsSb. For the measurements of the contact angle of the Ga droplets, Ga was deposited for 5 min on samples D–F at 625 °C by only keeping the Ga shutter open. For the core-shell nanowires, the Ga droplet was solidified (to GaAs) after the GaAs core growth by stopping the Ga supply and supplying an As<sub>2</sub> flux of  $8 \times 10^{-6}$  Torr for 10 min. Subsequently, a radial Al<sub>0.3</sub>Ga<sub>0.7</sub>As shell and a GaAs cap were grown to nominal thicknesses of 14 and 6 nm, respectively. After the growth, the morphological features of the nanowires were studied with a Hitachi S5500 scanning electron microscope (SEM), equipped with a Bruker XFlash energy-dispersive x-ray spectroscopy (EDX) Detector, operated at 10–30 kV. To investigate the optical properties, room-temperature (295 K) and low-temperature (11 K)  $\mu$ -PL measurements were carried out on single broken-off nanowires using a 532 nm laser as excitation source. The laser beam with 10  $\mu$ W excitation power was focused to a spot size of  $\sim 2$   $\mu$ m by a 50 $\times$ , 0.65 numerical aperture, infinity-corrected Mitutoyo microscope lens. The emitted light was collected by the same lens and dispersed with a Horiba Jobin-Yvon single grating spectrograph, and the PL signal was detected with an Andor Newton Si charge-coupled camera.

### III. RESULTS AND DISCUSSION

XRD diffractograms taken before (red upper graph) and after (green lower graph) annealing of a MIC substrate with 50 nm amorphous Si and 50 nm Al are shown in Fig. 2.

TABLE I. Summary of the surface condition for each sample before loading into the MBE system.

Sample number	A (GaAs nanowire)	B (GaAs nanowire)	C (GaAs nanowire)	D (droplets deposition)
Surface condition	No oxide	Self-formed oxide after 8 days	Annealed oxide	No oxide
Sample number	E (droplets deposition)	F (droplets deposition)	G (high temp growth)	H (GaAsSb nanowire)
Surface condition	Self-formed oxide after 8 days	Annealed oxide	Annealed oxide	Annealed oxide

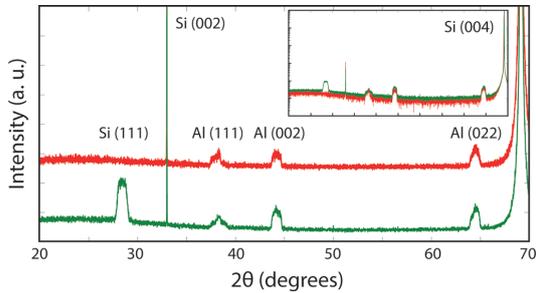


FIG. 2. (Color online) X-ray diffractograms from  $2\theta/\omega$  scan of a MIC sample with 50 nm amorphous Si and 50 nm Al before (red upper graph) and after (green lower graph) the thermal annealing process. The inset shows a logarithmic plot of the two graphs, including the (002)- and (004)-peaks at  $32.96^\circ$  and  $69.13^\circ$ , respectively, from the Si(001) wafer. All data have been normalized to the (004)-peak from the Si(001) wafer.

Before the thermal annealing process, only Al peaks were observed, apart from the reflections from the Si(001) wafer. However, a strong Si(111) peak was observed after the thermal annealing process, suggesting a successful formation of a crystallized and (111)-oriented thin film on top of the amorphous substrate, which is further used for the nanowire growth study.

It has been reported that the oxide layer on top of the substrate has a great influence on self-catalyzed GaAs nanowire growth on monocrystalline Si(111) substrates.<sup>20,21</sup> Different thickness of the oxide layer results in morphological difference among the nanowires as well as in different density of vertical nanowires on the monocrystalline substrate, which should also apply for the MIC substrates.<sup>20</sup> HF etchant is widely used for removing the oxide layer on top of Si substrates for epitaxial semiconductor growth. We used a 5% HF etchant for 2 s to remove the native surface oxide. Since all the samples were immersed in isopropanol for the prevention of oxidation after HF etching and sample A was directly loaded into the MBE system, with minimized exposure to air, the thickness of the top oxide layer in this sample is the thinnest among the three samples A–C. As samples A–C were grown with the same nanowire growth procedure and conditions, the morphological differences between the nanowires from the three samples should therefore result from the sample preparation (i.e., oxidation) method after the HF etching and before the sample loading into the MBE system.

As shown in Fig. 3(a), inhomogeneous-sparsely distributed vertical nanowires were observed for sample A, with parasitic GaAs crystals covering almost the whole sample surface. This parasitic crystal growth suppresses the Ga surface diffusion on the substrate and changes the local nanowire growth environment, which further causes the inhomogeneous morphologies of the nanowires. Parasitic GaAs crystal growth has also been reported for monocrystalline Si(111) substrates with a very thin oxide layer on top, and a low contact angle of the Ga droplets could be attributed as the cause for the massive parasitic GaAs crystal growth.<sup>20</sup> We expect that a too low contact angle of the Ga catalyst droplet is also the cause for the parasitic crystal growth on the MIC substrate with very thin oxide layer (sample A).

As is suggested for the GaAs nanowire growth on monocrystalline Si substrates, a proper Ga contact angle is essential to achieve a high density of vertical nanowires.<sup>20</sup> An oxide layer with proper thickness should thus be formed before loading the substrate into the MBE system in order to keep an optimum contact angle of the droplets. Flow bench air-exposure for a specific duration has been reported to be a method for vertical nanowire density improvement on monocrystalline Si substrates.<sup>20</sup> Sample B was therefore placed in an air flow bench for 8 days in air to form a top oxide layer after the HF etching. However, the parasitic crystal growth on the sample with oxide formation in air for 8 days is even more serious than for sample A without any oxide formation step. For a monocrystalline Si(111) substrate, 8 days air-exposure corresponds to a  $\sim 1.1$  nm oxide thickness, which has been shown to deliver very high density vertical nanowires on monocrystalline Si(111).<sup>20</sup> Compared to the monocrystalline Si(111) substrate, the MIC polycrystalline Si(111) has been formed by an annealing process resulting in many grain boundaries and a lower crystalline quality. Thus, sample B is expected to have a thicker oxide layer than the literature-reported oxide thickness of a monocrystalline Si(111) substrate. Since a thicker oxide layer on top of MIC Si leads to less pin-hole densities where the nanowires nucleate from, the lower density of vertical nanowires on MIC Si by adopting the same preparation procedure as for a monocrystalline Si substrate could be explained. It was also observed in Fig. 3(b) that there is no Ga catalyst droplets on top of the vertical nanowires, which we believe is due to the severe parasitic crystal growth consuming the surface-diffusing Ga adatoms

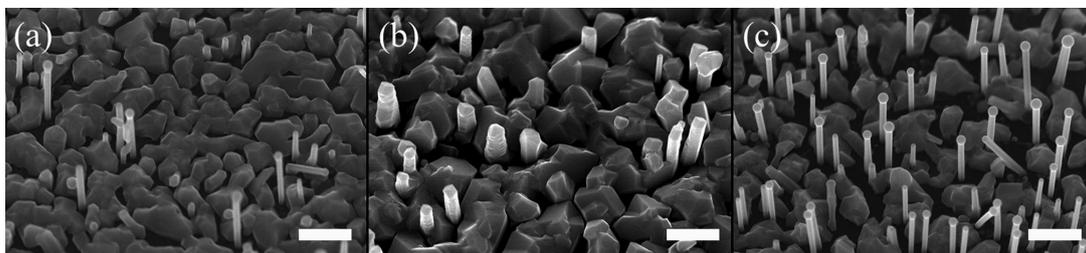


FIG. 3.  $30^\circ$  tilted view SEM images of GaAs nanowires grown on (a) sample A, (b) sample B, and (c) sample C. All scale bars are 1  $\mu\text{m}$ .

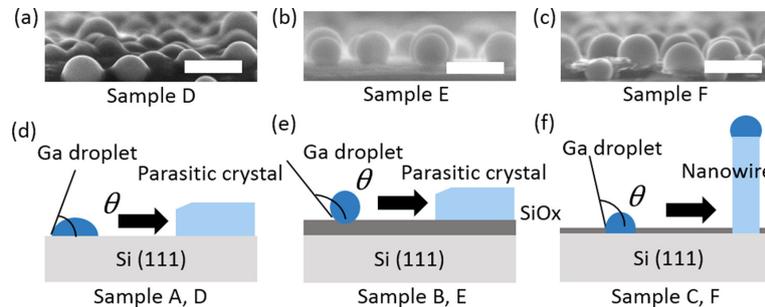


FIG. 4. (Color online) SEM images of cross-section views of (a) sample D, (b) sample E, and (c) sample F. Scale bars are 200 nm. Schematic of the nanowire growth trend on the MIC samples: (d) samples A and D without an oxide layer, (e) samples B and E with a thick oxide layer from 8 days air exposure, and (f) samples C and F with an oxide layer formed by thermal annealing.

that should maintain the Ga catalyst droplets, and thus, the nanowire growth deteriorates in the vapor–solid–liquid regime and results in inhomogeneous nanowire length and diameter.

Hot-plate annealing has been reported to be another effective method for the formation of an oxide layer for vertical nanowire growth.<sup>22</sup> After forming a thin layer of  $\text{SiO}_x$  by hot-plate annealing in air (room temperature  $\sim 20^\circ\text{C}$  with humidity  $\sim 30\%$ ) for 20 min at  $250^\circ\text{C}$ , the nanowire uniformity and vertical nanowire density were improved, as seen from Fig. 3(c). Moreover, the formation of parasitic crystals is reduced. We observe that more of the substrate surface is visible in Fig. 3(c), as compared to for the samples depicted in Figs. 3(a) and 3(b). This thermal annealing step helps the nanowire growth, which could be attributed to two aspects. First, this thin oxide layer keeps the contact angle of the Ga catalyst in a preferential range for vertical nanowire growth. As discussed for nanowire growth on a monocrystalline Si(111) substrate, the freshly etched Si(111) surface has a higher surface energy and the contact angle is too small for vertical nanowire growth.<sup>20</sup> For the thicker oxide formed in sample B, the pinhole density was reduced and the vertical nanowire density was reduced accordingly. It is worth mentioning that the contact angle of the Ga catalyst is larger for particles that are formed on the thicker oxide layer. Second, a possible explanation for nonvertical nanowire growth on the thicker oxide layer could be the increased supersaturation in the droplet as the As flux absorbed by the catalyst is dependent on the

contact angle of the catalyst via a  $1/\sin^2\theta$  relation, where  $\theta$  is the contact angle of the catalyst.<sup>23</sup> Since an increased supersaturation could increase the density of twinning at the nanowire/substrate interface, the nanowire can grow in other directions than the vertical one, for example, as surface nanowires, by the formation of 3D rotational twinning.<sup>24</sup> This mechanism could also explain the observation that more nanowires grow in tilted directions with a thicker oxide layer on the monocrystalline Si(111) substrate.<sup>20</sup>

To investigate the influence of the different pregrowth oxidation treatments on the contact angle of the Ga catalyst, we deposited Ga at the growth temperature to form droplets on three samples (D–F) exposed to the same three different pregrowth oxidation treatments as for samples A–C. SEM images of the resulting droplets on samples D–F are shown in the top part of Fig. 4. With (almost) no surface oxide, the surface energy of sample D is high, resulting in a more wetted surface than for samples E and F. Sample F, which was annealed in air for 20 min, gives more proper contact angles than samples D and E,<sup>20</sup> and upon subsequent nanowire growth, the density of vertical GaAs nanowires would be higher than for samples D and E. A schematic to illustrate the influence of surface oxide on nanowire growth on the MIC polycrystalline Si(111) is shown in the bottom part of Fig. 4.

To investigate the effect of an elevated growth temperature on the nanowire growth on the MIC substrate, sample G was grown at  $640^\circ\text{C}$  using the same pregrowth oxidation treatment as for sample C. Figure 5(a) shows a representative

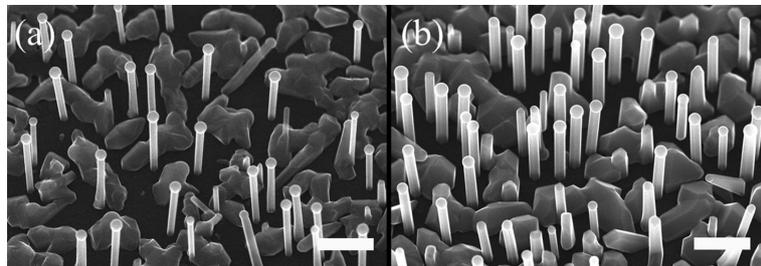


FIG. 5.  $30^\circ$  tilted view SEM images of (a) GaAs nanowires grown on sample G at  $640^\circ\text{C}$  and (b) GaAsSb nanowires grown on sample H at  $625^\circ\text{C}$ . All scale bars are  $1\ \mu\text{m}$ .

SEM image of sample G. Whereas larger clean surface areas without parasitic crystals could be observed for sample G as compared to sample C [Fig. 3(c)], which was grown at 625 °C, the density of vertical nanowires is slightly reduced. It has been previously reported that the three-dimensional twinning phenomenon can result in the formation of unwanted parasitic nonvertical nanowires for self-catalyzed GaAs nanowires.<sup>24</sup> This suggests that a reduction of the unwanted twinning for self-catalyzed GaAs-based nanowires should benefit the vertical nanowire growth with a higher density on the MIC substrate. It has been found that the incorporation of Sb in self-catalyzed GaAs-based nanowires can stabilize the crystal phase in the zinc blende structure,<sup>25</sup> which reduces the twinning density in nanowires. Thus, to investigate if incorporation of Sb improves the density of nanowires on the MIC substrate, a sample H with self-catalyzed GaAsSb nanowires were grown at 625 °C using the same pregrowth oxidation treatment as for samples C and G. A representative SEM image of sample H is shown in Fig. 5(b). The density of vertical nanowires is found to be much higher for self-catalyzed GaAsSb nanowires compared with the GaAs nanowires, demonstrating that the incorporation of Sb (~11% estimated by EDX) helps the vertical growth of self-catalyzed GaAs-based nanowires on the MIC substrate.

PL measurements were carried out on single GaAs/AlGaAs core-shell nanowires at room temperature (295 K) and low temperature (11 K) to evaluate the optical quality of the GaAs nanowires grown on a MIC polycrystalline Si(111) substrate that underwent the same sample preparation procedure as sample C. In Fig. 6, the PL spectrum at room temperature shows an emission peak at 1.43 eV, which corresponds to the bandgap of GaAs at room temperature. The low-temperature spectrum shows PL peaks at 1.48 and 1.51 eV. The 1.51 eV peak is due to GaAs free-exciton emission, which is usually observed in GaAs/AlGaAs core-shell nanowires,<sup>26</sup> whereas the 1.48 eV peak is most probably due to defect-induced emission, also observed for self-catalyzed GaAs nanowires grown on monocrystalline Si(111) under relatively high effective Ga/As flux ratios.<sup>27</sup> The PL emission is similar to what we have

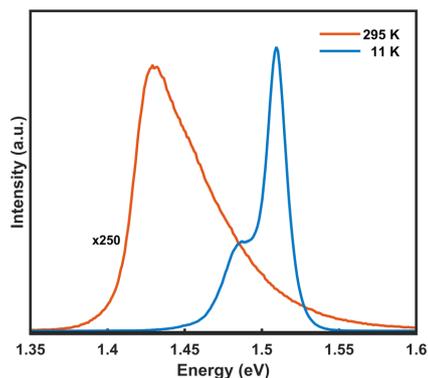


FIG. 6. (Color online) PL spectra of a single GaAs/AlGaAs core-shell nanowire grown on MIC polycrystalline Si(111) substrate measured at 295 and 11 K.

observed for GaAs nanowires grown on monocrystalline Si(111), indicating that the nanowires grown on MIC polycrystalline Si(111) substrates are of similar high optical quality.

#### IV. SUMMARY AND CONCLUSIONS

In conclusion, a MIC process was utilized to form a Si layer with (111)-oriented surface on an amorphous substrate to grow vertical self-catalyzed GaAs nanowires by MBE. We demonstrated the importance of pregrowth oxide formation on the MIC Si surface for the growth of GaAs nanowires. By thermally annealing the substrates in air, the density of vertical nanowires was improved and the parasitic GaAs crystal growth was reduced further by increasing the growth temperature. By incorporating Sb during nanowire growth, the density of vertical nanowires was considerably improved. The optical measurements of the nanowires grown by this process show a high quality similar to nanowires grown on a monocrystalline Si(111) substrate. Our results show a route toward optimized conditions for the growth of self-catalyzed GaAs-based nanowires on a MIC substrate for achieving optoelectronic devices with high density of vertical nanowires on arbitrary substrates.

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## Paper III

# Graphene as Transparent Conducting Substrate for The Fabrication of Flip-chip Ultraviolet Light-Emitting Diode Based on GaN/AlGaN Nanocolumns

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To be submitted (2020)

PAPER III. GRAPHENE AS TRANSPARENT CONDUCTING  
SUBSTRATE FOR THE FABRICATION OF FLIP-CHIP ULTRAVIOLET  
LIGHT-EMITTING DIODE BASED ON GAN/ALGAN NANOCOLUMNS

This Paper is awaiting publication and is not included in NTNU Open

## Paper IV

# GaN/AlGaN nanocolumn ultraviolet LED using double-layer graphene as substrate and transparent electrode

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PAPER IV. GAN/ALGAN NANOCOLUMN ULTRAVIOLET LED USING  
DOUBLE-LAYER GRAPHENE AS SUBSTRATE AND TRANSPARENT  
ELECTRODE

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## GaN/AlGaIn Nanocolumn Ultraviolet Light-Emitting Diode Using Double-Layer Graphene as Substrate and Transparent Electrode

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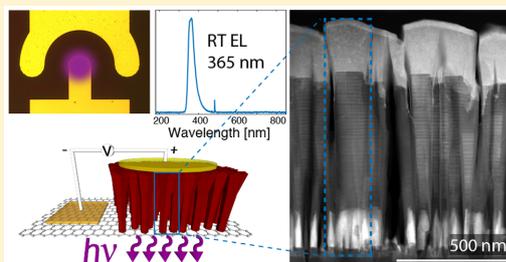
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### Supporting Information

**ABSTRACT:** The many outstanding properties of graphene have impressed and intrigued scientists for the last few decades. Its transparency to light of all wavelengths combined with a low sheet resistance makes it a promising electrode material for novel optoelectronics. So far, no one has utilized graphene as both the substrate and transparent electrode of a functional optoelectronic device. Here, we demonstrate the use of double-layer graphene as a growth substrate and transparent conductive electrode for an ultraviolet light-emitting diode in a flip-chip configuration, where GaN/AlGaIn nanocolumns are grown as the light-emitting structure using plasma-assisted molecular beam epitaxy. Although the sheet resistance is increased after nanocolumn growth compared with pristine double-layer graphene, our experiments show that the double-layer graphene functions adequately as an electrode. The GaN/AlGaIn nanocolumns are found to exhibit a high crystal quality with no observable defects or stacking faults. Room-temperature electroluminescence measurements show a GaN related near bandgap emission peak at 365 nm and no defect-related yellow emission.

**KEYWORDS:** Graphene, semiconductor nanocolumn, UV optoelectronics, LED, nitride-based devices, electrical injection



With the emergence of new semiconductor nanomaterials and heterostructures, new possibilities for optoelectronics arise. The semiconductor materials most commonly used for optoelectronics today, such as Si,<sup>1</sup> GaAs,<sup>2</sup> InAs,<sup>2</sup> ZnO,<sup>3</sup> and GaN with its alloys,<sup>2</sup> exhibit structural imperfections when grown as heteroepitaxial thin-films, for instance, twinning defects, threading dislocations, and stacking faults. This is due to a large lattice mismatch between these materials as well as with conventional substrates. By nanostructuring the semiconductor materials in the forms of columns or pyramids, new combinations of materials can be explored, and new substrates can be employed for the epitaxial growth.

An intriguing potential substrate for epitaxial growth of semiconductors is graphene, the single-layer form of carbon, as it can not only act as an atomically thin crystalline growth template but also has outstanding functional properties when it comes to strength, flexibility, and electron and thermal conductivity.<sup>4,5</sup> Hybrid systems based on the growth of semiconductor nanocolumns on different graphitic substrates have been intensively studied in the past decade with the aim of developing new functionalities and higher efficiency optoelectronic devices as, for example, solar cells, photodetectors, light-emitting diodes (LEDs) and lasers. Such hybrid

systems have been demonstrated for GaAs,<sup>6</sup> InAs,<sup>7–9</sup> InAsSb,<sup>10</sup> In(Ga)As,<sup>11,12</sup> ZnO,<sup>13,14</sup> and GaN. With regards to the growth of GaN nanocolumns, different graphitic forms have been used as growth substrate, for instance, graphite,<sup>15</sup> transferred chemical vapor deposition (CVD) graphene (single- and multilayer),<sup>16–25</sup> and epitaxial graphene.<sup>26</sup> However, these studies mostly focused on the growth of the nanocolumns without further demonstration of a hybrid device realization.

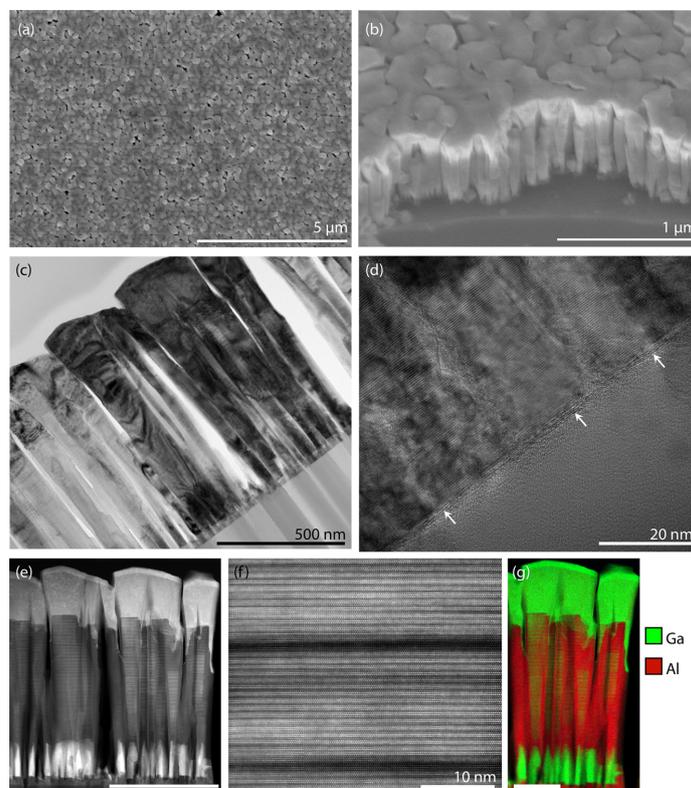
In addition to the attributes already mentioned, graphene has the attractive property of being transparent in all parts of the electromagnetic spectrum and has been demonstrated as a top-emitting transparent conductive electrode (TCE) for GaN<sup>27,28</sup> and InGaIn LEDs.<sup>29–31</sup> In contrast to the traditional TCE in optoelectronic devices, indium tin oxide, graphene is transparent in the whole UV region of the electromagnetic spectrum (100–350 nm),<sup>32</sup> offering a potential solution for devices operating in this region.

Recently, our group showed GaN/AlGaIn nanocolumn growth with a single-layer graphene substrate as the bottom

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**Figure 1.** Overview of self-assembled GaN/AlGaIn nanocolumns by SEM and their structural details by TEM. (a,b) Top- and bird-view SEM images of nanocolumns grown on DLG transferred onto amorphous silica glass. (c) BF TEM image of the nanocolumns shows local preferential orientation as several neighboring nanocolumns are simultaneously on-axis, indicating epitaxy with the graphene substrate. The nanocolumns grow in the [0001]-direction. (d) High-resolution BF TEM image showing the DLG (white arrows) between the amorphous silica glass support and the crystalline nanocolumns. (e) A superlattice-like structure can be observed by HAADF STEM (scale bar 500 nm). (f) High-resolution HAADF STEM image of alternating Al-rich/Ga-rich layers in the superlattice-like n-AlGaIn nanocolumn segment. (g) Compositional mapping by EDS and EELS of the different GaN/AlGaIn segments shows an actual nanocolumn heterostructure consisting of n-AlN/n-GaN/n-Al<sub>0.76</sub>Ga<sub>0.24</sub>N/p-Al<sub>0.42</sub>Ga<sub>0.58</sub>N/p-GaN (scale bar 200 nm).

electrode.<sup>25</sup> However, so far there has been no realization of utilizing graphene simultaneously as the growth substrate and the TCE of a semiconductor device. Here, we demonstrate a UV-A LED using transferred double-layer graphene (DLG) both as the substrate for GaN/AlGaIn nanocolumn growth and as the TCE in the processed device. Along with the reduced sheet resistance of DLG compared to single-layer graphene,<sup>33</sup> it is expected that the additional top layer of graphene will protect the bottom layer of graphene from plasma nitridation damage during growth. The electric current is thus injected directly from the conducting DLG substrate in a “vertical” flip-chip device configuration, which can be advantageous when compared to traditional mesa LED structures with lateral current injection that suffer from current crowding.<sup>34–36</sup>

**Nanocolumn Growth and Structural Characterization.** In this work, we have grown catalyst-free, self-assembled Al<sub>x</sub>Ga<sub>1-x</sub>N/GaN nanocolumn heterostructures on transferred DLG on amorphous silica glass by radio frequency plasma-assisted molecular beam epitaxy (RF-PAMBE) under N-rich conditions (see *Methods* for the detailed information on the growth). The intended LED structure is shown schematically

in *Figure S1a* in the *Supporting Information*, where each nanocolumn is designed to consist of 40 nm n-AlN, 140 nm n-GaN, 550 nm n-Al<sub>0.25</sub>Ga<sub>0.75</sub>N, 27 nm undoped GaN, 200 nm p-Al<sub>0.25</sub>Ga<sub>0.75</sub>N, and 20 nm p-GaN. Here, we would like to emphasize that the length of each aforementioned segment is based on nominal values. In addition, the indicated Al and Ga compositions are nominal compositions, that is, based on the ratio between the Al and Ga fluxes (see *Table S1* in *Supporting Information*). To verify these values, further transmission electron microscopy (TEM) investigations were carried out and will be discussed in the following paragraphs. A thin AlN buffer layer does not only serve as a nucleation site for n-GaN<sup>17,23–25</sup> but it also reduces damage to the graphene induced by impinging active N species generated by the RF plasma source<sup>17,23–26,37</sup> and in-plane strain generated by GaN nucleation.<sup>23,38</sup> To achieve an even higher density of nanocolumns, the AlN deposition method is modified<sup>25</sup> from the migration enhanced epitaxy (MEE) technique which was utilized to obtain 1 μm long vertically aligned GaN nanocolumns on single-layer<sup>23,24</sup> and multilayer graphene.<sup>17</sup> In addition, a higher probability of vertical growth of n-GaN

nanocolumns on graphene was achieved, which is important for the subsequent vertical n-AlGaIn nanocolumn growth.<sup>39,40</sup>

Shown in Figure 1a,b are the top- and bird-view scanning electron microscopy (SEM) images of the self-assembled GaN/AlGaIn nanocolumns grown on DLG. It can be seen that the nanocolumns coalesce with each other, forming an almost continuous filmlike layer in the top part of the nanocolumns. The top-view SEM image from the center area of the sample (Figure 1a) shows that the geometry of some of the uncoalesced nanocolumns exhibits near-perfect hexagonal morphology. In addition, there are a few small gaps (less than 50 nm) between some nanocolumns and their neighbors. From some of the nanocolumns with distinguished hexagonal cross-sectional geometrical shape, the average top diameter is found to be about 220 nm. Figure 1b shows a bird-view SEM image, indicating that the nanocolumns are highly dense and vertically oriented with respect to the graphene/glass substrate, as well as demonstrating a relatively uniform height distribution. Figure S1b in the Supporting Information is a representative side-view SEM image of the grown GaN/AlGaIn nanocolumns, where the average height and average bottom- and top-diameter of the grown nanocolumns, as derived from 20 SEM images, are found to be 1070, 35, and 220 nm, respectively. It is evident that the nanocolumn geometry exhibits a highly inverse-tapered structure due to the abrupt growth temperature reduction by 200–220 °C starting from the p-AlGaIn segment, forming a champagne glass-like structure, similar to the work reported by Sekiguchi et al.<sup>39</sup> As a result of the low growth temperature (675–695 °C), the nanocolumns tend to grow faster in the radial direction, causing the top part of the nanocolumns to coalesce with each other. Such coalesced nanocolumns are used in order to ensure a uniform and continuous metal contact to the top p-GaN segment in the subsequent LED processing, preventing discontinuous metal deposition on p-GaN as shown in previous work.<sup>25</sup> Furthermore, metal can be deposited without the use of any insulating filler material between nanocolumns. The reasons for lowering the growth temperature during growth of the p-AlGaIn and p-GaN segments of the device structure are explained in more detail in the Supporting Information.

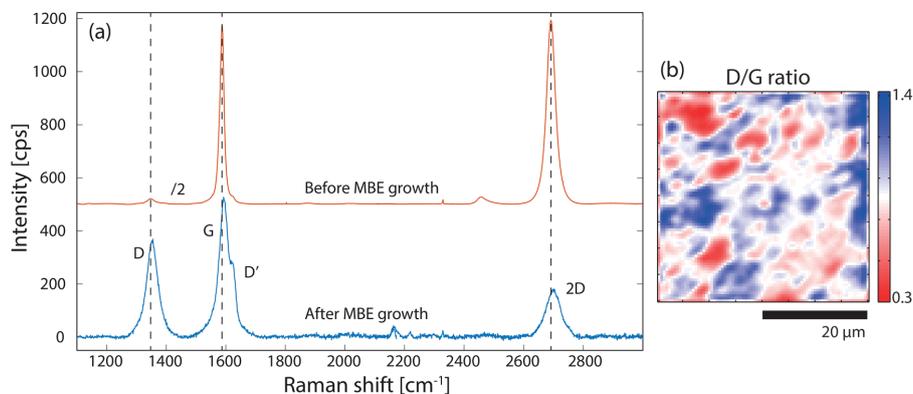
Detailed structural characterization was further carried out by TEM. Figure 1c shows a bright-field (BF) TEM overview image of the self-assembled GaN/AlGaIn nanocolumns. All nanocolumns grow in the [0001]-direction, which was observed by electron diffraction for more than 20 nanocolumns and is exemplified in the diffraction pattern in Figure S2a in the Supporting Information. This is consistent with previous reports of GaN nanocolumns grown on single-layer<sup>16,18,23,24</sup> and multilayer graphene.<sup>17,26</sup> The darker contrast nanocolumns shown in Figure 1c are oriented with the electron beam parallel to the [2110]-direction, that is, they possess a very similar in-plane orientation. Tilting the sample to different in-plane orientations reveals several clusters of identically oriented nanocolumns on the micrometer-scale. Since the CVD DLG used as a substrate is polycrystalline, the observed preferred in-plane orientation of the nanocolumns is an indication that they adopt an epitaxial orientation related to the graphene lattice and thus follow the orientation of a particular graphene grain.<sup>6</sup> The DLG can be distinguished in Figure 1d as indicated by the red arrows. The exact number of layers cannot be confirmed by this image, as the graphene layers are buckled and the two-dimensional image of the TEM

lamella thus indicates more than two layers.<sup>23</sup> The nanocolumns exhibit a pure wurtzite crystal structure and no interfacial layer, which is identical with our observation in the growth of n-GaN nanocolumns on graphene using an MEE-AlN buffer layer<sup>23</sup> but different from n-GaN nanocolumns grown directly on silica glass.<sup>41</sup> No dislocations, stacking faults or other defects are found in the GaN- and AlGaIn-nanocolumn segments. The AlN buffer layer, however, is found to have some dislocations and point defects. Using high-angle annular dark-field scanning TEM (HAADF STEM) to get a Z-contrast image of the nanocolumns in Figure 1c, the different segments of the GaN/AlGaIn nanocolumns can be distinguished, as shown in Figure 1e.

The AlN buffer layer, seen in the base of the nanocolumns, tends to assemble as a continuous layer, although there are a few AlN islands as well. Short stems consisting of n-GaN are clearly visible below the n-AlGaIn nanocolumn segments. A slight oscillation of the Ga/Al-ratio in the n-AlGaIn segment is noticeable, forming a superlattice-like structure as is more evident in the HAADF STEM image in Figure 1f (the line scan can be seen in Figure S2b in the Supporting Information). The main reason for such composition inhomogeneity could be kinetical;<sup>42</sup> as a consequence of a difference in sticking coefficients and diffusion lengths for Al and Ga adatoms as well as a competition between Al and Ga incorporation during the nanocolumn growth. This would be the case for both the direct impingement on the top of the nanocolumns and for diffusion along the nanocolumn sidewalls.<sup>42,43</sup> As the higher Al-content barriers in the superlattice-like structure in the n-AlGaIn segment are only ~2–3 nm thick, it is unlikely that they will affect the electronic properties of the nanocolumns. From Figure S2c in the Supporting Information, a higher Al-content nanocolumn shell-layer can be seen surrounding the AlGaIn nanocolumn core, which might act as a self-passivation layer for the nanocolumn side facets. No intrinsic GaN segment is observed in the TEM images, which is likely caused by the complete desorption of this layer during the growth interruption needed to reduce the temperature for the subsequent p-AlGaIn growth, as the Ga desorption rate is very high at these substrate temperatures.<sup>44</sup> The p-AlGaIn segment and thin p-GaN contact layer grow highly inverse-tapered (as desired for the subsequent process of top contact metallization), indicating a switch from N-polar to Ga-polar growth mode (for improvement of p-type doping efficiency),<sup>45</sup> which is further evidenced by a switch from planar to inclined interfaces at the top of the nanocolumns.

The elemental composition of the different segments is estimated by combining X-ray electron dispersive spectroscopy (EDS) with electron energy loss spectroscopy (EELS), using the pure AlN and GaN layers at the bottom and top of the nanocolumns as references, respectively. The results shown in Figure 1g indicate that the n-AlGaIn segment has a composition of 76% Al close to the p–n junction, while the p-AlGaIn segment has a composition of 42% Al (more detailed in Figure S2c in the Supporting Information). These values may have contributions from the Al-rich shell leading to an overestimation of the Al-content in the n- and p-AlGaIn segments. However, most of the large deviation from the designed n- and p-AlGaIn segment composition of 25% Al is most likely caused by the higher Ga desorption rate as explained above.

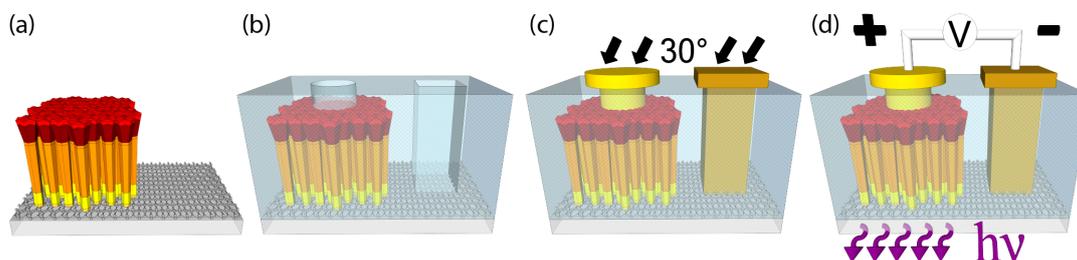
**Graphene Electrode.** The nitrogen plasma sources utilized during RF-PAMBE growth of III–N nanocolumns



**Figure 2.** Micro-Raman characterization of DLG before and after RF-PAMBE GaN/AlGaIn nanocolumn growth. (a) Averaged micro-Raman spectra from a  $40 \times 40 \mu\text{m}$  area with a  $1 \mu\text{m}$  step size before (offset by 500 cps for clarity) and after nanocolumn growth, respectively. The intensity of the spectra taken before nanocolumn growth have been divided by two, and peak positions are indicated by the dashed lines. (b) Map of the same area shows the spatial variation of defects as represented by D/G peak intensity ratio.

**Table 1. Micro-Raman Peak Positions, Intensities, and Ratios**

sample	median D/G ratio	median G		median 2D			median 2D/G ratio
		position [ $\text{cm}^{-1}$ ]	intensity [cps]	position [ $\text{cm}^{-1}$ ]	intensity [cps]	fwhm [ $\text{cm}^{-1}$ ]	
DLG before MBE growth	0.04	1587	1003	2692	1314	37	1.31
DLG after MBE growth	0.9	1597	532	2698	169	58	0.32



**Figure 3.** Schematic of the fabrication steps of the flip-chip UV LED device. (a) The nanocolumns are grown by RF-PAMBE on a DLG/silica glass substrate. (b) An insulating polymer is deposited and separate areas of graphene and nanocolumns are opened for the bottom and top metal contacts, respectively. (c) A Ni/Au metal stack contacts the top layer of p-GaN of the nanocolumns (deposited at an angle of  $30^\circ$  with the substrate plane), while Au contacts the graphene at the bottom. (d) The LED device is biased between the two contacts, and light is emitted through the graphene/silica glass substrate in a flip-chip configuration.

are known to have a damaging effect to graphene.<sup>23–26,37</sup> To assess the extent of the possible damage, the DLG was characterized by micro-Raman spectroscopy and sheet resistance measurements before and after nanocolumn growth. Figure 2a shows the average micro-Raman spectrum from 1600 measurements of DLG before and after nanocolumn growth. The graphene is notably damaged after growth, as evidenced by the increase in the defect-related D-peak at  $\sim 1350 \text{ cm}^{-1}$ , the reduction in the G- and 2D-peaks at  $\sim 1600 \text{ cm}^{-1}$  and  $\sim 2700 \text{ cm}^{-1}$  and the appearance of the D'-peak at  $\sim 1620 \text{ cm}^{-1}$ . Mapping the peak intensity ratio of the D- and G-peaks in Figure 2b reveals that the defect distribution is nonuniform in graphene after the nanocolumn growth with some areas resembling the pregrowth graphene quality while others are extensively damaged. The increased presence of defects in graphene may lead to an increase in carrier scattering and therefore an increase in the graphene sheet resistance. This is

confirmed by van der Pauw measurements, where the sheet resistance is found to increase from  $329 \Omega/\square$  before nanocolumn growth to  $2326 \Omega/\square$  after growth for the DLG. For single-layer graphene, the sheet resistance increases more severely, that is, from  $779 \Omega/\square$  before nanocolumn growth to  $86869 \Omega/\square$  after growth. It is worth to mention that the nitrogen plasma emission during nanocolumn growth is two times higher and the total growth time is two times longer than for our previous work<sup>25</sup> (see Table S1 in Supporting Information), resulting in more defective graphene and consequently a larger sheet resistance, especially for the single-layer graphene. However, for the case of DLG, the limited increase in sheet resistance shows that the top layer of graphene protects the bottom layer and thus limits the extent of the damage in the bottom layer. The UV transparency of transferred DLG on silica glass is reduced by an additional  $\sim 3\%$  compared to that of transferred single-layer graphene on

the same substrate carrier, retaining a total transmission of more than 80%.<sup>46</sup>

Table 1 shows the D, G, and 2D peak positions, intensities, and ratios of the micro-Raman spectroscopy mapping, and maps of these parameters can be found in Figure S3 in the Supporting Information. The apparent blue-shift of the G- and 2D-peaks for the DLG could be due to doping and/or strain in graphene after the nanocolumn growth.<sup>47</sup> It is known that exposure to nitrogen plasma may n-type dope graphene.<sup>37</sup> Using the correlation analysis developed by Lee et al.,<sup>48</sup> one can untangle how much strain and doping contributes to the Raman shift, but as there is a notable occurrence of defects in the DLG after nanocolumn growth it is not possible to conclude on the exact origin of the peak-shifts.

**LED Fabrication and Electrical Characterization.** The graphene-nanocolumn LED devices were fabricated as shown schematically in Figure 3. After nanocolumn growth, Ti was removed from the backside by mechanical removal and etching the sample in a buffered oxide etch, where hydrofluoric acid dissolves the Ti (Figure 3a). Contact areas to the graphene and nanocolumns were defined by photolithography (Figure 3b), and the metal contacts were deposited by electron beam evaporation (Figure 3c). A Ni/Au metal stack of 50/100 nm thickness was used as a top contact to the thin-film like p-GaN surface layer of the nanocolumns. To avoid deposition on the graphene, the top contact metals were deposited at an  $\sim 30^\circ$  angle with regards to the substrate plane. For the bottom metal contact to the graphene, 200 nm Au was used, which is known to give an ohmic contact to graphene with a low contact resistance.<sup>49</sup> In this configuration, light can be emitted through the transparent graphene/silica glass substrate of the sample as a flip-chip type device (Figure 3d), and the continuous graphene electrode allows for vertical current injection through the nanocolumns. Figure 4a shows an optical microscopy

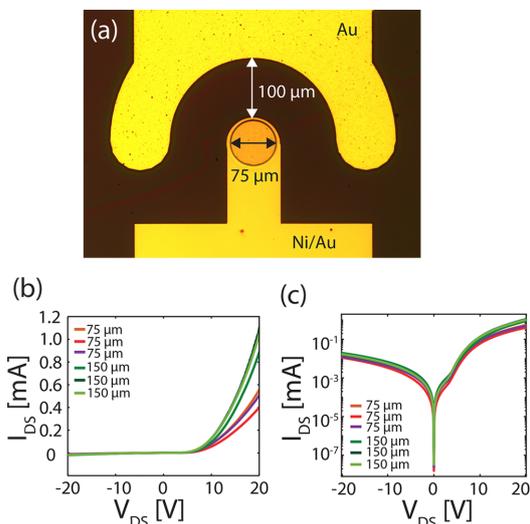
image of the LED device with the graphene–Au contact at the top of the image and p-GaN nanocolumn–Ni/Au contact at the bottom. The LED devices have apertures of 75 or 150  $\mu\text{m}$  diameter, and the distances between the top and bottom metal contacts were fixed at  $\sim 100 \mu\text{m}$ .

Figure 4b shows the current–voltage ( $I$ – $V$ ) curves measured for six different LED devices on the same sample, and Figure 4c shows the same data in a semilogarithmic scale. The different curves are from devices with different LED apertures. Devices with the same size show similar diode characteristics, indicating uniform nanocolumn growth and junction formation. For the same bias voltage, one would expect a quadrupled current level for the device with a doubled diameter, but as the current only increases by a factor of  $\sim 2$  it is evident that the injection current does not scale with the aperture area. This could be an effect of the defect generation in the graphene layers caused by nanocolumn growth, which also causes a relatively large sheet resistance, as was discussed above. The turn-on voltage is found to be 7.7 V (by intersecting the semilinear region of the  $I$ – $V$  curve between 10 and 12 V and the voltage axis), somewhat larger than expected for a GaN/AlGaIn nanocolumn LED,<sup>50</sup> but considering the high Al-content of the n-AlGaIn and p-AlGaIn layers a higher turn-on voltage is more reasonable. However, the high resistance of the device makes it difficult to define an exact turn-on voltage, as multiple semilinear regions could possibly be used to find different intersections. In the semilog-plot in Figure 4c, two voltage regions can be distinguished. A less steep slope below  $\sim 3.5$  V can be seen, and the current below this value is attributed to leakage due to acceptor level recombination and electron overshoot.<sup>51</sup>

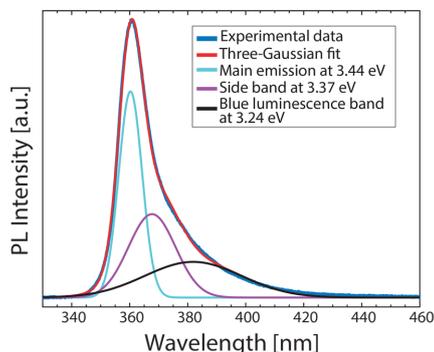
Using the elemental compositions measured by combined EDS and EELS for the Al<sub>1-x</sub>Ga<sub>x</sub>N segments, the band gaps can be calculated by a model using local density approximation (LDA-1/2)<sup>52</sup>. The band gap of AlN is 6.28 eV and GaN 3.44 eV, so using a bowing parameter of 0.8 eV yields band gaps of 5.45 eV (227 nm) and 4.44 eV (279 nm) for the n-Al<sub>0.76</sub>Ga<sub>0.24</sub>N and p-Al<sub>0.42</sub>Ga<sub>0.58</sub>N segments, respectively.<sup>52</sup> The higher Al-composition at the n-doped side will increase electron leakage to the p-AlGaIn side of the p–n junction.

**LED Emission and Optical Power Output.** Low temperature photoluminescence (PL) measurements show a main emission peak at 360 nm (3.44 eV), in addition to two weaker and less defined bands at 368 nm (3.37 eV) and 382 nm (3.25 eV), as shown in Figure 5. The latter band, typically referred to as the blue luminescence band, originating from donor–acceptor-pair recombination, in conjunction with the absence of a yellow luminescence band strongly indicates that the PL emission originates from the top p-type GaN nanocolumn layer. The main emission peak at 360 nm (365 nm at room temperature (RT)) is most likely attributable to Mg<sub>Ga</sub> acceptor bound excitons, as commonly done in the literature.<sup>53</sup> The internal quantum efficiency (IQE) at RT is estimated from the ratio of the integrated PL intensity at RT to the interpolated value at  $T = 0$  K (see Figure S4 in Supporting Information for further details). The obtained IQE is dependent on the excitation power density used,<sup>54</sup> and the maximum value determined in our experiments was  $\sim 46\%$  at an excitation power of 5.5 mW.

The LED device performance was further investigated by RT continuous current injection electroluminescence (EL) measurements, where the EL is detected either by a UV sensitive detector inside an integrating sphere for power



**Figure 4.** Processed LED device and  $I$ – $V$  characteristics. (a) Optical microscope image from the p-GaN side of a 75  $\mu\text{m}$  diameter aperture LED device (before flip-chip). (b,c) Linear and logarithmic  $I$ – $V$  characteristics, respectively, from six LED devices with aperture sizes of 75 and 150  $\mu\text{m}$  diameters.

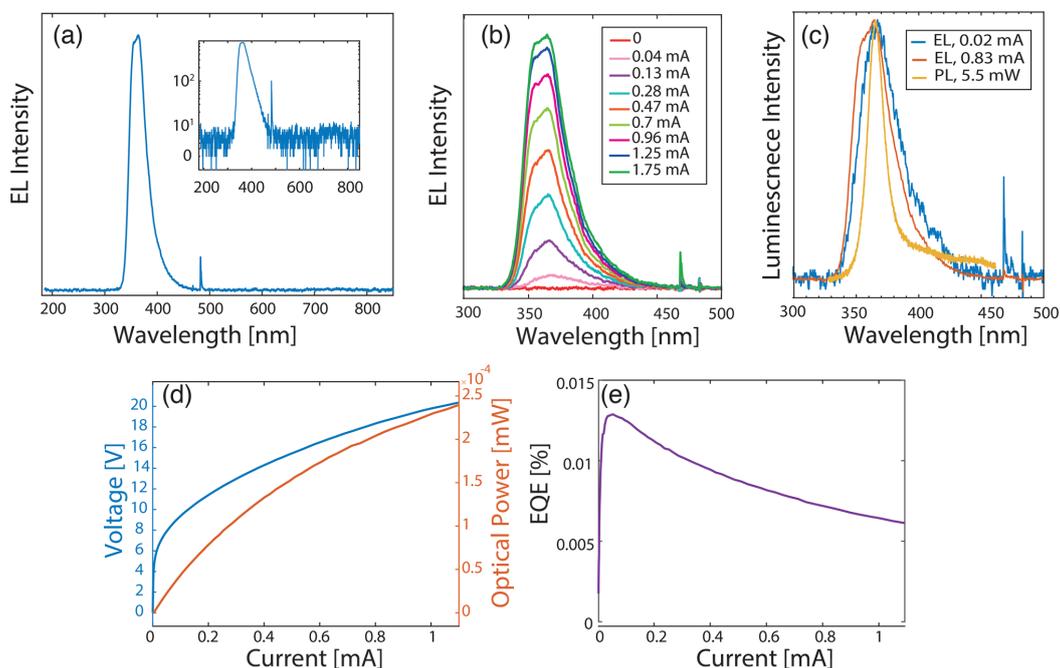


**Figure 5.** Low-temperature 10 K photoluminescence spectrum of the LED device. The main PL emission is at 360 nm (3.44 eV) with two side bands at 368 nm (3.37 eV) and 382 nm (3.24 eV). For an interpretation of the PL spectrum see main text.

measurements, or a spectrometer for spectral information. Figure 6a,b shows the measured light under different current injection conditions, with a main peak emission at 365 nm with a full width at half-maximum (fwhm) of 37 nm at 20 V, which is slightly broader than near-UV GaN/AlGaIn nanocolumn LEDs grown on Si substrates.<sup>55</sup> As already discussed above in relation with the TEM images in Figure 1e,g, there is no intrinsic GaN layer observed between the n-Al<sub>0.76</sub>Ga<sub>0.24</sub>N and

p-Al<sub>0.42</sub>Ga<sub>0.58</sub>N nanocolumn segments. In addition, the main EL emission measured at 365 nm resembles closely the main PL emission band at RT with the exception of the weak UV and blue-luminescence defect-related PL bands and a shorter-wavelength shoulder in the EL spectra appearing at high forward bias, as illustrated in Figure 6c. Therefore, it is most likely that similarly to the PL recombination, the EL recombination also occurs in the p-GaN nanocolumn layer. Several peaks contribute to the EL emission around 365 nm, indicating some local inhomogeneity in the thin p-GaN nanocolumn contact layer. There is no notable EL peak shift with increasing injection currents up to 1.1 mA. EL emission is detected from ~4.5 V, and the intensity is seen to increase linearly with the injected current at lower voltages before saturating at higher voltages >18 V. No defect-related yellow EL emission was detected,<sup>56</sup> as evidenced by the semi-logarithmic data representation of the inset in Figure 6a.

The external quantum efficiency (EQE) of the LED is a product of the IQE, the current injection efficiency (CIE) and the light extraction efficiency (LEE). Figure 6d shows the measured optical power with respect to the injected current. The slope of the dependence gradually decreases as the current increases due to droop,<sup>57</sup> which can be more clearly seen by calculating the EQE as a function of injection current. The EQE is defined as the ratio of emitted photons over the number of injected electrons as given by the expression



**Figure 6.** Room-temperature electroluminescence measurements and LED device efficiency. (a) Electroluminescence spectrum measured for a 150  $\mu\text{m}$  diameter aperture LED device under a bias of 20 V, with the logarithmic plot in the inset, showing a peak emission at 365 nm. (b) EL spectra at different injection currents. (c) Comparison between RT PL and EL spectra normalized to their respective maximum intensity. (d) Voltage and optical output power dependency on injection current. (e) External quantum efficiency (EQE) at varying injection current measured using an integrating sphere.

$$\text{EQE} = \frac{q^*P_{\text{opt}}}{I^*h\nu} \quad (1)$$

where  $q$  is the electron charge,  $P_{\text{opt}}$  is the measured optical power,  $I$  is the injected current, and  $h\nu$  is the energy of the emitted photons. The measured EQE is shown in Figure 6e, and it is clear that the LED device is most efficient at current injections around 0.05 mA for a 150  $\mu\text{m}$  diameter aperture device, with a continuous decrease in the EQE with increasing forward bias. A major factor for the low EQE of this LED is believed to be the low effective hole doping in especially the p-AlGaIn segment causing hole-blocking at the p-GaN/p-AlGaIn interface. Because of this, the holes cannot reach the middle of the p-n junction and instead the EL recombination occurs in the thin p-GaN contact layer which is intrinsically a region with a low EQE. The absorption of the 140 nm long n-GaN segment at the emission wavelength of 365 nm can be considered to be negligible. However, one must design a shorter n-GaN segment for UV LEDs emitting below 365 nm as the absorption coefficient increases abruptly above the GaN band gap.<sup>58</sup> In this study, the nanocolumns are randomly positioned (by self-assembly) across the graphene substrate. However, controlling the nanocolumn diameter and spacing by, for example, selective area growth with a hole-patterned mask can potentially increase the EQE by enabling coupling of the light emission into guided modes along the nanocolumns, as demonstrated in AlGaIn- and InGaIn-based nanocolumn/nanopyramid arrays.<sup>50,59–62</sup> Furthermore, one can reduce EQE droop by inserting an electron blocking layer on the p-side of the active layer, preventing electrons from overshooting the recombination region.<sup>63</sup> By incorporating quantum wells in the active layers, the efficiency can be further improved as the probability of radiative recombination increases.<sup>64</sup> Reducing the sheet resistance of graphene would lower the operating voltage of the LED, and there are several methods to achieve this. The reduction of plasma-damage has already been discussed, but in addition conducting elements can be deposited on the graphene if the LED is delaminated from the glass substrate.<sup>65</sup> Examples of conducting elements are Ag nanowires<sup>66</sup> and Au dots.<sup>67</sup>

To summarize and conclude, we have shown that DLG can be used as a substrate for RF-PAMBE growth of GaN/AlGaIn nanocolumns, and subsequently as the transparent electrode in a fabricated UV-A LED device. Although graphene gets damaged by plasma-activated nitrogen during the nanocolumn RF-PAMBE growth, the DLG retains its prominent characteristics and functions as a transparent electrode. Electroluminescence emission is achieved during continuous biasing at a wavelength of 365 nm with no defect-related yellow emission. On the basis of temperature-dependent PL, an IQE of  $\sim 46\%$  is estimated, confirming the high crystal quality of the nanocolumns. These results indicate that graphene can be used as a functional substrate and electrode for III-nitride-based device technology. Furthermore, we have indicated several possible steps for growth and device design optimization to improve the EQE now that this platform has been established.

**Methods. Substrate Preparation.** The DLG is formed by two successive transfers of single-layer graphene. In this work, we used commercially available DLG as a substrate which was synthesized using CVD on Cu foil<sup>33</sup> and transferred to a substrate carrier of amorphous silica glass by Graphene Platform Corp. (Tokyo, Japan). The backside of the substrate was coated with an approximately 300 nm thick Ti layer for

efficient and uniform absorption of thermal radiation from the heater to the substrate, as well as assisting the pyrometer reading during nanocolumn growth.

**Growth of GaN/AlGaIn Nanocolumns.** The catalyst-free and self-assembled GaN/Al<sub>x</sub>Ga<sub>1-x</sub>N nanocolumn heterostructures were grown in an EpiQuest RF-PAMBE system under N-rich conditions.<sup>17,39</sup> Standard effusion cells were used to supply Al, Ga, Mg (p-type dopant), and Si (n-type dopant) atoms, while atomic nitrogen was supplied from an RF plasma source operating at 450 W. Growth temperatures were recorded both from thermocouple readings near the Ti-coated backside of the silica glass substrate carrier and from pyrometer readings in order to obtain as good as possible control over the substrate temperature. For the purpose of consistency, the growth temperatures stated hereafter refer to the pyrometer readings. The length/thickness for each segment/layer mentioned in the next paragraph are nominal values based on the ratio between the Al and Ga fluxes (see Table S1 in Supporting Information).

To start the nanocolumn growth, an Al seeding layer with Si atoms were deposited at 805 °C before the graphene substrate was exposed to N plasma. After that, the Si, Al, and N shutters were opened simultaneously to form an n-AlN buffer layer with a thickness of approximately 40 nm.<sup>25</sup> Afterward, a segment of about 140 nm<sup>25</sup> high n-GaN nanocolumn segments were formed at 895 °C, acting as a template for n-AlGaIn,<sup>39</sup> minimizing the chance of coalescence and/or quasi-film-like structures.<sup>40</sup> Subsequently, 550 nm long n-Al<sub>0.25</sub>Ga<sub>0.75</sub>N nanocolumn segments were grown at 915 °C, followed by an active region of 27 nm thick intrinsic GaN segment grown at 895 °C. Radial nanocolumn development is anticipated, increasing the chance of achieving champagne-glass structure for the following nanocolumn segments.<sup>39</sup> Using this method, one can increase the diameter of nanocolumns and thus coverage without introducing a higher Al flux.<sup>25</sup> Next, a 200 nm thick p-Al<sub>0.25</sub>Ga<sub>0.75</sub>N segment was grown at 695 °C, and finally, 20 nm thick p-GaN grown at 675 °C was used as a p-type contact layer. Each nanocolumn segment has its own distinctive growth condition with respect to Al, Ga, Si, and Mg beam equivalent pressures, N<sub>2</sub> flow rate and growth time, as summarized in Table S1 in the Supporting Information.

**Micro-Raman Measurements.** A Renishaw inVia Reflex system with a 100 mW 532 nm laser, a 50X confocal objective and a spectral resolution of less than 1 cm<sup>-1</sup> was used to map 40 × 40  $\mu\text{m}$  areas on the samples. Ten milliwatts laser power with a dwell time of 10 s was used for the acquisitions, and spectra shown in Figure 2a are averaged from 1600 individual measurements.

**SEM Imaging.** Secondary electron images were taken with a Hitachi SU8000 system at an acceleration voltage of 5 kV.

**TEM Imaging.** The cross-section TEM lamella was prepared by a FEI Helios G4 UX dual-beam FIB-SEM. Two protection layers of carbon, the first one made by e-beam-assisted deposition and the second by ion-beam-assisted deposition, were deposited on the surface of the selected area prior to milling. Coarse thinning was performed at 30 kV ion-beam acceleration voltage, while the final thinning was performed at 5 and finally 2 kV to minimize Ga implantation and surface amorphization.

TEM characterization was performed with a double Cs-corrected cold-FEG JEOL ARM 200CF, operated at 200 kV and equipped with a 100 mm<sup>2</sup> (0.98 sr solid angle) Centurio SDD for X-ray energy dispersive spectroscopy (EDS) and a Quantum ER GIF for electron energy loss spectroscopy

(EELS). In order to remove surficial hydrocarbons, the TEM lamella was gently plasma cleaned with a shielding holder  $2 \times 10$  s prior to TEM characterization. Simultaneous EDS and dual-EELS were performed in scanning TEM (STEM) mode for chemical compositional analysis.

**Electrical Measurements.** For van der Pauw measurements, Au contacts to graphene were made in the corners of a quadratic  $0.5 \times 0.5$  cm<sup>2</sup> sample. The voltage was measured on opposite sides of the bias current path for both polarities to find the corresponding resistance, giving a total of eight measurements. These values were then inserted into the van der Pauw formula and the equation was solved for  $R_s$  numerically. The current–voltage measurements were done on a two-probe station connected to a Keithley 2636A sourcemeter.

**Photoluminescence Measurements.** Continuous-wave (CW) excitation was achieved with a Kimmon Koha He–Cd laser operating at 325 nm. The excitation beam was focused on the sample using a 5 mm lens, achieving a spot size of  $\sim 0.42$  mm. The sample was placed inside a Cryo Industries closed-cycle liquid He microscopy cryostat system equipped with a sample heater and thermometer for precise sample temperature control. PL detection was achieved with an Andor Shamrock 303i imaging spectrograph, using a 600 lines/mm grating blazed at 500 nm, dispersing the signal onto an Andor Newton electron multiplying charge-coupled device (EMCCD).

**Electroluminescence Spectral Measurements.** For LED electroluminescence measurements, a StellarNet EPP2000 UV–vis (185 nm – 850 nm) compact spectrometer with a resolution between 0.4 nm (UV) and 0.25 nm (VIS), 2048 channels, was used with a UV-transparent fiber.

**Electroluminescence Integrating Sphere Measurements.** The integrating sphere measurement system consists of a 50 cm diameter integrating sphere (BaSO<sub>4</sub> coating) and a spectrometer consisting of a grating monochromator with step motor and photomultiplier tube. The optical resolution of the entire system is about 1.2 nm. According to the manufacturer, the minimum spectroradiometric accuracy of the system is  $\pm 1\%$  in the UVA and visible spectral region for each individual wavelength step. The LED sample is positioned in the center of the integrating sphere and contacted via contact probes. The LED is electrically driven and measured using a Keithley 2400 sourcemeter.

## ■ ASSOCIATED CONTENT

### ⑤ Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acs.nanolett.8b04607.

Illustrative growth design diagram and additional SEM image (S1); detailed growth information (Table S1); explanation for using low growth temperature during p-type doping of nanocolumn structure; TEM analysis (S2); Raman measurements (S3); IQE measurements (S4) (PDF)

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## Notes

The authors declare no competing financial interest.

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Supporting Information -  
GaN/AlGaN nanocolumn  
ultraviolet LED using  
double-layer graphene as  
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PAPER IV. GAN/ALGAN NANOCOLUMN ULTRAVIOLET LED USING  
DOUBLE-LAYER GRAPHENE AS SUBSTRATE AND TRANSPARENT  
ELECTRODE

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## Supporting Information

# GaN/AlGaN Nanocolumn Ultraviolet Light-Emitting Diode Using Double-Layer Graphene as Substrate and Transparent Electrode

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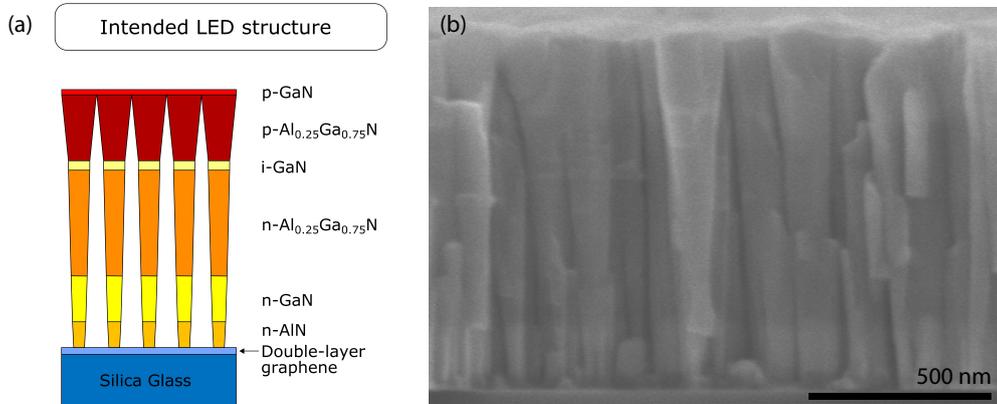
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## Illustrative diagram and additional SEM image



**Figure S1.** Nanocolumn design and SEM image of grown nanocolumns. (a) Schematic of the intended GaN/AlGa<sub>N</sub> nanocolumn device structure. (b) Side-view SEM image of self-assembled GaN/AlGa<sub>N</sub> nanocolumns grown on double-layer graphene transferred onto silica glass, where the nanocolumn dimensions are found to be ~1070, ~35 and ~220 nm for the length, bottom- and top-diameter, respectively.

## Growth information

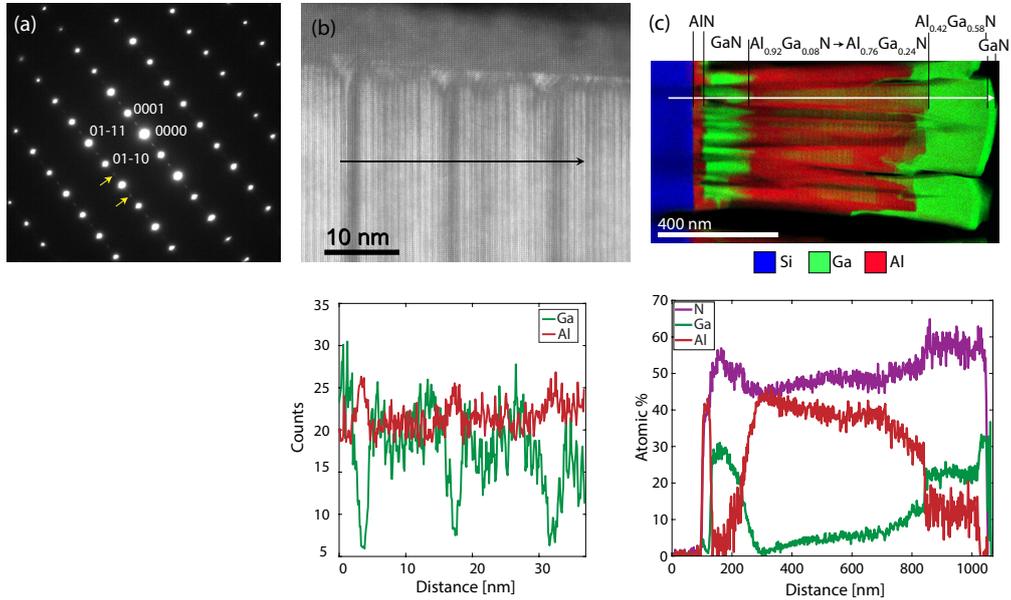
**Table S1.** Growth conditions of the GaN/AlGaN nanocolumns.

Nanocolumn segment/layer	Growth temperature, pyrometer reading (°C)	Beam equivalent pressure (Pa)			Si cell temperature (°C)	N <sub>2</sub> flow rate/plasma emission (sccm/mV)	Growth time (sec)
		Al	Ga	Mg			
Al seeding with Si	805	$8.0 \times 10^{-5}$	-	-	1050	-	35
Nitridation	805	-	-	-	-	2.00/10.13	60
n-AlN	805	$8.0 \times 10^{-5}$	-	-	1050	2.00/10.13	200
n-GaN	895	-	$2.5 \times 10^{-4}$	-	1050	2.75/10.08	600
n-Al <sub>0.25</sub> Ga <sub>0.75</sub> N	915	$6.7 \times 10^{-5}$	$2.0 \times 10^{-4}$	-	1050	1.00/8.715	3600
i-GaN	895	-	$2.5 \times 10^{-4}$	-	-	2.75/10.025	30
p-Al <sub>0.25</sub> Ga <sub>0.75</sub> N	695	$2.7 \times 10^{-5}$	$8.0 \times 10^{-5}$	$6.0 \times 10^{-6}$	-	2.00/10.075	1500
p-GaN	675	-	$8.0 \times 10^{-5}$	$6.0 \times 10^{-6}$	-	3.00/9.94	300

## Explanation for using low growth temperature during p-type doping of the nanocolumns

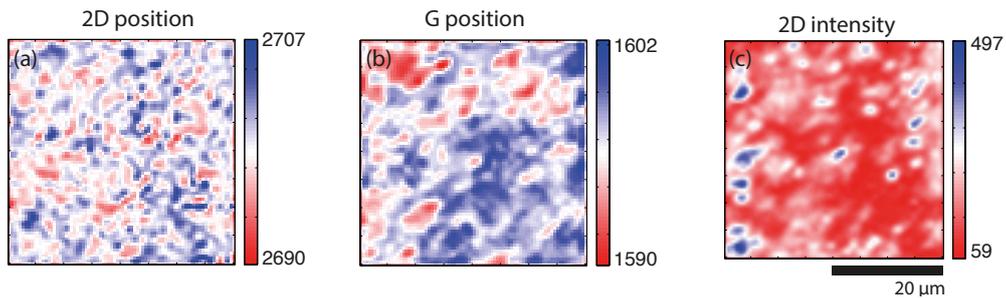
At a growth temperature slightly below 700°C, it is expected that Mg atoms are reasonably incorporated into the p-AlGa<sub>N</sub> and p-GaN layers<sup>1-3</sup>. If grown at a similar temperature as the n-AlGa<sub>N</sub> layers, the high vapor pressure of Mg could lead to a reduced Mg incorporation efficiency and an enhancement of Mg segregation<sup>4</sup>. However, further reduction of the growth temperature below 675 °C for the p-AlGa<sub>N</sub> and p-GaN layers may induce polarity inversion from Ga-polar to N-polar, leading to undesirable consequences such as a low Mg doping efficiency<sup>3,5</sup>, which is accompanied with highly resistive or semi-insulating behavior<sup>6</sup>. Another important parameter to control in order to improve the efficiency of the p-type doping is the flux of supplied Mg. In GaN thin films grown under extreme Ga-rich conditions, an excessive Mg flux has been found to induce polarity inversion from Ga-polar to N-polar<sup>7</sup>. An increase of the growth temperature avoids this inversion, however then the Mg flux needs to be increased to compensate the strong desorption rate<sup>1,2</sup>, suggesting that a balance between these two parameters has to be reached. This is further complicated by the very narrow Mg cell temperature window that can be used to achieve optimized nanocolumn growth<sup>2,8</sup>. For this work, the value of Mg flux being used is based on a previous study on GaN/AlGa<sub>N</sub>-based nanocolumn LEDs<sup>9</sup>.

## TEM analysis



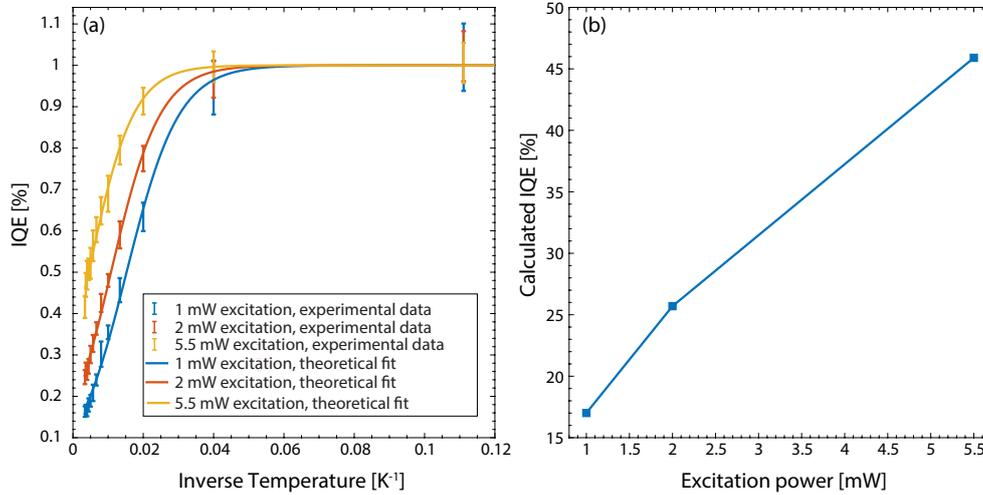
**Figure S2.** Transmission electron microscopy diffraction data and line scans. (a) Diffraction pattern taken from n-AlGa<sub>0.58</sub>N segment of nanocolumns shown in Figure 1c in the main text confirms that they grow along the hexagonal c-axis. Diffraction from the semi-periodic superlattice-like structure can also be observed in the pattern, as marked by yellow arrows. (b) HAADF STEM image and line scan across the superlattice-like structure in the n-AlGa<sub>0.58</sub>N segment. (c) Compositional nanocolumn EDS and EELS mapping presented together with its line scan in the bottom.

## Raman measurements



**Figure S3.** Micro-Raman maps of peak positions and intensities of the double-layer graphene after the GaN/AlGa<sub>0.58</sub>N nanocolumn growth. Maps taken from same area as shown in Figure 2 in the main text. (a, b) Peak positions of 2D- and G-peak. (c) 2D peak intensity.

## IQE measurements



**Figure S4.** Power and temperature dependence of the IQE. (a) Temperature dependence of the IQE for three different excitation powers. Experimental points correspond to the average integrated intensity of the main emission peak over ten randomly selected spots per temperature step, and error bars represent the standard deviation. Theoretical fits were obtained using the model equation  $I(T) = I(0)/(1+\alpha\exp(-E_a/kT))$ , with  $I(0)$ ,  $\alpha$  and  $E_a$  as fitting parameters. (b) Excitation power dependence of the IQE at room temperature.

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