A High-Voltage Cascode-Connected Three-Level Pulse-Generator for Bio-Medical Ultrasound Applications

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***Abstract*—This paper presents a high-voltage three-level pulse-generator circuit which reduces the driving requirement of the input signals. This is achieved by cascoding making it possible to use low-voltage input transistors. The reduced driving requirement of the input signals makes it possible to use simple two-component capacitive level-shifters. The circuit is implemented in a commercially available 180nm high-voltage CMOS process. Circuit functionality is verified by simulation on schematic and layout using high supply voltages of positive and negative 70V. Simulation results indicate a reduction in input gate-charge by a factor of about 28. Average power consumption of about 0.61mW and 0.44mW is observed for a three-level and a two level 4-period 5MHz pulse using a pulse-repetition frequency of 5kHz.**

I. Introduction

Converting electrical energy into acoustic energy is the crucial first step in ultrasound image formation. Exciting the transducer to produce the desired sound pressure level and pulse shape is important for the resulting image quality and is the responsibility of the pulse generator. This makes the design of pulse generators for ultrasound imaging an important task.

For imaging techniques that require a high channel count, like 3D imaging, integrating transmitter and receiver electronics into the probe is necessary [1].

Several challenges are associated with the design of ultrasound pulse generators. These range from the driving requirements of the input signals, to speed, power, and area limitations. In addition, ultrasound harmonic imaging puts requirements on the harmonic content of the transmitted pulse.

A number of integrated high-voltage ultrasound pulse-generators have been published over the last years. [2] reported on a three-level pulse generator for CMUT transducers, using latch based full-swing level-shifters. They also reported on the possibility of achieving higher efficiency by using multi-level pulsing with regulated supplies. [3] reported on a three-level pulse-generator circuit using low V_{GS} high-voltage MOSFET devices and capacitive latch-based level-shifters. [4] proposed a differential three-level pulse generator to drive a CMUT transducer. The design used pulse-triggered level-shifters as gate drivers for the high-voltage transistors in the pulse-generator. [5] proposed a three-level pulse-generator which was able to generate an output voltage nearly twice the supply voltage. It was implemented using simple two transistor level-shifters as gate-drivers for the high-side transistors. [6] reported on a three-level pulse generator for piezo transducers with slew-rate and amplitude control. They did not report any specifics on the level-shifters used. [7] and [8] reported prototype measurement results using the circuit from [3] for different voltage levels. Neither of the two papers gives any information about level-shifters and gate drivers used.

[2], [4], [5], and [6] use level-shifters as gate drivers, while [3], [7], and [8] use level-shifters and dedicated gate-drivers. The need for gate-drivers is due to the large input capacitance of the high-voltage MOSFET transistors. [2] - [8] deal with this problem using different circuits and techniques. This ranges from complex multi-device circuits like in [4] to simple two transistor level-shifters like in [5]. But they are all driving the gates of the high-voltage transistors with additional circuitry which may increase power, area, or both.

By contrast, this paper addresses the issue concerning the high input capacitance of the high-voltage transistors by using the well-known technique of cascoding. This makes it possible to drive the inputs of high-voltage transistors without additional circuitry. It shows that this reduces the driving requirement of the input signals which makes it possible to use simple and small two-component capacitive level-shifters. This paper proposes a high-voltage cascode-connected three-level pulse-generator circuit with simple two-component capacitive level-shifters. The circuit is implemented in a commercially available 180nm high-voltage CMOS process, and simulations indicate that the charge the signal is required to deliver in order to switch the circuit is reduced by a factor of about 28.

The paper is organized with an introduction in Section I. This is followed by design considerations and circuit details in Section II. The simulation results are presented in Section III followed by a discussion in Section IV. The paper ends with a conclusion in Section V.

II. Design Considerations

A. Pulse Generator

An ultrasound pulse-generator typically generates high-voltage square pulses from low-voltage control signals. The resulting pulses can be unipolar, bi-polar, or have a number of intermediate voltage levels. This paper describes the implementation of a three level pulse-generator. Fig.1a shows a

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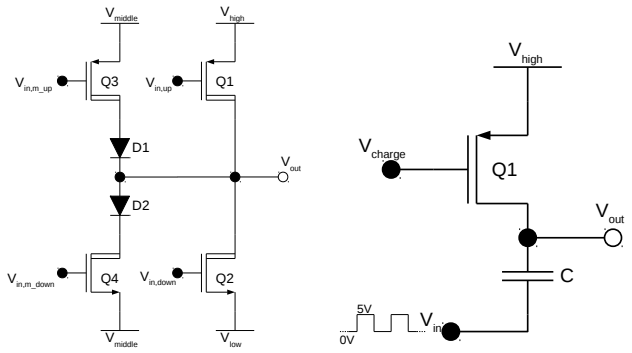
three-level pulse-generator implementation like the one used in [3] and similar to the one used in [6]. In this circuit all transistors are high-voltage devices with individual control signals. The high-voltage diodes, D1 and D2, protects transistors Q3 and Q4 by keeping their gate-drain voltage within safe limits.



(a) Three-Level Pulse-Generator (b) Level-up shifter

Fig. 1.

B. High-Voltage MOSFETs and Gate-Charge

In Fig.1a all the transistors are high-voltage devices. To achieve the high voltage blocking properties, high-voltage MOSFETs require a different device structure and are often large. This will add to the parasitics such as the gate-source and the gate-drain capacitance which may result in the need for a substantial gate current in order to switch a device fast. This puts high demands on the gate driver to deliver the current efficiently.

A measure of the amount of charge needed to switch a high-voltage MOSFET can be found from the gate-charge curve. This is useful since it can be used to calculate the gate current required to switch the device. In this paper, gate-charge curves were found by switching a MOSFET with a voltage across it from off to on. This was done with a constant drain current and a Norton equivalent driving the gate. The gate-charge was then calculated by the time integral of the gate-current.

C. Cascode

To reduce the driving requirement of the input signals, we use the well known technique of cascoding. This technique is well known in RF circuit-design to reduce the impact of the parasitic gate-drain capacitance of high-voltage MOSFETs. It has also previously been used in a discrete-component high-voltage pulse-generator circuit to reduce input capacitance and to achieve high transition speed [9]. Recent research [10], [11] indicates that using cascoding with discrete components in hard switching operation can even give a performance gain due to the efficient charging of the gate capacitance.

To utilize this technique, a low-voltage transistor is used as the input transistor with a high-voltage transistor placed in cascode. The cascode transistor is biased with a gate voltage that will turn it on when the input transistor is turned on. The low-voltage transistor will have lower gate capacitances than the high-voltage transistor, due to the smaller device size, and therefore the input capacitance of the circuit is reduced. The charge needed to drive the high-voltage MOSFET is efficiently delivered by the bias source and this eliminates the need for a dedicated gate driver. This reduces the driving requirement of the input signals, which makes it possible to use small and simple capacitive level-shifters as in Fig.1b.

By using this technique, we suggest a cascode-connected three-level pulse-generator using the capacitive level-shifters described in Section II-D. The suggested three-level pulse-generator with cascoding can be seen in Fig.2. The low-voltage input devices, Q1, Q6, Q7, and Q12, are protected from the high-voltage output by the high-voltage cascode devices, Q3, Q4, Q9, and Q10. Transistors Q2, Q5, Q8, and Q11 have been added to protect the input transistors by keeping their drain nodes at a fixed voltage when they are off. This works by turning the protection transistors on when the input transistors are off. These transistors also protect the gate-source junctions of the cascode transistors. From Fig.2 it can be seen that no additional control signal is needed since the protection transistors can be driven by the same signal as the input. The high-voltage diodes D1 and D2 have the same function as described in Section II-A for Fig.1a.

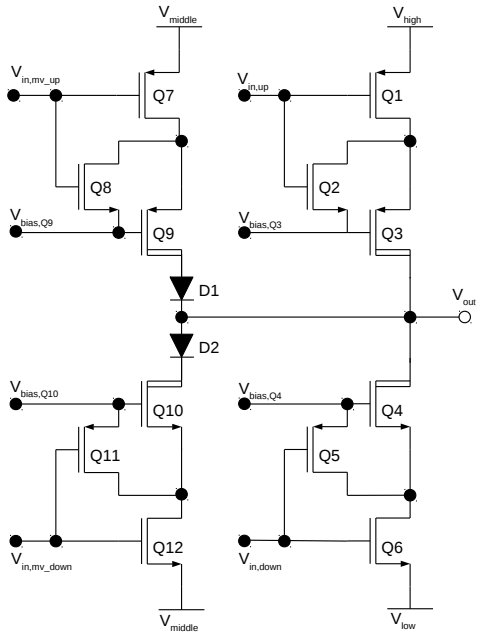


Fig. 2. Cascode-Connected Three-Level Pulse-Generator.

D. Level-Shifters

In this work we have investigated the use of simple two-component level-shifters. The level-shifters are made up of a low-voltage MOSFET and a high-voltage capacitor as can be seen in Fig.1b for the level-up shifter. The level-down shifter uses a NMOS transistor with the source terminal connected to the low supply voltage instead of a PMOS.

The level-shifters works by charging the output node to the supply voltage through the transistor by switching it on. Then

the transistor is switched off before applying a low-voltage digital signal to the input, V_{in}. The capacitive coupling will make the voltage change on the output equal to the voltage change on the input. The output node of the level-shifter, V_{out}, does not need to be recharged to the supply voltage very often, and an ultrasound pulse can be transmitted without recharging. The V_{charge} control signal from Fig.1b may be generated by a static level-shifter, like those used in [5], and shared by multiple channels. How often recharging is needed would be determined by the capacitor self-discharge rate, the pulse-repetition frequency, and the transistor leakage.

E. Output Stage

To drive the load, a simple class B power amplifier connected as a source follower was chosen. This was also done for the pulse generator in [6]. Due to the low gate-source voltage rating of 5V, careful design is necessary to keep the circuit within the rating.

F. Simulation

The voltage levels used for design and simulation in this paper are a high positive supply voltage of 70V, a middle supply connected to ground, and a high negative supply voltage of -70V. The control signals are low-voltage digital signals with high and low values of 5V and 0V respectively. The circuit requires four bias voltages for the cascode transistors. Referring to Fig.2 these are, $V_{bias,Q3}$ = 65V, $V_{bias,Q4}$ = -65V, $V_{bias,Q9}$ = -5V, and $V_{bias,Q10}$ = 5V.

The pulse generator is designed to drive a piezo element which is mainly a capacitive load. A model of such an element has been used as a load for the simulation results presented in this paper. The simulations were done using low-voltage digital input signals to generate a 5MHz three-level output signal with an amplitude of about 69V, and a 5MHz two-level output signal with an amplitude of about 70V.

III. Results

A. Gate Charge

Fig.3 shows the gate and drain voltages when switching a minimum size high-voltage NMOS transistor, and a NMOS cascode connection sized as in the three-level pulser. The NMOS cascode connection is the same as the connection of Q4, Q5, and Q6 in Fig.2. Referring to Fig.3, the gate-voltage of the cascode-connection is the gate-voltage of the low-voltage input transistor, and the drain-voltage is the drain-voltage of the high-voltage cascode transistor.

Fig.4 shows the gate-charge curves for switching the single minimum size high-voltage NMOS, and for switching the NMOS cascode connection. The gate-charge curve for the NMOS cascode connection is for the input of the cascode connection, which is the gate of the low-voltage input transistor.

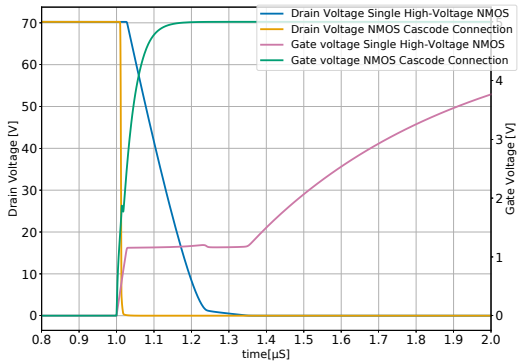


Fig. 3. Gate and drain voltage of a single high-voltage NMOS and NMOS transistors in cascode connection when switching.

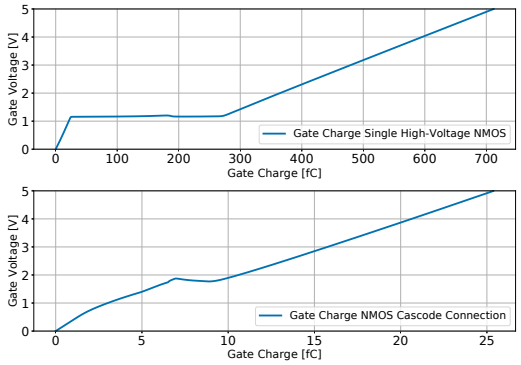


Fig. 4. Gate-charge curve for the single minimum size high-voltage NMOS, and the NMOS cascode connection.

B. Pulse Generation

For simulation, two pulses were generated. A three-level 5MHz pulse, and a two-level 5MHz pulse. The pulse length of both pulses is 4 periods. Fig.5 shows the pulses generated from post-layout simulations. The figure shows that the generated three-level pulse has an output voltage of about $138V_{peak\text{-}peak}$, and that the two-level pulse has an output voltage of $140V_{peak\text{-}peak}$. It also shows that the three-level pulse does not have accurate 0V levels.

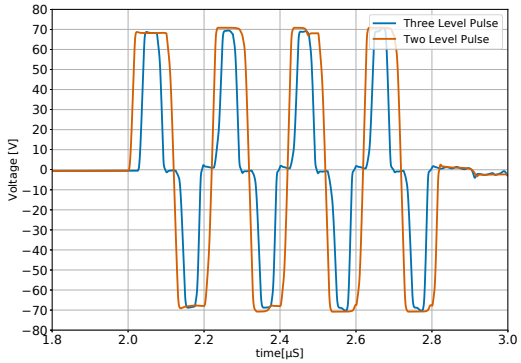


Fig. 5. Output of the pulse-generator for two different 5MHz pulses.

C. Power, Area, and Harmonics

The average power and second harmonic level estimated from simulations are presented in Table I for the typical corner. The average power results assumes a pulse-repetition frequency of 5kHz. The second harmonic level is found to be sensitive to process variation with this circuit. The variation across corners is about 20dB for the three-level pulse, and about 10dB for the two-level pulse.

TABLE I
POWER CONSUMPTION AND SECOND HARMONIC LEVEL FROM POST-LAYOUT SIMULATIONS IN THE TYPICAL CORNER

	Power [mW]	**HD2 [dBc]**
Three-Level Pulse	0.61*	-37
Two-Level Pulse	0.44*	-33

* Pulse-repetition frequency = 5kHz

The layout of the three-level pulse-generator is shown in Fig.6. The layout area is 0.0246 mm^2. The capacitors of the level-shifters can be made small, and is comparable to the size of a minimum size high-voltage transistor in this process.

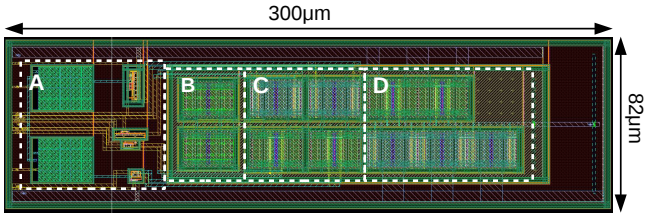


Fig. 6. Layout of the three-level pulse-generator. Referring to Fig.2, Area A is the level-shifters and low-voltage transistors. Area B is the diodes D1 and D2. Area C is the cascode transistors, and Area D is the output stage.

IV. DISCUSSION

In Fig.2 the input transistors are protected from excessive drain-source voltage by the transistors placed between the source and gate of the associated high-voltage transistor. This protection transistor also protects the gate-source junction of the high-voltage transistor. It is possible to omit this protection transistor by scaling the input and high-voltage cascode transistors. But scaling increases area and it was found that a better solution for this application was to implement the protection transistors and have minimum size high-voltage cascode transistors. The input transistors Q1, Q6, Q7, and Q12, were scaled to drive the output stage. The devices of the output stage were scaled to drive the load.

Comparing the voltages in Fig.3 we observe the cascode connection switches faster than the single high-voltage device. That the cascode connection reduces the input capacitance is confirmed by comparing the gate-charge in Fig.4. The gate-charge required to switch the cascode connection is about 28 times smaller than the charge required to switch the single minimum size high-voltage NMOS. This confirms the effectiveness of using cascoding to reduce input capacitance and, consequently, in reducing the driving requirement of the input signals.

Fig.5 shows the output waveform of the pulse-generator for two different 4-period 5MHz pulses. It is observed that the protection diodes, D1 and D2 from Fig.2, keep the output of the pulse-generator from reaching 0V. This is propagated to the output stage and is an imperfection in the output waveform. In this work we did not try to eliminate this effect.

The power consumption is difficult to compare with other papers since the load, frequency, and voltage varies between papers. The same holds for area. But area and power may be saved in this implementation. First, the gate-charge needed by the high-voltage transistors in Fig.2 is effectively delivered by the bias sources. Since we do not have any dedicated driver circuit for these transistors, we do not have any loss associated with this. Second, the capacitive level-shifters are efficient since we are able to use the same charge for the entire pulse. Third, we also save area compared to other implementations since we do not need any high-voltage transistors in the level-shifters. The capacitors in the level-shifters are also small due to the reduced input capacitance. [5] used simple two-transistor level-shifters that could have had comparable area, but the static power consumption made it unsuitable for this implementation.

V. CONCLUSION

In this paper we have showed that, by using cascoding in a three-level pulse-generator, we reduce the driving requirements of the input signals making it possible to use simple capacitive level-shifters. The reduction in input gate-charge was found to be a factor of about 28. The high-voltage cascode transistors are drawing the required gate-charge directly from the bias sources eliminating the need for dedicated gate drivers. A transistor between the drain node of the input transistor and the associated bias source protects the input transistor and the gate-source junction of the high-voltage cascode transistor when they are off. This protection circuit also reduces the sizing requirements of the input and cascode transistors making it possible to use smaller high-voltage devices. All high-voltage cascode devices in this paper have minimum size.

The pulse-generator was simulated after layout generating a three-level and a two-level 4-period 5MHz square-wave driving a model of a piezo element for ultrasound generation. Using supply voltages of ±70V, the circuit showed an average power consumption of about 0.61mW when generating a three-level pulse, and 0.44mW when generating a two-level pulse using a pulse-repetition frequency of 5kHz.

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