# Nwise: an Area Efficient and Highly Reliable Radiation Hardened Memory Cell Designed for Space Applications

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***Abstract*—In the electronics space industry, memory cells are one of the main concerns, especially in term of reliability, since radiation particles may hit cell nodes and disturb the state of the cell, possibly causing fatal errors. In this paper we propose the Nwise SRAM cell, an area-efficient and highly reliable radiation hardened memory cell for use in high-density memories for space applications. Simulations confirm that the proposed Nwise cell is fully tolerant to single event upsets (SEU) in any one of its nodes regardless of upset polarity. Meanwhile, compared with the RHBD-10T cell, the latest area-efficient radiation hardened memory cell, it has higher robustness: the minimum critical charge of Nwise is 4.1× higher than the minimum critical charge of the RHBD-10T cell. It also shows 23% and 12% improvements in read and write static noise margin (SNM). Furthermore, compared with RHBD-10T, up to 18.4% and 7.0% power savings are obtainable during write and read operations respectively. Nwise is about 2.28× faster than RHBD-10T during the more frequent read operation, with a similar penalty in write time. Finally, Nwise is the first proposed high density and reliable radiation hardened memory cell that has been designed using the 28nm FD-SOI technology node.**

***Index Terms*—space applications, radiation hardening, single event upset (SEU), multiple event upset (MEU), SRAM design, 28nm FD-SOI, reliability, soft errors, Nwise cell**

## I. Introduction

SRAM cells are extensively used to design cache memories in digital processing systems, occupying a large part of the processors [1]. Hence, they play a key role in determining the performance and power consumption of the systems. In electronics space industry, having robust SRAM cell designs are an equally important key factor, since the systems stay exposed to high doses of radiation strikes for a long time with a limited energy budget [2].

If a radiation strike hits the SRAM cell node and changes the stored data of the SRAM, a single event upset (SEU) occurs [2] that leads to system function disorder that may cause serious or even fatal errors. Therefore, it is essential to design SRAM cells with the ability of SEU effects mitigation [2], or phrased differently, with higher tolerance capability. Several solutions have been proposed focusing on different aspects at both the architecture and circuit level to mitigate SEU effects in memory designs [2] ... [14]. In this paper, we concentrate on circuit level techniques and propose the Nwise cell that improves power and area efficiency as well as reliability compared with the latest area-efficient radiation hardened memory cells.

Although technology scaling that commensurate with Moore's law considerably improves the computing technology [15], it has resulted in several unwanted consequences. For instance, it exacerbates radiation effects on SRAM cells since transistors are more prone to SEUs in lower supply voltages and smaller feature sizes [2]. This motivates researchers to explore alternative solutions to maintain the ability of further scaling.

The Fully Depleted Silicon On Isolator (FD-SOI) technology has been suggested as a promising candidate providing attractive characteristics, such as power consumption reduction and reliability improvement compared with corresponding circuits designed with Bulk CMOS technology. FD-SOI is a planar process technology that incorporates an ultra-thin layer of insulator (a buried oxide) within the substrate to dramatically reduce the leakage current. This also lowers the parasitic capacitance between the source and the drain, hence, improves transistor electrostatic characteristics, which causes better mobility and less variability and enhances the performance of FD-SOI circuits. Furthermore, the transistor channel that is implemented by a very thin silicon film makes the transistor fully depleted without any channel doping requirement [16], [17]. These valuable properties make FD-SOI an appealing technology for integrated circuits fabrication [18]. Therefore, in this paper, we leverage 28nm FD-SOI technology to design the Nwise cell.

To show the effectiveness of our design, the Nwise cell and three previously offered radiation hardened cells are simulated and compared with each other in this paper. The simulations are done with Cadence Spectre at nominal voltage level and temperature (1V and 27°C). The contributions of the paper are as follows:

1- Compared with the most area efficient and state of the art radiation hardened SRAM cell, our proposed Nwise cell

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has lower power consumption, higher robustness, and higher read and write static noise margin (SNM).

2- Compared with the most area efficient and state of the art radiation hardened SRAM cell, the Nwise cell has higher read speed, which make it an appealing candidate to implement in cache memories of processors.

3- Compared with other SRAM cells that are insensitive to the upset polarity, Nwise is more area efficient and has a higher level of robustness.

4- To the best of our knowledge, it is the first area efficient hardened SRAM cell that has been designed with FD-SOI 28nm technology.

The rest of the paper is organized as follows: In Section II, we review recent robust memory designs. In Section III, we propose our Nwise memory cell design and explain its schematic and operational behavior. Also, we analyze the SEU robustness of the proposed cell. In Section IV, we analyze and compare the robustness as well as cell costs including access times, power consumptions and SNM of the Nwise cell with the recent SRAM cells. Finally, Section V concludes this paper.

## II. REVIEW: PREVIOUS RADIATION HARDENED MEMORY CELL DESIGNS

To provide fault tolerant protection, conventional techniques such as Error Correction Coding (ECC) [4], Dual Modular Redundancy (DMR) [5] and Triple Modular Redundancy (TMR) [6] are employed at the architectural level to mitigate the SEU issues in memory blocks. However, even though minimum sized (6T) memory cells can be used, these techniques cause high area overhead and power consumption as well as increased delay and added complexity to the system [7].

On the other hand, circuit-level techniques to enhance the immunity add to the size of individual memory cells but avoid the architectural overhead. This make them more effective in reduction of area overhead and delay as well as power consumption. The Dual Interlocked storage CEll known as DICE is a 12T cell and one of the well-known hardening design approaches widely used in latch, flip-flop and memory designs thanks to its full tolerant capability to SEU [8]. Although using dual node feedback control provides full SEU immunity, its high area overhead restricts the applicability where area efficiency is essential [2].

Authors in [9] proposed a 10T hardened SRAM cell named Quatro-10T. As an alternative to DICE, it is more area efficient and more reliable in low voltage applications with larger noise margin and less leakage current [9]. It uses negative internal feedbacks to improve the immunity of the cell nodes against SEUs. However, Quatro-10T cannot provide full immunity to all SEUs and some internal nodes may flip during $0 \rightarrow 1$ SEU [2], [10].

Using circuit-level hardening techniques, a new RHBD-10T memory cell is proposed with low area overhead compared to previous radiation hardened memory cells [10]. However, it is shown that the proposed 10T cell suffered from high read access time that may affect its application wherever high speed is indispensable [10], [3]. Furthermore, even if providing SEU tolerance regardless of the upset polarity, the tolerance capability is not high compared to previously proposed cells [3].

Two robust single-ended hardened SRAM cell, the 13T and 11T cells, are proposed in [11] and [12], respectively. Both 13T and 11T designs deploy a similar technique to improve the reliability: using a refreshing mechanism and periodically cutting off the loop paths to block the particle strike effects. However, the required peripheral circuitry has high area overhead and longer operation time due to extra transistors in the refreshing mechanism. Meanwhile, they require more power consumption compared with recent smaller designs.

A memory cell proposed in [13], RHD12T, improves robustness against SEU by deploying circuit level hardening techniques together with layout-level approaches. However, this memory cell suffers from high area overhead and power consumption. Finally, two 18T and 24T cells have been proposed in [14] that provide complete tolerance against SEUs but at the cost of considerable increase in area overhead (composed of $1.8\times$ and $2.4\times$ more transistors compared with Nwise).

## III. PROPOSED NWISE MEMORY CELL DESIGN

### A. Nwise Cell Schematic

Figure 1 shows the circuit structure of our proposed Nwise cell. The access transistors, NMOS pass gates N7 and N8, which are controlled by the word line (WL), connect the bit-lines (BL and BLB) to the main storage nodes Q and QB, respectively. Furthermore, two cross-coupled NMOS transistor pairs, N1-N2 and N5-N6, shape two data latches where one creates data redundancy for the other. Therefore, the Nwise cell has four storage nodes Q, QB, P, and PB, where P and PB provide the redundant stored data for Q and QB. Inspired from the RHBD-10T cell design [10], the circuit is equipped with two feedback paths, P1-N4 and P2-N3 that help storage nodes recover to their initial value after particle strikes and provide enough robustness under high-radiation conditions. However, we apply both NMOS and PMOS transistors in the Nwise feedbacks to enhance the read operation speed , and use a different transistor interconnection structure for increased tolerance capability.

### B. Operation Analysis

Figure 2 shows the circuit structure of a one-column set consisting of 64 Nwise cells and associated peripheral circuitry including a precharge circuit, a write circuit, and an output sense amplifier [19], [20]. Here we demonstrate how a cell located in this column set operates, both through text and simulation results. We will come back to the simulation setup in Section IV.

In the hold mode, the logic state of WL is set to 0 and thus N7 and N8 are OFF. Let us assume that the memory is in state 1 (i.e., Q = 1, QB= 0, PB = 0, and P = 1, see Figure 1). Thus, transistors N2, N4, N6, and P2 are ON, and the others are

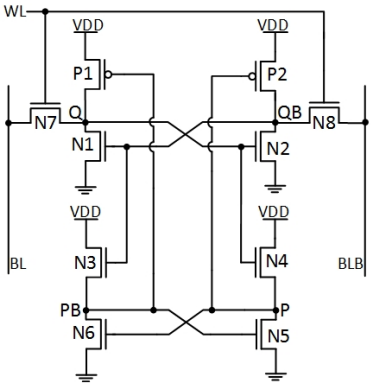


Fig. 1: The circuit structure of the proposed Nwise cell.

OFF. Hence, the proposed cell can maintain its initial stored state.

Figure 3 depicts transient simulation results of a cell located in this column set for a sequence of operations "Write 0, Read 0, Write 1, Read 1". It demonstrates that the write and read operations can be accomplished successfully. To write data 0 into the Nwise cell, BL and BLB are set to 0 and VDD respectively. Afterwards, when WL is changed to VDD, Q is discharged to 0, and QB is charged to VDD. Therefore, transistors N1, N3, N5, and P1 become ON, and transistors N2, N4, N6, and P2 become OFF, so that the logical value of the cell is correctly changed to state 0. Then, once WL is pulled back to 0, the write operation is completed successfully. Since the Nwise cell has a symmetrical structure, similar explanations are given for write data 1 into the cell (nodes and transistors are replaced by their symmetric pairs in the above description).

Before executing a read operation, BL and BLB are precharged to VDD by activating the precharge circuit. Once WL is set to VDD, the read operation begins. Thus, the two access transistors N7 and N8 are turned on. Nodes Q, QB, P, and PB keep their initial value, e.g., Q = P = 1 and QB = PB = 0 for a Read 1 operation. Hence, the voltage of BL remains unchanged while BLB is discharged through transistor N2 since N2 is ON and creates a path from BLB to GND. Hereafter, the voltage difference between BL and BLB is recognized and amplified by the differential sense amplifier connected with them, and thus, the state of the stored data is output. After the read operation is completed, and WL is set to 0, the storage nodes (Q, QB, P, and PB) still maintain their stored values. Since the Nwise cell has a symmetrical structure, similar explanations are given for read data 0 from the cell (nodes and transistors are replaced by their symmetric pairs in the above description).

### C. SEU Recovery Analysis

Here, the SEU robustness of the proposed cell is analyzed, both through text and simulation as depicted in Figure 4. We will come back to the simulation setup in Section IV. When an energetic particle passes through a semiconductor device, electron-hole pairs are created along its path as it loses

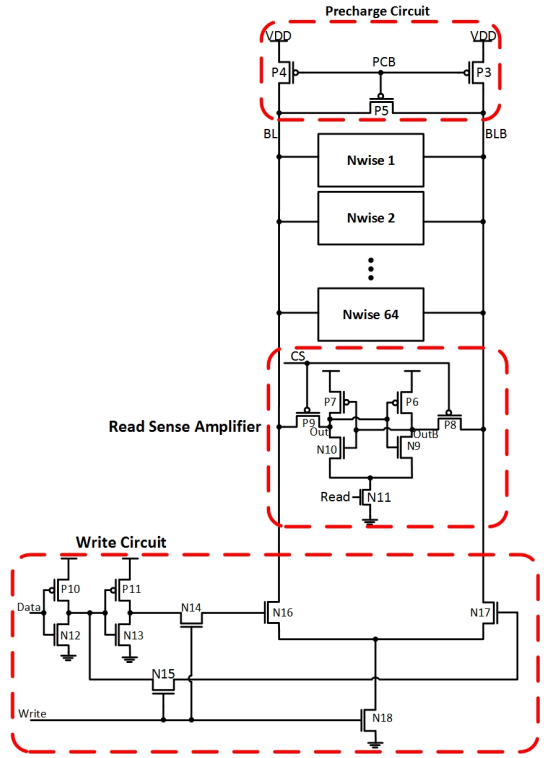


Fig. 2: The structure of a one-column set that containing 64 Nwise cells, a precharge circuit, a write circuit, and an output sense amplifier.

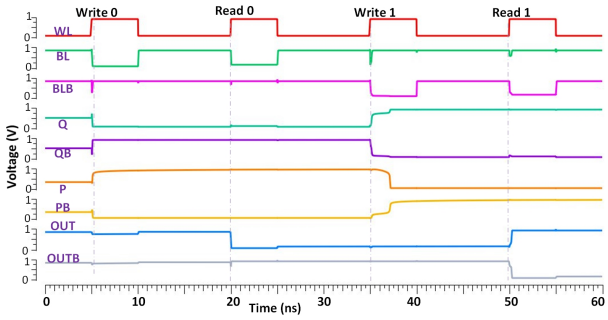


Fig. 3: The simulation waveform of Nwise cell for a sequential set of operations Write 0, Read 0, Write 1, Read 1.

energy [21], [22], [23]. If such an energetic particle hits a reverse-biased junction depletion region, the injected charge is transported by drift current and leads to an accumulation of extra charge at the node [21]. This causes a transient current pulse that changes the value of the node when the injected charge exceeds the critical charge collected in the node (Qcrit) [23], [21]. Therefore, sensitive nodes of the cell are the nodes surrounded by the reverse-biased drain junction of transistor(s) biased in the OFF state [24]. Hence, when a radiation particle strikes a PMOS transistor, only a positive transient pulse (0→1 or 1→1) can be generated, while, when a radiation particle strikes an NMOS transistor, only a negative transient pulse (1→0 or 0→0) can be induced [24]. Let us assume that the Nwise cell is in state 1, where Q = 1, QB = 0, PB = 0, and P = 1. Thus, transistors N2, N4, N6, and P1 are ON, and the

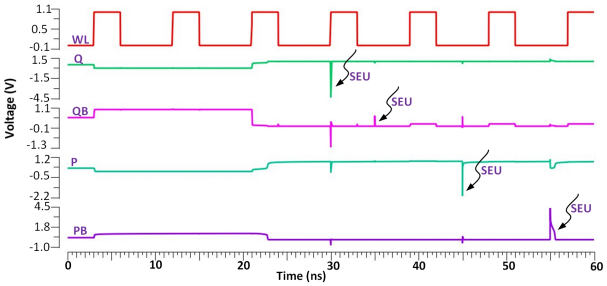


Fig. 4: SEU tolerance simulation of Nwise cell.

others are OFF. Therefore, at the given state of the cell, Q, QB, and P are sensitive nodes while PB is not sensitive to the particle strike.

(1) If Q is flipped to state 0 by a charged particle strike (Q: 1→0), transistors N2 and N4 become temporarily OFF, hence, P and QB will become floated. Therefore, their 1 and 0 state will be kept since the high impedance state does not have effect on the state of the node [3]. Hence, transistor N1 remains OFF. Meanwhile, the state of node PB remains unchanged (0). Controlled by PB, transistor P1 remains ON and eventually recovers the state of node Q through the pull-up path.

2) If QB is flipped to state 1 by a charged particle strike (QB: 0→1), node P keeps its state, thus, transistor P2 remains OFF. Consequently, there is not any ON path connected to VDD to keep the high state of QB. On the other hand, transistor N2 is already ON hence node QB discharges through the ON path of N2 to its initial state.

3) If P is flipped to state 0 by a charged particle strike (P: 1→0), transistors N6 and P2 are turned off and on, respectively. Consequently, node PB becomes floated and its state is not changed. Consequently, transistor P1 stays ON; hence, node Q stays unchanged and keeps transistor N4 and N2 ON pulling node P up to its initial state through ON transistor N4.

In part, the recovery described above requires careful sizing of the transistors. We will come back to this in Section IV. Since the Nwise cell has a symmetrical structure, similar recovery behavior is seen for state 0 of the cell (nodes and transistors are replaced by their symmetric pairs in the above description). This shows that the Nwise cell can recover the flipped storage nodes irrespectively of the upset polarity.

## IV. Design Methodology and Simulation Results

To show the effectiveness of our design, we compare the Nwise cell with three previously published radiation hardened cells mentioned in Section II: DICE is a popular radiation hardened cell consisting of 12 transistors, Quatro-10T is an area-efficient well-known radiation hardened cell, and finally RHBD-10T is a recently proposed area-efficient radiation hardened cell.

As depicted in Figure 2, the circuit structure of a one-column set consists of 64 SRAM cells, and associated peripheral circuitry. For Nwise as well as other three selected SRAM cells, this column-set is designed and simulated. The high-level structure is a column in a cache memory as proposed and described in [19], [20]. Necessary signal drivers and wire capacitances are added to the bitlines (BL and BLB) and wordlines (WL) based on the SRAM layout sizes drawn in [21], [25], [7], [3]. Since these are the same for all four cells structures, the comparison between the cells are just. Transistor sizes of the peripheral circuitry as well as SRAM cells are optimized to get the maximum robustness as well as minimum read/write power consumption, minimum read/write access times, and minimum area. However, robustness has been given higher weight when the optimization goals have been conflicting. We use standard manual optimization, tuning transistor sizes to find a global optimized solution. The same time has been spent on optimization for all four memory cell structures. The simulations are done with Cadence Spectre at nominal voltage level and temperature (1V and 27°C). All the SRAM cells are designed with a commercially available 28 nm FD-SOI technology. Experiments with layout and process variations are left for future work.

From the simulations, we find read and write power consumptions, read and write access times, Qcrit, and three different static noise margins (Hold, Write and Read SNMs, i.e. HSNM, WSNM, and RSNM). SNMs express the voltage immunity of the memories during read, write, and hold operations, and they are calculated based on information found in [26].

To simulate the effects of a particle strike in Cadence Spectre, an exponential current pulse is injected into the sensitive nodes Q, QB, P, respectively. For this injection we employ a double exponential current model given in Equation 1 proposed in [27], and widely used by researchers for instance in [12], [3].

$$I(t) = \frac{Q_{dep}}{\tau_f - \tau_r}(e^{\frac{-t}{\tau_f}} - e^{\frac{-t}{\tau_r}}) \quad (1)$$

$Q_{dep}$ is the total charge deposited at the node hit by the particle strike. $\tau_r$ is the collection time constant of the junction and $\tau_f$ is the ion-track establishing time constant. Both are material dependent time constants [27]. According to [28], we set $\tau_r = 1ps$ and $\tau_f = 5ps$ for the considered 28nm FD-SOI technology node. The critical charge ($Q_{crit}$) is obtained by increasing $Q_{dep}$ until the state of a sensitive node is changed. The cell $Q_{crit}$ is the minimum $Q_{crit}$ among all sensitive nodes of the cell. The higher the $Q_{crit}$ is, the lower the probability of the cell being flipped by an SEU is. Hence, a cell with higher $Q_{crit}$ have higher SEU tolerance [3].

### A. SEU Recovery Simulation

In the simulations depicted in Figure 4, SEU fault injections happen at 12ns, 15ns, and 43ns, respectively. At 12ns, a 0→1 transient fault occurs at node Q. We see from the simulations that node Q recovers to its initial state, and followed by Q, two other nodes, QB and P, return to their initial state. At 15ns, a 0→1 transient fault occurs at node QB. Again, the internal nodes of the Nwise cell recover their initial state after

TABLE I: COST COMPARISON OF FOUR CONSIDERED RADIATION HARDENED CELLS.

| Cell Type | # of Transistors | Write Power | Read Power | Read Access Time | Write Access Time | HSNM | WSNM | RSNM | Qcrit (fC) | Full SEU Immunity? |
|---|---|---|---|---|---|---|---|---|---|---|
| Nwise | 10 | 25.6uW | 13.1uW | 0.227ns | 0.173ns | 380mV | 530mV | 210mV | 0.98 | Yes |
| RHBD | 10 | 31.4uW | 14.1uW | 0.518ns | 0.075ns | 400mV | 470mV | 170mV | 0.24 | Yes |
| Quatro | 10 | 13.3uW | 13.1uW | 0.200ns | 0.054ns | 370mV | 260mV | 175mV | 0.87 | No |
| DICE | 12 | 14.1uW | 13.0uW | 0.133ns | 0.161ns | 220mV | 570mV | 200mV | 1 | Yes |

the injected fault. Finally, at 43ns, a transient 0→1 fault hits node P. Again, P comes back its initial state, followed by the other internal nodes.

The Qcrit for all four considered cells are reported in Table I. DICE has the highest critical charge, however, with higher area overhead. This confirms that it is not a proper choice where area efficiency is required. Quatro has almost as high Qcrit as Nwise, but as described in Section II, it cannot provide full tolerance against SEUs. It is therefore not a suitable choice for harsh environments. Nwise has four times higher critical charge compared with RHDB, the other 10T counterpart that also provides full SEU tolerance against any single node upset.

Compared with Bulk technology, the critical charge is lower in circuits designed with FD-SOI. This is because the FD-SOI technology has a very thin body, source and drain, which decreases the collected charge. However, in this paper, all the compared cells are designed and simulated with 28nm FD-SOI so comparisons are correct. The proposed Nwise cell characteristics are, however, not dependent on the used technology and they can be achieved with Bulk technology as well.

### *B. Cost Comparative Analyses: comparison of cell area and access times, power consumptions and static noise margins*

Table I shows the full performance comparison of the proposed Nwise cell with previous radiation hardened cells, DICE, Quatro-10T, and RHBD-10T. The comparisons include the power consumptions during read and write operations, read access times, write access times, and different static noise margins (HSNM, WSNM, and RSNM).

The Nwise cell has 18.4% and 7.0% improvement in write and read power consumptions compared with RHBD-10T. Moreover, the Nwise cell has 12% and 23% improvement in WSNM and RSNM respectively while the HSNM is 5% lower compared with RHBD-10T. Similar trends to our reported cost values have been reported for the DICE, Quatro and RHBD-10T cells in previous articles [3], [7], [10], [21].

Furthermore, Table I shows that the Nwise cell has a read time that is 43.8% of RHBD-10T read time. This happens since more PMOS transistors are ON during a read in RHBD-10T. On the other hand, the Nwise cell is 43.3% slower than RHBD-10T during write operation. This is because the N2 and N4 transistors that have been added to the feedback paths to enhance the robustness of the cell increase the driving loads in Q and QB, thus making the write operation slower. However, in typical applications, the number of read operations is considerably higher than the number of writes [29], [30], which alleviates the effect of slow writing and confirms the usefulness of the Nwise cell in cache circuits designs. There is also a much better balance between the read and write delays in Nwise compared to RHDB-10T.

## V. Conclusions

In this paper we propose the Nwise cell, the first area efficient and highly reliable radiation hardened memory cell that has been designed with 28nm FD-SOI technology. Simulations show that Nwise provides full tolerance to SEUs in any one of its single nodes irrespective of the upset polarity. Compared with the RHBD-10T cell, the latest area-efficient radiation hardened memory cell, the Nwise cell has higher robustness, less power consumption during read and write operations, higher RSNM and WSNM, and finally lower read operation time. These factors make the Nwise cell a promising candidate for highly reliable, area and power efficient space applications.

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