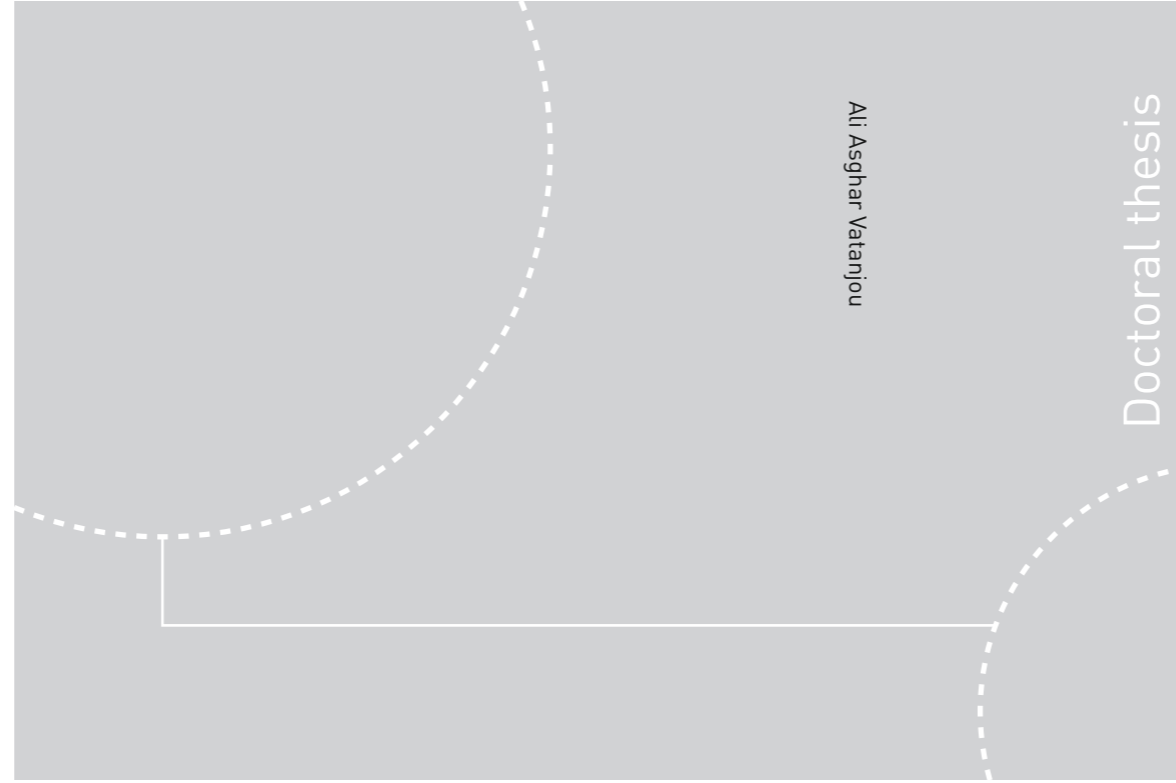


ISBN 978-82-326-4322-6 (printed ver.)  
ISBN 978-82-326-4323-3 (electronic ver.)  
ISSN 1503-8181



Doctoral theses at NTNU, 2019:362

Ali Asghar Vatanjou

# Ultra Low-Power/Low-Energy CMOS Mixed-Signal Building Blocks

Doctoral theses at NTNU, 2019:362

**NTNU**  
Norwegian University of Science and  
Technology Thesis for the Degree of  
Philosophiae Doctor  
Faculty of Information Technology and  
Electrical Engineering  
Department of Electronic Systems

 **NTNU**  
Norwegian University of  
Science and Technology

 **NTNU**  
Norwegian University of  
Science and Technology

 NTNU

Ali Asghar Vatanjou

# Ultra Low-Power/Low-Energy CMOS Mixed-Signal Building Blocks

Thesis for the Degree of Philosophiae Doctor

Trondheim, December 2019

Norwegian University of Science and Technology  
Faculty of Information Technology and Electrical Engineering  
Department of Electronic Systems

 **NTNU**  
Norwegian University of  
Science and Technology

**NTNU**

Norwegian University of Science and Technology

Thesis for the Degree of Philosophiae Doctor

Faculty of Information Technology and Electrical Engineering  
Department of Electronic Systems

© Ali Asghar Vatanjou

ISBN 978-82-326-4322-6 (printed ver.)  
ISBN 978-82-326-4323-3 (electronic ver.)  
ISSN 1503-8181

Doctoral theses at NTNU, 2019:362

Printed by NTNU Grafisk senter

## ACKNOWLEDGEMENTS

This thesis is submitted to Department of Electronic Systems, Faculty of Information Technology and Electrical Engineering at Norwegian University of Science and Technology as a part of the requirements for fulfilling the Degree of Doctor of Philosophy.

First, I would like to thank my main supervisor professor Snorre Aunet and my co-supervisor professor Trond Ytterdal for their guidance and support during my PhD studies. Thanks also to Norwegian Nano-Network for funding chip fabrications. Thanks to my colleague at NTNU Even Låte for his collaboration in my publications and his friendship. I wish to acknowledge Jonathan Edvard Bjerkedok for the collaboration we had in the first publication for this PhD work.

I would like to thank my family specially my wife Mahsa and my parents for their unlimited support and encouragement during my work towards this PhD.





## CONTENTS

1. <i>Introduction</i> . . . . .	3
1.1 CMOS circuits operation in subthreshold . . . . .	3
1.2 Motivation for ultra-low voltage CMOS circuits . . . . .	5
1.3 Challenges for ultra-low voltage design . . . . .	6
1.4 List of publications . . . . .	8
1.5 Summary of paper contributions . . . . .	10
2. <i>Thesis Summary</i> . . . . .	12
2.1 Subthreshold logic gates design . . . . .	12
2.1.1 Logic gates based on 4 transistors slices . . . . .	12
2.1.2 Symmetrical VTC and balancing Pull-up and pull-down networks . . . . .	13
2.1.3 Minority-3 logic gates . . . . .	15
2.2 Device sizing for ultra-low voltage applications . . . . .	18
2.2.1 Threshold voltage choice for subthreshold applications . . . . .	19
2.2.2 Higher order effects . . . . .	20
2.2.3 Back-gate and poly biasing . . . . .	24
2.2.4 Physical implementation and layout choices . . . . .	25
2.3 Ultra low-power/voltage full adder design . . . . .	26
2.3.1 FA based on min-3 and Boolean logic gates . . . . .	27
2.3.2 Characteristics of the RCAs developed in 65 nm and 28 nm . . . . .	27
2.3.3 MAC and multiplier blocks based on developed FAs . . . . .	27
2.4 Design considerations for ultra-low voltage flip-flops . . . . .	32
2.5 Subthreshold level-shifter design . . . . .	40
3. <i>Conclusion</i> . . . . .	42

---

4. <i>Publications</i> . . . . .	44
4.1 paper I . . . . .	45
4.2 paper II . . . . .	52
4.3 paper III . . . . .	59
4.4 paper IV . . . . .	64
4.5 paper V . . . . .	69
4.6 paper VI . . . . .	76
4.7 paper VII . . . . .	81
4.8 paper VIII . . . . .	86
4.9 paper IX . . . . .	97
4.10 paper X . . . . .	107
4.11 Appendix . . . . .	113

---

## Abstract

In the present day microelectronics, supply voltage scaling has received an intense attention as an efficient approach to reduce the power consumption in battery-operated and energy-harvested wireless systems. However, process, voltage and temperature (PVT) variations increase with lowering the supply voltage. This poses a challenge to ultra-low voltage (ULV) design to make robust circuits while maintaining the energy efficiency.

In this dissertation, ultra-low voltage building blocks are developed in 65 nm Bulk CMOS and 28 nm FDSOI technologies. The work focuses on making an optimal trade-off between the energy efficiency and the robustness of the building-blocks. At device level, combinations of higher order effects were considered. Static CMOS logic was used throughout the logic cells development. A constant effort was made to balance the drive strengths of the pull-up and pull-down networks with less area overhead and increase the functional yield of the cells. For the sequential elements, a single-phase clocked and contention free flip-flop structure was used. Measurement results confirmed robustness and energy efficiency of the circuits both in the 65 nm Bulk and 28 nm FDSOI technologies.

In 65 nm, the obtained 119 mV and 84 mV minimum supply voltages for the Ripple Carry Adders (RCA) proved the robustness of two types of logic cells with thick and thin Gate-Oxide thicknesses. The functionality of the single-phase clocked D type flip-flops were proven down to 132 mV in a divide-by-3 circuit.

In 28 nm FDSOI, a minimum functional supply voltage of 110 mV was achieved for RCAs and 8-bit multiplier based on Regular Threshold Voltage (RTV) devices. This is a demonstration of the functionality of both the combinational and sequential elements as the 8-bit multiplier contains the single-phased clocked flip-flops to sample outputs of the multiplier. Moreover, the minimum supply voltages of the 32-bit RCA samples reduced down to 80 mV by applying reverse back-gate voltages to the PMOS transistors. The 32-bit RCA based on minority-3 gates in 28 nm achieved an average energy per 1-bit addition of 0.65 fJ from the measurement results of nine samples. The average of measured energy per 1-bit addition of the 16-bit RCA was 0.77 fJ. From the measurements of ten samples, the implemented 8-bit multiplier in 28 nm obtained a minimum energy point of 47.2 fJ/cycle on average. The implemented logic cell library based on the Low Threshold Voltage (LVT) devices in 28 nm FDSOI was extended by adding specialized

inverters for clock tree distribution and fixing the hold time violations. A simple approach for clock distribution is also presented when the sequential elements of the circuit are single-phase clocked and race free.

A level-shifter capable of up-converting 39 mV to 1 V was implemented in 28 nm FDSOI. The diode connected devices were utilized to reduce the leakage current and decrease the minimum convertible input voltage levels. Moreover, the Single-NWELL (SNW) layout strategy was used along with the back-gate biasing and poly-biasing to create an adequate balance between the PMOS and NMOS drive strengths.

# 1. INTRODUCTION

## 1.1 CMOS circuits operation in subthreshold

Supply voltage scaling has been considered as a fundamental design parameter for reducing the power consumption and hence improving the energy efficiency of digital systems over the past decades due to the quadratic dependence of active power and energy on the supply voltage. Scaling supply voltage down to below the absolute values of devices threshold voltages, known as subthreshold region, has been known since late 1960 [1]. However, the increasing demand for low-power and energy efficient circuits along with new features of modern technologies brings the significance of ultra-low voltage (ULV) design back. The drain current in the subthreshold region is due to diffusion in a weakly inverted channel and hence has an exponential dependency on the threshold and gate-source voltages. The drain current of an NMOS transistor in the subthreshold region is given by [2]:

$$I_{SUBTH} = \mu_N C_{ox} \frac{W_N}{L_N} V_t^2 \exp \left[ \frac{V_{GS} - V_{TH}}{nV_t} \right] \left[ 1 - \exp \left[ -\frac{V_{DS}}{V_t} \right] \right] \quad (1.1)$$

In the above equation,  $\mu_N$  is the electron carrier mobility,  $C_{ox}$  is the gate capacitance per unit area,  $V_t$  is the thermal voltage,  $V_{TH}$  is the threshold voltage,  $W_n$  is the device width,  $L_n$  is the devices length,  $V_{GS}$  is the gate-source voltage,  $V_{DS}$  is the drain-source voltage and  $n$  is the inverse slope of the subthreshold current which is given by:

$$n = 1 + \frac{C_D}{C_{ox}} \quad (1.2)$$

In Eq 1.2,  $C_D$  is the depletion channel region capacitance per unit area. The advantage of operating digital CMOS circuits in the subthreshold region for achieving minimum energy per operation was first introduced in [3]. The concept of minimum energy point (MEP) was revisited and its dependence

on activity factor ( $\alpha$ ) was explained in [4]. The total power consumption of a digital circuit can be explained as:

$$P_{tot} = P_{dyn} + P_{stat} = \alpha f C_{tot} V_{dd}^2 + I_{leak} V_{dd} \quad (1.3)$$

In equation 1.3,  $\alpha$  is activity factor,  $f$  is operating clock frequency,  $C_{tot}$  is the total switched capacitance of the circuit and  $I_{leak}$  is the total leakage current of the circuit. The leakage current can be determined from equation 1.1 when  $V_{GS} = 0$ . With  $t_{clk}$  being period of the clock signal, the total energy of the digital circuit can be explained as:

$$E_{tot} = E_{dyn} + E_{stat} = P_{tot} \times t_{clk} = \alpha C_{tot} V_{dd}^2 t_{clk} + I_{leak} V_{dd} t_{clk} \quad (1.4)$$

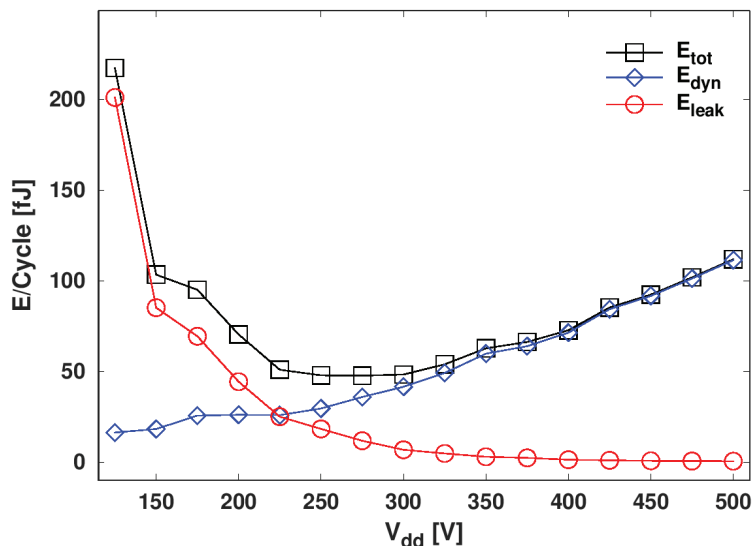


Fig. 1.1: Dynamic and static energy consumption of an 8-bit parallel multiplier as a function of  $V_{dd}$

By reducing  $V_{dd}$ , dynamic energy reduces while the static energy increases because of exponential increment in the circuit delay. Theoretically, the supply voltage ( $V_{ddopt}$ ) at which the MEP occurs can be found by solving  $\partial E_{tot} / \partial V_{dd} = 0$  [5]. Figure 1.1 shows the measured total, dynamic and static energy consumptions of an 8-bit parallel multiplier implemented in 28 nm FDSOI CMOS technology as an example. This circuit achieves a minimum

---

energy of 47.7 fJ at 275 mV while the static energy reaches dynamic energy consumption at a supply voltage of 225 mV. A detailed description and more measurement results of the multiplier circuit are provided in section 2.3.3.

## 1.2 *Motivation for ultra-low voltage CMOS circuits*

Circuits operating in ultra-low voltage domain provide solution for a wide range of applications with limited power or energy budget.

Battery operated wireless sensor networks (WSNs) are becoming more common with the advent of the Internet-of-Things (IoT). As the MEP of digital circuits occurs in the subthreshold or nearthreshold region, considerable improvement in energy efficiency (up to 10x [6]) can be achieved by lowering the supply voltage down to the threshold voltage of transistors. This in turn prolongs the battery lifetime of WSNs.

While the energy efficiency is the main focus for the battery-operated systems, there are some applications where the power consumption and the minimum operating voltage of the circuit is the main concern. Battery-less systems operating directly from the energy harvesting source and always-on circuits in a microcontroller (e.g. wake-up circuitry) are examples for systems where the limiting factor comes from the power budget and the minimum required supply voltage.

Schmitt-Trigger based logic cells operating down to 62 mV supply voltage were used in [7] to reduce the minimum functional supply voltage of the digital circuits. This in turn reduces the required supply voltage at which an active operation can start. Dynamic leakage-suppression logic (DLSL) is introduced in [8] to dramatically reduce the static power of logic cells. The power consumptions of the developed logic gates were in the range of few fW at extremely low operating frequencies. The size of the energy harvesting source can be reduced by using DLSL thanks to the extremely low power consumptions of circuits based on DLSL.

The power and energy density of CMOS processors increase as transistors density increases without supply voltage scaling. As a result, part of silicon, known as dark silicon [9], cannot be powered-on at any given time. Despite the performance degradation of ultra-low voltage circuits, near-threshold circuits can be useful in processors with multiple cores. The functionality and energy efficiency of an IA-32 processor in ULV domain has been proven in [10]. Furthermore, it has been discussed in [11], [12] that processors op-



erating in near-threshold helps to overcome the dark silicon effect in a chip multiprocessor.

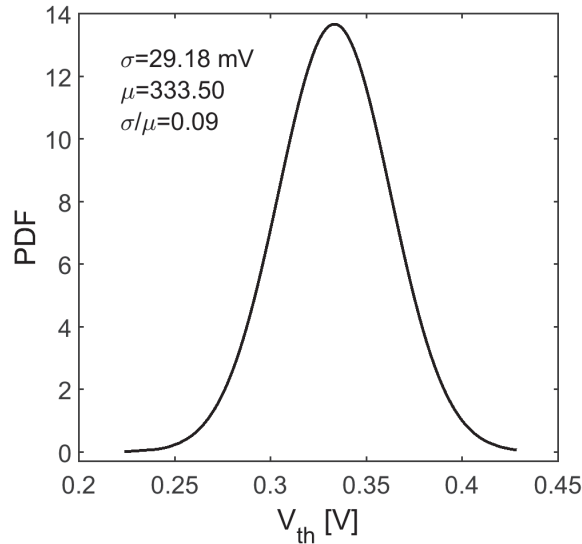


Fig. 1.2: NMOS threshold voltage distribution

### 1.3 Challenges for ultra-low voltage design

The threshold voltage variations in CMOS technologies follows a Gaussian distribution [13]. Due to the quadric dependence of on-current on the threshold voltage, the drain current of the CMOS devices shows also a normal distribution in super-threshold region. However, the on-current of the CMOS transistors exhibit a lognormal distribution in subthreshold region because of the exponential dependence of the drain current on threshold voltage in this region [14].

A Lognormal distribution has a long tail and hence higher variability ( $\sigma/\mu$ ). Figure 1.2 shows the statistical distribution of threshold voltage for a minimum sized NMOS ( $W=80$  nm and  $L=30$  nm) transistor in a 28 nm UTBB-FDSOI CMOS technology obtained from 2000 Monte Carlo (MC) runs at  $V_{ds} = V_{gs} = 1$  V. The threshold voltage has an average ( $\mu$ ) value of 333.5 mV and a standard deviation ( $\sigma$ ) of 29.18 mV. The resultant statistical distributions of drain current for a minimum sized NMOS at 1 V and

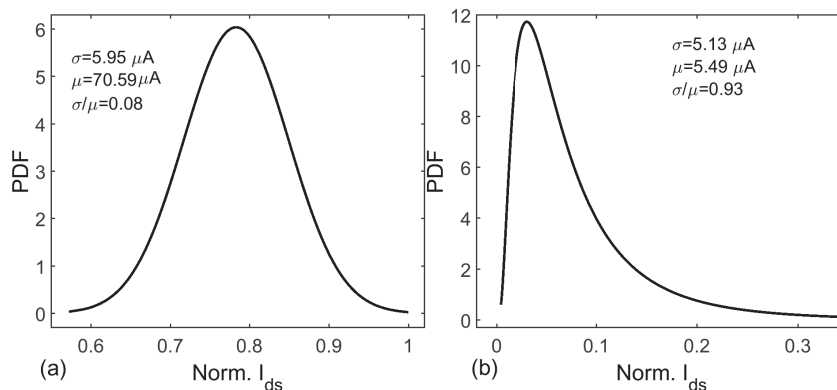


Fig. 1.3: NMOS on-current distribution in (a) super-threshold and (b) subthreshold regions

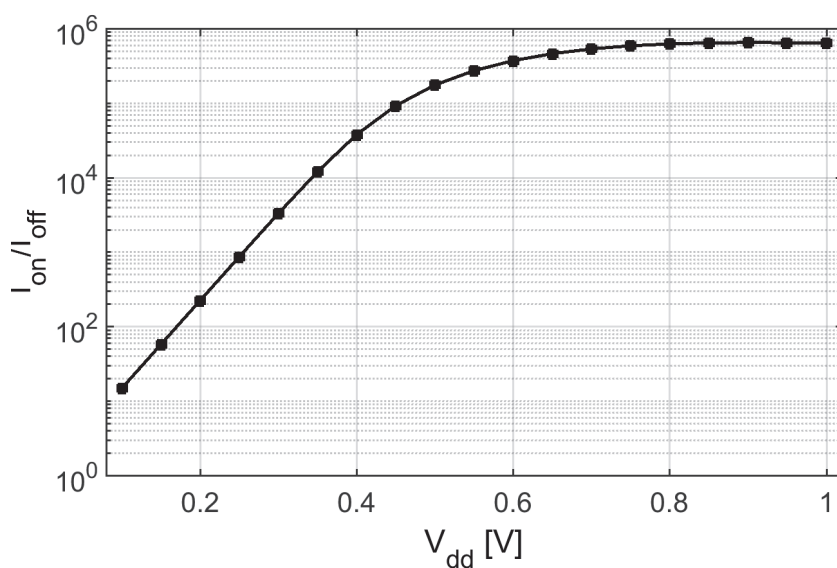


Fig. 1.4: Ion/Ioff Ratio of a minimum sized NMOS as a function of  $V_{dd}$

200 mV are also depicted in Figure 1.3(a) and (b), respectively. As can be observed from Figure 1.3, the variability of the drain current at 200 mV is 0.93 which is much higher than the variability at 1 V. The delay of CMOS logic gates is proportional to the transistors on current in the subthreshold region ( $t_d \propto \frac{C_l V_{dd}}{I_0 \exp(V_{dd} - V_{th}/nV_t)}$ ) [14]. Therefore, the delay in the subthreshold region

exhibits much wider variations compared to the delay in super-threshold region because of the wider variations range of devices current in subthreshold. Another main issue that makes circuit design more challenging in subthreshold region is extremely degraded  $I_{on}/I_{off}$ -ratio of transistors in ultra-low supply voltages. This can be seen in Figure 1.4 where the  $I_{on}/I_{off}$  ratio for a minimum sized NMOS transistor in 28 nm UTBB FDSOI technology is shown as a function of supply voltage. Process, voltage and temperature (PVT) variations can worsen the weak  $I_{on}/I_{off}$  ratio in subthreshold and consequently result in functional failure.

### 1.4 List of publications

This thesis is based on a collection of papers that are related to ultra-low voltage/power and energy efficient circuits.

In addition to the following papers, three items are also included in chapter 2: (a) It is shown in section 2.1.3 that the 10-transistor minority-3 gate we used in [15] does not restrict the functional yield of the subthreshold cell library when supply voltage is above a specific value (i.e.  $V_{dd} > 130mV$ ). (b) Measurement results of an 8-bit multiplier which is based on the same full adders we reported in [15] are shown in section 2.3.3. (c) In section 2.4, the custom library cell we presented in [16] is extended by adding specialized inverters for clock tree distribution and fixing hold time violations. In the following list, Paper VIII and Paper IX are extended versions of Paper VI and Paper VII, respectively, published in the MICPRO journal. Paper II received a best paper award in 2015 IEEE ASQED conference [17] (see Appendix).

- Paper I: J. E. Bjerkedok, A. A. Vatanjou, T. Ytterdal and S. Aunet, "Modular layout-friendly cell library design applied for subthreshold CMOS," 2014 NORCHIP, Tampere, 2014, pp. 1-6.
- Paper II: A. A. Vatanjou, T. Ytterdal and S. Aunet, "Energy efficient sub/near-threshold ripple-carry adder in standard 65 nm CMOS," 2015 6th Asia Symposium on Quality Electronic Design (ASQED), Kuala Lumpur, 2015, pp. 7-12.
- Paper III: A. A. Vatanjou, T. Ytterdal and S. Aunet, "Exploiting short channel effects and multi-Vt technology for increased robustness and reduced energy consumption, with application to a 16-bit subthreshold

---

adder implemented in 65 nm CMOS,” 2015 European Conference on Circuit Theory and Design (ECCTD), Trondheim, 2015, pp. 1-4.

- Paper IV: A. A. Vatanjou, T. Ytterdal and S. Aunet, ”4 Sub-/near-threshold flip-flops with application to frequency dividers,” 2015 European Conference on Circuit Theory and Design (ECCTD), Trondheim, 2015, pp. 1-4.
- Paper V: A. A. Vatanjou, T. Ytterdal and S. Aunet, ”28 nm UTBB-FDSOI energy efficient and variation tolerant custom digital-cell library with application to a subthreshold MAC block,” 2016 MIXDES - 23rd International Conference Mixed Design of Integrated Circuits and Systems, Lodz, 2016, pp. 105-110.
- Paper VI: E. Låte, A. A. Vatanjou, T. Ytterdal and S. Aunet, ”Comparative analysis of flip-flop architectures for subthreshold applications in 28nm FDSOI,” 2015 Nordic Circuits and Systems Conference (NORCAS): NORCHIP & International Symposium on System-on-Chip (SoC), Oslo, 2015, pp. 1-4.
- Paper VII: A. A. Vatanjou, E. Låte, T. Ytterdal and S. Aunet, ”Ultra-low voltage adders in 28 nm FDSOI exploring poly-biasing for device sizing,” 2016 IEEE Nordic Circuits and Systems Conference (NORCAS), Copenhagen, 2016, pp. 1-4.
- Paper VIII: Even Låte, Ali Asghar Vatanjou, Trond Ytterdal, Snorre Aunet, ”Extended Comparative Analysis of Flip-Flop Architectures for Subthreshold Applications in 28 nm FD-SOI”, *Microprocessors and Microsystems*, Volume 48, 2017, Pages 11-20, ISSN 0141-9331.
- Paper IX: Ali Asghar Vatanjou, Even Låte, Trond Ytterdal, Snorre Aunet, ”Ultra-low voltage and energy efficient adders in 28 nm FD-SOI exploring poly-biasing for device sizing”, *Microprocessors and Microsystems*, Volume 56, 2018, Pages 92-100, ISSN 0141-9331.
- Paper X: A. A. Vatanjou, T. Ytterdal and S. Aunet, ”An Ultra-Low Voltage and Low-Energy Level Shifter in 28-nm UTBB-FDSOI,” in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 66, no. 6, pp. 899-903, June 2019.

### 1.5 Summary of paper contributions

The major contributions and achievements of the publications related to this thesis are as following:

In Paper I [18], the development of logic cells based on the identical slices of stacked transistors has been proposed. This leads to less variability in the delay of the logic cells, increases manufacturability of the logic cells and decreases the leakage current.

In Paper II [35], it has been shown that the required  $W_p/W_n$  ratio for balancing the switching point of an inverter at  $V_{dd}/2$  reduces by increasing the channel length of the transistors up to an optimal value even though the on-current of NMOS and PMOS do not increase with increasing the channel length. Additionally, the required PMOS width for balancing its drive strength with the NMOS decreases more rapidly thanks to the Inverse Narrow Width Effect (INWE). This in turn results in less parasitic switching capacitance and reduces the energy consumption of the circuit. The delay of the circuit, on the other hand, increases as the on-current of the transistors decreases by increasing the channel length. However, the rise in the propagation delay can be compensated by increasing the operating supply voltage while consuming less energy for given delay. The reported 84 mV operating voltage of the 32-bit RCA was, to the best of the author's knowledge, the lowest reported supply voltage for the static CMOS logic gates.

In Paper III [20] and Paper IV [21], we used Reverse Short Channel Effect (RSCE) and Inverse Narrow Width Effect (INWE) together with different threshold voltage flavors in the pull-up and pull-down networks to achieve a robust ultra-low voltage operation and increase the energy efficiency of the logic cells. Measurement results confirmed a minimum operating voltage of 132 mV for the divide-by-3 circuit based on the single-phase clocked D flip-flops. A minimum operating voltage of 119 mV was also achieved for a 16-bit Ripple Carry Adder (RCA) based on the Boolean logic gates.

In paper V [16], we developed an energy efficient custom logic cell library based on LVT 28 nm transistors for subthreshold applications. We focused on making a satisfactory trade-off between sensitivity to the variations and energy consumption of the digital logic cells. We considered the threshold voltage reduction with the transistors width, known as Narrow width Effect (NWE), to make a trade-off between the robustness and parasitic switching capacitance of the logic cells. Moreover, use of longer channel length resulted in 46% improvement in the  $I_{on}/I_{off}$  ratio of the transistors at the cost of a

13.4% increase in the energy consumption. The asymmetric back-gate biasing scheme provided much better balance between the drive strength of the NMOS and PMOS. Compared to the state of the art MAC blocks, the synthesized MAC block based on the developed cell library reveals more energy efficiency for the clock frequencies in the MHz-range. The presented library cell in this paper was extended by adding proper inverters for clock distribution and buffers for fixing hold-time violations.

In paper VI [22] and paper VIII [23], nine D-type flip-flop architectures were implemented in 28 nm FDSOI technology. The flip-flops structures were evaluated in terms of timing constraints, energy consumption, leakage, area and minimum operating supply voltage.

In paper VII [24] and paper IX [15], ultra-low voltage and energy efficient adders based on min-3 and Boolean logic gates has been presented. The logic cells implemented using the Regular Threshold Voltage (RVT) devices in 28 nm FDSOI technology. We explored poly-biasing and back-gate biasing techniques to balance the drive-strength of the pull-up and pull-down networks with relatively equal area for the PMOS and NMOS transistors. This causes both the standard deviation and mean values of the inverter to have similar values. Both the adders obtained a minimum  $V_{dd}$  of 110 mV while the minimum  $V_{dd}$  of the 32-bit adder based on min-3 gates decreased to 80 mV by applying reverse back-bias voltages to the PMOS transistors. One sample was functional at 79 mV with a 430 mV reverse back bias voltage applied to its PMOS devices. From the measurement results of nine samples, the 32-bit adder based on min-3 gates and the 16-bit adder based on Boolean gates achieved an average minimum energy per 1-bit addition of 0.65 fJ and 0.77 fJ, respectively.

In Paper X, we reported an energy efficient level-shifter in 28 nm FDSOI technology. The level shifter topology uses top diode connected devices together with the current limiter diodes. This topology along with the single-NWELL layout strategy allows to achieve a balanced pull-up network (PUN) and pull-down network(PDN) at extremely low  $V_{ddLs}$ . The level-shifter were capable of up-converting 39 mV input voltage to 1 V.

## 2. THESIS SUMMARY

### 2.1 *Subthreshold logic gates design*

Although static logic families provide the most simple and robust approach to implement logic gates [26], several logic styles have been proposed for ULV applications to meet specific requirements. In [27], stacked NMOS transistors utilized in transmission gate (TG) logic to have a relaxed PMOS sizing and reduced leakage. Operating frequencies in the MHz range were achieved in subthreshold region by implementing highly pipelined datapath blocks (MAC and ADDER) based on TG-logic with stacked NMOSs and low-Vt (LVT) transistors. It has been demonstrated in [7] that digital circuits based on Schmitt-trigger (ST) logic gates are able to operate at very low supply voltages down to 62 mV. The main application of the ST logic gates is in systems powered by energy harvesting sources (e.g. thermal generator) where the use of ST logic gates reduces the minimum  $V_{DD}$  that an active operation can start. Another proposed logic style for ultra low power (ULP) applications is Dynamic Leakage-Suppression Logic (DLSL) [8] that consumes 10 fW active power per gate. DLSL family is proper for battery-less WSNs power by energy harvesting source with very low throughput requirements (operating frequency in the range of few Hz).

For works related to this thesis, we used static CMOS logic style as basic topology in our subthreshold logic libraries due to simplicity and robustness of this topology. We focused on optimizing static logic gates for subthreshold applications by accurate device sizing.

#### 2.1.1 *Logic gates based on 4 transistors slices*

Logic gates based on identical slices of stacked transistors (2 stacked NMOS and 2 stacked PMOS) have been introduced and discussed in Paper I [18]. The main idea behind developing logic gate libraries based on identical slices of stacked transistors is to improve manufacturability and yield for scaled

CMOS technologies through increasing the regularity of the design. It has been shown in Paper I [18] that the delay variability ( $\sigma/\mu$ ) of logic gates based on the identical slices of stacked transistors is lower compared to the conventional static CMOS logic gates with the same total area. As an example, parameters of the NAND gate based on identical slice of stacked transistors (8T-NAND2) were compared to the parameters of two conventional NAND gates. One with the same footprint area (4T-NAND2II) and one with the minimum device dimensions (4T-NAND2I). The schematic and layouts of NAND gates are shown in figure 2.1. It has been shown that the 8T-NAND2 has less rise and fall delays variability compared to 4T-NAND2I and less power consumption compared to the 4T-NAND2II. The delay variability for 8T-NAND2 was about 53.5% lower than the corresponding value for the 4T-NAND2I while energy per operation of the 4T-NAND2I was 38% lower than energy per operation of the 8T-NAND2. The 8T-NAND2 had 44% more delay variability and 51% less energy per operation in comparison to 4T-NAND2II with equal total area. Figure 2.2 [18] shows relative comparison between these three NAND implementations.

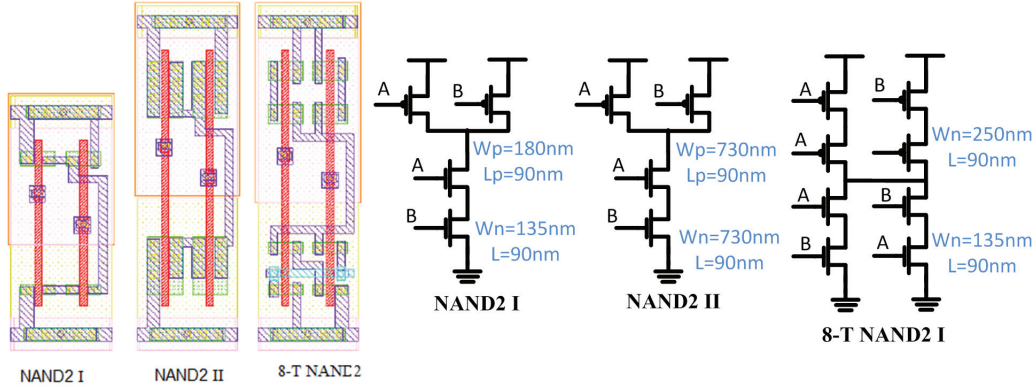


Fig. 2.1: Schematic and layout of the 4T-NAND2I, 4T-NAND2II, 8T-NAND2 gates.

### 2.1.2 Symmetrical VTC and balancing Pull-up and pull-down networks

Balancing pull-up network (PUN) and pull-down network (PDN) drive strengths is a key issue to increase the functional yield of static CMOS logic gates especially in deep subthreshold applications. To have equal rise and fall delays,



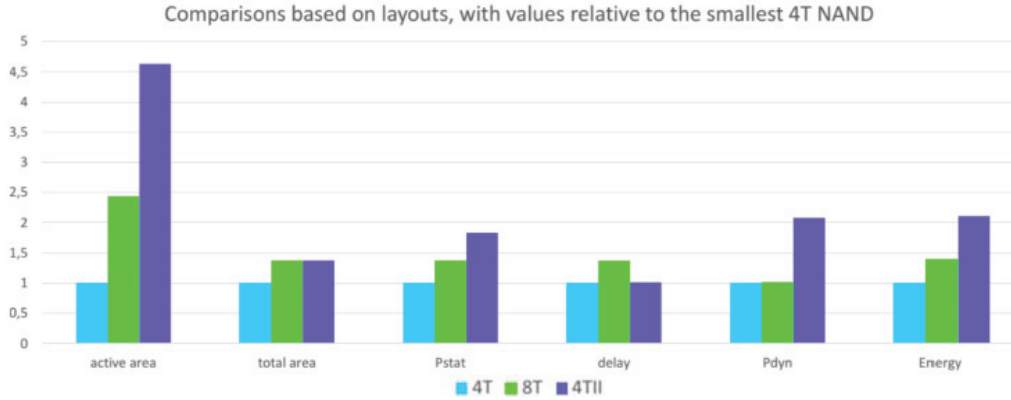


Fig. 2.2: Relative comparisons between the three NAND implementations [18].

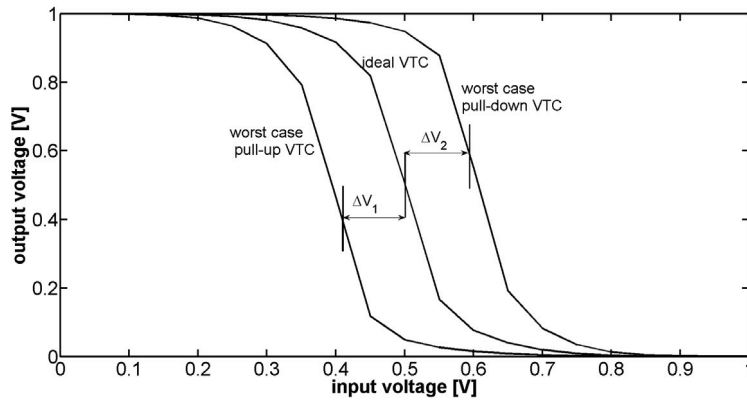


Fig. 2.3: Sizing of logic gates with symmetrical VTC [20].

drive strength of the pull-up and pull-down networks must be identical. Additionally, unbalanced high and low noise margins leads to extra leakage energy overhead in subthreshold circuits [28]. As shown in paper III [20], equalizing the switching point deviation of worst cases voltage transfer curves (VTC) from  $V_{DD}/2$  maximizes the static noise margin (SNM) in the logic gates with more than one inputs. This is shown graphically in figure 2.3

For minimum sized devices, the on-current ratio of the PMOS with respect to the NMOS is usually too small in the ULV domain. So, in a balanced logic gate the PMOS transistors must be much wider than the NMOS transistors. For example, to balance PUN/PDN the PMOS gate width should be more

than 7x [20] and 4x [15] of the NMOS gate width in 65 nm bulk and 28 nm FDSOI technologies, respectively. This in turn leads to wider variations in the fall time of a logic gate compared to its rise time. It is proposed in paper IX [15] to use relatively equal active areas for PUN and PDN to achieve a better match in the rise and fall delays variability. Figure 2.4 [15]<sup>1</sup> compares the mismatch simulations of rise and fall FO4 delays for three inverters. The schematics of the inverters are shown in figure 2.5. In figure 2.4, the drive strengths of PMOS and NMOS are balanced by upsizing PMOS width in INV1. INV2 has the same total area as INV1 but the PMOS/NMOS drive strengths are unbalanced. The PMOS and the NMOS of INV3 are balanced with relatively equal active areas. Although the average values of rise and fall delays are equal in INV1, the fall delay standard deviation is 2.5x of the rise delay standard deviation. Despite the small difference in rise and fall delays variability in INV2, its rise delay mean value is 2.8x fall delay mean value. The difference in fall and rise delay variability of INV3 is only 2%, and its fall delay mean value is comparable to the rise delay mean value. Therefore, the importance of balancing PUN and PDN derive strengths with relatively equal active area for PMOS and NMOS transistors is recognized when the variations are considered in subthreshold region. The balancing of NMOS and PMOS drive strengths will be discussed furthermore in sections 2.2.3 and 2.2.4.

### 2.1.3 Minority-3 logic gates

Minority-3 (min-3) is a three-input logic gate, and its output is high only when two or three inputs are low. Figure 2.6 [29] represents the schematic and truth table of a 10-transistor min-3 logic gate. The robustness and reliability of different min-3 logic gates have been discussed in [30], and the possibilities of making synchronous or asynchronous systems from min-3 gates has been demonstrated.

The 10-transistor min-3 logic gate is used in developed logic libraries of this work due to its energy efficiency, robustness, regular topology and relatively small area. In [31], the functionality of logic cells has been evaluated by connecting a minimum sized inverter back-to-back with the logic cells whose outputs provide worst cases input-high ( $V_{IH}$ ) and input-low ( $V_{IL}$ ) voltages.

<sup>1</sup> In [15], the  $t_{PHL}$  distribution for INV2 was incorrectly placed in the position of INV3  $t_{PHL}$  distribution. This is corrected in the current version of the figure.

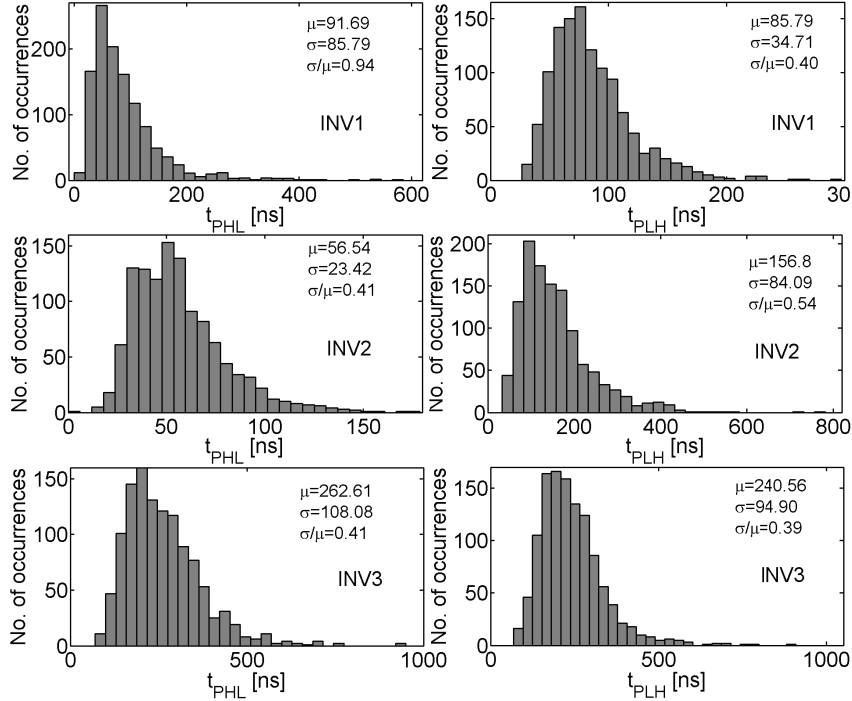


Fig. 2.4: Rise and fall FO4 delays variability with different sizing approaches at a supply voltage of 200 mv.

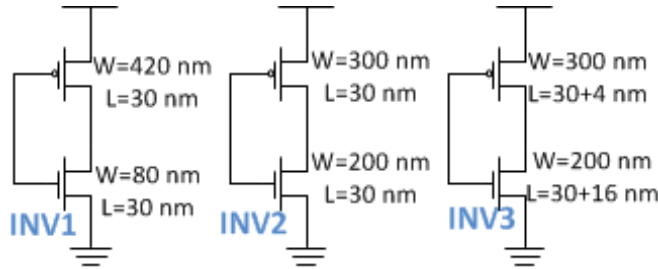


Fig. 2.5: Schematic of three inverters used for rise and fall delays analysis.

Assuming a library cell with the maximum fan-in of two and logic cells with symmetrical VTCs [20], the worst case configuration to evaluate the output-low ( $V_{OL}$ ) voltage of a 1x strength inverter is shown in Figure 2.7(a). The test-bench for quantifying the output-high ( $V_{OH}$ ) voltage is illustrated in Figure 2.7(b). If minority-3 (min3) gates are also added to the library, min3

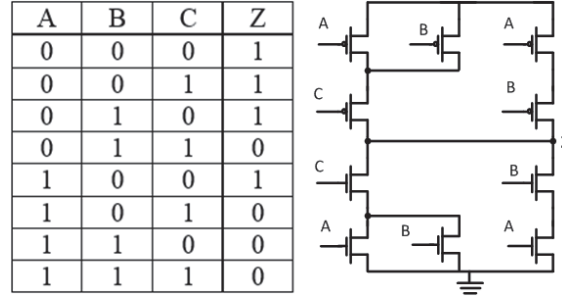


Fig. 2.6: schematic and truth table of a 10-transistor min-3 logic gate.

gates with input configurations shown in Figure 2.7(c) and (d) provide the most stringent  $V_{IH}$  and  $V_{IL}$ , respectively. Therefore, the test-benches for evaluating  $V_{OL}$  and  $V_{OH}$  of a 1x strength inverter are shown in Figure 2.7(c) and (d), respectively. The static noise margin (SNM) follows a Gaussian distribution and is determined by the methodology presented in [32]. Assuming that a logic cell to be failing when its SNM is less than  $V_L$ , the corresponding functional failure probability of the logic cell is as equation 2.1 [33]

$$P_{fail} = \frac{1}{\sigma_{SNM}\sqrt{2\pi}} \int_{-\infty}^{V_L} \exp\left(-\frac{(x - \mu_{SNM})^2}{\sigma_{SNM}^2}\right) dx \quad (2.1)$$

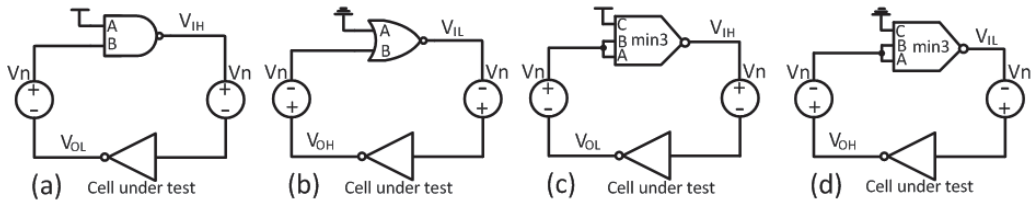


Fig. 2.7: Benchmark circuits to measure SNM of logic cells (a)  $V_{IH}$  is generated by NAND2 (b)  $V_{IL}$  is generated by NOR2 (c)  $V_{IH}$  is generated by min3 (d)  $V_{IL}$  is generated by min3.

In equation 2.7,  $\sigma_{SNM}$  is the standard deviation and  $\mu_{SNM}$  is the average of the SNM. From equation 2.1, the functional failure rate of logic cells depends on the variability ( $\sigma/\mu$ ) of the SNM. Figure 2.8(a) shows the variability of an inverter SNM when  $V_{IH}$  and  $V_{IL}$  are generated by NAND2, NOR2 and min3 gates. The analysis here considers a logic cell to be failing when its

SNM is less than 0. The output swing failure rate of the inverter is depicted in Figure 2.8(b). As can be observed from Figure 2.8(b), the probability that the 1x strength inverter functionality fails is lower when  $V_{IH}$  and  $V_{IL}$  are generated by the min-3 gate instead of NAND2/NOR2 gates if  $V_{dd} > 130$  mV. Thereby, the min-3 gate does not restrict the functional yield of the logic cells developed in [15] when  $V_{dd} > 130$  mV. The maximum  $\sigma/\mu$  of the inverter high or low SNM was used to calculate the failure rate in Figure 2.8(b). It is worth noting that for  $V_{dd} > 190$  mV, the functional failure probability of the inverter is 0 when skewed VTCs of the min-3 gate are assumed to give the worst  $V_{IH}/V_{IL}$ .

The measurement results of the full adders (FA) based on the min3 and Boolean logic gates, reported in paper IX [15], showed that the worst minimum operating voltage of different chip samples were 125 mV for both adder topologies. This is in agreement with the results that are presented here.

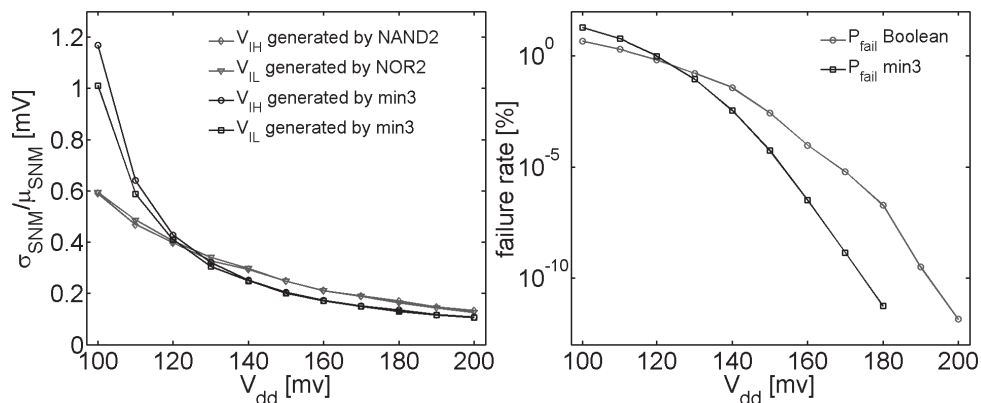


Fig. 2.8: (a) Variability of the SNM vs  $V_{dd}$  (b) output swing failure rate vs  $V_{dd}$ .

## 2.2 Device sizing for ultra-low voltage applications

In the subthreshold region, the performance of circuits changes drastically with fluctuations in the threshold voltage of the transistors due to the exponential dependency of drain-source current on threshold voltage. As discussed in the previous section, imbalanced PUN and PDN drive strengths results in functional failure and more leakage power consumption in ULV

circuits. Moreover, PMOS and NMOS devices should have relatively equal active area to have similar variability in rise/fall delays and reduce parasitic capacitance and leakage of CMOS logic gates [15]. Therefore, higher order effects and different techniques offered by the available technology should be taken into account during circuit design to suppress variations and create a good balance between PMOS and NMOS drive strength. In this thesis, 65 nm bulk CMOS and 28 nm FDSOI technologies are used to develop building blocks and cell libraries for subthreshold applications.

### 2.2.1 *Threshold voltage choice for subthreshold applications*

Multi-Vt devices are featured in both 65 nm bulk and 28 nm FDSOI technologies used here. A good trade-off between the static power consumption and performance of logic cells can be achieved through the proper selection of the devices threshold voltage taking the required data throughput into account. This means that low threshold voltage devices are appropriate for the applications with high throughput requirements and transistors with high threshold voltage are preferable when the data throughput is low [34]. Therefore, we developed libraries based on devices with different threshold voltages. The 65 nm bulk technology that has been used offers low-power (LP) and general-purpose (GP) devices. The GP process features a thin gate oxide and hence GP transistors are proper choice for applications with high operating frequencies. The LP process, on the other hand, offers devices with thick gate oxide and lower leakage. Additionally, multi-Vt transistors are implemented through different dopant in channel area. We developed an energy efficient 32-bit adder in paper II [35] based on the low-Vt GP transistors for medical ultrasound applications (2.3 ns delay per 1-bit addition) [36]. The power consumption of 8-bit Ripple-Carry Adders (RCA) based on standard-Vt (SVT), low-Vt (LVT) or high-Vt GP-devices operating at different frequencies are listed in TABLE 2.1 [35]. As can be seen from Table 2.1, LVT transistors provided the lowest power consumption for the frequencies above 50 MHz.

Transistor level intra-cell multi-Vt design has been used in [37] to make a trade-off between delay and leakage current of static CMOS logic cells. In the logic gates we developed in paper III [20], low-power (LP) LVT-PMOS devices are in the PUN of all the logic gates and LP-SVT-NMOS devices are in the PDN of all the logic gates. In addition to smaller PMOS dimensions, this offers the possibility of utilizing reverse short channel effect (RSCE)

Tab. 2.1: 8-bit RCA power consumption as a function of threshold voltage and operating frequency

	SVT	LVT	HVT
P [nW]@ 10MHz	77.1	118.5	100.9
$V_{dd}$ [mV]@ 10MHz	240	175	340
P [nW]@ 50MHz	569.1	546.5	758.3
$V_{dd}$ [mV]@ 50MHz	355	280	430
P [nW]@ 100MHz	1520	1400	2250
$V_{dd}$ [mV]@ 100MHz	420	350	520

in both NMOS and POMS transistors. This in turn decreases the energy consumption and increases the robustness of the logic cells.

### 2.2.2 Higher order effects

Short channel effect (SCE) [38], Reverse Short channel Effect (RSCE) [39], Narrow Width Effect (NWE) [40] and Inverse Narrow Width Effect (INWE) [41] are notable examples of various high order effects that cause modification in the threshold voltage of devices in deep sub-micron technologies. These effects should be considered carefully during logic cell development for sub-threshold applications because any change in the threshold voltage of devices has an exponential effect on the drain-source current.

RSCE:

A non-uniform channel doping (HALO doping) can be used to mitigate variations in the threshold voltage due to the short channel effect (SCE) and drain induced barrier lowering (DIBL) [39]. As a result, the threshold voltage of devices with HALO doping decreases when increasing the device channel length. Since the drain-source current has an exponential dependency on the threshold voltage in subthreshold region, the RSCE can be used to increase the drive capability of the MOS devices [42]. In addition, the total gate capacitance can be reduced by increasing the channel length up to an optimal value [42]. Thereby, a given on-current can be achieved with less load capacitance by increasing the channel length rather than the channel width.

The mechanism of RSCE is not identical for all transistor types, and for some devices it might results in non-monotonic changes in the drain current. In paper II [35], we used RSCE to balance drive strengths of the NMOS and PMOS transistors. The optimum channel length results in min-

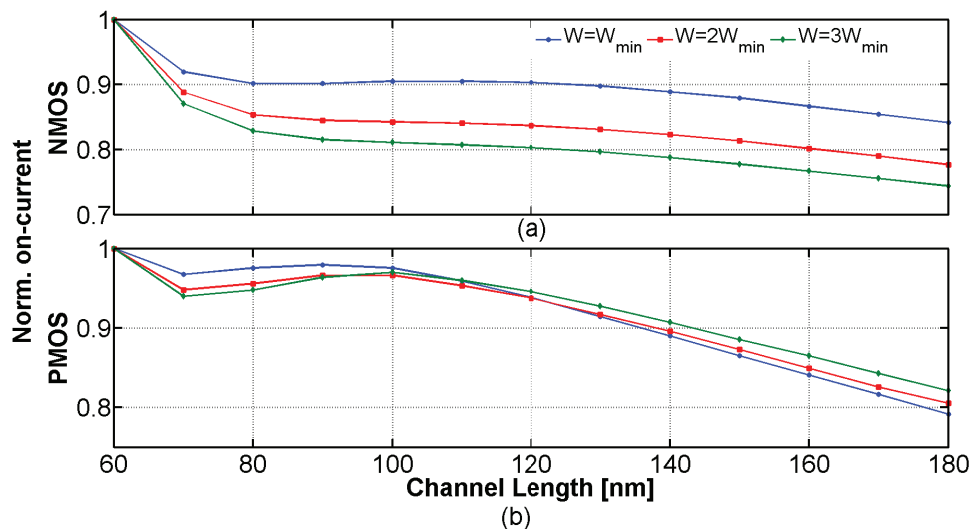


Fig. 2.9: (a) Normalized on-currents vs. channel length (a) NMOS (b) PMOS [35].

imum PMOS/NMOS width ratio in the procedure for balancing the drive strengths of the NMOS and PMOS. Figure 2.9 shows normalized LVT-GP NMOS and PMOS drain current ratios for three different multiples of the minimum transistor widths (135 nm) in 65 nm bulk technology. The optimum channel length is the channel length for which the PMOS on-current ratio over NMOS on-current ratio is minimum.

In the dual-Vt logic gates of paper III [20], LVT-LP PMOS devices are used in the PUN and SVT-LP NMOS transistors are used in the PDN of all the logic gates. By doing so, the RSCE is strong enough in both PMOS and NMOS transistors to increase the drain current with the channel length increment. In dual-Vt logic gates [20], longer channel length results in improved energy efficiency, less variability in cells delay and significant improvement in the functional yield. By using a channel length of 200 nm instead of 60 nm, a five-stage ring-oscillator which was comprised of dual-Vt basic logic gates showed 17% less variability in the propagation delay and 31% less energy consumption for a supply voltage of 150 mV. The overhead of having a 200 nm channel length was 12% larger footprint area. Additionally, as shown in figure 2.10, a significant improvement in the functional yield of the logic gates were achieved by increasing the channel length to 200 nm.

INWE:



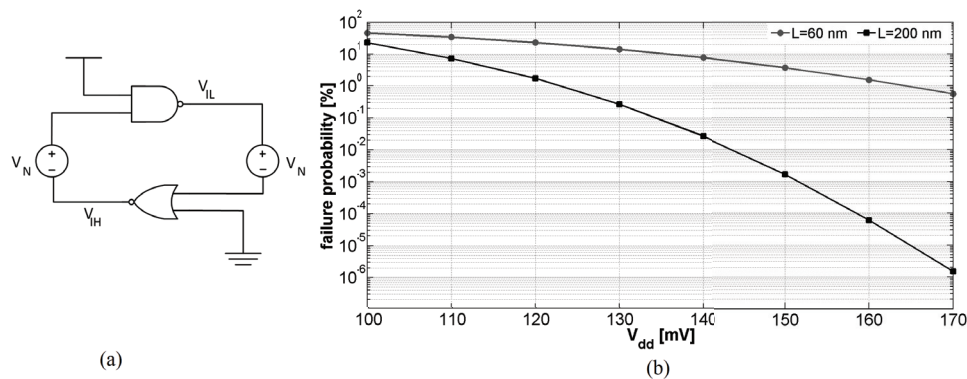


Fig. 2.10: (a) Test-bench to evaluate the worst case logic output swing (b) probability of output swing failure as a function of  $V_{dd}$  ( $T = 27$  °C and 2k MC runs) [20].

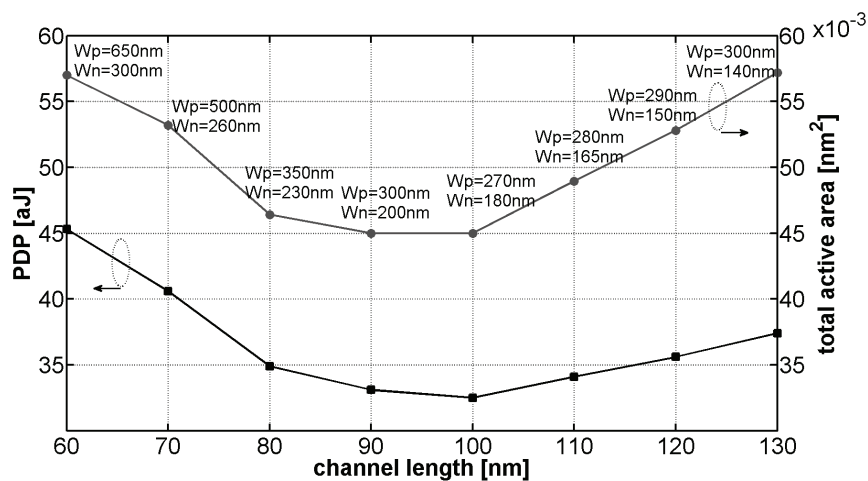


Fig. 2.11: PDP and total area of an inverter versus channel length [35].

The mechanism of device threshold voltage shift as a function of the channel width depends on the isolation oxide structure [43]. The threshold voltage increases with increasing the channel width when shallow trench isolation (STI) is used to isolate transistors [43]. Both subthreshold logic cells in paper II [35] and paper III [20] we developed in 65 nm bulk technology are INWE-aware.

It is shown in paper II [35] that the required  $W_p/W_n$  to balance the switch-

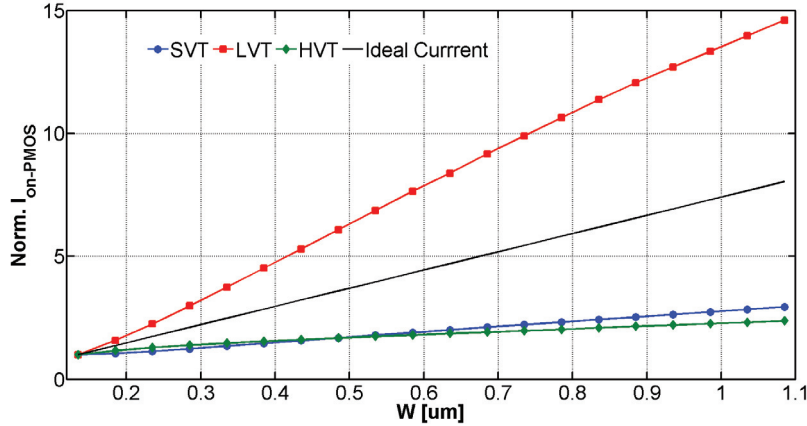


Fig. 2.12: Normalized on-current of PMOS transistors with different threshold voltages as a function of  $W$  [20].

ing point of an inverter at  $V_{dd}/2$  reduces by increasing the channel length up to 100 nm. In figure 2.11, the total active area of the NMOS was kept constant (not to lose robustness) and the PMOS width selected to balance an inverter. This reduction in the required  $W_p/W_n$  ratio is for two reasons. Firstly, as discussed earlier, the RSCE strength on used PMOS and NMOS devices is not identical and  $I_{on-NMOS}/I_{on-PMOS}$  decreases by increasing the channel length up to 100 nm [35]. Secondly, the PMOS on-current per width increases by decreasing its width due to the INWE.

Figure 2.12 [20] illustrates the normalized on-current of the LP-PMOS transistors with different threshold voltages versus the channel width. The black line represents the normalized ideal drain-source current which is proportional to the channel width. The drain-source current of SVT and HVT devices increases more slowly than what was expected because their threshold voltage increases with channel width as a result of INWE. The drain-source current of the LVT-PMOS transistor on the other hand increases even more rapidly than what was expected due to the lower bulk implant dose. Therefore, the reduced drain-source current due to the INWE can be avoided in the developed subthreshold logic gates in paper III [20] by using minimum sized SVT-NMOS devices in pull-down transistors and LVT-PMOS devices in pull-up transistors.

NWE:

In silicon on insulator (SOI) technology, threshold voltage shift with respect

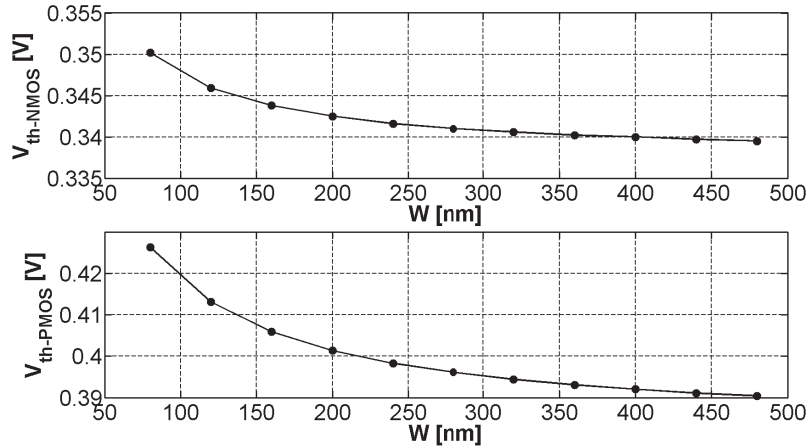


Fig. 2.13: Threshold voltage shift of PMOS and NMOS as a function of channel width,  $V_{ds} = 0.2$  V and  $L=34$  nm. [16].

to the channel width depends on the buried oxide (BOX) thickness, and the threshold voltage decreases with increasing the channel width for SOI technologies with thin oxide thickness [44]. The threshold voltage of transistors in the 28 nm FDSOI technology that was used increases by decreasing the channel width as shown in figure 2.13 [16]. To mitigate threshold voltage variations due to lithography effects on matching property of the transistors, a minimum gate width was selected considering the threshold voltage shift as a function of channel widths in both logic gates in paper V [16] and paper IX [15].

### 2.2.3 Back-gate and poly biasing

The 28 nm FDSOI technology that was used offers effective knobs such as back-gate biasing (BB) and poly biasing (PB). For an authorized poly pitch in the 28 nm FDSOI technology, the poly-biasing allows to modulate the effective channel length of transistors from 24 nm up to 40 nm without area overhead [45]. Thanks to the ultra-thin buried oxide of this technology, a wide range of back-gate biasing voltages can be applied to the back-gate of devices to adjust the leakage current and the performance of logic cells. In the logic cells we developed based on the 28 nm FDSOI LVT device in paper V [16], a 46% improvement in the  $I_{on}/I_{off}$  ratio was achieved at the cost of 13% more energy consumption by applying a poly-biasing of 4 nm

to all the logic gates. Moreover, after choosing the minimum used channel width considering NWE, an additional constant forward back-gate biasing (FBB) voltage was applied to the back-gate of PMOS transistors to balance PMOS/NMOS strength ratio.

The logic cells based on the 28 nm FDSOI RVT devices in paper IX [15] were developed for applications with lower throughput requirements and we aimed to reduce the leakage current. Therefore, we created a balance between the NMOS and PMOS drive strength by applying a 16 nm poly-biasing to the NMOS devices. In these logic cells, the NMOS transistors channel length was also increased by 4 nm through the poly-biasing to reduce the leakage current further and improve the functional yield of the cells. We did not apply a reverse bias to the back-gate of PMOS transistors and the back-gate of PMOS transistors had same potential as that of the NMOS transistors [15] (both grounded for normal back-biasing).

#### 2.2.4 *Physical implementation and layout choices*

Layout-induced physical effects have been considered in the layout of all the subthreshold blocks as this has a significant influence on the device matching and manufacturability. To limit systematic shifts in the threshold voltage and mobility of the transistors, both the Well Proximity Effect (WPE) and the STI stress effect [46] have been taken into account. The WPE was mitigated by increasing the gate distances to the well edge. To limit the STI stress effect on the channel mobility and threshold voltage the number of transistors fingers were limited to be less than two [46]. Additionally, we focused on developing very regular layout for subthreshold blocks to increase the matching properties of the devices [47]. In the layout of the logic cells, there is no rounding and routing in the poly layer. Moreover, regular diffusion areas have been drawn in the layout and all the poly polygons have single direction. Well ties are placed close to the devices active area to provide a uniform potential for the channel area or the back-gate of transistors. Figures 2.14 [35] and 2.15 [15] illustrate the representative layout of 1-bit full adders implemented in 65 nm bulk and 28 nm FDSOI technologies.

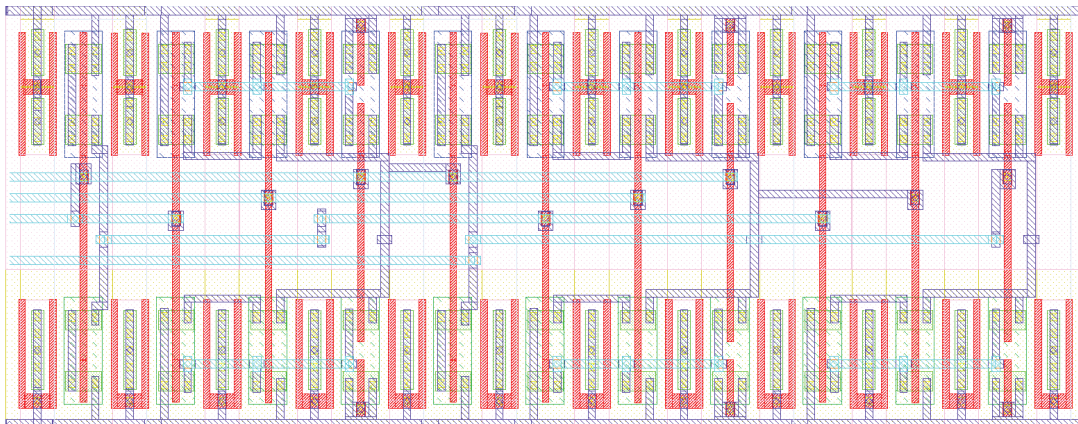


Fig. 2.14: Layout of the 1-bit Full Adder developed in 65 nm [35].

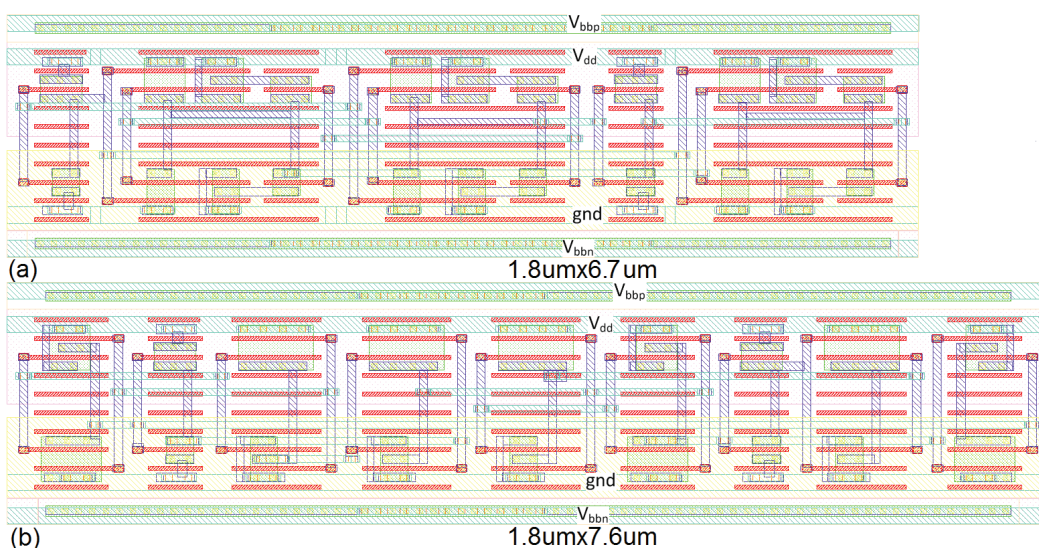


Fig. 2.15: Layout view of the 1-bit full adder (a) implemented with min-3 gates (b) implemented with Boolean gates [15].

### 2.3 Ultra low-power/voltage full adder design

As one of the fundamental components of datapath circuits, the full adder is an important element of digital systems. Therefore, full adders have been considered in the development of ultra-low voltage building blocks of this

thesis both in 65 nm Bulk and 28 nm FDSOI technologies. To have robust circuits we used static CMOS logic gates in the implementation of all the FAs. The ripple carry adder (RCA) topology has been chosen because the energy consumption of the serial adders may be lower than the parallel adders while maintaining the same speed, when operated in subthreshold [48].

### 2.3.1 *FA based on min-3 and Boolean logic gates*

A 16-bit RCA based on Boolean gates and a 32-bit RCA based on min-3 logic gate have been implemented with same device sizing strategy in paper IX [15]. It has been reported in [15] that more samples of RCA based on Boolean gates achieves minimum supply voltage of 110 mV. However, this comes at the cost of higher energy consumption and larger area. Additionally, all the samples of 32-bit and 16-bit RCAs were able to operate correctly down to 125 mV. This is in line with the results in section 2.1.3, which show that the designed min-3 logic gate does not mitigate the functional yield of a subthreshold cell library for supply voltages higher than 130 mV. The minimum operating voltage of all the 32-bit RCA samples in [15] reduced to 80 mV by applying reverse back bias voltages to the back-gate of the PMOS transistors. This indicates that the min-3 logic cells have a robust performance against the mismatch variations.

### 2.3.2 *Characteristics of the RCAs developed in 65 nm and 28 nm*

TABLE 2.2 compares the developed adders in this thesis to the state-of-the-art subthreshold adders. To the best of author's knowledge and up until publication dates of [35] and [15]: I) The minimum operating voltage of 84 mV is the lowest reported supply voltage for static CMOS logic gates [35]. II) The 32-bit adder based on min-3 logic gates in [15] achieved 0.65 fJ per 1-bit addition, which was the lowest reported energy per 1-bit addition based on the measurement results.

### 2.3.3 *MAC and multiplier blocks based on developed FAs*

An 8-bit multiply-accumulate (MAC) was implemented in 28 nm FDSOI using the FAs based on min-3 gates. The MAC is reported in paper V [16]. Comparing specifications of the designed MAC to the state of the art subthreshold MAC blocks, reveals better energy efficiency for the MAC block



Tab. 2.2: Comparison with existing ULV full adders

	[35] paperII	[15] paperIX	[15] paperIX	[49]	[50]	[51]*	[51]*	[52]*
# bits	32	32	16	32	32	32	16	9
technology	65nm	28nm FDSOI	28nm FDSOI	90nm	90nm	28nm FDSOI	28nm FDSOI	28nm FDSOI
$E_{min1-bit}$	1.59fJ*	0.65fJ	0.77fJ	2.96fJ	12.75fJ	6.48fJ	4.68fJ	1.03fJ
Delay@MEP	82.52ns	3.24 $\mu$ s	6.2 $\mu$ s	10 $\mu$ s	52.6ns	0.898 $\mu$ s	0.448 $\mu$ s	0.555 $\mu$ s
$V_{dd}@MEP$	275mV*	300mV	250mV	330mV	190mV	300mV	300mV	240mV
$V_{dmin}$	84mV	110mV	110mV	250mV	190mV	N. A.	N. A.	N. A.

\* Post-layout simulation results.

in [16], so that the speed drop could be overcompensated by increasing the supply voltage. The minimum energy point of the 8-bit MAC block was 0.051 pJ at 275 mV and 5.3 MHz clock frequency.

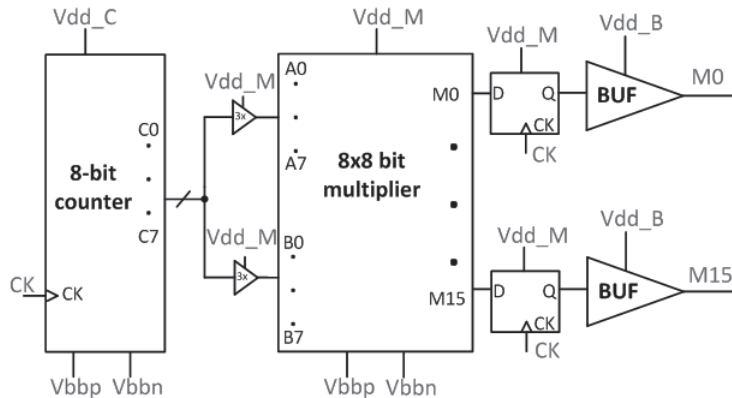


Fig. 2.16: Block Diagram of test circuit for the 8x8 bit multiplier.

An 8x8 parallel multiplier based on the min-3 FAs of paper IX [15] was fabricated in the same 28 nm FDSOI technology. Figure 2.16 shows the block diagram of the circuit that was implemented to test the multiplier. The binary counter generates input test vectors for the multiplier. M0 (LSB output) and M15 (MSB output) output signals are sampled at the rising edge of the clock signal. The outputs of the flip-flops are buffered to the I/O pads using LVT inverter chains. The counter counts from (00000000)<sub>2</sub> to (11111111)<sub>2</sub>. The state of M0 switches at each rising edge of the clock sig-

nal. The M15 output stays at 0 until the input test vector switches from  $(10110101)_2$  to  $(10110110)_2$  and then returns to 0 when the input becomes  $(00000000)_2$  again. Therefore, the frequency of the M0 will be half of the clock frequency and its duty cycle will be 50%. The M15, on the other hand, will have a positive duty cycle of 28.9% and its frequency will be  $1/256$ th of the clock frequency. The race-free flip-flop topology that we presented in paper IV [21] were used in implementation of the multiplier. The imple-

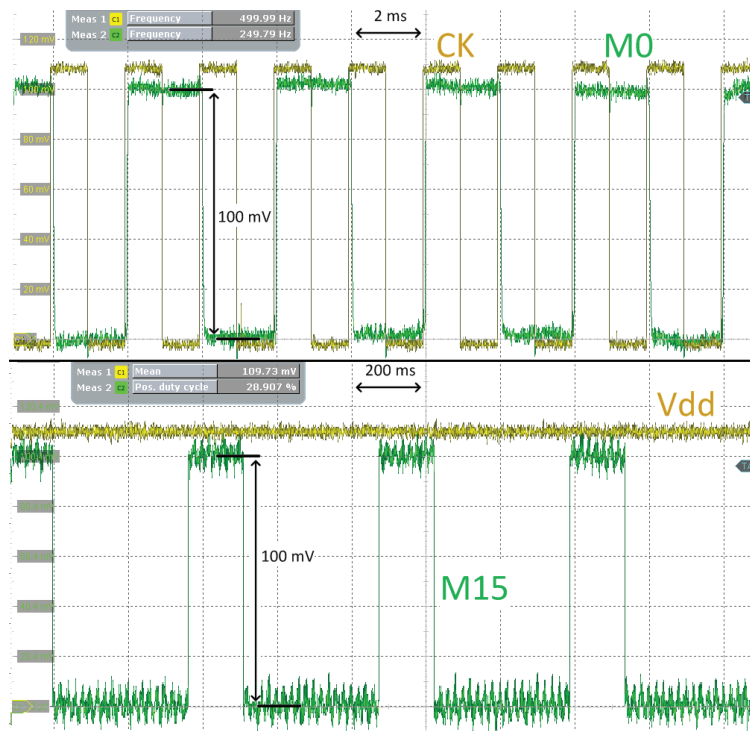


Fig. 2.17: Oscilloscope plots of output signals at a 110 mV supply voltage (a) LSB output of the multiplier (b) MSB output of the multiplier.

mented multiplier was able to operate correctly down to a supply voltage of 110 mV while back-gate of NMOS and PMOS transistors were grounded. Figure 2.17 shows the oscilloscope plots of the MSB and the LSB outputs of the multiplier. To assess the minimum functional voltage of the multiplier, we measure ten chip samples. Figure 2.18 illustrates the minimum  $V_{dd}$  of the adders as a histogram for ten measured samples. According to the measurement results of ten chip samples, the minimum energy per cycle of the



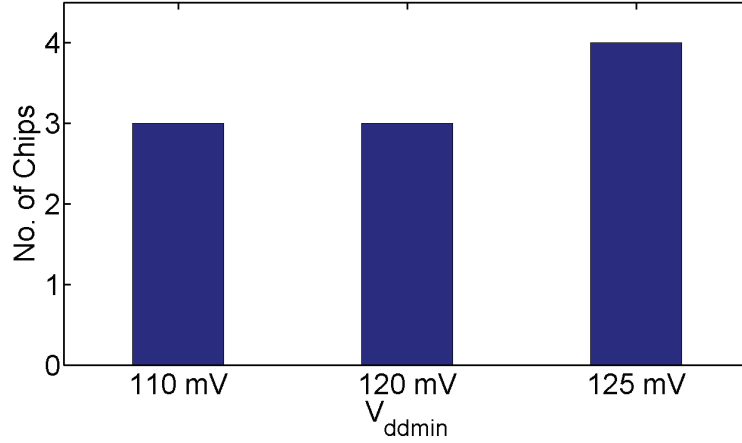


Fig. 2.18: Distribution of the measured minimum functional  $V_{dd}$  of ten samples.

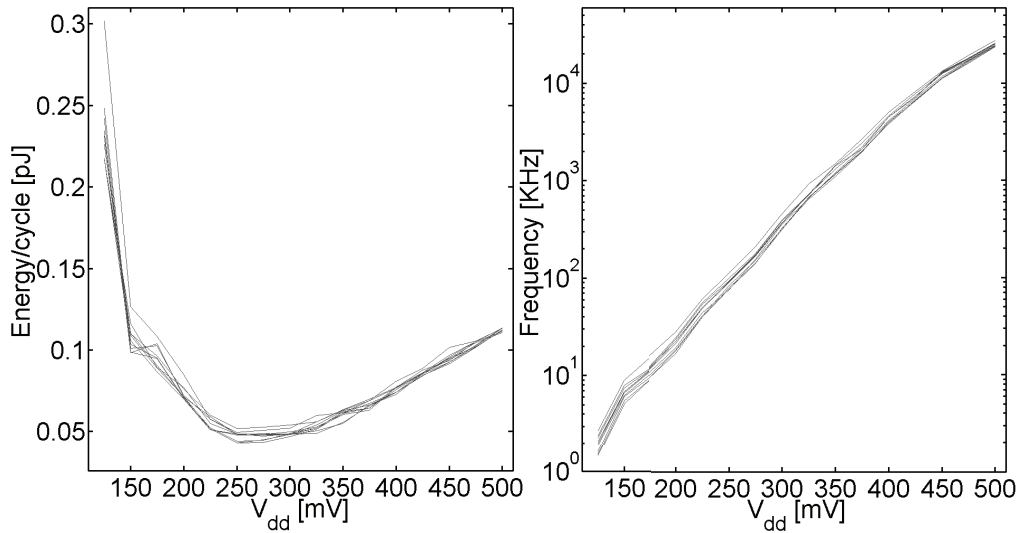


Fig. 2.19: Measured energy per cycle and maximum operating frequency of the multiplier as a function of  $V_{dd}$  for ten samples.

implemented 8x8 multiplier was down to 43 fJ/cycle for the sample with the lowest energy consumption and it had a robust performance. Figure 2.19(a) illustrates the energy dissipation per cycle of 8x8 multiplier versus supply voltage for ten measured chips. For the power measurements of the circuit, the maximum applicable clock frequency for a given supply voltage was ap-

plied. From Figure 2.19(a), the average minimum energy point of ten samples is 47.2 fJ/cycle at 250 mV. The measured maximum operating frequency of ten multiplier samples versus supply voltage is shown in Figure 2.19(b). The

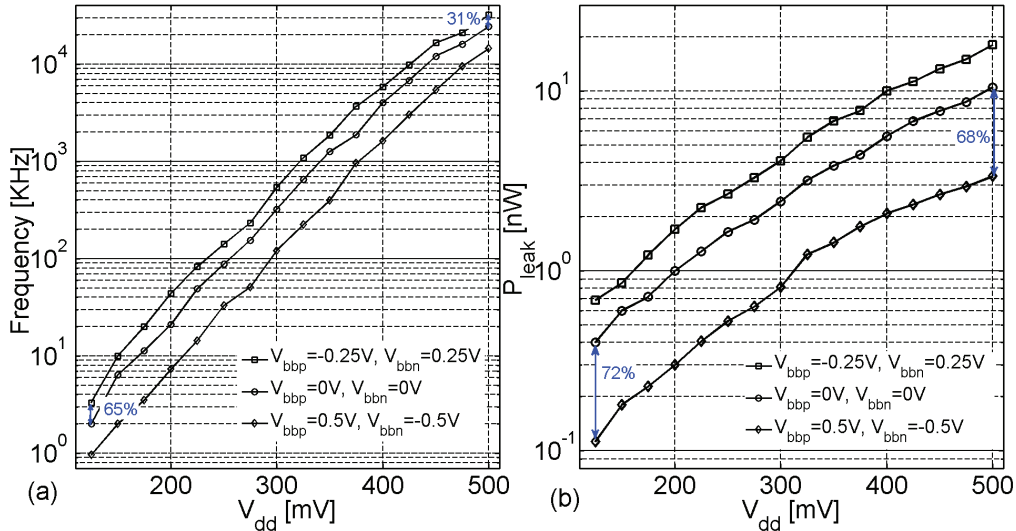


Fig. 2.20: Measured (a) maximum operating frequency and (b) leakage power consumption of multiplier versus  $V_{dd}$  for multiple back-gate bias voltages.

performance and the leakage of the multiplier were investigated for reverse and forward back-gate biasing schemes. To apply a forward back-gate bias, we applied 0.25 V to the back-gate of NMOS transistors ( $V_{bbn}$ ) and -0.25 V to the back-gate of PMOS transistors ( $V_{bbp}$ ). The leakage current through the parasitic PWELL/NWELL diodes was measured to be 31.5 nA in this case with 0.25 V forward back-gate bias. For a forward back-bias voltage of 0.3 V, the voltage drop over the parasitic WELL diodes is 0.6 V and the leakage current through the diodes increases to 1.5  $\mu$ A. Thus, we limited the forward back-gate bias to be 0.25 V. As shown in figure 2.20(a), the maximum operating frequency of the circuit increased by 65% and 31% at supply voltages of 125 mV and 500 mV, respectively. The reverse back-biasing scheme of the multiplier was explored with  $V_{bbn} = -0.5$  V and  $V_{bbp} = 0.5$  V. The leakage current through the parasitic diodes in this case was 1.1 nA. The power consumption due to the parasitic diodes leakage current was not taken into account for calculating power consumption of the multiplier. Figure 2.20(b) illustrates the static power of the circuit with three different back-biasing

schemes. The static power of the multiplier decreases by 72% at 125 mV and 68% at 500 mV by applying a 0.5 V reverse back-gate bias. We did not apply higher reverse back-gate bias voltages because the speed of circuit at lower supply voltages drops drastically with larger reverse back-gate bias voltage. As shown in Figure 2.21, a Verilog-A module was used to analyze the output of the multiplier and check the functionality of the circuit at the low supply voltages. The Verilog-A module compares the outputs of the multiplier with the expected values of multiplication. The F output will be 1 if the output of the multiplier equals the expected value of the multiplication, otherwise it will be 0. To determine the minimum operating supply voltage,  $V_{dd}$  was reduced with 5 mV steps. The multiplier was functional down to a  $V_{dd}$  of 85 mV in both FS and SF process corners.

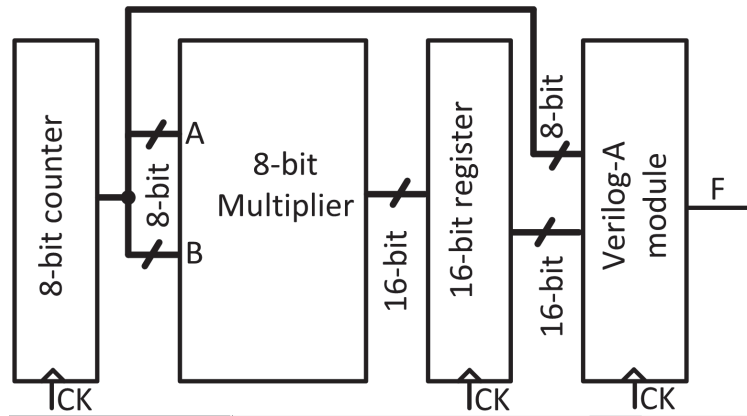


Fig. 2.21: Test-bench to apply stimuli to the multiplier circuit and analyze its output to verify functionality of the circuit.

#### 2.4 Design considerations for ultra-low voltage flip-flops

Flip-flops are the fundamental elements of synchronous systems and are reported to have a significant impact on power and robustness of the digital systems [53]. Sequential elements are more susceptible to PVT variations in comparison to combinational logic gates. Conventional master-slave flip-flops operating with true and complementary clock phases have drawbacks such as: a) High dynamic power consumption due to the redundant toggling of local clock inverters; b) Sensitivity to the overlap between clock and its

complement when the slope of the clock is not high [54]. These disadvantages of the master-slave DFFs with two-phase clocking schemes make them less attractive to be used in ultra-low voltage applications [55]. A PowerPC 603 D flip-flop is shown in Figure 2.22 as an example of a generic master-slave flip-flop to show contention in its internal nodes. 28 nm FDSOI technology was used to implement the DFF in Figure 2.22. RVT devices were used and  $L_n=30+16$  nm (poly-biasing of 16 nm),  $L_p=30+4$  nm (poly-biasing of 4 nm),  $W_n=200$  nm and  $W_p=300$  nm.

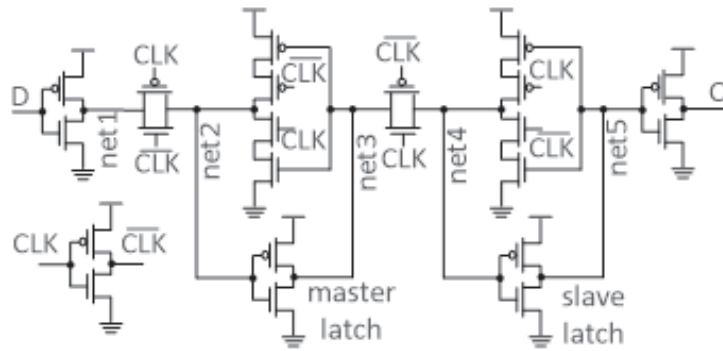


Fig. 2.22: Conventional PowerPC 603 D flip-flop.

As the clock slope is not high at ULV domain, one challenge of using DFFs with two clock phases is that the overlap between the main clock and inverted clock signals might cause a contention in the internal nodes of a master-slave flip-flop and consequently results in a functional failure. Figure 2.23 demonstrates the race condition between the inverter of the master latch and the clocked inverter of the slave latch. In Figure 2.23 example, before the falling edge of the clock both net3 and net4 are high and when clock is low net4 remains at high and net3 switches to low. However, due to the clock-overlap at the falling edge of the clock signal, the PMOS transistor of the second transmission gate and the PMOS transistor of the clocked inverter in the slave latch are simultaneously on for a short period of time. This results in a race condition at node net4 where the inverter of the master latch tries to pull it down and the clocked inverter of the slave latch tries to keep it at logic-1. An inverter was added between the master latch and the second

transmission-gate of the PowerPC 603 DFF (see figure 2.22) to delay the turn-on of the master latch and avoid reverse current flow and hence mitigate the contention [31]. Additionally, the overlap time between CLK and CLKb signals depends on the slope of the input clock signal and is susceptible to PVT variations. This increases sensitive of master-slave DFFs to the slope of the input clock signal [54]. Larger or more clock tree inverters are required to make sure that clock slope is steep enough in the sinks, which in turn, results in a higher power consumption or a larger clock skew, respectively.

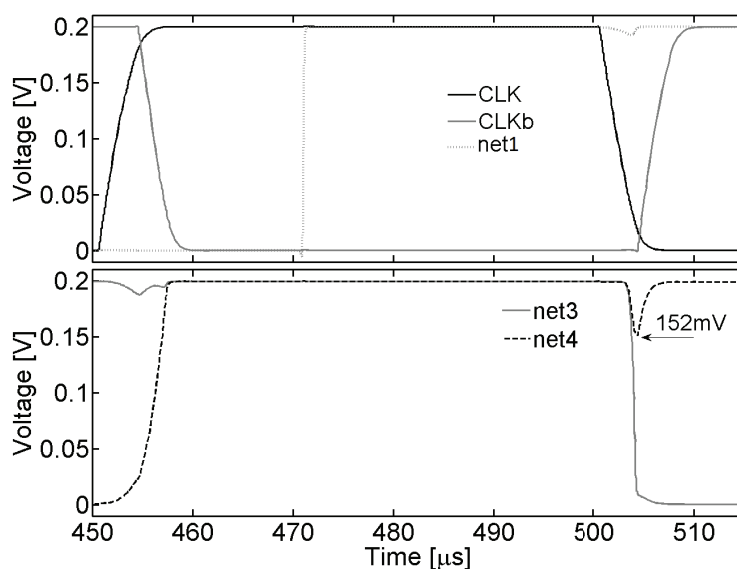


Fig. 2.23: Sensitivity to clock overlap in 603 D flip-flop.

The race-free single-phase clocked D flip-flop (R-DFF) structure, introduced in [56], was used in the ULV logic cell libraries developed in this thesis. The circuit topology of a rising edge triggered race-free D flip-flops is shown in figure 2.24. A falling edge triggered version can be implemented by replacing all the NAND gates with NOR gates. Four extra transistors are required to add an asynchronous reset signal to these flip-flops. The measurement results of a divide-by-3 circuit implemented based on different versions of this DFF topology [21] (paper IV) confirm its functionality in ultra-low voltages domain down to 132 mV. The operation principle of the positive edge triggered

DFF in figure 2.24(a) is that when  $CK=0$  the outputs of gate3 and gate4 are 1 and the output of these gates will not change with changes in net2, thus the state of the output latch (gate5 and 6) will not change. For  $CK=1$ , D signal flows through the gate1, gate2 and inverter and changes the state of net3 or net4 to 0 this in turn changes the output latch state. As net3 or net4 discharged to 0 the output of gate2 or gate1 will be tied to Vdd, hence net2 will be completely isolated from changes in D.

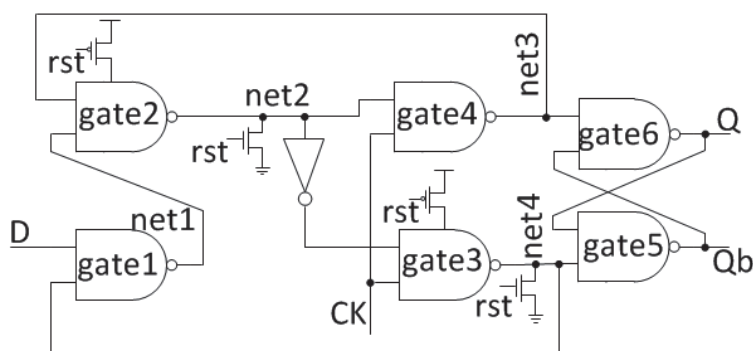


Fig. 2.24: Race-free single-phase clocked D flip-flop with asynchronous reset.

We have made a comparison between nine D-type flip-flops in paper VII [23]. According to the results reported in [23], the race-free (R-free) flip-flop has the second smallest core area and the second lowest energy per cycle (E/cycle) after the pass gate DFF. However, the pass gate DFF does not have a high yield compared to the other DFFs in Table 2 of paper VII [23]. According to the results presented in paper VII [23], the race-free DFF is among the flip-flops with low hold time and set-up time variations. It is worth mentioning that the applied clock signal to the flip-flops during the simulations in [23] had relatively sharp edges as it was buffered through two inverters and the load of the buffer was only a single flip-flop. Recall that the master-slave DFFs with two clock phases are more sensitive to the clock slew and longer transition times increases overlap between the clock and its complement.

The number of transistors in the race-free DFF can be reduced by merging the logically equivalent transistors [57]. In figure 2.24, the NMOS transistors of gate3 and gate4 with gate terminals connected to the clock can be shared. By the same token, the NMOS transistors in gate2 and gate6 with gate terminals connected to net3, and the NMOS transistors in gate1 and gate5 with

gate terminals connected to net4, can be merged. Therefore, total number of the transistors in the R-free DFF can be reduced to 23 devices. I avoided transistor sharing during the DFF development as we aimed at having layouts based on identical patterns to increase the regularity of the logic cells. The custom library cells, introduced in paper V [16], was expanded by adding hold buffers for fixing hold-time violations and specialized inverters to be used in the clock tree.

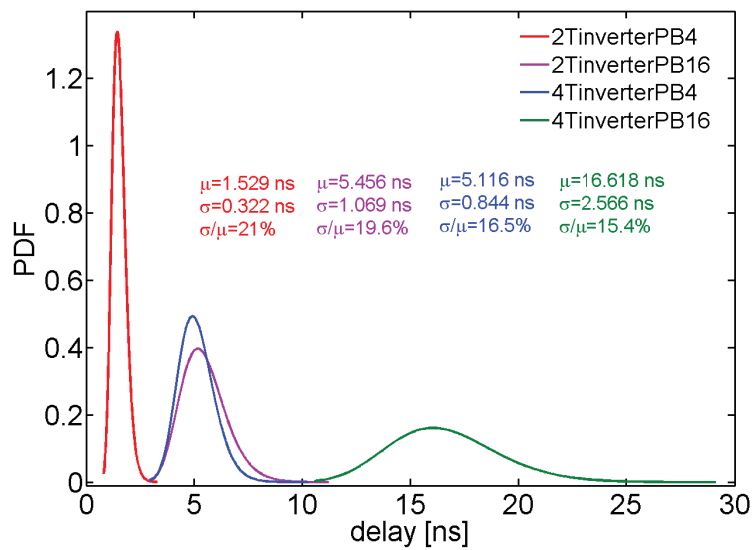


Fig. 2.25: Delay distributions of four different inverters.

As presented in paper I [18], the stacked logic cells have larger delay and less delay variability compared to the conventional static CMOS logic cells. Therefore, the stacked inverters together with a slight increase in the gate length were added to the library cell to be used in buffering for fixing hold-time violations. The gate length of logic cells in the developed custom cell library [16] have increased by 4 nm to improve  $I_{on}/I_{off}$  ratio of the cells. Another inverter with 16 nm poly biasing was also added to the library for fixing hold-time violations. Figure 2.25 shows delay distribution of different version of inverters. 2T-inverter-PB4 is a 2-transistors inverter with 4 nm poly biasing. 2T-inverter-PB16 is a 2-transistors inverter with 16 nm poly biasing. T-inverter-PB4 is an inverter with 4 stacked transistors and 4 nm poly biasing. 4T-inverter-PB16 is an inverter with 4 stacked transistors and

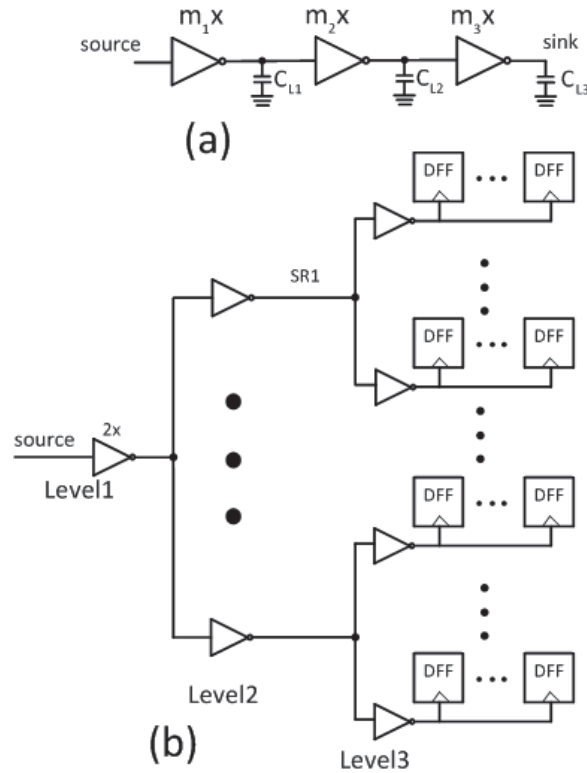


Fig. 2.26: 3-level clock tree clock tree architecture.

16 nm poly biasing.

Tab. 2.3: Parasitic capacitance and number of inverters at each level of the clock tree.

INVs@ Level-2	INVs@ Level-3	CL1 [fF]	max/min CL2[fF]	max/min CL3[fF]	Skew [ns]
2INVx4	6INVx16	13.7	28.7/27.2	98.2/89.2	0.6

It is shown in [58] that in ultra-low voltage (ULV) domain, wires resistance is negligible compared to the devices on-resistance. Consequently, developing clock networks with few levels of clock hierarchy and large buffers for sub-modules result in less clock skew imposed by clock buffers mismatch.



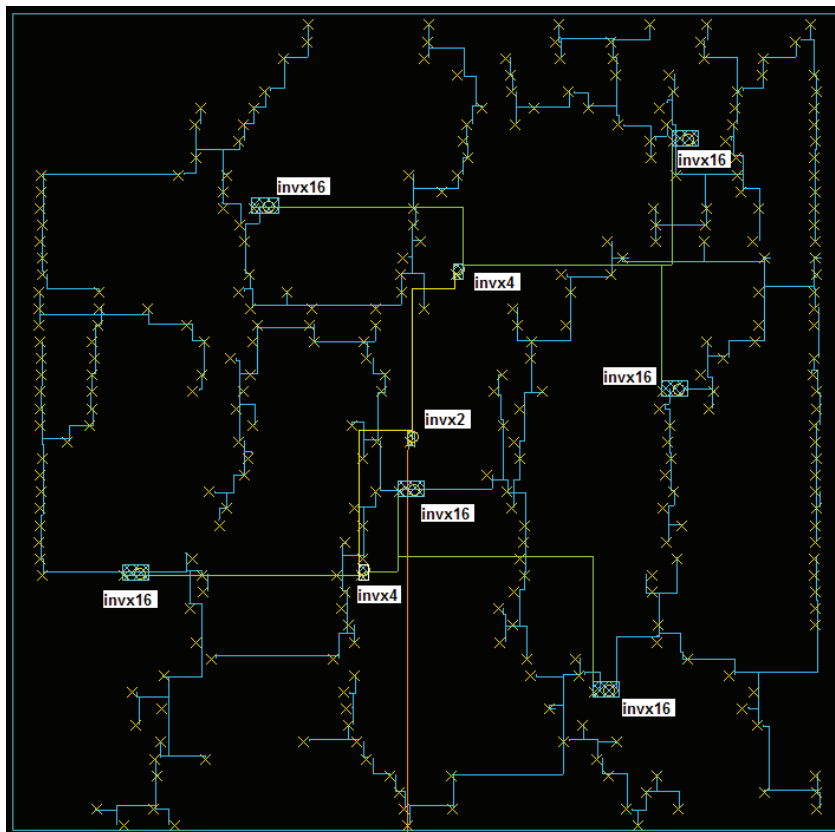


Fig. 2.27: 3-level clock tree routed for a pipeline multiplier with 296 sinks.

However, as demonstrated in [59] and [60], input slew variations can result in larger buffer delay variations, and hence, larger clock skew. Therefore, clock slew rate must be taken into account during the clock tree design in ULV domain.

As shown in figure 2.26, a 3-level clock-tree is designed for a 16-bit pipeline multiplier [61] with 296 sinks (i.e. flip-flops). Table 2.3 lists parasitic capacitance, number of inverters at each level, drive strength of inverters and estimated deterministic clock skew achieved from place and route tool (Cadence Encounter) for the developed clock network. Layout view of the routed clock tree for a 16-bit pipeline multiplier is shown in figure 2.27.

Figure 2.28, shows clock signals at the sinks of the 16-bit pipeline multiplier. An extracted netlist of the multiplier was used to draw the clock signal at

the sinks. The worst interconnect corner (RC-max) was used during the extraction. The maximum deterministic clock skew from Figure 2.28 is 0.8 ns. To estimate the statistical clock skew, clock paths with minimum and maximum delays were extracted from the place and route tool. The benchmark in Figure 2.29 was used to calculate the statistical clock skew of the implemented clock tree. 3000 Monte Carlo runs were carried out at typical process corner and 300 mV supply voltage. Figure 2.30(a) shows the clock skew distribution at 300 mV. The distribution of the slew-rate at the sink of the maximum clock path is shown in 2.30(b).

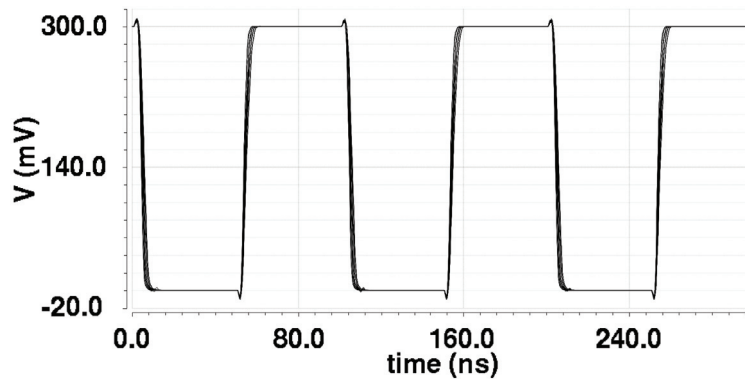


Fig. 2.28: Deterministic clock skew.

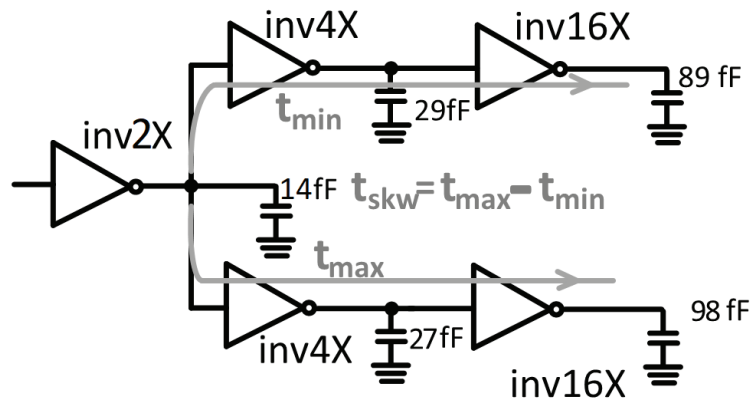


Fig. 2.29: Benchmark for statistical clock skew analysis.

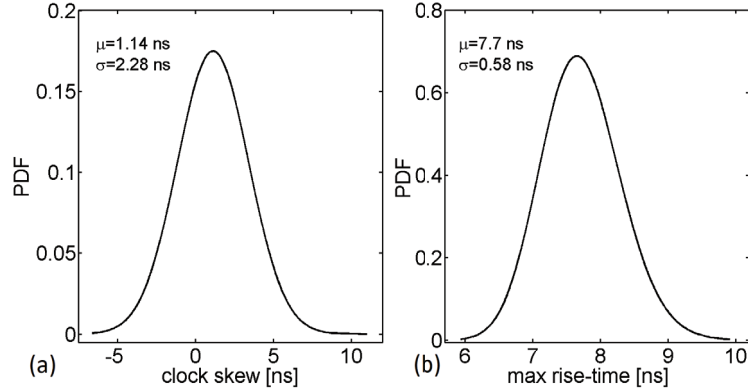


Fig. 2.30: Statistical clock skew and slew

### 2.5 Subthreshold level-shifter design

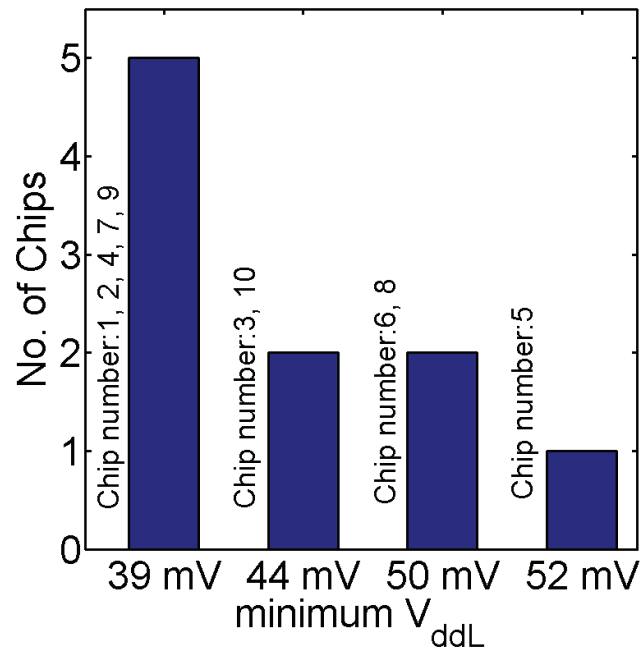


Fig. 2.31: Measured minimum  $V_{ddL}$ s of ten LS samples as a histogram.

Multiple voltage domains are usually employed to address issues such as speed, area and robustness of ultra-low voltage and ultra-low power systems.

---

Level-shifters (LS) are essential blocks to ensure correct signal communication between different voltage levels. For example, more than hundred level-shifters were used in [6] to communicate between 14 voltage domains including an ARM Cortex-M0+ processor which had a minimum operating voltage of 250 mV. Energy harvesting systems scavenge energy from extremely low-input voltage levels. A robust level-shifter capable of up-converting extremely low-voltage levels can be used to drive the charge-pump switches [62] in energy harvesting systems.

In paper X [25], we presented an energy efficient level-shifter with ability to upconvert sub-50mV input voltage to nominal 1 V. The top diode connected devices are proposed to be used along with the current-limiter diodes. Additionally, a single-NWELL (SNW) configuration together with backgate and poly biasing techniques create an adequate balance between the drive strength of PUN and PDN.

The distribution of the minimum convertible  $V_{ddL}$  for ten measured chip samples is shown in figure 2.31. Five samples were able to up-convert a 39 mV input to 1V while the minimum convertible input voltage level was 52 mV for one sample. At 0.2 V and 1 MHz, the energy per switching and the delay of the design LS was 5.2 fJ and 10.1 ns, respectively.

### 3. CONCLUSION

This thesis focused on developing ultra-low voltage building blocks for power and energy efficient systems. Design considerations for development of ultra-low voltage and robust logic cell libraries demonstrated throughout this thesis at different abstraction levels. We developed building blocks in 65 nm bulk and 28 nm FDSOI technologies including logic cells, full adders, flip-flops and a level-shifter. The logic cell library based on low-threshold 28 nm FDSOI devices (reported in paper V) extended by adding delay elements for fixing hold-time violations and inverters to be used for developing a robust and low-power clock tree.

In 65 nm bulk technology, we designed logic cells based on thin-oxide (paper II) and thick-oxide (paper III and IV) transistors. Reverse short-channel effect and inverse narrow width effect were considered in the design of the logic cells to improve the robustness and energy efficiency of the cells. Moreover, different threshold voltage flavors examined to meet the required performance or power consumption. We also utilized very regular layout techniques to improve manufacturability of the cells. The developed logic cells were used in implementation of the full-adders and flip-flops. The measurement results were reported in papers II, III and IV.

In 28 nm FDSOI technology, we developed logic cells based on low-V<sub>t</sub> (flipped well) and regular-V<sub>t</sub> devices. The low-V<sub>t</sub> based library cell was reported in Paper V and are proper for applications where the circuit throughput can be an important parameter. Logic cells based on the regular-V<sub>t</sub> devices were reported in Paper IX. These cells are appropriate for applications with more relaxed throughput requirements. For the 28 nm FDSOI cells, we used knobs such as back-gate biasing and poly biasing and the narrow width effect was taken into account to have a good balance between area and robustness of the cells. An ultra-low voltage and energy efficient level-shifter with a single-NWEL layout was also implemented in 28 nm FDSOI technology and reported in Paper X.

To the best of author's knowledge: 1) the minimum operating voltage of 84 mV in Paper II was the lowest reported supply voltage for the static CMOS logic gates. 2) The 32-bit adder based on min-3 logic gates in Paper IX achieved the lowest reported energy per 1-bit addition of 0.65fJ. 3) the level-shifter in Paper X achieved the lowest reported  $V_{ddL}$  of 39 mV. We also showed a very robust performance for the flip-flop cells. According to the measurement results presented in Paper IV, the minimum operating voltage of 132 mV was achieved for a divide-by-3 circuit which was implemented using the race-free flip-flop structure. The same flip-flop topology was used in the implementation of the reported 8x8 multiplier in section 2.3.3.

## 4. PUBLICATIONS

4.1 *paper I*

**Modular Layout-friendly Cell Library Design Applied  
for Subthreshold CMOS**

Conference publication presented at IEEE NORCHIP 2014.

Publication date: 08 January 2015.

This paper is not included due to copyright available at  
<https://doi.org/10.1109/NORCHIP.2014.7004747>









4.3 *paper III*

**Exploiting short channel effects and multi-V<sub>t</sub> technology for increased robustness and reduced energy consumption, with application to a 16-bit subthreshold adder implemented in 65 nm CMOS**

Conference publication presented at IEEE European Conference on Circuit Theory and Design (ECCTD-2015).  
Publication date: 19 October 2015.

This paper is not included due to copyright available at <https://doi.org/10.1109/ECCTD.2015.7300053>



4.4 *paper IV*

**4 Sub-/near-threshold flip-flops with application to frequency dividers**

Conference publication presented at IEEE European Conference on Circuit Theory and Design (ECCTD-2015).

Publication date: 19 October 2015.

This paper is not included due to copyright available at <https://doi.org/10.1109/ECCTD.2015.7300058>



4.5 *paper V*

**28 nm UTBB-FDSOI energy efficient and variation tolerant custom digital-cell library with application to a subthreshold MAC block**

Conference publication presented at IEEE 23rd International Conference Mixed Design of Integrated Circuits and Systems (2016 MIXDES).

Publication date: 04 August 2016.





# 28 nm UTBB-FDSOI Energy Efficient and Variation Tolerant Custom Digital-Cell Library with Application to a Subthreshold MAC Block

Ali Asghar Vatanjou, Trond Ytterdal, Snorre Aunet

Department of Electronics and Telecommunications, Norwegian University of Science and Technology

O. S. Bragstads Plass 2 A, 7491 Trondheim, Norway

Email: ali.vatanjou@iet.ntnu.no

**Abstract**—This paper presents the design of digital logic cells for subthreshold applications using 28 nm ultra-thin body and box fully depleted silicon on insulator technology. The sizing approach relies on balancing pull-up/pull-down networks (PUN/PDN) strength ratio by applying an additional forward back-gate biasing (FBB) voltage to the back-gate of PMOS transistors. The minimum width of PMOS and NMOS transistors have been chosen by taking the narrow width effect into account. Moreover, to increase the functional yield of the logic cells, a trade-off has been made between  $I_{on}/I_{off}$  ratio and energy consumption through increasing the channel length by 4 nm. Energy consumption of logic gates analyzed using ring-oscillators consisting of basic logic gates. It has been shown that balancing logic gates through applying an additional FBB to the PMOS back-gate instead of up-sizing PUN results in 30% lower energy consumption in ring-oscillators. An 8-bit multiply-accumulate (MAC) block was synthesized using the fully customized logic cells with asymmetric back-gate biasing. Compared to a state-of-the-art MAC, the energy consumption of our MAC was improved by 21% at a relatively high speed (147 MHz).

**Index Terms**—Subthreshold, CMOS FDSOI, back-gate biasing, Low-power/voltage.

## I. INTRODUCTION

Various process techniques have been introduced to reduce short channel effects in CMOS devices. Among them, the ultra-thin body and box (UTBB) fully depleted silicon on insulator (FDSOI) technology is one of the potential technologies to continue the CMOS technology roadmap. Lower random dopant fluctuations (RDF) and reduced short channel effects such as higher subthreshold slope and lower drain induced barrier lowering (DIBL) make this technology a proper choice for ultra-low voltage (ULV) applications [1]. Additionally, UTBB-FDSOI provides effective knobs such as back-gate biasing (BB) and poly biasing, which helps designers to make trade-offs between power, speed and area [2].

In this paper, the design of logic cells for subthreshold applications is demonstrated using 28 nm UTBB-FDSOI technology. Dimensioning of the logic cells has been done in different steps. As variability is the primary concern in subthreshold design, device dimensions have been chosen to be larger than minimum allowed dimensions to mitigate variability of the cells. In the first step, the gate length of the transistors was increased by 4 nm using poly-biasing. This leads to a trade-off between energy consumption and noise margin where

with 13.4% more energy consumption 46% improvement in  $I_{on}/I_{off}$  ratio of the transistors was achievable. Threshold voltage of 28 nm UTBB-FDSOI transistors decreases with increasing the device width owing to the Narrow Width Effect (NWE). In the second step, a minimum width for PMOS and NMOS transistors was chosen considering threshold voltage variations versus devices width to reduce threshold voltage variations due to NWE. Subsequently in third step, an additional constant FBB voltage was applied to the back-gate of PMOS to balance PMOS/NMOS strength ratio.

Various back-gate biasing schemes of the FDSOI technology have been discussed in [3] and it has been shown that adaptive and inverse adaptive BB schemes are very effective approaches to cancel systematic mismatch between PMOS and NMOS in subthreshold region. However in [3], different BB schemes on commercial standard cell library are investigated at schematic level. In this paper, we developed a full custom cell library at layout level. Moreover, we will demonstrate that with a constant additional BB voltage applied to the back-gate of the PMOS, strength ratio of the PMOS and NMOS can be modified over a  $V_{dd}$  range from 0.15 V to 0.4 V and back-gate voltage from -400 mV to 900 mV. Therefore, the design of on-chip body bias generator [4] is more straightforward because additional back-gate biasing voltage which is applied to the PMOS is constant over  $V_{dd}$  and BB voltages. Ring-oscillators made of basic logic gates used to evaluate energy consumption of the logic gates. Logic gates sized to have maximum Static Noise Margin (SNM) using symmetric and asymmetric back-gate biasing schemes. SPICE simulations confirmed that energy per operation of the ring-oscillator with asymmetric back-gate biasing was improved by 30% compared to energy per operation of the ring-oscillator with symmetric back-gate biasing. We synthesized an 8-bit MAC using the developed costume cell library. The designed MAC was compared to the other subthreshold MACs [5], [6] and [7]. The MAC presented in this work achieves lower energy and EDP (21% and 24% saving, respectively) at 147 MHz operating frequency compared to the MAC in [7].

In this paper, first we will describe logic cells dimensioning. The back-gate biasing scheme is discussed in section III. In section IV, the design of sequential element is shown. Section V presents design of an 8-bit MAC block.

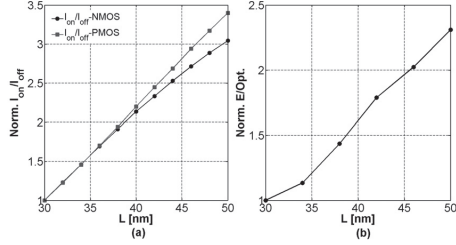


Fig. 1. (a)  $I_{on}/I_{off}$  ratio of NMOS and PMOS vs.  $L$  (b) Energy per operation of the ring-oscillator vs.  $L$  ( $V_{ds}=200$  mV).

## II. DEVICE SIZING

### A. Increasing the channel length to improve $I_{on}/I_{off}$

In subthreshold region, the  $I_{on}/I_{off}$  ratio of transistors decreases exponentially with  $V_{dd}$ . A lower  $I_{on}/I_{off}$  ratio reduces functional yield of the circuit, especially at ultra-low supply voltages. Increasing channel length usually increases the  $I_{on}/I_{off}$  ratio of transistors as shown in Figure 1 (a). Nevertheless, longer channel length results in more parasitic capacitance and consequently higher energy consumption. Figure 1 (b) shows normalized energy per operation of a ring-oscillator versus channel length at 200 mV. A logic depth of 11 was chosen for the ringoscillator to have noticeable leakage energy. For all the channel lengths, switching voltage of the inverters is adjusted at  $V_{dd}/2$  to have maximum SNM. From Figure 1 (a) and (b), with increasing the channel length by 4 nm, the  $I_{on}/I_{off}$  ratio of both the PMOS and NMOS transistors increases by 46% at the expense of 13.4% more energy per operation of the ring-oscillator. Therefore, we chose to increase the channel length of all the transistors by 4 nm using poly-biasing.

### B. Narrow width effect (NWE)

Logic cells operating in subthreshold region are very susceptible to threshold voltage variations due to exponential dependencies between the drain current and threshold voltage [8]. It is well-known that upsizing the devices results in less threshold voltage variations [9]. However, wider device widths results in increased parasitic capacitance and consequently higher energy consumption. Therefore, it is of crucial importance to make a good trade-off between variability and energy consumption of the circuit. The mechanism of device threshold voltage shift as a function of channel width depends on the isolation oxide structure [10], [11]. For example, in bulk CMOS technologies used in [12], threshold voltage of the device increases as channel width increases. In contrast, the threshold voltage decreases with channel width increment in 28 nm FDSOI technology used in this work. In this paper, we chose a minimum width for PMOS and NMOS considering NWE. Figure 2 shows PMOS and NMOS transistors threshold voltage shift versus transistor channel widths with  $V_{ds}=200$  mV and  $L=34$  nm. In order to alleviate threshold voltage variations due to lithography effects on matching property of the transistors, a minimum gate width is selected considering threshold voltage

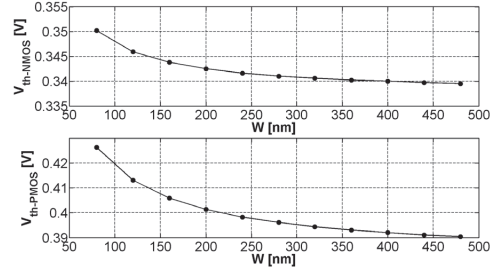


Fig. 2. Threshold voltage shift of PMOS and NMOS as a function of channel width,  $V_{ds} = 0.2$  V and  $L=34$  nm.

shift as a function of PMOS and NMOS widths in Figure 2. As with wider devices a large energy overhead is traded off with a small reduction in threshold voltage fluctuations, the minimum PMOS and NMOS widths are selected to be 270 and 200 nm, respectively. Figure 3 illustrates drain current variability of PMOS and NMOS versus channel width for 2000 Monte-Carlo runs at 0.2 V. The number of MC runs was chosen to be 2000 because this is sufficient for  $3\sigma$  verification [13]. Threshold voltage variations are in inverse proportion to the active area of the device (i.e.  $\sigma(V_t) \propto 1/\sqrt{W \cdot L}$ ) and it obeys a Gaussian distribution. Accordingly as shown in Figure 3, drain current variability of the transistors decreases with increasing channel width. However, the slope of the drain current variability reduction decreases as channel width increases. This implies that for wider transistors, robustness of the circuit is achieved at the expense of higher energy consumption.

## III. BACK-GATE BIASING

### A. FDSOI back-biasing mechanism

In the 28 nm FDSOI technology used in this work, RVT and LVT transistors are made by conventional and flipped wells. Because the buried-oxide (BO) isolates the drain and source nodes from wells, threshold and breakdown voltages of the PWELL to NWELL diode determine the back-gate biasing voltage range [4]. In order to apply a FBB voltage to LVT device (flipped well), a positive voltage must be applied to NMOS back-gate (NWELL) and a negative voltage must be applied to the back-gate of PMOS (PWELL). Thus, PWELL to NWELL diode is reverse biased and the breakdown voltage of diode is the limiting factor in forward biasing scenario of

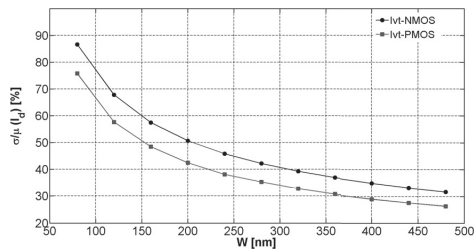


Fig. 3. PMOS and NMOS drain current variability vs.  $W$  ( $V_{dd} = 200$  mV).

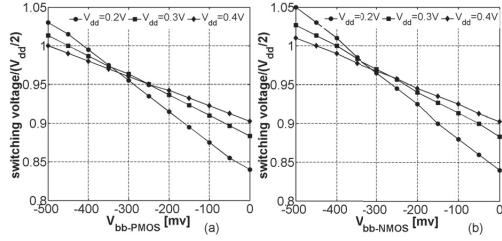


Fig. 4. Normalized switching voltage of inverter versus (a) PMOS back-gate bias and (b) NMOS back-gate bias.

the LVT device. In the reverse biasing scenario of the LVT device, a negative voltage is applied to the NWELL and a positive voltage is applied to the PWELL, thus the threshold voltage of PWELL to NWELL diode is the limiting factor. For the RVT device, the break-down and threshold voltages of the PWELL to NWELL diode are limiting factors in reverse and forward biasing scenario, respectively. Therefore, LVT device is forward bias oriented and RVT device is reverse bias oriented.

#### B. Asymmetric Back-gate Biasing

Subthreshold circuits suffer from output levels deviation resulting from degraded  $I_{on}/I_{off}$  ratio and higher susceptibility to the process, voltage and temperature (PVT) variations. Furthermore, there are some applications where lower operating voltages are desired, e.g. minimum energy point (MEP) voltage can be reduced by using a super-pipelined structure [14]. Therefore, balancing the PUN/PDN ratio is of crucial importance in subthreshold applications.

In [3], it had been shown that the rise and fall times of the logic cells can be balanced through applying an asymmetric voltage to the PMOS or NMOS back-gates. If  $V_{BB}$  is the back-gate bias voltage, this can be explained by  $V_{BB\ NMOS} = V_{BB}$  and  $V_{BB\ PMOS} = -V_{BB} - V_{add}$ .  $V_{add}$  is an additional voltage which is required to be applied to the back-gate of PMOS to balance strength ratio of PMOS/NMOS. We will find the required  $V_{add}$  to have balanced PUN/PDN, by balancing the switching voltage of an inverter at  $V_{dd}/2$ . As discussed in Section III, the inverter dimensions are  $L_n=L_p=34$  nm,  $W_p=270$  nm and  $W_n=200$  nm. Figure 4 (a) and (b) illustrate normalized switching voltage of the inverter versus back-gate voltages of PMOS and NMOS at three different supply voltages. If the back-bias voltage is only applied to the PMOS back-gate and  $V_{BB\ NMOS} = 0$  (See Figure 4 (a)), PMOS is forward biased and for  $V_{BB\ PMOS} = -400$  mV the maximum deviation of the switching voltage of the inverter from  $V_{dd}/2$  is 2% for three different supply voltages. If NMOS is reverse biased and  $V_{BB\ PMOS} = 0$  (See Figure 4 (b)), again for  $V_{BB\ NMOS} = -400$  mV the maximum deviation of switching voltage of the inverter from  $V_{dd}/2$  is only 1% for three different supply voltages. Therefore with an additional constant voltage ( $V_{add}$ ) of 400 mV applied to the back-gate of PMOS, the PUN and PDN networks strength ratio can be

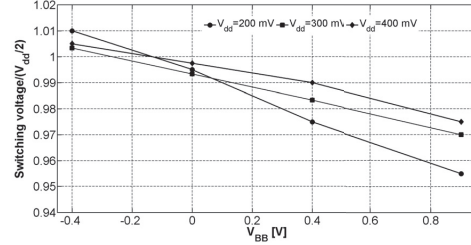


Fig. 5. Switching voltage of the inverter vs.  $V_{BB}$  for three different  $V_{dd}$ s.

balanced in the subthreshold region. With a 400 mV additional voltage at the back-gate of PMOS, if a back bias voltage ( $V_{BB}$ ) is applied to the circuit,  $V_{BB\ PMOS} = -(V_{BB} + 0.4)V$  and  $V_{BB\ NMOS} = V_{BB}$ . Since the models provided by the foundry are evaluated up to 1.3 V forward bias for the technology used here, we will apply maximum  $V_{BB}$  of 0.9 V to the back-gate of transistors, i.e.  $V_{BB\ PMOS} = -1.3V$  and  $V_{BB\ NMOS} = 0.9V$ . Moreover, to avoid turning PWELL to NWELL diode on, the smallest reverse back bias voltage is  $-0.4$  V, i.e.  $V_{BB\ PMOS} = 0V$  and  $V_{BB\ NMOS} = -0.4V$ .

Figure 5 shows shift of switching voltage of the inverter versus back-gate bias voltage ( $V_{BB}$ ) for three supply voltages. As depicted in Figure 5, the worst-case deviation of the switching voltage of the inverter from  $V_{dd}/2$  is below 4.5%. The worst case deviation occurs when maximum forward biasing ( $V_{BB} = 0.9V$ ) is applied to the inverter. Also, this deviation is 1% for extreme reverse biasing ( $V_{BB} = -0.4V$ ). If only 2-input logic gates are included from a library, the worst-case for verifying logic gates output deviation is as shown in Figure 6(a) [15]. Figure 6(b) shows average and standard deviation of SNM versus  $V_{dd}$  for 2000 MC runs including both mismatch and process variations. As can be seen from Figure 6(b), at 150 mV  $\sigma/\mu = 0.39$ , and hence, the corresponding probability of functional failure is 1.1%. At  $V_{dd} = 200$  mV,  $\sigma/\mu = 0.2$ , and hence, corresponding probability of failure is 0 for supply voltages larger than 200 mV.

In order to compare energy consumption of the logic cells with an asymmetric back-gate biasing scheme to logic cells with symmetric back-gate biasing scheme, the energy per operation of two ring oscillators are compared. The ring-oscillators consist of 55 basic logic gates including inverter, NOR-2 and NAND-2 gates to emulate the critical path of the 8-bit MAC. Table 1 lists dimensions of logic gates balanced

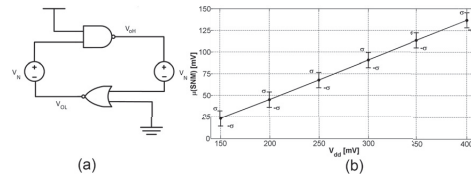


Fig. 6. (a) test-bench to measure SNM. (b) SNM versus  $V_{dd}$  (2K MC runs).

TABLE I  
DIMENSIONS OF LOGIC GATES USED IN RING OSCILLATORS  
( $L_p = L_n = 34nm$ )

Gate		INV	NAND2	NOR2
Asymmetric BB	$W_p$ [nm]	270	275	460
	$W_n$ [nm]	200	420	200
Symmetric BB	$W_p$ [nm]	490	485	840
	$W_n$ [nm]	200	420	200

for maximum SNM with asymmetric and symmetric back-gate biasing schemes. Note that as described in the previous section, the minimum width of PMOS in both biasing schemes is 270 nm and the minimum width of NMOS is 200 nm. As shown in Figure 7, the energy per operation of the ring-oscillator made of asymmetrically biased logic gates is improved in forward and reverse back-gate biasing schemes. The operating frequency range of the ring-oscillators is achieved by sweeping  $V_{dd}$  from 0.15 V to 0.4 V. With  $V_{BB} = 0V$  (i.e.  $V_{BB PMOS} = -0.4V$  and  $V_{BB NMOS} = 0$ ), the minimum energy of the ring oscillator with asymmetric back-biasing scheme is decreased by 29%. With maximum forward back biasing (i.e.  $V_{BB} = 0.9V$ ,  $V_{BB PMOS} = -1.3V$  and  $V_{BB NMOS} = 0.9V$ ), the minimum energy of the ring oscillator with asymmetric back-gate biasing scheme is decreased by 31%. With extreme reverse back biasing (i.e.  $V_{BB} = -0.4V$ ,  $V_{BB PMOS} = 0V$  and  $V_{BB NMOS} = -0.4V$ ), the minimum energy of the ring oscillator with asymmetric back-biasing scheme is decreased by 30%. Additionally, as observed from Figure 7, the energy per operation of the ring-oscillator balanced by asymmetric back-gate biasing is smaller than the symmetrically biased ring-oscillator over all frequency range, for each back-biasing scheme.

#### IV. FLIP-FLOP DESIGN

We used a gate based edge-triggered D type flip-flop introduced in [16]. The measurement results of different versions of this DFF confirm its functionality in ultra-low voltages domain down to 132 mV [17]. Figure 8 shows schematic and layout view of the DFF with 26 transistors. The operation principle of the DFF is that when CK=0 the outputs of gate3 and gate4 are 1 and the output of these gates will not change with changes in net2, thus the state of the output latch (gate5 and 6) will not change. For CK=1, D signal flows through the gate1, gate2 and inverter and changes the state of net3 or net4 to 0 this in

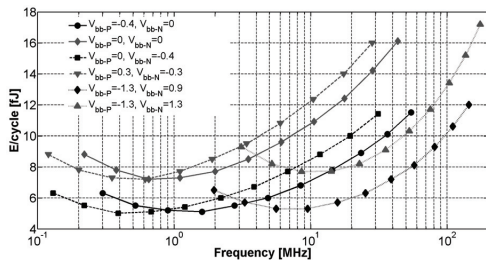


Fig. 7. Energy per operation of ring-oscillators with different back-gate biasing schemes versus oscillation frequency.

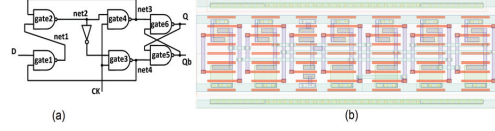


Fig. 8. (a) Schematic view of DFF (b) layout view of used DFF.

turn changes output latch state. As net3 or net4 discharged to 0 the output of gate2 or gate1 will be tied to  $V_{dd}$ , hence net2 will be completely isolated from changes in D.

The DFF has following advantages: 1- It has very regular structure which leads to a regular layout as shown in Figure 8(b). 2- It has a single-phase clock signal. Overlap between true and complementary clock signals causes contention in feedback loops of master-slave flip-flops. 3- Contention-free, there is no node subject to contention in the DFF.

Since hold time violations cause timing failures independent of clock frequency, this parameter of flip-flops deserves to be explored in more detail. If D is high, net3 will be discharged to 0 after rising edge of clock signal and the feedback pass from the output of gate 4 to gate 2 will isolate circuit from changes in the input. Similarly, when D is low, net4 will be discharged to 0 after rising edge of the clock signal, and hence, gate1 will be nontransparent for a high input. To have a proper operation with D=0 at the input, net4 must be discharged to 0 before changes in the input reset net1 to 0. Likewise with D=1 at the input, net3 must be discharged to 0 before changes in the input D resets output of gate2 to 0. Taking above discussions about hold time into account, the worst case hold time in DFF is when input D is low and it changes from logic 0 to 1 just after the rising edge of the clock signal.

Figure 9 (a) illustrates the normalized CK-to-Q delay versus CK-to-D delay. The hold-time is defined as the CK-to-D delay for which the CK-to-Q delay increases 5% from its nominal value [18]. The average and standard deviation of the hold time versus  $V_{dd}$  is illustrated in Figure 9 (b). We did MC analysis taking mismatch and process variations into account. To find  $\sigma$  and  $\mu$  of hold time, CK-to-Q delay versus CK-to-D delay curves were drawn for each MC run and hold time was calculated from these curves. To save simulations run time, the number of MC runs was chosen to be 100.

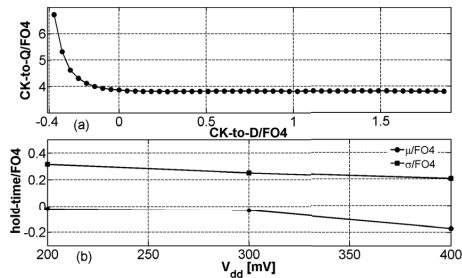


Fig. 9. (a) Normalized CK to Q delay versus CK to D delay to find hold time of the DFF at  $V_{dd} = 200 mV$  (b) 100 MC runs at three different  $V_{dd}$ s.



## V. MAC BLOCK

An 8-bit MAC has been synthesized using our fully customized cell library with standard EDA tools. The library comprises basic logic gates such as the inverter, buffer, NAND2, NOR2 and filler cells. A 1-bit full adder and 2 flip-flops with and without asynchronous 'set' signal are also included in the library. Minority-3 gates were used to implement the 1-bit full adder from [19] and, the flip-flops have same structure as discussed in section IV. As shown in Figure 10 (a), the 8-bit MAC has two pipeline stages with 16-bit input, output and middle registers. Figure 10 (b) shows the layout view of the MAC after place and route. The active area is  $48 \times 46 \mu m^2$ .

Figure 11 (a) shows delay distribution of the shortest path in the FF process corner. This minimum delay path was extracted from synthesis tool. The maximum allowable clock skew can be calculated from minimum delay constraint as shown in equation 1.  $\mu - 3\sigma$  of the clock-to-Q delay in FF process corner is 13.5 ns. Calculating  $\mu - 3\sigma$  of the minimum delay path from Figure 11 (a) and  $\mu + 3\sigma$  of the hold time from Figure 9 (b), the maximum allowable clock skew was calculated to be 46 ns which equals to 4FO4 delay.

$$t_{skew} \leq t_{logic,min} + t_{cq,min} - t_{hold,max} \quad (1)$$

To find the maximum operating frequency of the MAC block, the critical path of the MAC block was extracted. Figure 11(b) shows delay distribution of the critical path in the SS process corner. At 200 mV  $V_{dd}$  and SS process corner,  $\mu + 3\sigma$  of the critical path is 1.14 us (clock-to-Q delay is included in this path), and set up time of the DFF is 32 ns. Accordingly, assuming maximum allowable clock skew of 4FO4, the maximum clock frequency at 200 mV is 830 KHz (See equation 2).

$$t_{ck} \geq t_{logic,max} + t_{cq,max} + t_{set\_up,max} + t_{skew} \quad (2)$$

Figure 12 shows energy per operation of the 8-bit MAC block versus the operating frequency for 3 different back-gate biasing schemes. The supply voltage had been varied from 150 mV to 400 mV for each biasing scheme. The maximum frequency for each supply voltage is calculated from equation 2. The SPICE simulations are based on the netlist extracted from the layout view taking both parasitic capacitance and resistance into account. The minimum energy per operation was achieved with  $V_{bb\_PMOS} = -0.4V$  and  $V_{bb\_NMOS} = 0$ . The 51 fJ MEP occurs at 275 mV supply voltage with a maximum operating frequency of 5.3 MHz. As can be observed from Figure 12, forward back-gate

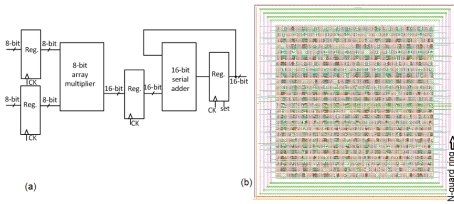


Fig. 10. (a) Block diagram view and (b) layout view of 8-bit MAC block.

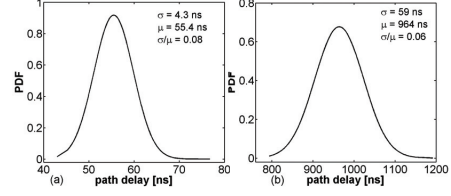


Fig. 11. (a) shortest path delay distribution in FF process corner (b) longest path delay distribution in SS process corner (2000 MC and  $V_{dd} = 200$  mV).

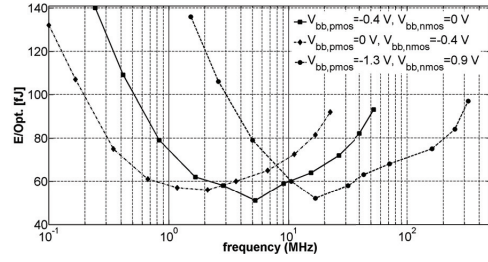


Fig. 12. 8-bit MAC energy per operation versus operating frequency for three back biasing schemes.

biasing is more energy efficient for higher speeds. With forward back-gate biasing, the MAC block consumes less energy per operation for operating frequencies higher than 11 MHz. The minimum  $V_{dd}$  has to be kept at 150 mV because functional yield degrades and variability of the circuit increases by lowering supply voltage. However, for the applications with more relaxed performance requirements, the power consumption can be reduced by decreasing  $V_{dd}$ . This is not possible because of minimum  $V_{dd}$  constraint. Therefore, reverse back-gate biasing is proper choice for applications with more relaxed performance requirements. As illustrated in Figure 12, reverse back-gate biasing is more energy efficient for frequencies smaller than 2 MHz.

Another important issue in extreme reverse back-gate biasing ( $V_{bb\_PMOS} = 0$  and  $V_{bb\_NMOS} = -0.4V$ ) is PWELL to NWELL diodes leakage current. To take this issue more into account, deep-NWELL and an NWELL guard-ring are used to isolate the PWELL of the core circuitry from P-substrate, as shown in Figure 10 (b). The total leakage power due to the parasitic PWELL/P-sub to NWELL diodes was 10 nW with extreme reverse back-gate biasing.

Table II provides a comparison between this work and existing subthreshold MAC blocks. Since the MAC in [7] is 16-bit and is implemented with the same 28 nm technology, specifications of an equivalent 16-bit MAC are listed in Table II to have a fair comparison. The MAC in this work consists of an array multiplier followed by a serial adder, so operating frequency ( $f_{opt}$ ) and number of the gates of 16-bit MAC will be 0.5x and 3.5x of the 8-bit MAC. This means that total parasitic capacitance ( $C_p$ ) and leakage current ( $I_{leak}$ ) of the 16-bit MAC is 3.5x of the 8-bit MAC. Therefore as shown in equations 3 and 4, the

TABLE II  
COMPARISON WITH EXISTING WORKS

	[5] 8-bit				[6] 16-bit				[7] 16-bit				This work(16-bit equivalent MAC)			
	@ $V_{ddmin}$	@ $V_{ddmin}$	@ $E_{min}$	@ 51MHz	@ $V_{BB}$ 0V	@ $V_{BB}$ 0.3V	@ $V_{BB}$ 1.5V	@ $V_{BB}$ 0V	@ $V_{BB}$ 0.4V	@ $V_{BB}$ 0.9V	@ 147MHz	@ $V_{BB}$ 0V	@ $V_{BB}$ 0.275	@ $V_{BB}$ 0.25	@ $V_{BB}$ 0.25	@ $V_{BB}$ 0.385
$V_{dd}[V]$	0.175	0.15	0.19	0.28	0.29	0.33	0.29	0.275	0.275	0.25	0.385	0.275	0.275	0.25	0.385	0.385
f[MHz]	0.166	5	10.5	51.3	25	26	147	2.6	1	8.3	147	2.6	1	8.3	147	147
P[μW]	0.014	4.8	9.1	66.2	7	8.3	61.7	0.65	0.28	2.2	48.5	0.65	0.28	2.2	48.5	48.5
E[pJ]	0.084	0.96	0.87	1.29	0.28	0.32	0.42	0.25	0.28	0.26	0.33	0.25	0.28	0.26	0.33	0.33
EDP[pJ.μs]	0.506	0.193	0.083	0.025	0.011	0.12	0.0029	0.096	0.28	0.0313	0.0022	0.096	0.28	0.0313	0.0022	0.0022

static and dynamic energy consumptions of the 16-bit MAC with the same structure increases by 7x and 3.5x, respectively.

$$E_{t\ 8bit} = I_{leak}V_{dd}/f_{opt} + \alpha C_p \cdot V_{dd}^2 \quad (3)$$

$$E_{t\ 16bit} = 3.5I_{leak}V_{dd}/(0.5f_{opt}) + \alpha 3.5C_p V_{dd}^2 \quad (4)$$

As listed in Table II, the MAC in [5] provides lowest energy and power consumptions considering its 140 nm technology, but at significantly lower computational speed than the other implementations. The MACs in [6] and [7] are faster, but this comes at cost of higher dynamic and static power consumptions. The lower speed of the MAC block in this work can be overcompensated by increasing the supply voltage. For example, to meet 147 MHz operating frequency for 16-bit MAC (i.e. 294 MHz for 8-bit MAC),  $V_{dd}$  is increased to 385 mV. The energy per operation of the equivalent 16-bit MAC at this  $V_{dd}$  is 0.33 pJ which is 21% lower than energy per operation of the MAC in [7] at 147 MHz operating frequency.

## VI. CONCLUSION

The development of logic cells for ULV applications has been discussed in this paper. We have focused on making a satisfactory trade-off between sensitivity to the variations and energy consumption of the digital logic cells. The designed cells are NWE aware and asymmetric back-gate biasing helps to have smaller PUN, and hence, lower energy consumption. Monte Carlo analysis of worst case back-to-back configuration for SNM evaluation shows adequate SNM for cells down to 150 mV. A full custom cell library has been developed, and a MAC block has been synthesized using the designed library. Comparing specifications of the designed MAC to the MAC in [7] reveals better energy efficiency for the MAC block in this work, so that the speed drop could be overcompensated by increasing the supply voltage. The minimum energy point of the 8-bit MAC block was 0.051 pJ at 275 mV and 5.3 MHz clock frequency.

## REFERENCES

- [1] Magarshack, Philippe; Flatresse, Philippe; Cesana, Giorgio, "UTBB FD-SOI: A process/design symbiosis for breakthrough energy-efficiency," in Design, Automation & Test in Europe Conference & Exhibition (DATE), 2013, vol., no., pp.952-957, 18-22 March 2013.
- [2] Skotnicki, T.; Fenouillet-Beranger, C.; Gallon, C.; Boeuf, F.; Monfray, S.; Payet, F.; Pouydebasque, A.; Szczap, M.; Farcy, A.; Arnaud, F.; Clerc, S.; Sellier, M.; Cathignol, A.; Schoellkopf, J.-P.; Perea, E.; Ferrant, R.; Mingam, H., "Innovative Materials, Devices, and CMOS Technologies for Low-Power Mobile Multimedia," in Electron Devices, IEEE Transactions on, vol.55, no.1, pp.96-130, Jan. 2008.
- [3] de Streeel, G.; Bol, D., "Impact of back gate biasing schemes on energy and robustness of ULV logic in 28nm UTBB FDSOI technology," in Low Power Electronics and Design (ISLPED), IEEE International Symposium on, vol., no., pp.255-260, 4-6 Sept. 2013.
- [4] Jacquet, D.; Hasbani, F.; Flatresse, P.; Wilson, R.; Arnaud, F.; Cesana, G.; Di Gilio, T.; Lecocq, C.; Roy, T.; Chhabra, A.; Grover, C.; Minez, O.; Uginet, J.; Durieu, G.; Adobati, C.; Casalotto, D.; Nyer, F.; Menut, P.; Cathelin, A.; Vongsavady, I.; Magarshack, P., "A 3 GHz Dual Core Processor ARM CortexTM-A9 in 28 nm UTBB FDSOI CMOS With Ultra-Wide Voltage Range and Energy Efficiency Optimization," in Solid-State Circuits, IEEE Journal of, vol.49, no.4, pp.812-826, 2014.
- [5] M. Miyazaki, J. Kao and A. P. Chandrakasan, "A 175 mV multiply-accumulate unit using an adaptive supply voltage and body bias (ASB) architecture," Solid-State Circuits Conference. Digest of Technical Papers. IEEE International, San Francisco, CA, USA, 2002, pp.58-444 vol.1
- [6] N. Reynders and W. Dehaene, "Variation-resilient sub-threshold circuit solutions for ultra-low-power Digital Signal Processors with 10MHz clock frequency," ESSCIRC, 2012 Proceedings of the, Bordeaux, pp. 474-477.
- [7] Reyserhove, H.; Reynders, N.; Dehaene, W., "Ultra-low voltage datapath blocks in 28nm UTBB FD-SOI," in Solid-State Circuits Conference, 2014 IEEE Asian, vol., no., pp.49-52, 10-12 Nov. 2014.
- [8] E. Vittoz and J. Fellrath, CMOS analog circuits based on weak inversion operation, JSSC, vol. SC-12, pp. 224-231, June 1977.
- [9] Calhoun, B.H.; Wang, A.; Chandrakasan, A., "Device sizing for minimum energy operation in subthreshold circuits," in Custom Integrated Circuits Conference. Proc. of the IEEE, pp.95-98, Oct. 2004.
- [10] Wang, P.P., "Device characteristics of short-channel and narrow-width MOSFETs," in Electron Devices, IEEE Transactions on, vol.25, no.7, pp.779-786, Jul 1978.
- [11] Akers, L.A., "The inverse-narrow-width effect," in Electron Device Letters, IEEE, vol.7, no.7, pp.419-421, Jul 1986.
- [12] H. K. O. Berge and S. Aunet, "Benefits of decomposing wide CMOS transistors into minimum-size gates," NORCHIP, 2009, pp. 1-4.
- [13] T. McConaghy, K. Breen, J. Dyck and A. Gupta, "Variation-Aware Design of Custom Integrated Circuits: A Hands-on Field Guide, Springer Science & Business Media, 2012.
- [14] Dongsuk Jeon; Mingoo Seok; Chakrabarti, C.; Blaauw, D.; Sylvester, D., "A Super-Pipelined Energy Efficient Subthreshold 240 MS/s FFT Core in 65 nm CMOS," in Solid State Circuits, IEEE Journal of, vol.47, no.1, pp.23-34, Jan. 2012.
- [15] A. A. Vatanjou, T. Ytterdal and S. Aunet, "Exploiting short channel effects and multi-Vt technology for increased robustness and reduced energy consumption, with application to a 16-bit subthreshold adder implemented in 65 nm CMOS," Circuit Theory and Design (ECCTD), 2015 European Conference on, Trondheim, 2015, pp. 1-4.
- [16] Okugawa, S.; Inoue, N., "Systematic design of D flip-flops using two state variables," in Electronics Letters, vol.23, no.17, pp.909-910, August 13 1987.
- [17] A. A. Vatanjou, T. Ytterdal and S. Aunet, "4 Sub-/near-threshold flip-flops with application to frequency dividers," Circuit Theory and Design, 2015 European Conference on, pp. 1-4.
- [18] Markovic, D.; Nikolic, B.; Brodersen, R.W., "Analysis and design of low-energy flip-flops," in Low Power Electronics and Design, International Symposium on, 2001., vol., no., pp.52-55, 2001.
- [19] S. Aunet, Y. Berg, "Three sub-fj power-delay-product subthreshold cmos gates," in Proceedings of 2005 International Conference on Very Large Scale Integration of System on Chip, Oct 2005, pp. 465470.

4.6 *paper VI*

**Comparative analysis of flip-flop architectures for sub-threshold applications in 28nm FDSOI**

Conference publication presented at IEEE Nordic Circuits and Systems Conference (NORCAS 2015).

Publication date: 28 December 2015.

This paper is not included due to copyright available at <https://doi.org/10.1109/NORCHIP.2015.7364372>





4.7 *paper VII*

**Ultra-low voltage adders in 28 nm FDSOI exploring poly-biasing for device sizing**

Conference publication presented at IEEE Nordic Circuits and Systems Conference (NORCAS 2016).

Publication date: 22 December 2016.

This paper is not included due to copyright <https://doi.org/10.1109/NORCHIP.2016.7792895>



4.8 *paper VIII*

**Extended Comparative Analysis of Flip-Flop Architectures for Subthreshold Applications in 28 nm FD-SOI**

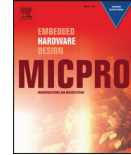
Journal publication printed in Elsevier Microprocessors and Microsystems.  
Volume 48, Pages 11-20, February 2017.





Contents lists available at ScienceDirect

## Microprocessors and Microsystems

journal homepage: [www.elsevier.com/locate/micpro](http://www.elsevier.com/locate/micpro)

## Extended Comparative Analysis of Flip-Flop Architectures for Subthreshold Applications in 28 nm FD-SOI<sup>☆</sup>



Even Låte<sup>1,\*</sup>, Ali Asghar Vatanjou<sup>2</sup>, Trond Ytterdal<sup>3</sup>, Snorre Aunet<sup>4</sup>

Department of Electronics and Telecommunications, Norwegian University of Science and Technology, O.S. Bragstads plass 2a, 7034, Trondheim

### ARTICLE INFO

**Article history:**  
Received 22 February 2016  
Revised 21 June 2016  
Accepted 21 July 2016  
Available online 22 July 2016

**Keywords:**  
Subthreshold  
28 nm FD-SOI  
D Flip-flop  
Comparison  
Setup Time  
Hold Time

### ABSTRACT

Nine D-type Flip-Flop (DFF) architectures were implemented in 28 nm FDSOI at a target, subthreshold, supply voltage of 200 mV. The goal was to identify promising DFFs for ultra low power applications. The single-transistor pass gate DFF, the PowerPC 603 DFF and the C<sup>2</sup>MOS DFF are considered to be the overall best candidates of the nine. The pass gate DFF had the lowest energy consumption per cycle for frequencies lower than 500 kHz and for supply voltages below 400 mV. It was implemented with the smallest physical footprint and it proved to be functional down to the lowest operating voltage of 65 mV in the typical process corner. During Monte Carlo (MC) process and mismatch simulations it was also found that the pass gate DFF is least prone to variations in both minimal setup- and minimal hold-time. Race conditions, during mismatch variations, occurred for the flip-flop that is constructed from NAND and inverter based multiplexers. The pass gate DFF is outperformed slightly when it comes to D-Q-based power-delay product and more significantly when it comes to the maximum clock frequency. The flip-flops having the shortest D-Q delays were the PowerPC 603 and the transmission gate D flip-flop, these also had the lowest D-Q-based power-delay of 26% and 30% respectively of that of the worst-case S<sup>2</sup>CFF power-delay product.

© 2016 Elsevier B.V. All rights reserved.

### 1. Introduction

Ever since the Centre Electronique Horloger (CEH) in Switzerland succeeded with low power integrated circuits [2], scientists have strived to create new and improved methods for designing low power systems. Subthreshold CMOS operation is such an approach and is applied both in the analog and in the digital circuit design domain. By reducing the supply voltage below the threshold voltage of the transistors, the power consumption can be reduced by several orders of magnitude. The principle of operating transistors in weak inversion dates back to 1967 [3]. Despite its early introduction, only a few niche-products exploiting subthreshold operation have been established in the consumer-electronics market until now. The sensor-network trend known as the Internet

of Things (IoT) has re-opened the interest for the ultra low power (ULP) benefits of operating transistors in the subthreshold region. ULP Sensor nodes driven by coin-cell batteries will last for a long time, or perpetually, if energy harvesting is used in combination with subthreshold operation.

D flip-flops (DFFs) are widely used in digital applications such as parallel storage and to serially manipulate internal circuit nodes in SoCs. These edge triggered devices account for large fractions of circuit area and power consumption and are also amongst the most difficult digital building blocks to push to lower supply voltage levels without experiencing problems with data corruption. Either the output (Q) is subject to voltage drop so that it fails to take its correct logical value, or the internal delay of the master latch is too high to allow the slave latch to latch on to the data (D) signal.

The objective of this work is to explore multiple flip-flop architectures and identify promising candidates among these for subthreshold applications in 28 nm Fully Depleted Silicon On Insulator (FDSOI).

In this paper, section 2 introduces details on a schematic level for the chosen set of DFF architectures. The simulation-setup and performance metrics for evaluating these are explained in section 3, followed by results and an evaluation of the schematics in section 4 & 5 respectively.

<sup>☆</sup> This paper is an extended version of the already published conference paper "Comparative analysis of flip-flop architectures for subthreshold applications in 28nm FDSOI" [1].

\* Corresponding author. Tel.: +4792893321.

E-mail addresses: [even.late@ntnu.no](mailto:even.late@ntnu.no), [even.laate@iet.ntnu.no](mailto:even.laate@iet.ntnu.no) (E. Låte).

<sup>1</sup> PhD Candidate

<sup>2</sup> PhD Candidate

<sup>3</sup> Professor & Supervisor

<sup>4</sup> Professor & Supervisor

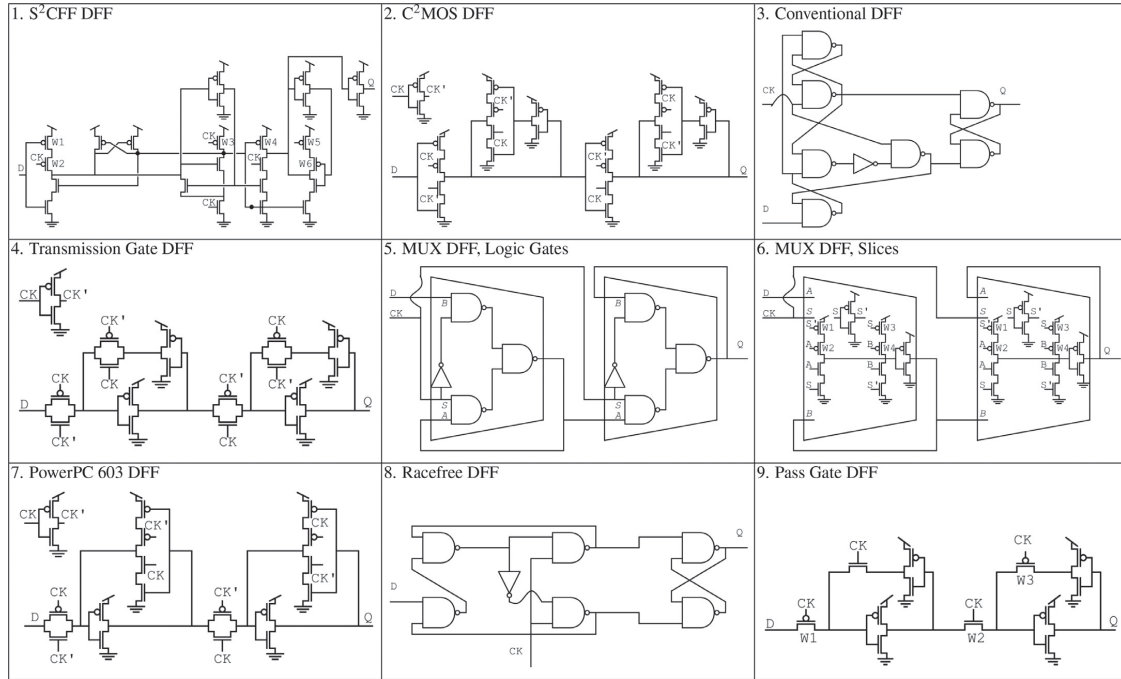


Fig. 1. Schematic overview of the flip-flop architectures that are considered in this study, the nand and inverter symbols in cell 3. and 5. are made with 4 and 2 LVT transistors respectively.

## 2. Materials and Methods

### 2.1. 9 D Flip-Flop Architectures

Nine static D flip-flop architectures were picked out for a comparative study of their subthreshold abilities. The schematics for each of them are illustrated in Fig. 1 and are further explained in the enumerations below:

1. The static single-phase contention-free flip-flop ( $S^2CFF$ ) [4,5] is shown in cell No. 1 in Fig. 1. It is based on a dynamic true single-phase flipflop and is made static by including a slave latch and some additional transistors. The  $S^2CFF$  was designed in 2014 for near threshold operation on a 45 nm SOI technology.
2. The second structure is the well known Clocked CMOS flip-flop ( $C^2MOS$ ) [6]. It consists of clocked 4T and basic 2T inverters and relies on two clock phases.
3. The conventional NAND-based design in cell 3 was used for its simplistic gate level structure together with Schmitt-trigger gates in [7] to push the lower limits of the supply voltage. The original design is made into a positive edge triggered DFF by removing one inverter on the clock (CK) input.
4. A flip-flop design consisting of transmission gates and inverters such as the one shown in cell number 4, is referred to as the Transmission Gate DFF. It is used extensively in sequential systems for its low power consumption and low transistor count. Note that two clock phases are used.
5. A static master slave flip-flop can be constructed using two multiplexers (MUXes) configured as latches. In this paper

two different MUX topologies are investigated for such a configuration. Cell number 5 shows such a DFF with MUXes built up from conventional logic gates.

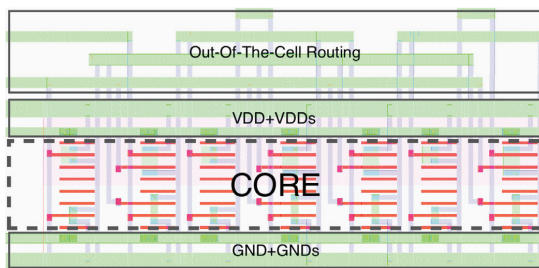
6. Cell number 6 shows a second MUX-based flip-flop where the MUXes are built in a XNOR-like fashion with logic branches.
7. The PowerPC 603 flip-flop in cell number 7 was used in the PowerPC 603 microprocessor [8]. The PowerPC flip-flop has been modified slightly since then, the two transistors controlling the scan mode of the DFF have been removed. This design has in previous comparative studies been found to have great subthreshold abilities [9–11].
8. Cell number 8 contains another NAND and inverter based flip-flop that is race free [12]. This design differs from the conventional NAND based flip-flop by the fact that it has less logic gates and thus occupies a smaller amount of area.
9. Transmission gates are normally used to achieve symmetrical transmission of logic high and logic low signals. The single pass gate design in cell number 9 exploits the area and single clock-phase benefits of using single transistors as pass gates instead of the 2T transmission gates [13], the trade-off is loss in signal integrity. In 2015, this DFF architecture was simulated in 28 nm FDSOI with promising results [14].

### 2.2. Flip-Flop Implementation, Sizing & Layout

For this study, all the DFF architectures were implemented for a supply voltage of 200 mV and with LVT transistors. The transistors were sized to give equal drive strength for pull up and pull down networks. Flip-flops consisting of logic building blocks were

**Table 1**  
Transistor dimensions, transistor counts and area of the implemented layout for the 9 DFFs in Fig. 1.

DFF	Transistor dimensions (nm), $W_{\text{default}}=80$ , $L_{\text{default}}=30$	Trans. Count	Area Full ( $\mu\text{m}^2$ )	Area Full (% of $S^2\text{CFF}$ )	Area Core ( $\mu\text{m}^2$ )	Area Core (% of $S^2\text{CFF}$ )
1. $S^2\text{CFF}$	$W_1 W_2 W_5 W_6 W_{\text{pINV}}=172, W_3=122, W_4=110$ ,	24	24.11	100.00	7.45	100.00
2. $C^2\text{MOS}$	$W_{\text{pCKINV}}, W_{\text{pINV}}=172$	22	15.30	63.46	5.02	67.40
3. Conv.	$W_{\text{pNAND}}=162, W_{\text{pINV}}=172$	30	17.95	74.45	5.44	73.02
4. Transm.	$W_{\text{pTransm}}=200, W_{\text{pINV}}=172$	18	18.90	78.39	5.75	77.18
5. MUX-1	$W_{\text{pNAND}}=162, W_{\text{pINV}}=172$	28	17.65	73.21	5.35	71.81
6. MUX-2	$W_1, W_2, W_3, W_4=170, W_{\text{pINV}}=172$	24	19.67	81.58	6.00	80.53
7. PowerPC	$W_{\text{pTransm}}=200, W_{\text{pCKINV}}, W_{\text{pINV}}=172$	18	16.34	67.78	5.39	72.34
8. Racefree	$W_{\text{pNAND}}=162, W_{\text{pINV}}=172$	26	15.81	65.57	4.75	63.76
9. Pass Gate	$W_1 W_2 W_3=200 W_{\text{pINV}}=172$	12	11.82	49.03	4.19	56.24



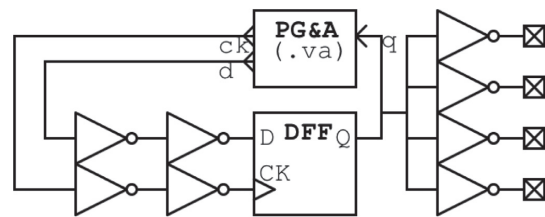
**Fig. 2.** Layout of the  $C^2\text{MOS}$  DFF, width = 5.613  $\mu\text{m}$ , full height = 2.726  $\mu\text{m}$ .

sized from the bottom and up. The drawn channel lengths ( $L$ ) of the transistors, in all flip-flops, were kept constant to minimize device mismatch and to simplify the architectural comparisons. All flip-flops were designed with drawn channel lengths equal to the 28 nm FDSOI process minimum at 30 nm.

For the basic 2T inverters, the width of the PMOS was found by locking the NMOS width to the process minimum while sweeping the input voltage such that the voltage transfer characteristic has an output equal to  $V_{DD}/2$  for an input equal to  $V_{DD}/2$ . For gates with multiple inputs, multiple transfer curves were achieved by holding non switching inputs in the on-state. The average of the multiple transfer curves was used for  $V_{DD}/2$ . This approach is ideal at uniform distributions of data input patterns. The transmission gate that is used in some of the DFFs was sized to have equal drain current for both NMOS and PMOS while being in the on-state.

Table 1 lists the settled transistor dimensions in the second column from the left. The transistors that are not mentioned in the table have minimum process dimensions i.e. drawn channel lengths equal to 30 nm and channel widths equal to 80 nm. The table also lists the differences in transistor count and area consumption for the 9 flip-flops.

Fig. 2 shows the layout of the  $C^2\text{MOS}$  DFF. A layout style where metal over gate-poly is avoided, is used for all DFF implementations in a similar fashion to make the comparison fair. The areas depend directly on the transistor counts and the regularity of the architectures, flip-flops with complex structures require extra area for routing outside of the cell. The out-of-the-cell routing makes it easier to visualize the differences in interconnect complexity for the flip-flops, which may ease the layout-process for the designer if taken into account during a flip-flop selection. See the four right-most columns of Table 1 for the area consumption of the flip-flops. The LVT transistors in 28 nm FDSOI are implemented in layout with flip well, N-channel devices reside in N-well and P-channel devices in P-well. The DFFs are compared with both the PMOS-network back-gate connection (VDDs), and the NMOS-network back-gate connection (GNDs), connected to the



**Fig. 3.** Test setup: A verilog A module for Pulse Generation and Analysis (PG & A), a FO4 load and realistic input signal drivers.

LVT-default ground potential. It could also be interesting to compare the DFFs to each other across the technology-given, feasible, range of body biasing but this is not done in this work.

All flip-flop layouts were analyzed with version 14.2 of the QRC parasitic extraction tool. Both the resulting post-layout-netlists and the pre-layout-schematics are used extensively in simulations throughout this paper.

### 2.3. Simulation Setup & Test Methodology

It is for subthreshold applications desired to compare the DFF topologies with respect to functionality, operating speed, power and robustness against process variations. The test-bench setup that is used in this comparative study is given for a single DFF instance in Fig. 3. The flip-flop architectures presented above were analyzed using similar comparative approaches as those proposed in [15]. Each flip-flop was simulated using double Inverters to drive the inputs and a fan-out of 4 inverters as output loads. Version 14.1 of the Spectre circuit simulator was used for all analog simulations in this study.

The test setup in Fig. 3 also includes a programmable Pulse Generation and Analysis (PG&A) module. Since this module is written in verilogA, it is compatible with the Spectre circuit simulator.

#### 2.3.1. Simulating Minimal Supply Voltage, Maximum Frequency & Functional Yield

The PG&A module generates data and clock signals such as the top two waves shown in Fig. 4. Functionality is verified by automatically probing the Q signal at the interval marked with circles in the on the Q-signal. To allow observation of functionality on each individual positive clock edge, the data signal toggles on every falling clock edge which gives symmetrical setup and hold times for the DFF. Functionality is then be tested on a uniform output data distribution with a 50% switching activity-factor.

The lowest functional supply voltage was found for all flip-flops by introducing a minimal value for logic high equal to 75% of  $V_{DD}$ . A maximum value for logic low was also set to be 25% of  $V_{DD}$ . The supply voltage was then reduced to the point where the logic level



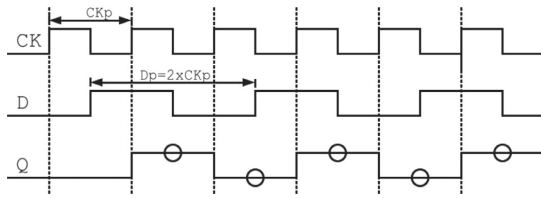


Fig. 4. Simulation stimuli used for verification of functionality.

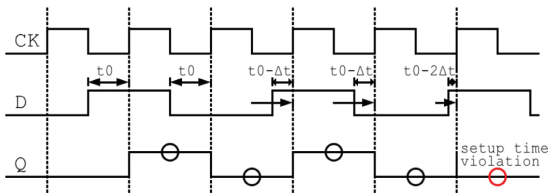


Fig. 5. Simulation stimuli used to map minimal setup time.

limits were breached by Q. For functionality comparisons at low operating voltages in the TT corner, the waveforms used in transient simulations were selected to allow settling of slow signals as a result of a low operating voltage. The lowest functional operating voltage was thus found with simulations at 1 kHz clock-frequency.

Maximum operating frequencies at 200 mV in the TT corner was also mapped with the functionality-test stimuli in Fig. 4. Having a symmetrical hold & setup time, makes the PG&A platform scalable and thus suitable for frequency adjustments with parametric sweeps. The frequency was simply increased until the verilogA module prompted a faulty output for each of the flip-flop architectures.

Functional yield was also simulated for the DFF architectures for many supply voltage levels. Also here the limits of logic high and logic low were set to 75% of  $V_{DD}$  and to 25% of  $V_{DD}$  respectively. The functional yield was simulated using the suitable number of 1000 Monte Carlo(MC) simulation-points for  $3\sigma$  accuracy [16] per DFF for every  $V_{DD}$  value.

### 2.3.2. Simulating the Limits of Setup- & Hold-Time

To map the minimal setup- and minimal hold- times of each flip-flop, the D signal transition was moved iteratively towards the CK edge until the DFF failed to propagate the change in the D input to the Q output on a positive clock edge. The minimal functional setup/hold time is then equal to the previous functional setup/hold time when such an event occurs. The PG&A module was made to sweep the hold and setup time and to detect events such as the one described above and then output the previous setup/hold time used. Using a variable in the delay parameter of the analog transition operator in verilogA allows for automatic sweeping of setup and hold time within the same transient simulation.

The waveform in Fig. 5 depicts a setup time sweep with a setup time violation on  $t_0 - 2\Delta t$ . The data signal transition is here moved from the left of the rising clock edge towards the edge.

The waveform in Fig. 6 shows us the corresponding hold time simulation waveform where a hold time violation is detected by the PG&A module yielding a minimal functional hold time equal to the initial hold time used minus one time quantum. The data signal transition is, for the hold time analysis, moved from the right of the clock cycle towards the clock cycle until the DFF fails to latch on to the previous data value.

By modifying the PG&A block to write each setup time or hold time value to a text file, statistical simulations for setup and hold

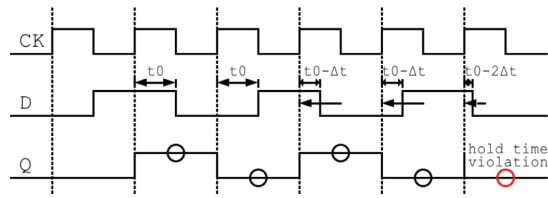


Fig. 6. Simulation stimuli used to map minimal hold time.

time were made possible. Once the output signal slips, the previously working time sample is written to a text file and a new statistical run can be initiated. For many Monte Carlo runs, the text file grows with delay samples for every transient run. This approach was used to map each DFF's timing-susceptibility to process variations which has a high correlation to yield in a larger system setting.

### 2.3.3. Simulating Power-Delay Products at Optimal Setup Times

Once the minimal setup time was identified for each DFF using the approach in subsection 2.3.2, the setup times were swept from this point and upwards, while observing the D-Q delay. The setup-time where the D-Q delay is minimal and optimal is often greater than the minimal setup time. This procedure was done for both rising and falling Q transitions, both for pure schematics netlists and for the extracted netlists from QRC. For rising and falling Q, the worst case optimal setup times of were chosen for PDP evaluation. This was done to account for asymmetry in the flip-flop schematics and to avoid functional errors deriving from optimistic clocking.

Using optimal setup times, and noting the minimal D-Q delay for a supply of 200 mV, average power consumption over one Q toggle period was probed for each DFF. Multiplying the average power consumptions per cycle by their corresponding D-Q delays gave the power-delay products for all flip-flops.

One should note here that the dual clock-phase flip-flops;  $C^2$ MOS, transmission gate and PowerPC 603 DFF were all implemented with local clock inversion. The local clock inverters were included in the power calculations of flip-flops using two clock phases. The inverted clock signal could also have been generated globally, but the additional power consumption from routing two clock signals would be difficult to model accurately.

### 2.3.4. Simulating Power & Energy/Cycle in Different Operating Regions

It is in many systems desirable to perform voltage and frequency scaling. This requires that circuit components remain functional over the scaling intervals, and that their performance and power consumption is adequate for all operating regions. To get a comparative overview of the scaling performance of the DFFs the supply voltage and the frequency was swept from 150 mV and 1 kHz, up to the LVT supply limit and up towards the maximum operating frequency of the DFFs. Current drawn from the supply was probed and the circuits correct functionality was simultaneously ensured using the PG&A module that was created. The idle leakage power of each architecture was probed both for the case of storing a logic 0 and the case of storing a logic 1. The leakage metric used here is the average of these two assuming a uniform data pattern.

## 3. Simulation Results

### 3.1. Minimum Supply Voltages & Minimal Clock Periods

The bar plot in Fig. 7 depicts the minimal operating voltage where the circuits are still functional for the typical process corner.

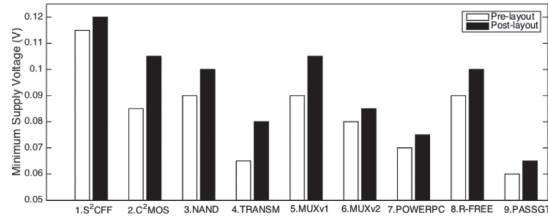


Fig. 7. Minimal functional supply voltage for the DFF architectures.

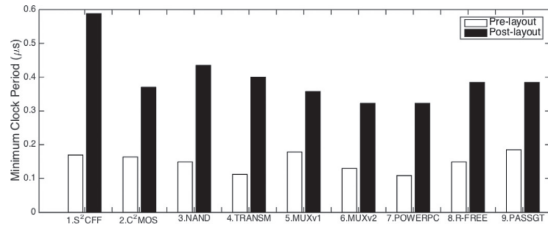


Fig. 8. Minimum functional clock period with symmetrical setup/hold time.

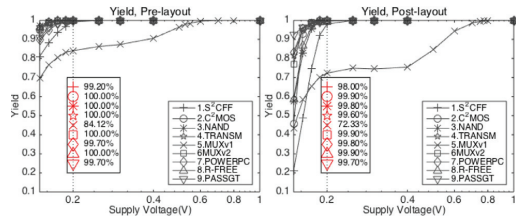


Fig. 9. Yield vs supply voltage for process & mismatch variations.

The bars in white represent simulation results from pre layout simulations, while the black bars represent results from simulations on extracted netlists. This colour encoding is repeated throughout the result section.

Fig. 8 shows the reciprocal of the maximum functional frequencies simulated with symmetrical hold and setup times also in the TT corner. Here, minimum clock period is used instead of maximum clock frequency to better visualize the differences in the post-layout results.

The yield curves in Fig. 9 are created from 1000 Monte Carlo Runs for various supply voltages. In the leftmost box in each plot window, the yield is listed for each DFF at the target supply voltage of 200 mV. The strong deviation in yield for the NAND&INV based mux DFF will be explained in the discussion section.

### 3.2. Setup Time and Hold Time Variations

In this subsection we will have a look at the results for the 9 DFF's timing simulations. Violation of both setup times and hold times leads to system failures so this aspect should be considered a top priority together with the yield aspect when selecting DFF topologies.

Fig. 10 shows us the variability of the minimal functional setup time in a box plot. The plot is created from 1000 time-samples per pre-layout and post-layout DFF architecture which is generated from 1000 Monte Carlo simulation points per test-bench, ref. Fig. 3. The central marks of the box plots are the median setup time for flip-flops exposed to process variations, the edges of the box are the 25th and 75th percentiles, while the whiskers extend to the

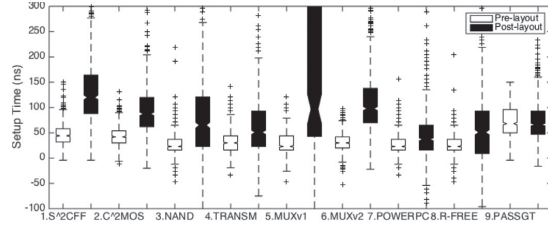


Fig. 10. Effect of process & mismatch on the minimal setup time.

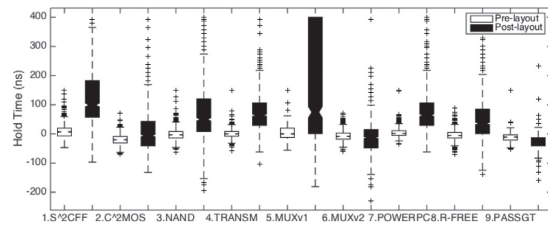


Fig. 11. Effect of process & mismatch on the minimal hold time.

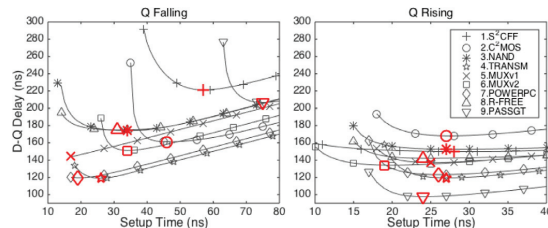


Fig. 12. D-Q delay varies with setup time, falling and rising Q for pre-layout netlist.

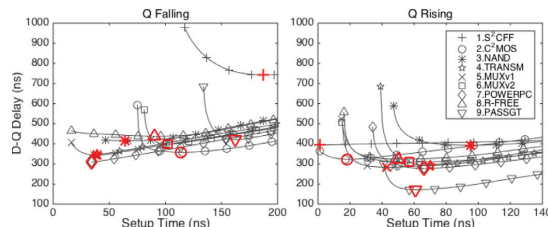


Fig. 13. D-Q delay varies with setup time, falling and rising Q for extracted netlists.

most extreme setup times that are not considered outliers of the setup-time data set. The crosses represent the outliers, that is any value that lies more than one and a half times the length of the box from either end of the box.

Similarly for the minimal functional hold time for each DFF, Fig. 11 is a box plot showing us how the minimal hold time is distributed for process and mismatch variations. This plot is also generated from 1000 Monte Carlo simulation points for each post and pre-layout DFF-netlist.

### 3.3. Comparative Power-Delay Products

The DFFs were compared with products of power consumption and D-Q delays in the typical corner for operation at optimal setup times. Fig. 12 and Fig. 13 show us how the D-Q delays vary for

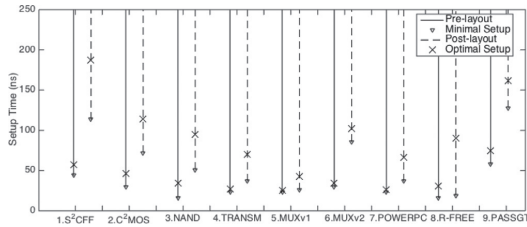


Fig. 14. Feasible ranges and optimal setup times for the 9 flip-flops in the typical process corner.

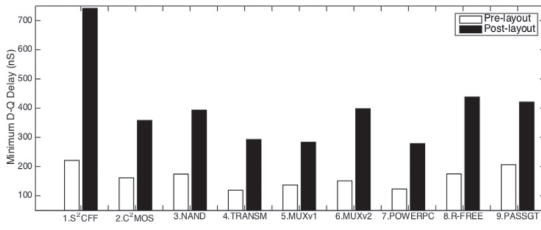


Fig. 15. D to Q delays using the optimal setup times in Fig. 14.

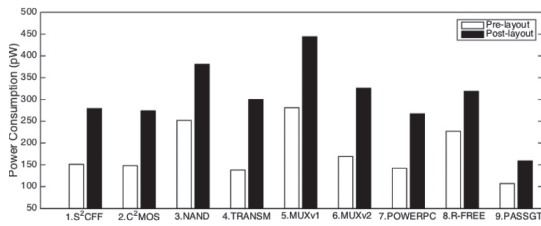


Fig. 16. Power consumptions at  $V_{DD} = 200$  mV using optimal setup times.

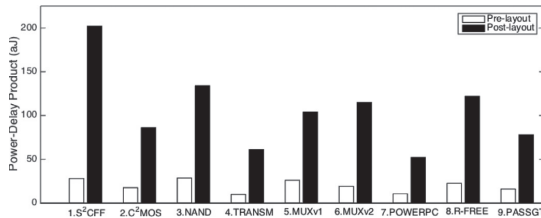


Fig. 17. Power-delay products (PDPs) for each flip-flop based on Fig. 16 and 15.

all flip-flop architectures as a function of setup-time. In the figures, the ideal setup times with respect to D-Q delays are marked with red. As a summary for the four plots, the feasible range of setup times and the optimal setup times for each architecture are given in Fig. 14. The corresponding minimal D-Q delays are plotted in Fig. 15. The average power consumed for one Q-toggle-cycle, of both rising and falling, for each of the DFFs, is given in Fig. 16. The two factors: Minimal D-Q delays and power consumptions, gives the power-delay bars in Fig. 17 when multiplied together.

3.4. Power and Energy in Different Operating Regions

For an idle DFF test-bench in the typical corner, the graphs in Fig. 18 shows us the leakage power that is consumed for different subthreshold supply voltages. The exponential nature of the leak-

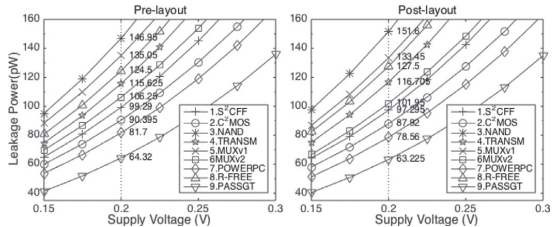


Fig. 18. Leakage power versus supply voltage level for each of the 9 DFFs on the extracted netlist.

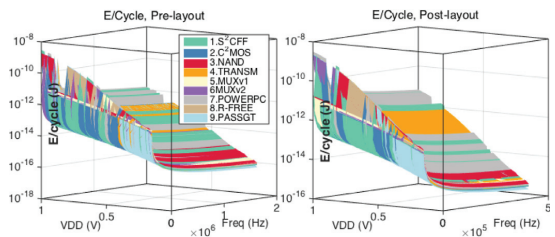


Fig. 19. Flip-flops and their energy consumption per clock cycle in the frequency- and supply-voltage- operation space. The best and the worst DFFs wrt. E/cycle, are further illustrated in Fig. 20, Fig. 21 and Fig. 22.

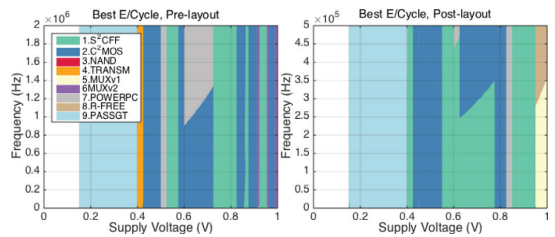


Fig. 20. The flip-flops having the least amount of energy consumed per cycle for given frequencies and supply voltages.

age power versus supply voltage plot continues all the way up to  $V_{DD}=1$ V without any deviations from the depicted pattern.

Varying both the operating frequency and the supply voltage, changes what DFF is optimal for specific areas of operation. Each DFF has its own energy per cycle plane in the frequency and supply voltage space. Fig. 19 shows each energy per cycle -surface, with different colors for each DFF, in the same coordinate system. All DFFs are functional at the displayed supply voltages and frequencies. The most significant information is highlighted in Fig. 20 & Fig. 21. Fig. 20 is essentially the same MATLAB surface plot as that in Fig. 19, it is simply rotated to a view from below. Fig. 21 gives us a transposed and rotated view of the same surfaces to list the DFFs that are worst with respect to energy consumption per cycle.

Since this comparative study is mainly intended for DFFs in the sub-threshold region, the average value for each of the surfaces for  $V_{DD} < 400$  mV are given in Fig. 22. It becomes evident that the pass gate DFF is most energy efficient in the subthreshold region.

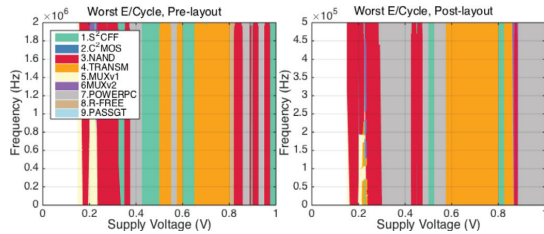


Fig. 21. The flip-flops having the most amount of energy consumed per cycle for given frequencies and supply voltages.

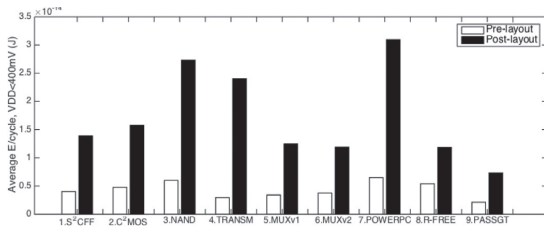


Fig. 22. Average energy per cycle in the sub-threshold region ( $V_{DD} < 400\text{ mV}$ ) of the surfaces in Figs. 19, 21, 20.

4. Discussion

The results section in this paper contains comparative results from manifold aspects of DFF properties that can be weighted differently by circuit designers for diverse applications. Table 2 lists each DFF’s rating relative to the other DFFs in the aspects of: Transistor Count, Minimal VDD, minimal clock period (maximum frequency), functional yield, variation of minimal setup- & hold-time, power-delay product, leakage power and energy per cycle in the subthreshold region. The smallest values in the sum-column represent the best DFFs if each property is weighted uniformly, normally this is not the case, however it is up to the circuit designer to weigh them.

Generally, the performance variations for pre- and post- layout simulations appear rather large through the result section. This is as expected for subthreshold applications as changes in nodal capacitance are more noticeable with low drive currents. The differences between pre- and post- layout simulations exist for all flip-flops, but to various degrees. Since the layout is made using the same out-of-the-cell routing-style for all the DFFs, the parasitic effects of gate-capacitances should be fair for all, thus making the simulation results depend largely on the schematical advantages of each topology, their drive characteristics, their routing complexity and their transistor count.

Of all the different topologies, the pass gate DFF has a superior area of its footprint compared to the other candidates as can be seen in Table 1. Using only 12 transistors, its footprint in this comparative implementation is only 49% as large as that of the worst case S<sup>2</sup>CFF. Depending on the circuit application, area is commonly a key criteria for topology selection.

All flip-flops are here designed for a supply voltage of 200 mV. Despite this fact, the lower the minimal operating voltage is, the greater the flexibility at a system level will be. A low limit for supply voltage reduction means having the possibility to perform voltage scaling over a larger voltage range, which again will increase the chances of finding a better global energy operating point, or lasting longer before a brown-out situation. Fig. 7 suggests that the pass gate design is best at this aspect, one should keep in mind that the minimal supply voltage levels found here are in the event of a typical corner.

The aspect of minimal functional clock period for symmetrical hold-& setup-times, also known as maximum clock frequency, is dominated by the XNOR-based MUX DFF and the PowerPC 603 DFF as Fig. 8 depicts. This is one of the weakest comparative checks for the pass-gate flip-flop since the n-channel and p-channel pass gates makes it highly asymmetrical when it comes to rise and fall times of the output, Q. The S<sup>2</sup>CFF is highly affected by parasitic capacitance from the out of the cell routing because of its routing complexity, it becomes the slowest DFF at 200 mV in the typical corner.

One of the most important comparison aspects is the functional yield, during a flip-flop topology selection this should have a high priority. Most DFFs have a yield in the top 90 percent category. This is, as mentioned section 3 and as depicted in Fig. 9, not the case for the MUX flip-flop that is built out of NANDs and inverters. It has at 200mV a yield of 84% for the pure schematic netlist and a yield of 72% for the post-layout netlist, which makes it useless for subthreshold applications as it stands. It can, however, be considered functional in the subthreshold region if the yield is improved to the top 90 percentage level. As can be seen of the schematic for the NAND&INV based MUX in Fig. 1, each MUX-latch has a feedback from the output of the MUX to either input A or input B for the slave and the master latch respectively. During a toggle of the clock signal, one logic branch is turned on and the other is turned off within one MUX. At the clock edge there is a race condition for the branches, and, depending on the mismatch of driving strengths, an erroneous output may be latched on to. By inserting delay elements in the feedback of each multiplexer-latch, the race condition is solved and, according to new simulations, the yield is improved to 99.2% for the pure schematic netlist. This increases the transistor count of the DFF by 8, making it the least desirable of the 9 with respect to transistor count.

Having a high functional yield as a solo device is important, however, in a system setting with propagation-delay variation, other aspects like resistance against minimal setup- and hold-time

Table 2 Summing up the findings for the extracted netlist-results with ratings, 1 = best, 9 = worst, the sum column weighs properties uniformly.

DFF type	# Trans.	Min. V <sub>DD</sub>	Min. Clock Period	Yield, Single DFF	Min. Setup T. Var.	Min. Hold T. Var.	PDP	Leakage Power	Avg E/cycle, V <sub>DD</sub> < 400 mV	SUM, Uniform Property Weight
1. S <sup>2</sup> CFF	6	9	9	8	6	7	9	4	5	63
2. C <sup>2</sup> MOS	4	7	3	3	3	4	4	3	6	37
3. Conv.	9	6	8	4	8	8	8	9	8	68
4. Transm.	3	3	7	7	4	5	2	6	7	44
5. MUX-1.	8	8	4	9	9	9	5	8	4	64
6. MUX-2.	5	4	1	1	7	2	6	5	3	34
7. PowerPC	2	2	2	5	2	3	1	2	9	28
8. Racefree	7	5	6	2	5	6	7	7	2	47
9. Pass Gate DFF	1	1	5	6	1	1	3	1	1	20 (best)



variation, comes into play. Low variation in the limits for setup and hold time together with proper clock routing makes it more likely that no hold or setup time violation is caused by clock skew in the total system. As the box-plots in Figs. 10 and 11 show, the boxes having the least variation in minimal limits of setup time is the pass gate DFF, tightly followed by the PowerPC 603 and the C<sup>2</sup>MOS. The same is true for the hold time variation, in addition to the 3 DFFs mentioned for the setup time variation, the XNOR-based MUX DFF looks particularly promising. As for the single functional yield, the NAND&INV DFF sticks out as the worst flip-flop for the same reason. Functionality violations that are caused by mismatch in the Monte Carlo simulations are independent of the setup- and hold-time that is used. The minimal functional setup- and hold-time values that are registered for the functionality violations becomes the initial values used for the setup and hold time sweeps, resulting in the stretched 25&75 percentiles of the data-set.

The Power delay product used here for all architectures is the D-Q delay at the found optimal setup-time multiplied by the average power consumption of the switching event. The pass gate flip-flop is, for the same reason as for the minimal clock-period aspect, not at the very top of the list. The use of single transistor pass gates makes the flip-flop highly asymmetrical when it comes to propagation delays and setup times for both logic high and logic low signals. D-Q delay is in this paper found as the worst case D-Q of a falling and rising Q signal event. So even though the pass-gate flip-flop toggles Q to a logic high using a short D-Q delay, the flip-flop is evaluated using its worst case D-Q delay that occurs in the falling Q event as can be seen in the horizontal placement of the upside down delta symbols in Fig. 13. This makes the worst case PDP for the pass gate DFF about 4 times larger than what it would have been for the rising Q signal case. As a result, the two flip-flop designs that have better power-delay products than the pass gate are the PowerPC 603 and the transmission gate DFFs with 52aj and 61aj respectively.

According to Figs. 10 & 11, the MUX-based flip-flop constructed using logic gates is by far the most prone architecture to statistical variations. The 8 other flip-flops prove to be quite robust in this aspect of the analysis. To minimize hold time and setup time violations in a system setting one would normally prefer D flip-flops with small variations in hold- & setup-time. The smaller the variation, the better the functional yield on a system level. The box plots suggest that the pass gate and the PowerPC DFFs are most desired from a setup time variation viewpoint and that the pass gate-, the MUXv2-, the C<sup>2</sup>MOS-, the PowerPC and the R-Free DFFs are best with respect to hold time variation. Overall the pass gate proves to be surprisingly robust to process variations.

In the result section we listed the leakage power consumption and the energy per cycle of each DFF for multiple operation regions. The top three flip-flops, having the least leakage power consumption in the idle state for the entire swept range of supply voltage, is the pass gate, the PowerPC and the C<sup>2</sup>MOS -DFFs, the worst is the conventional NAND&INV based DFF most likely due to its high amount of gates and thus relatively low resistance between V<sub>DD</sub> and GND. When it comes to energy per cycle, the pass gate is best while the conventional NAND&INV based DFF is worst for a supply voltage range of 150 mV to 400 mV. The flip-flops having the best energy consumption per cycle according to Fig. 20 proves to depend almost solely on the supply voltage and not that much on the frequency, with the exception on the voltage range from 0.6V to 0.8V, here the PowerPC 603 performs best for high frequencies while the C<sup>2</sup>MOS performs better for low frequencies on Pre-Layout simulations. For post layout simulations the S2CFF is best for low frequencies in this region while the C<sup>2</sup>MOS is best for high frequencies.

The simulation results found here, corresponds quite well to the earlier comparative studies in [9,10] and [11] where the PowerPC

603 DFF sticks out as the best architecture with respect to PDP. The results presented here supports these findings, but also broadens the DFF scope by shedding light on the pass gate flip-flop which performs better than the PowerPC 603 design on a broader basis except for maximum clock speed and energy per cycle outside of the subthreshold supply voltage region. The PDP of the PowerPC design in [10] is equal to 1 femtojoule at 200 mV post-layout, the lower PDP found here in 28 nm FDSOI may be explained by scaling advantages and the fact that the FDSOI process is more energy friendly than common bulk technologies.

## 5. Conclusion

In this paper various DFF structures are evaluated by their performance in the subthreshold region. The single-transistor pass gate flip-flop scores overall superior results compared to the other DFFs. It takes up silicon space equal to 49% of the S<sup>2</sup>CFF DFF area with the comparable layout approach described. Simulations point out that the pass gate design can be operated at lower voltages than the other DFFs. It is, however, worse than most DFFs for superthreshold operation, and it is not scoring very well on maximum clock frequency. The PowerPC 603 DFF is with a PDP of 52 attojoules, once again, found to be the flip-flop that has the lowest power-delay product followed by the transmission gate and the pass gate DFFs.

Energy efficiency is a significant challenge for IoT hardware, reducing the energy consumption of wireless sensor circuitry to the point where it can operate perpetually without the need for battery change is crucial to make the various IoT systems maintainable as they scale. Recent developments within the field are plentiful, for instance, in the 2016 January issue of IEEE JSSC, a sub-threshold ARM processing sub-system was designed [17] with an energy consumption of 11.7 pJ/cycle as a result of system- and software-level optimization for energy consumption. The authors highlight the importance of low-power circuit and system components for IoT applications. The ARM processing sub-system was implemented with 6.5 % of its cells as state-retention flip-flops (RFF) that consists of a modified version of the conventional master-slave DFF that is analyzed here. According to their source of inspiration [18], the RFF may be implemented using any kind of master-slave DFF that is scan-testable, making each DFF discussed in the work performed here, eligible. By selecting another DFF topology to base the RFF on, they could, according to the study performed here, improve both the power consumption and the overall performance of the ARM processing subsystem even further.

All flip-flop architectures discussed in this paper are yet to be analyzed with silicon measurements, such investigations will reveal impact of any parasitic effects that are neglected by the QRC resistance and capacitance extraction tool used in this work. At the time of writing, the GDS files of a 1mm<sup>2</sup> test-die has been sent to Circuits Multi-Projects(CMP) for fabrication, the test chip completion- and delivery-date is scheduled to be in the summer of 2016.

## References

- [1] E. Late, A.A. Vatanjou, T. Ytterdal, S. Aunet, Comparative analysis of flip-flop architectures for subthreshold applications in 28nm fdsOI, in: Nordic Circuits and Systems Conference (NORCAS): NORCHIP & International Symposium on System-on-Chip (SoC), 2015, IEEE, 2015, pp. 1–4.
- [2] C. Piguet, The First Quartz Electronic Watch, in: B. Hoehet, A.J. Acosta, M.J. Bel-lido (Eds.), Integrated Circuit Design. Power and Timing Modeling, Optimization and Simulation, no. 2451 in Lecture Notes in Computer Science, Springer Berlin Heidelberg, 2002, pp. 1–15.
- [3] Y. Tsvividis, Eric Vittoz and the Strong Impact of Weak Inversion Circuits, IEEE Solid-State Circuits Society Newsletter 13 (3) (2008) 56–58.

- [4] Y. Kim, W. Jung, I. Lee, Q. Dong, M. Henry, D. Sylvester, D. Blaauw, 27.8 A static contention-free single-phase-clocked 24t flip-flop in 45nm for low-power applications, in: Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2014 IEEE International, 2014, pp. 466–467.
- [5] F. Klass, Semi-dynamic and dynamic flip-flops with embedded logic, in: VLSI Circuits, 1998. Digest of Technical Papers. 1998 Symposium on, IEEE, 1998, pp. 108–109.
- [6] Y. Suzuki, M. Hirasawa, K. Odagawa, Clocked CMOS calculator circuitry, in: Solid-State Circuits Conference. Digest of Technical Papers. 1973 IEEE International, XVI, 1973, pp. 58–59.
- [7] N. Lotze, Y. Manoli, A 62 mV 0.13 m CMOS Standard-Cell-Based Design Technique Using Schmitt-Trigger Logic, *IEEE Journal of Solid-State Circuits* 47 (1) (2012) 47–60.
- [8] G. Gerosa, S. Gary, C. Dietz, D. Pham, K. Hoover, J. Alvarez, H. Sanchez, P. Ippolito, T. Ngo, S. Litch, J. Eno, J. Golab, N. Vanderschaaf, J. Kahle, A 2.2 W, 80 MHz superscalar RISC microprocessor, *IEEE Journal of Solid-State Circuits* 29 (12) (1994) 1440–1454.
- [9] H. Alstad, S. Aunet, Seven subthreshold flip-flop cells, in: *Norchip*, 2007, 2007, pp. 1–4.
- [10] M. Voernes, T. Ytterdal, S. Aunet, Performance comparison of 5 subthreshold CMOS flip-flops under process-, voltage-, and temperature variations, based on netlists from layout, in: *NORCHIP*, 2014, 2014, pp. 1–6.
- [11] H. Alstad, S. Aunet, Three Subthreshold Flip-Flop Cells Characterized in 90 nm and 65 nm CMOS Technology, in: 11th IEEE Workshop on Design and Diagnostics of Electronic Circuits and Systems, 2008. DDECS 2008, 2008, pp. 1–4.
- [12] S. Okugawa, N. Inoue, Systematic design of D flip-flops using two state variables, *Electronics Letters* 23 (17) (1987) 909–910.
- [13] H. Harris Weste Neil. David M., *Cmos Vlsi Design: A Circuits And Systems Perspective*, 3d, Pearson Education India, 2006.
- [14] S. Farideh, in: *Design of Reliable and Efficient Flip-Flops for Subthreshold Operation using Multi-Threshold MOSFETs and Transistor Sizing Technique.*, 2015.
- [15] V. Stojanovic, V. Oklobdzija, Comparative analysis of master-slave latches and flip-flops for high-performance and low-power systems, *IEEE Journal of Solid-State Circuits* 34 (4) (1999) 536–548.
- [16] T. McConaghy, K. Breen, J. Dyck, A. Gupta, *Variation-Aware Design of Custom Integrated Circuits: A Hands-on Field Guide*, Springer Science & Business Media, 2012.
- [17] J. Myers, A. Savanth, R. Gaddh, D. Howard, P. Prabhat, D. Flynn, A subthreshold arm cortex-m0+ subsystem in 65 nm cmos for wsn applications with 14 power domains, 10t sram, and integrated voltage regulator (2016).
- [18] M. Keating, D. Flynn, R. Aitken, A. Gibbons, K. Shi, *Low power methodology manual: for system-on-chip design*, Springer Publishing Company, Incorporated, 2007.



**Even Låte** graduated from the Norwegian University of Science and Technology (NTNU) with a M.Sc. degree in Electrical Engineering in 2014. His work on "Transaction Level Modeling of a PCI Express Root Complex" was awarded with the best master's thesis prize within the field of microelectronics at NTNU. Since the fall of 2014, Even has been employed as a PhD candidate at the Circuits and Systems Group. His research focus is mitigation of the dark silicon effect by designing ultra low power CMOS memory for use in the "Single-ISA Heterogeneous Many-Core Computer" project at NTNU.



**Ali Asghar Vatanjou** received his M.Sc. from University of Tabriz in 2010. During his M.Sc. degree, he worked towards pipeline ADC design. Since 2012, he started his PhD at Circuits and Systems Group, Norwegian University of Science and Technology (NTNU). He is currently working towards his PhD thesis at NTNU with main focus on ultra-low power and voltage digital circuit design. His main research interests includes ultra-low power and voltage VLSI and mixed-mode circuit design.



**Trond Ytterdal** received his M.Sc. and Ph.D. degrees in electrical engineering from the Norwegian Institute of Technology in 1990 and 1995, respectively. He is a Professor at the Department of Electronics and Telecommunications, Norwegian University of Science and Technology. Current main research interests include design of analog integrated circuits and modeling of novel nanoscale transistors. He has authored and co-authored more than 180 scientific papers in international journals and conference proceedings. He is a co-author of three books. Prof. Ytterdal is a member of The Norwegian Academy of Technological Sciences and a Senior Member of IEEE.



**Snorre Aunet** received the Cand. Scient. degree in informatics from the University of Oslo (UiO) in 1993, and the Dr. Ing. degree in physical electronics from the Norwegian University of Science and Technology (NTNU), in 2002. He worked with ASIC design at Nordic VLSI from 1994 to 1997, prior to doctoral studies. Later, he worked at NTNU and UiO, and is currently a professor at NTNU. He has been a visiting researcher at the University of Paderborn (2004-2012). From August 2015 to July 2016 he stays at University of California, San Diego (UCSD). Research interests include ultra low-power mixed-signal circuits.

4.9 *paper IX*

**Ultra-low voltage and energy efficient adders in 28 nm FDSOI exploring poly-biasing for device sizing**

Journal publication printed in Elsevier Microprocessors and Microsystems.  
Volume 56, Pages 92-100, February 2018.

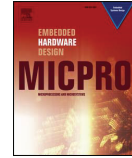






Contents lists available at ScienceDirect

## Microprocessors and Microsystems

journal homepage: [www.elsevier.com/locate/micpro](http://www.elsevier.com/locate/micpro)

## Ultra-low voltage and energy efficient adders in 28 nm FDSOI exploring poly-biasing for device sizing

Ali Asghar Vatanjou\*, Even Låte, Trond Ytterdal, Snorre Aunet

Department of Electronic Systems, Faculty of Information Technology and Electrical Engineering, Norwegian University of Science and Technology (NTNU), O.S. Bragstads plass 2a, Trondheim, 7491, Norway



## ARTICLE INFO

**Keywords:**  
Subthreshold  
28 nm FD-SOI  
CMOS  
Full-adder  
Ultra-low power

## ABSTRACT

Balancing the PMOS/NMOS strength ratio is a key issue to maximize the noise margin, and hence, the functional yield of CMOS logic gates and minimize the leakage energy per cycle in the subthreshold region. In this work, the PMOS/NMOS strength ratio was balanced using a poly-biasing technique in conjunction with back-gate biasing provided in a 28 nm fully depleted silicon on insulator (FDSOI) CMOS technology. A 32-bit adder based on minority-3 (min-3) gates and a 16-bit adder based on Boolean gates have been implemented. Chip measurement results of nine samples show highly energy efficient adders. The 32-bit and 16-bit adders achieved mean minimum energy points (MEP) of 20.8 fJ at 300 mV and 12.34 fJ at 250 mV, respectively. In comparison to adders reported in other works in the same technology, the energy per 1-bit addition of the 32-bit adder is improved by 37%. This improvement in energy consumption is 25% for the 16-bit adder. According to the measurement results of ten chips, the designed adders exhibited functionality down to supply voltages of 110 mV–125 mV, without body biasing. Additionally, the minimum  $V_{dd}$  of all the 32-bit adders based on minority-3 gates decreased to 80 mV by applying a reverse back bias voltage to the PMOS devices. One sample was functional at 79 mV with a 430 mV reverse back bias voltage applied to its PMOS devices.

## 1. Introduction

Reducing power consumption to ultimately break heat walls or to reduce energy consumption to prolong battery lifetime are key issues in present day microelectronics. The growing number of battery driven wireless devices, as well as the increasing energy demand of the applications to which these are intended, create a need for innovations in ultra-low power (ULP) circuitry. Subthreshold operation, potentially providing higher energy efficiency than other known low power circuits, has been known since the 1960s [1]. However the increasing demand mentioned above, and new features of modern process technologies, brings relevance of subthreshold design back.

A commercially available 28 nm FDSOI CMOS process tackles some of the key challenges faced by the scaling of conventional bulk silicon devices better, and so enables prolongation of Moore's law [2]. In this technology, the junction capacitance is significantly reduced and the drain induced barrier lowering (DIBL) effect is also lowered due to the ultra thin body and buried oxide [2], this while increasing the efficiency of back-gate biasing. In addition, the random dopant fluctuation is suppressed because threshold voltage adjustments do not depend on doping levels.

This manuscript present several extensions to the contents in [3] with respect to both statistical simulations and new measurements on additional chip samples. The extensions to simulations include variability in on-currents and delay as functions of sizing, and how sizing can affect energy per cycle for the designed logic cells. Post-layout simulations were also added, and compared to measurements results. Additionally, new measurements results have been added, which include effects of applying back-gate biasing voltages. Further extensions to [3] include measurements of static power consumption for nine 16-bit and 32-bit adder samples.

We here report highly energy efficient logic gates by exploiting both poly-biasing [4] as well as back-gate biasing techniques. Both techniques allow us to reduce the size of the pull up devices, thus reducing the leakage current and parasitic capacitance of the cells. This in turn leads to reduced power consumption. The poly-biasing technique increases the effective channel gate length without increasing the active area of the devices. Applying poly-biasing while connecting the PWELL/NWELL ties to ground improves the strength of the PMOS transistors. Moreover, the regular threshold voltage (RVT) devices have been chosen to reduce the leakage current further, compared to low threshold voltage (LVT) devices. Although higher threshold voltage

\* Corresponding author.

E-mail addresses: [ali.vatanjou@ntnu.no](mailto:ali.vatanjou@ntnu.no) (A.A. Vatanjou), [even.late@iet.ntnu.no](mailto:even.late@iet.ntnu.no) (E. Låte), [trond.ytterdal@ntnu.no](mailto:trond.ytterdal@ntnu.no) (T. Ytterdal), [snorre.aunet@ntnu.no](mailto:snorre.aunet@ntnu.no) (S. Aunet).

<https://doi.org/10.1016/j.micpro.2017.11.002>

Received 20 February 2017; Received in revised form 2 November 2017; Accepted 8 November 2017

Available online 09 November 2017

0141-9331 / © 2017 Elsevier B.V. All rights reserved.

leads to slower circuits, it can reduce the energy consumption of circuits with more relaxed throughput requirements [5]. The computational demands of wireless sensor networks (WSNs) have been discussed in [6], and the sensor-network applications were categorized into three groups: 1- low-bandwidth rates (sample rate less than 100 Hz), 2- mid-bandwidth rates (sample rate 100 Hz-1 KHz) and 3- high-bandwidth rates (sample rate higher than 1 KHz). It was shown in [6] that the performance of a processor with 168 KHz clock was more than four times of the desired performance for mid-bandwidth applications. For such systems with relaxed throughput requirements, a lower static power and robust functionality at ultra-low voltages translates into a lower energy consumption. Moreover, the use of RVT devices enables applying extreme reverse back-bias schemes to save leakage energy in the sleep mode, and avoid costly power-gating.

To validate the proposed sizing techniques, we have implemented a 32-bit adder based on min-3 gates [7] and a 16-bit adder based on traditional Boolean gates. The ripple carry adder (RCA) topology has been chosen because the energy consumption of the serial adders may be lower than the parallel adders while maintaining the same speed, when operated in subthreshold [8]. Comparing to adders reported in the same 28 nm FDSOI process technology [9], the minimum energy per 1-bit addition of the 32-bit and 16-bit adders have been improved by 37% and 25%, respectively.

To the knowledge of the authors, the 32-bit adder provides the lowest energy per 1-bit addition and the lowest functional  $V_{dd}$  among static CMOS circuits with more complex functionalities than simple inverters or ring-oscillators.

The remainder of the paper is organized as follows: The device sizing is discussed in Section 2. Two implementations of subthreshold adders are presented in Section 3. Measurement results are shown in Section 4, and is followed by a discussion in Section 5, before the final conclusions in Section 6.

## 2. Device sizing for balanced PMOS/NMOS

### 2.1. Transistor dimensions

Balancing the driving strength of the pull-up/pull-down networks (PUN/PDN) is a key issue to properly operate logic gates in the ultra-low voltage (ULV) domain. In addition, unbalanced PMOS/NMOS increases the leakage energy of subthreshold circuits [10]. Nevertheless as shown in Fig. 1, the on-current ratio of the PMOS with respect to NMOS is too small in the ULV domain. In Fig. 1, the NMOS device width is 200 nm,  $L=30$  nm and the drain-source voltage is set equal to the supply voltage. For example, the PMOS gate width should be upsized by more than 4X to have a balanced PUN/PDN at a supply voltage of 150 mV. This causes asymmetry in the layout of the cells. Additionally, both leakage current and parasitic capacitances, and consequently the power consumption of the circuit, increase with wider PMOS

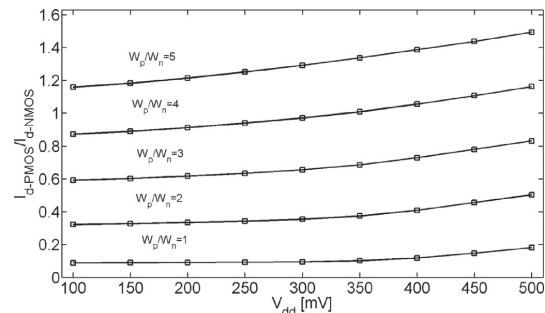


Fig. 1. PMOS/NMOS on-current ratio versus  $V_{dd}$  for  $W_n=200$  nm and  $L_n=L_p=30$  nm.

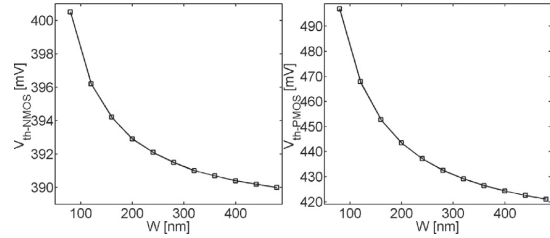


Fig. 2. Dependency of the threshold voltage on channel width (a) NMOS (b) PMOS.

transistors. Therefore using techniques to improve the strength ratio between PMOS and NMOS, can be an effective approach to reduce both power consumption and minimum operating supply voltage of sub-threshold circuits.

In this work we increased the effective gate length of the NMOS transistors by 16 nm using poly-biasing to balance NMOS and PMOS driving strengths. We also connected both NWELL and PWELL ties to ground, thus the bulk-source junction of PMOS transistors were forward biased. In order to reduce the leakage current further, the effective PMOS gate length was also increased by 4 nm using poly-biasing, while maintaining the switching voltage at  $V_{dd}/2$ . As can be observed from Fig. 2, the threshold voltage of this 28 nm FDSOI technology is inversely proportional to the gate width of the devices. In Fig. 2,  $L_{nmos} = L_{min} + 16$  nm,  $L_{pmos} = L_{min} + 4$  nm and  $V_{dd} = 200$  mV. The NMOS and PMOS transistor channel widths were chosen taking into account the channel width dependency of the threshold voltage. The minimum width of the NMOS devices was chosen to be 200 nm and the corresponding PMOS width that resulted in a switching voltage of  $V_{dd}/2$  for an inverter was 300 nm. Although a  $W_p/W_n$  ratio of 1.5 is required for balancing the PMOS and NMOS transistors, this is a reasonable ratio comparing with for example [11], where for  $W_p/W_n = 5$ , PMOS/NMOS strength ratio is balanced and for  $W_p/W_n = 2$ , the PMOS and NMOS transistors are still unbalanced. Fig. 3 shows the schematics and device sizes for the basic logic cells that were used to implement the 1-bit full adders (FA).

### 2.2. Exploring variability and energy efficiency

In order to explore the robustness of the proposed sizing approach, the drain current variability of an inverter (INV3) based on the proposed sizing approach was simulated and compared to two other inverters. The drive strength of the pull-up/down devices of the first inverter (INV1) were balanced and the active area of the PMOS was more than 5X the NMOS active area with  $W_p=420$  nm,  $W_n=80$  nm and  $L_p=L_n=30$  nm. The second inverter (INV2) had the same total area as INV1 but the PMOS/NMOS drive strengths are not balanced ( $W_p=300$  nm,  $W_n=200$  nm and  $L_p=L_n=30$  nm). The active area of the PMOS in INV3 is only 1.1X the NMOS active area where  $W_p=300$  nm,  $W_n=200$  nm,  $L_p=30+4$  nm and  $L_n=30+16$  nm.

Fig. 4 shows the NMOS/PMOS on-currents variability for the above discussed inverters as a function of supply voltage. Monte Carlo

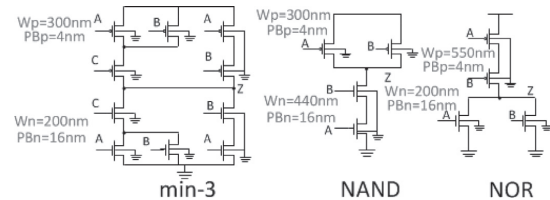


Fig. 3. Schematic view and corresponding device sizes of the basic logic gates used to implement FAs.

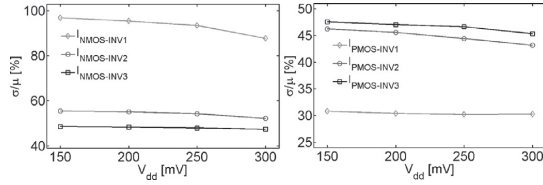


Fig. 4. Percentage variability of the NMOS/PMOS on-currents for different inverter implementations.

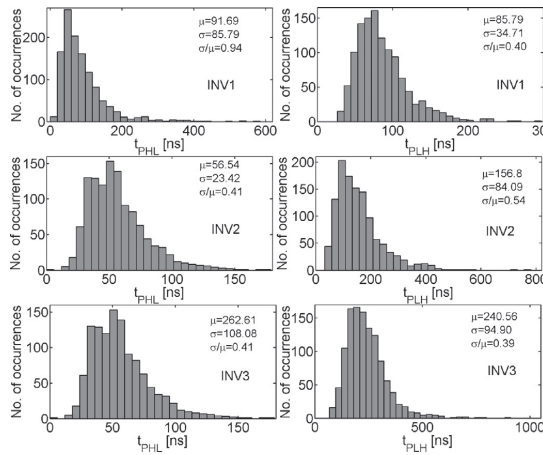


Fig. 5. Rise and fall FO4 delay variability of different sizing approaches at a supply voltage of 200 mV.

simulations have been carried out at the typical process corner (TT) considering mismatch and process variations. The NMOS on-current variability in INV1 is much higher than that of the PMOS. In INV2, the variability of the PMOS on-current is slightly lower than the NMOS on-current variability, but the NMOS is stronger than the PMOS for this inverter. For INV3, the on-current variability of the NMOS and PMOS are almost the same and the drive strength of the transistors are balanced. Therefore, logic cells with relatively equal active areas of PMOS and NMOS devices might benefit from similarity in rise and fall delays variability. Fig. 5 shows Monte Carlo simulations of the rise/fall FO4 delays of INV1, INV2 and INV3 with 3- $\sigma$  accuracy (99.73% target yield) at the TT process corner and 200 mV taking mismatch and process variations into account. It can be observed from Fig. 5 that the variability of the fall delay of INV1 is 2.3X the variability of its rise delay. Despite the small difference in rise and fall delays variability in INV2, its rise delay mean value is 2.8X fall delay mean value. However, the difference in fall and rise delay variability is only 2% for INV3, and the fall delay mean value is comparable to the rise delay mean value. Increasing the channel length of transistors results in longer delays. Nevertheless, as discussed previously, it reduces the delay variability and improves the functional yield of the logic cells. In order to investigate if the drop in the speed of logic cells can be compensated without energy overhead by increasing the supply voltage, the energy of inverter chains with 20 FO4 delay logic depth was simulated versus  $V_{dd}$ . The logic depth of 20 was chosen because as it is discussed in [12] and [13], a logic depth of 20 to 17 results in a balance between the path delay variability and the energy efficiency. Fig. 6 shows the total energy per cycle of 20 FO4 delay inverter chains consist of INV1, INV2 and INV3 versus supply voltage, with a switching activity of 0.25. For example at a target operating frequency of 1 MHz, the energy per operation of INV3 chain is 6.08 fJ (@283 mV) which is 9% lower than the

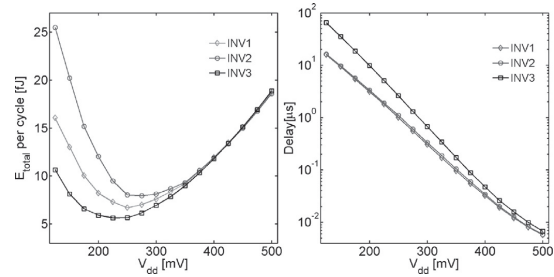


Fig. 6. Energy per cycle and delay of the 20 FO4 delay inverter chains.

energy per operation of INV1 chain (6.68 fJ @ 250 mV) and 24% lower than the energy per operation of the INV2 chain (7.97 fJ @ 254 mV). Therefore, the resultant drop in the speed due to the larger channel lengths can be compensated by increasing the supply voltage without increasing the energy consumption.

### 2.3. Back-gate biasing effects

The FDSOI technology offers a relatively wide range of back-gate biasing voltages, due to the buried oxide, that regulates the threshold voltages of the transistors. The effect of back-gate biasing voltage on the delay and leakage of subthreshold circuits can be estimated taking the exponential dependency of the drain-source current on  $V_{th}$  ( $I_{ds} \propto \exp((V_{GS} - V_{th})/nV_t)$ ) and linear dependency of  $V_{th}$  on back-bias voltage [16] into account.

The linear relationship between the threshold voltage,  $V_{th}$ , and the back-gate voltage,  $V_{BS}$ , of FDSOI devices, can be expressed as [17]:

$$V_{th} = V_{th0} - \gamma V_{BS} \quad (1)$$

In [17],  $\gamma$  was approximated to be 85 mV/V.

Considering the exponential dependency of the drain-to-source current on the threshold voltage in the subthreshold region, we can write the following expressions for the delay ratio and the leakage current ratio for different back-gate biasing voltages with a fixed supply voltage:

$$\frac{t_{D1}}{t_{D0}} \propto \exp((V_{th1} - V_{th0})/nV_t) = \exp(-\gamma V_{BS}/nV_t) \quad (2)$$

$$\frac{I_{leak1}}{I_{leak0}} \propto \exp((V_{th0} - V_{th1})/nV_t) = \exp(\gamma V_{BS}/nV_t) \quad (3)$$

In Eqs. (2) and (3),  $n$  is the inverse slope of the subthreshold current,  $V_{th0}$  is the threshold voltage of the device with no body biasing voltage, and  $V_t$  is the thermal voltage ( $4kT/q \approx 26$  mV at room temperature). We will use these equations later, in Section 4, to compare our calculations to the measurement results.

### 3. Adder circuit design

Fig. 7 illustrates 1-bit FA cells of the two different logic styles. The FA based on min-3 gates [7] was used to implement a 32-bit RCA [8]. A 16-bit RCA was also implemented using the FA based on Boolean logic gates. The layout views of the FAs are shown in Fig. 8. We focused on layout regularity to increase the matching properties of the devices and alleviate local systematic matching errors [18]. There is no rounding and routing in the poly layer. All the poly polygons have single direction, and 106 nm poly pitch was used to be able to apply poly-biasing on transistors gates. As a result, the mismatch between transistors gate lengths should decrease [18], as well as leakage currents and  $I_{on-NMOS}/I_{on-PMOS}$ . Back-bias voltage rails are routed in parallel with the supply and ground rails and well ties are placed on top and bottom of each cell to reduce the device's active area distance to the well ties.

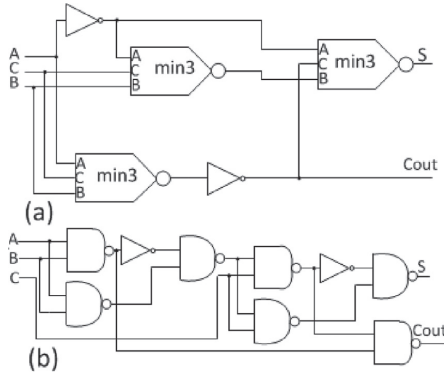


Fig. 7. Block-diagram of 1-bit FA (a) implemented with min-3 gates (b) implemented with Boolean gates.

4. Simulation and measurement results

Fig. 9 shows the PCB and QFN44 socket that was used for measuring the ten chips. Fig. 10 illustrates the test chip block diagram. A toggling input carry was applied to the adders while all the A inputs were shorted to  $V_{dd}$ , and the B inputs connected to ground. This exercised the critical path and caused the longest delay [8]. The RVT devices that were used in the core circuitry had threshold voltages of around 430 mV. The buffers were implemented with LVT transistors to make the delay through the buffers and I/O pads negligible compared to that of the adders. The absolute value of the threshold voltages of the LVT transistors used in the buffers is around 390 mV. An HP 6632A DC power supply was used for the supply voltages of the adders. The input carry signal was generated by an Agilent 33522A function generator. To measure the currents, a Keithley 6485 Picoammeter was used. The output/input waveforms were captured by a ROHDE & SCHWARZ RTE 1022 oscilloscope.

Fig. 11 (a) shows measured energy per operation of the 32-bit adder versus supply voltage at maximum operating speed. The delay of the 32-bit adder versus  $V_{dd}$  is also shown in Fig. 11 (b). The MEP of nine samples was measured for the 32-bit and 16-bit RCAs. The 32-bit RCA achieved a minimum energy point of 20.8 fJ on average at a 300 mV  $V_{dd}$  and the mean delay at this  $V_{dd}$  was 3.2  $\mu$ s. This means that the mean MEP per 1-bit addition is 0.65 fJ for this adder. Measured energy and delay of the 16-bit adder versus supply voltage are depicted in Fig. 12(a) and (b). The average of the minimum energy point of the 16-

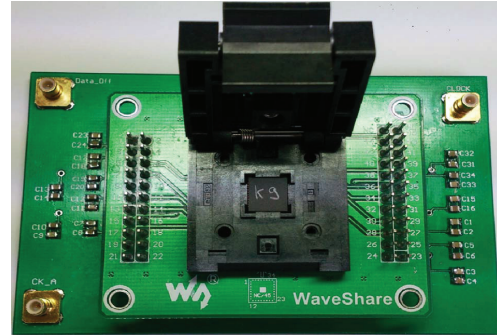


Fig. 9. The PCB and QFN44 socket for measuring chip samples.

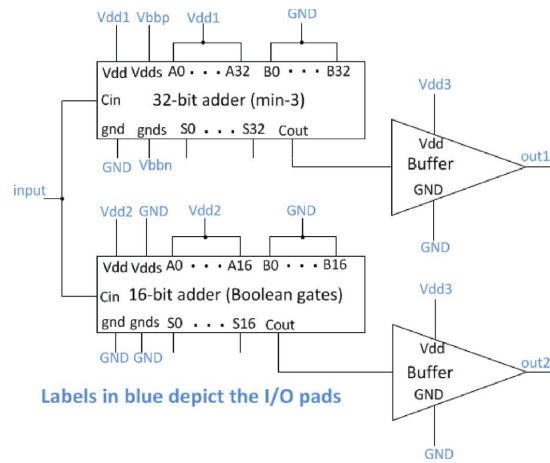


Fig. 10. Block-diagram of the test chip.

bit adder for nine samples was measured to be 12.34 fJ at 250 mV. Thus, the minimum required energy per 1-bit addition of this adder is 0.77 fJ on average. The mean delay of the 16-bit adder was 6.2  $\mu$ s at the MEP (@250 mV).

Fig. 13 shows the measured static power consumption of nine 32-bit RCA and 16-bit RCA samples. During leakage current measurements,

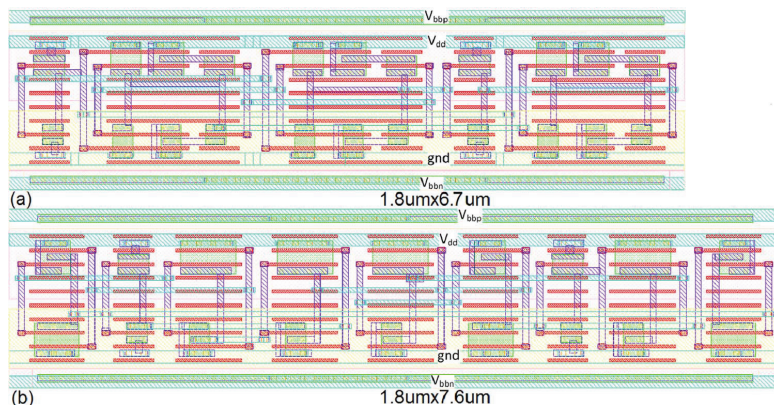


Fig. 8. Layout view of the 1-bit full adder (a) implemented with min-3 gates (b) implemented with Boolean gates.



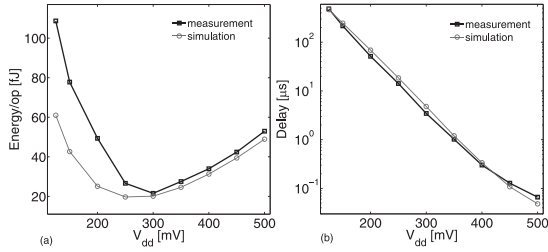


Fig. 11. Measured energy and delay of the 32-bit adder versus  $V_{dd}$ .

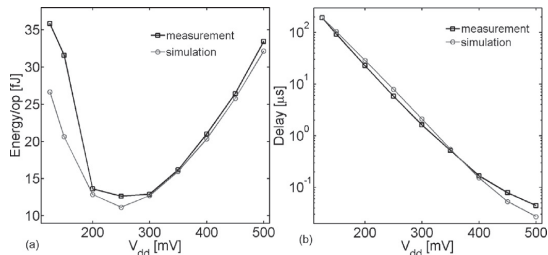


Fig. 12. Measured energy and delay of the 16-bit adder versus  $V_{dd}$ .

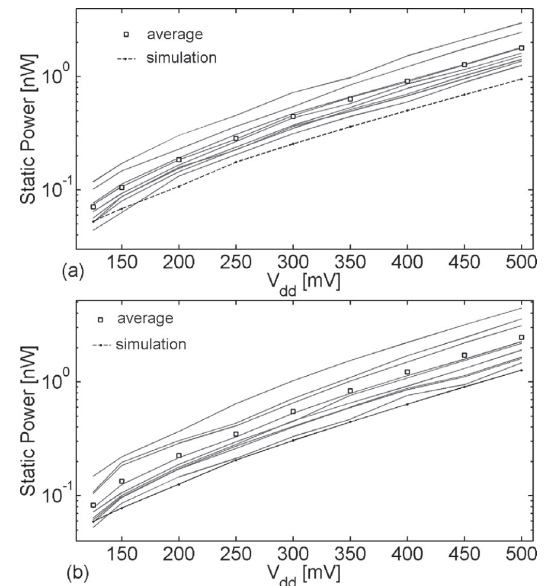


Fig. 13. Measured static power consumption of nine (a) 32-bit adder samples (b) 16-bit adder samples.

using a Keithley 6485 Picoammeter, the carry in of both adders was grounded. Chip number 8 was damaged during these measurements, so its static power consumption is not included in Fig. 13. The simulated and average measured static power consumptions of nine samples is also depicted in Fig. 13 (with square markers).

To draw a fair comparison between the static power of the FAs based on min-3 and Boolean logic gates, the static power consumption of 1-bit FAs were extracted from the mean measured static power in Fig. 13, and is illustrated in Fig. 14. As can be observed from Fig. 14,

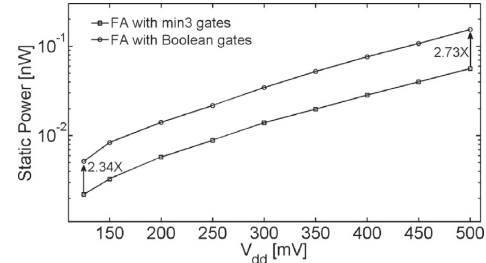


Fig. 14. Static power consumption of the 1-bit FAs.

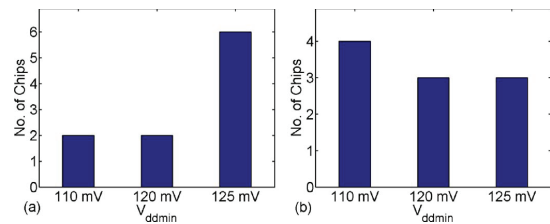


Fig. 15. Minimum  $V_{dd}$  distribution of (a) 32-bit adders implemented with min-3 gates (b) 16-bit adders implemented with Boolean gates.

the static power consumption of the 1-bit FA based on Boolean gates is more than 2X of the static power of the 1-bit FA implemented with min-3 gates. At the supply voltages of 125 mV and 500 mV, the static power consumption of the FA based on Boolean gates is 2.34X and 2.73X the static power of the FA implemented with min-3 gates, respectively.

We measured ten chips to explore the functionality of the adders at extremely low supply voltages. Fig. 15 shows the minimum  $V_{dd}$  of the adders as a histogram for ten measured chips with both PMOS and NMOS back-gates ( $V_{bbp}$  and  $V_{bbn}$ ) shorted to ground. The minimum  $V_{dd}$ s were all between 110 and 125 mV for both types of adders, when having their back-gates connected to ground. In the 32-bit adder case, two chips out of ten measured samples were functional down to 110 mV. For the 16-bit adder, four chip samples out of ten were functional down to 110 mV.

As shown in Fig. 10, the PWELL/NWELL contacts of the 32-bit adder are routed to the I/O pads, which enables applying off-chip back bias voltages to this adder. The  $V_{bbp}$  and  $V_{bbn}$  voltages were generated by off-chip MASCOT 719 DC power supplies. We were able to decrease the minimum  $V_{dd}$  of the first 32-bit adder sample down to 79 mV by applying a 430 mV positive  $V_{bbp}$  to the PMOS transistors, i.e. applying a reverse back bias voltage to the PMOS transistors. The oscilloscope plots of the input/output carries of the 32-bit adder at a supply voltage of 79 mV with  $V_{bbp} = 430$  mV and  $V_{bbn} = 0$  V are shown in Fig. 16. Fig. 17 depicts the input/output carries of the 16-bit adder for a  $V_{dd}$  of 110 mV. The minimum  $V_{dd}$  of all the 32-bit adder samples decreased by applying a reverse back bias (RBB) to the PMOS transistors. The required back-gate voltages for PMOS devices of the 32-bit adders to achieve a minimum functional  $V_{dd}$  of 80 mV, and corresponding leakage currents of the 32-bit adder samples at 80 mV, are listed in Table 1.

Unlike the conventional back biasing of the RVT transistors where  $V_{bbp} = V_{dd} - V_{bb}$  and  $V_{bbn} = V_{bb}$  [20], the absolute values of the PMOS and NMOS back bias voltages are equal in the logic cells we developed, i.e.  $V_{bbp} = -V_{bb}$  and  $V_{bbn} = V_{bb}$ . In order to decrease the delay of the 32-bit RCA, we applied a forward back bias (FBB) voltage equal to 0.25 V ( $V_{bbp} = -0.25$  V and  $V_{bbn} = 0.25$  V). Fig. 18(a) shows the measured delay of the 32-bit adder with three different back biasing schemes as a function of supply voltage. The delay of the 32-bit adder decreased by

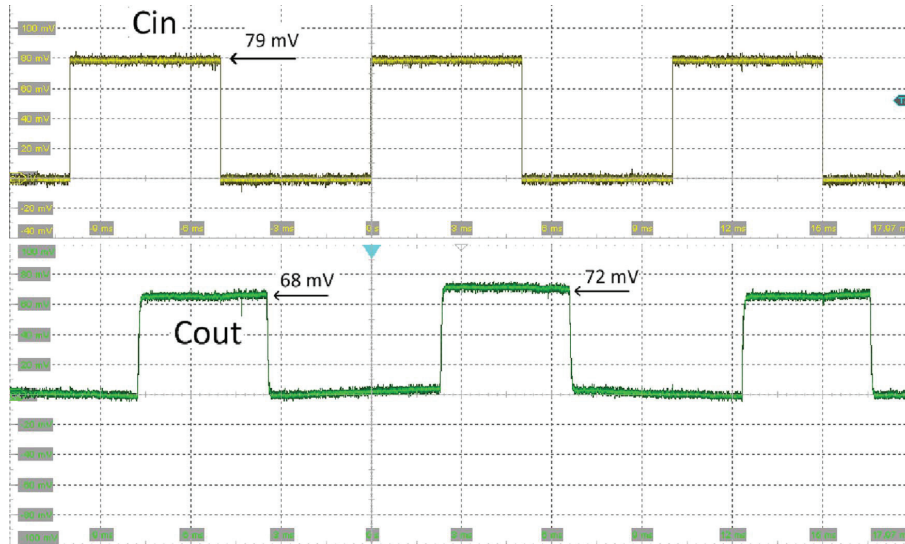


Fig. 16. Oscilloscope plots proving that the 32-bit adder is functional at 79 mV with  $V_{bbp} = 430$  mV and  $V_{bbn} = 0$  V.

39% at 125 mV and 23% at 500 mV when a 0.25 V forward back bias was applied to this adder.

A 0.5 V reverse back bias voltage ( $V_{bbp} = 0.5$  V and  $V_{bbn} = -0.5$  V) was also applied to the adder to reduce the leakage current of the circuit. As can be observed from Fig. 18(b), a static power reduction of 70% at 125 mV and 68% at 500 mV was achieved by applying a 0.5 V back-gate bias voltage to the 32-bit adder. For a supply voltage of 200 mV and 0.25 V FBB, the resulting reduction in delay was measured to be 1.8X, while the RBB of 0.5 V reduced the leakage current by a factor of 3.3X. Eqs. (2) and (3) combined with extracted values based on simulations, for a  $V_{dd}$  of 200 mV, were used for comparisons with

measured data. The inverse slope of the subthreshold current,  $n$ , was found to be 1.22 for the NMOS and 1.18 for the PMOS. The body factor [17] was found to be 64 mV/V for the NMOS, and 71 mV/V for the PMOS, respectively. Using the average value of the parameters for the PMOS and NMOS transistors, the measured reduction in delay of 1.8X was estimated as 1.7X based on Eq. (2), while the measured reduction in the leakage current (RBB of 0.5 V) of 3.3X was estimated to be 2.9X, based on Eq. (3).

Fig. 19 shows the layout view of the 32-bit RCA and the parasitic PWELL/NWELL diodes. A deep-NWELL (D-NWELL) and an NWELL guard-ring was used to isolate the PWELL of the adder from the p-

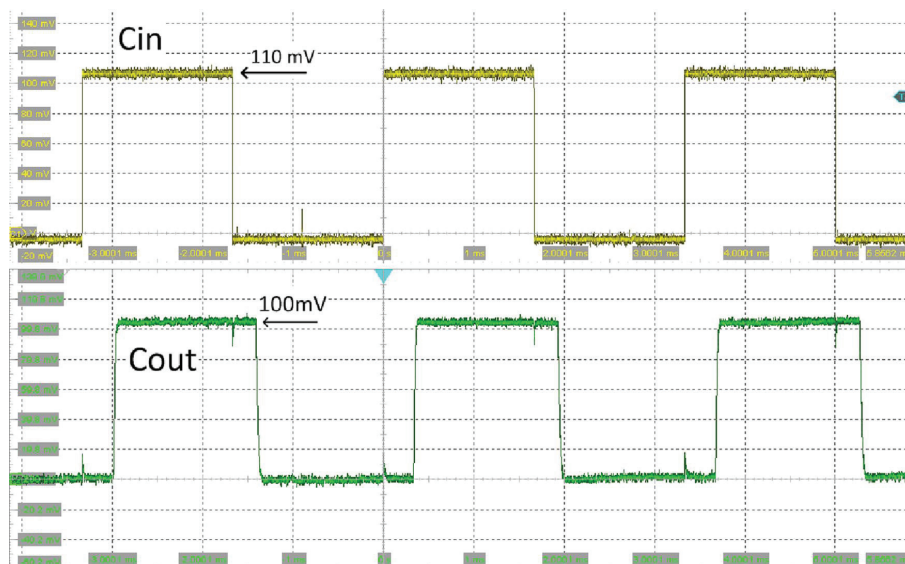


Fig. 17. Oscilloscope plots proving that the 16-bit adder is functional at 110 mV with  $V_{bbp} = V_{bbn} = 0$  V.

Table 1

Required back-bias voltage for the PMOS devices of ten 32-bit adder samples to reduce the minimum functional  $V_{dd}$  of the adders down to 80 mV and the corresponding measured leakage current of each sample at 80 mV.

	Chip1	Chip2	Chip3	Chip4	Chip5	Chip6	Chip7	Chip8	Chip9	Chip10
$V_{bbp}$ [mV]	420	355	530	315	625	535	355	685	610	475
$I_{leak}$ [nA]	0.27	0.25	0.15	0.21	0.29	0.31	0.23	N/A	0.17	0.24

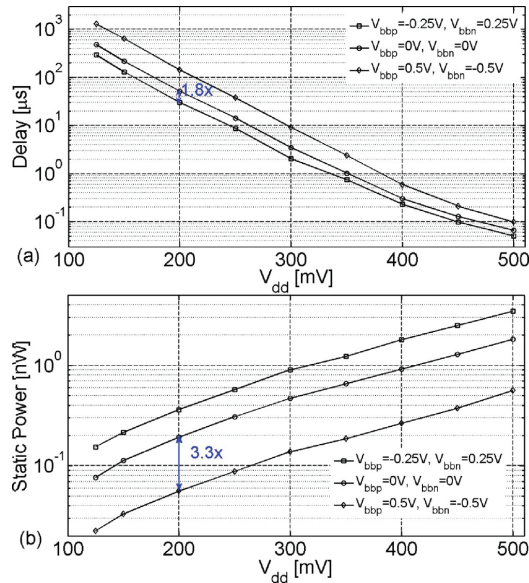


Fig. 18. Measured (a) Delay and (b) static power of the 32-bit adder (first sample) for three back-biasing schemes.

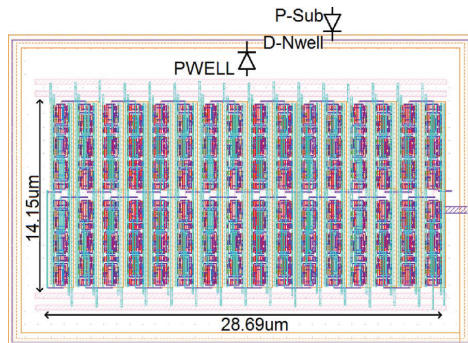


Fig. 19. Layout view of the 32-bit adder and corresponding parasitic PWELL/NWELL diodes.

substrate. The breakdown voltage of the PWELL/NWELL diode restricts the reverse back bias voltage range. For the forward back bias scenario, the limiting factor comes from the threshold voltage of these diodes. Therefore, the applicable reverse back bias voltage to the RVT devices is wider than the forward back bias voltage range. The leakage current of the PWELL/NWELL diode was measured to be 12.6 nA when a 0.25 V forward back bias was applied to the adder. This leakage current increased to 1.44  $\mu$ A when the applied forward back bias voltage was increased to the 0.3 V. Thus, we limited the forward back bias voltage to be 0.25 V to reduce the leakage current through the parasitic diodes.

## 5. Discussion

Table 2 compares the measurement results of the designed adders with the post-layout simulation results of existing works in terms of energy, delay and area. The 32-bit RCA presented here achieved 0.65 fJ per 1-bit addition. This is the lowest energy per 1-bit addition among the works listed in Table 2. In comparison to [9] which has the lowest reported energy per 1-bit addition (1.03 fJ) among the other works, the energy per 1-bit addition of the 32-bit and 16-bit adders are improved by 37% and 25%, respectively.

Comparing the 1-bit addition delay times at 300 mV, the adder in [9] has the shortest delay of 1.7 ns, thanks to the LVT devices and forward body biasing. The 1-bit addition delay times the 32-bit and 16-bit adders in [19] are 28 ns. This means that the adders in [19] are 3.8X and 3.6X faster than the presented 32-bit and 16-bit adders, respectively, when  $V_{bbp} = V_{bnn} = 0$ . As listed in Table 2, the static power consumption of the reported 32-bit RCA in [19] is 15.9X higher than the static power of the 32-bit adder and the 16-bit adder in this work. The low speed of the designed adders was not unexpected considering RVT transistors and longer channel lengths of the devices. Nevertheless, the delay of the 32-bit adder at 300 mV decreased to 2.04  $\mu$ s (i.e. 63.75 ns per 1-bit addition) when a 0.25 V forward back bias was applied. Moreover, there are many applications with very low operating frequency requirements where wireless sensor networks are utilized to monitor phenomena with low sample rates [6,21].

The minimum supply voltage of the 32-bit adder decreased by applying a reverse back-bias voltage to the PMOS devices, and the same trend was observed for all the samples (Table 1). Therefore, the dies position might be towards the slow-NMOS fast-PMOS (SF) process corner.

Despite the fact that the FA based on min-3 gates has 34 transistors and the FA based on Boolean gates has 32 transistors, the footprint area of the FA based on min-3 gates (12.06  $\mu\text{m}^2$ ) is smaller than the area of FA based on Boolean gates (13.68  $\mu\text{m}^2$ ). The area of the 32-bit adder is 3% smaller than the 32-bit adder in [19], while the 16-bit adder has 9% more area in comparison with the 16-bit adder in [19].

The leakage power of the 32-bit RCA was lower than the leakage power of the 16-bit RCA. From Fig. 14, the static power of the 1-bit FA based on Boolean gates is more than 2X of that of the 1-bit FA implemented with min-3 gates. The static power consumption accounts for a considerable part of the total power consumption at extremely low supply voltages where the operating frequency of the system is relatively low. Thus, the leakage current plays a significant role on energy consumption at ultra-low  $V_{dd}$ s and a high leakage current deteriorates the energy consumption of the circuit. Thereby, a lower MEP at a lower supply voltage could be achieved by using FAs based on min-3 gates in the datapath blocks of the system.

Schmitt-Trigger logic cells functioning down to a supply voltage of 62 mV have been reported in [22]. However, these logic cells were not energy and area efficient. An ultra-low voltage subthreshold adder based on static CMOS logic cells, implemented in 65 nm CMOS, have been reported in [23], which was capable of working correctly down to a supply voltage of 84 mV. LVT devices have been used in [23], hence the leakage current is relatively high. Although the minimum reported  $V_{dd}$  is higher compared to [22], the logic cells are more area and power efficient. Thereby, the proposed approach can also be useful for applications powered by an energy harvesting source where the limiting factor comes from the power consumption of the system [24].



**Table 2**  
Comparison with existing works in 28 nm FDSOI technology.

	This work 32-bit adder	This work 16-bit adder	[19] 32-bit adder	[19] 16-bit adder	[9] 9-bit adder
$E_{min}$	20.8* fJ	12.34* fJ	207.4 fJ	74.9 fJ	9.27 fJ
$P_{static}$ @ 0.3 V	0.446* nW	0.549* nW	7.10 nW	3.74 nW	N.A.
Delay @ MEP	3.24* $\mu$ s	6.2* $\mu$ s	0.898 $\mu$ s	0.448 $\mu$ s	0.555 $\mu$ s
$V_{dd}$ @ MEP	300 mV	250 mV	300 mV	300 mV	240 mV
Devices	RVT	RVT	RVT/LVT	RVT/LVT	LVT
Area	406 $\mu$ m <sup>2</sup>	230.3 $\mu$ m <sup>2</sup>	418.56 $\mu$ m <sup>2</sup>	209.28 $\mu$ m <sup>2</sup>	N.A.
Results	Measurement	Measurement	Post-layout	Post-layout	Post-layout

\* Average of nine measured samples.

## 6. Conclusion

The development of ultra-low energy subthreshold adders in a 28 nm FDSOI CMOS technology has been presented. Poly and back-gate biasing techniques has been used to balance PMOS/NMOS strength ratio. This combined with selected building block topology and regular layout which in turn resulted in a robust and energy efficient adder. To the knowledge of the authors, the measured 0.65 fJ energy per 1-bit addition of the 32-bit adder is the lowest measured energy reported so far. Both the 32-bit and the 16-bit adders were functional in the deep subthreshold region during measurements. The minimum functional supply voltage of the 32-bit adder was found to be 79 mV with a 430 mV reverse back-gate bias applied to PMOS transistors. The back biasing knob has been utilized to enhance the performance of the 32-bit adder or reduce its leakage power consumption.

## References

- [1] Y. Tsvitov, Eric vittoz and the strong impact of weak inversion circuits, *IEEE Solid-State Circuits Soc. Newslett.* 13 (3) (2008) 56–58.
- [2] T. Skotnicki, C. Fenouillet-Beranger, C. Gallon, F. Boeuf, S. Monfray, F. Payet, A. Pouydebasque, M. Szczap, A. Farcy, F. Arnaud, S. Clerc, M. Sellier, A. Cathignol, J.P. Schoellkopf, E. Perea, R. Ferrant, H. Mingam, Innovative materials, devices, and cmos technologies for low-power mobile multimedia, *IEEE Trans. Electron Devices* 55 (1) (2008) 96–130.
- [3] A.A. Vatanjou, E. Late, T. Ytterdal, S. Aunet, Ultra-low voltage adders in 28 nm fdsoi exploring poly-biasing for device sizing, 2016 IEEE Nordic Circuits and Systems Conference (NORCAS), (2016), pp. 1–4.
- [4] D. Jacquet, F. Hasbani, P. Flatresse, R. Wilson, F. Arnaud, G. Cesana, T.D. Gilio, C. Lecocq, T. Roy, A. Chhabra, C. Grover, O. Minez, J. Uginet, G. Durieu, C. Adobati, D. Casalotto, F. Nyer, P. Menut, A. Cathelin, I. Vongsavady, P. Magarshack, A 3 ghz dual core processor arm cortex tm -a9 in 28 nm utbb fd-soi cmos with ultra-wide voltage range and energy efficiency optimization, *IEEE J. Solid-State Circuits* 49 (4) (2014) 812–826.
- [5] D. Bol, R. Ambroise, D. Flandre, J.D. Legat, Analysis and minimization of practical energy in 45nm subthreshold logic circuits, 2008 IEEE International Conference on Computer Design, (2008), pp. 294–300.
- [6] B. Zhai, S. Pant, L. Nazhandali, S. Hanson, J. Olson, A. Reeves, M. Minuth, R. Helfand, T. Austin, D. Sylvester, D. Blaauw, Energy-efficient subthreshold processor design, *IEEE Trans. Very Large Scale Integrat. (VLSI) Syst.* 17 (8) (2009) 1127–1137.
- [7] S. Aunet, Y. Berg, Three sub-fJ power-delay-product subthreshold cmos gates, 2005 IFIP International Conference on Very Large Scale Integration, (2005), pp. 465–470.
- [8] V. Beiu, A. Djupdal, S. Aunet, Ultra Low-Power Neural Inspired Addition: When Serial Might Outperform Parallel Architectures, Springer Berlin Heidelberg, Berlin, Heidelberg, 2005.
- [9] H. Attarzadeh, S. Aunet, T. Ytterdal, An ultra-low-power/high-speed 9-bit adder design: analysis and comparison vs. technology from 130nm-1p to utbb fd-soi-28 nm, 2015 Nordic Circuits and Systems Conference (NORCAS): NORCHIP International Symposium on System-on-Chip (SoC), (2015), pp. 1–4.
- [10] S. Hanson, B. Zhai, M. Seok, B. Cline, K. Zhou, M. Singhal, M. Minuth, J. Olson, L. Nazhandali, T. Austin, D. Sylvester, D. Blaauw, Exploring variability and performance in a sub-200-mv processor, *IEEE J. Solid-State Circuits* 43 (4) (2008) 881–891.
- [11] M.Z. Li, C.I. Jeong, M.K. Law, P.I. Mak, M.I. Vai, S.H. Pun, R.P. Martins, Energy optimized subthreshold vlsi logic family with unbalanced pull-up/down network and inverse narrow-width techniques, *IEEE Trans. Very Large Scale Integrat. (VLSI) Syst.* 23 (12) (2015) 3119–3123.
- [12] B. Zhai, S. Hanson, D. Blaauw, D. Sylvester, Analysis and mitigation of variability in subthreshold design, ISLPED '05. Proceedings of the 2005 International Symposium on Low Power Electronics and Design, 2005. (2005), pp. 20–25.
- [13] M. Seok, D. Jeon, C. Chakrabarti, D. Blaauw, D. Sylvester, Pipeline strategy for improving optimal energy efficiency in ultra-low voltage design, 2011 48th ACM/EDAC/IEEE Design Automation Conference (DAC), (2011), pp. 990–995.
- [14] M. Belleville, O. Faynot, Evolution of deep submicron bulk and soi technologies, in: C. Piguet (Ed.), *Low-Power CMOS Circuits Technology, Logic Design and CAD Tools*, Taylor & Francis Group, 2006.
- [15] A. Ferré, J. Figueras, Leakage in cmos nanometric technologies, in: C. Piguet (Ed.), *Low-Power CMOS Circuits Technology, Logic Design and CAD Tools*, Taylor & Francis Group, 2006.
- [16] J.P. Noel, O. Thomas, M.A. Jaud, O. Weber, T. Poiroux, C. Fenouillet-Beranger, P. Rivallin, P. Scheiblin, F. Andrieu, M. Vinet, O. Rozeau, F. Boeuf, O. Faynot, A. Amara, Multi-v<sub>t</sub> utbb fdsoi device architectures for low-power cmos circuit, *IEEE Trans. Electron Devices* 58 (8) (2011) 2473–2482.
- [17] E. Beigné, A. Valentian, I. Miro-Panades, R. Wilson, P. Flatresse, F. Abouzeid, T. Benoist, C. Bernard, S. Bernard, O. Billoint, S. Clerc, B. Giraud, A. Grover, J.L. Coz, J.P. Noel, O. Thomas, Y. Thonnart, A 460 mhz at 397 mv, 2.6 ghz at 1.3 v, 32 bits vliw dsp embedding f max tracking, *IEEE J. Solid-State Circuits* 50 (1) (2015) 125–136.
- [18] L.L. Lewyn, T. Ytterdal, C. Wulff, K. Martin, Analog circuit design in nanoscale cmos technologies, *Proc. IEEE* 97 (10) (2009) 1687–1714.
- [19] R. Taco, I. Levi, M. Lanuzza, A. Fish, Extended exploration of low granularity back biasing control in 28nm utbb fd-soi technology, 2016 IEEE International Symposium on Circuits and Systems (ISCAS), (2016), pp. 41–44.
- [20] A. Bryant, J. Brown, P. Cottrell, M. Ketchen, J. Ellis-Monaghan, E.J. Nowak, Low-power cmos at vdd = 4kt/q, Device Research Conference. Conference Digest, (2001), pp. 22–23.
- [21] L. Nazhandali, M. Minuth, T. Austin, Sensebench: toward an accurate evaluation of sensor network processors, *IEEE International. 2005 Proceedings of the IEEE Workload Characterization Symposium*, 2005. (2005), pp. 197–203.
- [22] N. Lotze, Y. Manoli, A 62 mv 0.13  $\mu$ m cmos standard-cell-based design technique using Schmitt-Trigger logic, 2011 IEEE International Solid-State Circuits Conference, (2011), pp. 340–342.
- [23] A.A. Vatanjou, T. Ytterdal, S. Aunet, Energy efficient sub/near-threshold ripple-carry adder in standard 65nm cmos, 2015 6th Asia Symposium on Quality Electronic Design (ASQED), (2015), pp. 7–12.
- [24] W. Lim, I. Lee, D. Sylvester, D. Blaauw, 8.2 batteryless sub-nw cortex-m0+; processor with dynamic leakage-suppression logic, 2015 IEEE International Solid-State Circuits Conference - (ISSCC) Digest of Technical Papers, (2015), pp. 1–3.



**Ali Asghar Vatanjou** received his M.Sc. from University of Tabriz in 2010. During his M.Sc. degree, he worked towards pipeline ADC design. Since 2012, he started his PhD at Circuits and Systems Group, Norwegian University of Science and Technology (NTNU). He is currently working towards his PhD thesis at NTNU with main focus on ultra-low power and voltage digital circuit design. His main research interests include ultra-low power and voltage VLSI and mixed-mode circuit design.



**Even Låte** graduated from the Norwegian University of Science and Technology (NTNU) with a M.Sc. degree in Electrical Engineering in 2014. His work on "Transaction Level Modeling of a PCI Express Root Complex" was awarded with the best master's thesis prize within the field of microelectronics at NTNU. Since the fall of 2014, Even has been employed as a PhD candidate at the Circuits and Systems Group. His research focus is mitigation of the dark silicon effect by designing ultra-low power CMOS memory for use in the Single-ISA Heterogeneous Many-Core Computer project at NTNU.



**Trond Ytterdal** received his M.Sc. and Ph.D. degrees in electrical engineering from the Norwegian Institute of Technology in 1990 and 1995, respectively. He is a Professor at the Department of Electronics and Telecommunications, Norwegian University of Science and Technology. Current main research interests include design of analog integrated circuits and modeling of novel nanoscale transistors. He has authored and co-authored more than 180 scientific papers in international journals and conference proceedings. He is a co-author of three books. Prof. Ytterdal is a member of The Norwegian Academy of Technological Sciences and a Senior Member of IEEE.



**Snorre Aunet** received the Cand. Scient. degree in informatics from the University of Oslo (UiO) in 1993, and the Dr. Ing. degree in physical electronics from the Norwegian University of Science and Technology (NTNU), in 2002. He worked with ASIC design at Nordic VLSI from 1994 to 1997, prior to doctoral studies. Later, he worked at NTNU and UiO, and is currently a professor at NTNU. He has been a visiting researcher at the University of Paderborn (2004–2012) and at University of California, San Diego (UCSD), during the academic year 2015/2016. Research interests include ultra low-power mixed-signal circuits.



4.10 *paper X*

**A sub-50 mV to 1 V Low-Power Level Shifter in 28 nm  
UTBB-FDSOI**

This paper is not included due to copyright available at <https://doi.org/10.1109/TCSII.2018.2871637>





4.11 *Appendix*





# ASQED 2015 Best Paper Candidates

## 1A.2

### **Energy Efficient Sub/Near-Threshold Ripple-Carry Adder in Standard 65 nm CMOS**

*Ali Asghar Vatanjou, Trond Ytterdal, Snorre Aunet*

**Norwegian University of Science and Technology, Trondheim, Norway**

## 2B.1

### **True 3D Antenna for UHF RFID Application**

*Yongsheng Zhang, Bin Wang, Haipeng Zhang, Weixin Kong\**

**Hangzhou University of Electronic Science and Technology \*Rice Microelectronics**

## 4A.2

### **A New 600V Partial SOI LDMOS with Step-doped Drift Region**

*Yue Hu<sup>1</sup>, Hao Wang<sup>1</sup>, Caixia Du<sup>1</sup>, Yuzhun Du<sup>1</sup>, Peigang Deng<sup>1</sup>, Jin He<sup>1</sup>, Lei Song<sup>2</sup>,*

*Haiqin Zhou<sup>3</sup> and Yong Wu<sup>3</sup>*

**<sup>1</sup>Peking University Shenzhen, <sup>2</sup>Shenzhen SuperD Co. Ltd., <sup>3</sup>Tianma Micro-Electronics Co. Ltd.**

# **ASQED 2015 Best Paper**

**1A.2**

**Energy Efficient Sub/Near-Threshold Ripple-Carry Adder in Standard 65 nm CMOS**

*Ali Asghar Vatanjou, Trond Ytterdal, Snorre Aunet*

**Norwegian University of Science and Technology, Trondheim, Norway**

## BIBLIOGRAPHY

- [1] Tsvividis, Y., "Eric Vittoz and the Strong Impact of Weak Inversion Circuits," Solid-State Circuits Society Newsletter, IEEE , vol.13, no.3, pp.56,58, Summer 2008.
- [2] A. Ferré , J. Figueras, Leakage in CMOS nanometric technologies, in: C. Piguet (Ed.), Low-Power CMOS Circuits Technology, Logic Design and CAD Tools, Taylor & Francis Group, 2006.
- [3] J. Burr and A. Peterson, "Ultra low power CMOS technology", 3rd NASA Symposium on VLSI Design, 1991, pp. 11.1.1- 11.1.12.
- [4] A. Wang, et all., "Optimal supply and threshold scaling for subthreshold CMOS circuits," Proceedings IEEE Computer Society Annual Symposium on VLSI. New Paradigms for VLSI Systems Design. ISVLSI 2002, Pittsburgh, PA, 2002, pp. 5-9.
- [5] E. Vittoz, Weak Inversion for Ultimate Low-Power Logic, in: C. Piguet (Ed.), Low-Power CMOS Circuits Technology, Logic Design and CAD Tools, Taylor & Francis Group, 2006.
- [6] J. Myers, A. Savanth, R. Gaddh, D. Howard, P. Prabhat and D. Flynn, "A Subthreshold ARM Cortex-M0+ Subsystem in 65 nm CMOS for WSN Applications with 14 Power Domains, 10T SRAM, and Integrated Voltage Regulator," in IEEE Journal of Solid-State Circuits, vol. 51, no. 1, pp. 31-44, Jan. 2016.
- [7] N. Lotze and Y. Manoli, "A 62 mV 0.13 $\mu$ m CMOS Standard-Cell-Based Design Technique Using Schmitt-Trigger Logic," in IEEE Journal of Solid-State Circuits, vol. 47, no. 1, pp. 47-60, Jan. 2012.
- [8] W. Lim, I. Lee, D. Sylvester and D. Blaauw, "8.2 Batteryless Sub-nW Cortex-M0+ processor with dynamic leakage-suppression logic," 2015

- 
- IEEE International Solid-State Circuits Conference - (ISSCC) Digest of Technical Papers, San Francisco, CA, 2015, pp. 1-3.
- [9] H. Esmailzadeh, E. Blem, R. S. Amant, K. Sankaralingam and D. Burger, "Dark silicon and the end of multicore scaling," 2011 38th Annual International Symposium on Computer Architecture (ISCA), San Jose, CA, 2011, pp. 365-376.
- [10] S. Jain et al., "A 280mV-to-1.2V wide-operating-range IA-32 processor in 32nm CMOS," 2012 IEEE International Solid-State Circuits Conference, San Francisco, CA, 2012, pp. 66-68.
- [11] B. Zhai, R. G. Dreslinski, D. Blaauw, T. Mudge and D. Sylvester, "Energy efficient near-threshold chip multi-processing," Proceedings of the 2007 international symposium on Low power electronics and design (ISLPED '07), Portland, OR, 2007, pp. 32-37.
- [12] N. Pinckney et al., "Impact of FinFET on Near-Threshold Voltage Scalability," in IEEE Design & Test, vol. 34, no. 2, pp. 31-38, April 2017.
- [13] M. J. M. Pelgrom, A. C. J. Duinmaijer and A. P. G. Welbers, "Matching properties of MOS transistors," in IEEE Journal of Solid-State Circuits, vol. 24, no. 5, pp. 1433-1439, Oct 1989.
- [14] Bo Zhai, S. Hanson, D. Blaauw and D. Sylvester, "Analysis and mitigation of variability in subthreshold design," ISLPED '05. Proceedings of the 2005 International Symposium on Low Power Electronics and Design, 2005., 2005, pp. 20-25.
- [15] Ali Asghar Vatanjou, Even Låte, Trond Ytterdal, Snorre Aunet, "Ultra-low voltage and energy efficient adders in 28 nm FDSOI exploring poly-biasing for device sizing", Microprocessors and Microsystems, Volume 56, 2018, Pages 92-100, ISSN 0141-9331.
- [16] A. A. Vatanjou, T. Ytterdal and S. Aunet, "28 nm UTBB-FDSOI energy efficient and variation tolerant custom digital-cell library with application to a subthreshold MAC block," 2016 MIXDES - 23rd International Conference Mixed Design of Integrated Circuits and Systems, Lodz, 2016, pp. 105-110.

- 
- [17] "ASQED 2015 Best Paper candidates," 2015 6th Asia Symposium on Quality Electronic Design (ASQED), Kula Lumpur, 2015, pp. 1-2.
- [18] J. E. Bjerkedok, A. A. Vatanjou, T. Ytterdal and S. Aunet, "Modular layout-friendly cell library design applied for subthreshold CMOS," 2014 NORCHIP, Tampere, 2014, pp. 1-6.
- [19] A. A. Vatanjou, T. Ytterdal and S. Aunet, "Energy efficient sub/near-threshold ripple-carry adder in standard 65 nm CMOS," 2015 6th Asia Symposium on Quality Electronic Design (ASQED), Kula Lumpur, 2015, pp. 7-12.
- [20] A. A. Vatanjou, T. Ytterdal and S. Aunet, "Exploiting short channel effects and multi-Vt technology for increased robustness and reduced energy consumption, with application to a 16-bit subthreshold adder implemented in 65 nm CMOS," 2015 European Conference on Circuit Theory and Design (ECCTD), Trondheim, 2015, pp. 1-4.
- [21] A. A. Vatanjou, T. Ytterdal and S. Aunet, "4 Sub-/near-threshold flip-flops with application to frequency dividers," 2015 European Conference on Circuit Theory and Design (ECCTD), Trondheim, 2015, pp. 1-4.
- [22] Even Låte, A. A. Vatanjou, T. Ytterdal and S. Aunet, "Comparative analysis of flip-flop architectures for subthreshold applications in 28nm FDSOI," 2015 Nordic Circuits and Systems Conference (NORCAS): NORCHIP & International Symposium on System-on-Chip (SoC), Oslo, 2015, pp. 1-4.
- [23] Even Låte, Ali Asghar Vatanjou, Trond Ytterdal, Snorre Aunet, "Extended Comparative Analysis of Flip-Flop Architectures for Subthreshold Applications in 28 nm FD-SOI", *Microprocessors and Microsystems*, Volume 48, 2017, Pages 11-20, ISSN 0141-9331.
- [24] A. A. Vatanjou, E. Late, T. Ytterdal and S. Aunet, "Ultra-low voltage adders in 28 nm FDSOI exploring poly-biasing for device sizing," 2016 IEEE Nordic Circuits and Systems Conference (NORCAS), Copenhagen, 2016, pp. 1-4.
- [25] A. A. Vatanjou, T. Ytterdal and S. Aunet, "An Ultra-Low Voltage and Low-Energy Level Shifter in 28-nm UTBB-FDSOI," in *IEEE Transac-*

- 
- tions on Circuits and Systems II: Express Briefs, vol. 66, no. 6, pp. 899-903, June 2019.
- [26] T. G. Noll and E. De Man, "Pushing the performance limits due to power dissipation of future ULSI chips," [Proceedings] 1992 IEEE International Symposium on Circuits and Systems, San Diego, CA, 1992, pp. 1652-1655 vol.4.
- [27] N. Reynders and W. Dehaene, "Variation-Resilient Building Blocks for Ultra-Low-Energy Sub-Threshold Design," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 59, no. 12, pp. 898-902, Dec. 2012.
- [28] S. Hanson et al., "Exploring Variability and Performance in a Sub-200-mV Processor," in IEEE Journal of Solid-State Circuits, vol. 43, no. 4, pp. 881-891, April 2008.
- [29] D. Hampel, K. J. Prost, and N. R. Scheinberg, "Threshold Logic Using Complementary MOS Device," U.S. Patent 3 900 742, Aug. 19, 1975.
- [30] S. Aunet, "On the reliability of ultra-low voltage circuits built from minority-3 gates," 2011 20th European Conference on Circuit Theory and Design (ECCTD), Linkoping, 2011, pp. 540-543.
- [31] N. Ickes et al., "A 28 nm 0.6 V Low Power DSP for Mobile Applications," in IEEE Journal of Solid-State Circuits, vol. 47, no. 1, pp. 35-46, Jan. 2012.
- [32] J. Kwong and A. Chandrakasan, "Variation-driven device sizing for minimum energy sub-threshold circuits," in Proc. ISLPED, 2006, pp. 8-13.
- [33] [www.mathworld.com](http://www.mathworld.com)
- [34] D. Bol, R. Ambroise, D. Flandre and J. D. Legat, "Analysis and minimization of practical energy in 45nm subthreshold logic circuits," 2008 IEEE International Conference on Computer Design, Lake Tahoe, CA, 2008, pp. 294-300.
- [35] A. A. Vatanjou, T. Ytterdal and S. Aunet, "Energy efficient sub/near-threshold ripple-carry adder in standard 65 nm CMOS," 2015 6th Asia Symposium on Quality Electronic Design (ASQED), Kula Lumpur, 2015, pp. 7-12.

- 
- [36] L. Schjolden, "Low Energy Implementation of Robust Digital Arithmetic in Sub/Near-Threshold Nanoscale CMOS For Ultrasound Beamforming," Norwegian University of Science and Technology, June 2013.
- [37] M. E. S. Elrabaa and M. I. Elmasry, "Split-Gate Logic circuits for multi-threshold technologies," ISCAS 2001. The 2001 IEEE International Symposium on Circuits and Systems (Cat. No.01CH37196), Sydney, NSW, 2001, pp. 798-801 vol. 4.
- [38] R. R. Troutman, "VLSI limitations from drain-induced barrier lowering," IEEE Trans. Electron Devices, vol. ED-26, no. 4, pp. 461-469, Apr. 1979.
- [39] C. Y. Lu and J. M. Sung, "Reverse short-channel effects on threshold voltage in submicrometer salicide devices," IEEE Electron Device Lett., vol. 10, no. 10, pp. 446-448, Oct. 1989.
- [40] Wang, P.P., "Device characteristics of short-channel and narrow-width MOSFET's," in Electron Devices, IEEE Transactions on, vol.25, no.7, pp.779-786, Jul 1978.
- [41] Akers, L.A., "The inverse-narrow-width effect," in Electron Device Letters, IEEE, vol.7, no.7, pp.419-421, Jul 1986.
- [42] T. H. Kim, J. Keane, H. Eom and C. H. Kim, "Utilizing Reverse Short-Channel Effect for Optimal Subthreshold Circuit Design," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 15, no. 7, pp. 821-829, July 2007.
- [43] Liu Xinfu et al., "A study of inverse narrow width effect of 65nm low power CMOS technology," 2008 9th International Conference on Solid-State and Integrated-Circuit Technology, Beijing, 2008, pp. 1138-1141.
- [44] Jong-Wook Lee, Hyung-Ki Kim, Min-Rok Oh and Yo-Hwan Koh, "Threshold voltage dependence of LOCOS-isolated thin-film SOI NMOS-FET on buried oxide thickness," in IEEE Electron Device Letters, vol. 20, no. 9, pp. 478-480, Sept. 1999.
- [45] D. Jacquet et al., "A 3 GHz Dual Core Processor ARM Cortex TM - A9 in 28 nm UTBB FD-SOI CMOS With Ultra-Wide Voltage Range and

- 
- Energy Efficiency Optimization,” in *IEEE Journal of Solid-State Circuits*, vol. 49, no. 4, pp. 812-826, April 2014.
- [46] P. G. Drennan, M. L. Kniffin and D. R. Locascio, ”Implications of Proximity Effects for Analog Design,” *IEEE Custom Integrated Circuits Conference 2006*, San Jose, CA, 2006, pp. 169-176.
- [47] L.L. Lewyn, T. Ytterdal, C. Wulff, K. Martin, Analog circuit design in nanoscale cmos technologies, *Proc. IEEE* 97 (10) (2009) 1687–1714.
- [48] Beiu, V.; Djupdal, A.; Aunet, S., ”Ultra Low-Power Neural Inspired Addition: When Serial Might Outperform Parallel Architectures,” *Lecture Notes in Computer Science, Computational Intelligence and Bioinspired Systems*, Springer, vol. 3512, pp. 486, 493, 2005.
- [49] B. H. Calhoun and A. Chandrakasan, ”Ultra-dynamic voltage scaling using sub-threshold operation and local voltage dithering in 90nm CMOS,” *ISSCC. 2005 IEEE International Digest of Technical Papers. Solid-State Circuits Conference, 2005.*, San Francisco, CA, 2005, pp. 300-599 Vol. 1.
- [50] N. Reynders and W. Dehaene, ”A 190mV supply, 10MHz, 90nm CMOS, pipelined sub-threshold adder using variation-resilient circuit techniques,” *IEEE Asian Solid-State Circuits Conference 2011, Jeju, 2011*, pp. 113-116.
- [51] R. Taco, I. Levi, M. Lanuzza, A. Fish, Extended exploration of low granularity back biasing control in 28nm utbb fd-soi technology, *2016 IEEE International Symposium on Circuits and Systems (ISCAS)*, (2016), pp. 41–44.
- [52] H. Attarzadeh, S. Aunet, T. Ytterdal, An ultra-low-power/high-speed 9-bit adder design: analysis and comparison vs. technology from 130nm-lp to utbb fd-soi-28 nm, *2015 Nordic Circuits and Systems Conference (NORCAS): NORCHIP International Symposium on System-on-Chip (SoC)*, (2015), pp. 1–4.
- [53] Y. Ueda et al., ”6.33mW MPEG audio decoding on a multimedia processor,” *2006 IEEE International Solid State Circuits Conference - Digest of Technical Papers*, San Francisco, CA, 2006, pp. 1636-1645.



- 
- [54] M. Afghahi, "A robust single phase clocking for low power, high-speed VLSI applications," in *IEEE Journal of Solid-State Circuits*, vol. 31, no. 2, pp. 247-254, Feb. 1996.
- [55] Y. Shizuku, T. Hirose, N. Kuroki, M. Numa and M. Okada, "A 24-transistor static flip-flop consisting of norns and inverters for low-power digital vlsis," 2014 IEEE 12th International New Circuits and Systems Conference (NEWCAS), Trois-Rivieres, QC, 2014, pp. 137-140.
- [56] S. Okugawa and N. Inoue, "Systematic design of D flip-flops using two state variables," in *Electronics Letters*, vol. 23, no. 17, pp. 909-910, 13 August 1987.
- [57] N. Kawai et al., "A fully static topologically-compressed 21-transistor flip-flop with 75% power saving," 2013 IEEE Asian Solid-State Circuits Conference (A-SSCC), Singapore, 2013, pp. 117-120.
- [58] M. Seok, D. Blaauw and D. Sylvester, "Robust Clock Network Design Methodology for Ultra-Low Voltage Operations," in *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 1, no. 2, pp. 120-130, June 2011.
- [59] J. R. Tolbert, X. Zhao, S. K. Lim and S. Mukhopadhyay, "Analysis and Design of Energy and Slew Aware Subthreshold Clock Systems," in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 30, no. 9, pp. 1349-1358, Sept. 2011.
- [60] X. Zhao, J. R. Tolbert, C. Liu, S. Mukhopadhyay and S. K. Lim, "Variation-aware clock network design methodology for ultra-low voltage (ULV) circuits," *IEEE/ACM International Symposium on Low Power Electronics and Design*, Fukuoka, 2011, pp. 9-14.
- [61] M. Seok, D. Jeon, C. Chakrabarti, D. Blaauw and D. Sylvester, "Pipeline strategy for improving optimal energy efficiency in ultra-low voltage design," 2011 48th ACM/EDAC/IEEE Design Automation Conference (DAC), New York, NY, 2011, pp. 990-995.
- [62] T. Ozaki, T. Hirose, H. Asano, N. Kuroki and M. Numa, "Fully-Integrated High-Conversion-Ratio Dual-Output Voltage Boost Converter With MPPT for Low-Voltage Energy Harvesting," in *IEEE Journal of Solid-State Circuits*, vol. 51, no. 10, pp. 2398-2407, Oct. 2016.