Minimization of dead time effect on bridge converter output voltage quality by use of advanced gate drivers

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***Abstract*—This paper presents a voltage-controlled multistage gate driver topology for delay time minimization that improves the converter output voltage quality while supplying a motor load. Three gate driver topologies for SiC MOSFETs are compared based on their dead time requirement in a bridge leg converter. Experimental results of the gate driver delay times are reported and are used as input to a simulated motor drive application. Results show that turn-off delay times can be reduced by up to 74 % for the multistage driver compared to the conventional counterpart when the rate of change for the converter voltage output is limited to 10 V/ns. Furthermore, minimizing the dead time increases the linearity region of the output voltage from the converter by 1.8 % to 3.8 % and reduces the current THD in the linear region by up to 7.7 % when switching at 15 kHz.**

***Index Terms*—Gate driver, wide band-gap, SiC MOSFET, dead time**

I. Introduction

Wide band-gap (WBG) semiconductor devices, such as silicon carbide (SiC) and gallium nitride (GaN) are commercially available and continue to increase their market share. Compared to their silicon (Si) counterparts, they enable faster switching, lower on-state resistance, higher blocking voltages and operation under higher temperatures [1]. Among the two, SiC is currently the most mature technology and it is assumed that SiC devices will take large market shares in high voltage and high power segments within the power electronic markets in the years to come [2], [3].

In motor drives, voltage-source inverters (VSI) are commonly used. A typical setup with a converter fed motor load is shown in Fig. 1. Replacing Si IGBTs with SiC MOSFETs of similar rating can improve converter performance in several ways. As the forward voltage drop of IGBTs are eliminated in MOSFETs, the conduction losses are reduced. Moreover, in motor drives, the switching frequency can be increased while having the same total switching losses as tail current losses are eliminated using SiC MOSFETs [4]. Yet, the switching speed cannot be increased as the cable length, winding insulation and induced bearing currents limit the maximum allowable dv/dt from the converter [5]. Furthermore, slowing down the SiC MOSFET to the same speed as IGBT results in larger turn-on and turn-off delay times ($T_{d,on}$ and $T_{d,off}$) and thus higher dead time (T_{dt}) requirement when using traditional gate drivers.

A. Dead time

To avoid shoot through when switching a bridge leg, a dead time where both switches are turned off must be added as indicated in Fig. 2. The dead time must be large enough so that the conducting switch is turned completely off before it is safe to turn on the complementary switch. In addition, a safety margin is usually added to ensure that the switch will not be turned back on due to the Miller effect when turning on the complementary switch. The minimum dead time is given by Eq. 1 where $T_{dv/dt}$ and $T_{di/dt}$ is the voltage and current commutations and T_{safe} is the added safety margin.

$$T_{dt} = T_{d,off} + T_{dv/dt} + T_{di/dt} + T_{safe} \tag{1}$$

Due to the Miller plateau's dependency on load current and junction temperature, $T_{d,off}$ and, thus, the dead time requirement will depend on the load current and junction temperature as well. Usually, the dead time is set based on the operating point with the largest dead time requirement. However, load current dependent dead time can be decreased by adaptive gate driving [6].

During dead time, the load current will be freewheeling through the anti-parallel diode of either the upper or the lower switch. For a positive load current, it must conduct through the lower anti-parallel diode thus dragging the bridge leg midpoint down to the negative DC-link voltage. Likewise for a negative load current that must conduct through the upper anti-parallel diode thus dragging the bridge leg midpoint up to the positive DC-link voltage. This gives voltage pulses that are load current dependent as shown in Fig. 2. Furthermore, if the body diode of SiC MOSFETs are used as anti-parallel diodes instead of an external Si power diode, the conduction losses during

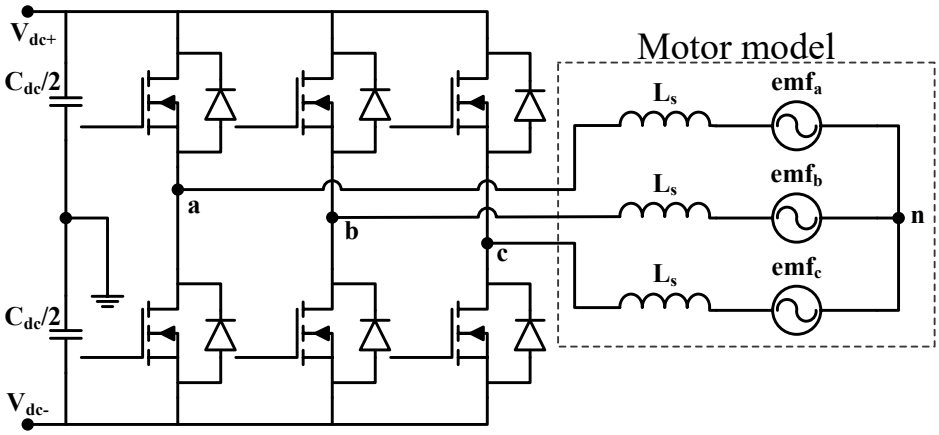


Fig. 1: Schematic diagram of a three phase inverter and the equivalent motor model.

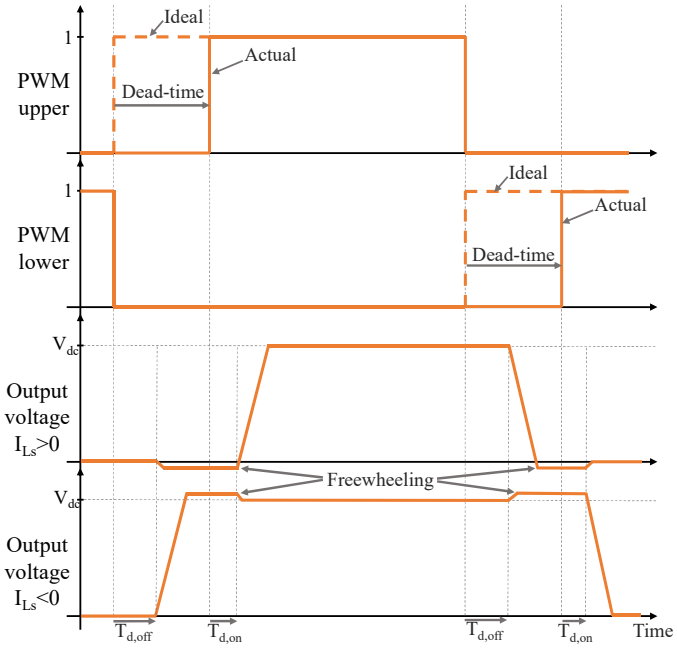


Fig. 2: Theoretical waveforms showing the impact from dead time in a bridge leg.

freewheeling are increased due to the higher forward voltage drop of WBG devices. Hence, minimizing dead time could increase the efficiency as well as the output voltage quality.

The dead time will affect the minimum pulse width (MPW) that can be allowed in PWM modulation. All PWM pulses shorter than MPW are blanked out. Thus, large dead times results in distorted voltage output that is further away from the ideal shape [6], [7].

This paper proposes an advanced multistage gate driver topology designed for minimizing the dead time requirement and investigates the impact from gate drivers on delay times and thus dead time requirements in a motor drive application. Firstly, three different gate driver topologies are presented and experimental results for minimal delay times are reported. Furthermore, the experimental results are transferred to a motor drive application to assess the impact of the gate drivers. Simulations are performed where the motor drive is controlled using three widespread PWM modulation techniques both for a conventional type gate driver and the multistage gate driver. Improvements of the output voltage quality and the THD of the line current are reported.

II. Gate Drivers

A gate driver is the circuitry that controls the turn-on and turn-off switching transients of a transistor. This section presents the three gate driver topologies that are validated experimentally.

The speed of the switching transient is determined according to the gate current delivered to the switching device [8], [9]. The most commonly used gate driver, termed conventional gate driver (CGD) in this paper, is shown in Fig. 3a. Its simplicity makes it an attractive solution, but it has limited degrees of freedom. It consists of a buffer stage with separate gate resistors for turn-on and turn-off. The gate resistor is usually chosen to meet the dv/dt limit for the application. However, as the delay times depends on the time constant created by the gate resistor and the input capacitor of the MOSFET, a large gate resistor gives large time delays thus increasing the requirements for dead time and MPW.

Several other gate driver concepts are found in the literature. A slightly more complex driver shown in Fig. 3b, termed RC driver in this paper, gives a new degree of freedom that boosts the gate current in the initial phase of the switching transient. The initial boost can be used to counter the delay time or even increase the switching speed [10] depending on the size of the chosen boost capacitor. In the experimental validation in this paper, the size of the boost capacitors is chosen to act on the delay times without affecting dv/dt or di/dt.

More complex gate drivers aims to act more directly on the switching transient by providing different gate resistors for the different stages within the switching event. The goal could be reduced switching losses without increasing the

current overshoot by boosting the voltage commutation [11], or achieving separate control of dv/dt and di/dt [12], [13], [14]. However, as they are all based on timing, variation in operation parameters such as temperature and load current can challenge their potential. Dynamic closed-loop gate drivers able to control delay times, dv/dt and di/dt separately have been presented for high power Si IGBTs [15]. However, for SiC MOSFETs, the driver will have challenges related to the bandwidth due to the larger time constants of Si IGBTs. A similar closed-loop gate driver created for SiC MOSFETs is presented in [16]. Yet, even though the gate driver is designed for SiC MOSFETs, the highest presented dv/dt target is 4V/ns, which is in the same range as for Si IGBTs.

The multistage driver, shown in Fig. 3c, is a driver concept aiming at minimizing delay times during a switching transient [9]. The driver is a two-stage driver with a conventional stage, similar to a conventional driver, and a boosting stage with boost voltages V_{pos2} for turn-on and V_{neg2} for turn-off. The operational principle is that for a turn-on or turn-off event, the MOSFET in the boosting stage of the driver $M_{b,***}$ will be turned on quickly to provide a low resistive path from the boost voltage to the gate. This allows for a large initial gate current that will charge or discharge the gate faster thus reducing delay times as seen in Figs. 4a and 4b for turn-off and turn-on respectively. For turn-off, diode D_2 will become reverse biased when the gate voltage equals V_{neg2} thus turning off the boosting stage. The rest of the switching stage is then controlled by the conventional part. By choosing V_{neg2} equal to the Miller plateau, the best possible reduction in turn-off delay time can be achieved without changing dv/dt. For turn-on transients, the diode, D_1, will become reverse biased when the gate voltage equals V_{pos2}. Hence, by choosing V_{pos2} so that D_1 blocks when the gate is at the threshold voltage, the best possible reduction in turn-on delay time is achieved without affecting di/dt.

Due to the diodes D_1 and D_2, the multistage driver can be considered to be voltage controlled. As long as the boost voltages are properly chosen, this is considered to be more robust than controlling the driver by timing due to manufacturing tolerances of passive components.

The operation principles of the multistage driver and the RC driver are quite similar. However, the boost capacitor in the RC driver is fixed and must be tuned for the worst-case operating point. While for the multistage driver, V_{pos2} and V_{neg2} can be chosen to be optimal at each operation point, thus, reducing the effect of load current and junction temperature dependent delay times. Yet, choosing optimal boost voltages based on the operation point requires measurements and functionality that allows the boost voltages to be changed dynamically. If such functionality is not implemented, V_{pos2} and V_{neg2} must be fixed and the tuning is similarly done for the worst-case operating point.

III. Experimental Validation of Driver Topologies

The three different gate driver topologies shown in Fig. 3 are tested experimentally and compared in terms of delay time for changing operational parameters.

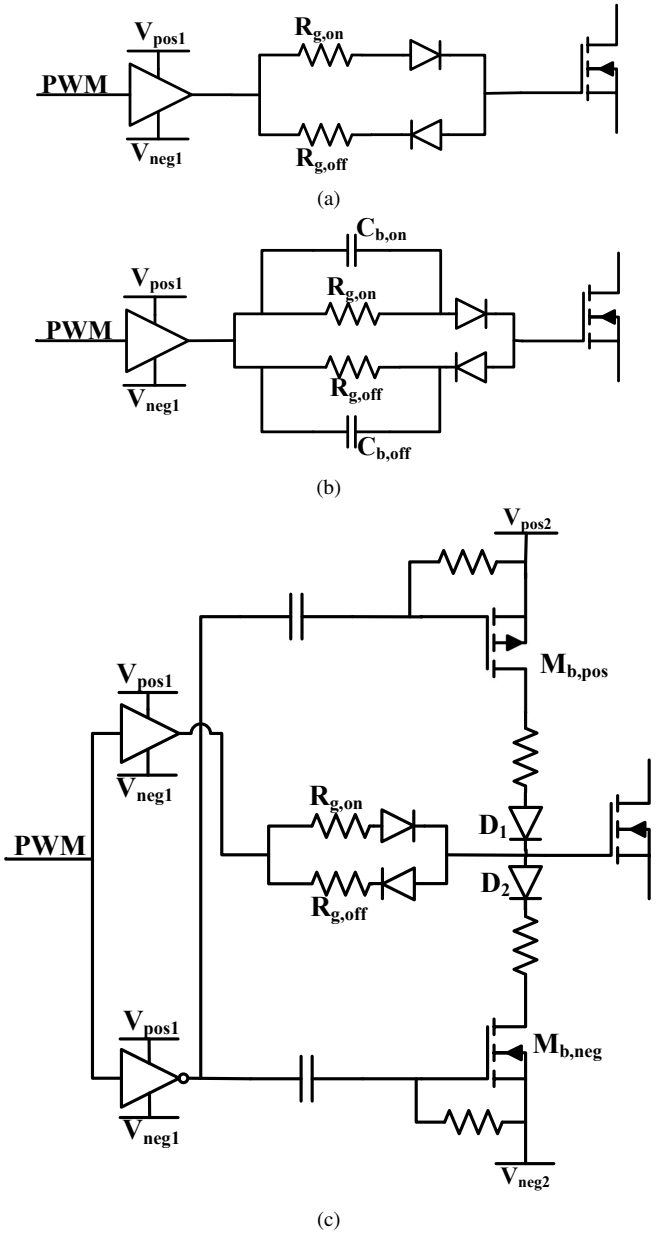


Fig. 3: Schematic diagrams of driver topologies. a) Conventional driver, b) RC driver and c) multistage driver.

A PCB with the possibility to test all three driver topologies was created and tested in the setup shown in Fig. 4c. In the tests, the gate resistors have been held constant while boost capacitors have been added for tests of the RC driver and the boosting stage is added for tests of the multistage driver. The waveforms in Fig. 4 verifies the driver concept for the multistage driver.

The reported results are obtained by double pulse testing of SiC MOSFET C3M007512K from Wolfspeed [17] in a halfbridge configuration with an inductive load. Waveforms are recorded using a Tektronix DPO 5104B 1 GHz oscillo-

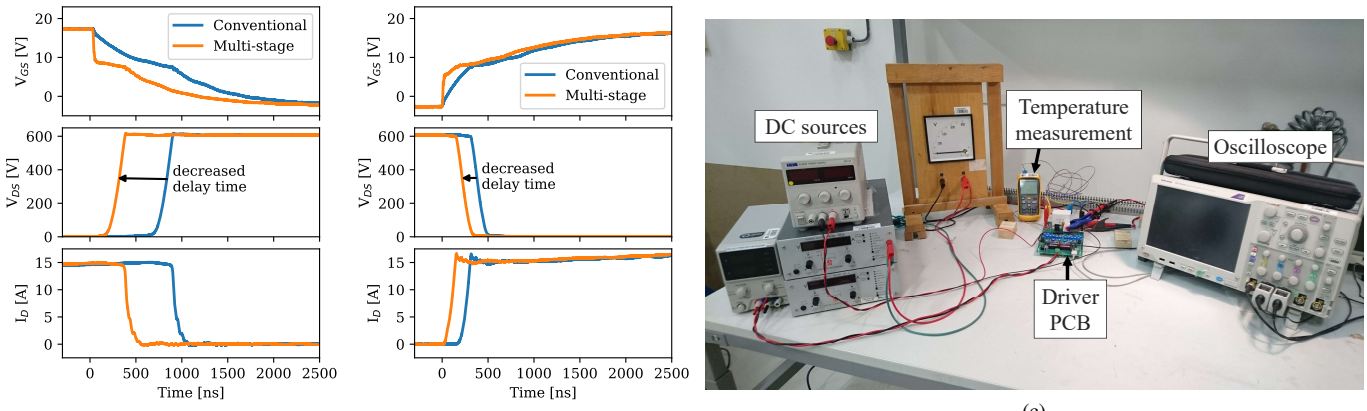


Fig. 4: Experimental waveforms verifying the driver concept. Delay times are reduced while di/dt and dv/dt are unchanged. a) Turn-off, b) Turn-on and c) Test setup.

TABLE I: Test parameters.

Driver	dv/dt	$R_{g,on/off}$	$C_{b,on/off}$	$V_{pos2/neg2}$
Conventional	10 V/ns	103/150 Ω		
RC driver	10 V/ns	103/150 Ω	470/1500 pF	
Multistage	10 V/ns	103/150 Ω		4.9/7.1 V

scope, Tektronix THDP0200 200 MHz voltage probes and a Rogowski PEM CWT06 30 MHz current probe. Time delays of the probes have been compensated according to their datasheet values. Junction temperature control is done by controlling the temperature of the drain metal on the back of the MOSFET die. The temperature is measured with a T-type thermocouple.

The turn-on delay times only depend on the threshold voltage of the SiC MOSFET, which in turn is junction temperature dependent. Hence, the results reported for turn-on is presented by the junction temperature dependency at a constant load current of 15 A. Turn-off delay times, however, depends on the Miller plateau which is affected by both the junction temperature and the load current. Hence, the turn-off results are presented both with the load current and junction temperature dependency.

To provide representative results for a motor drive application, a target dv/dt of 10 V/ns is chosen as this could be a typical value for applications with fast switching Si IGBTs. The circuit parameters are presented in Table I.

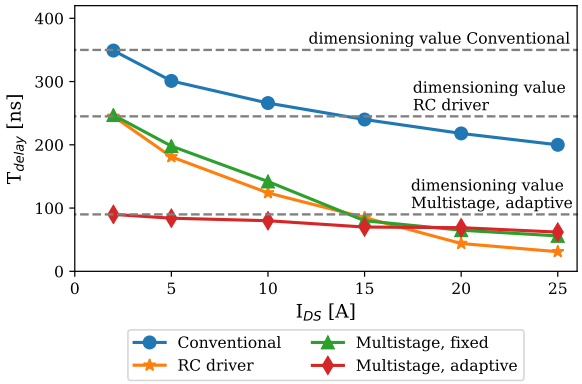
Two strategies for controlling the boost voltages V_{pos2} and V_{neg2} have been investigated. The boost voltages can either be fixed at a constant voltage level or optimized at each operation point to provide the largest reduction in delay time without affecting dv/dt or di/dt. The fixed solution is referred to as the fixed multistage driver while the solution with optimized boost voltages is referred to as the adaptive multistage driver. The boost voltages presented in Table I is used for the fixed multistage driver.

If the fixed solution is chosen, the voltage levels must be fixed according to worst case. For turn-off, as V_{neg2} ideally should be as low as possible to give a high initial gate current, worst case will be for low junction temperatures and high load currents due to the high location of the Miller plateau at that operation point. V_{neg2} is therefore fixed at 7.1 V in the reported results. For turn-on, the datasheet gives that threshold voltage is reduced by approximately 0.5 V from junction temperature 25 °C to 125 °C [17]. Hence, as V_{pos2} ideally should be as high as possible, worst case is for high temperatures. V_{pos2} is therefore fixed at 4.9 V in the reported results for the fixed multistage driver. Choosing the size for the boost capacitors in the RC driver must be done for the same operation points and dimensioned so that dv/dt and di/dt are not affected.

Fig. 5a shows the minimum delay times achieved for turn-off with different gate drivers at a junction temperature of 25 °C. The delay times for all drivers are reduced with increasing load current as the Miller plateau is located at higher gate voltage levels. The possible reduction in delay time when going from the conventional driver to the fixed multistage is approximately 100 ns for low currents and 150 ns for high currents. If the RC driver is used, the improvement is similar for low currents. For high currents however, the RC driver gives shorter delay times than the multistage driver. However, due to the available discrete values, the capacitor used to obtain the results is chosen to be a bit too large and dv/dt is slightly affected for high currents. If the capacitor is chosen smaller so that dv/dt was unchanged, the improvement in delay time would be similar to the fixed multistage driver.

The largest improvement in delay time for turn-off is found when using the adaptive multistage driver as seen in Fig. 5a. The improvement is found to be 259 ns or 74 % for low load currents at 25 °C junction temperature. When setting the dead time in a bridge leg, the worst delay time will be the design parameter. Hence, by changing from a conventional driver to a multistage driver with adaptive boost voltage, the dead time can be reduced by 259 ns. The delay times for all drivers at turn-off and 25 °C are presented in Table II.

Turn-on delay times are shown in Fig. 5b. The improvement in delay time when going from the conventional driver to the



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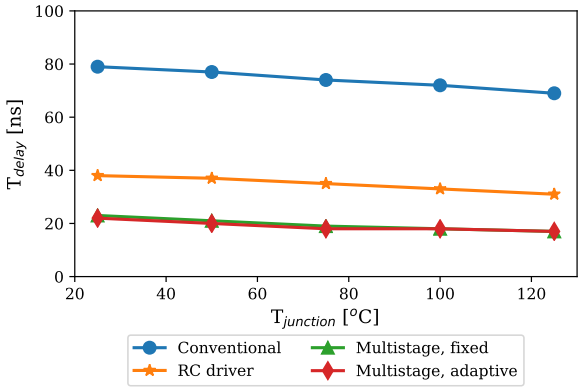

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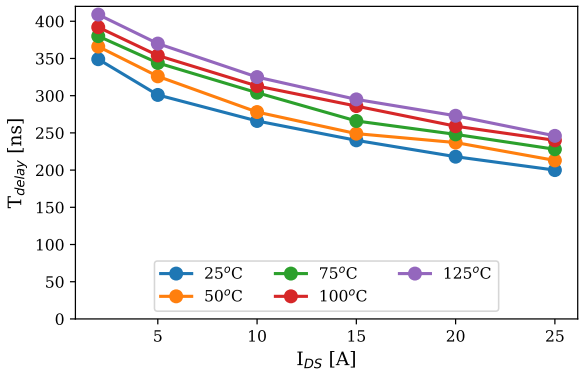
Fig. 5: Experimental results for delay times using different drivers. a) Turn-off, b) Turn-on.



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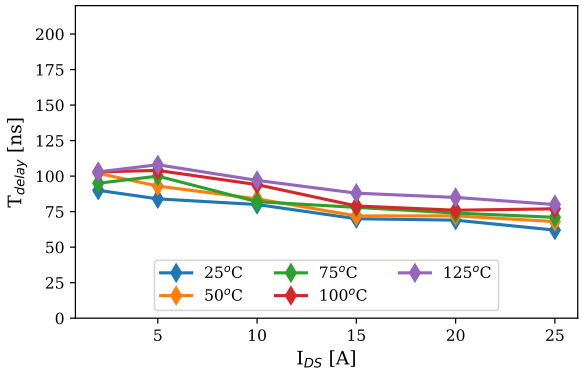

(b)

Fig. 6: Experimental results for delay times at different junction temperatures with a) conventional gate driver and b) adaptive multistage driver.

TABLE II: Turn-off delay time improvements at 25 °C.

Driver	$T_{d,off}$	$\Delta T_{d,off}$	Improvement
Conventional	349 ns		
RC driver	245 ns	104 ns	30 %
Multistage fixed	247 ns	102 ns	29 %
Multistage adaptive	90 ns	259 ns	74 %

fixed multistage driver is 56 ns or 71 % for 25 °C junction temperature. If the adaptive multistage driver is used, the improvement is 57 ns or 72 % for the same junction temperature. A similar percent-wise improvement is found for the rest of the tested junction temperatures as well, both for the fixed and adaptive multistage drivers. Due to the relatively low difference in threshold voltage at 25 °C and 125 °C, the performance from the fixed and adaptive multistage driver is very similar.

TABLE III: Turn-on delay time improvements.

Driver	$T_{d,on}$	$\Delta T_{d,on}$	Improvement
Conventional	79 ns		
RC driver	38 ns	41 ns	52 %
Multistage fixed	23 ns	56 ns	71 %
Multistage adaptive	22 ns	57 ns	72 %

For the RC driver, the improvement in delay time at 25 °C was 41 ns or 52 %. However, due to the available discrete capacitor values, the result is not ideal. An improvement in delay time more equal to the one obtained with the multistage drivers can be expected if the best choice for the boost capacitor is made. Hence, the added complexity from introducing the multistage driver can be reduced for turn-on by only consider the RC driver instead. Turn-on delay time improvements for the worst operation point, i.e at the lowest tested junction temperature is presented in Table III.

As the Miller plateau is lowered for increasing junction temperature for the same load current, the turn-off delay times increases with increasing temperature. For the conventional gate driver, the delay times are shown in Fig. 6a. At 2 A the delay time is increased by 60 ns when the junction temperature increases from 25 °C to 125 °C. This increases the requirements for dead time if the application should have a safe operation at 125 °C.

Turn-off delay times when using the multistage driver with an adaptive boost voltage is shown in Fig. 6b. Similar as for the conventional driver, the delay times increases with temperature. The highest measured delay time is 108 ns at 125 °C junction temperature. The delay times at 125 °C is presented in Table IV.

TABLE IV: Turn-off delay time improvements at 125 °C.

Driver	$T_{d,off}$	$\Delta T_{d,off}$	Improvement
Conventional	409 ns		
Multistage adaptive	108 ns	301 ns	74 %

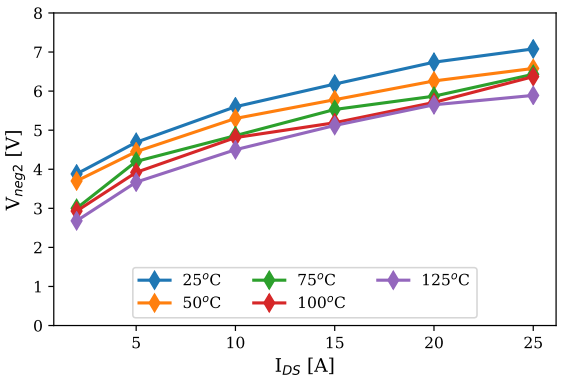

Fig. 7: Turn-off boost voltages at different junction temperatures and load currents for adaptive multistage driver.

To provide the largest possible reduction in delay time, the boost voltage in the multistage driver must be chosen optimally. When the Miller plateau is lowered due to increasing temperature or lower load current, a lower V_{neg2} without affecting dv/dt during turn-off is allowed hence increasing the effect of the boosting stage. Fig. 7 shows the optimal choice for boost voltages used for turn-off at the different operation points. If V_{neg2} is chosen to be fixed, thus using the fixed multistage driver, it must be chosen according to the highest operation temperature and load current. However, the results show that implementing the adaptive multistage driver by far gives the largest reduced delay times during turn-off. Therefore, the adaptive multistage driver is used as benchmark in the following parts of this paper.

IV. Effect of Dead Time on Different PWM Modulation Techniques

In PWM, the amplitude and frequency of the fundamental output voltage are controlled by comparing a control signal, V_c, to a triangular carrier, V_{tri}. Each inverter phase leg is controlled individually. The control signal V_c shapes the phase to neutral output voltage. For an AC output voltage, the control signal must have a fundamental part equal to the desired output voltage and with the desired frequency.

The ratio between the amplitude of the fundamental part of the control signal $\hat{V}_c$ and the triangular carrier wave $\hat{V}_{tri}$, is termed the modulation index M_a [8]:

$$M_a = \frac{\hat{V}_c}{\hat{V}_{tri}} \tag{2}$$

In addition to the fundamental part, triplen harmonics can be added to the control signal in a three-phase inverter as they are neutralised in the line voltage [18]. Furthermore, when the VSI drives a load with an isolated neutral point such as a motor, an arbitrary zero-sequence signal can be injected to the control signal in all phases [19], [20].

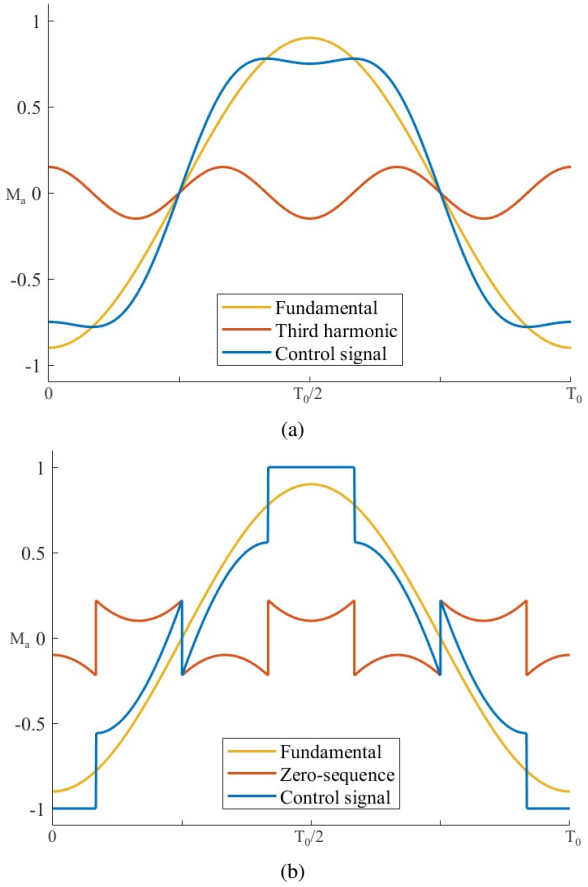

Fig. 8: PWM modulation techniques. a) THIPWM, b) DPWM, SPWM equals the fundamental signal.

A simple solution is to use a control signal consisting only of a sinusoidal wave, called SPWM. The control signal is shaped as $M_a sin(2\pi f_o t)$ resulting in the desired frequency, f_0 and amplitude, M_a. The SPWM technique is linear up to M_a equal to 1, after that overmodulation occurs [8].

By injecting a third harmonic signal to the control signal (THIPWM) as shown in Fig. 8a, the linear region for the line voltage can be increased. By choosing the amplitude to be 1/6 of the amplitude of the fundamental part, the linear region can be increased until $M_a = 1.15$. Thus, a 15 % higher output line voltage can be achieved without overmodulation [18].

Injecting a discontinuous zero-sequence signal to the control signal (DPWM) is suggested to improve the VSI performance in the overmodulation region in terms of voltage linearity and current harmonics [19], [21]. The control signal is shown in Fig. 8b for M_a equal to 0.9.

The control signal equals 1 in absolute amplitude for 1/3 of the period when using DPWM. This reduces the number of voltage pulses, and hence voltage commutations, for the same carrier frequency thus reducing switching losses. The carrier frequency can therefore be increased by a factor of 1.5 to have

TABLE V: Simulation parameters.

Driver	dv/dt	Dead time	Minimum pulse width
Conventional	10 V/ns	810 ns	2.43 µs
Multistage	10 V/ns	470 ns	1.41 µs

the same average switching frequency and switching losses as for the continuous PWM methods [19].

The impact of the multistage driver compared to a conventional driver have been investigated for a motor drive through simulations. The simulations have been done by building a MATLAB script. The simulation case is a motor drive application with a motor model and a VSI, similar to the setup shown in Fig. 1. The motor is assumed to be a round rotor 15 kW PM synchronous machine, supplied by a 600 V dc-link. The three different PWM modulation techniques, SPWM, THIPWM and DPWM, have been investigated with the conventional gate driver and the adaptive multistage driver.

The required dead time for the two drivers have been calculated according to Eq. 1 with the delay times obtained from the experimental work. The safety margin have been set to 200 ns and maximum dv/dt to 10 V/ns at the converter output. The MPW is set to be three times the dead time. All pulses shorter than the MPW are blanked out. Simulation parameters are presented in Table V.

Simulations are run with a carrier frequency of 15 kHz for SPWM and THIPWM. For DPWM, a carrier frequency which is 1.5 times higher, i.e. 22.5 kHz is used as previously described. The modulation index, M_a, is varied in the range from 0.8 to 1.5 to cover both the linear region and the overmodulation region [8]. For all modulation indices, the load current magnitude and the power factor have been held constant at 21.2 A rms (30 A peak) and 0.9 respectively.

To quantify the quality of the line current, total harmonic distortion (THD) is commonly used. If I_1 is the fundamental component and I_h is the h^{th} harmonic for $h \neq 1$, then THD is calculated as:

$$THD = \frac{\sqrt{\Sigma_{h=2}^{\infty} I_h^2}}{I_1} \tag{3}$$

Simulation results in terms of output line voltage and line current THD are shown in Figs. 9 and 10 respectively. When the conventional gate driver is used, a non-linear bubble shaped output voltage is observed in the last part of the theoretical linear region due to the minimum pulse width. The bubble starts at modulation index 0.92 for SPWM, 1.06 for THIPWM and 1.09 for DPWM. For control signals with an amplitude higher than these values, the voltage pulses are blanked out giving a higher fundamental component and voltage distortion. The distortion is visible in the current THD as well by a large peak for the same M_a as the line voltage becomes non-linear.

As shorter voltage pulses are accepted when using the multistage driver, the control signal is allowed to cross the triangular carrier wave at higher values before the pulses are blanked out. This increases the linear region for the output voltage and reduces the size of the observed bubble as

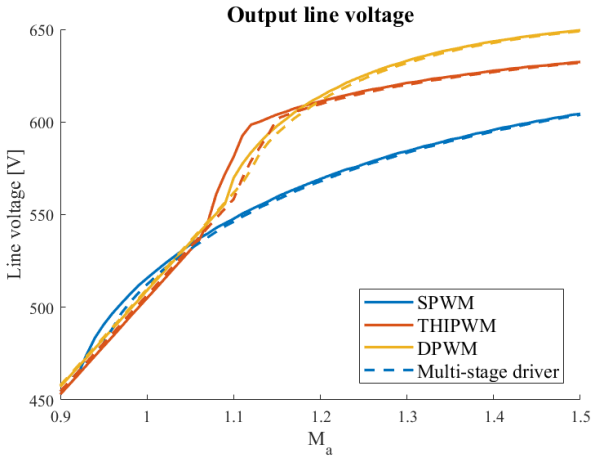

Fig. 9: Output peak line voltage for different PWM modulation techniques. Solid lines are from conventional gate driver while dotted lines are with the multistage driver.

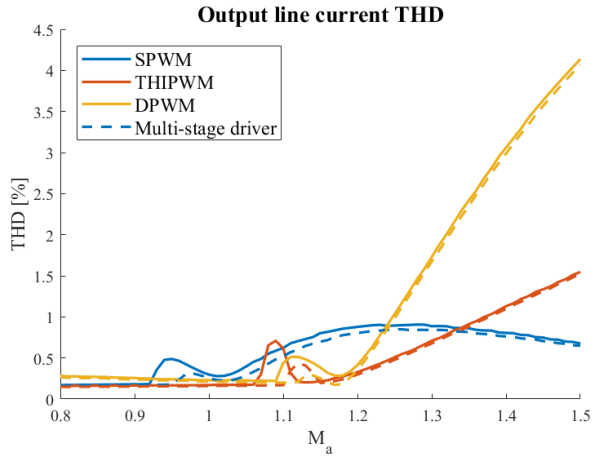

Fig. 10: Line current THD for different PWM modulation techniques. Solid lines are from conventional gate driver while dotted lines are with the multistage driver.

observed in Fig. 9. The linear regions are increased to 0.95 for SPWM, 1.10 for THIPWM and 1.11 for DPWM as presented in Table VI. The same trend is seen for the line current THD as the peak that is found when the voltage becomes non-linear is shifted towards higher modulation indices. At the same time, this peak is reduced.

Within the linear region, the peak output voltage when using the conventional gate driver and the multistage driver are similar. However, due to the reduced delay times for the multistage driver, the current freewheeling is reduced thus providing voltage shapes that are more equal to the ideal. With more ideal voltage pulses, the current harmonics are reduced and THD improved as presented in Table VI. When using DPWM, the improvement in current harmonics is found to be 7.7 % which is the largest improvement. However, DPWM is still the PWM method that creates most current harmonics in the linear region. For SPWM and THIPWM, which perform

TABLE VI: Maximum M_a and current THD for linear regions for different PWM methods.

	SPWM		THIPWM		DPWM	
Driver	$M_{a,max}$	THD	$M_{a,max}$	THD	$M_{a,max}$	THD
Conventional	0.92	0.18 %	1.06	0.17 %	1.09	0.25 %
Multistage	0.95	0.17 %	1.1	0.16 %	1.11	0.23 %
Improvement	3.3 %	5.1 %	3.8 %	6.6 %	1.8 %	7.7 %

more equal in the linear region, the reduction in THD were found to be 5.1 % and 6.6 % respectively.

V. Conclusion

An advanced multistage gate driver designed for delay time minimization was presented and compared experimentally to a conventional gate driver and a RC driver. Possible reduction in delay times and dead time requirements for the multistage driver and the RC driver were reported compared to the conventional gate driver. The experimental results showed a possible reduction in delay time of 71 % for turn-on and 74 % for turn-off while not affecting dv/dt or di/dt by changing from a conventional driver to the multistage driver with adaptive boost voltages. The reduction in required dead time was 42 %. Transferring the dead time reduction to a VSI in a motor drive application, the output voltage linearity region was increased by up to 3.8 % and the current THD reduced by up to 7.7 % in the linear region when using the multistage driver compared to the conventional counterpart. Hence, converter voltage output quality can be improved by implementing the presented driver topology.

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