Virtual Impedance Design for Power Quality and Harmonic Sharing Improvement in Microgrids

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Abstract—One of the main challenges of decentrally operated islanded microgrids has been proper harmonic sharing for parallel connected inverters. This is largely affected by differences in the feeder impedances of the inverters. Virtual impedances are able to improve the harmonic current sharing, at the cost of deteriorating the power quality at the outputs of the inverters. This paper proposes a method for minimally setting the virtual impedances based on an optimization algorithm and estimation of the feeder impedances. The scheme ensures proper sharing between the units, while the power quality at the inverter terminals are minimally affected. The scheme is verified by numerically simulating a test microgrid.

Index Terms—Harmonic Sharing, Power Quality, Virtual Impedance, Microgrid.

I. INTRODUCTION

Power quality in islanded microgrids is an important concern due to the proliferation of nonlinear loads in the distribution grid [1]. Without proper action, this can lead to severely distorted voltages, which might cause malfunction of other loads connected adjacently [2]. If several inverters are operating in parallel, an additional challenge has been proper harmonic sharing. In particular, if the feeder impedances of the inverters are unequal, poor sharing of the harmonic burden may result. Hence, the control of the inverters needs to consider the power quality and harmonic sharing.

From the perspective of distributed generators (DGs) there are three main approaches for considering harmonic problems [3]. The simplest approach is denoted harmonic rejection, in which the DGs controls their output voltage to be perfectly sinusoidal. This approach provides clean voltage waveforms at the terminals of the DGs, but can give poor voltage quality at the loads, in addition to unequal harmonic current sharing if the feeder impedances differ. The second approach is local load compensation, which works by compensating the non-linear currents generated by local loads, similar to an active power filter (APF). An advantage of this scheme is that the harmonics are dealt with locally, thereby reducing the harmonic losses in the lines. However, harmonic distribution and voltage quality are not controlled. For microgrids with mainly unidentifiable loads, the local compensation might be inefficient. The third category aims at improving the voltage quality further down from the inverter. This is done by emulating the DG as an impedance at harmonic frequencies. This results in a local voltage distortion. This third category will be considered in the following.

A popular hierarchical control scheme utilizes a measurement of the voltage at a sensitive load bus (SLB) which is used to modify the DG voltage reference [4]. This approach effectively reduces the total harmonic distortion (THD) at the SLB by increasing the THD at the DGs. In [5], several SLBs are defined, and a tertiary controller optimizes the system in order to ensure that all SLBs are within their voltage unbalance limits. A drawback of the hierarchical scheme is the need for communication, thereby reducing the reliability.

A widely used decentralized control scheme is based on utilizing virtual impedances [6]. By properly setting the virtual impedances, it is possible to adjust the trade-off between voltage quality and current sharing [7]. The virtual impedance should be large enough to compensate unequal feeders of different DG units in order to achieve proper sharing. Yet, the virtual impedance should not be excessive, in order to limit the voltage and power quality reduction at the outputs of the inverters. Thus, the virtual impedances need to be set based on an inherent trade-off [8].

This paper presents a method for minimizing the voltage distortion, while simultaneously ensuring good sharing between the DGs. This is done by formulating an optimization problem that minimizes the virtual impedances of the converters, where the physical feeder impedances are included as constraints. To this end, the physical feeder impedances are first estimated by each DG. Then, a centralized controller performs the optimization algorithm, and distributes the optimal virtual impedance for each DG. This ensures that the DGs share the nonlinear load, while simultaneously keeping the voltage THD at the nodes of the microgrid at a minimum.

The rest of the paper is organized as follows: Section II describes how harmonic power sharing can be performed using virtual impedances, and how this is done in the synchronous reference frame. Section III describes the proposed control method. This includes how the feeder impedance estimation is performed and the details regarding the optimization algorithm. Then, Section IV shows some simulation results, before Section V concludes the paper.

II. HARMONIC POWER SHARING USING VIRTUAL IMPEDANCES

This section reviews how harmonic power sharing can be improved by using virtual impedances for a decentrally controlled microgrid.

Fig. 1 shows n DGs operating in parallel to supply a common linear and nonlinear load. In the general case, the feeder impedances differ, which causes unequal power sharing between the inverters. An outline of the droop control with virtual impedance is shown for DG n. The scheme uses a cascaded controller with an inner loop current controller and an outer loop voltage controller [7].

The fundamental voltage amplitude and angle references are provided by the Pf and QV droop control [9]. An outer virtual impedance is used to modify the fundamental and harmonic voltage reference [10]. In particular, the inverter feeder current i_o is multiplied by the virtual impedance Z_{vi}.

In order to understand how to select the virtual impedance, consider the dq impedance of a physical resistive-inductive line:

$$\mathbf{Z_{dq}} = \begin{bmatrix} sL + R & -\omega L \\ \omega L & sL + R \end{bmatrix} \tag{1}$$

where s is the Laplace variable, R is the resistance, L is the inductance and ω is the angular frequency of the rotating dq frame. Thus, if a dq frame other than the one corresponding to the fundamental component is used, ω must be modified accordingly. In particular, for negative sequence components a negative sign must be included. For example, for the negative sequence 5th harmonic, $\omega = -5\omega_1$, where ω_1 denotes the fundamental angular frequency.

Typically, the harmonic virtual impedance is set to replicate an impedance in steady state. The virtual impedance of a resistive-inductive element is then given by:

$$\mathbf{Z_{dq,v}} = \begin{bmatrix} R_v & -\omega L_v \\ \omega L_v & R_v \end{bmatrix} \tag{2}$$

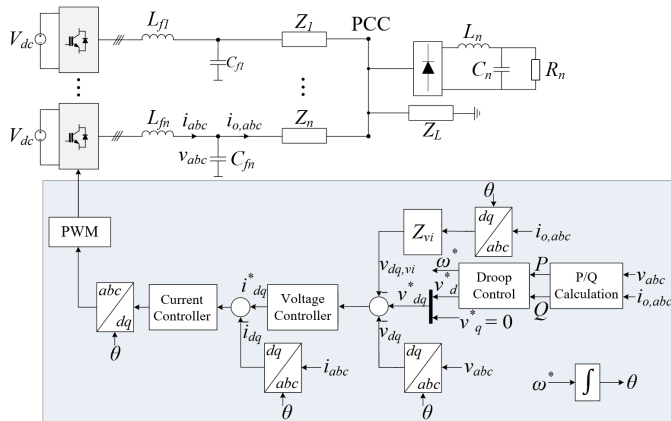where R_v and L_v are the virtual resistance and inductance, respectively.

In [6], a design methodology for setting the virtual impedance is presented, in order to achieve PQ decoupling for effective droop control, as well as achieving sufficient stability margins and transient performance. Here, negative resistances are employed for improving the performance. However, in this work, the same virtual impedance is applied to all components of the load current.

In [8], the virtual impedance is set to be inductive for the fundamental component and resistive for the harmonic components. Another approach is proposed in [7], where the virtual impedance is set differently for the fundamental and harmonic frequencies. This is done by decomposing the feeder current into the fundamental and higher-order harmonics, and then applying a virtual impedance to each of the components. In particular, negative virtual harmonic inductances were used to reduce the equivalent feeder impedance. An important note was that the negative virtual impedance should not be larger than the physical impedance in order to preserve stability. Thus, since the actual impedance of the line was unknown, a relatively large margin needed to be set.

The effect of setting the virtual impedance differently at the fundamental and harmonic frequencies can be visualized by the phasor diagrams in Fig. 2 [11], which display a simplified case with two DGs operating in parallel. At fundamental
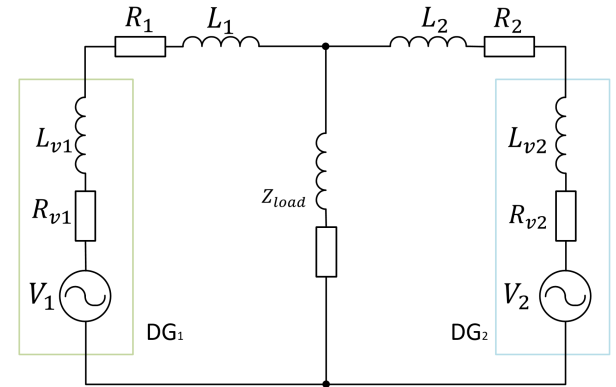
(a) Equivalent diagram at fundamental frequency.
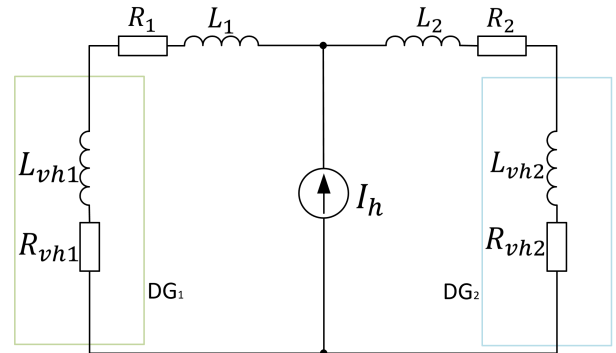
(b) Equivalent diagram at harmonic frequency h.

Fig. 2. Equivalent phasor diagrams for a decentrally controlled microgrid with fundamental and harmonic virtual impedances. a) fundamental positive sequence and b) harmonic component h.

Fig. 1. Control structure of droop-controlled inverter with virtual impedance.

frequency, the system is modelled by a passive load, Z_{load}, connected to the DGs via feeder impedances modelled as resistive-inductive lines. The DGs appear as voltage sources in series with their virtual impedances. At the harmonics where the virtual impedances are implemented, the DGs are modelled by their virtual harmonic impedance, while the load is modelled as the current source I_h.

From the diagrams in Fig. 2 it is clear that the condition for equal sharing between the two units corresponds to having the same equivalent impedance between the voltage sources and the load. For a given frequency ω, this can be expressed as

$$R_{v1}+R_1+j\omega(L_{v1}+L_1) = R_{v2}+R_2+j\omega(L_{v2}+L_2) \quad (3)$$

where R and L indicate the physical resistances and inductances, while R_v and L_v are the virtual resistances and inductances. The subscripts 1 and 2 indicate impedances belonging to DG 1 and DG 2, respectively.

Consider again the phasor diagram in Fig. 2(b). Assuming that the harmonic current source I_h is constant, it is evident that the voltage THD at the load and inverter terminals for a given harmonic is depending on the equivalent impedances seen by the load. Larger equivalent impedances lead to larger harmonic voltage drops, which further lead to more distorted voltages in the microgrid. Thus, in order to minimize the harmonic voltage drops, the equivalent impedance at harmonic frequencies should be as small as possible. This amounts to setting the virtual impedance such that the equivalent impedances are minimized. A proposed solution for doing this is given in the next section.

III. PROPOSED CONTROL METHOD

This section presents the proposed control method. First, the impedance estimation is outlined, before the optimization algorithm for finding the virtual impedances is presented. Finally, the virtual impedance implementation is presented.

A. Feeder Impedance Estimation

Several techniques for impedance estimation exist [12]. In this work, the maximum length binary sequence (MLBS) has been chosen as the signal is periodic and deterministic, such that multiple injection periods can be used to reduce the amplitude of the disturbance [12]. Moreover, the MLBS signal can be added easily in the existing control loops of the DGs.

The impedance estimation technique needs a steady-state operating point around which it can perform a linearization [13]. This can be achieved in the synchronous reference frame (SRF), provided that the system is balanced. Once a steady state operating point is achieved, the MLBS is used to add a disturbance at the current reference. This enables estimating the impedance up until the bandwidth of the current controller. If high-frequency components should be estimated, the MLBS should also be injected at the duty cycle [14]. The resulting voltages and currents are then transformed to the dq frame where a Fast Fourier Transform (FFT) is performed on the variables. A nonparametric impedance matrix can then be

calculated at the angular frequencies corresponding to the FFT bins ω' as [15]:

$$\begin{bmatrix} Z_{dd}(\omega') & Z_{dq}(\omega') \\ Z_{qd}(\omega') & Z_{qq}(\omega') \end{bmatrix} = \begin{bmatrix} V_{d1}(\omega') & V_{d2}(\omega') \\ V_{q1}(\omega') & V_{q2}(\omega') \end{bmatrix}\begin{bmatrix} I_{d1}(\omega') & I_{d2}(\omega') \\ I_{q1}(\omega') & I_{q2}(\omega') \end{bmatrix}^{-1} \quad (4)$$

where Z_{dd}, Z_{dq}, Z_{qd} and Z_{qq} are the elements of the dq impedance matrix, while V_{dq} and I_{dq} denote the voltages and currents for the d and q axes. The subscripts 1 and 2 denote the two injections that are needed in order to solve the system of equations. Typically, the injections are done into the d and q axes, respectively, in order to ensure linearly independent injections [16].

In this work, only the feeder impedances Z_i in Fig. 1 will be estimated. Hence, the voltage at the PCC must be measured for the estimation. Assuming that the PCC voltage V_{PCC} is measured, the feeder impedance can be estimated using (4) if the voltage measurements are swapped with $V - V_{PCC}$, where V now denotes the inverter output voltage. The resulting equation is thus (the dependency on ω' is left out for a more compact expression):

$$\begin{bmatrix} Z_{dd} & Z_{dq} \\ Z_{qd} & Z_{qq} \end{bmatrix} = \begin{bmatrix} V_{d1} - V_{d1,PCC} & V_{d2} - V_{d2,PCC} \\ V_{q1} - V_{q1,PCC} & V_{q2} - V_{q2,PCC} \end{bmatrix}\begin{bmatrix} I_{d1} & I_{d2} \\ I_{q1} & I_{q2} \end{bmatrix}^{-1} \quad (5)$$

The physical inductance and resistance of the feeder are estimated based on (1). At low frequencies, the diagonal terms can be approximated as depending only on the resistance. The estimated feeder resistance $\hat{R}$ can then be calculated based on the average of the first k elements of the diagonal terms as:

$$\hat{R} = \frac{1}{2k}\sum_{j=1}^{k}(Z_{dd}(\omega'_j) + Z_{qq}(\omega'_j)) \quad (6)$$

while the estimated inductance is found in a similar way based on the off-diagonal terms as:

$$\hat{L} = \frac{1}{2k}\sum_{j=1}^{k}\frac{Z_{qd}(\omega'_j) - Z_{dq}(\omega'_j)}{\omega_1} \quad (7)$$

Once the feeder impedances are estimated locally at each DG, the estimated values are sent to a central controller, which calculates the minimal virtual impedances that fulfills the control objective. This is described in more detail in Section III-B.

A limitation of the scheme is the necessity of measuring the PCC voltage. However, as the cost of monitoring devices such as μPMUs is reducing, this could be feasible. Note that the measurement of the PCC voltage is only needed for the estimation, and not during normal operation. Hence, it does not represent an increased reliability risk, as the system will continue to work even if the measurement unit fails.

Another challenge of the scheme is that the voltage measurements should be properly synchronized. If the voltage measurements are performed at slightly different times, this will be translated into a phase difference, which will affect the phase of the impedance estimation. The current work assumes that the measurements are compensated for any delay. This issue is left for further work.

B. Optimal Virtual Impedance Setting

Based on the estimates of the feeder impedances, a central controller calculates the optimal virtual impedances. According to the discussion in Section II, the DG equivalent impedances seen from the load should be equal to ensure proper sharing, while the equivalent harmonic impedances should be minimized in order to limit the voltage THD. The following describes in detail how the virtual impedances should be set to achieve that for the fundamental and harmonic frequencies for the case where n DGs operate in parallel with unequal interconnecting feeder impedances.

1) Virtual Fundamental Impedance: For the fundamental frequency, in addition to complying with (3), it is also desired to have $X/R \geq 1$, i.e. that the perceived impedance is mainly inductive. This is to ensure sufficient decoupling for the standard Pf, QV droop control. For low-voltage networks, the ratio of the physical reactance to resistance is typically less than unity. Thus, the virtual inductance should be large enough to achieve the desired ratio.

Considering that the virtual fundamental resistance should be the same for the different DGs, yet as small as possible to achieve the wanted decoupling, the following optimization problem can be formulated:

$$
\begin{aligned}
\min R_{v,tot} &= \sum_{j=1}^{n} R_{v,j} \\
\text{s.t.} \quad R_{eq,j} &= \hat{R}_j + R_{v,j} \qquad \forall j \\
R_{v,j} &\geq 0 \qquad \qquad \forall j \\
R_{eq,j} &= \frac{1}{n} \sum_{k=1}^{n} R_{eq,k} \qquad \forall j
\end{aligned}
\tag{8}
$$

In (8), $R_{v,j}$ is the virtual resistance of DG j, $\hat{R}_j$ is the estimated physical feeder resistance for DG j, while $R_{eq,j}$ is the equivalent feeder resistance for DG j.

The first constraint in (8) defines the equivalent resistance as the sum of the estimated and the virtual resistance. The second constraint ensures that all virtual resistances are positive, in order to ensure negative feedback of the virtual impedance loops. The third constraint specifies that the equivalent resistance of each DG should be equal, thereby improving the sharing between the units. Finally, the objective function aims at minimizing the virtual resistances of each DG. This objective is chosen in order to minimize the necessary virtual inductance.

A similar linear programming problem can be established for the fundamental virtual inductance, as seen in (9). The only difference to (8) is the second constraint, which is formulated to ensure an equivalent X/R-ratio specified by the parameter γ.

$$
\begin{aligned}
\min L_{v,tot} &= \sum_{j=1}^{n} L_{v,j} \\
\text{s.t.} \quad L_{eq,j} &= \hat{L}_j + L_{v,j} \qquad \forall j \\
L_{eq,j} &\geq \gamma R_{eq,j} \qquad \forall j \\
L_{eq,j} &= \frac{1}{n} \sum_{k=1}^{n} L_{eq,k} \qquad \forall j
\end{aligned}
\tag{9}
$$

In (9), $L_{v,j}$ is the virtual inductance of DG j, $\hat{L}_j$ is the estimated physical feeder inductance for DG j, and $L_{eq,j}$ is the equivalent feeder inductance for DG j.

The accuracy of the settings is, of course, subject to the accuracy of the feeder estimation. Moreover, also the impedance created by the control loop affects the result output impedance, but it is neglected in this analysis.

2) Virtual Harmonic Impedance: Accurate harmonic sharing is achieved when the equivalent harmonic impedances of the DGs are equal, while the voltage THD is minimized when the equivalent harmonic impedances seen from the load are as small as possible. The following linear programming problem can then be formulated for finding the virtual harmonic inductances that satisfy the mentioned criteria:

$$
\begin{aligned}
\min L_{h,tot} &= \sum_{j=1}^{n} L_{vh,j} \\
\text{s.t.} \quad L_{eq,h,j} &= \hat{L}_j + L_{vh,j} \qquad \qquad \forall j \\
L_{eq,h,j} &\geq L_{min,h,j} \geq 0 \qquad \forall j \\
\frac{1-\epsilon_h}{n} \sum_{k=1}^{n} L_{eq,h,k} \leq L_{eq,h,j} &\leq \frac{1+\epsilon_h}{n} \sum_{k=1}^{n} L_{eq,h,k} \quad \forall j
\end{aligned}
\tag{10}
$$

In (10), $L_{vh,j}$ is the virtual harmonic inductance of DG j, while $L_{eq,h,j}$ is the equivalent harmonic feeder inductance for DG j. The parameter $L_{min,h,j}$ is a constant that the equivalent harmonic inductance needs to be larger than. The parameter ϵ_h specifies the degree of sharing between the DGs.

The objective function in (10) minimizes the sum of the virtual harmonic inductances of the DGs. The first constraint defines the equivalent inductance of DG j as the sum of the estimated and the virtual harmonic inductance, while the second constraint ensures that the equivalent inductance is larger than some minimum inductance. Moreover, $L_{min,h,j} \geq 0$ in order to preserve stability. The third constraint specifies the sharing between the DGs; if the parameter $\epsilon_h = 0$, all equivalent inductances are forced to be equal. If neglecting the errors in the estimates of the inductances, this causes perfect sharing of the harmonic load current. By setting $\epsilon_h > 0$, unequal sharing between the DG units is possible. Assuming that the feeder estimates differ, this effectively leads to reduced harmonic inductances for one or more of the DGs, which will further reduce the voltage THD. The trade-off between voltage THD and harmonic current sharing is thus evident.

A similar optimization problem can be formulated for the resistive part:

$$\min R_{h,abs,tot} = \sum_{j=1}^{n} |R_{vh,j}|$$

$$\text{s.t.} \quad R_{eq,h,j} = \hat{R}_j + R_{vh,j} \qquad \forall j \quad (11)$$

$$R_{eq,h,j} \geq R_{min,h,j} \geq 0 \qquad \forall j$$

$$\frac{1 - \epsilon_h}{n} \sum_{k=1}^{n} R_{eq,h,k} \leq R_{eq,h,j} \leq \frac{1 + \epsilon_h}{n} \sum_{k=1}^{n} R_{eq,h,k} \; \forall j$$

In (11), $R_{vh,j}$ is the virtual harmonic resistance of DG j, while $R_{eq,h,j}$ is the equivalent harmonic feeder resistance for DG j. The parameter $R_{min,h,j}$ is a constant that the equivalent harmonic resistance needs to be larger than.

The constraints in (11) are similar to the constraints in (10). On the other hand, the objective function here minimizes the sum of the absolute values of the resistances. This effectively tries to minimize the use of virtual harmonic resistances, which is done in order to limit the use of large negative virtual resistances to get a larger stability margin.

C. Virtual Impedance and Control in the dq Frame

The proposed virtual impedance implementation at each DG for the dq frame is seen in Fig. 3. The feeder current is decomposed into the fundamental and several other harmonics [7]. In particular, the 1st, 5th, 7th, 11th and 13th components of the feeder current are extracted in their own SRF. Then, a virtual impedance is applied to each component as shown in (2), where ω is varying for each dq frame. The virtual resistances and inductances for the fundamental and harmonic frequencies are set according to (8)-(11).

Assuming that the system is balanced, the negative sequence harmonics drawn by the system are given by $\omega_{hn} = (6k - 1)\omega_1$, $k \in \mathbb{N}$, while the positive sequence harmonics drawn by the system are given by $\omega_{hp} = (6k + 1)\omega_1$, $k \in \mathbb{N}$. When operating in the fundamental frequency SRF, all natural
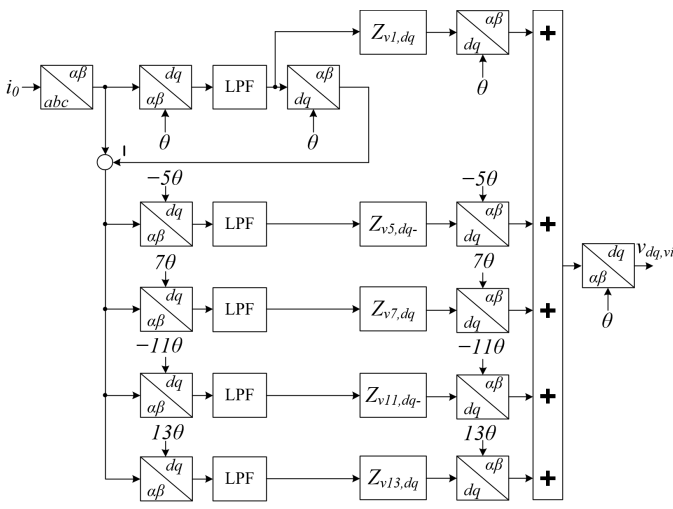
frequencies are shifted by the fundamental frequency. This effectively shifts both the positive and negative sequence harmonics such that they appear at the harmonic frequencies given by $\omega_{h,dq} = 6k\omega_1, k \in \mathbb{N}$.

In order to reduce the steady state error at these harmonic frequencies, resonant controllers are added at the frequencies of the virtual impedances in the dq domain. According to the discussion above, resonant controllers are therefore added to reduce the steady state error for the 6th and 12th harmonic [17]. The resulting voltage controller is then given by

$$C_v(s) = k_{pv} + \frac{k_{iv}}{s} + \sum_{h=6,12} \frac{2K_h \omega_c s}{s^2 + 2\omega_c s + (h\omega_1)^2} \quad (12)$$

where k_{pv} and k_{iv} are the proportional and integral gain of the PI controller, K_h determines the gain for the resonant controller corresponding to harmonic h, while ω_c defines the width where the resonant controller is effective.

IV. NUMERICAL SIMULATION RESULTS

This section shows simulation results of the feeder impedance estimation as well as the harmonic sharing resulting from setting the virtual impedances according to the optimization algorithm. The test microgrid in Fig. 1 is used with three DGs connected in parallel with a common load. The main parameters for the simulation are given in Table I.

A. Feeder Impedance Estimation

As explained in Section III-A, the MLBS is used to inject a disturbance at the current reference when the system is in steady state. The disturbance amplitude was set to 10 % of the steady state operating point of the inverter. The resulting inverter filter currents and filter capacitor voltages of DG 1 are shown in Fig. 4. The distorted waveforms are due to the nonlinear load at the PCC. At $t = 800\,\text{ms}$, the MLBS is added to the current reference for the d-channel. As seen, the disturbance is mainly affecting the current, while the disturbance of the voltage is attenuated.

Bode plots of the estimated feeder impedances are shown in Fig. 5, together with the analytical models given by (1). The estimated feeder impedances correspond quite well to the analytical model for the diagonal elements, as well as for lower frequencies. The off-diagonal elements do not correspond as

Fig. 3. Proposed virtual impedance control structure.

TABLE I
SIMULATION PARAMETERS

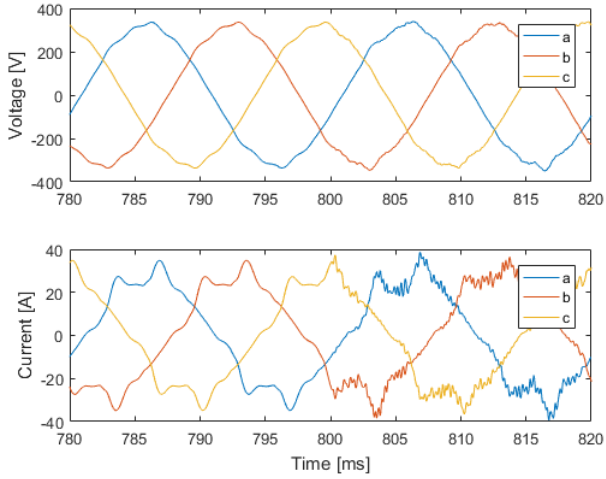| Parameter	Value	Parameter	Value
f	50 Hz	k_{pi}	1.03 p.u.
Line voltage	400 V	k_{ii}	3553 p u
V_{dc}	800 V	k_{pv}	0.603 p.u.
S	20 kVA	k_{iv}	227.4 p.u.
L_f	500 µH	K_6	1000 p.u.
C_f	50 µF	K_{12}	200 p.u.
Z_1	$0.540 + j0.330\ \Omega$	ω_c	1 rad/s
Z_2	$0.273 + j0.196\ \Omega$	γ	1
Z_3	$0.140 + j0.130\ \Omega$	ϵ_h	0
Z_L	$6 + j2\ \Omega$	R_n	48.6 Ω
L_n	84 µH	C_n	235 µF

Fig. 4. Response of voltage and current waveforms during MLBS disturbance.

TABLE II
ESTIMATED AND REAL FEEDER IMPEDANCES

Parameter	Estimated	Real
R_{L1}	0.572 Ω	0.540 Ω
L_{L1}	0.976 mH	1.049 mH
R_{L2}	0.252 Ω	0.273 Ω
L_{L2}	0.491 mH	0.624 mH
R_{L3}	0.125 Ω	0.140 Ω
L_{L3}	0.400 mH	0.412 mH

well, particularly for higher frequencies. However, as the aim here is to estimate the values of the resistive and inductive elements, the low-frequency estimated values are sufficient. The estimated resistance and inductance of the two feeders according to (6) and (7) are summarized in Table II.

B. Harmonic Sharing Using Estimated Impedances

In order to test the performance and accuracy of the proposed sharing method, the case without any virtual impedance is used as a base case. Hence, in this mode of operation, the DGs control their voltages to be purely sinusoidal. The resulting measured PCC voltages are shown in Fig. 6(a). The voltages are clearly distorted.

Now, the virtual impedances are set according to the proposed control, based on the feeder estimation and the optimization problems. The resulting voltages at the PCC are shown in Fig. 6(b). The waveforms are more sinusoidal than in the case without any virtual impedance. A comparison of the voltage harmonic levels at the PCC for the two cases is shown in Fig. 7 at the harmonics where the virtual impedances are implemented. This confirms the improved voltage quality of the PCC voltages with the proposed control.

The output currents for phase a of the three DGs for the case without virtual impedance is shown in Fig. 8(a). The currents are clearly distorted due to the nonlinear load at the PCC. It is also seen that the DGs are not supplying the same currents due to the different feeder impedances.
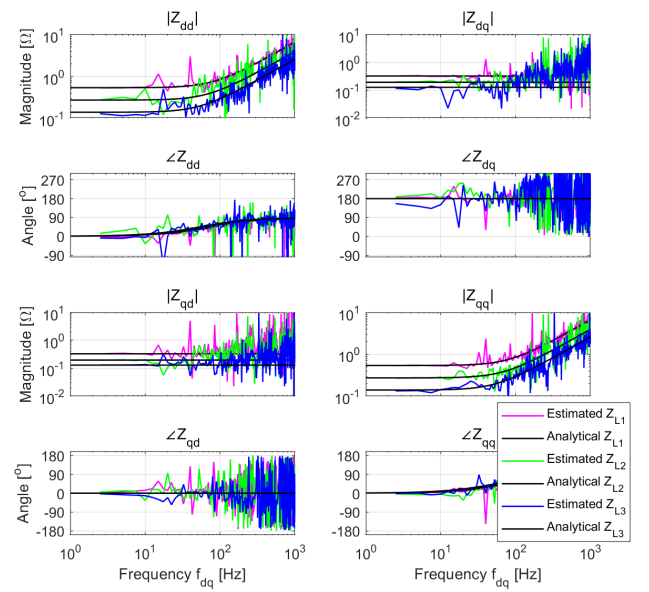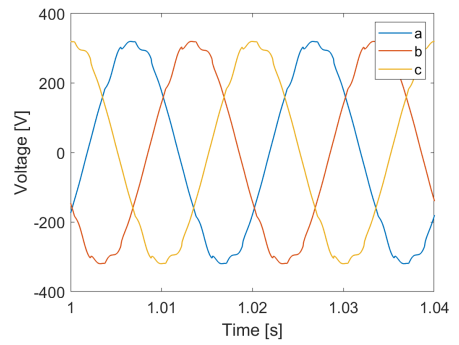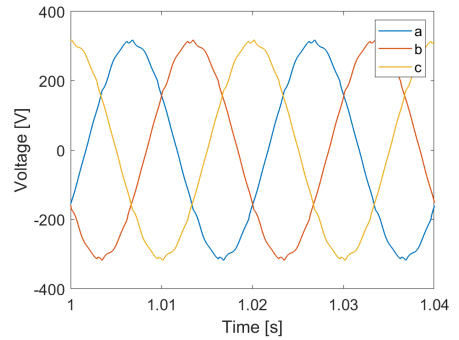

Fig. 5. Estimated and analytical feeder impedances.

(a) Without virtual impedance

(b) With proposed virtual impedance

Fig. 6. PCC voltages

Fig. 8(b) shows the output currents for phase a for the three DGs when the proposed virtual impedance control is applied. It can be seen that the currents are matching closely in this case, thus showing improved sharing.
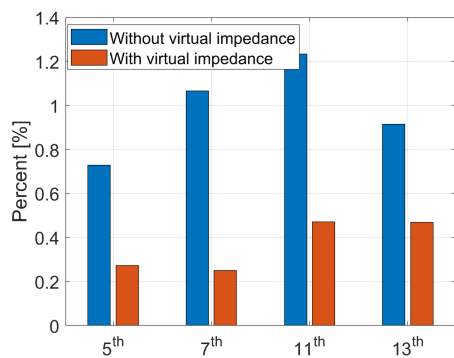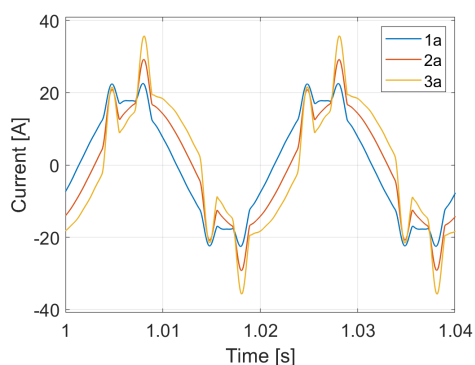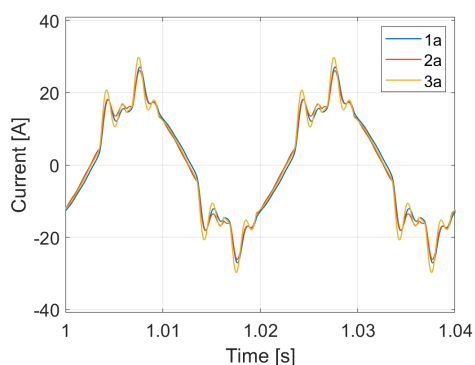
Fig. 7. Voltage harmonics at the PCC voltage with and without virtual impedance control as percentage of the fundamental voltage.

(a) Without virtual impedance

(b) With proposed virtual impedances

Fig. 8. Inverter phase a output currents.

V. CONCLUSION

Proper sharing of harmonic loads and limitation of the overall THD are important concerns for islanded microgrids with parallel connected DGs. This paper has presented a scheme for finding the minimal virtual impedances of the DGs that achieve the mentioned control objectives, without reducing the voltage quality at the inverters unnecessarily. The impedance estimation is done by the utilizing the MLBS sequence, which is used as an input to an optimization problem that further finds the optimal virtual impedances of each

DG. The effectiveness of the proposed concept is shown by numerical simulations.

REFERENCES

[1] J. C. Das, *Power System Harmonics and Passive Filter Designs*. John Wiley & Sons, 2015.
[2] EN 50160, *Voltage Characteristics of Electricity Supplied by Public Electricity Networks*, 2010.
[3] Y. W. Li and J. He, "Distribution system harmonic compensation methods: An overview of DG-interfacing inverters," *IEEE Industrial Electronics Magazine*, vol. 8, no. 4, pp. 18–31, 2014.
[4] M. Savaghebi, A. Jalilian, J. C. Vasquez, and J. M. Guerrero, "Secondary Control for Voltage Quality Enhancement in Microgrids," *IEEE Transactions on Smart Grid*, vol. 3, no. 4, p. 4799, 2012.
[5] L. Meng, F. Tang, M. Savaghebi, J. C. Vasquez, and J. M. Guerrero, "Tertiary control of voltage unbalance compensation for optimal power quality in islanded microgrids," *IEEE Transactions on Energy Conversion*, vol. 29, no. 4, pp. 802–815, 2014.
[6] J. He and Y. W. Li, "Analysis, Design, and Implementation of Virtual Impedance for Power Electronics Interfaced Distributed Generation," *IEEE Transactions on Industry Applications*, vol. 47, no. 6, pp. 2525–2538, 11 2011.
[7] X. Wang, F. Blaabjerg, and Z. Chen, "Autonomous Control of Inverter Interfaced Distributed Generation Units for Harmonic Current Filtering and Resonance Damping in an Islanded Microgrid," *IEEE Transactions on Industry Applications*, vol. 50, no. 1, pp. 452–461, 2014.
[8] J. M. Guerrero, J. Matas, L. G. De Vicuña, M. Castilla, and J. Miret, "Wireless-control strategy for parallel operation of distributed-generation inverters," *IEEE Transactions on Industrial Electronics*, vol. 53, no. 5, pp. 1461–1470, 2006.
[9] M. C. Chandorkar, D. M. Divan, and R. Adapa, "Control of parallel connected inverters in standalone ac supply systems," *IEEE Transactions on Industry Applications*, vol. 29, no. 1, pp. 136–143, 1993.
[10] X. Wang, Y. W. Li, F. Blaabjerg, and P. C. Loh, "Virtual-Impedance-Based Control for Voltage-Source and Current-Source Converters," *IEEE Transactions on Power Electronics*, vol. 30, no. 12, pp. 7019–7037, 2015.
[11] J. He, Y. W. Li, and F. Blaabjerg, "An Enhanced Islanding Microgrid Reactive Power, Imbalance Power, and Harmonic Power Sharing Scheme," *IEEE Transactions on Power Electronics*, vol. 30, no. 6, pp. 3389–3401, 2015.
[12] T. Roinila, M. Vilkko, and J. Sun, "Broadband methods for online grid impedance measurement," *2013 IEEE Energy Conversion Congress and Exposition, ECCE 2013*, pp. 3003–3010, 2013.
[13] J. Sun, "Small-signal methods for AC distributed power systems-A review," *IEEE Transactions on Power Electronics*, vol. 24, no. 11, pp. 2545–2554, 2009.
[14] A. Riccobono, M. Mirz, and A. Monti, "Noninvasive Online Parametric Identification of Three-Phase AC Power Impedances to Assess the Stability of Grid-Tied Power Electronic Inverters in LV Networks," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 6, no. 2, pp. 629–647, 2018.
[15] A. Rygg, "Impedance-based methods for small-signal analysis of systems dominated by power electronics," Ph.D. dissertation, Norwegian University of Science and Technology, 2018.
[16] Y. A. Familiant, J. Huang, K. A. Corzine, and M. Belkhayat, "New Techniques for Measuring Impedance Characteristics of Three-Phase AC Power Systems," *IEEE Transactions on Power Electronics*, vol. 24, no. 7, pp. 1802–1810, 2009.
[17] R. Teodorescu, F. Blaabjerg, M. Liserre, and P. C. Loh, "Proportional-resonant controllers and filters for grid-connected voltage-source converters," *IEE Proceedings - Electric Power Applications*, vol. 153, no. 5, pp. 750–762, 2006.