Resynchronization of Distributed Generation based on the Universal Droop Controller for Seamless Transfer Between Operation Modes

Mohammad Amin, *Member, IEEE*, and Qing-Chang Zhong, *Fellow, IEEE*

Abstract—**Distributed generation (DG) inverters can operate in the islanded mode and the grid-connected mode. When these DG inverters operate in the islanded mode, they often form a microgrid. The magnitude and phase of the main grid voltage deviate from the microgrid voltage. If the microgrid is connected to the main grid under such condition, it results in a high transient overcurrent which is harmful to the system. This paper presents a new, simple and effective resynchronization mechanism for the universal droop control (UDC) DG inverters to achieve a seamless transfer from the islanded mode to the grid-connected mode. Simulation and experimental results are provided to verify the effectiveness of the proposed method. The result shows that the high transient overcurrent can be avoided and a seamless connection/reconnection to the main grid can be achieved.**

Index Terms—**Resynchronization, seamless transfer, islanded mode, microgrid, universal droop control inverter, distributed generation.**

I. INTRODUCTION

POWER electronics inverters are the enabling technology for integrating renewable energy such as wind power, solar power-based distributed generation (DG) to the grid [1]–[5]. They often form a microgrid before being connected to the main grid [6]. A simplified structure of such microgrid is shown in Fig. 1. Both the inverter and local load are connected to the main grid through an active switch S_1. The state of the switch S_1, as well as the operation mode of the DG inverter, depend upon the state of the main grid. Considering this study case, two operating modes of the DG inverter can be achieved. The first operating mode is the grid-connected mode. In this mode, the main objective of the inverter is to export the available power from the renewable sources to the grid. Moreover, the inverter offers ancillary services to the grid. In particular, the ancillary services provided by these inverters are the voltage and frequency support [7], [8]. Such application is gaining popularity and even becomes mandatory in the new

grid code at the state level and upcoming IEEE Standards. Another operation mode of the inverter refers to the islanded mode or microgrid operation. During the grid fault or other abnormal operation, the inverter is disconnected from the main grid when the inverter supplies power to the local load. Under such condition, the inverter works in the grid forming mode and regulates the voltage and frequency of the microgrid [9], [10]. When the grid voltage is restored, the magnitude and phase of the microgrid voltage deviate from the main grid. If the inverter is connected to the grid under such condition, it results in a high transient overcurrent which is harmful to the system. Therefore, before turning on the switch S_1, it is necessary to resynchronize the microgrid voltage to the main grid to avoid such a high inrush current.

Many researches have been conducted for a seamless transfer between operation modes of the DG inverter-based microgrid [11]–[26]. The transfer from the grid-connected mode to the islanded mode can be obtained with a mechanism embedded in the control of the inverter by simply turning off the switch S_1 and inverters share the load naturally based on their droop setting in the islanded mode [27], [28]. However, the reconnection of the microgrid to the main grid is not that straight forward as only turning on the switch S_1. For a smooth transfer from the islanded mode to the grid-connected mode, the voltage of the microgrid must be synchronized with the grid before connection. The synchronization is usually accomplished by detecting the phase difference between the main grid and microgrid voltage, where the phase is detected using a phase-locked-loop (PLL) [13]–[18]. The PLL presents a proper performance under a balance voltage condition, however, its performance deficits significantly under an unbalanced and distorted condition of the grid voltage. Moreover, its
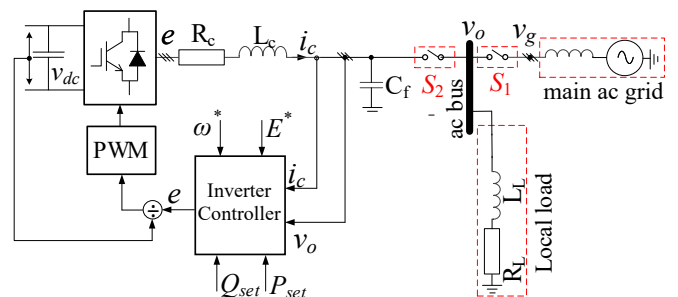

Fig. 1: A simple microgrid: a DG inverter with a local load.

performance is very sensitive to a sudden change of phase of the voltage, even sometimes, it introduces an instability problem in DG inverters [29]. Frequency-locked-loop (FLL) is often used for synchronization purpose [19]. However, the FLL brings a computational complexity in tuning the parameters and is difficult in hardware realization. A droop-based synchronization mechanism is proposed in [13] where it needs a dedicated dispatch unit only for the purpose of mode transfer. Hu *et al* in [12] proposed a virtual impedance-based mode transfer. The virtual impedance takes into action to limit the inrush current when it detects a high current in the inverter, however, a resynchronization is not achieved before connection.

Recently, a universal droop controller (UDC) is proposed in [30] for inverters where an initial synchronization mechanism is embedded with the UDC to form a self-synchronized UDC without a PLL or FLL [31]. The UDC inverter operates both the grid-connected mode and islanded mode. The UDC presented in [30], [31] can transfer its operation mode from the grid-connected mode to the islanded mode, however, it cannot switch its operation mode from the islanded mode to the grid-connected mode due to lack of resynchronization of the microgrid voltage with the main grid voltage. This paper fills this gap by proposing a voltage resynchronization mechanism that allows the UDC a smooth mode transfer from the islanded mode to the grid-connected mode. The contribution of this paper to the state-of-the-art comprises the following:

- Proposing a new, simple and effective resynchronization mechanism for DG based on the UDC to achieve seamless transfer from the islanded mode to the grid-connected mode.
- Developing a line-frequency-averaged small-signal model considering both frequency and voltage control loops of the inverter to investigate the dynamic stability of the integrated resynchronization loop.

Extensive simulation and experimental results are provided to verify the effectiveness of the proposed resynchronization method. The result shows that the high transient overcurrent can be avoided and a seamless connection/reconnection of the DGs based on the UDC to the grid is achieved. Though the proposed resynchronization mechanism is embedded for the UDC, the proposed method can be extended to other controllers for a smooth transfer of modes between the microgrid and the grid-connected mode. Future work will focus on such applications.

The rest of the paper is organized in the following. Section II presents the proposed resynchronization mechanism. Section III presents the realization of the proposed resynchronization mechanism with the UDC inverter. The frequency domain analysis of the resynchronization-loop is discussed in Section IV. The simulation and experimental validation are presented in Section V. Finally, this study is concluded in Section VI.

II. THE PROPOSED RESYNCHRONIZATION MECHANISM

During an abnormal operation and fault conditions of the grid, the DG inverter is disconnected from the main ac grid when the inverter supplies power to the local load. Under such
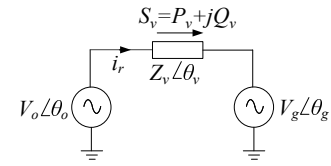

Fig. 2: A simplified circuit diagram for power flow calculation.

condition, the inverter forms a microgrid and regulates the voltage and frequency of the microgrid. When the grid voltage is restored, the magnitude and phase of the microgrid voltage deviate from the main grid. The voltage error between the microgrid and the main grid can be given by

$$v_{err} = v_o - v_g. \tag{1}$$

For the purpose of implementing the resynchronization mechanism, a virtual impedance $Z_v = sL + R$ is introduced in between the microgrid ac bus and main grid. A virtual current i_r can be generated via passing the voltage error v_{err} through the virtual impedance as

$$i_r = \frac{v_o - v_g}{sL + R}. \tag{2}$$

As shown in Fig. 2, the virtual active power and reactive power flow between the microgrid and the main grid due to this virtual current can be calculated as

$$P_v + jQ_v = v_o i_r^*. \tag{3}$$

Thus, the virtual real power and reactive power can be given by

$$\begin{bmatrix} P_v \\ Q_v \end{bmatrix} = \begin{bmatrix} \cos\theta_v & -\sin\theta_v \\ \sin\theta_v & \cos\theta_v \end{bmatrix} \begin{bmatrix} \frac{V_o V_g}{Z_v}\cos(\theta_o - \theta_g) - \frac{V_o^2}{Z_v} \\ -\frac{V_o V_g}{Z_v}\sin(\theta_o - \theta_g) \end{bmatrix} \tag{4}$$

where V_o and V_g are the RMS value of the microgrid ac bus voltage and the main grid voltage, respectively, and θ_o and θ_g are their corresponding phase angle, Z_v and θ_v is the magnitude and angle of the virtual impedance.

The virtual impedance can be selected to be an inductive or resistive depending on the control implementation of the resynchronization loop. θ_v is $\pi/2$ rad for an inductive impedance, thus, the active power and reactive power resulting from the virtual current can be given by

$$\begin{bmatrix} P_v \\ Q_v \end{bmatrix} = \begin{bmatrix} \frac{V_o V_g}{Z_v}\sin(\theta_o - \theta_g) \\ \frac{V_o V_g}{Z_v}\cos(\theta_o - \theta_g) - \frac{V_o^2}{Z_v} \end{bmatrix}. \tag{5}$$

If the virtual impedance is assumed to be resistive, the impedance angle becomes $\theta_v = 0$. Hence, the active power and reactive power resulting from the virtual current can be given by

$$\begin{bmatrix} P_v \\ Q_v \end{bmatrix} = \begin{bmatrix} \frac{V_o V_g}{Z_v}\cos(\theta_o - \theta_g) - \frac{V_o^2}{Z_v} \\ -\frac{V_o V_g}{Z_v}\sin(\theta_o - \theta_g) \end{bmatrix}. \tag{6}$$

The equations (5) and (6) indicate that the virtual active power P_v and reactive power Q_v can only be zero when

$$V_o = V_g \text{ and } \theta_o = \theta_g, \tag{7}$$
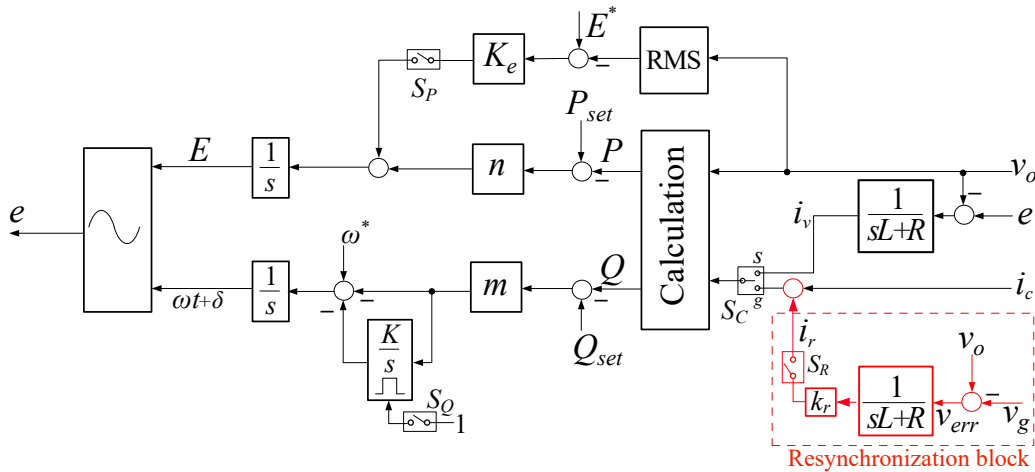
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Fig. 3: Self-synchronized universal droop controller with the resynchronization mechanism

in other words, when the microgrid voltage v_o is synchronized with the grid voltage v_g. In order to achieve this, the current carried by the virtual impedance will be regulated to zero in the steady-state by the inverter controller. Hence, both P_v and Q_v will be eventually driven to zero as required for the resynchronization condition.

III. REALIZATION OF THE RESYNCHRONIZATION MECHANISM WITH THE UDC

A. Overview of the Self-synchronized UDC

The self-synchronized universal droop controller (UDC) is shown in Fig. 3 without the dashed box. The UDC is proposed as [30]

$$E = \frac{1}{s}\left[n\left(P_{set} - P\right) + S_P K_e\left(E^* - V_o\right)\right] \quad (8)$$

$$\omega = \omega^* - m\left(Q_{set} - Q\right)\left(1 + S_Q \frac{K}{s}\right) \quad (9)$$

where E^* is the reference RMS value of the output voltage; ω^* is the rated system frequency; n and m are the droop coefficient; P_{set} and Q_{set} are the reference active and reactive power, respectively; K_e and K are positive gain, and S_P and S_Q are switching states, 1 for ON and 0 for OFF. The UDC is applicable to inverters with an impedance angle of $-\pi/2$ to $\pi/2$ rad [30].

Before turning on the PWM, the inverter voltage e should be synchronized with the terminal voltage v_o. In order to achieve that, the switch S_C is put at the position "s" and the power reference values P_{set} and Q_{set} are set zero, respectively. A virtual current i_v is generated via passing the voltage error $e - v_o$ through the virtual impedance $sL + R$ as shown in Fig. 3 for the initial synchronization. More detailed on this self-synchronization mechanism can be found in [31].

B. Resynchronization Process

When the grid voltage is restored, the voltage magnitude may or may not remain the same and it is usual that the phase will not be the same. The transient overcurrent results in mainly for the phase difference between these two voltages

[19]. The magnitude of the virtual current can be as high as several times of the rated current depending on the phase difference and magnitude of the virtual impedance. Such a high transient current may introduce an instability problem with the controller. Therefore, a positive constant k_r is introduced, which value is kept in between $0 < k_1 \leq 0.5$, in order to limit the virtual current. Moreover, an additional switch S_R is added with the UDC for enabling the resynchronization mechanism. Fig. 3 depicts the self-synchronized UDC with the resynchronization block in the dashed box. When the switch S_R is ON, the total current of the controller is

$$i_t = i_c + i_r \quad (10)$$

where i_c is the inverter actual current. The actual power send by the inverter is calculated using the ac bus voltage v_o and inverter current i_c as $S = P + jQ = v_o i_c^*$, when the virtual power is calculated using the virtual current i_r as given by (3). Hence, the total active power and reactive power are

$$P = P_i + P_v \text{ and } Q = Q_i + Q_v \quad (11)$$

where P_i and Q_i are the actual active power and reactive power drawn by the connected local load during the resynchronization period. Since no active power and reactive power will be exchanged between the main grid and microgrid at the steady-state, the current carried by the virtual impedance is regulated to zero. Both P_v and Q_v will eventually drive to zero. P_v and Q_v become zero when $V_o = V_g$ and $\theta_o = \theta_g$, meaning that the microgrid voltage v_o is synchronized with the grid voltage v_g. Now, the switch S_1 can be turned on, any time to reconnect the inverter to the grid.

IV. RESYNCHRONIZATION LOOP ANALYSIS

Improper design of the resynchronization-loop parameters such as the virtual impedance and the positive gain may bring an instability problem. Therefore, proper design and control-loop analysis need to be carried out before the hardware realization of the resynchronization mechanism. In order to investigate the performance and stability of the resynchronization loop, a line-frequency-averaged small-signal model is derived. The small-signal model has been derived based on
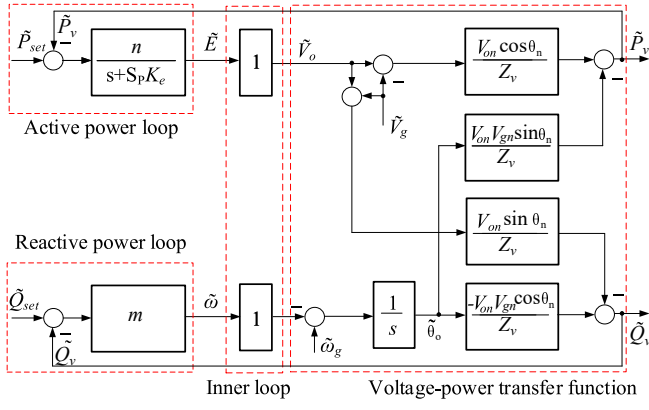
Fig. 4: Line-frequency-averaged small-signal model of the UDC for the resynchronization-loop.

the mathematical model of the UDC and the resynchronization mechanism described in previous sections.

With a proper design of the control loop, the capacitor voltage can accurately track the reference voltage, thus, it can be written as

$$E \approx V_o. \tag{12}$$

During the resynchronization period, the inverter operates in the droop mode. Thus, the output voltage of the UDC in (8) can be given in the small-signal form by

$$\tilde{V}_o = \frac{n}{s + K_e} \left(\tilde{P}_{set} - \tilde{P}_i - \tilde{P}_v \right) \tag{13}$$

where the tilde sign ˜ is used to represent the variables in the small-signal form.

The frequency of the inverter from (9) can be given in the small-signal form by

$$\tilde{\omega} = \tilde{\omega}_g - m \left(\tilde{Q}_{set} - \tilde{Q}_i - \tilde{Q}_v \right). \tag{14}$$

As shown in Fig. 3, the phase of the output voltage of the UDC is obtained by applying Laplace transformation to (14). In the small-signal form, the phase can be given by

$$\tilde{\theta}_o = \frac{1}{s} \left(\tilde{\omega}_g - m \left(\tilde{Q}_{set} - \tilde{Q}_i - \tilde{Q}_v \right) \right). \tag{15}$$

Eqns. (13) and (14) give a voltage to the active power and a frequency to the reactive power relationship, respectively. In order to complete the model, it needs a voltage-power transfer function. Note that the UDC (8-9) takes the form of the droop controller for R-inverters, i.e., the impedance is dominantly resistive. The virtual impedance is also assume dominantly resistive. Therefore, the active power and reactive power in (6) can be presented in the small-signal form as

$$\tilde{P}_v = -\frac{V_{on}V_{gn}\sin\theta_n}{Z_v}\tilde{\theta} + \frac{V_{on}\cos\theta_n}{Z_v}\left(\tilde{V}_g - \tilde{V}_o\right) \tag{16}$$

$$\tilde{Q}_v = -\frac{V_{on}V_{gn}\cos\theta_n}{Z_v}\tilde{\theta} - \frac{V_{on}\sin\theta_n}{Z_v}\left(\tilde{V}_g + \tilde{V}_o\right) \tag{17}$$

where $\theta = \theta_o - \theta_g$, the subscript "$n$" is used to represent the value of the variable at a steady-state point. Assumed that the phase of the grid voltage is the reference phase, i.e., $\theta_g = 0$, hence, it can be written as $\theta = \theta_o$.

TABLE I: Parameters of the experimental system.

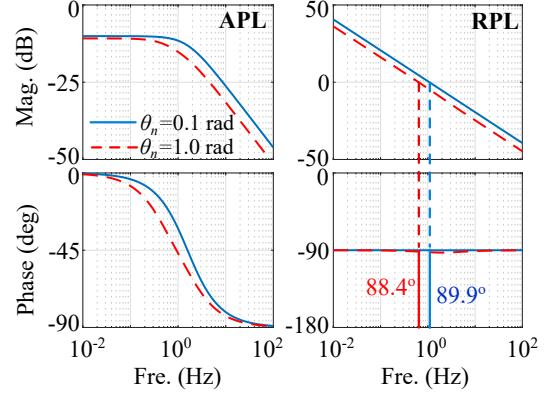| Parameters	Values
Rated phase voltage (RMS), V_o	120 V
Rated dc voltage,V_{dc}	400 V
Rated frequency, f	60 Hz
Inverter series inductance, L_c	2.2 mH
Filter capacitance, C_f	22 μF
Virtual inductance, L	2.2 mH
Virtual Resistance, R	8 Ω
Positive gain, k_r	0.5

Fig. 5: Frequency response of the APR and RPL for different phase difference between the microgrid voltage and the main ac grid voltage.

During the resynchronization process, the actual active power P_i and reactive power Q_i of the inverter will be constant if we assume that the local load remains unchanged for this short period. Therefore, when deriving the small-signal model for the resynchronization loop, $\tilde{P}_i$ and $\tilde{Q}_i$ are assumed to be disturbances, and they are set to zero in (13) and (15). Hence, based on (13)-(17), a line-frequency-averaged small-signal model of the UDC for the resynchronization-loop is derived as shown in Fig. 4.

According to Fig. 4, if the coupling terms are ignored, the open-loop gain of the active power loop (APL), $T_p(s)$ and
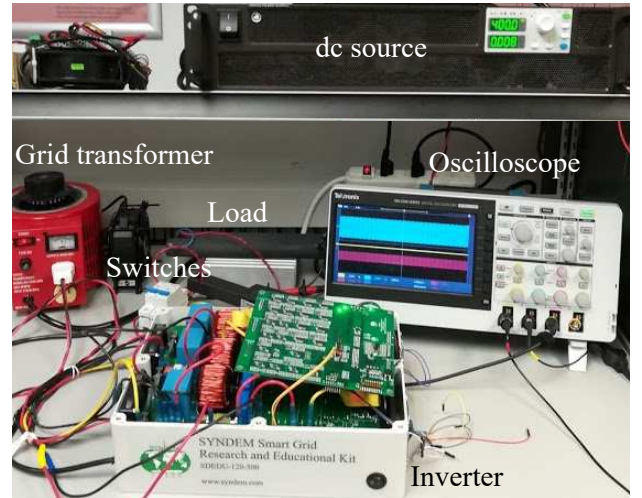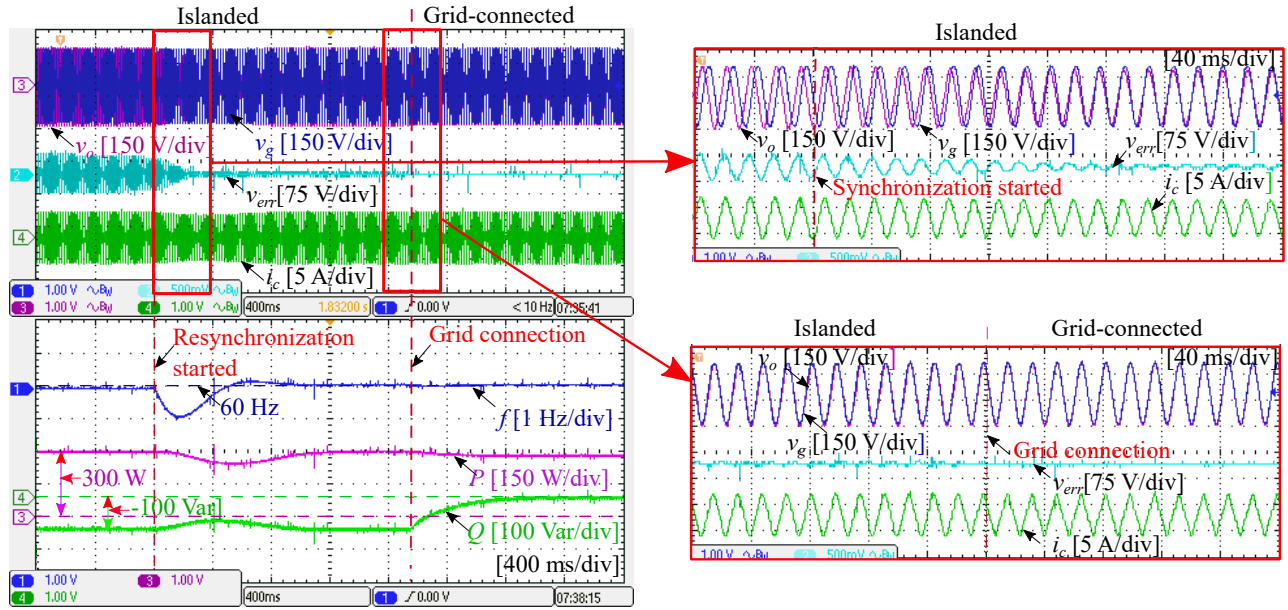

Fig. 6: Experimental setup.

Fig. 7: Experiment of the resynchronization and mode transfer from the islanded mode to the grid-connected mode.

reactive power loop (RPL), $T_q(s)$ can be obtained as

$$T_p(s) = \frac{V_{on}\cos\theta_n}{Z_v}\frac{n}{s+K_e} \qquad (18)$$

$$T_q(s) = \frac{V_{on}V_{gn}\cos\theta_n}{Z_v}\frac{m}{s}. \qquad (19)$$

When deriving the APL transfer function, $\tilde{V}_g$, $\tilde{\omega}_g$ and $\tilde{Q}_{set}$ are assumed to be disturbances, and they are set to zero. Thus, considering the coupling effect, the loop-gain of the APL is obtained as

$$T_{pc}(s) = T_p(s)\left(1 + \frac{T_q(s)}{1+T_q(s)}\sin^2\theta_n\right). \qquad (20)$$

Similarly, when deriving the RPL transfer function, $\tilde{V}_g$, $\tilde{\omega}_g$ and $\tilde{P}_{set}$ are assumed to be disturbances, and they are set to zero. Considering the coupling effect, the loop-gain of the RPL is obtained as given by

$$T_{qc}(s) = T_q(s)\left(1 + \frac{T_p(s)}{1+T_p(s)}\sin^2\theta_n\right). \qquad (21)$$

The APL and RPL should have a sufficient phase margin to ensure a robust resynchronization for a seamless transfer of the operation modes. Frequency responses of the APL and RPL have been studied to ensure a sufficient phase margin of the control-loop for different phase difference of the voltage with the designed parameters. The virtual impedance is selected in such a way that the impedance becomes dominantly resistive. The parameters of the experimental system are given in Table I. The virtual inductor is selected $L = 0.5 \times L_c \approx 1$ mH and the virtual resistor is set to $R = 10 \times \omega_g L_c \approx 8\,\Omega$ in order to have a dominant resistive impedance. Fig. 5 shows the bode plot of the APL and RPL for two values of the phase difference, i.e., $\theta = 0.1$ rad and 1.0 rad between the microgrid and main grid voltage. As can be seen, both APL and RPL have a sufficient phase margin, which ensures the robustness and the stability of the resynchronization loop. Eqns. (18) and (19) indicate

that a higher value of the virtual impedance increases the stability margin, on the other hand, it decreases the response time. Therefore, the selection of the virtual impedance is a trade-off between the response time and the stability of the resynchronization loop.

V. VALIDATION OF THE RESYNCHRONIZATION MECHANISM THROUGH EXPERIMENT AND SIMULATION

In order to verify the effectiveness of the proposed resynchronization method for mode transfer, simulation and experiments are carried out. First, experiments have been carried out for a single-phase system having one inverter. After successfully validated for one inverter, it has been tested for a system having three inverters.

A. Experimental Results from a Microgrid with one Inverter

The investigated microgrid system is shown in Fig. 1. The self-synchronized UDC together with the resynchronization mechanism is implemented on a TMS320F28335 DSP with the sampling frequency of 10 kHz. Some signals are sent out via a DAC chip and recorded with an oscilloscope. A photo of the experimental setup based on a SYNDEM smart grid research and educational kit is shown in Fig. 6. The parameters of the inverter system are given in Table I. The local load is 300 W. The experimental result is shown in Fig. 7. As can be seen, initially, the inverter operates in the islanded mode and supplies power to the local load, while regulating the rated voltage and frequency. The first transient at 800 ms in Fig. 7 is for turning on the switch S_R to start the resynchronization. A zoom view of the resynchronization is shown in the right-top plot of Fig. 7. As can be seen, before starting the resynchronization, there is a large phase difference between the voltage of the microgrid and main grid. When the switch S_R is on, the phase difference and v_{err} start reducing.
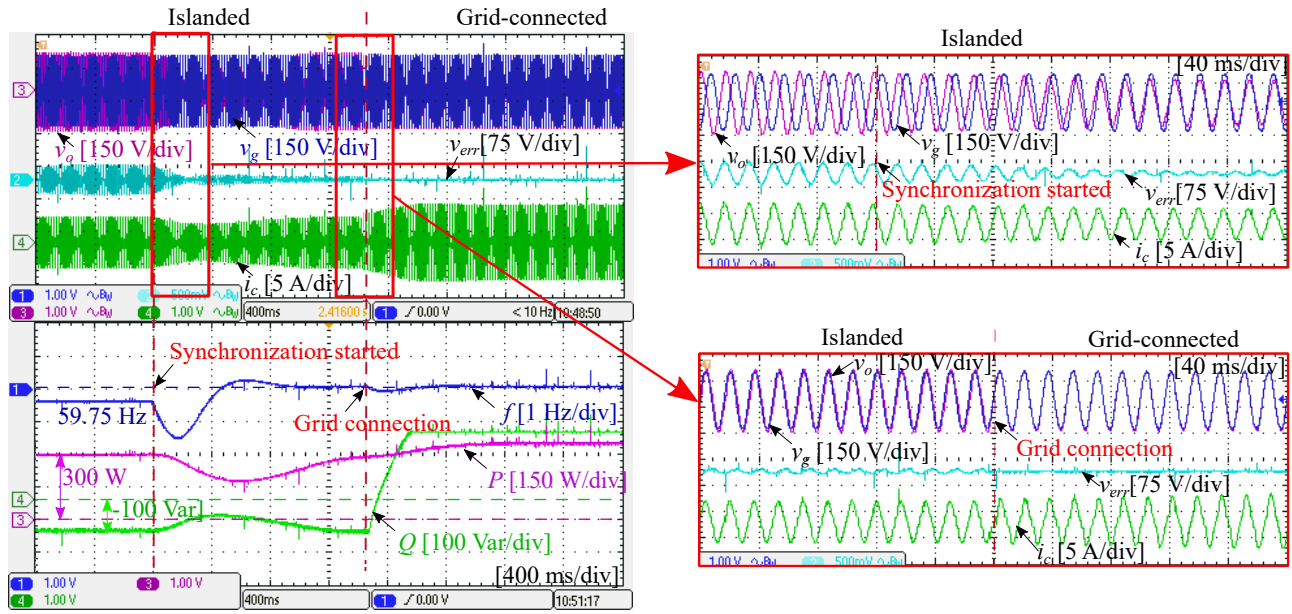
Fig. 8: Experiment of the resynchronization and mode transfer from the islanded mode to the grid-connected mode: the main grid frequency is higher than the microgrid frequency.
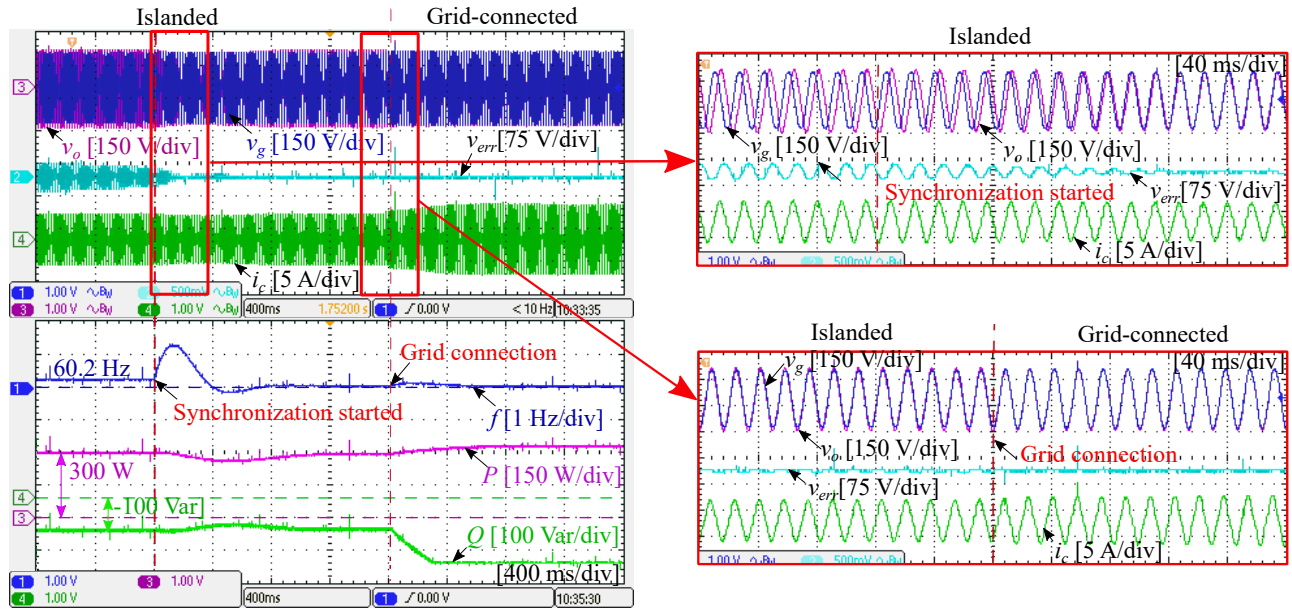

Fig. 9: Experiment of the resynchronization and mode transfer from the islanded mode to the grid-connected mode: the main grid frequency is lower than the microgrid frequency.

After some cycles, v_{err} becomes nearly zero, which means that the microgrid voltage synchronizes with the main grid. When the synchronization is completed, the active switch S_1 can be turned on anytime to connect the microgrid to the main grid. The grid connection is also shown in Fig. 7. The right-bottom plot shows the grid connection. The microgrid is smoothly reconnected to the main grid without any transient overcurrent.

The next two experiments are carried out for the case when the frequency of the microgrid is not the same as the main grid. In the first experiment, the microgrid operates with a frequency lower than the main grid frequency. The experimental result is

presented in Fig. 8. The resynchronization is started when the microgrid frequency is 59.75 Hz. As the switch S_R is turned on for resynchronization, the controller quickly responded to synchronize with the grid. Within a few cycles, the microgrid is able to track the frequency of the main grid. The voltage error v_{err} becomes nearly zero. A zoom view of the resynchronization is shown in the right-top plot of Fig. 8. As can be seen, before starting the resynchronization, there is a big phase difference between the voltage of the microgrid and main grid. When the switch S_R is on, the phase difference and v_{err} start reducing. After some cycles, v_{err} becomes nearly zero. The microgrid voltage has synchronized with the main grid. When
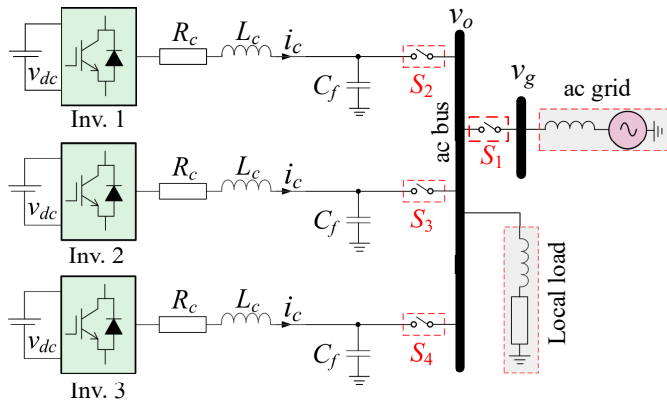
Fig. 10: Microgrid: DG inverters with a local load.

TABLE II: Parameters of the simulated system.

Parameters	Values
Rated Power of the inverter	20 kVA
Rated phase voltage (RMS), V_o	120 V
dc voltage, V_{dc}	400 V
Rated frequency, f	60 Hz
Inverter series inductance, L_c	1.4345 mH
Inverter series resistance, R_c	0.1082 Ω
Filter capacitance, C_f	22 μF
Virtual inductance, L	0.14 mH
Virtual Resistance, R	0.1082 Ω
Positive gain, k_r	0.5

the synchronization is complete, the switch S_1 is turned on to connect the microgrid to the main grid. The grid connection is shown in the right-bottom plot of Fig. 8. The microgrid is smoothly connected to the main grid without any transient overcurrent.

The last experiment is for the case when the main ac grid frequency is lower than the microgrid frequency. The experimental result is presented in Fig. 9. The resynchronization is started when the microgrid frequency is 60.2 Hz. When the switch S_R is turned to start the resynchronization, the controller quickly responded to synchronize with the grid. Within a few cycles, the microgrid voltage is able to track the voltage of the main grid. Before starting the synchronization, there is a big phase difference between voltages. When the switch S_R is on, the phase difference starts reducing. After some cycles v_{err} becomes zero. When the synchronization is complete, the active switch S_1 is turned on to connect the microgrid to the main grid. The right-bottom plot of Fig. 9 shows the grid connection. The microgrid is smoothly reconnected to the main grid without any transient overcurrent.

B. Microgrid with Multiple DG Inverters Connected in Parallel

The resynchronization method can be applied to a microgrid having multiple DG inverters operating in parallel. A simulation example of a such microgrid is shown in Fig. 10 which has three three-phase 20-kVA DG inverters connected in parallel. The parameters of inverters are given in Table II. The UDC is used as the control of these inverters. The active power is set to 20 kW for inverter 1, 15 kW for inverter 2 and 10 kW for
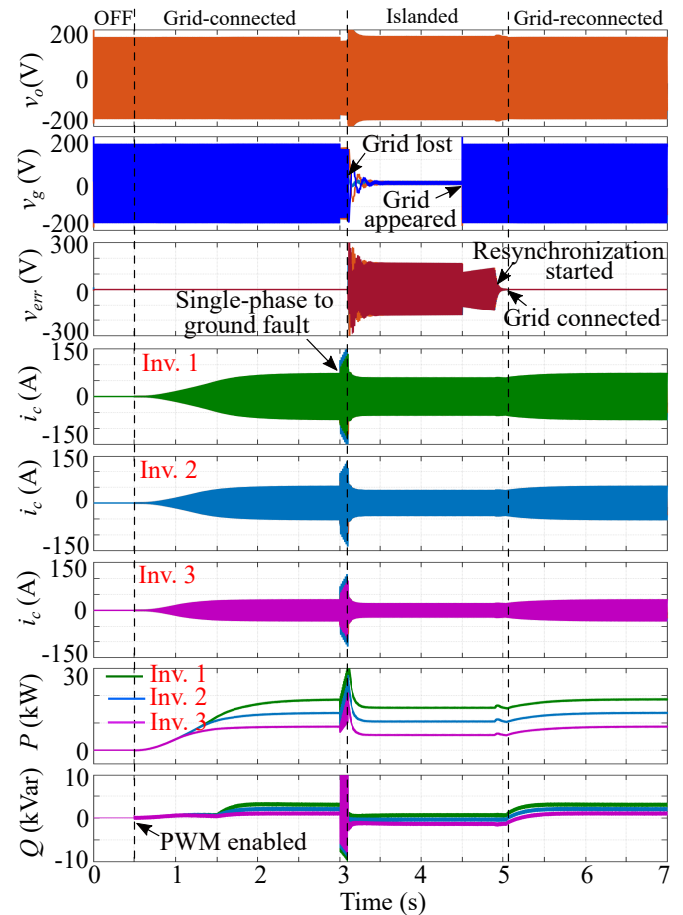

Fig. 11: Simulation of an extended microgrid: Initially, the inverter is OFF. The PWM is enabled at 0.5 s. A single-phase to ground fault occurs at 3.0 s. The switch S1 is opened at 3.1 s to isolate the faulty grid. The grid is restored at 4.5 s. The resynchronization started at 4.90 s and the islanded mode transferred to the grid-connected mode at 5.05 s.

inverter 3, respectively, and the reactive power is set to 3 kVar, 2 kVar and 1 kVar, respectively. The local load power is 30 kW. The microgrid has been implemented in MATLAB/Simulink association with the SimPower blockset. A simulation has been carried out and the simulation results are presented in Fig. 11. The simulation scenario is divided into four parts: i) inverter OFF; ii) grid-connected operation, iii) islanded operation and resynchronization and iv) grid-reconnected. Fig. 11 shows the ac bus voltages, grid voltages, voltage error, inverter currents, inverter output active power and reactive power. Initially, all inverters operate in the self-synchronization mode when the PWM of inverters is off. The local load is powered by the main grid. At 0.50 s, the PWM of the inverters is enabled and inverters start sending power according to their set power. At 3.0 s, a single-phase to ground fault occurs. The switch S_1 is opened at 3.1 s to isolate the faulty grid. The inverters supply power to the local load and share the load according to their droop gain and set power. At 4.50 s, the main grid is restored. As can be seen, there is a large voltage error v_{err} when the main grid is lost which remain consistent after the grid appeared. A zoom view of the resynchronization and grid
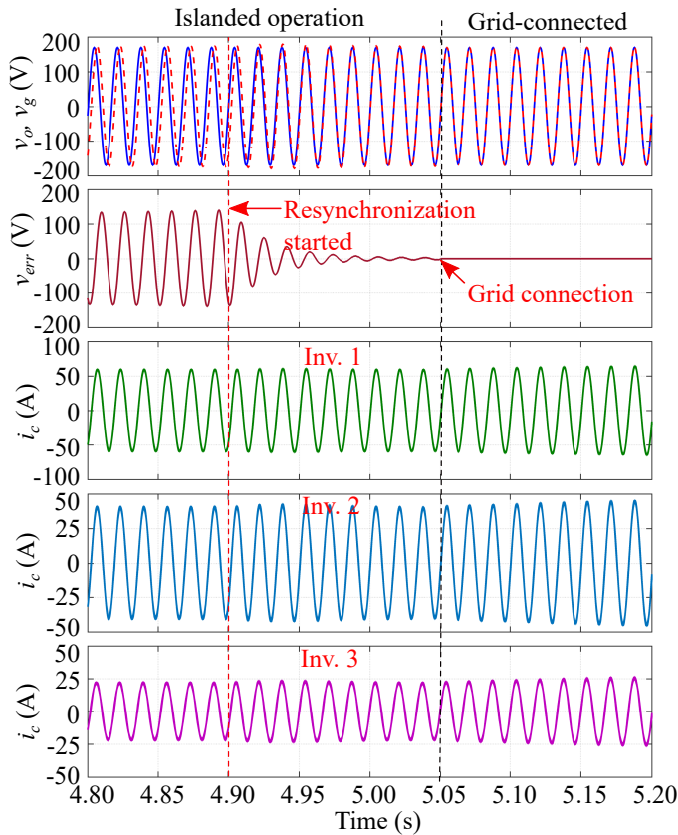
Fig. 12: Simulation of resynchronization and grid reconnection: at 4.90 s, the switch S_R is on to start the resynchronization process; at 5.05 s, the switch S_1 is turned on and the islanded mode transferred to the grid-connected mode.

connection is shown in Fig. 12. The top plot of Fig. 12 shows the phase-A voltage of the main grid and microgrid. As can be seen, the voltage magnitude and phase are different. At 4.90 s, the switch S_R is turned on to start the resynchronization. The microgrid voltage is able to track the main grid. Within a few cycles, the microgrid ac bus voltage is synchronized with the main grid. Since the voltage is synchronized, the active switch S_1 can be turned on anytime to connect the microgrid to the main grid. At 5.05 s, the active switch S_1 is turned on to connect the microgrid to the main grid. Since the voltages are synchronized properly, there is no transient overcurrent. The islanded mode has transferred to the grid-connected mode smoothly.

VI. CONCLUSION

The paper presents a simple and effective resynchronization mechanism for DGs based on the universal droop controller to achieve a seamless transfer from the islanded mode to the grid-connected mode. A line-frequency-averaged small-signal model is developed considering both frequency and voltage control loops of the system involving the proposed control and synchronization to investigate the dynamic stability and behavior of the integrated resynchronization loop. Extensive simulation and experimental results are provided to verify the effectiveness of the proposed resynchronization method. The result shows that the high transient overcurrent can be avoided and a seamless connection/reconnection to the main grid can be achieved.

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Qing-Chang Zhong (M'04-SM'04-F'17) received two Ph.D. degrees, one from Imperial College London in 2004 and the other from Shanghai Jiao Tong University in 2000. He holds the Max McGraw Endowed Chair Professor in Energy and Power Engineering at Dept. of Electrical and Computer Engineering, Illinois Institute of Technology, and is the Founder & CEO of Syndem LLC, Chicago, USA. He serves/d as a Steering Committee member for IEEE Smart Grid, a Distinguished Lecturer for IEEE PELS/CSS/PES societies, an Associate Editor for IEEE TAC/TIE/TPELS/TCST/Access/JESTPE, and a Vice-Chair for IFAC TC Power and Energy Systems. He spent nearly 15 years in the UK and was the Chair Professor in Control and Systems Engineering at University of Sheffield before moving to Chicago. He was a Senior Research Fellow of Royal Academy of Engineering, UK, and the UK Representative to European Control Association. He proposed the synchronized and democratized (SYNDEM) smart grid architecture to unify the integration of non-synchronous distributed energy resources and flexible loads. He is the (co-)author of four research monographs.

Mohammad Amin (M'11) received the B.Sc. degree in electrical and electronic engineering from Chittagong University of Engineering and Technology, Bangladesh, in 2008, the M.Sc. degree in electric power engineering from Chalmers University of Technology, Sweden, in 2011 and the Ph.D. degree in engineering cybernetics from Norwegian University of Science and Technology, Norway, in 2017.

From 2008 to 2013, he was with the Department of Electrical and Electronic Engineering, International Islamic University Chittagong, Bangladesh. In 2015, he was a Ph.D. Visiting Scholar with the Wind Power Research Center, Shanghai Jiao Tong University, Shanghai, China. From 2017 to 2019, he was a Senior Research Associate with the Department of Electrical and Computer Engineering, Illinois Institute of Technology, Chicago, IL, USA. Currently, Dr. Amin is an Associate Professor with the Department of Electric Power Engineering at Norwegian University of Science and Technology. He is the recepient of the 2018 IEEE JESTPE First Prize Paper Award from IEEE Power Electronics Society. His research interest focus on power electronics application to power system, wind and solar energy integration, high voltage direct current (HVDC) transmission, microgrid, smart grids, hybrid or fully electric vehicles, and robust control theory for power electronics system.