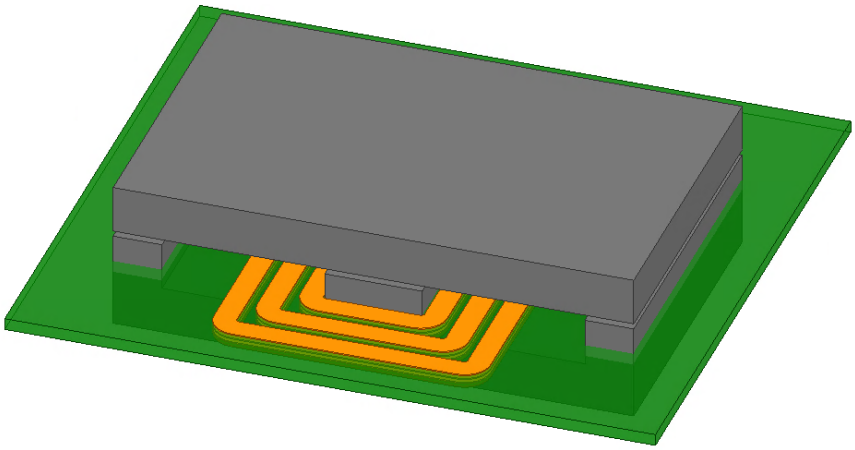
Masteroppgåve

NTNU
Noregs teknisk-naturvitskaplege universitet
Fakultet for informasjonsteknologi og elektroteknikk
Institutt for elkrafteknikk

Ådne Finnes Engetrøen

A 1 kW PFC converter with GaN-transistors and planar magnetics

Masteroppgåve i Energi og miljø
Veileder: Roy Nilsen, Tore M. Undeland & Ole Christian Spro
Juni 2019



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Preface

This master's thesis concludes my degree in Energy and Environmental Engineering carried out at the Department of Electrical Power Engineering at Norwegian University of Science and Technology (NTNU) in Trondheim, June 2019.

The thesis is a continuation of a specialization project conducted during the autumn of 2018. This specialization project worked as a preliminary analysis and literature study for this master's thesis. Both the specialization project and the master thesis has been conducted in collaboration with Eltek.

This last year has been one of the most challenging, but also one of the years with highest learning outcome in my life. It has been very exciting to work both with power semiconductors and magnetic components. To see the advantages of one device giving mutual benefits throughout the rest of the converter has been interesting. The power electronics industry faces a shift towards faster switching devices enabled by new materials, which opens possibilities for new and creative solutions. This is one of the things I find most motivational and intriguing, and it is also the main reason I chose to write my master's thesis within this field.

I would like to express my sincere gratitude to Ph.D candidate Ole C. Spro and Professor Tore M. Undeland for valuable guidance sessions throughout both the specialization project and the master. I would also like to give a special thanks to the R&D division and the rest of the staff at Eltek. Eltek was helpful, hospitable and gave valuable advice and guidance.

Ådne Finnes Engetrøen

Trondheim, June 2019

Summary

Increased power density, cost reduction, increased efficiency and increased reliability are four of the most important targets in the semiconductor and converter industry today. With GaN-transistors, multiple of these targets are achievable. The four important targets can be achieved in larger systems such as converters and even on the power system basis, not only in specific components.

Supreme characteristics of GaN-devices paves the way for high frequency and high efficiency converters. The low switching losses allow a high switching frequency which opens new possibilities regarding new converter topologies and better utilization of conventional converters. The increased switching frequency also opens possibilities of a reduction in physical sizes of magnetic components. Innovative designs of magnetic components which previously have been neglected can become more of a reality with the advantages of GaN-devices, and have become important for Eltek. This master thesis examines the advantages of wide bandgap (WBG) devices, mostly GaN-devices, compared to the traditional silicon devices. The thesis found that the advantages of GaN-devices propagates throughout a converter, especially in reducing magnetic components.

For inductors in converters, the inductance requirement tends to drop with increasing frequency, and for transformers, the core volume decreases with increasing frequency. A planar inductor was designed and optimized for use in an Eltek 1 kW classic PFC boost converter with GaN-transistors, giving a switching frequency of 600 kHz. Both the parametric sweeps performed, and the optimization process pointed towards optimal results. Distributing air gaps, keeping conductors far from the air gaps, and aligning conductors parallel, not orthogonal to the fringing flux are three specific examples of design rules which can be concluded from this thesis. Placing the conductors parallel to the fringing flux, or rather placing air gaps such that this occurs, goes against the typical manufacturing these types of cores. Distributed air gaps with fringing fields parallel to the wide side of the planar conductors showed total loss reduction of about 21% in some specific cases.

Samandrag

Auka krafttettleik, kostnadsreduksjon, auka effektivitet og auka driftssikkerheit er fire av dei viktigaste målsetjingane i halvleiarindustrien i dag. Ved bruk av GaN-halvleiarar er fleire av desse målsetjingane innan rekkevidde, ikkje berre på komponentbasis men også på større system som omformarar og sjølv kraftsystemet.

Dei overlegne materialeigenskapane til GaN banar veg for høgfrekvente og høgeffektive kraftomformarar. Låge svitsjetap åpnar opp for høge svitsjefrekvensar som igjen åpnar opp moglegheiter for nye omformartopologiar og betre utnytting av konvensjonelle omformarar. Den auka svitsjefrekvensen mogleggjer også reduksjon i fysisk storleik på magnetiske komponentar. Innovative design av magnetiske komponentar som tidlegare har blitt gløymt kan igjen bli realistisk ved utnytting av eigenskapane til GaN, og dette er viktig for Eltek. Denne masteroppgåva undersøkjer fordelane til einingar med bredt bandgap (WBG), for det meste GaN, opp mot det meir tradisjonelt brukte silisium. Oppgåva har gitt resultat som viser at fordelane til GaN-einingar forplantar seg gjennom omformaren, særskild i å redusere magnetiske komponentar.

For spolar i omformarar er induktanskravet generelt synkande for aukande svitsjefrekvensar. For transformatorar er den same trenden til stades, nemlig at kravet til tverrsnitt, og dermed volum på kjerna synkjer for aukande frekvens. Ein planarspole vart designa og optimert for bruk i ein Eltek 1 kW klassisk PFC boost omformar med GaN-transistorar, noko som gav ein svitsjefrekvens på 600 kHz. To optimeringsmetoder vart nytta, og begge peika mot same optimal løysing. Fordelte luftgap, halde koparen langt frå luftgapa, og å rette inn koparen parallell, og ikkje ortogonal på det magnetiske spredefeltet er tre konkrete eksempel på designreglar ein kan konkludere med i denne oppgåva. Å plassere koparen parallell til spredefeltet, eller meir presist, å plassere luftgapet slik dette skjer, er ikkje ein typisk måte kjernar vert produserte. Fordelte luftgap med magnetisk spredefelt parallelt til den breie sida av koparen viste total tapsreduksjon på omlag 21% i visse tilfeller.

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Abbreviations

Acronym	Definition
WBG	Wide Bandgap
PFC	Power Factor Correction
THD	Total Harmonic Distortion
CM	Common Mode
DM	Differential Mode
RF	Radio Frequency
e-mode	Enhancement mode
d-mode	Depletion mode
HEMT	High-Electron-Mobility Transistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PCB	Printed Circuit Board
EMI	Electromagnetic Interference
IGBT	Insulated-Gate Bipolar Transistor
SJ	Super-Junction
FEM	Finite Element Method
CCM	Continuous Conduction Mode
CrCM	Critical Conduction Mode
DCM	Discontinuous Conduction Mode
EMF	Electromotive Force
MMF	Magnetomotive Force
DSP	Digital Signal Processor

Chapter 1

Introduction

This chapter introduces and explains the background of the thesis. It will also provide information about challenges and considerations taken into account in the thesis work. A project outline is also included.

1.1 Background & motivation

The demand on data traffic is rapidly increasing. This increase is fueled by the widespread of PCs, tablets and smart phones with easy access to 4G and 5G networks that offers more data traffic. Data centers use electrical energy to power server equipment, control and process data. The energy consumed in data centers today accounts for 4% of total consumed energy worldwide. In addition, the power that is lost in the processors and power supplies in form of heat requires more energy in order to cool down the data center. Most of this electrical energy is generated using fossil fuel with a high environmental impact. For example, in the last four years Googles power usage has went up 12 folds. Amazon, Facebook and Apple are growing in a similar pattern. In order to reduce the carbon dioxide footprint of its data centers, Google announced in 2016 they will buy 781 MW of renewable sources. Still this only makes up 37% of today's demand [1]. With the help of new power electronic devices, it is possible to increase the efficiency of power conversion within the data center reducing the power loss and thus the CO_2 footprint. New semiconductor materials like SiC and GaN enables efficiency and power density increase. While high efficiency means less power loss, or in other words lower operating costs, the high density contributes to reducing the size of the data center infrastructure resulting in a lower investment cost. Therefore, with the introduction of wide bandgap devices, telecom and data centers will have lower operating and initial costs. Moreover, the reduction in converter size means less material is used which means lower environmental impact as well as lower cost.

1.2 Problem description

In nonlinear loads, for example in switch mode power supplies (SMPS), the current drawn from the grid is distorted. This results in a poor power factor and a high total harmonic distortion (THD). A power factor correction (PFC) stage is commonly used to mitigate the negative effects of high THD on the grid. The PFC stage often comprises, in addition to switching devices, a magnetic element to store energy. With the advent of wide bandgap devices, the performance of the switching device is greatly improved. A reduction in conduction and switching losses is possible. Moreover, new topologies can be realized utilizing the capabilities of these new devices.

This master's thesis will examine the benefit of wide bandgap devices, especially GaN, and its impact on design and performance of a classic PFC boost converter. The main active PFC topologies is to be reviewed and briefly compared. The classic PFC boost converter is shown in fig. 1.1 and will be the main topology in this project. The foundation for designing a planar inductor will be outlined and explained and magnetic design considerations when designing a planar inductor will be presented. Furthermore, the role of different non-ideal effects and their impact on design will be investigated. A large part of this thesis will be optimization of a planar inductor used as a boost inductor in this classic PFC boost topology shown in fig. 1.1.

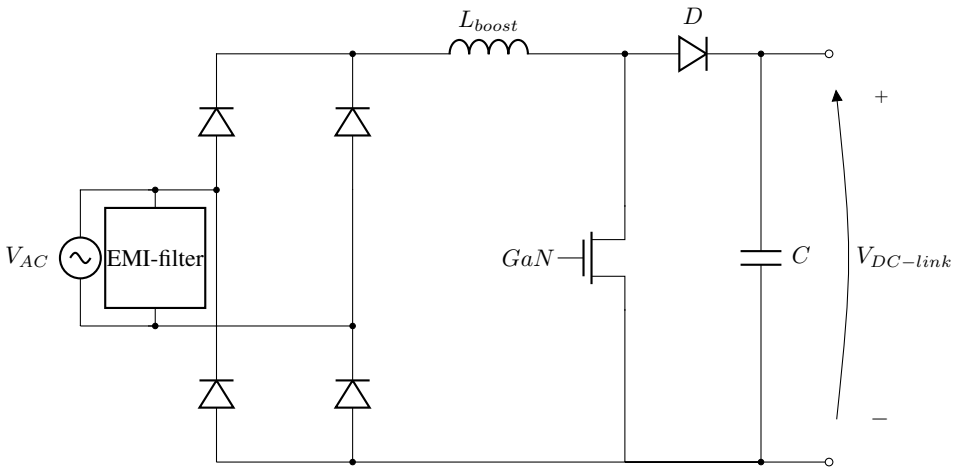


Figure 1.1: A PFC boost rectifier.

1.3 Project outline

The master's thesis will start with a presentation of wide bandgap semiconductors, especially GaN, its material properties and status in the market. Basic switching properties and electrical modeling of GaN-device will then be examined. The advantageous GaN-device characteristics lay the foundation for the rest of the master thesis, as it opens up new possibilities regarding the utilization of components in a converter. The project re-

port will present active power factor correction converters of interest, and a brief topology comparison will be conducted. Planar magnetic design will then be outlined, and relevant materials and geometries presented. Printed circuit board (PCB) design theory is then introduced, and different layouts/stackups are considered. Limitations in PCB manufacturing will also be a topic, as it lays the foundation for design considerations when designing a planar inductor. Following this, magnetic design considerations are outlined, and the basis of non-ideal magnetic and electric effects are presented. Relevant core materials for high frequency application are presented and reviewed. The finite element method (FEM) is central in this thesis, and this theory is presented in a separate chapter. The results and analysis part of this thesis is the largest and contains results from the simulations performed. In addition to presenting the results, this chapter also discusses and analyses section of the results.

Chapter 2

Theory & Literature Review

The theory presented in this chapter is a continuation of the theory presented in this thesis' associated specialization project. The parts that still are relevant for this master's thesis are taken from the specialization project. Basic knowledge of power electronic converters and semiconductors is a prerequisite for this theory.

2.1 Gallium Nitride - GaN

2.1.1 History of semiconductors

Silicon has been the dominant semiconductor material for almost 60 years. Its advantages over other earlier semiconductor materials such as germanium and selenium were low cost, reliability and its basic physical properties [2]. Cost and efficiency have been driving forces in the development of semiconductors. The first power MOSFET was introduced to the world in the late 1970s, with a breakdown voltage V_{BD} =100 V and an on-resistance R_{DS} =0.1 Ω , as an alternative to bipolar junction transistors. With a resistance of 0.1 Ω and a die size of 40 mm^2, it had a resistivity figure of merit of 4 Ωmm^2. Now, 40 years later, the figure of merit is about 60 times lower ($\approx$ 0.07 Ωmm^2) for a benchmark 100 V MOSFET. This figure of merit does of course not tell the full story, but it gives an idea of the magnitudes of improvement. In addition, IGBTs and super-junction devices have achieved conductivity improvements beyond the theoretical limits of a simple vertical majority-carrier MOSFET [2]. As silicon approached its limit both in terms of scaling and physical properties, wide bandgap devices started getting more and more of a realistic option as a substitute for silicon [3]. Among the wide bandgap materials of interest, silicon carbide (SiC) and gallium nitride (GaN) showed the best properties [2]. SiC was adopted for high-end applications in space and defense fields [3]. GaN was deemed an excellent next generation power semiconductor material in the mid 1990s [4]. Material parameters like bandgap and electron mobility was excellent for high power and high frequency application. In 2004, the first GaN high electron mobility transistor (HEMT) appeared. These were GaN-on-SiC substrates and primarily used in radio frequency (RF) application. In

2009, EPC introduced the first enhancement mode GaN (eGaN) grown on silicon. This offered similar properties as power MOSFETs, namely a ”normally-off” device. GaN fulfilled key requirements as controllability, reliability, efficiency and especially low cost. The low cost became possible by using standard silicon manufacturing technology and facilities [2].

2.1.2 Key power-switching requirements

In power electronics, there is a distinction between two-terminal and three-terminal devices. Two-terminal devices are mainly variations of diodes and three-terminal devices are controllable switches, typically transistors. Both two- and three-terminal devices share some desirable requirements such as high blocking voltage, low on-state resistance for given blocking voltage and high switching speed capabilities [5]. For transistors, it is also desired that the device operates in blocking state when no control voltage is applied. This feature is termed normally-off device, and as the name suggests, the devices are turned off when no control signal is applied and turns on with a positive voltage control signal. Figure 2.1 shows a simple silicon pn-junction diode and its drift region when forward and reverse biased.

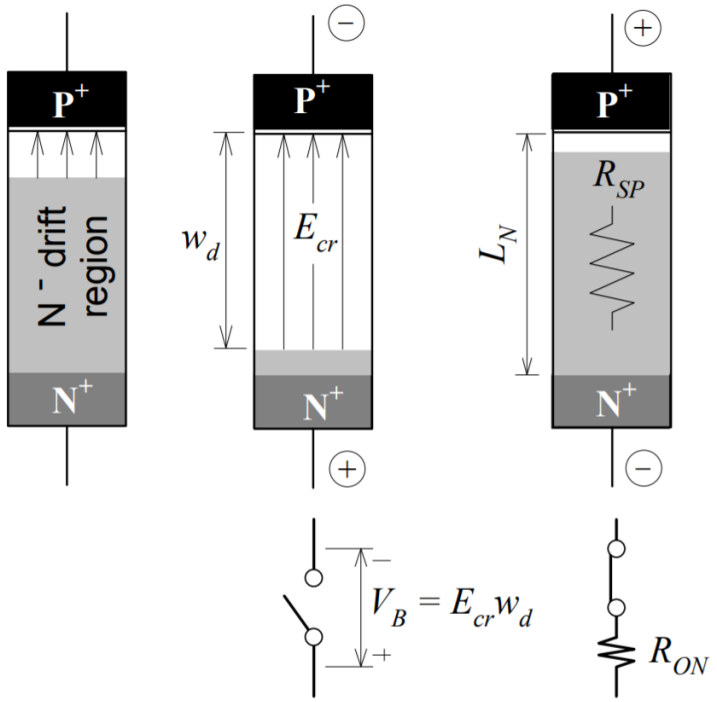


Figure 2.1: PN-junction with no, reverse and forward bias. Obtained from [5].

Blocking voltage V_B is given from eq. (2.1) with E_{cr} being the maximum electric field given by material properties, q the electron charge, N_D the doping of the drift region and

ε_s the permittivity of the material. It can be seen that it is only the doping which can alter the blocking voltage for silicon devices, as the other parameters are material given properties [5].

$$V_B = \frac{\varepsilon_s E_{cr}^2}{2qN_D} \tag{2.1}$$

$$L_N \approx w_d = \sqrt{\frac{2\varepsilon_s E_{cr}^2}{2qN_D}} \tag{2.2}$$

Equation (2.2) shows the approximate length of the drift region, given it's not significantly shorter than the depletion layer width, w_d. Defining the specific on-resistance of the drift region as on-resistance for a given area, the relationship between blocking voltage and specific on-resistance becomes [5]:

$$R_{on,sp} = \rho L_N = \frac{L_N}{q\mu_n N_D}$$

where L_N is the length of the N^--region shown in fig. 2.1. The specific on-state resistance then becomes:

$$R_{on,sp} = \frac{4V_B^2}{\varepsilon_s \mu_n E_{cr}^3} \tag{2.3}$$

Table 2.1: Material properties of Silicon, Gallium Nitride and Silicon Carbide (at room temperature), obtained from [2].

Parameter	Symbol	Unit	Si	GaN	SiC
Band Gap	E_g	eV	1.12	3.39	3.26
Critical Field	E_{crit}	MV/cm	0.23	3.3	2.2
Electron Mobility	μ_n	cm^2/Vs	1400	1500	950
Relative permittivity	ε_r	[-]	11.8	9	9.7
Thermal conductivity	λ	W/(cm·K)	1.5	1.3	3.8

From table 2.1 the tenfold increase in the critical field of wide-bandgap devices such as SiC and GaN is observed. This enables superior power switches with at least 10 times blocking voltage for same on-state resistance and physical size. SiC has additionally superior thermal conductivity over both Si and GaN. This enables better heat conduction away from the power switch, which is very desirable [5]. GaN shows the highest critical field and electron mobility among the three semiconductor materials.

2.1.3 Wide bandgap

Wide bandgap (WBG) is a term used to characterize semiconductor materials and refers to the energy required for an electron to jump from the valence band to the conduction band. Bandgap is measured in electron volts and is the difference in energy from the top of the valence band to the bottom of the conduction band. A typical lower limit for wide

bandgap semiconductors is 2 eV. A direct consequence of the wider bandgap is lower intrinsic leakage current and higher operating temperatures [2].

2.1.4 Critical field

The wide bandgap is caused by strong chemical bonds. This also leads to a higher critical field required to cause electron avalanche and thus breakdown. The breakdown voltage of a device is in fact directly proportional to the critical field and the width of the drift region, as shown in fig. 2.1. Hence, with the WBG semiconductors having approximately 10 times the critical field of silicon, the drift region can be about 10 times smaller in a WBG semiconductor. From another perspective, with eq. (2.3) in mind, this massively impacts the theoretical on-state resistance of the device. In order to support the increased electric field, there need to be carriers in the drift region that are depleted away at the point where the device reaches the critical field [2].

$$q \cdot N_D = \varepsilon_0 \cdot \varepsilon_r \cdot \frac{E_{cr}}{w_d} \tag{2.4}$$

Equation (2.4) is a variation of Poisson's equation where q is, as before, electron charge and N_D the total number of electrons in the volume (assuming N-type semiconductor). This equation can help understand the huge advantage with high critical fields. The breakdown voltage is assumed proportional with the width of the drift region. An increase of critical field strength of 10 times (illustrative number, real number in table 2.1), and the electrical terminals 10 times closer, the number of electrons can be 100 times greater [2].

2.1.5 Electron mobility

The theoretical on-resistance of a semiconductor is inversely proportional to the electron mobility, μ_n, as shown in eq. (2.3). This means that larger electron mobility gives a lower on-state resistance. Conductivity can be modeled as electron or carrier density multiplied with the mobility.

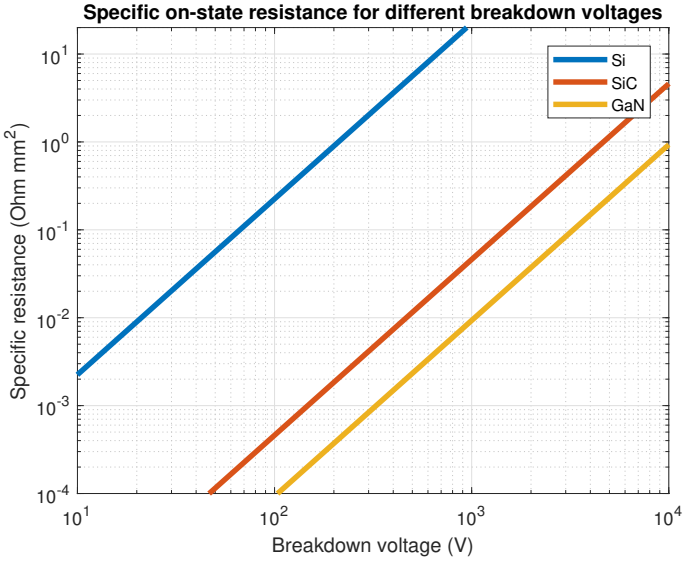


Figure 2.2: Specific on-state resistance for different breakdown voltages, calculated and plotted using eq. (2.3) and values from table 2.1.

Figure 2.2 is a logarithmic plot of the theoretical specific on-state resistance for Si, SiC and GaN versus the breakdown voltage. It is plotted using values obtained from table 2.1 and the formula in eq. (2.3). From the figure, it can be seen that theoretical limits for both GaN and SiC go way beyond Si, meaning a much lower on-state resistance is obtainable (per chip area).

2.1.6 GaN structure

High electron mobility transistors (HEMT) are field effect transistors (FETs) which utilize two materials with different bandgaps to form a heterojunction as opposed to the more conventional way of doping two regions and form a PN-junction. HEMTs are enabled by the electron channel formed at the heterojunction between *undoped* GaN and AlGaN [5], shown in fig. 2.3.

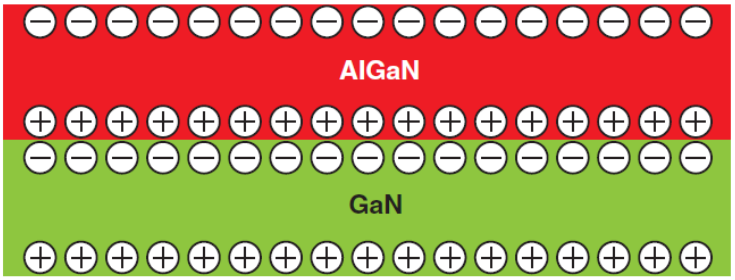


Figure 2.3: Heterojunction formed between undoped GaN and AlGaN, obtained from [2].

The fixed polarization charge attracts the electrons to create a channel. This channel is referred to as a two-dimensional electron gas (2DEG). This term indicates that the electrons virtually are restricted to movement in two dimensions, meaning an ultrathin layer of electrons [5]. The ability to form this ultrathin, highly conductive channel, without the use of any extrinsic dopants or applied electric field is one of the more unique properties of GaN, and it sets GaN apart from most other semiconductors [3]. This formation with no extrinsic dopants is also possible with for instance gallium arsenide (GaAs) and aluminum gallium arsenide (AlGaAs), but the formation with GaN is regarded of greater interest due to its superior characteristics. The crystal structure of GaN leads to piezoelectric properties. This is central in the ability of high conductivity in GaN. Piezoelectricity is the ability of GaN to accumulate charge when applying mechanical stress to it. An electric field will be caused by the displacement of charged elements in the crystal lattice [2], and more strain causes a greater electric field. This will be further regarded when recessed gate e-mode transistor is presented later in this section. A big and important difference between the wide bandgap GaN and SiC devices is that GaN is usually grown on other substrates, such as sapphire and also on SiC/Si wafers. When grown on SiC, GaN components becomes more expensive than SiC components themselves, and this is therefore not frequently used. GaN grown on Si substrate is a much more low cost solution [6].

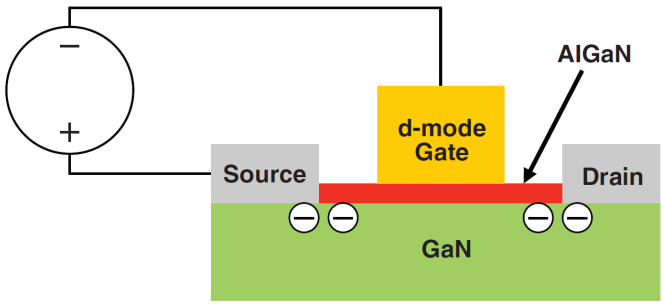


Figure 2.4: Depletion mode HEMT, obtained from [2].

In fig. 2.4 a depletion mode HEMT with a negative voltage applied to the gate is shown. When no voltage is applied, it can be seen that the source and drain electrodes are in contact with the 2DEG. This short circuits the terminals source and drain, until the ”pool” of electrons is depleted. The negative voltage applied as in fig. 2.4 depletes the electrons in the 2DEG out of the device, which makes the basis of a depletion mode, normally-on, (d-mode) HEMT. As presented in section 2.1.2, this is an undesirable feature of a transistor. Depletion mode HEMT is equivalent to a normally-on device. If a converter were to start up without a negative bias applied to the gates of the d-mode HEMTs, short-circuit would occur. It is therefore more interesting to look at what is called an enhancement mode GaN-device, a normally-off device. There are four popular structures that enable enhancement mode. These are: *cascode hybrid, pGaN gate, recessed gate* and *implanted gate* [2].

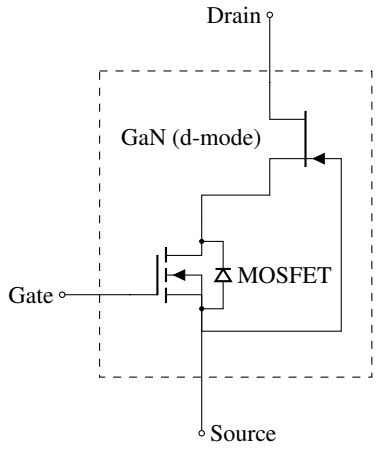


Figure 2.5: Cascode hybrid enhancement-mode structure. Low voltage e-mode Si MOSFET and d-mode GaN HEMT.

Figure 2.5 shows a *hybrid cascode enhancement-mode GaN transistor*. It consists of an enhancement-mode (low voltage) Si MOSFET in series with a depletion-mode GaN transistor. With a positive voltage on the main gate, the MOSFET is turned on. The gate-source voltage of the GaN-device then becomes near zero (as the MOSFET is on), which means the GaN-device device is on. Current can now flow from the main drain to the main source. With no voltage at the MOSFET gate, it is turned off, and there will build up a negative voltage between the GaN transistor gate and source. This will turn the device off, and no current can flow between the main drain and source. For the hybrid cascode transistor to work, the on-state resistance of the GaN transistor should be much higher than the MOSFET. Cascode solutions are therefore most effective for high voltage GaN HEMT.

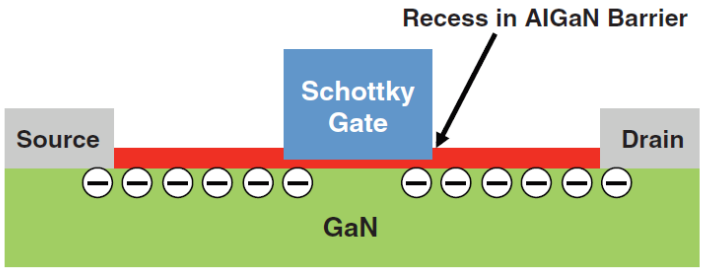


Figure 2.6: Recessed gate e-mode HEMT, obtained from [2].

Recessed gate e-mode is created by thinning the AlGaN barrier layer above the 2DEG structure [7]. The voltage generated by piezoelectric fields will be reduced proportionally with the reduction in AlGaN-thickness [8]. By utilizing a Schottky metal gate, with a built-in electric potential larger then the piezoelectric voltage generated, the 2DEG is eliminated when zero voltage is applied on the gate. This is shown in fig. 2.6.

Implanted gate e-mode utilizes implantation of fluorine atoms in the AlGaN layer. This causes negative charge in the AlGaN-layer, which in turn depletes the 2DEG-channel. The e-mode structure is completed by adding a Schottky gate.

The last of the four popular e-mode structures is the *pGaN gate e-mode* structure. This works with the same philosophy as recessed gate e-mode. The goal is to deplete the 2DEG-channel by additional electric potential larger than the piezoelectric voltage generated. In pGaN gate e-mode structures, this is achieved by adding a layer of positive charges (pGaN-layer) with a built-in voltage that exceeds the piezoelectric effect. Based on fig. 2.6, the Schottky gate of the recessed gate e-mode is replaced with a pGaN and a metal layer to achieve enhancement mode.

2.1.7 Reverse conduction in GaN transistors

So far, only a positive current from drain to source has been regarded. With e-mode GaN transistors, however, the current can also flow in the opposite direction. This is possible provided the gate-drain voltage is higher than the threshold voltage (described in section 2.1.8). Advantages of eHEMT are that they are unipolar, no doping is required, and that no minority carrier conduction is present. A result of the last advantage is that when the gate voltage is removed, the device will turn off instantly [9]. This is a powerful advantage, as reverse recovery losses are eliminated. For hybrid cascode devices, this is however not the case. When the device conducts in the reverse direction, there will be a voltage drop through the body-diode of the Si MOSFET, creating a positive gate-source voltage in the GaN dHEMT. This dHEMT will then be turned on, and the on-resistance will be added to the voltage drop in the MOSFET body diode [2]. Due to the injection of minority carriers in the body diode of the silicon-based MOSFET, the cascode configuration will have a recovery time, giving rise to recovery losses [10].

2.1.8 Capacitance model and switching characteristics

The capacitance model of a transistor tells something about how fast the transistor is able to switch. Figure 2.7 shows the physical origin of the parasitic capacitances. The three main parasitic capacitances for an enhancement mode GaN-FET are all the same as for a MOSFET [2]. These capacitances are gate-source, C_{gs}, gate-drain, C_{gd} and the drain-source capacitance, C_{ds} [11].

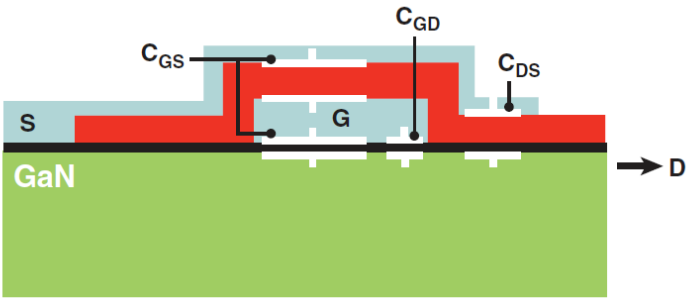


Figure 2.7: The physical origin of the parasitic capacitances, obtained from [2].

The electrical equivalent is shown in fig. 2.8. The capacitance given in a datasheet is often the capacitances seen at a terminal. It is therefore normal to define three other capacitances, namely C_{ISS}, C_{OSS} and C_{RSS}. These are defined in table 2.2.

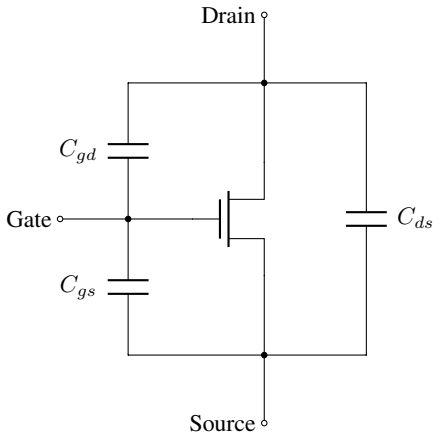


Figure 2.8: Capacitance model of GaN-FET.

Table 2.2: Capacitance definitions.

Symbol	Expression	Meaning
C_{iss}	C_{gs}+C_{gd}	Input capacitance
C_{oss}	C_{ds}+C_{gd}	Output capacitance
C_{rss}	C_{gd}	Feedback capacitance

The capacitances C_{ISS}, C_{OSS} and C_{RSS} are not constant, but voltage-dependent [11]. This is due to the capacitance contribution from the depletion layers. The depletion layers will increase and decrease with varying voltage, making the capacitances vary. The capacitance values determines the switching speed, and thus the energy lost in each switching transition.

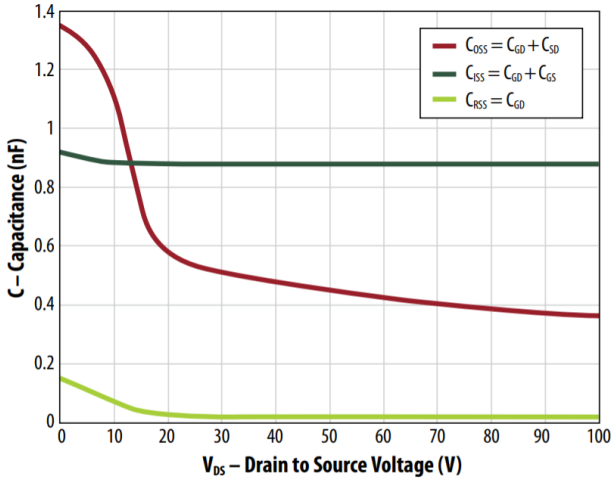


Figure 2.9: Different terminal capacitances for a EPC2001 eGaN FET, obtained from the datasheet [12].

To be able to calculate the switching waveforms, an idealization is often done. This is depicted in fig. 2.10. When approximating C_{gd} with two values, as in this figure, the change between C_{gd1} and C_{gd2} occurs when the gate-source voltage equals the drain-source voltage. At this drain-source voltage the FET is either entering or leaving the ohmic area [11]. C_{gs} and C_{ds} is in this idealization assumed constant and equal the final value.

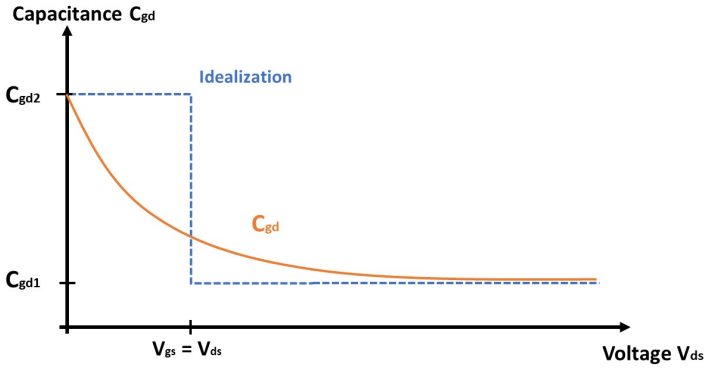


Figure 2.10: Idealization of capacitance, recreated figure from [11].

It can be convenient to consider the amount of charge necessary to change the gate-source voltage. Integration over time of the gate current equals the gate charge. Figure 2.11 shows the gate-source voltage versus the gate charge of a real eGaN FET. The gate charge, Q_G, is obtained by integrating C_{ISS} from the starting gate-source voltage to the end. The connection between charge and how fast a device is, can be illustrated by a simplified example. Imagine 4 V gate-source voltage is desirable, as this hypothetically ensures the device to always stay on. To achieve this, it can be seen from the graph that about 7 nC of charge is needed. If the gate driving circuit can supply a current of 1 A, it would take about 7 ns to achieve 4 V gate-source [13].

As for capacitances, charges Q_{gd} and Q_{gs} are also often specified separately as they impact switching speeds. The ratio $\frac{Q_{gd}}{Q_{gs}}$ is an interesting number and is called the Miller ratio [2]. This ratio is important when considering unintentional turn-on (Miller turn-on) and the determination of dv/dt-immunity [14] [15], but as this is outside the scope of this specialization project, it will not be considered further.

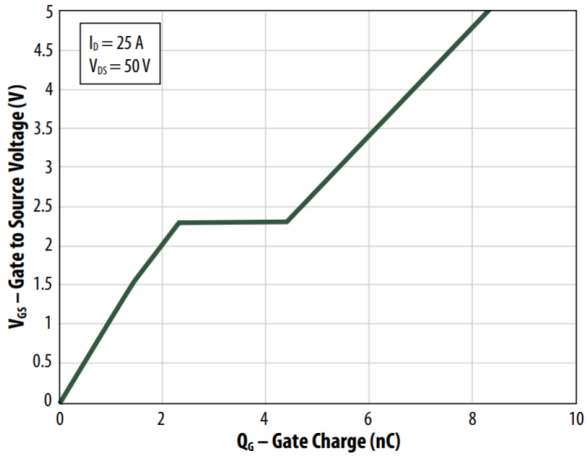


Figure 2.11: V_{gs} vs. gate charge for a EPC2001 eGaN FET, obtained from the datasheet [12].

To turn a device on, a voltage of at least the threshold voltage, V_{th}, between the gate and source terminals must be applied. The enhancement mode devices, including cascode, have positive threshold voltages, and depletion mode devices have negative threshold voltages and will turn off when it is applied. The threshold voltage in a GaN HEMT is relatively unaffected by temperature, as the strain in the AlGaN remains constant with temperature [16]. This is however not the case for cascode devices, as it will decline due to the decline in threshold voltage of the low-voltage Si MOSFET [2]. Physically, in GaN power devices, the threshold voltage is when the 2DEG is fully depleted by the voltage applied on the gate [17]. As previously mentioned, some enhancement-mode devices have a built-in voltage due to the gate metallurgy (Schottky, pGaN), and the threshold voltage at the gate is simply the additional voltage needed on the gate.

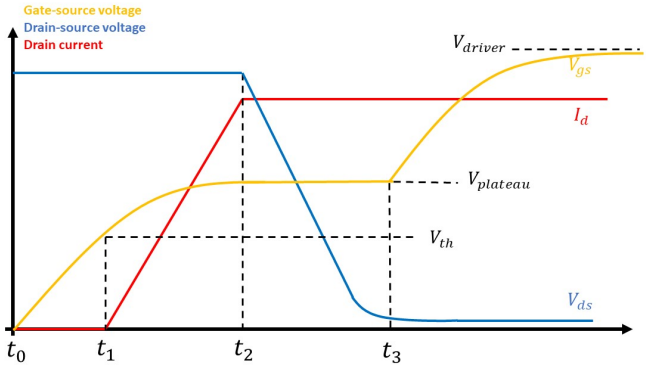


Figure 2.12: Switching characteristics during turn-on.

Figure 2.12 shows a typically idealized switching characteristic of a turn-on process. The load is assumed clamped inductive, behaving like a current source [18]. Switching characteristics are based on pages 583-587 in [11]. Gate voltage is assumed applied at t_0. During the first time-step to t_1, a current flows in the two capacitances C_{gs} and C_{gd}, and charges these. As the threshold voltage is reached, at the time instant t_1, current begins to flow from the drain to the source. The drain-source voltage remains while the drain current builds up to reach the load current. As this drain current is achieved, the gate current flows through C_{gd} and the gate-source voltage is temporarily clamped at $V_{plateau}$. This occurs at time t_2 and causes the drain-source voltage to decrease. As it has dropped to its final value, namely the voltage drop $V_{ds,on}$ caused by the on-state resistance, the gate-source voltage becomes unclamped and approaches the gate driving voltage. This happens at time t_3 in illustrated fig. 2.12 [19].

2.1.9 Challenges with GaN

The following challenges with GaN are widely based on the topical review study ”The 2018 GaN power electronics roadmap” [20].

The strong desire for normally-off devices due to safety reasons (short circuit issue as presented in section 2.1.6) presents manufacturing issues for GaN. GaN transistors in its most simple state are ”inherently” normally-on devices, and even if there are solutions to make normally-off devices, as presented in section 2.1.6, reliability can be an issue.

Dynamic on-resistance is another issue. Some GaN transistors show a dynamic and higher resistance immediately after turn-on, before it decays to the static value. The physical phenomenon charge trapping, known as a current collapse, leads to increased resistance in the HEMT channel [21]. The practical consequence of this is losses that are not accounted for in the design stage.

Even if the GaN transistor does not have an intrinsic body diode, current can flow in the reverse direction. However, the source-drain voltage drop v_{sd} increases with decreasing gate-source voltage v_{gs}.

Parasitic inductances and capacitances and their influence are similar to that of Si and SiC. However, GaN has a narrow gate voltage margin compared to its competing semiconductors, which can affect the reliability and cause short circuits and device destruction. In general, electromagnetic interference can become a bigger problem as higher switching frequencies and higher power densities is a reality.

2.2 Power Factor Correction Converters

A power factor correction converter is, as the name suggests, a converter which improves the power factor compared to a conventional converter. As mentioned in the introduction, the current drawn from the grid by nonlinear loads suffers from harmonic distortion and poor power factor. The power factor is defined as the ratio between the real power (P) and the apparent power (S). If both currents and voltages are purely sinusoidal, the power factor is simply a matter of phase shift between voltage and current. This is however rarely the case, as most power supplies draws non-sinusoidal currents [22]. The power factor then consists of two factors, namely the displacement factor related to phase shift and a distortion factor describing the current shape. Total current harmonics distortion and power factor are calculated as follows

$$THD_i = \sqrt{\sum_{h \neq 1} \left(\frac{I_{sh}}{I_{s1}} \right)^2} \tag{2.5}$$

where I_{sh} is the rms-current of the h'th harmonic frequency ($f_h = hf_1$)

$$PF = \frac{1}{\sqrt{1 + THD_i^2}} \cdot DPF \tag{2.6}$$

where the displacement power factor, DPF is

$$DPF = cos\phi_1$$

and ϕ_1 is the displacement angle of the first harmonic.

A *passive* PFC converter utilizes passive elements such as inductors and capacitors to improve the waveform of the current drawn from the utility grid. The simplest approach is to work on the AC-side of the rectifier bridge and add an inductor. This can be seen as a higher effective AC-side inductance, which improves the power factor [11]. A more complicated network of capacitors and inductors is also possible, but will not be considered further in this thesis.

Active PFC converters take advantage of active elements such as transistors to actively improve the power factor [11]. To actively improve the power factor, the current must be shaped, and a very common topology to do this is the PFC boost converter. This converter makes use of a boost (step-up dc/dc) converter in combination with a rectifying bridge to shape the input current. The topology is illustrated in the introduction in fig. 1.1.

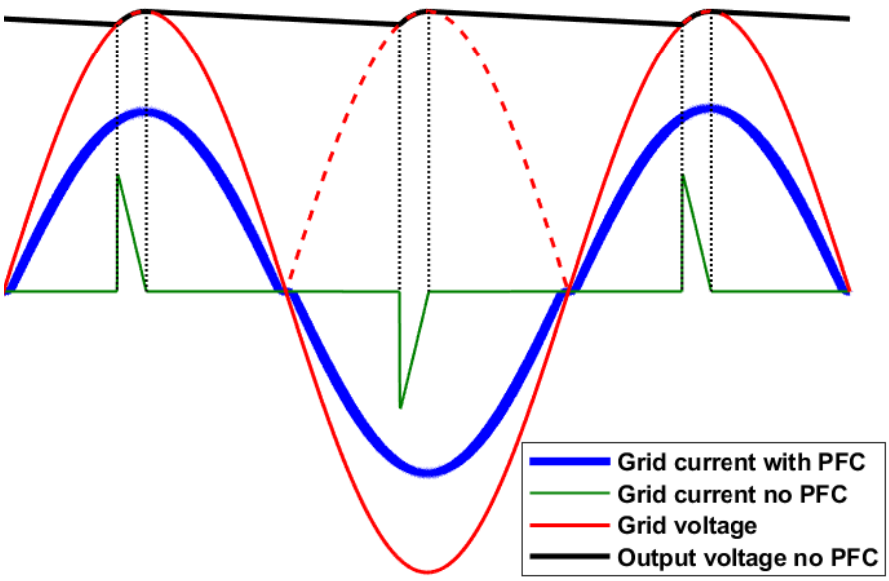


Figure 2.13: Grid voltage and currents with and without a PFC converter.

Figure 2.13 shows the grid voltage and current of a PFC converter compared to the grid current without PFC. The waveforms are for illustrative purposes, and thus no axes are included. The cases with and without PFC both draw the same amount of power, but the current graphs are scaled differently. The grid current for the case with PFC is for instance scaled up with a large scaling factor to make it more visible that the current is not a pure sinusoidal shape, but in fact it is more like a triangular wave of high frequency with a sine reference. The signal is also showed in fig. 2.14, and in this figure it the switching waveform is more visible. The PFC topology is a simple PFC boost as presented in fig. 1.1 and implemented using Simulink. The Simulink model is included in appendix C. The example without PFC is the same Simulink model, but stripped for boost inductor, transistor, and forward diode. It is seen that the grid current when there is no PFC is formed as spikes. These spikes occur when the grid voltage becomes higher than the output voltage, which is kept relatively constant by the output capacitor. With fig. 1.1 in mind, the current can during this period actually flow through the rectifying bridge. During this period, the DC-link capacitor gets charged, and the load is also supplied directly from the grid. When the capacitor is charged and the grid voltage instantaneous value starts to decline from its peak, the rectifying bridge gets reverse biased, and no current can flow from the grid once again.

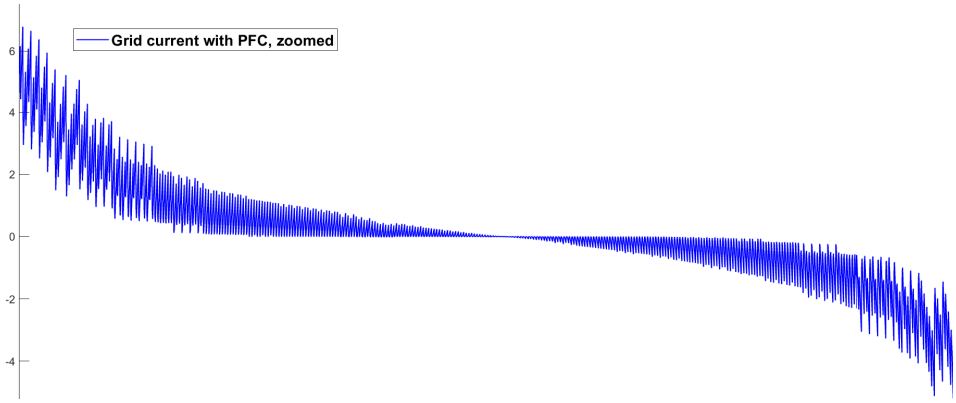


Figure 2.14: Grid current at and around zero-crossing for case with PFC converter.

Table 2.3: Total harmonic distortion and power factor with and without PFC.

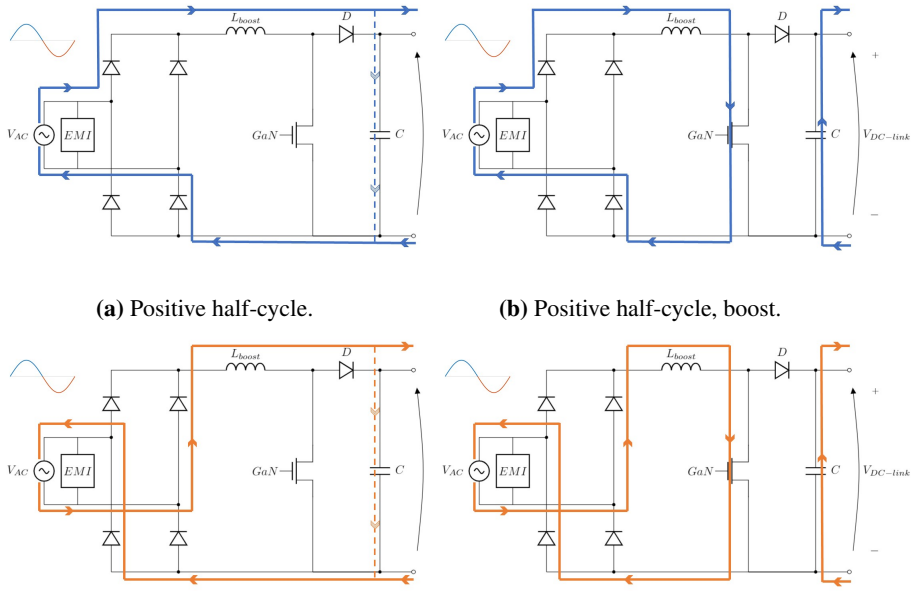
Quantity	With PFC	Without PFC
Current THD	14.45%	167%
Power factor from grid	0.9897	0.5149

Both the results in figs. 2.13 and 2.14 and table 2.3 are for illustrative purposes, and obtained using the Simulink model described in appendix C. The poor power factor is mainly caused by the harmonic distortion in the current, and not because of the displacement in the fundamental harmonic. The distortion in the current with no PFC can easily be seen in fig. 2.13. The current is in phase with the voltage, meaning the DPF is close to unity, but the current does not have a sine wave shape. This is reflected through the high current THD and the total PF. It must be emphasized that the values in table 2.3 are strongly dependent on control structure and passive elements etc., but it illustrates why power factor correction is important. When the grid voltage is close to zero, the boost converter struggles to supply the DC-link voltage, as the transistor operates with a duty cycle close to unity to strive for the high gain. This is illustrated around the zero-crossings in fig. 2.13, and the zoomed in version in fig. 2.14. The control system in the Simulink model which produced these figures is simplified and does not allow the current to enter DCM around zero-crossings, even if this is a common control philosophy [23] [24]. The zero-crossing-problem will be a repeating subject in this thesis, also when presenting design criteria for a planar inductor in section 4.3. For a closer look at the control system, control structures, control philosophy etc. of the PFC boost converter, the ELK21-report attached in appendix F covers this.

2.2.1 Classic boost PFC

The classic boost PFC consists of a diode rectifying bridge, followed by a boost converter as shown in fig. 1.1. The step-up conversion ensures that the DC-link voltage always is

greater than the input voltage. An active PFC can also be achieved by using a buck or a buck-boost stage instead of the more popular boost stage [25]. Both these have drawbacks, however. Buck converters always steps-down the voltage, forcing the DC-link voltage to be lower than the lowest AC input voltage. For buck-boost, the drawback is higher switching voltage stress [26] [11].



(a) Positive half-cycle.

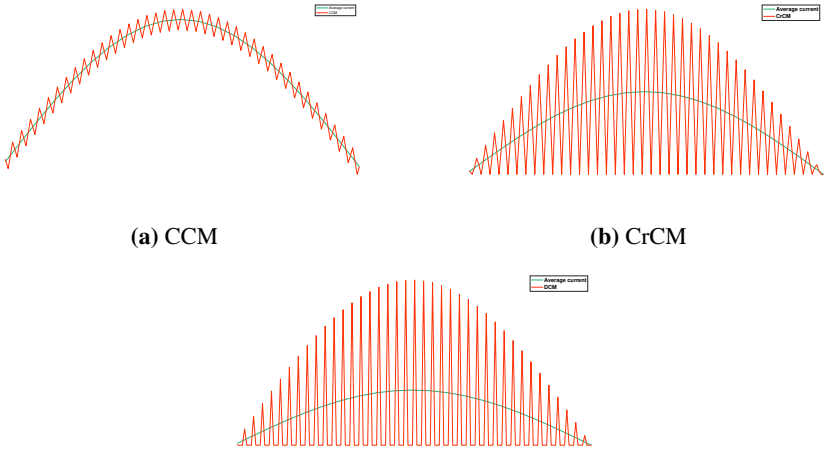
(b) Positive half-cycle, boost.

(c) Negative half-cycle.

(d) Negative half-cycle, boost.

Figure 2.15: Current flow of a classic PFC boost converter.

Figure 2.15 shows the flow of current during one period of the AC-input. The working principle of the converter is as for a step-up converter (p.172-178 in [11]). The only difference is the input voltage is not a pure DC-quantity, but a rectified sine. When the switch is closed, current flows through it, and the current from the grid builds up according to the voltage over the inductor and the inductance. The load current is supplied by the capacitor. As the switch is open, the current flows through the diode and supplies the load and charges the capacitor. There are three operational modes for the boost converter to operate in. These are: continuous conduction mode (CCM), critical conduction mode (CrCM) and discontinuous conduction mode (DCM). The difference between these is illustrated in fig. 2.16. In CCM, the input current, and thus the inductor current only becomes zero around the point when the sinusoidal voltage crosses zero. CrCM becomes zero at each switching cycle, just for an instant, while DCM becomes and stays zero for a while each switching cycle. CCM draws the lowest peak current from the grid, but it also needs a larger boost inductor to shape the current. CrCM and DCM can allow smaller boost inductors but draws high peak currents at the same power ratings as for CCM.



(a) CCM

(b) CrCM

(c) DCM

Figure 2.16: The fundamental operational modes of a PFC boost converter. The green graph is the average current and is equal in all three operation modes.

Control strategies are different for the different operational modes. There are two control objectives in a PFC boost converter. The output voltage should be regulated to a constant value for varying input voltage, and the input current should be shaped to improve THD and thus the power factor. The actuator in the system is the gate of the transistor, and in principle, the duty cycle and the switching frequency can be varied [27]. Control schemes such as peak current control and average current control are based on a constant switching frequency and varying duty cycle. With hysteresis control, on the other hand, the switching frequency is variable. Hysteresis control in a PFC boost converter is often referred to as bang-bang control, as there is an upper and lower limit at which determines turn on or turn off. The zero-crossing can often create problem for the PFC boost circuit. When the voltage is near zero (twice per period), the boost ratio is given by the duty cycle (p.173 [11]) needs to be very large, which is practically difficult [28]. The zero-crossing issue is depicted in a way in figs. 2.13 and 2.14. It can be seen that the current waveform is not very sinusoidal during zero-crossings. A solution is to allow discontinuous current at each zero-crossing, while running continuous current mode the rest of the half-period. Other solutions to this problem are presented in the literature [27], [24].

One of the problems with the PFC boost converter is the forward voltage drop, and thus conduction loss of the diodes. At every time instant, the current flows through at least two diodes, three when not boosting. This gives a large forward voltage drop. When not boosting, there is still some small conduction losses through the GaN HEMT. These conduction losses set a limit for the efficiency of the PFC boost converter, and when pursuing higher efficiency, other topologies have become popular. In the pursuit of efficiency, bridgeless PFC topologies are of high interest, as it limits the forward voltage drop problem [29]. The term bridgeless simply refers to a lack of diode rectifying bridge.

2.2.2 Bridgeless totem-pole PFC

The bridgeless totem-pole PFC converter is shown in fig. 2.17. The principle of a totem-pole PFC converter is that it has one fast switching leg (illustrated with GaN in fig. 2.17) and one slow switching leg (illustrated with SJ). The super junction MOSFETs in the slow switching leg could in principle just be diodes, but to limit the forward voltage drop, MOSFETs with low on-resistance can be used [30]. The converter looks like a full-bridge converter, but is controlled to operate like a totem-pole converter with diodes on the slow switching leg [31]. The term totem-pole refers to the positioning of the fast switches and "slow" switches (optionally: diodes). They are respectively positioned on the same leg, on top of each other, like a totem-pole.

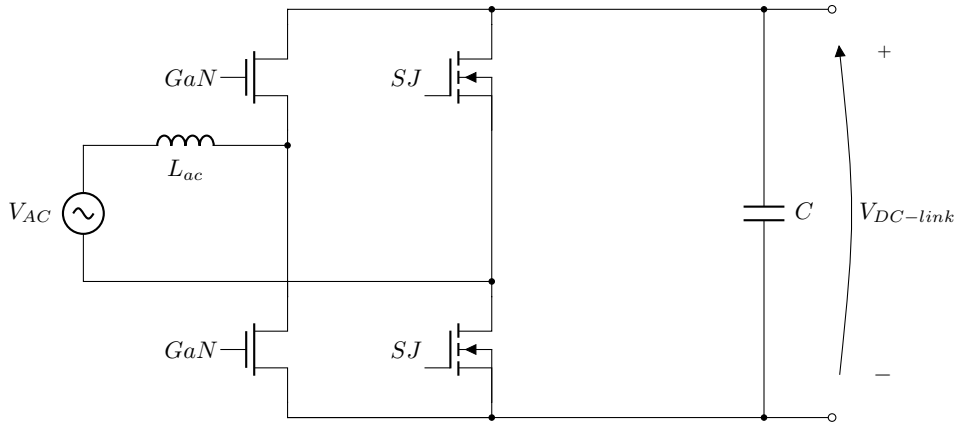
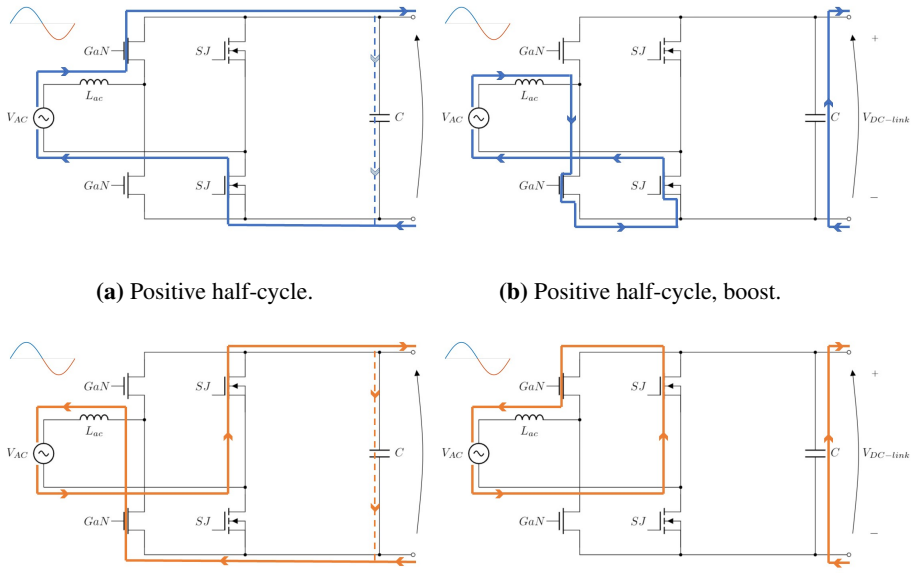


Figure 2.17: A bridgeless totem-pole PFC converter.

The current flow during the positive and negative half-cycle of one period is shown in fig. 2.18. During the positive half-cycle, the lower GaN-switch acts as an active boost switch, switching on and off to boost the inductor current. The upper GaN-switch free-wheels the inductor current and discharges the inductor energy when not boosting. In the negative half-cycle, the roles are reversed for the upper and lower switch, and they act like boost and freewheel respectively. The super-junction MOSFETs handles the synchronized line rectification at input line frequency and does, as previously mentioned, in principle work as a diode. Large reverse recovery problems of existing silicon MOSFETs makes the CCM operation of the bridgeless totem-pole impractical and reduces efficiency [30]. The low reverse recovery charge in GaN HEMT, however, makes this topology practical, and among the bridgeless topologies, bridgeless totem-pole PFC has shown the highest efficiency ([29], [32]).



(a) Positive half-cycle.

(b) Positive half-cycle, boost.

(c) Negative half-cycle.

(d) Negative half-cycle, boost.

Figure 2.18: Current flow of a bridgeless totem-pole PFC converter.

The bridgeless totem-pole does suffer from a similar problem as the PFC boost, namely the zero-crossing. When the converter transitions from the positive to negative half-cycle, the duty ratio of the lower GaN-switch changes abruptly from 1 to 0, and oppositely from 0 to 1 for the upper GaN-switch. The relatively slow reverse recovery of the body-diode on the MOSFETs prevents the voltage at the slow switching leg to jump to the DC-link voltage instantly. This leads to a current spike [30]. To avoid this current spike, there is a need for soft-start each zero-crossing, meaning a gentle reversing of the duty-cycle. Paper [30] proposes only a few switching cycles is enough to handle the problem. Reverse recovery losses make CCM virtually impossible for MOSFETs in the fast switching leg. GaN not only eliminates the reverse recovery issue, but also has very low switching losses [32]. Hard-switching in a totem-pole PFC limits the switching frequency, as the turn-on losses still dominate total power losses in a hard-switched totem-pole. This, in turn, limits the power density, as other passive elements such as filters and inductor still will be large in volume due to its frequency dependency [2]. The only way to maintain high efficiency and reduce the power density will be to implement soft-switching, as this can increase switching frequency without reducing efficiency. Implementation of control circuitry is more complex than for instance the classic PFC boost, which is a drawback for the totem-pole PFC. Inrush current is not regarded here, but is usually handled by pre-charging the capacitors with bypass-diodes.

2.2.3 Dual boost bridgeless PFC

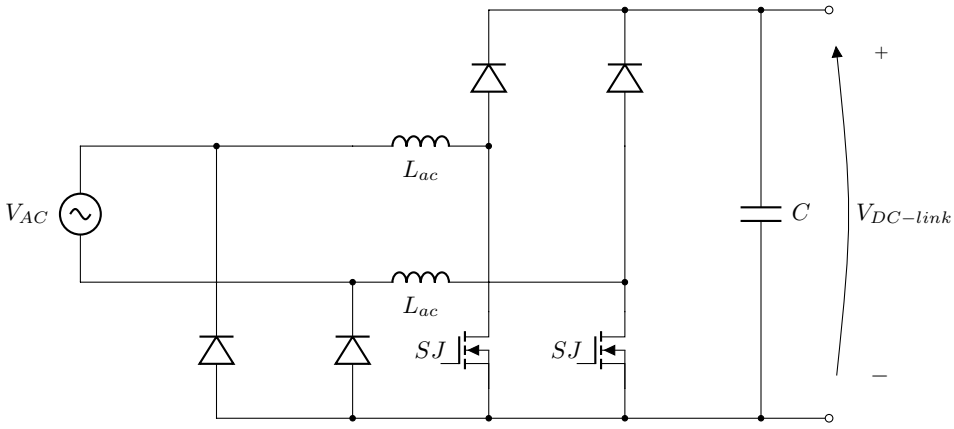
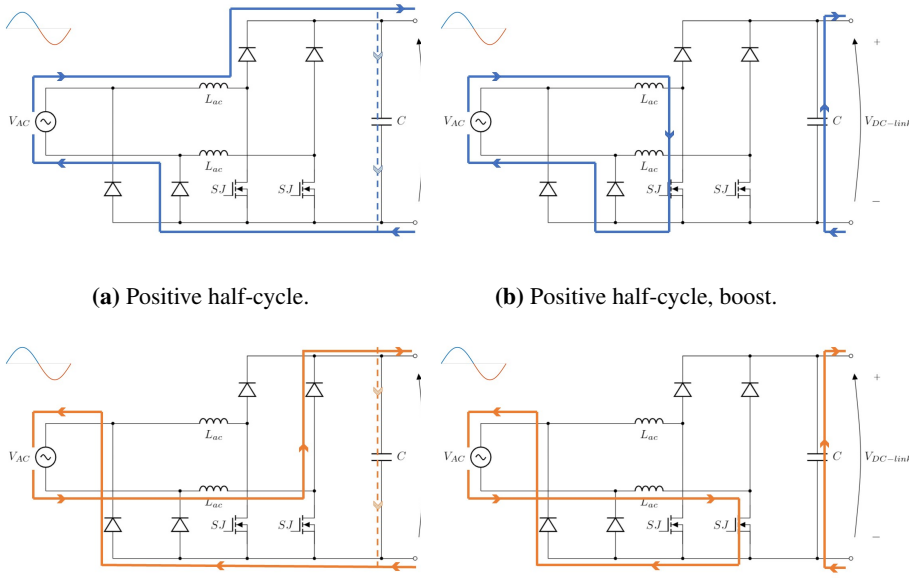


Figure 2.19: A dual boost bridgeless PFC converter.

The dual boost bridgeless PFC is an improvement of the boost bridgeless PFC, which only has one inductor, two diodes, and two MOSFETs. The dual boost brigdeless circuit can be seen as two dc/dc boost circuits, one for each half-cycle [33]. The flow of current for the dual boost circuit for positive and negative half-cycle is shown in fig. 2.20. Both the power transistors in the circuit, shown with SJ in fig. 2.19, can be driven with the same control signal. This does simplify the control circuit of this converter, and is especially an advantage as opposed to the totem-pole structure. A drawback of the dual boost bridgeless PFC is however that two inductors are needed. This is added cost and volume to the converter, but it comes with the advantage of better thermal performance. Low utilization of the inductors and other components lowers the power density. The efficiency improvement of the dual boost bridgeless PFC over the classic boost PFC is limited by the on-state resistance of the boost switches [34]. Even if the switches in the figs. 2.19 and 2.20 are illustrated with superjunction MOSFETs, GaN HEMTs are very interesting with its high electron mobility [35]. Since the lower diodes in fig. 2.19 directly connects the grid to the DC-side, the common mode (CM) noise is low [32].



(a) Positive half-cycle.

(b) Positive half-cycle, boost.

(c) Negative half-cycle.

(d) Negative half-cycle, boost.

Figure 2.20: Current flow of a dual boost bridgeless PFC converter.

2.2.4 Topology summary

The three topologies: classic boost PFC, dual boost bridgeless PFC, and bridgeless totem-pole PFC has now been briefly introduced. Summarized characteristics are shown in table 2.4. The main issue with the classic PFC boost is the forward voltage drop of the diode rectifying bridge, in which two diodes always conduct, plus either the boost diode or boost switch. It also has the zero-crossing issue. Its main advantage is the simple operation and control structure. Bridgeless solutions like the dual boost and totem-pole PFC have lower conduction losses due to fewer semiconductors in the conduction path. [34] shows a significant improvement of efficiency with dual boost bridgeless PFC over classic boost PFC, both for CCM and DCM. Totem-pole PFC has a complex control structure, but with GaN HEMTs, it shows the highest possible efficiency of the reviewed topologies [29]. Implementation of soft-switching in totem-pole PFCs can greatly increase the power density while maintaining very high efficiency. This argument only holds for GaN transistors in the fast switching leg due to the lack of reverse recovery. Cost is however also an aspect to consider, and as multiple papers suggest ([32], [34], [29]), even if the theoretical efficiency of the totem-pole PFC is the highest, the cost is also so. The bridgeless dual boost PFC also has a higher cost of materials compared to the classic boost PFC, as the classic boost only have one transistor and one inductor. Studies ([20], [36]) suggests cost reduction in GaN-on-substrate production is highly probable, and advances within bulk GaN production is realistic. Major investments are being made by industrial companies in a wide variety of markets to optimize system advantages offered by GaN transistors [20].

Table 2.4: Topology review.

Attribute	Classic boost PFC	Dual boost bridgeless PFC	Bridgeless totem-pole PFC
Semicond. in cond. path	3	2	2
Diodes	5	4	0
Transistors	1	2	4
Total semicond. comp.	6	6	4
Magnetic components	1	2	1

2.3 Inductor

2.3.1 Inductance

Inductance is the electrical property which describes the electromotive force (EMF) induced by a change in the electrical current through an electrical conductor. The change in the current makes the B-field and thus the flux in the inductor change. This flux change due to the current change defines the self-inductance of a conductor. The mutual inductance is the induced EMF in an electrical conductor caused by the change in current of another conductor. Ampere's law, given in eq. (2.7), is the basis when calculating inductance of a winding with a magnetic core.

$$\oint_C \mathbf{H} \cdot d\mathbf{l} = I_{f,enc} \tag{2.7}$$

which for most practical magnetic circuits can be rewritten as

$$\sum_k H_k l_k = \sum_m N_m i_m$$

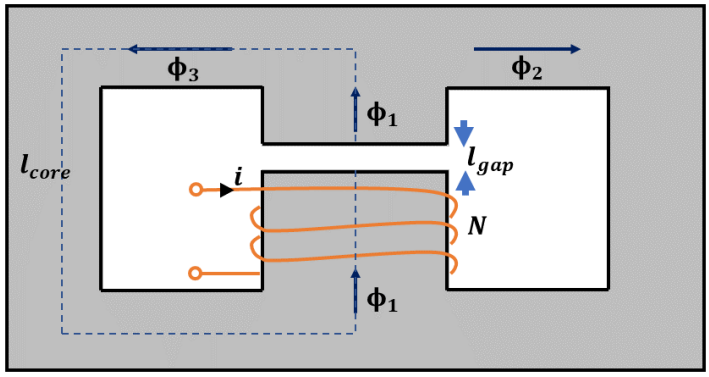


Figure 2.21: Typical EE-core inductor.

Figure 2.21 shows a typical magnetic circuit for an inductor with magnetic core. The figure shows a coil with N number of turns carrying a current i. The flux produced from this current is denoted ϕ_1. By utilizing the relation between *B* and *H*, $B = \mu H$ and introducing reluctance $\Re_k = \dfrac{l_k}{\mu_k A_k}$ as a magnetic equivalent to the electrical property resistance, following can be obtained:

$$\sum_k \phi_k \frac{l_k}{\mu_k A_k} = \sum_m N_m i_m$$

$$\phi = \frac{\sum_m N_m i_m}{\sum_k \Re_k} \tag{2.8}$$

This last transition with $\phi = \phi_k$ is based on the continuity of flux. This is called the law of *no magnetic monopoles*

$$\oint_S \mathbf{B} \cdot d\mathbf{A} = 0 \tag{2.9}$$

and states that the magnetic flux lines must be closed, meaning they every flux line leaving a surface must also enter the surface. Equation (2.8) can be seen as the magnetic equivalent to Kirschoff's voltage law. Self-inductance of a coil is defined

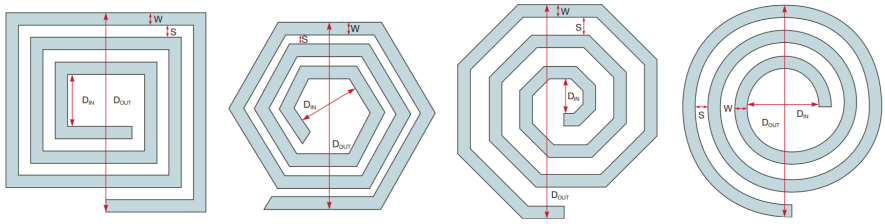
$$L = \frac{N\phi}{i} \tag{2.10}$$

where N is the number of turns in the coil, ϕ is the flux and i is the current through the coil. By substituting the flux, ϕ, from eq. (2.8) into eq. (2.10), a simple analytical formula for the inductance can be obtained.

$$L = N^2 \cdot \frac{\mu_g A_g}{l_g} \tag{2.11}$$

The full derivation can be found on p. 46-52 in [11]. All the H-field is here assumed to be over the mean length l_k. For a magnetic core with air gap, the reluctance of the air gap is often assumed so much bigger than the magnetic reluctance of the core, that all the H-field is in the air gap ($\mu_{core} >> \mu_g$). The mean length l_k then simply becomes the length of the total air gap l_g, as in eq. (2.11). The area A_g is the cross-sectional area of the air gap. If the air gap length is very small compared to the cross-sectional dimensions of the core, $A_g \approx A_c$. The fringing fields effect causes the flux density to be somewhat less in the air gap than in the core. This can be compensated in the analytical model as done in Power Electronics book [11]. Here, it is suggested to add the air gap length to the width and depth of the core, effectively increasing the cross-sectional area of the air gap. Under the assumption of no fringing fields, and that all flux created by the coil is generated within the magnetic core, and no leakage flux, the copper layout does not affect the total self-inductance. There is also an assumption that magnetic saturation does not occur due to the introduction of air gap (i.e linear permeability assumed) . All these assumptions are rough, and not as suited for planar inductors as conventional inductors. In chapter 4 this analytic expression will be compared to simulation results. Inductors can also be made without a magnetic core

and rather utilize the air as a core for the flux. When there is no magnetic core, only air, the inductance calculation becomes very difficult to do analytically. An empirical formula for the inductance of an inductor with air-core is given in eq. (2.12). Air-core is not really a core, just air, but the term is used in lack of a better.



(a) Square **(b)** Hexagonal **(c)** Octagonal **(d)** Circle

Figure 2.22: Different planar inductor layouts. Obtained from [37].

Figure 2.22 combined with eq. (2.12) shows some of the importance of the geometry of the coil when designing an air-core inductor.

$$L = \frac{\mu_0 N^2 D_{avg} C_1}{2} \cdot \left[ln\left(\frac{C_2}{\rho}\right) + C_3\rho + C_4\rho^2 \right] \tag{2.12}$$

where C_1, C_2, C_3 and C_4 are empirical coefficients depending on the electrical geometry. Air-core inductors are most relevant in radio-frequency (RF) applications, due to its magnetic interference and relatively low inductance compared to magnetic core inductors [37]. Air-core also avoids magnetic saturation, and core losses. In chapter 4 a brief comparison of an inductor with and without magnetic core is shown.

2.3.2 Planar inductor

Conventional inductors for PFC and many other applications are toroidal cores with hand-woven windings of copper. Inductance in a PFC boost converter is given in eq. (2.13). With the increased switching frequency made possible by utilizing GaN-HEMT in the boost stage, the inductance of the boost inductor can be reduced for the same ripple current requirement [35].

$$L_{boost} \geq \frac{V_{peak} \cdot d_{max}}{f_s \cdot \Delta i_L} \tag{2.13}$$

Equation (2.13) gives the minimum inductance value of a boost inductor in a classic PFC circuit with switching frequency f_s, peak input AC-voltage V_{peak}, maximum duty cycle d_{max} and maximum ripple on the input current, Δi_L. The maximum input ripple on the current is often limited by a THD requirement. This is however a simplification of the inductance requirement, as the current THD also is dependent on the control system. From this eq. (2.13), the link between GaN-transistors and inductor types become apparent. GaN-transistors can operate at a higher switching frequency for the same losses as a comparable Si-transistor, thus lowering the boost inductor inductance requirement. This

opens up possibilities for unconventional inductor types, such as planar. The definition of a planar inductor can vary in the industry, but in this master thesis, a planar inductor is an inductor with the copper printed on a printed circuit board. The inductor also includes a magnetic core. The advantages of planar magnetics can be summarized as low profile, excellent repeatability, economical assembly, mechanical integrity and superior thermal characteristics [38]. Planar magnetics also has some obvious drawbacks, these can be summarized as low copper fill factor, limited number of turns, relatively high winding capacitance and a large PCB footprint [39]. Planar magnetic devices such as planar inductors and planar transformers are getting more and more used in power converters [40], and an additional drawback is the complexity of designing a planar inductor, as it is not precisely modeled and predicted by conventional inductance/transformer models. Effects like the skin and proximity effect are complex to model. Hysteresis losses becomes complex as the MMF applied to the core is non-sinusoidal, but this is also the case for non-planar inductors. FEM-simulations, which will be introduced in chapter 3, seems to be the only adequate way to model these effects.

A typical way of electrically modeling an inductor is shown in fig. 2.23. This model has an inductance, L_s, which corresponds to the self-inductance of the magnetic core. The resistance is frequency dependent and models proximity effect and the skin effect and its impact on the resistance. The turn-to-turn and turn-to-core capacitance is modeled by the capacitance C_s. The capacitance to ground is modeled by C_{FR4}. FR4 has some dielectric properties ($\varepsilon_r \approx 4.4$), which will be further explained in the next section. As a consequence of the model having both capacitance and inductance, it will have a self-resonance frequency. Above this frequency, the inductor shows capacitive behavior [41]. This self-resonance frequency is assumed much higher than the switching frequency in this master thesis, thus having no, or very low impact, in this project.

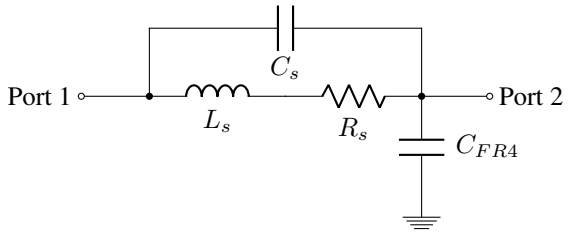


Figure 2.23: Proposed equivalent circuit model of a planar inductor [40].

2.3.3 PCB

The printed circuit board (PCB) is the board which electrically connects the different components in the circuit together and supports them mechanically. It is built with laminated layers of different materials. The PCB is usually made of alternating sheets of fiberglass and copper traces as shown in fig. 2.24. On the outermost layer, there is also a layer of solder mask. This layer is for protecting the copper layer, and for preventing short-circuit. It also helps to solder at the right places where the solder mask is not laid, hence the solder mask. This layer is what traditionally gives the PCB a green color, although multiple other colors are available. On top of the solder mask layer, there is a layer of silkscreen, which

labels different part numbers, symbols and test points. During manufacturing of the PCB, drilling holes between layers can be made, to electrically connect traces in different layers. The copper traces can be made by different approaches. One approach is to utilize a photoresist film on a copper sheet to lay out the traces and expose the copper with light to remove undesirable parts of the sheet. Another technique is to utilize laser etching to lay out the copper traces. The substrate between the copper sheets is usually a glass-reinforced epoxy laminate called FR-4. It is worth mentioning that FR-4 is not a specific material, but rather a grade of material. As shown in fig. 2.24, it is often distinguished between core and ”pre-preg”. The term pre-preg is short for pre-impregnated, and the substrate is solidified during a process of applying pressure, heating and cooling. In principle, cores and pre-preg serve the same purpose, isolation between copper traces and mechanical support for the circuit. Technically, the core is prefabricated with copper on each side, while pre-preg is used to laminate together etched cores. More details regarding the process of making a PCB will not be considered in here. For insight in this topic, paper [42] and note [43] are recommended.

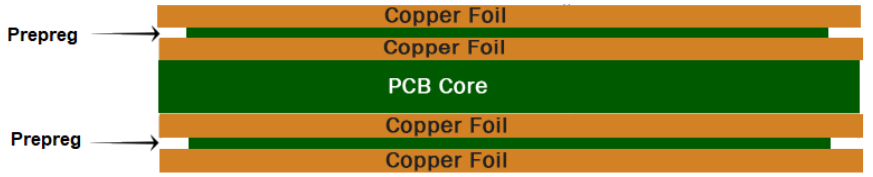


Figure 2.24: 4-layer PCB stackup, illustration obtained from [44].

There are some limitations to the PCB stackup and layout. To a certain extent, the PCB manufacturers can customize thicknesses of core, pre-preg and copper, making very many layout combinations. However, there are some thicknesses more standardized than others [45]. Two of the most standard thicknesses are 35 μm and 70 μm, but customization is very much available, however at added cost.

2.4 Magnetic design and non-ideal effects

When designing magnetic components for power converters operating at switching frequencies in the hundreds of kHz, many considerations regarding non-ideal effects must be done. The high frequency is necessary to reduce the size of the power electronics equipment. Primary design challenges when utilizing switching frequencies in the hundreds of kHz are magnetic core losses and eddy-current effects affecting copper losses. The non-ideal effects will now be examined.

2.4.1 Eddy currents

Equation (2.15) is Faraday's law of induction, which is a version of the more general Maxwell-Faraday equation given in eq. (2.14). This states that an induced electromotive force (EMF) is equal the negative of the time derivative of the flux density. This gives rise to eddy currents. Eddy currents are currents that flow in closed loops within the conductor, perpendicular to the magnetic field [46]. Eddy currents are the basis of several non-ideal effects which will be described later. From Lenz's law, which is described by the negative sign in Faraday's law of induction eq. (2.15), it can be seen that eddy currents create a magnetic field that opposes the external magnetic field. Eddy currents are not only present in pure conductors, but any material with conductive properties.

$$\nabla \times \mathbf{E} = -\frac{\partial \mathbf{B}}{\partial t} \tag{2.14}$$

$$EMF = -\frac{d\phi_{tot}}{dt} \tag{2.15}$$

Some ferromagnetic materials, such as iron, has conductive properties and can be exposed to eddy current losses. Losses in ferromagnetic materials related to eddy currents are simply resistive losses dissipated as heat. There are mainly two philosophies to reduce the eddy current losses in a magnetic core. It is possible to reduce the conductivity by choosing a different material, or it is also possible to reduce the current loop path by laminating the core. The latter is a method of utilizing multiple small magnetic sheets, each electrically isolated from the other, to reduce the path in eddy current loops. The more magnetic sheets one utilizes in a core of fixed size, the smaller loops can be formed by eddy currents and less power is dissipated. Finding materials with low conductivity and high permeability is not an easy task, but ferrite has promising properties. Ferrite is made of iron oxide with small portions of additional metallic elements. The most common additional metallic elements are zinc, manganese, nickel and barium. Ferrites are divided into two main groups, soft and hard ferrites. The soft ferrites are most interesting in power electronic application, as it has the property of low coercivity. Coercivity is explained in section 2.4.4 and is shown in fig. 2.27. Hard ferrites have other applications, mainly permanent magnets, as it has large coercivity. The low conductivity of ferrites helps prevents eddy currents in inductor and transformer applications. The trade-off is lower permeability than for instance iron. The eddy current effect can either occur due to an external magnetic field, or the materials own magnetic field. An example of the first is fringing fields from a magnetic core causing eddy currents. Eddy currents caused by the materials own magnetic field can be summarized in the following sections on skin and proximity effect.

2.4.2 Skin effect

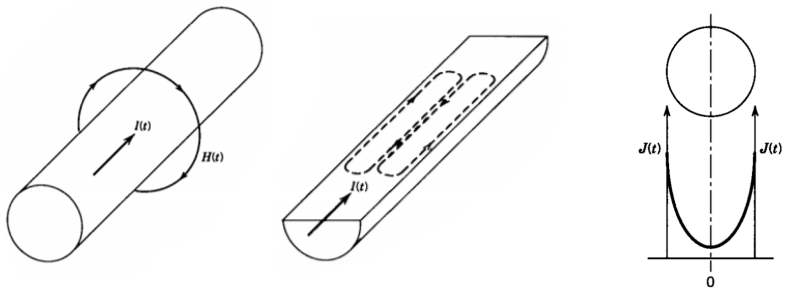
The skin effect is the tendency that alternating current flows more in the outer layer of a conductor and less in the inner part of a conductor. The effect intensifies with increasing frequency. Skin effect is a consequence of eddy currents induced due to the magnetic field circulating the conductor. This means that skin effect is caused by the conductors own current flowing and creating the magnetic field. The eddy currents circulate within the

conductor to set up an opposing magnetic field, resulting in an increased flow of current at the surface of the conductor. The current density decays exponentially with distance into the interior of the conductor [11]. The effect is visualized in fig. 2.25. The effective resistance will increase in a conductor affected by the skin effect. This is due to the decrease in the effective cross-sectional area the current flows through compared to a direct current with no skin effect. The skin depth of a conductor at a frequency is defined so that the current density, J, at the skin depth, δ, is $\frac{1}{e}$ of the current at the surface. Equation (2.16) describes the skin depth at a given frequency. The permittivity, μ, and conductivity, σ, are material-based parameters. For copper, $\mu_r \approx 1$ and $\sigma = 5.8{\cdot}10^7$ at 20^{o}C. Values in table 2.5 are based on these constants.

$$\delta = \sqrt{\frac{2}{\omega\mu\sigma}} = \sqrt{\frac{2}{2\pi f\mu_r\mu_0\sigma}} \tag{2.16}$$

$$R = \frac{\rho L}{A} \tag{2.17}$$

where R is the resistance of a conductor with resistivity ρ, length L, and cross-sectional area A.



(a) Current flow and magnetic field.

(b) Induced current due to circulating magnetic field.

(c) Current distribution.

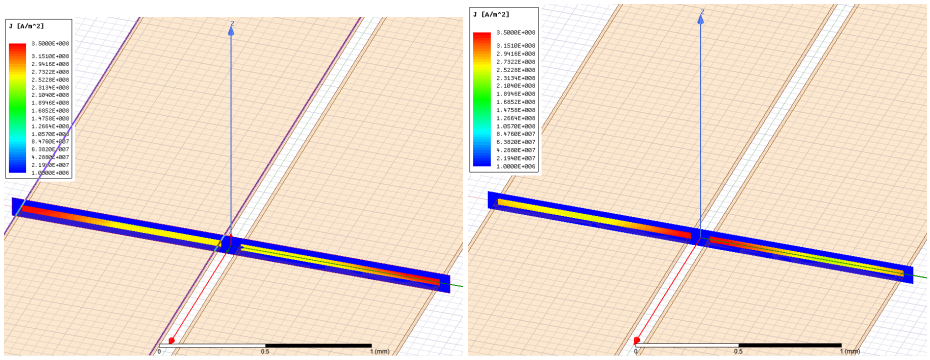
Figure 2.25: Illustration of skin effect obtained from [11].

Table 2.5: Skin depth of copper at 20^{o}C at different frequencies, calculated using eq. (2.16).

Frequency, f	**Skin depth,** δ
50 Hz	9.22 mm
1 kHz	2.06 mm
10 kHz	652 μm
100 kHz	206 μm
300 kHz	119 μm
600 kHz	84.2 μm
1 MHz	65.2 μm
5 MHz	29.2 μm
10 MHz	20.6 μm

2.4.3 Proximity effect

If two nearby conductors carry a flow of alternating current, the current distribution in one conductor will be influenced by the current in the other conductor. The magnetic field circulating one conductor (due to its own current) will induce eddy currents on the second conductor, resulting in an unbalanced current density. If two parallel conductors share the same current, or at least have current in the same direction, the current will be constricted to the opposite edges of the conductors. The two close edges will have a lower current density, as shown in fig. 2.26a. If the two parallel conductors have opposite flow of current, the current density will be largest at the edges of the conductors closest to each other, as shown in fig. 2.26b. The red areas show the highest current density in the figure, while the yellow and green areas have less current density. The complexity increases as more conductors are involved and multiple other effects play a role. The result of the proximity effect is increased resistance. By the same logic as for the skin effect, the current has a more constricted path through a smaller cross-sectional area, thus making the effective resistance larger.



(a) 1MHz AC, same direction. **(b)** 1MHz AC, opposite direction.

Figure 2.26: Two parallel flat copper conductors, height$=35\mu$m width$=1$ mm. Each conductor has a current of 10 A flowing through it.

Both skin and proximity effect can conventionally be reduced by the use of litz wire. Litz wire is a braided wire design with multiple smaller isolated conductors. The advantage of this type of conductor is that each smaller conductor is thinner than a skin depth, giving a much more uniform current distribution within each conductor. Litz wire is not an option for planar inductors, although its principle might be used.

2.4.4 Hysteresis loss

Magnetic hysteresis is a feature all ferromagnetic cores have to some extent, namely that a time-varying flux will dissipate power in the core. The physical phenomena responsible for this power loss is magnetization and demagnetization of the core. When an external field is applied, and the atomic dipoles align with the field, the core becomes magnetized.

Demagnetization of this can be done with an external field pointing in the opposite direction. The phenomena can be described by the B-H-characteristics of a material. This is shown in fig. 2.27. When the core is demagnetized, both B and H are equal to zero. Initially, when magnetizing the core material, it follows the dotted line shown in fig. 2.27. After a while, the core reaches saturation and an increase in magnetizing force will not further increase the magnetization of the material. When saturated, almost all of the magnetic domains in the core are aligned, and a further increase in flux density will require an extreme magnetizing force. When **H** is then reduced, it can be seen from the figure that some magnetic flux remains in the core. This magnetization is often referred to as remanent magnetization, or sometimes the retentivity of a magnetic material. Physically this illustrates that some of the magnetic domains are still aligned with the initial magnetization, and some has lost its alignment. The magnetizing force, **H**, is then further reduced to negative values. The point at which the B-H curve crosses the H-axis, i.e zero flux density, is called the coercivity of the magnetic material. The magnetizing force is further reduced, and a new saturation is reached. This time the saturation of the magnetization is in the opposite direction, but otherwise equivalent of the positive saturation. When the magnetizing force is increased once again, it does not return at the origin, but rather mirrors the path from positive to negative saturation. The B-H curve will not pass the origin and there will be a positive coercivity. A *coercive force* will be needed to return the magnetic flux to zero. The B-H curve encloses a loop. The area of the B-H loop is equal to the energy lost as heat per ”cycle”. The power dissipated is proportional to the frequency of the alternating magnetizing force created by the current in the inductor. The higher the frequency of the current, the higher the total hysteresis losses will become, because there are more looping cycles per unit of time.

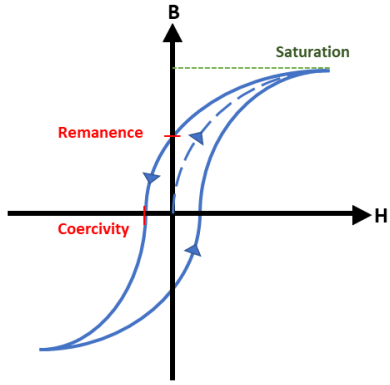


Figure 2.27: Hysteresis curve of an arbitrary ferromagnetic core.

Further examination of the physics behind hysteresis losses will not be considered in this project, but can be found in [47].

2.4.5 Core loss

Core losses are the sum of losses in the magnetic core. As previously presented, this consists of eddy current and hysteresis losses. Core losses also include excessive losses beyond what hysteresis and eddy current losses models, and these are often labelled anomalous or excess losses. The most used equation to characterize core losses is the Steinmetz equation [48], which is given in eq. (2.18). This equation is an empirical, volume specific power loss equation based on material parameters k,α and β (Steinmetz parameters).

$$P_v = kf^{\alpha}\hat{B}^{\beta} \tag{2.18}$$

$\hat{B}$ is the peak flux density induced, by a *sinusoidal* current with frequency f. The major drawback of this equation is the dependency of a sinusoidal excitation. In power electronic applications, it is very often the case that the current through an inductor, and thus the flux density in the core is not sinusoidal. To avoid the sinusoidal dependency, many versions of "improved" Steinmetz equations have been proposed. Many different modifications of the Steinmetz equation is outlined in the paper "Global Loss Evaluation Methods for Nonsinusoidally Fed Medium-Frequency Power Transformers" [49]. Two of these modifications will now be presented, namely the modified Steinmetz (MSE) and the improved general Steinmetz (iGSE). The modified Steinmetz equation is given in eq. (2.19). This equation relates the rate of change of the magnetic flux density to core losses.

$$f_{eq} = \frac{2}{\Delta B^2 \pi^2} \int_0^T \left(\frac{dB(t)}{dt} \right)^2 dt$$

$$P_v = (kf_{eq}^{\alpha-1}\hat{B}^{\beta})f_r \tag{2.19}$$

where k,α and β are same as before (as in eq. (2.18)), and f_r is the fundamental frequency of the waveform. The time derivative of the flux density is given as $\frac{dB(t)}{dt}$ and ΔB is the peak to peak change in the flux density. This can also be said to be the flux density ripple created by the ripple in the inductor current. The improved general Steinmetz (iGSE) is given in eq. (2.20).

$$P_v = \frac{1}{T} \int_0^T k_i \left| \frac{dB(t)}{dt} \right|^{\alpha} (\Delta B)^{\beta-\alpha} dt \tag{2.20}$$

where

$$k_i = \frac{K}{(2\pi)^{\alpha-1} \int_0^{2\pi} |cos\theta|^{\alpha} 2^{\beta-\alpha} d\theta}$$

The improved general Steinmetz takes into account the time derivative of the flux density, the instantaneous and also the peak-to-peak value of magnetic induction. All these different improvements of the Steinmetz equation helps account for the fact that the current through the inductor, and thus the flux density in the magnetic core, contains a ripple and is not sinusoidal. Using conventional core loss models for non-sinusoidal flux variations can potentially be very unprecise. Actual losses can far exceed the modeled losses in such cases, and this is the reason why the improved Steinmetz variants can be relevant for this specialization project [50].

2.5 Core materials

When designing an inductor, the choice of core material is essential to maximize performance. It is often a trade-off between different magnetic properties like magnetic saturation, permeability etc. and other parameters like volume, weight and price. For high frequency applications, there are mainly four categories of magnetic cores. These are iron alloys, amorphous materials, magnetic ferrites and powder core materials. Silicon steel is one of the most popular examples in the iron alloy category. These have the characteristic of high saturation flux density ($\approx$ 1.5-1.8 T) and good permeability [51]. Iron alloys do however often have the major drawback of high electrical conductivity. Eddy current losses may become severe already at medium frequencies ($\approx$ 0.5-10 kHz), and becomes useless at high frequency applications, due to high losses. Iron alloys are more suitable and therefore widely used for low frequency applications.

Amorphous materials have high resistivity, good permeability and low core losses at higher frequencies [51]. Some amorphous alloys are often labelled by the trade name METGLAS [11]. The alloys have a medium high saturation flux density ($\approx$ 0.7 T). This is however also dependent on the exact alloy composition.

Examples of powdered cores are magnetics molypermalloy powder (MPP) cores and Kool Mμ (Magnetics®) cores. Kool Mμ falls into the category sendust magnetic material. Both MPP and Kool Mμ have the advantages of distributed air gap, thus giving them medium to high saturation flux density. MPP has a typically a saturation flux of $\approx$ 0.75 T and Kool Mμ $\approx$ 1 T. Both MPP and Kool Mμ has stable magnetic performance with varying temperature.

The last of the four main categories high frequency core materials is ferrite. Ferrite materials are oxide mixtures of iron and other magnetic elements. Examples of soft ferrites are manganese zinc (MnZn) and nickel zinc (NiZn). The main characteristics of ferrites are high resistivity and high permeability, but relatively low saturation flux density ($\approx$ 0.3 T). The high electrical resistivity of ferrites virtually eliminates eddy current losses, leaving hysteresis losses as the only substantial contributor to core losses.

Chapter 3

FEM-software

This chapter gives insight in how FEM-modelling works, both generally and specifically Ansys Maxwell.

3.1 FEM

The finite element method (FEM) breaks down a design/body, normally 2D or 3D, into a preferably large, but finite number of smaller elements/bodies. These smaller elements or bodies share nodes, boundaries and surfaces depending on the complexity of the geometry. For 1D, a line can be broken down to line segments separated by nodes. In 2D, a plane can be broken into several triangles or shell elements. For 3D, a very common way of meshing is by using tetrahedrons, but as for 2D and 1D other geometric shapes can also be used. The advantage of discretizing a model is that even a relatively complex geometry is broken down into arbitrary smaller geometries, in which the partial differential equations are solvable. The study and analysis performed by the use of finite element method is often referred to as FEA, finite element analysis. It is also referred to as FEMM, finite element method modelling. In this thesis, the FEM-term is used both for finite element method and for finite element method modelling. Maxwells equations, which is the foundation for solving electromagnetic problems are as follows:

$$\nabla \cdot \mathbf{D} = \rho \tag{3.1}$$

$$\nabla \cdot \mathbf{B} = 0 \tag{3.2}$$

$$\nabla \times \mathbf{E} = -\frac{\partial \mathbf{B}}{\partial t} \tag{3.3}$$

$$\nabla \times \mathbf{H} = \frac{\partial \mathbf{D}}{\partial t} + \mathbf{J} \tag{3.4}$$

3.2 Ansys Maxwell

ANSYS Maxwell is a FEM-software for electromagnetic and electromechanical simulations in two or three dimensions. The software provides three different solvers/environment within both the electric and magnetic domain. These three are static, frequency-domain and transient. The frequency-domain environment (also named Eddy-current) provides solutions for purely sinusoidal EMF and MMF, and also gives the possibility to sweep over different frequencies. The transient solver gives the ability to have an arbitrary time-varying EMF or MMF, and the static environment provides, as the name suggests, static or constant MMF/EMF. As the transient solver utilize an arbitrary time-varying EMF/MMF, it is by far the most time consuming of the three solvers. The transient solver discretizes the geometry into smaller elements, but it also discretizes time into time steps. For the static and eddy-current domain, the solver starts with a predefined mesh and solves for the electric and magnetic fields for this mesh. For each mesh-element, the energy is calculated and summed up over all elements. The mesh then gets refined by a predefined percentage, and the same procedure with calculating fields and energy for the new mesh is done. If the change in energy from before and after the refinement is acceptable low, there are no further refinements, and the solution is valid. The limit of what is acceptable low energy error is defined by the user. The refinement based on energy error is referred to as adaptive mesh refinement by Ansys Maxwell. This adaptive mesh refinement technique is not used for the transient solver. The transient solver requires the mesh to be predefined. One of the reasons for this is simply computational considerations, as the transient solver solves for multiple time steps, and a refinement would be heavy to compute [52]. The process of defining the mesh for transient problems is therefore a more time-consuming process then for the static and eddy current solvers. The three different solvers all have basis in Maxwells equations given in eqs. (3.1) to (3.4). The static solver only needs to solve the scalar potentials, as there are no time-dependent quantities, while the eddy current solver needs to solve the vector potentials.

3.2.1 Optimization

Ansys Maxwell has a built-in optimization tool. There are some different optimizer modules such as *Sequential Nonlinear Programming*, *Quasi Newton*, *Pattern Search* and *Genetic Algorithm*. These are fundamentally different and should be used for different purposes. Following description of the different optimization algorithms is obtained from Ansys' own Maxwell manuals [53]. The *Sequential Nonlinear Programming* uses Taylor Series approximation and creates a response surface. This surface is used to determine the gradients and calculates the next step direction and distance. The *Quasi Newton* is a version of the Newton-Raphson method. *Quasi Newton* methods are not unambiguous, meaning it is a general term for multiple methods. Where *Newton-Raphson method* calculates the exact Jacobian matrix, *Quasi Newton* methods approximates this same matrix. The *Quasi Newton* method in Ansys Maxwell utilizes a cost function, and tries to minimize/maximize this. *Pattern Search* performs a grid-based simplex search, which effectively iterates towards a minima/maxima. A simplex is a generalization of a triangle in the n'th dimension. The dimension is determined by the number of unknown variables. For three unknown, the simplex becomes a "triangle in 3D", i.e. a tetrahedron. To un-

derstand a simplex search, it is easiest to visualize a geographical two-dimensional map with contour lines representing constant altitude, and an objective to find the highest peak. The method starts with a triangle superimposed over the map, as a starting point. The altitude at the vertices of the triangle gets evaluated. The corner with the lowest altitude gets moved one direction, and the process gets repeated until a sufficient solution is obtained. If the altitude plot is not too complicated, the triangle trends towards a narrower shape and iterates towards the optimal solution (here: highest altitude). This example can help illustrate the problems of such a simplex search. If it is started with a to narrow ”search field”, the simplex search often end up with a local minima/maxima. The last of the optimization modules is the *Genetic Algorithm*. It does not utilize a cost function to determine further design space, but rather uses random selection applied in a structured manner. The advantage is robustness in finding global minima/maxima, but a drawback is number of iterations might be large.

Chapter 4

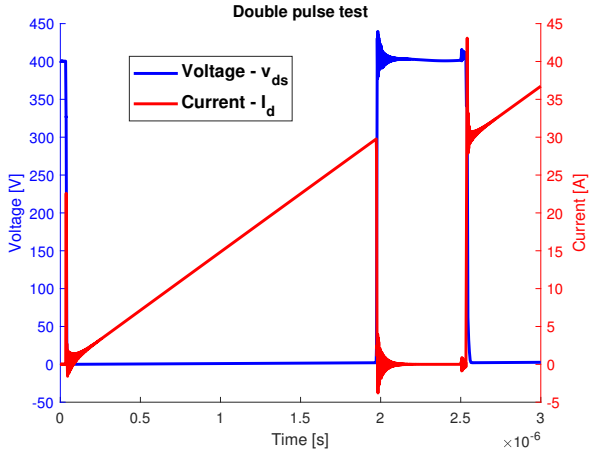
Results and Analysis

This chapter will present some of the main results obtained while working on this master thesis. It will start with a short presentation of switching characteristics for GaN-transistors versus Si-MOSFETs. This section lays the foundation for the major part of this chapter, which will be optimization of a planar inductor. The results and analysis will show the advantage of magnetic core over air-core inductors, and further present parametric sweeps and optimization of a 4-layer planar inductor.

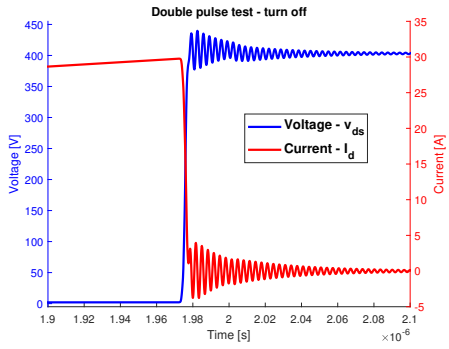
4.1 Switching characteristics of power semiconductors

To describe some of the typical switching characteristics and losses of a GaN transistor, a double-pulse test in LTSpice was performed. The double pulse test was also performed on a comparable Si-MOSFET, to compare the switching losses. Comparing a GaN-device to a Si-device has weaknesses, as the two devices are inherently constructed differently. The GaN- and Si-devices to be compared were picked with comparable $R_{ds,on}$, breakdown voltage and typical drain current. The gate-source, gate-drain and drain-source capacitances along with other parameters then becomes very different for the Si-device compared to the GaN-device. A 650 V e-mode GaN transistor with $R_{ds,on}$ of typically 50 mΩ was chosen to be compared to a 650 V Si-MOSFET with maximum $R_{ds,on}$ of about 45 mΩ. Both these resistances are temperature dependent, but this is not regarded in this thesis. The GaN-device is a GS66508T manufactured by GaN-Systems [54] and the Si-device is a IPB65R045C7 from Infineon [55].

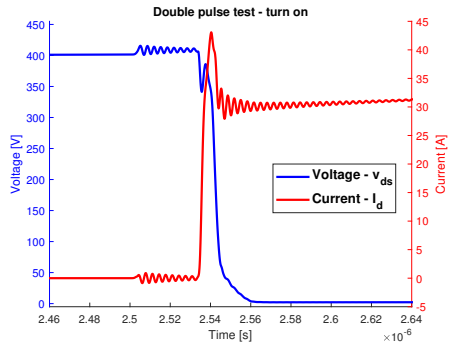
The first device under test (DUT) in the double pulse test is a GS66508T GaN e-mode power switch from GaN Systems [54]. The full LTSpice-circuit and its parameters are shown in appendix E, but a simplified circuit is shown in fig. 4.2. The model includes parasitic inductances at the gate, in the external source and in the power loop. These are respectively L_{GATE}, L_{EX} and L_{DS} shown in the figures in appendix E.



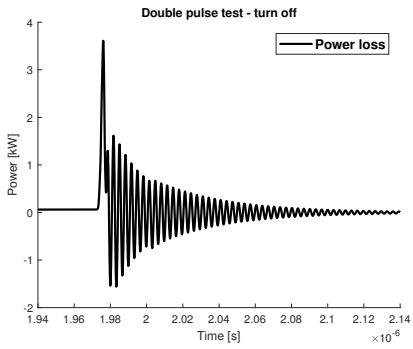
(a) Current and voltage during double pulse test.



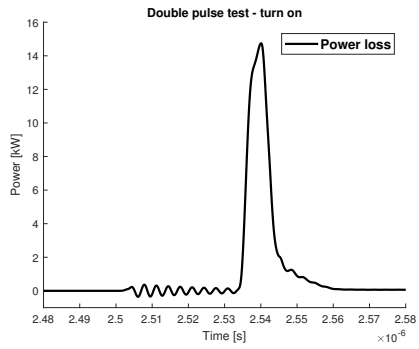
(b) Current and voltage during turn off.



(c) Current and voltage during turn on.



(d) Power loss during turn off.



(e) Power loss during turn on.

Figure 4.1: Double pulse test for the e-mode GaN transistor (GS66508T) from GaN Systems [54].

Figures 4.1a to 4.1b show the voltage and current characteristics during a double pulse test. The half bridge double pulse test circuit is shown in fig. 4.2. The double pulse in-

ductance, L_{DPT}, is chosen so that the drain current of DUT increases to the predefined switching current at a predefined time instance. In fig. 4.1a, the turn off is chosen to occur at 2 μs and turn on at 2.5 μs. The voltages and currents oscillate due to the parasitic inductances. The current during turn on also has a significant overshoot. Figures 4.1d and 4.1e show the power losses during turn off and turn on. The turn-on losses are generally larger than the turn-off losses.

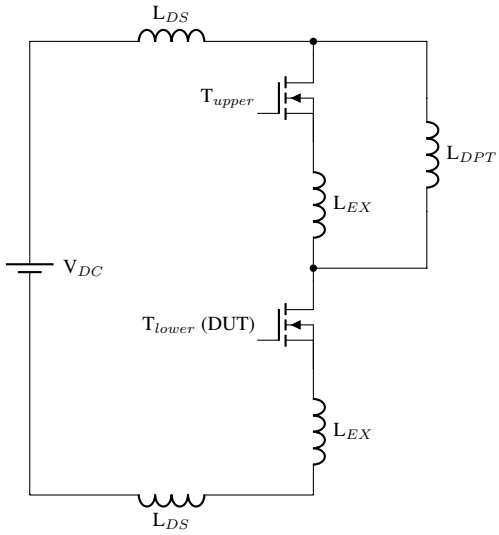
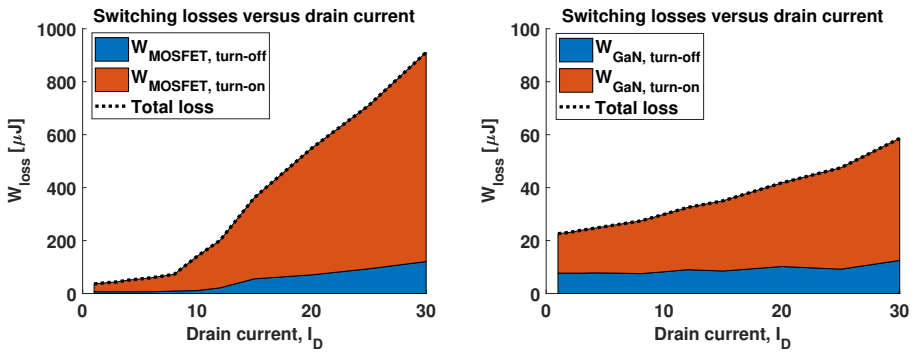


Figure 4.2: Half bridge double pulse test circuit.

The switching losses of the turn-on and turn-off processes can be found by integrating the power loss curves. The integral is performed by the LTSpice software. The gate driving circuit does influence the switching times and thus the switching losses in the transistors. For the GaN-circuit, the positive (turn-on) gate voltage applied was 6 V, and the negative (turn-off) voltage was -3 V. For the MOSFET, the gate voltages were respectively 15 V and 0 V. Different gate-resistances were tested. The most stable gate-resistances for the GaN-test were 8 Ω turn-on and 2.2 Ω turn-off. These values were used during all double pulse tests. No snubber circuits were considered. Figure 4.3 shows the turn-off and turn-on losses stacked on top of each other for both the GaN- and Si-device. Notice the y-axis-limit for the Si-device is ten times larger than for the GaN-device. It is seen that MOSFET switching losses are much larger than for the GaN-transistor. The large difference in losses are mainly due to the reverse recovery of the MOSFET body diode. This does not occur in the GaN HEMT, as they inherently do not have a reverse body diode (ref. section 2.1.7). As the PFC boost converter operates in high frequency CCM, with hard switching, reverse recovery might become a large problem.



(a) Si-MOSFET switching losses.

(b) GaN-transistor switching losses.

Figure 4.3: Switching losses for a double pulse test performed both for the e-mode GaN transistor (GS66508T) from GaN Systems [54] and the Si-MOSFET from Infineon (IPB65R045C7) [55].

Conduction losses due to the on-state resistance are not taken into account. These losses are expected to be fairly similar in the two devices, as they have roughly the same on-state resistance. The switching losses (fig. 4.3) of the Si-device are 10-15 times larger than for the GaN-device in the area around the rated continuous drain current (30 A). For low frequency applications, the switching losses might be negligible, compared to conduction losses. Switching losses (here: power losses, not energy losses) increases with the number of switching cycles per time, i.e. the frequency. The switching losses must therefore be reduced to obtain high switching frequencies, which again reduces power converter size.

4.2 Magnetic core versus air-core

High switching frequencies are the foundation for reducing magnetic components size. Inductor theory was presented in section 2.3. A brief comparison for air-core and magnetic core inductors is now presented. Core losses can be avoided by utilizing air-core inductors, as presented in the section 2.3. Section 2.3 presented an empirical formula for the inductance in an air-core inductor (eq. (2.12)), and an analytical formula for the inductance in an inductor with magnetic core (eq. (2.11)). The corresponding coefficients for this equation are given in table 4.2. A comparison between air-core inductors and magnetic core inductors is difficult to perform, as they are so fundamentally different in their behaviour. The air-core inductor parameters are only dependent on the copper layout. The magnetic core inductor parameters are however strongly dependent on the magnetic material (BH-curve, saturation, conductivity etc.), the air gap length etc. For a direct comparison while occupying the same PCB area, identical copper layouts were chosen for both inductors. The copper layout was made as square turns surrounding a square void. This is an equivalent layout as the one presented in fig. 2.22a with an inner diameter of 6mm and 12 turns. As a core, the ferrite type 3F36 [56] from Ferroxcube was chosen due to its interesting properties at high frequencies (300 kHz - 1 MHz). A more thorough analysis of core materials and geometries will be presented later in this chapter, in section 4.3. The core geometry

was chosen to be an EI-core depicted in fig. 4.6. The current was set to a sinusoidal current of amplitude 1 A and a frequency 600 kHz. To avoid any saturation in the core, an air gap of 0.2 mm was introduced.

Table 4.1: Inductor restrictions for air-core versus magnetic core.

Parameter	Restriction	Description
D_{in}	6 mm	Inner diameter of copper layout
D_{out}	24.6 mm	Outer diameter of copper layout
w	0.5 mm	Copper width
s	0.3 mm	Copper space between turns
h	70 μm	Copper height
N	12	Number of turns
l_g	0.2 mm	Air gap length
Current	1 A	Peak, sinusoidal
Frequency	600 kHz	
Core geometry	EI	Air gap distributed on three legs

Figure 4.4 shows the copper layout of the inductor. The copper layouts are identical for the case with and without magnetic core. It is seen that every turn forms a closed loop, which of course will not be the case for a real inductor. This is a trick to make the design of the inductor in Ansys Maxwell simpler, and more manageable. All turns carry the same current, which is defined as a current excitation through a cross sectional area of the turn. The analyses of air-core and magnetic core inductor are both done in the eddy-current domain of Maxwell, which means only sinusoidal EMF/MMF.

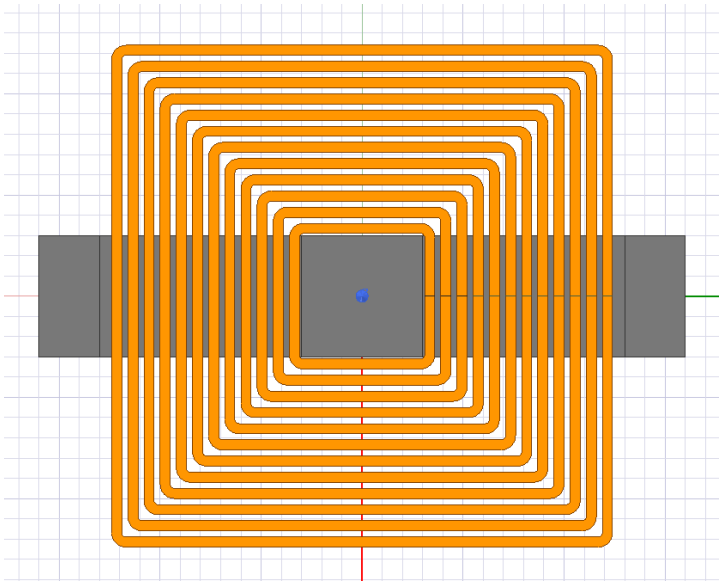


Figure 4.4: Top view of the inductor design including the magnetic core.

4.2.1 Analytical/Empirical calculations

The DC-resistance is theoretically the same in both inductors because they have identical copper layouts. The inductance of the air-core and magnetic core inductors are however different and are now calculated.

Air-core inductor

To calculate the inductance of the air-core inductor, empirical constants are needed.

Table 4.2: Layout-dependent coefficients for air-core inductors. Coefficients used in eq. (2.12) and obtained from [37].

Layout	$\mathbf{C}_1$	$\mathbf{C}_2$	$\mathbf{C}_3$	$\mathbf{C}_4$
Square	1.27	2.07	0.18	0.13
Hexagonal	1.09	2.23	0.18	0.17
Octagonal	1.07	2.29	0	0.19
Circle	1	2.46	0	0.2

The following relationships are also used to calculate the inductance of an air-core inductor (as in [37]):

$\rho = \dfrac{D_{out} - D_{in}}{D_{out} + D_{in}} \approx 0.6078$ is the fill factor, and $D_{avg} = \dfrac{D_{out} + D_{in}}{2} = 15.3$ mm is the average diameter of the inductor. With the use of the square-coefficients in table 4.2 and eq. (2.12), the inductance becomes:

$$L_{empirical} \approx \underline{2.43\ \mu\text{H}}$$

The resistance of the inductor can also be calculated. This is done by calculating the total length of the copper, and using eq. (2.17). A formula for calculating the total copper length can be found in appendix A. In this appendix, the copper length is also calculated for the case with parameters as in table 4.1. With the total copper length of $l_{tot} = 655.2$ mm, a cross-sectional area of A_c=70 μm $\cdot$ 0.5 mm = $3.5 \cdot 10^{-8}$ m^2 and the resistivity of copper at 25^{o}C of $\rho = 1.75 \cdot 10^{-8}$ Ω·m the analytical resistance becomes:

$$R \approx \underline{327.6\ \text{m}\Omega}$$

This is the DC-resistance of the inductor with assumptions of no skin, proximity and external eddy effects.

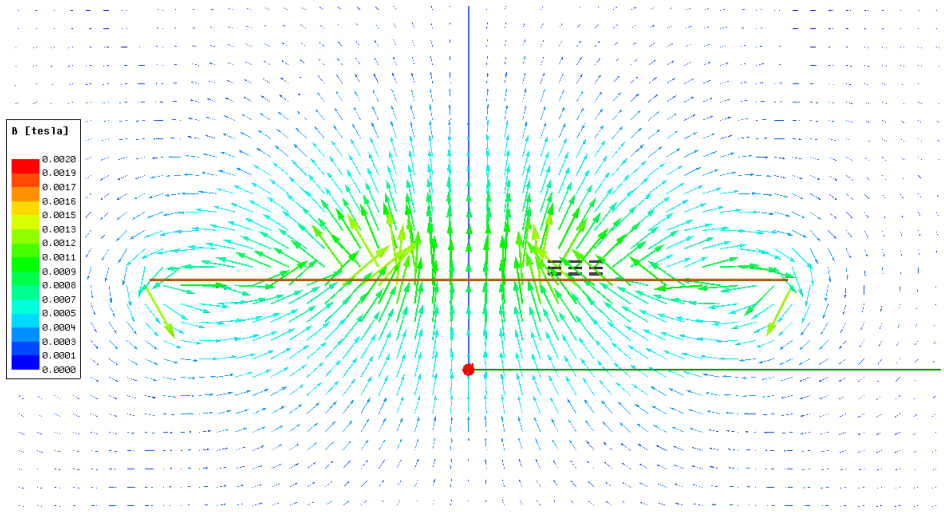
Magnetic core inductor

The magnetic core with the specified 3F36 ferrite material had a chosen air gap length of 0.2 mm to avoid saturation at the given current. With this air gap, the inductance can be calculated:

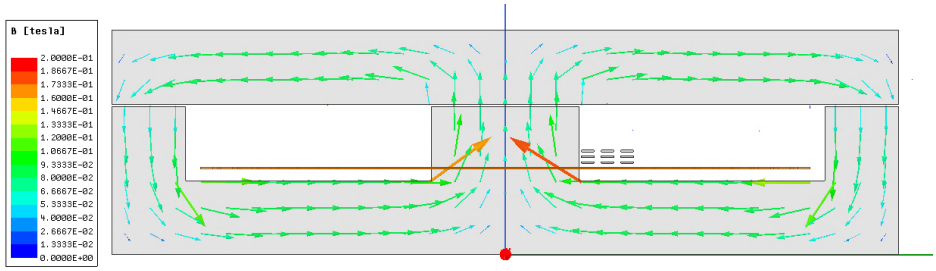
$$L \approx \underline{34.78\mu\text{H}}$$

4.2.2 Simulated inductor parameters

To validate the importance of magnetic core, FEM-simulations were done with the same parameters as given in table 4.1.



(a) Air-core



(b) Magnetic core

Figure 4.5: Air-core flux versus magnetic core flux. Notice that the flux density scale on fig. 4.5b is 100 times larger than in fig. 4.5a.

As expected, the flux paths (i.e. flux densities shown in fig. 4.5) are very different for air-core and magnetic core inductors. Almost all flux is contained within the core for the case with magnetic core, while the flux lines spread through the air with the air-core inductor. The difference in permeability between air and copper is the reason why the flux mainly goes through the core. The relative permeability for air is very close to 1, while the permeability for 3F36 at about 25^{o}C is $\mu_{r,25^oC} \approx$1600. The flux flows through the path of least reluctance in a magnetic circuit, equivalent to current flowing through the path of least resistance in an electric circuit. The effective reluctance of the air-core inductor is much larger than for the magnetic core, which is reflected through the much higher flux density

in the case of magnetic core. The fringing field effect is present in fig. 4.5b, but is so small compared to the flux density in the core that it is invisible in this figure. Fringing effects are covered more detailed in section 4.3. The current distribution in the two inductors are similar, which is reflected through the similar AC-resistance in table 4.3. The current density plots for both air-core and magnetic core inductors are given in appendix B. The flux distribution in fig. 4.5a illustrates one of the problems with air-core inductors. The electromagnetic interference (EMI) this inductor can create, can have severe impact on nearby components. While the magnetic flux mainly is contained within the ferrite core in fig. 4.5b, with the exception of some fringing flux, this is not the case for the air-core flux distribution shown in fig. 4.5a. In theory, a series connection of several air-core inductors could achieve the same level of inductance as the magnetic core inductor, and still have no core losses. This would however violate the industry desire to make compact converters with low EMI.

Table 4.3: Simulated and analytical/empirical inductor values summarized. The difference-column acknowledges the simulated values as the *true* values, and calculates deviation of the empirical/analytical from these.

Air-core				
Parameter	**Description**	**Simulated**	**Empirical**	**Difference**
Inductance	L	2.28 μH	2.43 μH	6.6%
Resistance (DC)	R_{DC}	361.93 mΩ	327.6 mΩ	-9.5%
Resistance (600kHz)	R_{600kHz}	394.99 mΩ		
Core loss	P_{core}	0		
Copper loss	P_{copper}	197.5 mW		

Magnetic core				
Parameter	**Description**	**Simulated**	**Analytical**	**Difference**
Inductance	L	39.52 μH	34.78 μH	-12%
Resistance (DC)	R_{DC}	361.93 mΩ	327.6 mΩ	-9.5%
Resistance (600kHz)	R_{600kHz}	399.91 mΩ		
Core loss	P_{core}	876.9 mW		
Copper loss	P_{copper}	199.95 mW		

In table 4.3, the results of the air-core and magnetic core inductor are summarized. Both the empirical model of the air-core inductor and the analytical model of the magnetic core inductor miss the simulated values by a fairly large margin. This is somewhat expected due to the rough assumptions presented in section 2.3. The simulated values are assumed to be the correct values, even though simulation tricks with closed loop copper layouts were done. The inductance achieved by using a 3F36 ferromagnetic core compared to air-core is approximately 17 times higher. The inductance of the magnetic core inductor is as mentioned dependent on the air gap length, but the air gap is chosen to achieve maximum inductance while avoiding saturation in the core, thus making the air-core and magnetic core cases comparable. The total losses of the air-core inductor are equal to the copper losses, which is $P_{tot,air} = P_{copper} = 197.5$ mW. The total losses for the magnetic

core inductor is $P_{tot,mag}$ = P_{copper} + P_{core} = 876.9 mW + 199.95 mW ≈ 1.08 W. These losses are valid for the current of 1 A_{peak} sinusoidal 600 kHz. The physical size of the magnetic core inductor, i.e. the "PCB-footprint" can be presented as an argument not to choose it above air-core. However, all of the flux generated by the air-core inductor can be defined as fringing, and when practically designing a PCB, the air-core inductor might even have a larger PCB-footprint without considering the inductance. By connecting 17 of the air-core inductors in series, the inductance is comparable to that of the magnetic core, i.e. $L_{air-core}$ ≈39μH. The total losses of this series connection becomes about three times the losses of the magnetic core inductor, i.e. $P_{tot,air}$ ≈3.36 W. Summarized, the air-core inductor will have about 17 times larger PCB-footprint and about three times larger total losses. With additional EMI-problems, air-core inductors are not, as of yet, feasible as a power inductor in converters with desire to be compact and have low losses.

4.3 Optimizing a planar inductor

The planar inductor and its advantages/disadvantages are briefly presented in section 2.3. Different planar inductor designs are now examined and described.

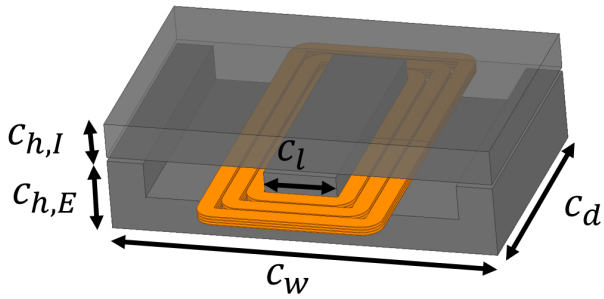


Figure 4.6: Overview of a planar inductor modelled in 3D in Ansys Maxwell.

Figure 4.6 shows a planar EI-core inductor. The name E-I-core simply describes the geometry, the lower part looks like an "E", and the upper core looks like an "I" from the side. The core width, c_w, and core depth, c_d, is the same for the E- and the I-part of the core. The respective height of the E- and I-part of the core is also given in the figure, denoted $c_{h,E}$ and $c_{h,I}$. The centre leg is denoted c_l and is twice as wide as the side legs. This is a common design procedure to avoid any flux density bottlenecks due to geometry. The flux then, at least ideally, penetrates the same cross-sectional area in all of the core. A choice to neglect the capacitance model of the inductor when optimizing the core, was made. Every turn has parasitic capacitance to ground, in addition to capacitance between each turn. The parasitic capacitances are the origin of the inductor having a self-resonnance frequency, as mentioned in section 2.3.2. The parasitic capacitance influences

the current behaviour of each turn, but does not affect the overall energy [39]. The capacitive behaviour is of course still modelled in Maxwell, even though its neglected as an optimizing parameter. All of the turns have slightly different potential, and to minimize the potential difference between neighbouring turns, interleaving can be done. Interleaving is the process to stack the turns of an inductor or transformer in such a way that the parasitic capacitances are minimized. As parasitic capacitances are not regarded in this thesis, neither is interleaving.

4.3.1 Objective and design criteria

The planar inductor is intended to be used as a boost inductor in a classic PFC boost converter as given in fig. 1.1. The inductor has some criteria it has to satisfy to behave as desired along with the rest of the converter. These can be summarized in the table 4.4.

Table 4.4: Design criteria for the PFC boost converter and associated planar inductor.

Parameter	Criteria
Input voltage (converter)	185-300 V_{ac}
Nominal input voltage	230 V_{ac}
DC-link voltage	385 V
Output power	1 kW
Operating temperature	max 100^{o}C
Converter/inductor height	$<$30 mm
Inductor type	4-layer planar PCB-mounted
Turns	12
THD	$<5\%$
Initial inductance	40-50 μH
Switching frequency	600 kHz

A THD of less than 5%, as a time average over 10 minutes, is a legal requirement rooted in the Norwegian regulation of quality of supply, and thus chosen in this thesis. The rest of the design criteria, i.e. the initial inductance, switching frequency, height, temperature, voltage and power corresponds to Elteks requirements for the converter which the boost inductor is a part of. Section 2.3.2 presented an analytical formula for the inductance in a PFC boost converter. It was mentioned that this was a simplification to find the inductance based on the peak to peak ripple in the current, not including the THD. The current THD of the converter is dependent on multiple variables. Among these are the inductance and the control system implemented in the DSP. Control structures and philosophies are presented in the ELK21-report in appendix F. The interdependence between THD and inductance design criteria lead to the choice of designing the planar inductor to the initial inductance given in table 4.4. Simulations in the Simulink model (in appendix C) with the inductance taken from the optimized inductor showed current THD exceeding the requirement (THD$_c$ $\approx$9.8$\%$). The Simulink model is however implemented with a simplified control system than what will be the case in the converter. An example of this, is that the Simulink model does not allow DCM near zero-crossings, which in reality is a common way to handle the zero-crossings.

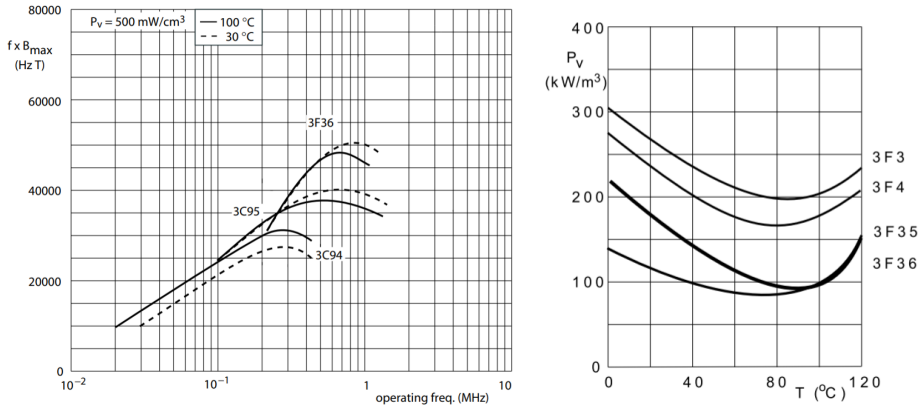
(a) Midgap **(b)** EI-gap

Figure 4.7: A cut section through the mid of the core depth, illustrating the two air gap placements. Notice that the two different cores have the same total air gap length, only distributed differently.

Two core geometries are regarded, or rather two versions of the same geometry. These are shown in fig. 4.7. Both are EI cores, but with different air gap placements. They are hereby named ”midgap” and ”EI” to avoid confusion. There are two main reasons why exactly these two geometries are chosen. First and foremost, these core geometries were among those who showed the best results in the specialization project. A second reason is that these two geometries are commonly used in the industry today, for similar applications [39]. Manufacturability of different magnetic cores is not a well-covered topic in the literature, but cores consisting of more than two separate ferrite pieces, typically held together by a clip, are almost non-existing [39].

4.3.2 Choice of core material

Different core material categories were presented in section 2.5. With the high switching frequency of 600 kHz, iron alloys are more or less infeasible due to its eddy current loss. The powdered core types like Kool Mμ and MPP does not, as of yet, supply planar E-cores, which means no available datasheets. A planar E-core differs from a conventional E-core in that it has a much lower profile, and often larger depth. According to fig. 4.6, this means a low $c_{h,E}$ and large c_d. The same goes for amorphous materials, it shows promising permeability and frequency behaviour, but is not yet available for planar E-cores. As for the air-core simulations, the material chosen to examine is the the MnZn-ferrite 3F36 [56] from Ferroxcube. Ferroxcube is a manufacturer within high performance ferrite materials, and does also have a lot of datasheets available for their products, which makes it possible to compare different materials. The 3F36 material is optimized for usage in the high frequency range (300 kHz-1 MHz), and it has flat power loss and permeability curve (versus temperature), and relatively high flux density saturation.



(a) Materials 3F36, 3C95 and 3C94 compared for their flux density and frequency performance.

(b) Materials 3F3, 3F4, 3F35 and 3F36 and their power losses compared.

Figure 4.8: Core material properties obtained from [57].

The graphs in fig. 4.8 are used to explain the choice of the ferrite material 3F36. Figure 4.8a shows the three materials 3F36, 3C95 and 3C94 and their performance versus frequency. For the same volume specific loss and the same frequency, 3F36 outperforms 3C95 and 3C94 by having a higher maximum saturation flux density, is one interpretation of the graph. Materials 3C95 and 3C94 are regarded to be best at lower frequencies, meaning upwards limited to about 500 kHz. Materials 3F3, 3F4, 3F35 and 3F36 are regarded as well-suited materials for high frequency applications, i.e. optimal for different frequencies between 200 kHz and 2 MHz. These limits are not by any means absolute, but can be regarded as guidelines. An advantage with 3F36 over its other competing materials for high frequencies is shown in fig. 4.8b, namely the low specific losses over a large temperature interval [57]. The PFC boost converter operates under a variety of loading and temperature conditions. A core material with low specific power losses over a broad temperature span is therefore desirable. Even if 3F35 maybe slightly outperform 3F36 at 100^{o}C according to fig. 4.8b, and the operating temperature is maximum 100^{o}C, 3F36 performs better at the lower temperatures.

4.3.3 Optimization setup

To optimize the planar inductor it was parameterized in Ansys Maxwell. As for the rest of the simulations, the Ansys Maxwell model was a 3D model. Multiple snapshots of the planar inductor model is included in appendix G. Four different parameters were selected as the parameters to optimize. These are *z-offset-fraction*, *sidemargin-fraction*, *copperwidth* and *copperspace*. All these four parameters are shown in fig. 4.9. The copper width, w, is measurable in length, here millimetres. The copper space is the space between each turn, also measured in millimetres. The side margin and z-offset fractions are dimensionless, scalar quantities. Both fractions are limited by zero and one. A side margin fraction of 0 means the innermost copper layer is touching the centre leg of the core, and a fraction of

1 corresponds to the outermost layer touching the side leg. Equivalently, a z-offset fraction of 0 corresponds to the lower layer touching the bottom of the inside of the core, and 1 means touching the upper. As the side margin is chosen as a fraction, it is of course dependent on the copper width and copper space of the turns, since the total sideways space depends on these. When minimizing the total losses of an inductor, it is almost always possible to do this by choosing a smaller inductor with less inductance. This is unacceptable. To avoid large inductance fluctuations, the core geometry and parameters were kept constant throughout the optimization process. With the core geometry and parameters fixed, the inductance should in theory be relatively constant, at least based on the simplified behaviour described in eq. (2.11). As the results presented later in section 4.3.4 shows, keeping the inductance constant is a challenge.

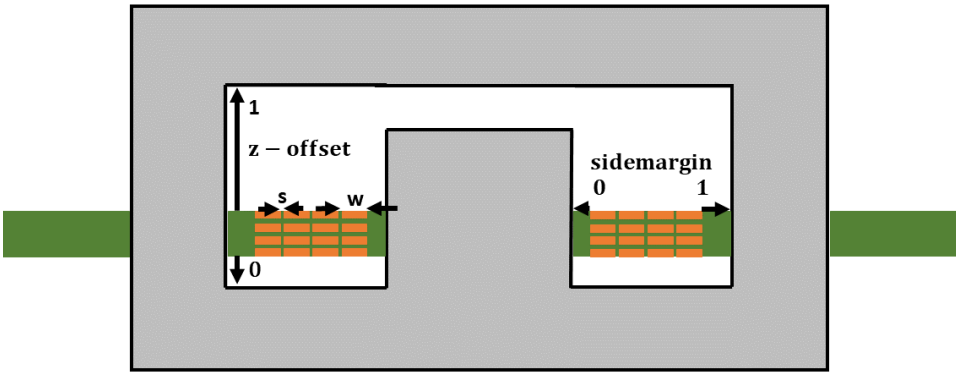


Figure 4.9: Variables for the parametric sweep.

The optimization of the inductor was separated into two different approaches. First each of the four parameters were swept separately while everything else were held constant. By sweeping each variable, while everything else were held constant, it was possible to get an indication of what designs were better than others. This approach does however have an obvious disadvantage. The problem is how to choose at which value the other three parameters should be held. If the z-offset sweep indicates that it is better to keep the PCB in the middle of the core, this might only be valid for the case that the other three parameters are fixed. If one of the other three parameters are changed, there is no guarantee that the previous optimum z-offset is still valid. This is the same as finding a local minimum rather than a global one. The second approach to optimize the inductor was to utilize the built-in optimization tool in Ansys Maxwell. A brief description of the optimization tool is found in section 3.2. The current that flows through the actual inductor

in the PFC converter will be similar to the current showed in figs. 2.13 and 2.14. It will be a rectified sine wave (50 Hz nominal) with a triangular wave ripple (600 kHz). The ripple current has a frequency 12000 times higher than the rectified sine (or 6000 times, as the rectified sine has twice the frequency of its parent sine wave). The consequence of this, is that over a number of ripple periods, the rectified voltage sine wave can be regarded as DC. The nominal voltage of the converter is given in table 4.4, V_{nom}=230 V_{rms}. This gives a nominal rms-current of:

$$I_{50Hz,rms} = \frac{P_{out}}{V_{nom}} \approx 4.35 \text{ A} \implies I_{peak,50Hz} = \sqrt{2} I_{50Hz,rms} \approx 6.15 \text{ A}$$

For a step-up DC/DC, the maximum current ripple is in the boundary between CCM and DCM. This is given by [11]:

$$\Delta i_L = \frac{V_o}{4fL} = \frac{385 \text{ V}}{4 \cdot 600 \text{ kHz} \cdot 45 \ \mu\text{H}} \approx 3.6 \text{ A} \tag{4.1}$$

Ideally, the nominal current of the inductor at nominal load should be dimensioning, when optimizing the planar inductor in Ansys Maxwell. To perform such a FEM-analysis with a complicated transient current is however extremely computational demanding. The complicated inductor current gives complicated flux flow over time. This gives rise to what is known as major and minor loop losses [58][59]. The major loop losses in this case is the core loss at the low (50 Hz) frequency. The minor loop loss is the high (600 kHz) frequency ripple core loss. As a simplification, to reduce the computational time of the optimization and according to the ripple current in eq. (4.1), the dimension optimizing current was chosen to be 2 A_{peak} sinusoidal. When this simplification was done, flux density saturation in the core was avoided by adjusting air gap and core parameters.

4.3.4 Parametric sweep

The parametric sweep considers both an EI-core and midgap-core inductor. The core, copper and test current parameters are given in table 4.5. The method to choose core parameters and air gap length was to first start with some core parameters from manufacturer, and then calculate the air gap length to avoid saturation. If the air gap length was to large compared to the core parameters (i.e. l_g/A_csignificant), larger core parameters were chosen, and the air gap calculated once again.

Table 4.5: Core and copper parameters. Core parameters are according to fig. 4.6 and copper parameters according to fig. 4.9.

Parameter	Description	Value
Core width	c_w	32 mm
Core depth	c_d	20 mm
Core height, I	$c_{h,I}$	3 mm
Core height, E	$c_{h,E}$	6 mm
Centre leg width	c_l	6 mm
Current (sinusoidal)	$I_{peak,ripple}$	2 A
Current frequency	f	600 kHz
Total air gap	l_g	0.7 mm
Total turns	N	12
PCB-layers	-	4
Turns per layer	-	3
Copper width	w	1.4 mm
Copper space	s	0.6 mm
z-axis offset	-	0.2
Side margin	-	0

The four last parameters given in table 4.5 are the parameters which one by one are getting swept. Three of these variables are fixed, while the fourth variable is getting swept.

To avoid saturation in the core, the dimensioning current was, as mentioned, the peak current during nominal load plus the peak of the current ripple. The dimensioning current for avoiding flux density saturation then becomes:

$$I_{dim} = I_{peak,50Hz} + I_{peak,ripple} = 8.15A$$

$$B_{core} \approx \frac{\phi_{tot}}{A_{core}} = \frac{NI_{dim}}{\Re_{eq}A_{core}} \approx \frac{2NI_{dim}\mu_0}{l_g}$$

Considering the 3F36 datasheet [56], and its BH-curve at 100^{o}C, the maximum flux density allowed, was set to 350 mT. A total air gap length of 0.7 mm was found to satisfy this flux density limit analytically, and therefore chosen.

Copper width sweep

The copper width variable, w, was swept over 8 different values between 0.4 mm and 2.4 mm for both the EI-core and the midgap-core. Figure 4.10 shows the inductance and resistance for both the EI-core and the midgap-core. It is observed that both the inductance and the resistance of the midgap-core generally increases with increasing copper width. The opposite tendency is observed for the EI-core. These results illustrates a similar problem

that was presented in section 4.3.3. When optimizing with total loss minimization as goal, the inductance should be kept constant. The DC-resistance is expected to drop with increasing copper width. This is simply because the cross-sectional area "grows" faster than the total copper length of the turns. This can be seen from the simple resistance formula given in eq. (2.17), and the copper length estimation in eq. (A1). By doubling the copper width, the cross-sectional area doubles, but the copper length "grows" with a factor less than two, forcing the resistance to decrease. This is under the assumption that all other parameters are fixed. The AC-resistance is however strongly dependent on the eddy currents induced in the copper (ref. section 2.4.1), and thus the frequency. In general, high frequencies gives more eddy current effects on the conductor, and the effective AC-resistance becomes higher. This will be discussed later in this section.

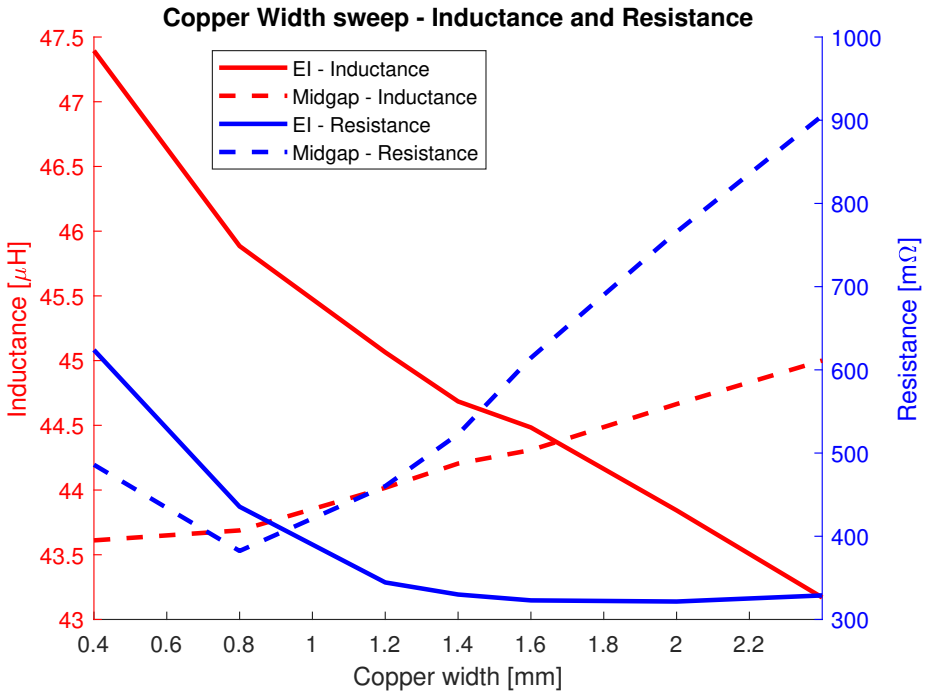


Figure 4.10: Copper width sweep - Inductance & resistance

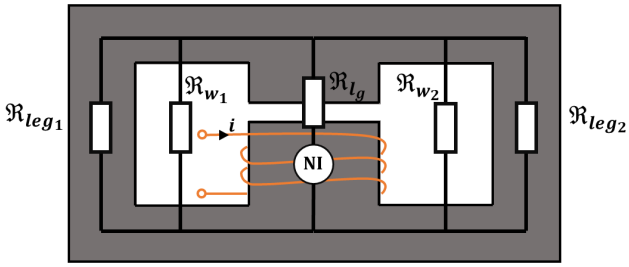


Figure 4.11: Magnetic circuit equivalent of an inductor.

The decrease in inductance for the EI-core can be described by utilizing a reluctance model briefly described in section 2.3. Equation (2.11) can be rewritten as

$$L = \frac{N^2}{\Re_{tot}}$$

The inductance is inversely proportional with the equivalent total reluctance. Fringing fields are actually contributing to a higher inductance. They can be seen as additional parallel branches of reluctance in fig. 4.11, which decreases the total equivalent reluctance, which again increases the inductance. The MMF is represented by the NI-source in fig. 4.11. The MMF in the magnetic circuit is fixed by the current and number of turns, and decreasing the reluctance increases the flux and thus the inductance. In figs. 4.12 and 4.13, opposite trends of fringing fields can be observed. Increasing the copper width decreases the fringing effects for the EI-core, while it increases the fringing effects for the midgap-core. This is why the EI-core has a decrease of inductance, while the midgap-core has an increase in inductance over the copper width sweep. The fringing effects are quantified in table 4.6. The fringing/leakage flux was calculated by use of the field calculator application in Ansys Maxwell. A surface barely slicing the core, but not including the core, at the lower end of the air gap was made. This was made so that all of the fringing and leakage flux from top to bottom went through the surface, not including the flux in the core and air gap. The total fringing/leakage flux was calculated by the field calculator according to

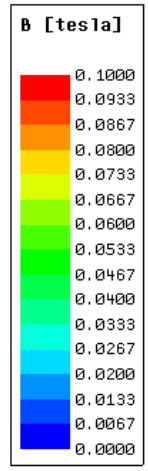
$$\phi_F = \iint_A \mathbf{B} \cdot d\mathbf{A}$$

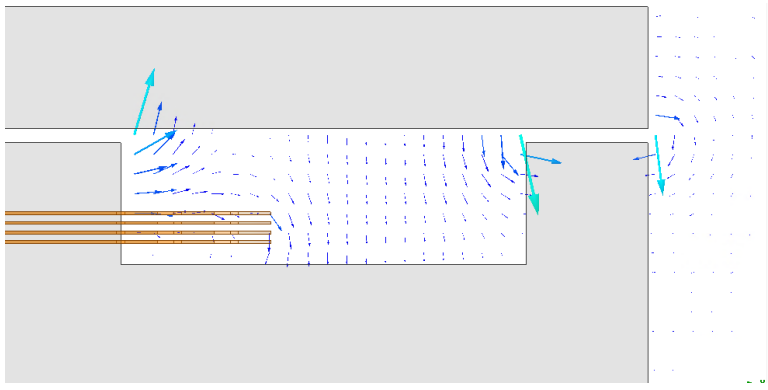
where **A** is the surface described above and **B** is the flux density throughout this surface.

Table 4.6: Quantification of fringing effects through copper width sweep. Current through the inductor is a sinusoidal 600 kHz 2 A_{peak}.

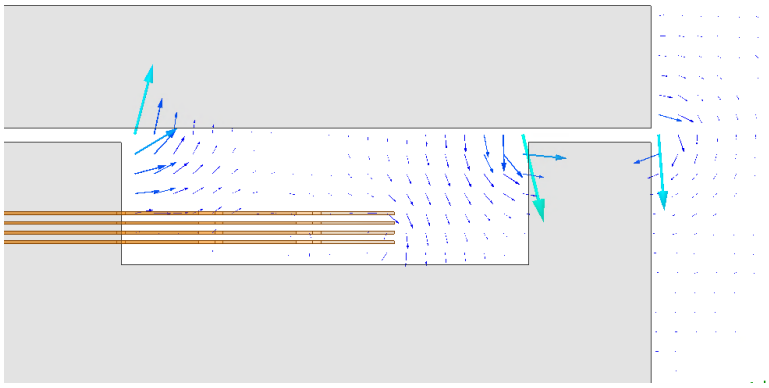
w	Fringing flux (EI-core), ϕ_{EI}	Fringing flux (midgap-core), ϕ_{mid}
0.8 mm	1.523 μWb	1.378 μWb
1.8 mm	1.064 μWb	1.746 μWb
2.8 mm	0.6972 μWb	1.993 μWb

The vector arrows in the following plots in figs. 4.12 and 4.13 have magnitude, color and direction. Both plots are flux density plots, and direction of the arrow gives the direction of the flux in the starting point of the arrow. Both the color and magnitude of the arrows represent the size of the flux density in the starting point of the arrow. The color scale used in all fringing flux plots is shown to the right. The scale was chosen so that differences in fringing effects became clearly visible. The flux density in the core remains much larger than the fringing flux density, and are thus not included in any flux plots.

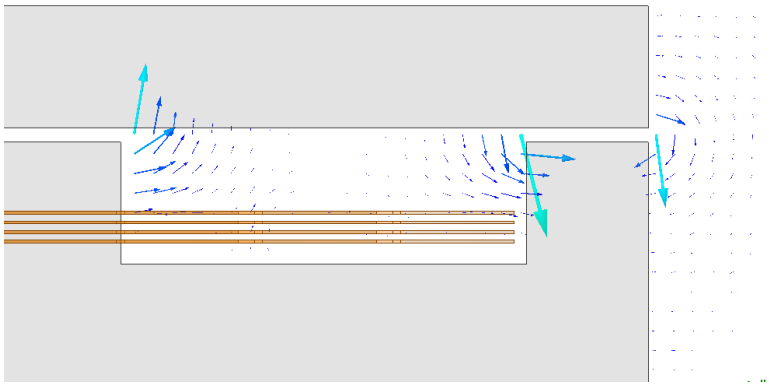




(a) EI, copper width, w = 0.8 mm

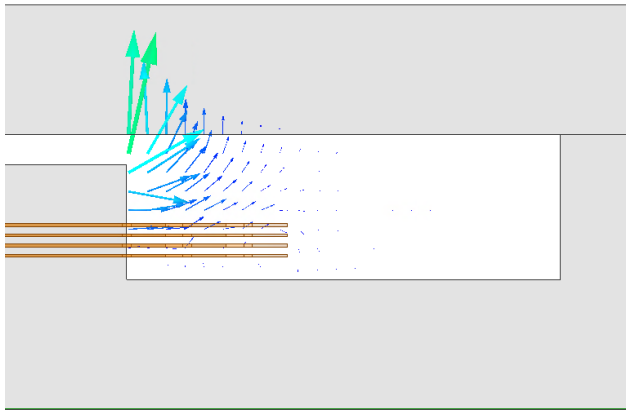


(b) EI, copper width, w = 1.8 mm

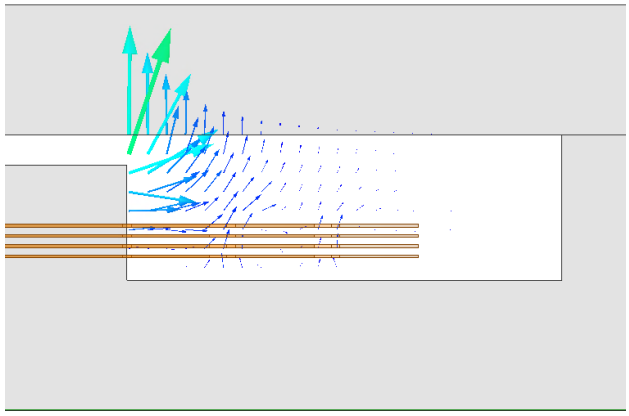


(c) EI, copper width, w = 2.8 mm

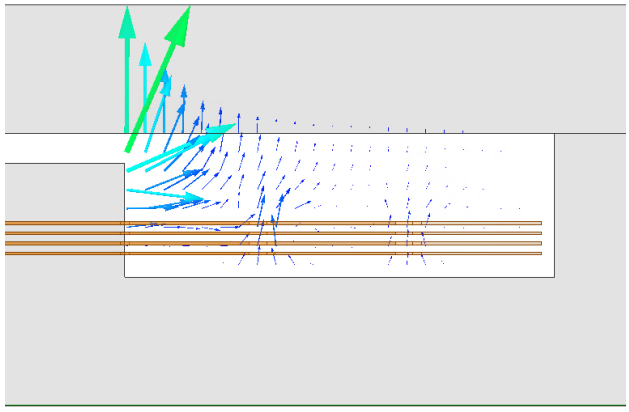
Figure 4.12: EI, copper width sweep, flux density distribution.



(a) Midgap, copper width, w = 0.8 mm



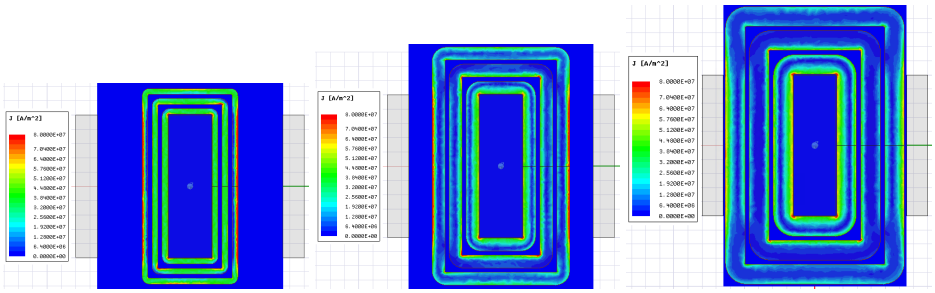
(b) Midgap, copper width, w = 1.8 mm



(c) Midgap, copper width, w = 2.8 mm.

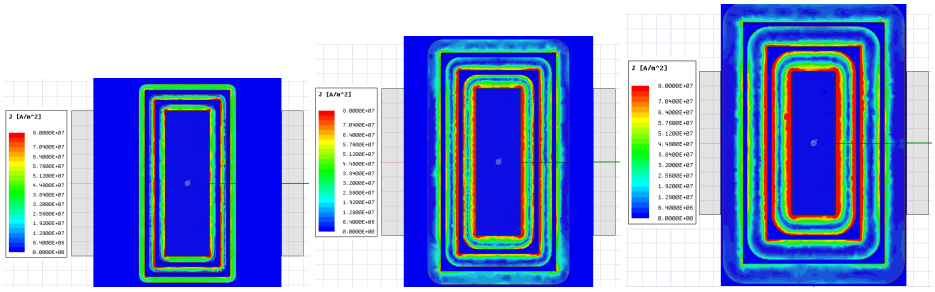
Figure 4.13: Midgap, copper width sweep, flux density distribution.

The resistance trends of the EI-core and the midgap-core are also opposite each other. The DC-resistance drops, as previously mentioned, but the AC-resistance is what is interesting in this application. Figure 4.14 and fig. 4.15 shows the current density in the upper layer of the inductor for the three cases w = 0.8, 1.8 and 2.8 mm. Red areas indicate current density hot spots, which are made by the eddy currents produced from the fringing and leakage flux. A major difference between the EI-core and midgap-core is observed. The current density plot for the conductor in the EI-inductor shows far less impact from eddy currents than for midgap-inductors. Some of the reason for this can be observed in the fringing flux plots shown in figs. 4.12 and 4.13. For the EI-core, the fringing flux is mostly parallel to the ”wide” side of the conductor. In section 2.4.1 it was mentioned that to reduce eddy currents, either reduce the current loop path or reduce the conductivity of the material. This is why the fringing flux ideally should be parallel to the ”wide” side of the conductor, because the eddy currents are induced perpendicular to the flux, and the eddy current path is shorter on the ”tall” side. In the midgap-core flux plots (fig. 4.13) it can be seen that more of the fringing/leakage flux forms perpendicular on the ”wide” side of the conductor, which amplifies eddy current effect and increase resistance.



(a) EI, w = 0.8 mm **(b)** EI, w = 1.8 mm **(c)** EI, w = 2.8 mm

Figure 4.14: Current distribution of EI-core, copper width sweep. Top view.

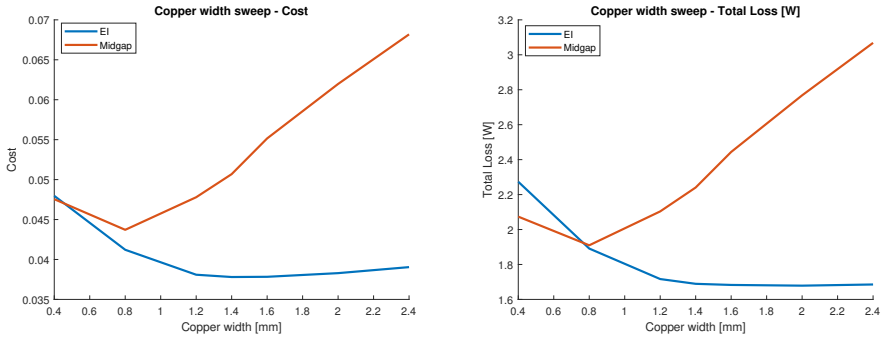


(a) Midgap, w = 0.8 mm **(b)** Midgap, w = 1.8 mm **(c)** Midgap, w = 2.8 mm

Figure 4.15: Current distribution of midgap-core, copper width sweep. Top view.

The total losses through the copper width sweep are shown in fig. 4.16b. The losses are not divided further into copper and core loss because the core loss is fairly constant

through the sweep, and the change in total losses mostly represents a change in the copper losses. The distribution of core loss and copper loss is shown in fig. 4.35.



(a) Copper width sweep - Cost **(b)** Copper width sweep - Total loss

Figure 4.16: Total and total specific losses for copper width sweep.

To try and compensate for the change in inductance through the sweeps, a cost variable was created. This is an objective function equivalent to total loss. This cost variable is later referred to as inductance specific losses, and is simply total losses normalized by inductance, with unit W/μH (later also W/H). By introducing this cost variable as an optimizing objective to minimize, a loss in inductance gets ”punished”. While the total losses for the EI-core are fairly constant from copper width 1.4 mm and upwards, the cost variable increases from this point. It is not obvious that the cost variable created is a better optimizing variable than total losses when designing an inductor. A difference in both total losses and inductance specific losses between the EI-core and midgap-core is observed. This is commented later, in section 4.3.5, after the three other sweeps.

Copper space sweep

The copper space variable, s, was swept over 8 different values between 0.2 mm and 2.6 mm. The copper space sweep shows some of the same characteristics as the copper width sweep, in that the EI-core and the midgap-core has opposite trends.

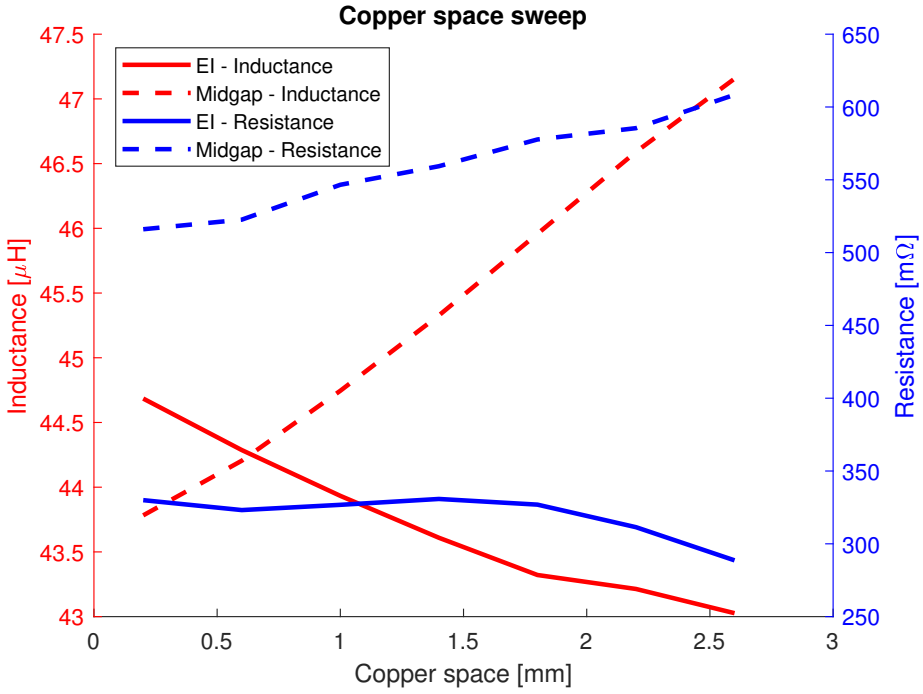
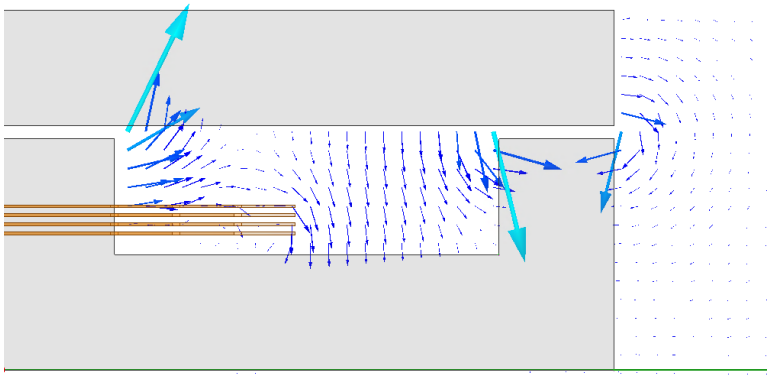


Figure 4.17: Copper space sweep - Inductance & resistance

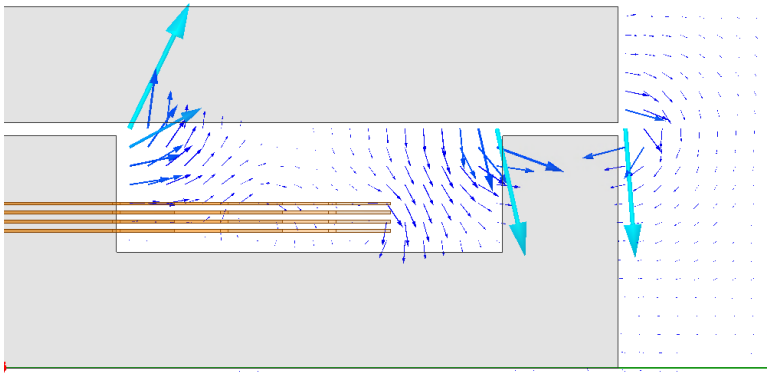
Figure 4.17 shows the inductance and resistance trends for the copper space sweep. The inductance and resistance for the midgap-core increases with increasing copper space, while it decreases for EI-core. The flux plots are given in figs. 4.18 and 4.19. The tendency seems to be decreasing fringing effects with increasing copper space for the EI-core, and opposite for the midgap-core. The fringing flux is also quantified by the use of Ansys Maxwells field calculator application. This result is shown intable 4.7. It is observed that the trends of the fringing flux correspond to the trends in inductance. More fringing flux leads to more inductance. The DC-resistance of the copper increases for increasing copper space, as the total length of the copper increases, and the cross-sectional area is the same. The AC-resistance decreases for increasing copper space for the EI-core inductor, which indicates that the eddy current effect is decreasing more rapidly than the DC-resistance increases through the copper space sweep.

Table 4.7: Quantification of fringing effects through copper space sweep. Current through the inductor is a sinusoidal 600 kHz 2 A_{peak}.

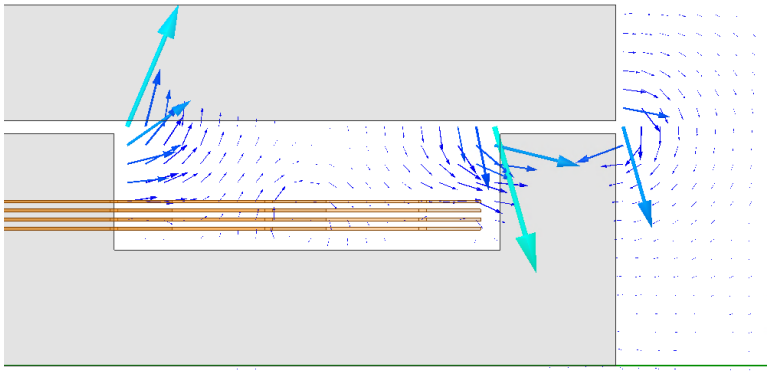
Copper width	Fringing flux (EI-core), ϕ_{EI}	Fringing flux (Midgap-core), ϕ_{mid}
0.2 mm	1.361 μWb	1.444 μWb
1.4 mm	0.9709 μWb	1.969 μWb
2.6 mm	0.6616 μWb	2.509 μWb



(a) EI, copper space, s = 0.2 mm

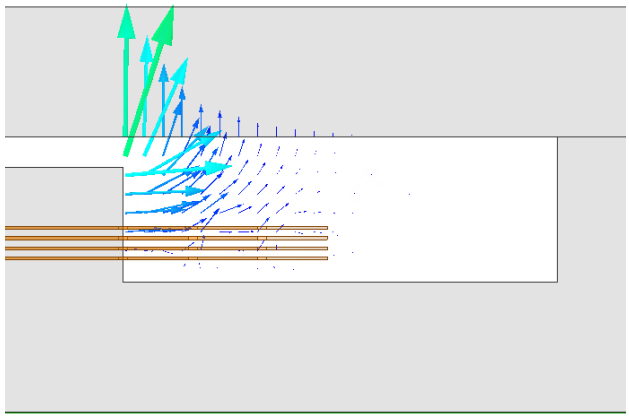


(b) EI, copper space, s = 1.4 mm

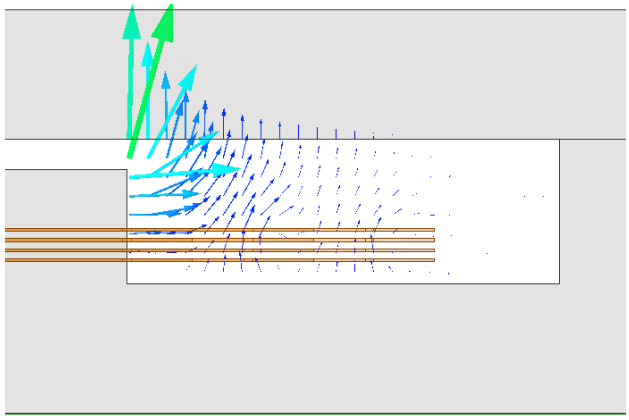


(c) EI, copper space, s = 2.6 mm

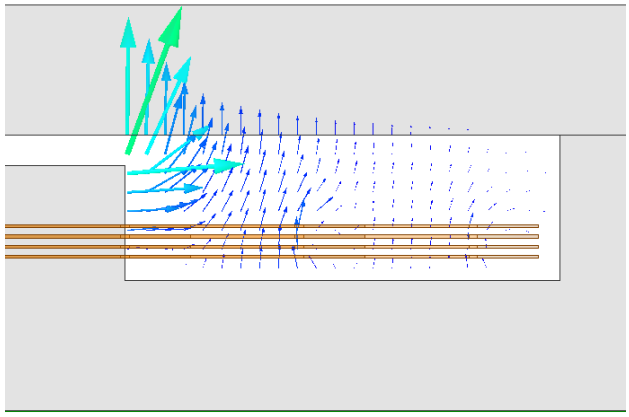
Figure 4.18: EI, copper space sweep, flux density distribution.



(a) Midgap, copper space, w = 0.2 mm

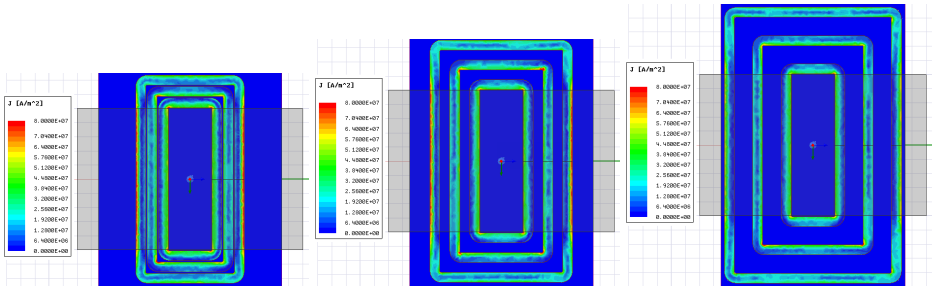


(b) Midgap, copper space, s = 1.4 mm



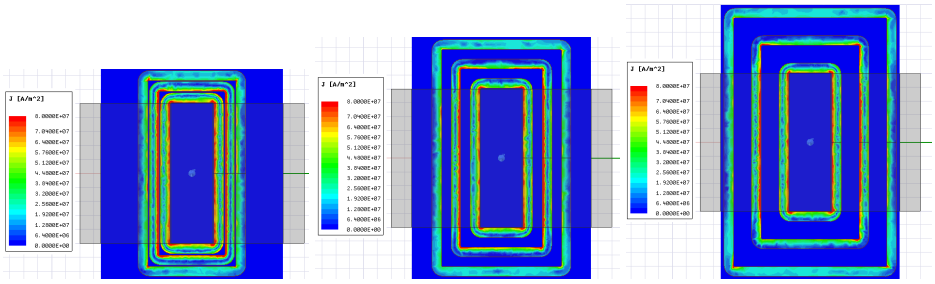
(c) Midgap, copper space, s = 2.6 mm

Figure 4.19: Midgap, copper space sweep, flux density distribution.



(a) EI, s = 0.2 mm **(b)** EI, s = 1.4 mm **(c)** EI, s = 2.6 mm

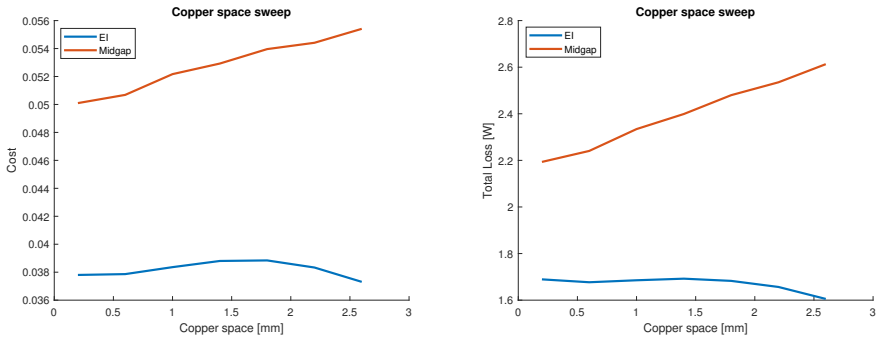
Figure 4.20: Current distribution of EI-core, copper space sweep. Top view.



(a) Midgap, s = 0.2 mm **(b)** Midgap, s = 1.4 mm **(c)** Midgap, s = 2.6 mm

Figure 4.21: Current distribution of midgap-core, copper space sweep. Top view.

Figures 4.20 and 4.21 shows the current distribution differences between EI-core and midgap-core inductors. The qualitative trend of decaying AC-resistance with increasing copper space for the EI-core can be seen in fig. 4.20. Eddy current effects are more prominent when the copper space is small. A closer look at the current distribution shows that the outermost copper layer of the EI-core has an increased current density at the outer parts of the copper, while the midgap-core always has higher current density at the innermost parts of the copper. This has to do with the direction of the flux that produces eddy currents. Snapshots of the current distribution are taken in the positive half-period of the sinusoidal current. The currents are defined to have counter-clockwise direction (when seen from above, as in figures). There is a difference if the fringing flux penetrates from top to bottom or bottom to top. Eddy currents circulates to create a flux that opposes the external flux. By use of the right-hand rule, the current can be visualized as being increased at the inner part of the conductors when the external fringing flux penetrates from below. Vice versa, the current gets reinforced on the outer part of the conductor when the fringing flux penetrates from above. Explanatory figures for the eddy currents are given in appendix D.



(a) Copper space sweep - Cost

(b) Copper space sweep - Total loss

Figure 4.22: Total and total specific losses for copper space sweep.

Once again, the total losses of the EI-core are significantly lower than for the midgap-core. While the total losses of the midgap-core increases significantly through the copper space sweep, the EI-core total losses remain flat.

Z-axis offset sweep

The z-axis offset fraction was swept from 0 to 1 with steps of 0.1, which corresponds to 11 values. For the z-axis offset fraction sweep, the trend is clear. Increasing the z-offset fraction, i.e. placing the PCB higher within the core, generally decreases the inductance and increases resistance, seen in fig. 4.23.

Figures 4.24 and 4.25 show the flux density distribution outside the core, i.e. fringing and leakage flux. The eddy currents circulating in the copper significantly reduces the fringing and leakage flux, by inherently opposing the external flux. This has a double negative effect in that it reduces the total inductance, but also significantly increases the AC-resistance. This tendency of eddy currents opposing the fringing and leakage flux is most observable in the midgap-core flux plots (fig. 4.25). The midgap-core has a drop of inductance of about 20% and about 8 times higher resistance for z-offset fraction 1 compared to 0. For the EI-core the inductance drop is just above 10% and about 5 times increase in resistance.

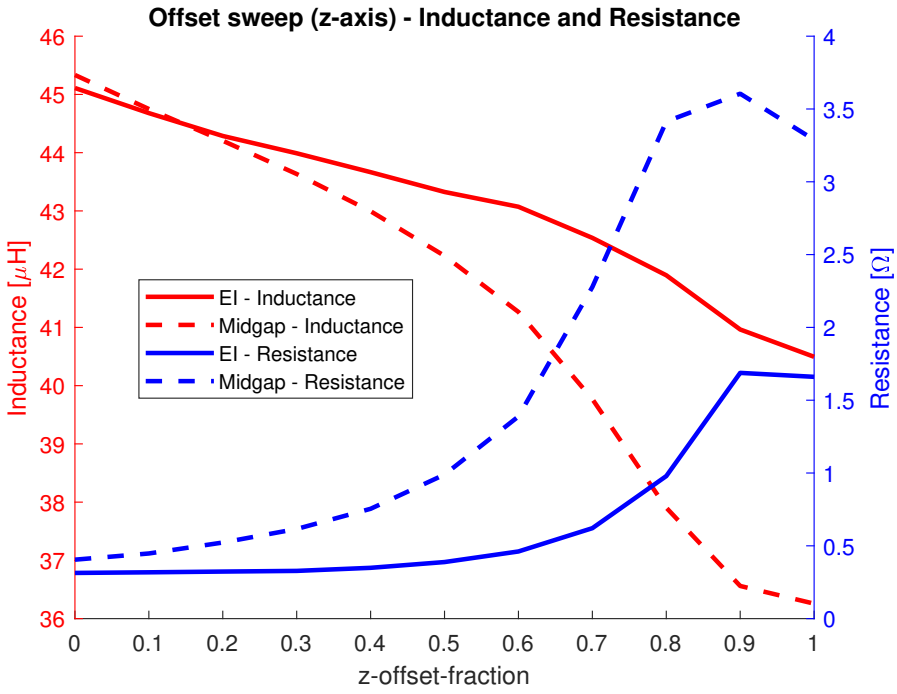
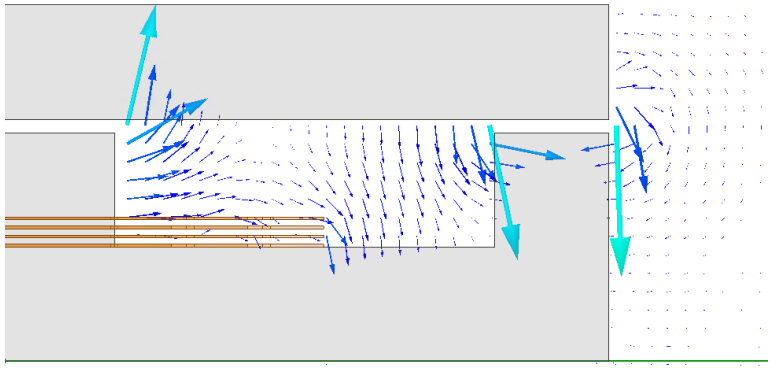
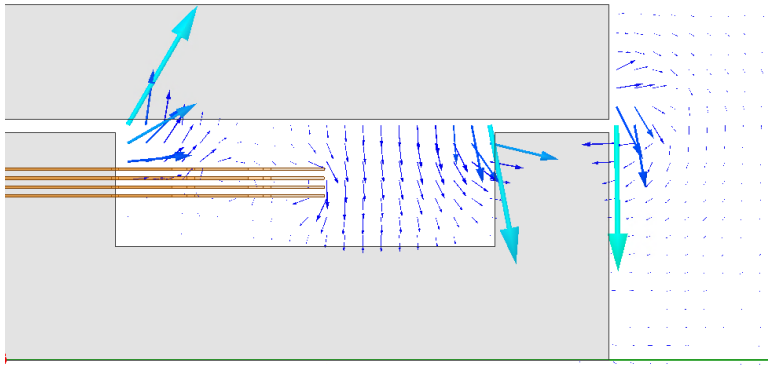


Figure 4.23: Offset sweep - Inductance & resistance

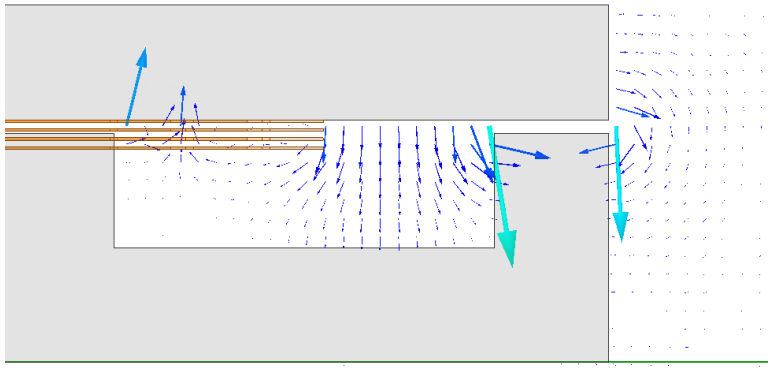
The two core types is seen to perform relatively equal at very low z-offset fraction in fig. 4.23. The trends of increasing resistance and decreasing inductance, however, are seen to be much stronger for the midgap-core.



(a) EI, z-offset = 0

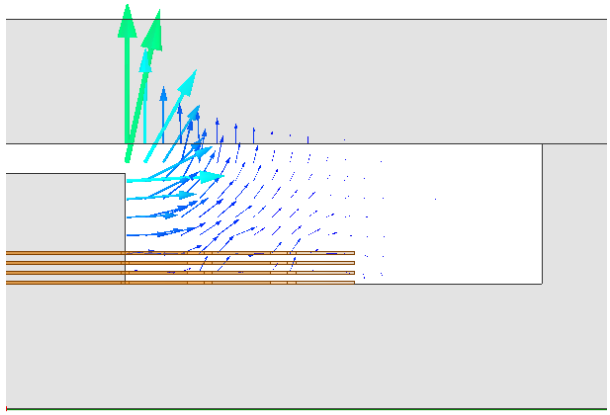


(b) EI, z-offset = 0.5

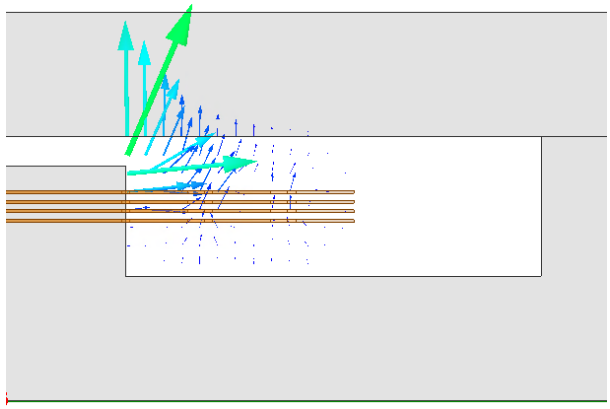


(c) EI, z-offset = 1

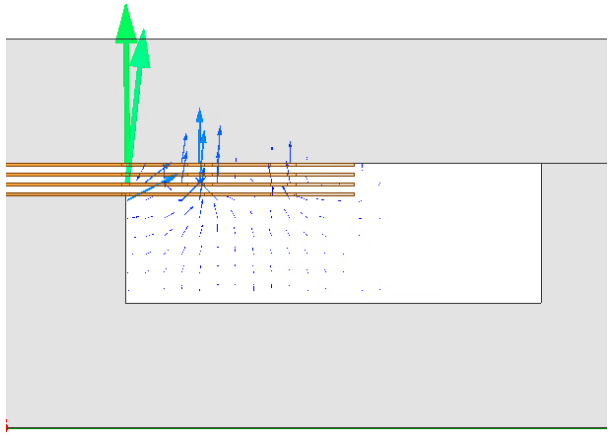
Figure 4.24: EI, z-offset fraction sweep, flux density distribution.



(a) Midgap, z-offset = 0

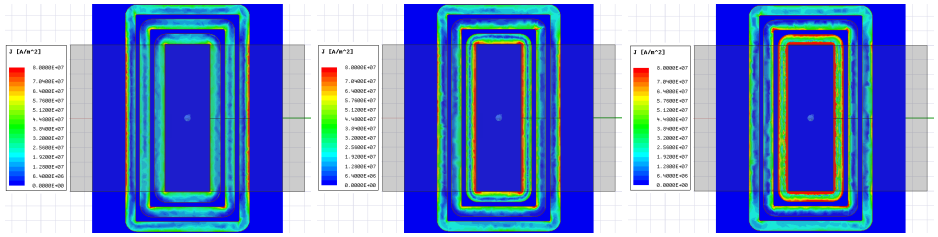


(b) Midgap, z-offset = 0.5



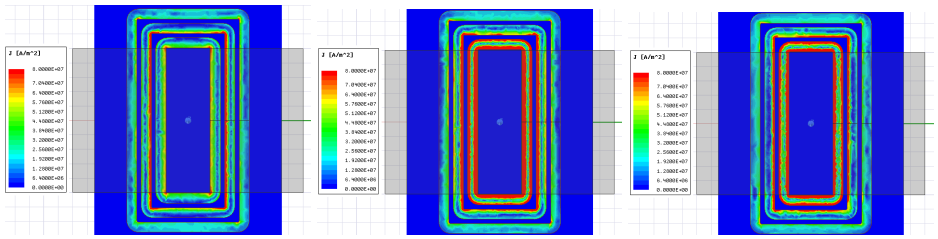
(c) Midgap, z-offset = 1

Figure 4.25: Midgap, z-offset fraction sweep, flux density distribution.



(a) EI, z-offset = 0 **(b)** EI, z-offset = 0.5 **(c)** EI, z-offset = 1

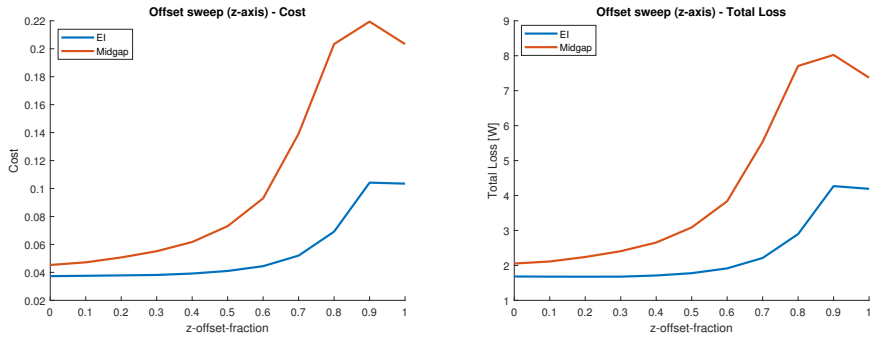
Figure 4.26: Current distribution of EI-core, z-offset fraction sweep. Top view.



(a) Midgap, z-offset = 0 **(b)** Midgap, z-offset = 0.5 **(c)** Midgap, z-offset = 1

Figure 4.27: Current distribution of midgap-core, z-offset fraction sweep. Top view.

The DC-resistance is constant through the z-axis offset sweep. The copper layout itself does not change, but the placement of the copper relative to the core does. It is only the increasing eddy current effect that influences the increasing resistance through the sweep. The current distributions through the z-offset fraction sweep are shown in figs. 4.26 and 4.27. From having low impact at a low z-offset fraction, the eddy current impact is severe at medium to high z-offset fraction.



(a) Offset sweep - Cost **(b)** Offset sweep - Total loss

Figure 4.28: Total and total specific losses for z-offset fraction sweep.

The total losses shown in fig. 4.28b substantiates the previously presented arguments to avoid the PCB near the air gaps. The midgap-core show significantly higher both total losses and inductance specific losses over the EI-core. The EI-core losses remain fairly constant up to a z-offset fraction of about 0.3.

Side margin sweep

The side margin sweep was set up identically as the z-axis offset sweep. The sweep went from 0 to 1 with steps of 0.1, which corresponds to 11 simulation points. The side margin sweep shows the same tendency for both the EI- and midgap-core inductor, seen in fig. 4.29. The trend is however much stronger for the midgap-core. An upwards trend of both inductance and resistance is expected due to the increased fringing flux argument earlier presented. The fringing flux plots are presented in figs. 4.30 and 4.31. The midgap-core has an increased inductance of about 18% and about 3 times higher resistance for side margin fraction 1 compared to 0. For the EI-core the inductance increase is just above 2% and about 1.5 times increase in resistance. This is qualitatively shown in the flux plots (figs. 4.30 and 4.31). For the midgap-core, the fringing and leakage flux strongly increase with increasing side margin, but the same trend is not observed for the EI-core.

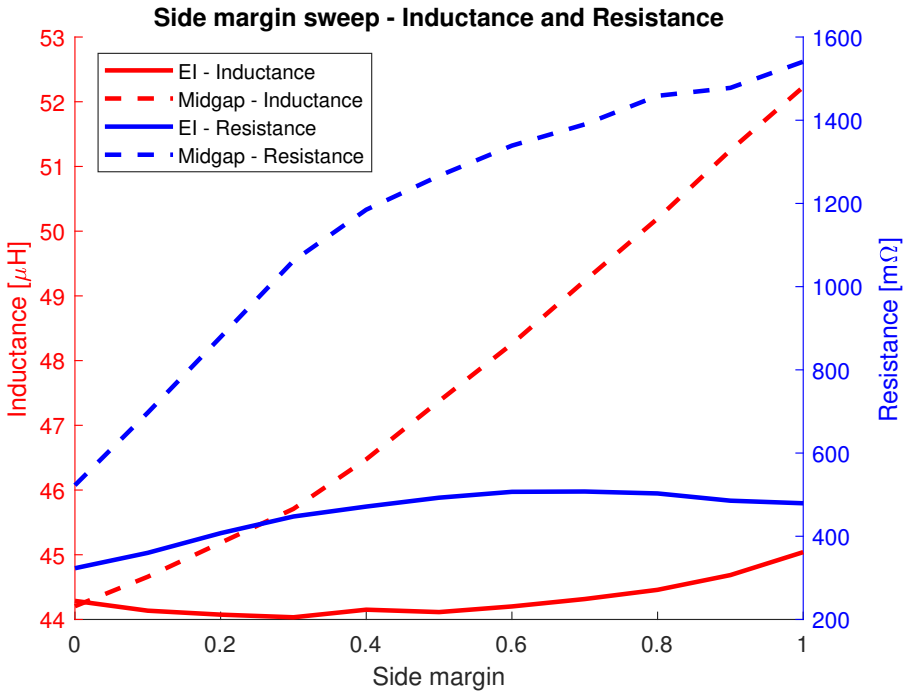
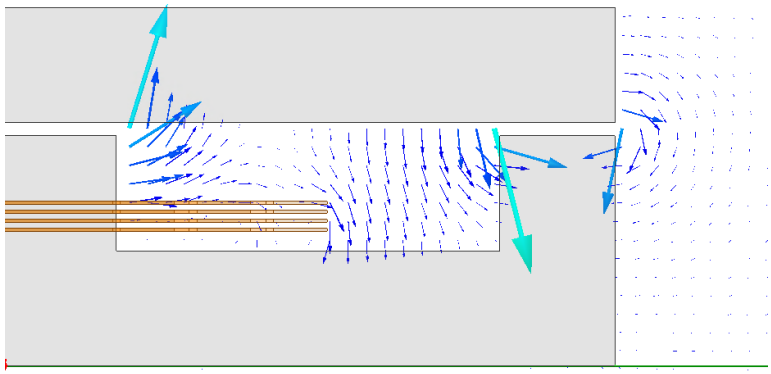
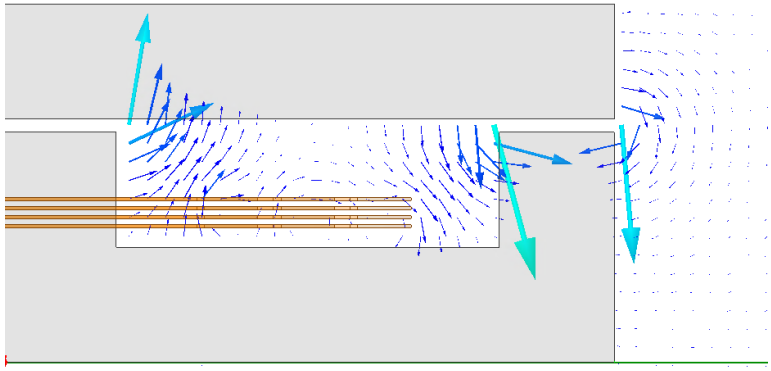


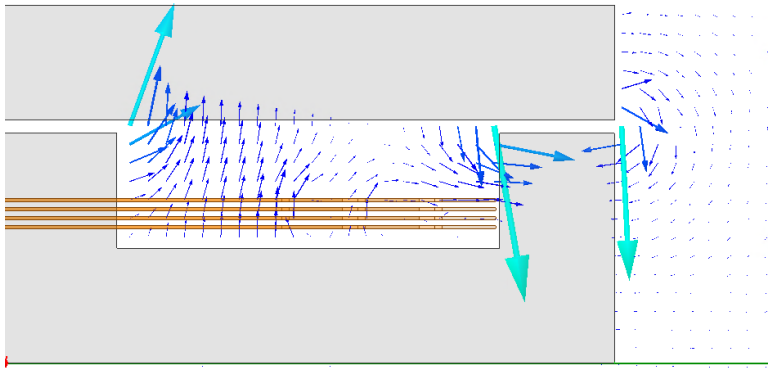
Figure 4.29: Side margin sweep - Inductance & resistance



(a) EI, side margin = 0

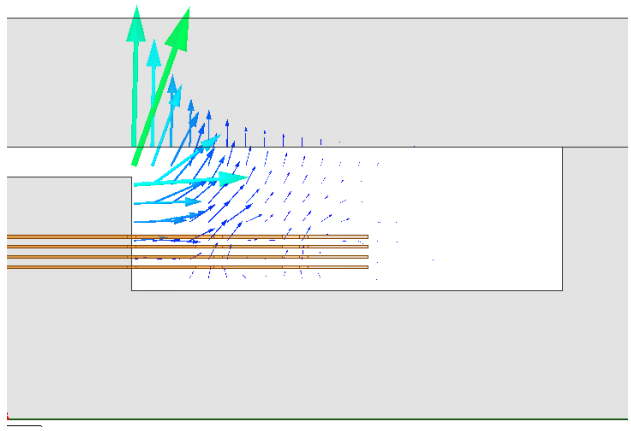


(b) EI, side margin = 0.5

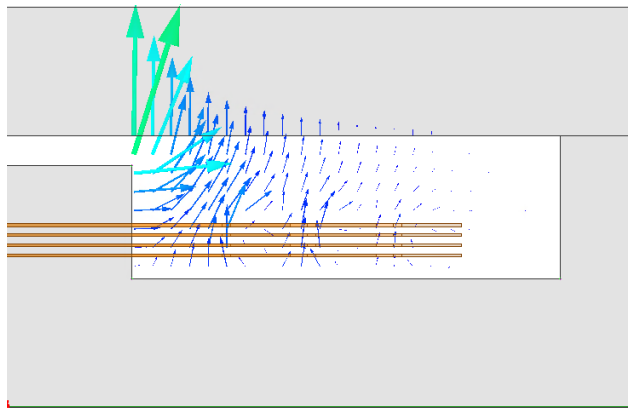


(c) EI, side margin = 1

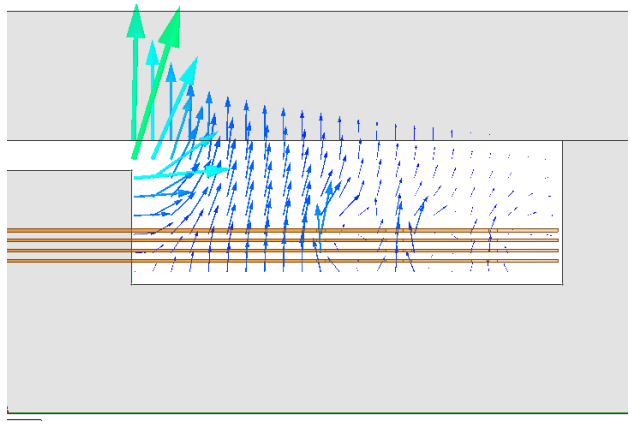
Figure 4.30: EI, side margin sweep, flux density distribution.



(a) Midgap, side margin = 0

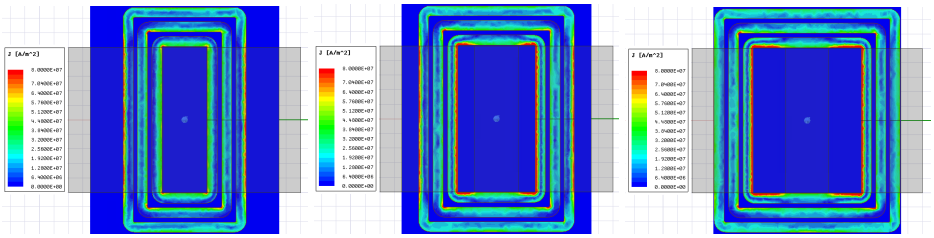


(b) Midgap, side margin = 0.5



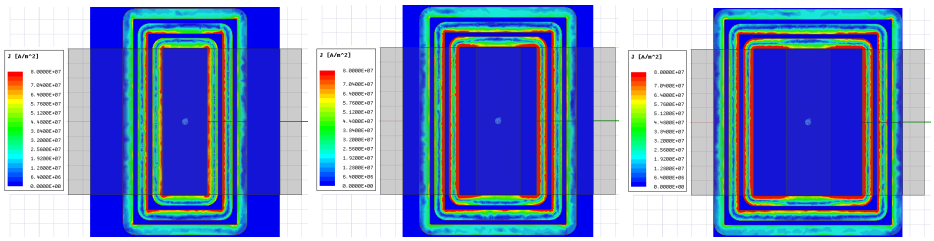
(c) Midgap, side margin = 1

Figure 4.31: Midgap, side margin sweep, flux density distribution.



(a) EI, side margin = 0 **(b)** EI, side margin = 0.5 **(c)** EI, side margin = 1

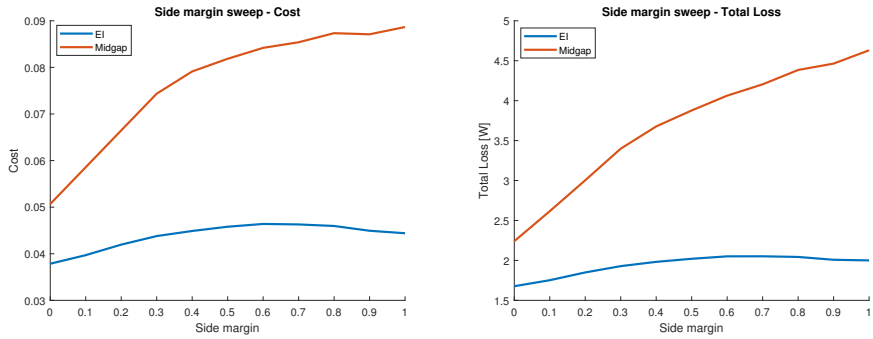
Figure 4.32: Current distribution of EI-core, side margin fraction sweep. Top view.



(a) Midgap, side margin = 0 **(b)** Midgap, side margin = 0.5 **(c)** Midgap, side margin = 1

Figure 4.33: Current distribution of midgap-core, side margin sweep. Top view.

The DC-resistance increases over the side margin sweep, as the length of the copper turns increases, and no change in the cross-sectional area of the conductor. The current density distribution of the top layer of both EI-core and midgap-core is shown in figs. 4.32 and 4.33. It is hard to conclude qualitatively from the current density plots, but the resistance plotted in fig. 4.29 show a strong increasing resistance over the side margin sweep for the midgap-core.



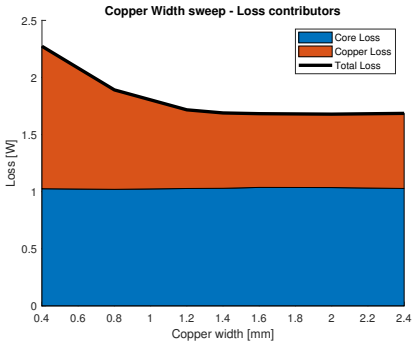
(a) Sidemargin sweep - Cost **(b)** Sidemargin sweep - Total loss

Figure 4.34: Total and total specific losses for side margin sweep.

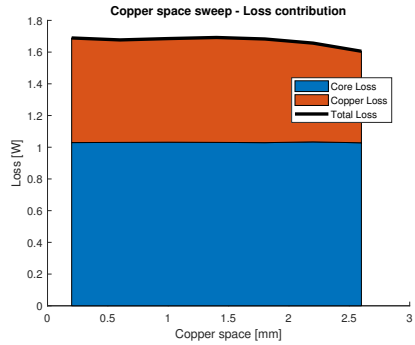
The total and specific losses are shown in fig. 4.34. It is seen that a low side margin, ideally zero, gives the lowest losses both for the midgap- and EI-core inductors.

4.3.5 Parametric sweep summary

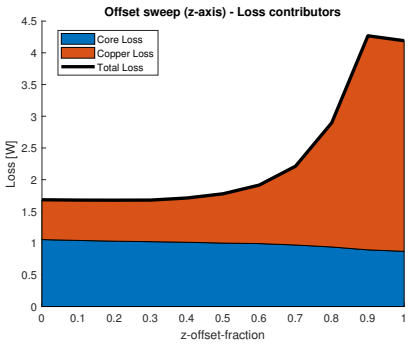
The four different parametric sweeps and its results have now been presented. Some clear trends for optimal designs are observed. Design rules and guidelines can be created from the trends observed. These rules can be summed up to put the copper far from the air gap (low z-fraction) and to have as low as possible side margin to the first turn. The copper width and spacing between turns are individually dependent on the current flowing in the conductor, and the shape of the magnetic core. For the simulations with a 2 A_{peak} sinusoidal current of 600 kHz, the optimal copper width for the EI-core is about 1.4-1.5 mm and low copper spacing, about 0.3-0.6 mm. For the midgap-core, optimal copper width is about 0.8 mm and a small copper spacing of about 0.2 mm. A downwards limit for the copper spacing is about 0.1 mm [39]. This is based on the electrical breakdown of the FR4, which typically is about 40 kV/mm. The losses regarded in this thesis are the copper losses and the core losses. The distribution of copper and core losses are strongly dependent on the current in the coils, i.e. the MMF applied. For the EI-core with 2 A sinusoidal 600 kHz current as regarded in the optimization, the core losses are largely constant through the parametric sweeps. This is plotted for the EI-core in fig. 4.35. The same trend goes for the midcap-core inductor, and it is therefore not shown here. Core losses are presented in the theory in section 2.4.5. For the improved Steinmetz approximation and the core loss model in Ansys Maxwell, it is the flux density, both its absolute value and time derivative, which influences the core losses of each finite element. The flux density in the core is expected to be relatively constant, both in absolute value and its time derivative, even for the different designs tested. This is due to the constant core geometry (and air gap). It is therefore reasonable that the core losses stays relatively constant through the different parameter sweeps.



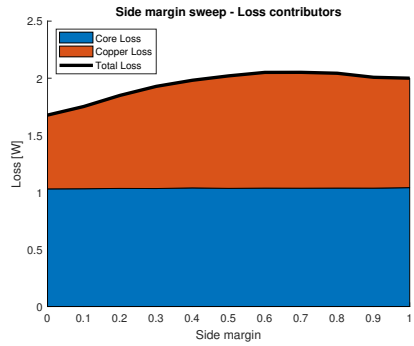
(a) Copper width sweep.



(b) Copper space sweep.



(c) Z-axis offset sweep



(d) Side margin sweep.

Figure 4.35: The core, copper and total losses for the four different parametric sweeps. Only EI-core regarded, similar behaviour for midgap.

4.3.6 Optimization

The second approach to optimize the planar inductor was to utilize the built-in optimization in Ansys Maxwell. Both the *Quasi-Newton* and *Pattern Search* optimization methods presented in section 3.2.1 was tested. The *Quasi-Newton* did not converge as fast as the *Pattern Search*. It was therefore chosen to use the *Pattern Search* for the most extensive optimizations. The objective function for the main optimization was the previously presented cost function, i.e. inductance specific losses.

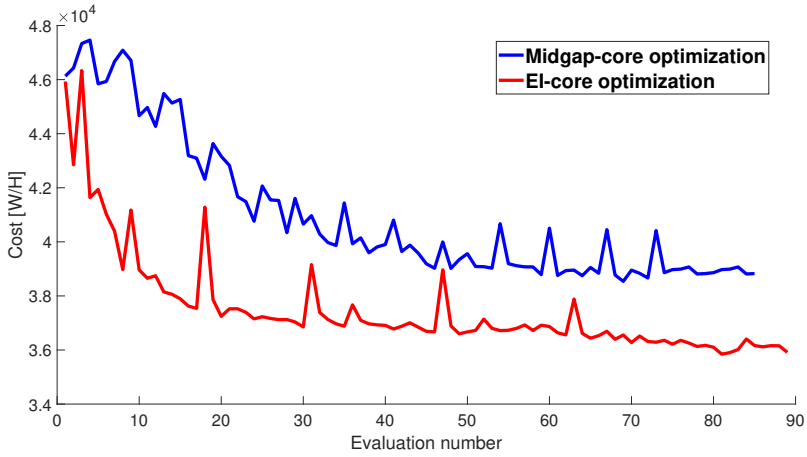


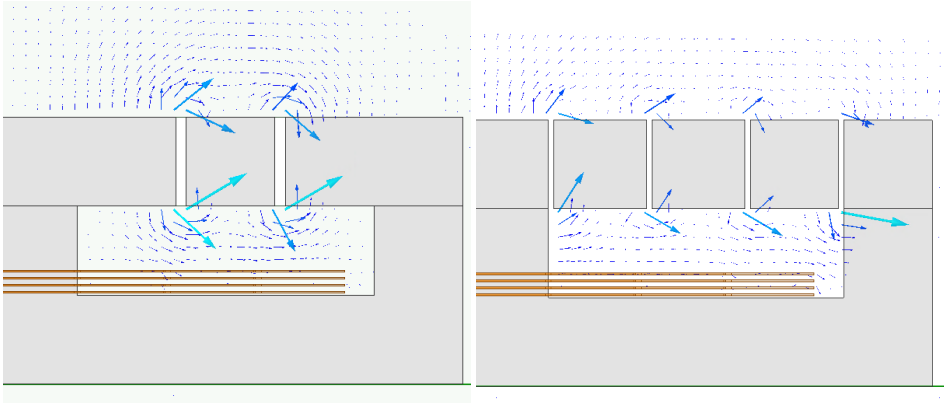
Figure 4.36: Cost-optimization for planar EI- and midgap-core inductor. Cost is still the variable total losses divided on inductance [W/H].

Table 4.8: Optimization results, *Pattern Search* optimization in Ansys Maxwell.

Parameter	EI-core	Midgap-core
Side margin fraction	0	0
Copper width	1.4 mm	0.837 mm
Copper space	0.1812 mm	0.3032 mm
z-fraction	0.025	0.0019
Cost	35845 W/H	38539 W/H
Evaluation number	81	69

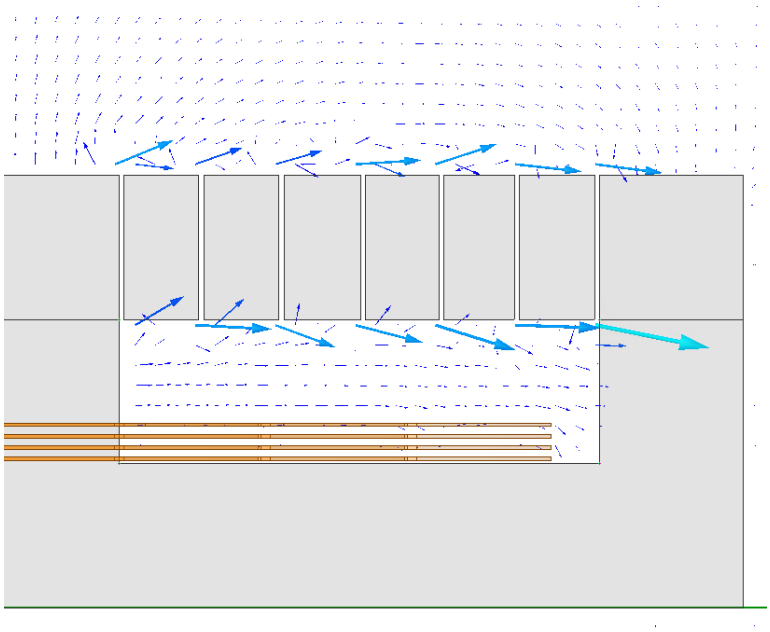
The optimal EI-core inductor with the design criteria given in section 4.3.1 are summed up in table 4.8. These results reinforce some of the design rules based on the parametric sweeps. A low z- and side margin fraction is desirable. Both the midgap- EI-optimization converged in between 80 and 90 evaluations. The cost for each evaluation is plotted in fig. 4.36. Spikes are observed at some evaluations. These occur as *Pattern Search* algorithm (explained in section 3.2.1) has a built-in element of random to try avoiding local minima. From table 4.8, it can be seen that the EI-core outperform the midgap-core with regard to specific losses (cost-variable). The total specific losses are 7.5% higher for the optimized midgap-core than for the optimized EI-core inductor.

4.3.7 Designs beyond design criteria



(a) 2 distributed air gaps in flux path. Total air gap = 0.7 mm.

(b) 4 distributed air gaps in flux path. Total air gap = 0.7 mm.



(c) 7 distributed air gaps in flux path. Total air gap = 0.7 mm.

Figure 4.37: Distributed air gaps at the top of an EI-core.

Figure 4.37 show solutions that outperform the solutions presented in the parametric sweeps and the optimization process. These designs are improvements based on design rules made from observations during the optimization process and in papers [39], [60] and [40]. Distributed air gaps increase the complexity of the manufacturing process. For instance, the solution with seven distributed air gaps each flux path (fig. 4.37c) consists of 13 pieces of ferrite which precisely needs to be mounted. The increased complexity of manufacturing is assumed to add much economic cost, if its even feasible technically.

Table 4.9: Solutions that outperform normal EI-core, but slightly different design criteria.

Geometry	Total losses [W]	Inductance [μH]	Cost [W/H]
2 distr. air gaps (fig. 4.37a)	1.56	48.1	32447
4 distr. air gaps (fig. 4.37b)	1.28	43.7	29389
7 distr. air gaps (fig. 4.37c)	1.22	43.0	28333

Table 4.9 quantify the trends observed in fig. 4.37. The different solutions with distributed air gaps are not thoroughly optimized, but design rules and guidelines previously observed are applied. Even if the designs are not optimized, they show large improvements in reduction of losses, both total and inductance specific. The inductance specific losses are 9.5%, 18.9% and 21% lower than the optimal EI-core inductor for 2,4 and 7 distributed air gaps respectively.

Chapter 5

Conclusion

This concludes the simulation results obtained and analysis performed. The chapter is segmented in small paragraphs that concludes each subject covered in the thesis. Further work is also included in this chapter.

An extensive study on the benefits of GaN-devices and its implications for utilizing planar magnetic devices has been carried out. The simulations regarding the planar inductor have mainly been conducted in the FEM-software Ansys Maxwell, apart for some small tests in Simulink. LTSpice has been used for the double pulse tests.

The double pulse test showed a GaN-transistor outperforming a comparable Si-MOSFET device with about 15 times lower switching losses at rated continuous drain current. Only one GaN-device was tested versus one Si-device, and the conclusions that can be drawn from this are limited. The fact that GaN- outperforms Si-devices at high switching frequencies is however well documented and presented during the theory and literature review in this thesis. The double pulse test amplifies this conclusion.

Analytical and empirical models of air-core and planar magnetic inductors have been compared to FEM-simulations. The analytical/empirical models of the inductors seem sufficient for initial guesses of the inductance, but simulations showed deviations of up to 12% regarding inductance. An extensive comparison of deviation between the analytical/empirical model and simulations was not performed. It was found that planar (PCB) air-core inductors are not feasible in power conversion, at least not for high power density converters with high switching frequencies. The problem for air-core inductors are the low inductance and relatively large PCB-footprint, i.e. the size of the inductor. Additional problems with EMI amplify this conclusion. In simulations, it was found that for the same

inductance specifications, the air-core had 17 times larger PCB-footprint and 3 times larger losses than a comparable inductor with ferromagnetic core.

A planar EI-core and midgap-core boost inductor was optimized with an inductance criterion of 40-50 μH, in addition to other design criteria to fit in a PFC boost converter. Two different methods were used, namely a parametric sweep and a *Pattern Search* (Simplex method). Both methods showed similar trends. It was found that the optimal EI-core inductor outperformed a midgap-core inductor with about 7.5$\%$ with regards to inductance specific losses [W/H] at sinusoidal 600 kHz current of 2 A_{peak}. Design rules that was found can be summarized as keeping copper far from air gaps, trying to maintain conductors parallel to the fringing flux and keeping a low side margin. Even better performing planar inductors can be achieved by adjusting some of the design criteria regarding distribution of air gaps. These solutions can outperform the initial optimal EI-core-solution by at least 21$\%$ with regards to inductance specific losses, simulations show. The designs beyond the design criteria are assumed to be much more difficult to manufacture, thus adding economical cost. Designs that demand comprehensive manufacturing serve against the planar inductor purpose, which are economical assembly, mechanical integrity and repeatability.

5.1 Further work

Laboratory experiments to validate simulation results in an actual PFC boost converter should be performed. Simulation models of power semiconductors have severe weaknesses, and to conclude why GaN-devices are better suited than Si-devices in the specific converter, real laboratory measurements should be done. Both standalone double pulse tests to confirm simulated switching losses and implementation of a GaN-transistor to measure efficiency increase in a PFC boost could be done. The change of the control and gate driving structures when using GaN-transistors above silicon MOSFETs is something that could and should be looked into. The benefits of GaN-transistors applied in other PFC topologies, like the totem-pole topology, is also interesting.

This thesis has only evaluated EI-core and midgap-core for the inductor. This choice was made as these core types are common in the industry today, and thus having available datasheets to replicate the behaviour in simulations. Other core geometries like ER-, EQ- and PQ-cores could be interesting to evaluate for use in planar magnetics. In addition to test different core geometries, it could also be interesting to optimize air gap versus core size (for instance cross-sectional area). Such an optimization could further increase power density, without a significant drop of efficiency.

A more extensive study on different core materials could reveal materials that previously have been neglected in conventional inductors. Planar inductors have different ground rules than conventional inductors, which could open possibilities for unconventional core materials.

To perform a more realistic optimization through simulation, the Ansys environment *Maxwell Circuits* could be integrated into the inductor model. By utilizing this environ-

ment, an accurate non-sinusoidal current through the inductor can be created, and thus a more accurate model is obtained. Thermal considerations have been neglected in this thesis, but this can also be implemented in Maxwell. Some of these potential tasks of further work are however computer-intensive, and supercomputers are recommended. A capacitance model can also be integrated into the model and considered when evaluating/optimizing different designs. With a capacitance model, it would also be interesting to look at the possibility of interleaving the different layers/turns to minimize parasitic capacitance.

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Appendices

A Copper length calculation

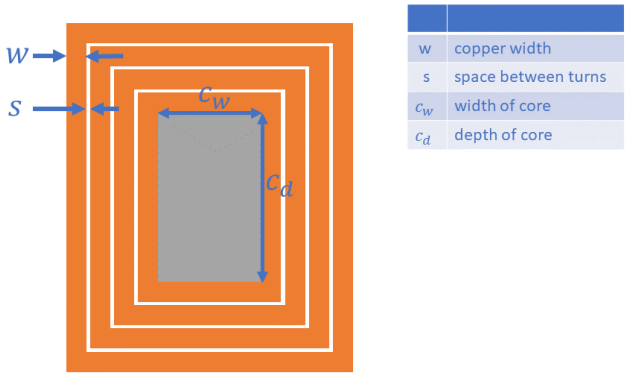


Figure A1: Estimating length of copper.

Length of innermost turn:

$$l_1 = 2(c_w + c_d + 4 \cdot \frac{w}{2}) = 2(c_w + c_d + 2w)$$

Length of turn number two:

$$l_2 = 2(c_w + 2w + 2s + w + c_d + 2w + 2s + w) = 2(c_w + c_d + 6w + 4s)$$

Length of turn number three:

$$l_3 = 2(c_w + c_d + 10w + 8s)$$

Length of turn number n:

$$l_n = 2(c_w + c_d + (2 + 4(n-1) \cdot w + 4(n-1) \cdot s)$$

Length of coil with n-turns:

$$l_{tot} = \sum_{k=1}^{n} l_k = \sum_{k=1}^{n} 2\Big(c_w + c_d + (2 + 4(k-1)) \cdot w + 4(k-1) \cdot s\Big)$$

$$= \underline{2n\Big(c_w + c_d + 2w \cdot n + (n-1)s\Big)} \tag{A1}$$

A.1 Example calculation

Calculating the length of the copper for the case in section 4.2, with parameters as given in table A1.

Table A1: Dimensions of the copper lay-out.

Quantity	Size
n	12 [turns]
c_w	6 [mm]
c_d	6 [mm]
w	0.5 [mm]
s	0.3 [mm]

$l_{tot} = 2n(c_w + c_d + 2w \cdot n + (n-1)s) = 2 \cdot 12 \cdot (6+6+2 \cdot 0.5 \cdot 12 + (12-1) \cdot 0.3)mm = \underline{\underline{655.2mm}}$

B Current density distribution for air-core and magnetic core

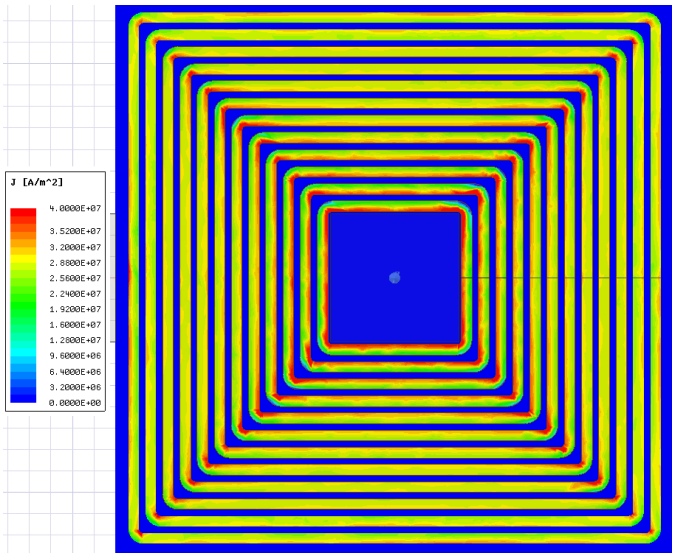


Figure B1: Current density distribution of the air-core inductor.

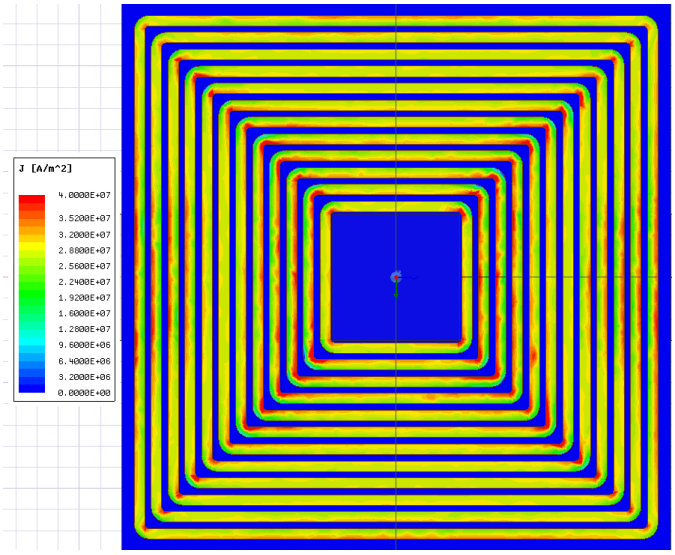
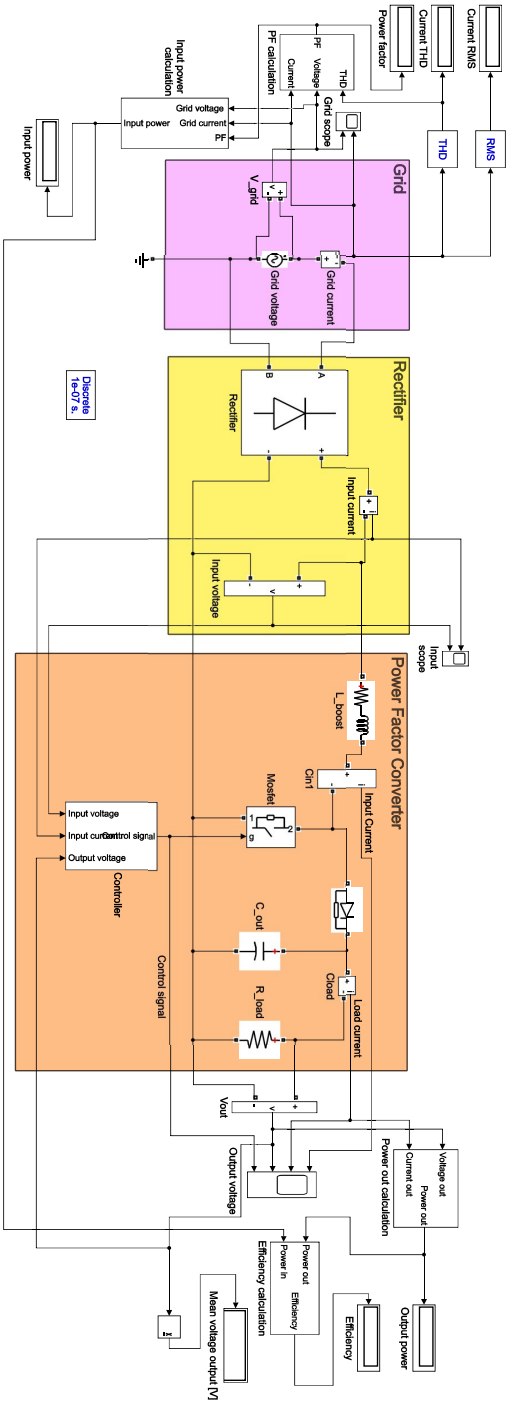


Figure B2: Current density distribution of the magnetic core inductor.

C Simulink model of a PFC boost converter



D Fringing flux and induced eddy currents

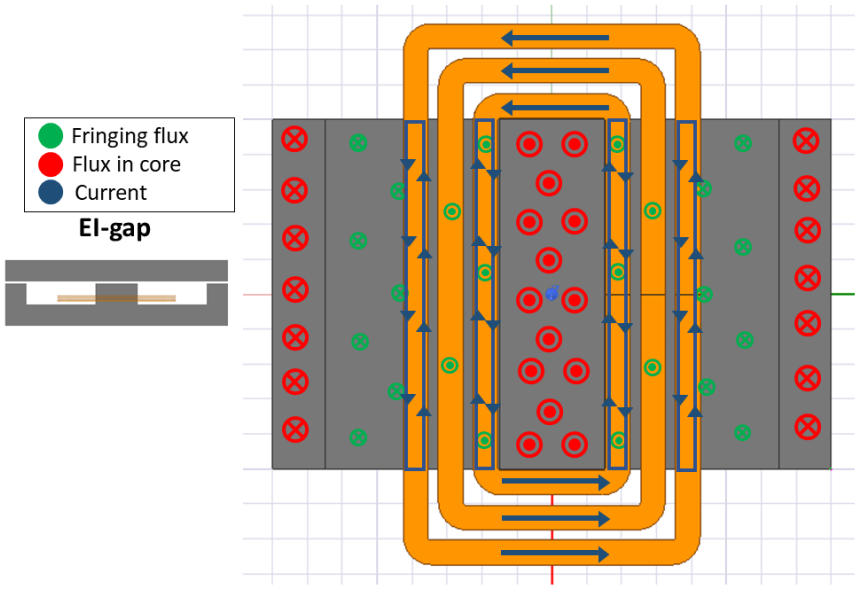


Figure D1: Eddy currents induced for EI-core inductor.

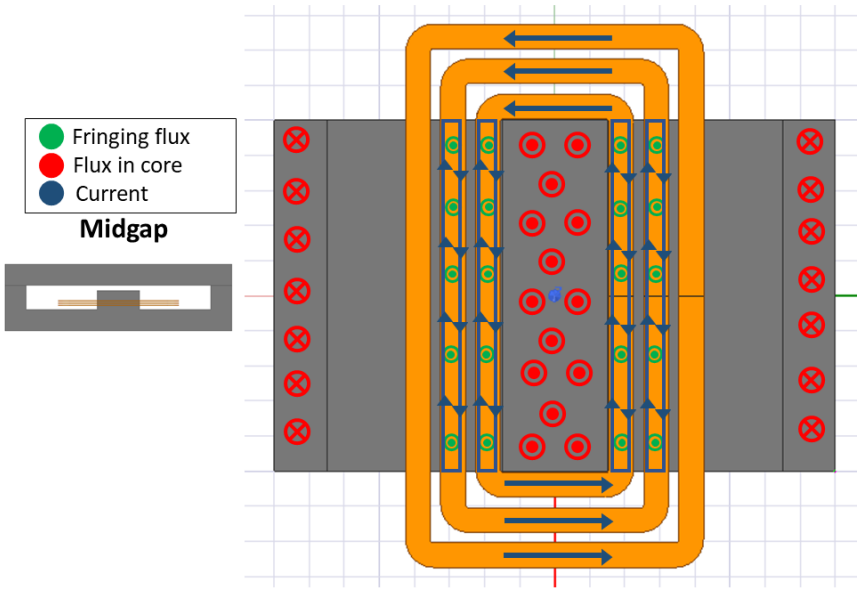


Figure D2: Eddy currents induced for midgap-core inductor.

E LTSpice model

The LTSpice-model used for the double pulse test is shown below.

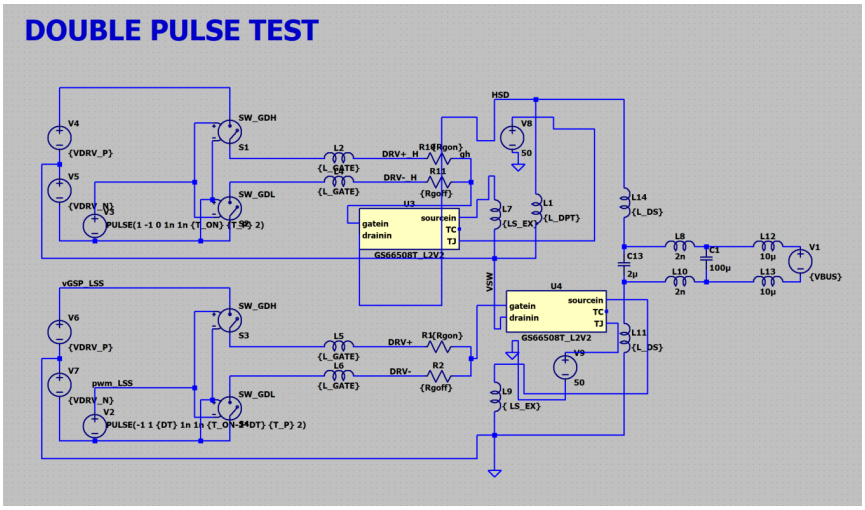


Figure E1: LTSpice model of double pulse test. Built from the GaN Systems-model [61].

Table E1: LTSpice parameters

Parameter	Description	Value
DC bus voltage	VBUS	400V
Switching current	ISW	30A
Turn-on gate resistor	RGON	8Ω
Turn-off gate resistor	RGOFF	2.2Ω
Turn-on gate voltage	VDRV_P	6V
Turn-off negative gate voltage	VDRV_N	-3V
Dead time	DT	100ns
Turn-on period	T_ON	2μs
Total period	T_P	2.5μs
Gate inductance	L_GATE	3nF
External source inductance	LS_EX	10pF
Power loop inductance inductance	L_DS	3nF

F ELK21

One of the specialization courses associated with the specialization project and master thesis was ELK 21 - Electronics for Power Conversion. This course has a goal to ”provide students with knowledge of the construction of electronic components and systems for instrumentation and control of electrical energy conversion”. This course included a mini-project, which was evaluated as a part of the grading in the course. The mini-project was associated to the specialization/master project and should present control structure, measurement methods and filter design. The mini-project report is included in its entirety in the following pages.

ELK21 - Electronics for Power Conversion

Digital control of a PFC boost converter

Ådne Finnes Engetrøen

November 2018

Contents

1 Introduction

The objective of this mini-project is to analyze the implementation of digital control in a conventional PFC boost converter.

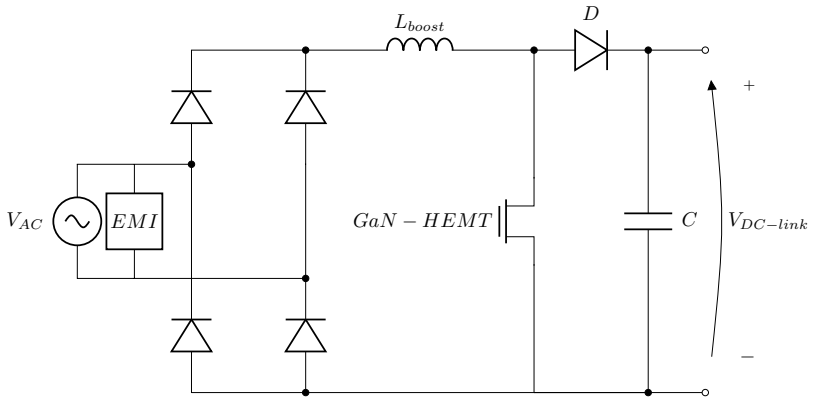


Figure 1: Bridge rectifier and DC-DC boost converter.

This mini-project is based on the specialization project which examines the possibility of utilizing GaN-transistors and a planar inductor in a conventional 1kW PFC boost converter. The PFC converter makes up one of several stages in a rectifier. Among other stages are a LLC-DCDC converter, an EMI-filter and some protection circuitry. These other stages will not be regarded in this mini-project, as it will focus solely on the PFC boost converter. Figure 1 shows the PFC converter. The input V_{AC} is from the grid and the output $V_{DC-link}$ is connected further to the LLC-DCDC converter, but will be regarded only as output. The main objective of the bigger project is to utilize the potential of GaN-transistors to reach higher switching frequencies than what is possible with conventional Si-MOSFETs. The advantage of higher switching frequency propagates through the rectifier and opens possibilities of a smaller inductor (both in inductance value and physical size). EMI-filters can also be reduced.

2 Methods and modelling

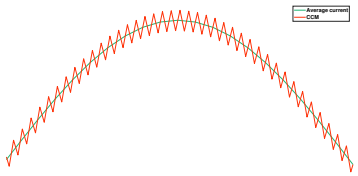
2.1 Control

2.1.1 Control purpose

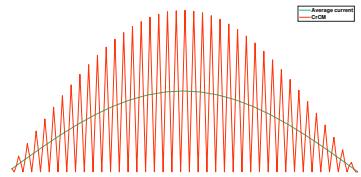
There are two control objectives in the PFC converter. The output voltage and the input current shall be controlled. The reason for making a PFC converter is to improve the power factor, and this is achieved by regulating the input current. It is also important to regulate the output voltage to be able to keep the voltage stable for different load conditions. The transistor/switch in the converter is the actuator in the control system, and it is controlled by a gate signal.

2.1.2 Control structure and operating mode

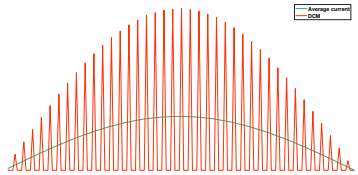
To be able to regulate both the input current and the output voltage, two control loops is needed. The output voltage is controlled by an outer loop, and the inner loop is a current control loop. There are multiple control schemes possible [1], and to choose one, operational mode of the converter must be chosen. The converter can operate in CCM (Continuous Conduction Mode), DCM (Discontinuous CM) and CrCM (Critical CM). These modes are shown in fig. 2. Some of the control schemes possible for the PFC converter are average current, peak current and hysteresis control [2]. These modes and schemes will just briefly be outlined, not thoroughly explained, as this is not main focus of the project. CCM is chosen due to its low current ripple, low EMI and its relatively simple control structure. The disadvantage of CCM is that the inductor needs to be larger, and reverse recovery losses are bigger [1]. Utilizing a GaN HEMT (High Electron Mobility Transistor) minimizes these issues by offering a high switching frequency and virtually no reverse recovery. Average current control has the advantages of constant switching frequency, low commutation noise and great input current waveform by reducing dead angle in input current [3]. The main disadvantage is that the inductor current must be sensed. Peak current control also has the advantage of constant switching frequency, but has the drawback of sub-harmonic oscillations, and a compensation ramp is needed. Hysteresis control share much of the properties of average current control, but has an additional disadvantage of variable switching frequency. Average current control is therefore preferred in this project.



(a) CCM.



(b) CrCM



(c) DCM

Figure 2: The fundamental operational modes of a PFC boost converter. The green graph is the average current and is equal in all three operation modes.

2.1.3 Measurements needed

By following the average current control scheme, with the restriction of both controlling the input current (inner loop) and the output voltage (outer loop), there are three measurements that needs to be made:

- Input voltage
- Input current
- Output voltage

The stage between the rectifying bridge and the DC-link, is nothing more than a boost DC/DC converter (step up converter). The measurements of the input voltage and current are the respective rectified values. These are both "DC-quantities", and most sensible to utilize in the control structure to avoid additional conditioning circuitry. The output voltage refers to the DC-link voltage.

2.2 Measurement ranges

2.2.1 Input voltage and current

Input voltage ranges from 185-300 V_{RMS} (from datasheet of the converters predecessor [4]) with a frequency range of 45-66 Hz. The input current will regardless of the frequency of the input voltage have some ripple from the switching and the charging/discharging of the inductor. This ripple will be at 600kHz, the same as the switching frequency. If one assumes the lowest input voltage, and an output power of 1kW with an efficiency of 95.5% [4], the highest input current can be calculated. This assumes the current to be a ripple-free sine wave. This is not the case, but will be considered further in measurement considerations.

$$I_{input,RMS} = \frac{1000W}{0.955 \cdot 185V_{RMS}} \approx 5.66A_{RMS}$$

A measurement range of 0-10A is chosen, to include the peak of the largest current with some margin. The measurement range of the voltage is chosen to be 0-500V, as this also includes the peak voltage with some margin.

2.2.2 Output voltage

The output voltage will be regulated to 400V. This DC voltage will have a ripple with twice the frequency of the input voltage [5]. It is assumed that the output voltage ripple condition is 5%, meaning that the voltage is, at steady-state, 400V $\pm$ 10V. A measurement range of 0-500V is chosen.

2.3 Digital Control

Controlling of a PFC converter can either be analog or digital. This mini-project will only consider implementation of digital control, but it is worth mentioning that analog control is also an adequate solution for a PFC converter. In analog control, the system is realized with operational amplifiers and compensator loops, while in digital control, the control structure is realized by a digital signal processor and computed binary. To implement digital control, the analog signals (physical voltages and currents) needs to be converted to digital signals (bits/bitstreams). This is done through ADC (analog-to-digital converters). The digital signals are then processed and handled digitally, before they are converted back to an analog control signal, which in this mini-project is a gate signal to control the GaN-transistor.

3 Analysis and discussion

3.1 Sensors

The input and output voltage are sensed by using voltage dividers. The resistors will have to be large to minimize the influence on the rest of the circuit. The inductor current is sensed by connecting a small resistor in the return path of the current. The small voltage drop over the resistor will represent the current in the inductor.

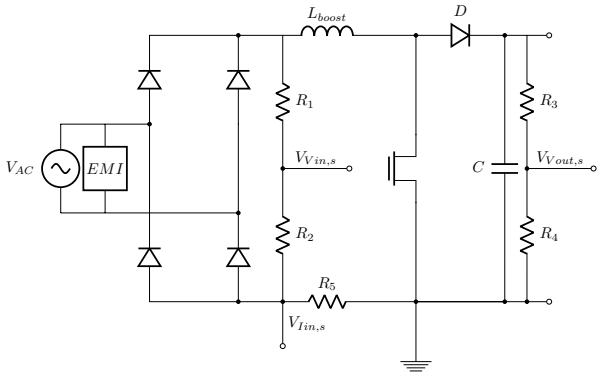


Figure 3: PFC converter with sensing resistors.

In the fig. 3 above, the voltage across resistors R_2 and R_4 represents the input and output voltage respectively. The voltage drop across R_5 represents the inductor current. Resistors R_1 to R_4 should be as large as possible while still maintaining desired precision to reduce the influence of the power circuit. Resistor R_5 should by the same logic be chosen as small as possible. The maximum input and output RMS voltages are 300V and 400V respectively. Voltages $V_{Vout,s}$ and $V_{Vin,s}$ are chosen to be in the range 0-3V. To achieve this, following criteria needs to be met:

$$\frac{R_2}{R_1+R_2} = \frac{V_{Vin,s}}{V_{in,rms}} = \frac{3V}{\cdot 300V} = \frac{1}{100} \implies R_1 = 99 \cdot R_2$$

$$\frac{R_4}{R_3+R_4} = \frac{V_{Vout,s}}{V_{out,rms}} = \frac{3V}{400V} = \frac{3}{400} \implies R_4 = 0.0075 \cdot R_3$$

For the voltage resistor network, VISHAY products are chosen[6]. R_3 is chosen to be 1MΩ, and it follows that R_4 must be 7.5kΩ. R_1 is also chosen to be 1MΩ and it follows that R_2 must be 10kΩ. All these resistors can handle up to 2W power dissipation and VISHAY guarantees less than 0.1% deviation. It also has a very low temperature coefficient of about 10 $\frac{ppm}{^\circ C}$ within the temperature range from -55°C to 125°C. The power dissipation is much less than 2W for all resistors, which will be more than enough:

$$P_{dissipation,Vin,s} = \frac{V_{in,rms}^2}{R_1+R_2} \approx 89mW$$

and

$$P_{dissipation,Vout,s} = \frac{V_{out,rms}^2}{R_3 + R_4} \approx 160mW$$

The current sensing resistor R_5 is chosen to be very small, yet precise. A $0.3m\Omega$ resistor from the company Isabellenhütte [7] is chosen. The voltage drop across this, when the current is 10A becomes (as the measurement range is 0-10A):

$$V_{Iin,s,10A} = R_5 \cdot I_{in} = 0.3 \cdot 10^{-3}\Omega \cdot 10A = 3mV$$

The highest RMS current in normal operation is about 5.66A.

$$P_{dissipation,Iin,s} = Iin, rms^2 \cdot R_5 \approx 10mW$$

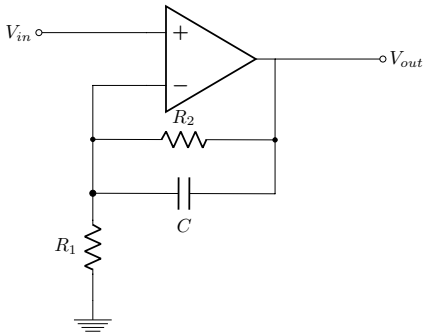
As the measured voltage drop is so small (3mV for 10A measured), the signal will be gained before entering the ADC. This will be explained in section 3.2.2.

3.2 Filtering

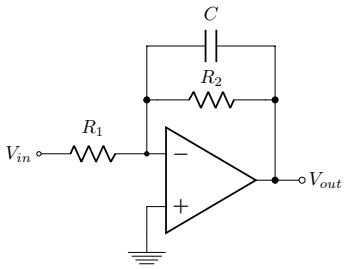
Filtering can be done either analogously or digitally. The reason for filtering is that some of the measurements contain undesirable ripples and disturbances. The filter will however affect the bandwidth of the control loops.

3.2.1 Output voltage filtering

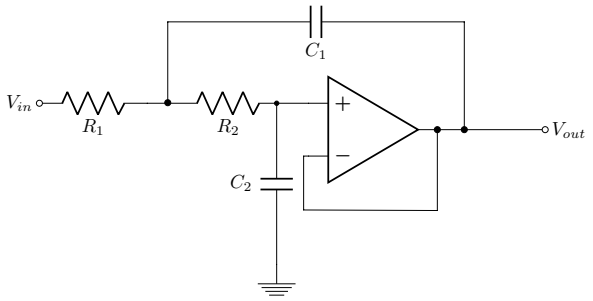
The output voltage contains a ripple of twice the grid frequency [5], i.e. the lowest ripple frequency will then be $2 \cdot 45\text{Hz} = 90\text{Hz}$. The measurement is chosen to be filtered by an analog filter, hence the ripple should not enter the DSP. An active low pass filter is therefore connected. The filter is chosen to have a cut-off frequency one decade lower than the lowest ripple frequency. This gives a cut-off frequency 9Hz. There are many low pass filter topologies to choose from, some are shown in the figure below.



(a) Non-inverting low pass filter.



(b) Inverting low pass filter.



(c) 2.order Sallen-Key low pass filter.

Figure 4: Simple 1.order low pass filters (a) and (b), and a Sallen-Key 2.order low pass filter (c).

A 2.order Sallen-Key filter is chosen. This has a transfer function [3]:

$$H_{S-K}(s) = \frac{V_{out}}{V_{in}} = \frac{\frac{1}{R_1 C_1 R_2 C_2}}{s^2 + (\frac{1}{R_2 C_1} + \frac{1}{R_1 C_1})s + \frac{1}{R_1 C_1 R_2 C_2}}$$

Choosing $R_1 = R_2 = 50M\Omega$ and $C_1 = 250p$F and $C_2 = 500p$F gives a desired cut-off frequency of

$$f_c = \frac{\omega_c}{2\pi} = \frac{1}{2\pi \cdot \sqrt{R_1 C_1 R_2 C_2}} = \frac{1}{2\pi \cdot \sqrt{50 \cdot 10^6 \cdot 50 \cdot 10^6 \cdot 500 \cdot 10^{-12} \cdot 250 \cdot 10^{-12}}} \approx 9Hz$$

Compared with the first order inverting filter with a transfer function of:

$$H_{1.order}(s) = \frac{V_{out}}{V_{in}} = -\frac{R_2}{R_1} \cdot \frac{1}{1 + R_2 C s}, f_c = \frac{\omega_c}{2\pi} = \frac{1}{2\pi \cdot R_2 \cdot C}$$

Figure 5 shows a bode plot of a 1st order filter and multiple 2nd order Sallen-Key filters. The Sallen-Key filters are tuned with different damping ratio [5], i.e. different ratios C_1/C_2. As can be seen from the plot, the 2nd order filters amplitude decays at 40dB per decade and the 1st order filters amplitude decays 20dB per decade at frequencies above f_c. This reflects the order of the filter. While the 2nd order filter suppresses the higher frequencies much better, it comes at a price. It needs more components, has a worse phase margin and worse gain margin response. A

Sallen-Key filter with lower damping ratio will have a undesirable resonant peak in the gain at the resonant frequency. With the tuning chosen in this task, the response is given by the yellow (Sallen_Key_1) line.

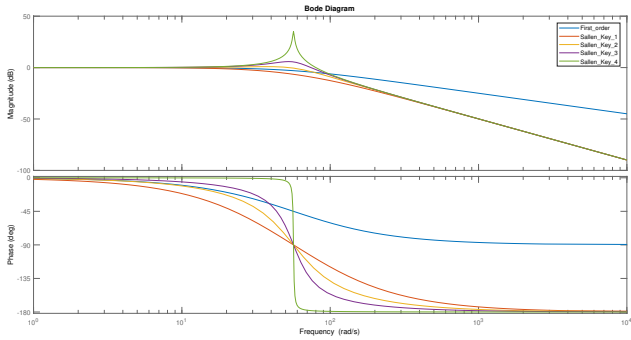


Figure 5: First order low pass filter vs. Second order Sallen-Key low pass filters

3.2.2 Input current filtering

The input current is a rectified sine wave with a ripple at the switching frequency. The switching frequency is much larger than the rectified sine frequency, $f_s = 600\text{kHz}$ and $90\text{Hz} < f_{rect,voltage} < 132\text{Hz}$, since the input frequency can vary from 45 to 66Hz. A filter with a bandwidth one decade lower than the switching (ripple) frequency is chosen. This results in a low pass filter with bandwidth 60kHz.

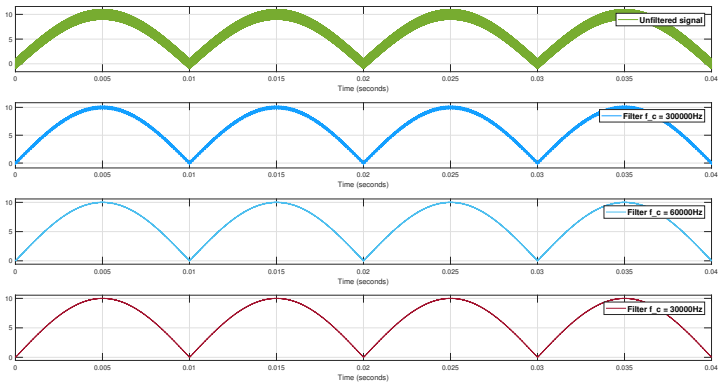


Figure 6: Signal filtered with low pass filters of different cut-off frequencies.

Figure 6 is showing the results of an ideal model of the current signal. The unfiltered signal is an ideal rectified sine wave at (twice) the grid frequency with a triangular ripple wave at switching frequency. The current and ripple amplitudes are chosen arbitrarily at 10A and 1A respectively,

to illustrate the point. As can be seen, the ripple is almost completely suppressed when filtering with $f_c = 60k$Hz.

An inverting low pass filter is chosen, and components are chosen according to section 3.2.1. As previously mentioned, the measurement signal should be gained before entering the ADC. This is done through the gain in the operational amplifier. The transfer function is

$$H(s) = \frac{V_{out}}{V_{in}} = -\frac{R_2}{R_1} \cdot \frac{1}{1 + R_2 C s}$$

Choosing $R_1 = 1k\Omega, R_2 = 1M\Omega$ and $C = 2.65p$F gives a desired cut-off frequency of

$$f_c = \frac{\omega_c}{2\pi} = \frac{1}{2\pi \cdot R_2 \cdot C} = \frac{1}{2\pi \cdot 1 \cdot 10^6 \cdot 2.65 \cdot 10^{-12}} \approx 60060Hz$$

and a gain of $\frac{R2}{R1} = 1000$.
As the signals will be handled digitally, inverted signals are no problem in theory. If this however becomes a practical problem, the signal can be inverted back again by an inverting operational amplifier.

3.2.3 Input voltage

The input voltage is considered a stiff grid voltage. It is therefore evaluated as not necessary to filter this signal. If however this signal has some harmonics or noise, the same filter philosophy as for the output voltage can be used. Other bandwidth considerations must however be done.

3.3 Analog-to-digital conversion

There are many methods available to convert a signal from analog to digital. An example is a successive-approximation ADC, which compares the signal and narrows the signal by half at each step. For instance, if the desired measured signal is 2.3V, and the measurement range is 8V, first 2.3V is compared with 4V. It is then found that it is less than 4V, and then tested against 2V, which it is larger than. It is then tested against 3V and so on, depending on the resolution. It always narrows the range by half of the last step. An other example is the sigma-delta ADC. The $\Delta\Sigma$-converter basically consists of an oversampling modulator followed by a digital/decimation filter that together produce a high-resolution data-stream output [8]. The $\Delta\Sigma$-converter have a limited sampling frequency as it uses oversampling. It is also Flash-based and have a tendency to draw a lot of power. As the sampling frequency is high in the PFC-application, successive-approximation ADCs are chosen. Advantages are low power, low cost and simple operation.

3.3.1 Sample and hold

The sample and hold circuit is used to discretize the signal. It samples with a frequency given by the switch (MOSFET). The capacitor takes some time (preferably very small) to charge up the voltage, and then holds the "sampled" value until the next sampling. The operational amplifier acts as a buffer amplifier. The capacitor needs to be large enough to keep the voltage through the hold time within an acceptable error. Both the input and output signal is analog in a sample and hold circuit. The simple circuit is shown in fig. 7. The reason for having a sample and hold circuit is to deny the signal to change during the calculating process of the ADC.

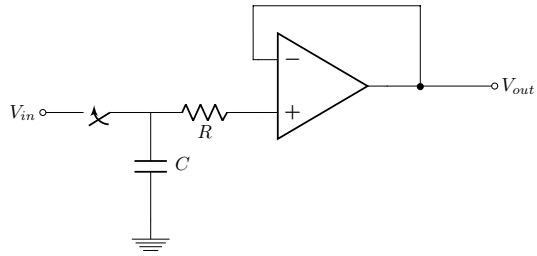


Figure 7: Sample and hold circuit.

3.3.2 Resolution and sampling frequency

The three measurement have different measurement ranges but are chosen to have the same resolution on the analog-to-digital converters. When all signals have the same resolution, the control structure does not "waste" resolutio.n The current measurement error is chosen to be less than 10mA. The current measurement range is 0-10A, and to have discrete values with an error less than 10mA, following equation must hold:

$$Discrete\ \ values \geq \frac{10A}{10mA} = 1000$$

To represent at least 1000 discrete values, 10-bit resolution is chosen. This represents $2^{10} = 1024$ values.

Measurement	Actual signal range	Measurement range	Bits	Resolution
Input voltage	0-500V	0-5V	10	$0.488V/step$
Input current	0-10A	0-3V	10	$9.77mA/step$
Output voltage	0-500V	0-5V	10	$0.488V/step$

Table 1: Measurement ranges and resolution.

Signals with greater frequency than half of the sampling frequency can affect the controller by the aliasing effect [1]. The sampling frequency in the current loop is set equal to the switching frequency, 600kHz. In addition there is a low pass filter, so aliasing effect should be no problem in the controller. For the voltages, the sampling frequency is chosen to be 5kHz, which is well above the bandwidth of the loops. The table summarize the signal ranges, resolution and measurement ranges. The measurement ranges are chosen to fit typical analog-to-digital converter voltage ranges of 0-5V and 0-3V. It is worth mentioning that the actual signal range has an upper band with "waste" of resolution. This is due to the margins chosen on top of the actual normal operation values. In practice, this means that there is a loss in ENOB (effective number of bits).

3.4 DSP, PWM and digital-to-analog conversion

The DSP contains ADC on the input and a pulse width modulator on the output. The clock frequency of the DSP and the resolution of the DPWM-signal (Digital Pulse Width Modulation Signal) is closely linked. The resolution of the DPWM-signal determines the duty cycles available. An 8-bit resolution is chosen, such that a given duty cycle can be represented with at least steps

of $\frac{1}{2^8-1} = \frac{1}{255} \approx 0.392\%$. This means duty cycles available are:

$$D = n \cdot \frac{1}{2^8-1}, \{n = 0, 1, 2...255\} = 0, 0.392\%, 0.784\%...99.61\%, 100\%$$

To have an 8-bit resolution on the DPWM with a switching frequency of 600kHz, following equation must be fulfilled:

$$\frac{f_{clock}}{f_{switch}} \geq Resolution_{DPWM} \implies f_{clock} \geq 2^8 \cdot 600 \cdot 10^3 \approx 154MHz$$

The clock frequency of the DSP needs to be larger than 154MHz. The digital to analog conversion is handled by the built in PWM, with the chosen 8-bit resolution. The PFC circuit also needs a gate driver to generate enough power to drive the transistor. This is not regarded in this mini-project.

4 Conclusion

Digital control of a PFC converter was examined and implemented. Different control schemes and structures was presented and discussed. Filters were chosen to be analog, and different filter topologies were presented. Resolutions and bandwidths are chosen in such a way that a fast inner current control loop and an outer voltage control loop is obtained. The use of digital control with DSPs are extensively in switch mode power supplies and motor drives, and multiple integrated solutions exist. The existing solutions were not regarded as the goal of this mini-project was to learn step-by-step to implement digital control in a chosen application. The software implementation is also disregarded in this project as it differs from the main scope of this project and the course ELK-21.

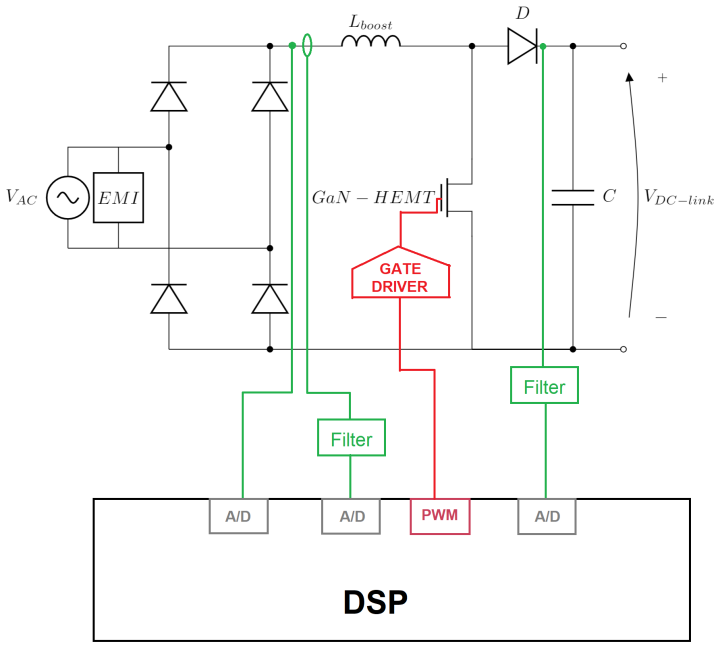


Figure 8: Illustration of possible control structure of a PFC boost converter.

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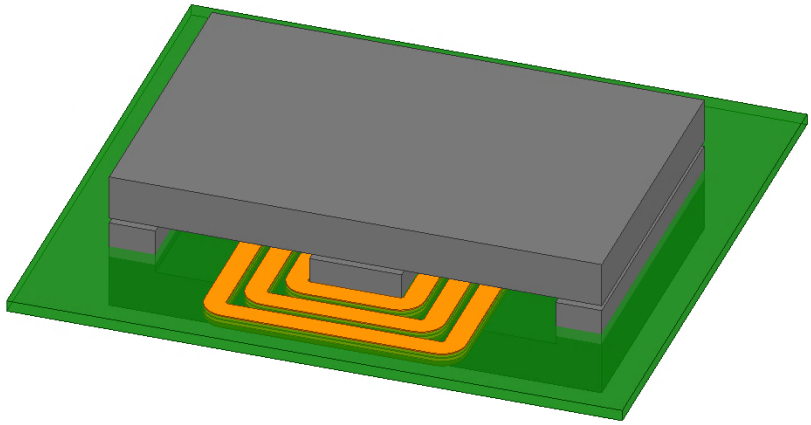
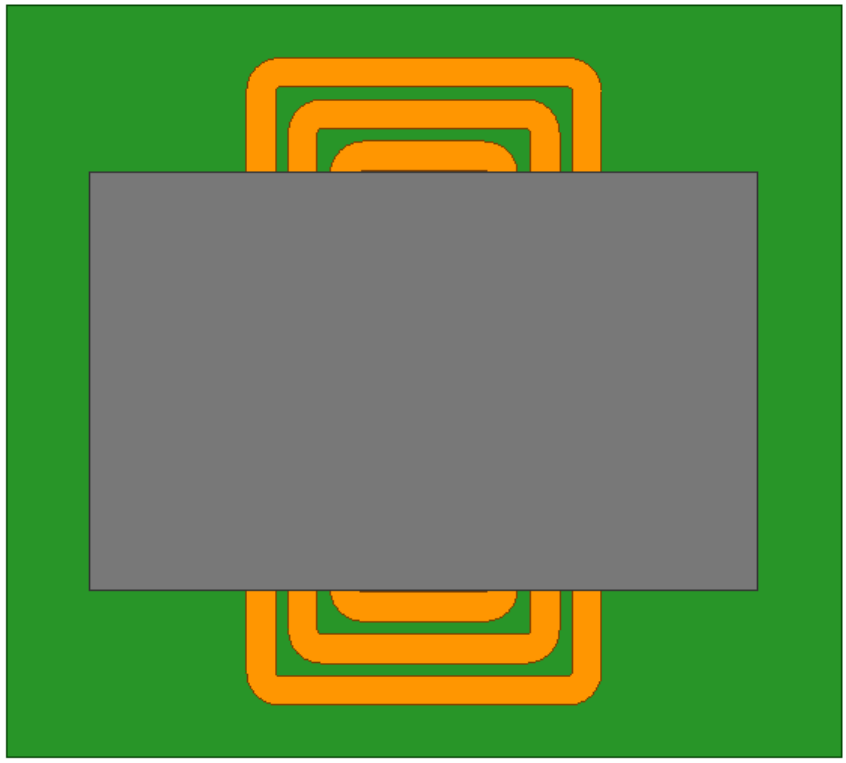
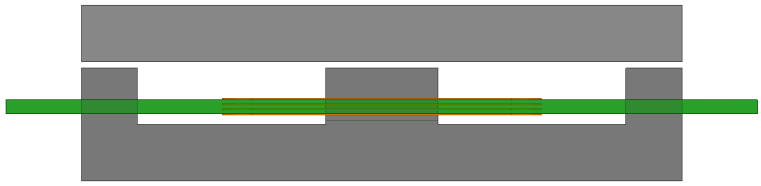
G Planar inductor design



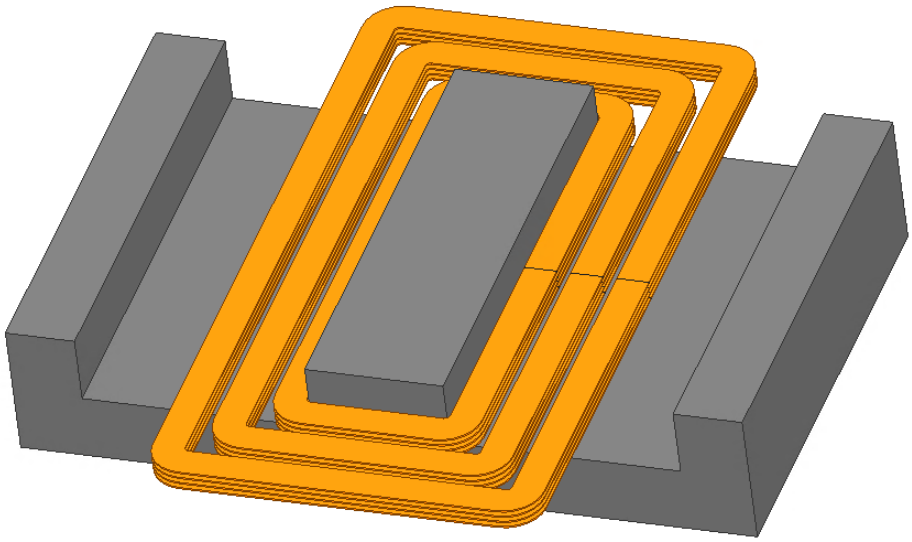
(a) 3D-view of the planar inductor.



(b) Top view of the planar inductor.



(c) Front view of the planar inductor.



(d) 3D-view without PCB.

Figure G1: Planar inductor, different views.

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A 1 kW PFC converter with GaN-transistors and planar magnetics

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