

Magnus Hirth

Hardware Acceleration of Asymmetric Elliptic Curve Cryptography

Master's thesis in Electronics Systems Design and Innovation
Supervisor: Per Gunnar Kjeldsberg
July 2019

Magnus Hirth

Hardware Acceleration of Asymmetric Elliptic Curve Cryptography

Master's thesis in Electronics Systems Design and Innovation
Supervisor: Per Gunnar Kjeldsberg
July 2019

Norwegian University of Science and Technology
Faculty of Information Technology and Electrical Engineering
Department of Electronic Systems

Asymmetric cryptography, which is also known as public-key cryptography, provide algorithms for encryption and decryption of data, digital signatures and authentication. Compared with traditional asymmetric techniques, e.g. the RSA algorithm, the elliptic curve cryptography (ECC) achieves an equivalent level of security with smaller key sizes resulting in memory as well as bandwidth savings. Computational intensive operations like scalar multiplication on elliptic curves are required during the processing of ECC protocols. Using dedicated hardware units for these operations improves execution time in an energy efficient manner. Most implementations are based on high-end CPUs and GPUs and their use in mobile devices with limited power resources such as smartcards is untested.

This assignment is a continuation of an autumn project focusing on a theoretical and practical study of ECC, including experiments and profiling using Python and C-based code versions. Based on the results from these profiling experiments, this master thesis work will test the hypothesis that a hardware accelerated ECC implementation where the entire scalar multiplication operation is optimized to minimize memory transfers leads to a more energy efficient yet generic implementation.

NTNU

Abstract

Faculty Name
IE

Master Thesis

Hardware Acceleration of Asymmetric Elliptic Curve Cryptography

by Magnus HIRTH

With the great number of mobile, battery powered devices and IoT devices being developed, there is a need for efficient, energy effective cryptography. Elliptic curve cryptography (ECC) provides high security with small key size, and seems very well suited for use in embedded, low-power systems.

The mathematics of ECC are based on set theory, performing operations on elliptic curves, usually over finite prime fields or binary fields. The security of these mathematical operations are based on the Elliptic Curve Discrete Logarithm Problem.

This thesis has explored how to design a coprocessor for accelerating elliptic curve cryptography, based on the results from a pre-study. The coprocessor designed in the thesis, ECCo, was designed for use with the ARM CM33 processor. The CM33 provides a coprocessor interface for tight integration of coprocessors, which allows instructions to be issued to connected coprocessors from software. This motivated the design of an instruction set for the coprocessor.

For the design in this thesis the operations of modular addition, modular multiplication and integer division was implemented. The design used for testing consisted of a controller, register bank and arithmetic module. A pure software implementation of elliptic curve cryptography, *libecc*, was compared to the ECCo. Results showed that the hardware accelerated design performed $3.8x - 27x$ times better than the pure software implementation.

Area estimates of the design was acquired through synthesis, using Quesasim. The ECCo accounted for 45% of the area when synthesizing ECCo+CM33. The estimates showed that the ECCo area consumption was largely dominated by the divisor (73.18% of the total ECCo area), which was implemented using the SystemVerilog division operator, "/", and no optimization in synthesis. However, the atomic operations of ECC, Modular Multiplication and Modular Addition, only occupied 1.97% and 1.92%, respectively.

Preface

This thesis is a continuation of an autumn project which explored how an hardware accelerator of elliptic curve cryptography should be implemented in order to address the shortcomings of elliptic curve cryptography in software. Part of the theory is reused from the project. The project will from now on be referred to as the pre-study.

Contents

| | |
|--|------------|
| Abstract | iii |
| Preface | v |
| 1 Introduction | 1 |
| 1.1 Asymmetric Cryptography | 1 |
| 1.2 Objective and Approach | 2 |
| 1.3 Main Contributions | 3 |
| 1.4 Structure | 3 |
| 2 Background | 5 |
| 2.1 Set theory | 5 |
| 2.1.1 Finite Field Arithmetic | 6 |
| 2.2 Elliptic Curves | 7 |
| 2.2.1 EC over \mathbb{F}_p | 7 |
| 2.2.2 EC over \mathbb{F}_{2^k} | 8 |
| 2.2.3 Point Arithmetics | 9 |
| 2.3 Scalar Multiplication | 10 |
| 2.4 Coordinate Systems | 11 |
| 2.5 ECC Algorithms | 11 |
| 2.6 Tools | 13 |
| 2.7 ARM Cortex M33 | 13 |
| 2.8 Hardware Acceleration | 13 |
| 2.9 libecc | 13 |
| 2.10 Python | 14 |
| 3 Previous Work | 15 |
| 3.1 Modular Addition Implementation | 15 |
| 3.2 Modular Multiplication Implementation | 16 |
| 3.3 FPGA Elliptic Curve Coprocessor | 18 |
| 3.4 Pre-Study | 18 |
| 4 Methodology and Architecture Design | 19 |
| 4.1 ECCo Design | 19 |
| 4.2 Choice of Algorithms | 20 |
| 4.3 Interpretation of Algorithms | 21 |
| 4.4 Test Data | 21 |
| 4.5 Verification | 22 |
| 4.6 Internal Interfaces | 22 |
| 4.7 Area Measurement | 23 |

| | | |
|----------|--|-----------|
| 5 | Implementation | 25 |
| 5.1 | ECCo Instruction Set | 25 |
| 5.2 | ECCo Architecture | 27 |
| 5.3 | Internal Interfaces | 28 |
| 5.4 | Register Bank | 29 |
| 5.5 | Arithmetic Module | 30 |
| 5.5.1 | Negation | 32 |
| 5.5.2 | Integer Division | 32 |
| 5.5.3 | Modular Addition | 33 |
| 5.5.4 | Modular Multiplication | 33 |
| 5.5.5 | Test Data | 34 |
| 5.5.6 | Verification - Arithmetic Module | 35 |
| 5.6 | Controller Module | 36 |
| 5.6.1 | Verification - Controller Module | 37 |
| 5.7 | Verification - ECCo | 38 |
| 5.8 | Software | 38 |
| 5.8.1 | ECCo Wrapper | 39 |
| 5.8.2 | Big Number library | 39 |
| 5.8.3 | Benchmark Software | 40 |
| 6 | Results | 43 |
| 6.1 | Speed | 43 |
| 6.2 | Area | 44 |
| 7 | Future Work | 47 |
| 7.1 | Instruction Set Architecture | 47 |
| 7.2 | Security | 47 |
| 7.3 | Algorithms | 47 |
| 8 | Conclusion | 49 |
| A | Test Data Python script | 51 |
| B | Internal Interfaces SV Code | 55 |
| C | Test Data | 57 |
| D | ECCo C Wrapper | 59 |
| E | ECCo Big Number library | 65 |
| F | Benchmark & Test program | 77 |

List of Abbreviations

| | |
|-------------|--|
| CM33 | ARM Cortex M33 |
| CP | CoProcessor |
| EC | Elliptic Curve |
| ECC | Elliptic Curve Cryptography |
| ECCo | Elliptic curve Cryptography Coprocessor |
| DMA | Direct Memory Access |
| DSP | Digital Signal Processor |
| DUT | Design Under Test |
| FPU | Floating Point Unit |
| FSM | Finite State Machine |
| ISA | Instruction Set Architecture |
| LSB | Least Significant Bit |
| MA | Modular Addition |
| MM | Modular Multiplication |
| MSB | Most Significant Bit |
| OOP | Object Oriented Programming |
| SIMD | Singel Instruction Multiple Data |
| SM | Scalar Multiplication |
| SV | SystemVerilog |
| SVA | SystemVerilog Assertions |
| TLS | Transport Level Security protocol |

Chapter 1

Introduction

Today, many mobile and embedded devices are being used daily, and the number of such devices are ever increasing. Embedded devices are used in many applications where security is a concern, be it for a company or personal privacy: In hospitals, smart cards (banking, SIM, access control), mobile phones, wifi routers, etc. Many of these use battery powered devices, which in addition to security issues require low power solutions. This issue motivates the exploration of low-power implementation of cryptographic algorithms. A field of cryptography which seems suited for low-power applications is Elliptic Curve Cryptography (ECC), which was introduced in the 80s by Neil Koblitz [1] and Victor Miller [2]. It has gained popularity for desktop and server use, and many of the algorithms in the Transport Level Security protocol 1.3 (TLS 1.3) are elliptic curve (EC) algorithms.

In this thesis an implementation of a coprocessor for the ARM Cortex-M33 (CM33) designed for accelerating Elliptic Curve Cryptography (ECC) is designed and tested. The work is a continuation of the autumn project on hardware acceleration of ECC, which concluded that the optimal use of a hardware accelerator were to perform the entire operation of scalar multiplication (SM) in hardware. The implementation in this thesis aims at accelerating the entire SM in hardware, and taking advantage of the features the coprocessor interface of the CM33 provides.

In this thesis *cryptosystem* is used in the same way as defined in [3]: “A cryptosystem is a general term referring to a set of cryptographic primitives used to provide information security services. Most often the term is used in conjunction with primitives providing confidentiality, i.e., encryption.”

Also, the term *big numbers* are used to refer to numbers of bit length longer than a processors word length.

1.1 Asymmetric Cryptography

Asymmetric cryptography, also known as public key cryptography, are cryptosystems which uses key pairs: A public key and a private key. The private key is only known to the owner, while the public key can be obtained by anyone without compromising the security of the system. The private key may be used to create a digital signature of a message, which allows anyone who got both the public key and the message to verify that the message has not

been corrupted, or the private key may be used to decrypt a message which has been encrypted using the public key.

The security of public key cryptography systems relies on the private key being infeasible for an attacker to compute, but not impossible given infinite time and resources. That is, public key cryptosystems are *computationally secure* and it is infeasible for an attacker to compute the private key if it requires $\approx 10^{100}$ instructions [4].

Another very common type of cryptosystems are symmetric cryptography which uses a single shared key. These systems usually require smaller key sizes and have lower power consumption compared to public key systems [5][6]. Because of this symmetric cryptosystems are preferred when encrypting large amounts of data, but since they require the shared key to be shared over a secure channel it is usually not sufficient to rely solely on symmetric key cryptography. As a possible solution to this, a public key cryptosystem was introduced in 1976 by Whitfield Diffie and Martin E. Hellman [4] which enables two parties to securely share a key over an insecure channel, thus allowing secure communication through a combination of asymmetric and symmetric cryptosystems.

This combination of symmetric and asymmetric cryptosystems are now standard and the TLS 1.3 [7] standard describes a set of cryptosystems to use for secure communication over insecure channels. A number of these systems are public key systems and with the increasing demand for high security without reducing the efficiency of low power devices such as IoT [8][9] and mobile devices [10] it seems like a good incentive to explore the possibilities of accelerating public key cryptosystems.

Further more, TLS defines a number of elliptic curve (EC) cryptosystems to use. EC cryptosystems are systems that uses mathematics based on elliptic curves and have traits that makes them suited for use in resource limited environments, such as for IoT devices. ECC algorithms are often considered safer than their non-EC counterparts [1], and this safety is provided with smaller key sizes. The benefit of smaller key sizes is that less storage for the variables of the algorithm is required and less data needs to be transferred between devices. An efficient and good implementation of ECC algorithms could potentially benefit IoT devices by reducing power consumption while still maintaining high security.

1.2 Objective and Approach

The objective of this thesis is to explore how to design a coprocessor for accelerating elliptic curve cryptography, based on the conclusion of the pre-study [11]. This thesis tries to describe how such a coprocessor could be implemented, and implement as much of the proposed design as possible. The implemented design should be benchmarked and compared to the performance of a pure software implementation, to show what benefits a coprocessor could provide.

The design approach is to consider multiple possible designs before choosing one that is appropriate for the setup used in this thesis. All modules

should be tested separately during the development process, using test data generated by software scripts, providing reliable test data.

1.3 Main Contributions

The main contributions of this thesis is the design of a flexible coprocessor aimed at accelerating elliptic curve cryptography, with the possibility of extending use to non-EC asynchronous cryptography. Detailing both the design and the design process.

Also, for this thesis a generic modular addition algorithm was designed.

A C library for big numbers was implemented. The library was designed for use with the elliptic curve coprocessor, supporting conversion to and from string representation and loading/storing to/from coprocessor registers.

1.4 Structure

Chapter 2 presents mathematical and other related background information necessary for the rest of the thesis. In Chapter 3 previous work relevant for this thesis is presented. Chapter 4 details the methodology and design choices of the coprocessor. Chapter 5 describes the implementation details of the design, and Chapter 6 presents the results of the thesis. Finally, Chapter 7 discusses thoughts on future work on the coprocessor, and Chapter 8 concludes the report.

Chapter 2

Background

This thesis is mainly concerned with elliptic curve cryptography, which are cryptosystems that uses mathematical operations on elliptic curves over finite fields. In order to give the reader a better understanding of these subjects this chapter gives a brief introduction into the mathematical field of set theory, focusing on the understanding of finite fields, and explaining the fundamentals of elliptic curves and related arithmetic operations on elliptic curves. Further, this chapter describes algorithms for implementation of modular arithmetic and elliptic curve operations in hardware, which are used later in the implementation of the coprocessor. Lastly this chapter also briefly describes the tools used.

2.1 Set theory

A *set* is (informally) a collection of objects (or elements). Sets are classified according to their mathematical properties. In this report the sets of interest are the finite fields, also called Galois fields, denoted by $GF(q)$ or \mathbb{F}_q . Finite fields are, without going into details, a set with a finite number, q , of elements where $q = p^k$ (p is prime and $k > 0$), on which the multiplication, addition, subtraction and division operations are defined [12, p.310]. In this thesis we are only interested in finite fields of integers, and, in particular, finite fields \mathbb{F}_q containing all integers from 0 up to, but not including, q . For the rest of the thesis all fields will be assumed to be of this kind. These fields can be constructed with the modulo operator, because: $x = y \pmod{q}$, where y can be any integer, x will always be in the range $0 \leq x < q$. A simple example of such a finite field is \mathbb{F}_7 , shown in Equation 2.1. It is a field with 7 elements, and can be constructed with modulo 7.

$$\mathbb{F}_7 = \{0, 1, 2, 3, 4, 5, 6\} \quad (2.1)$$

If there exists a positive integer n such that $n \cdot a = 0$ for all $a \in \mathbb{F}$ then the smallest such number is called the *characteristic* of \mathbb{F} . If no such number exist then the characteristic of \mathbb{F} is said to be zero [12, p.170]. In our example of \mathbb{F}_7 the characteristic is 7, since $7 \cdot a \equiv 0 \pmod{7}$ for $a \in \mathbb{F}_7$. The characteristic of any finite field $GF(p^k)$ is p [12, p.311]. The size of a field, q , is also called the order of the field.

Of particular interest when working with elliptic curves are finite fields where $q = p^1$, *prime fields*, and finite fields where $q = 2^k$, *binary fields*.

2.1.1 Finite Field Arithmetic

For this report we are only concerned with finite fields, which implies that all arithmetic operations in field elements are, in fact, modular arithmetic operations.

The reader is assumed to have basic knowledge of modular arithmetics, but examples of the basic operations on \mathbb{F}_7 are illustrated in Equations 2.2-2.5.

$$4 + 6 = 3 \tag{2.2}$$

$$1 - 5 = 3 \tag{2.3}$$

$$2 \cdot 5 = 3 \tag{2.4}$$

$$5 \cdot 4^{-1} = 3 \tag{2.5}$$

Equations 2.2, 2.4 and 2.5 is 3 since $10 \equiv 3 \pmod{7}$ and Equation 2.3 is 3 since $-4 \equiv 3 \pmod{7}$. Equation 2.5 is an example of modular division which is the most complicated operation of the four. In order to perform modular division one needs to find the modular inverse of the divisor, which is why modular division often is written as in Equation 2.5, avoiding the division operator, "/", to avoid confusion with integer division. [13]

To find the modular inverse of a field element the Extended Euclidean Algorithm is used [14]. It is an extension to the Euclidean Algorithm which is an algorithm for finding the greatest common divisor of two numbers, a and b [15]. The extended algorithm can further be used to find two numbers, x and y , such that:

$$ax + by = \gcd(a, b) \tag{2.6}$$

For the level of details needed in this report we can now simply say that a and b has to be co-prime ($\gcd(a, b) = 1$) and assign $b = q$, the field size. It can be shown that this leads to Equation 2.7.

$$ax \equiv 1 \pmod{q} \tag{2.7}$$

This allows us to find the inverse x of element a by solving for x ($x \in \mathbb{F}_q$). In Equation 2.5 $a = 4$ and $q = 7$, and so, we can find the inverse of 4 by solving for x in Equation 2.7:

$$4x \equiv 1 \pmod{7}$$

$$\Downarrow$$

$$x = 2$$

Equation 2.5 can then be explained by replacing 4^{-1} with the modular inverse of 4:

$$5 \cdot 2 \equiv 3 \pmod{7}$$

2.2 Elliptic Curves

Only elliptic curves over \mathbb{F}_p and \mathbb{F}_{2^m} are presented as these are the most common in ECC. Details will not be provided, only required conditions and a brief explanation of arithmetic on the curves are provided. A more detailed explanation can be found in [16]. The goal of this section is to get an intuitive understanding of what elliptic curves are, and the difference between continuous and discrete elliptic curves.

2.2.1 EC over \mathbb{F}_p

“Let \mathbb{F}_p be a prime finite field so that p is an odd prime number, and let $a, b \in \mathbb{F}_p$ satisfy $4a^3 + 27b^2 \not\equiv 0 \pmod{p}$. Then an elliptic curve $E(\mathbb{F}_p)$ over \mathbb{F}_p defined by the parameters $a, b \in \mathbb{F}_p$ consists of the set of solutions or points $P = (x, y)$ for $x, y \in \mathbb{F}_p$ to the equation:

$$y^2 \equiv x^3 + ax + b \pmod{p} \quad (2.8)$$

together with an extra point \mathcal{O} called the point at infinity.” [16]

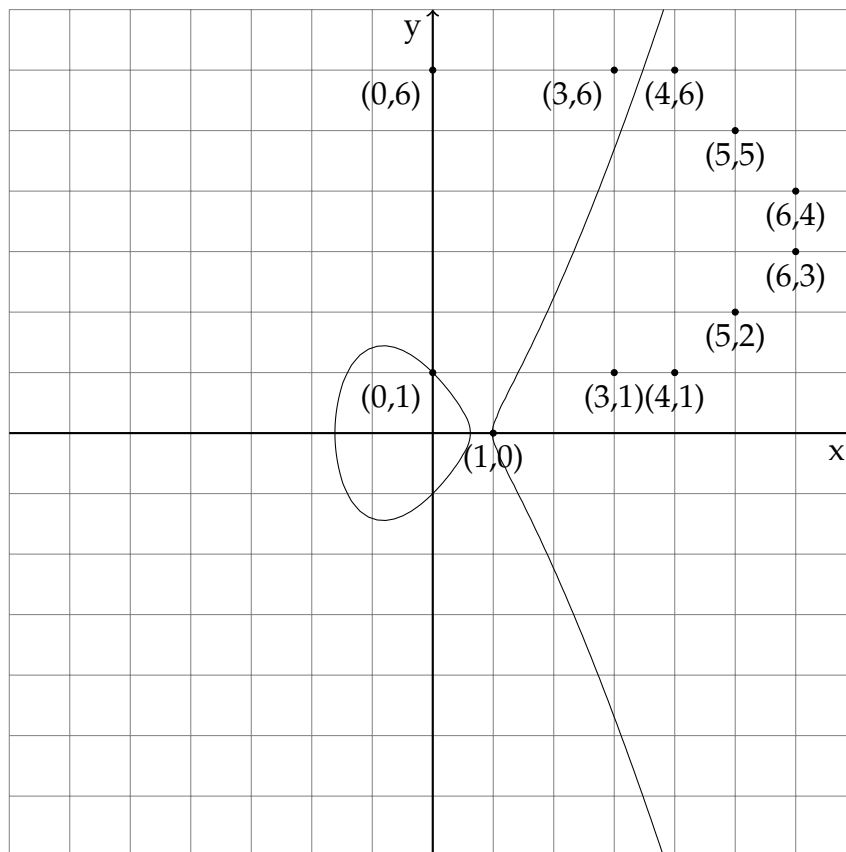


FIGURE 2.1: Illustration of $y^2 = x^3 - 2x + 1$ with the solutions to Equation 2.8 in \mathbb{F}_7 plotted.

Figure 2.1 illustrates the elliptic curve $y^2 = x^3 - 2x + 1$, $x \in [-7, 7]$. The continuous curve is the common way to illustrate an elliptic curve, over an

infinite field. However, in cryptography finite fields are used, in which case there only exists discrete solutions to the elliptic curve, and for all of the solutions the x and y values must be in \mathbb{F}_p .

The discrete solutions to the elliptic curve (Equation 2.8) are plotted in Figure 2.1, and it is apparent that only the solutions $(0,1)$ and $(1,0)$ lie on the curve itself. This is because the x and/or y values resulting in the other solutions produced a LHS or RHS value in Equation 2.8 which were ≥ 7 .

2.2.2 EC over \mathbb{F}_{2^k}

“Let \mathbb{F}_{2^m} be a characteristic 2 finite field, and let $a, b \in \mathbb{F}_{2^m}$ satisfy $b \neq 0$ in \mathbb{F}_{2^m} . Then a elliptic curve $E(\mathbb{F}_{2^m})$ over \mathbb{F}_{2^m} defined by the parameters $a, b \in \mathbb{F}_{2^m}$ consists of the set of solutions or points $P = (x, y)$ for $x, y \in \mathbb{F}_{2^m}$ to the equation:

$$y^2 + xy \equiv x^3 + ax^2 + b \pmod{p} \quad (2.9)$$

together with an extra point \mathcal{O} called the point at infinity.” [16]

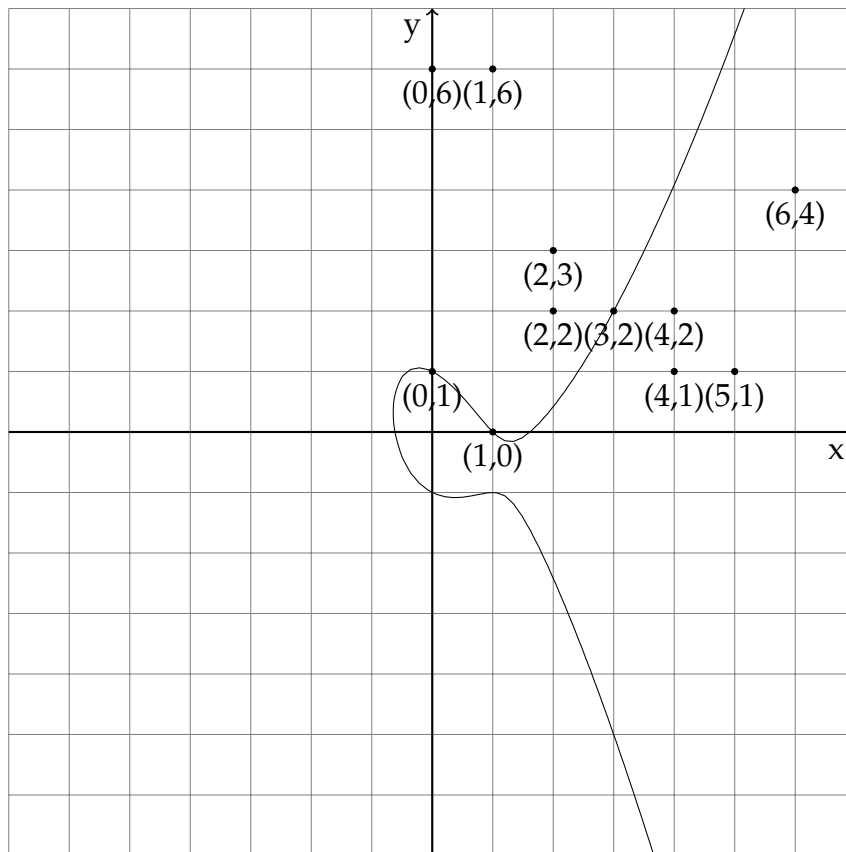


FIGURE 2.2: Illustration of $y^2 + xy = x^3 - 2x^2 + 1$ with the solutions to Equation 2.9 in \mathbb{F}_7 plotted.

Figure 2.2 illustrates the elliptic curve $y^2 + xy = x^3 - 2x^2 + 1$, $x \in [-7, 7]$. Also here both the continuous curve over an infinite field is plotted, along with the discrete solutions to the elliptic curve.

2.2.3 Point Arithmetics

In this report the arithmetic operations we are interested in on elliptic curves are point addition and point doubling. An intuitive geometric understanding of these operations were provided by Neal Koblitz [1], as illustrated in Figure 2.3.

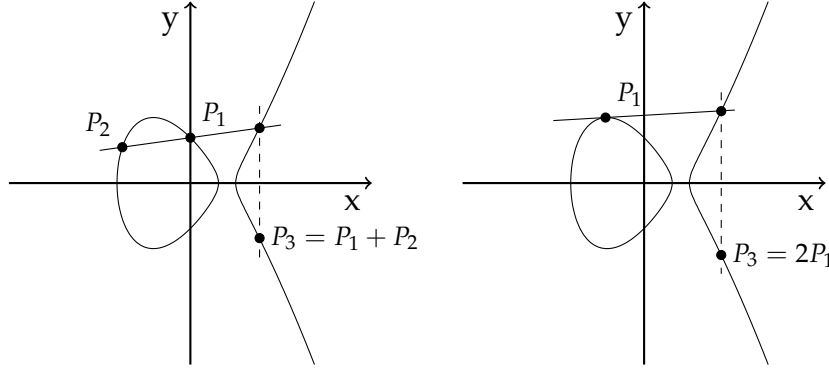


FIGURE 2.3: Illustration of elliptic curve point addition and doubling.

Let $P_1 = (x_1, y_1)$, $P_2 = (x_2, y_2)$ and $P_3 = (x_3, y_3)$ be points on an elliptic curve, where $P_3 = P_1 + P_2$. Draw a line $\overline{P_1P_2}$ through P_1 and P_2 , then their sum P_3 will be the negative of the intersection of $\overline{P_1P_2}$ and the curve.

The following equations is a result of the observations from Figure 2.3, but there is not provided enough information to prove it. For a detailed explanation see [1].

$$x_3 \equiv -x_1 - x_2 + \alpha^2 \pmod{p} \quad (2.10)$$

$$y_3 \equiv -y_1 + \alpha(x_1 - x_3) \pmod{p} \quad (2.11)$$

where

$$\alpha = \begin{cases} \frac{y_2 - y_1}{x_2 - x_1} & \text{if } P_1 \neq P_2 \\ \frac{3x_1^2 + a}{2y_1} & \text{if } P_1 = P_2 \end{cases} \quad (2.12)$$

In the case of elliptic curves over \mathbb{F}_{2^m} , when $P_1 \neq P_2$:

$$x_3 \equiv \alpha^2 + \alpha + x_1 + x_2 + a \pmod{p} \quad (2.13)$$

$$y_3 \equiv \alpha(x_1 + x_3) + x_3 + y_1 \pmod{p} \quad (2.14)$$

$$\alpha = \frac{y_1 + y_2}{x_1 + x_2} \quad (2.15)$$

and when $P_1 = P_2$:

$$x_3 \equiv \alpha^2 + \alpha + a \pmod{p} \quad (2.16)$$

$$y_3 \equiv x_1^2 + (\alpha + 1)x_3 \pmod{p} \quad (2.17)$$

$$\alpha = x_1 + \frac{y_1}{x_1} \quad (2.18)$$

Note that all of these operations require modular inversion for the division in the calculation of α , which is an expensive operation.

2.3 Scalar Multiplication

The central mathematical operation in all EC cryptosystems are the scalar multiplication, which is to multiply a scalar with a point on an elliptic curve. There are multiple different algorithms for performing a scalar multiplication. Most of these are based on the observation that any multiplication of a point and a scalar can be expressed as a combination of point additions and doublings, e.g. $11P = P + 2(P + 2(2P))$. There are many optimized algorithms for this, and in many applications it is desirable to use algorithms that have a constant execution time, for security reasons. However, in this thesis a basic algorithm, with varying execution time, is presented.

Algorithm 1 displays the pseudocode for this algorithm, called *Double-and-add (left-to-right)*.

Algorithm 1 Double-and-add (left-to-right) [17]

INPUT: Base point $P \in E_F$, scalar $k = (k_{t-1}, \dots, k_0)_2$

OUTPUT: Point $Q = k \cdot P$

```

1:  $R_0 \leftarrow \infty; R_1 \leftarrow P$ 
2: for  $i$  from  $t - 1$  downto 0 do
3:    $R_0 \leftarrow 2R_0$ 
4:   if  $k_i = 1$  then
5:      $R_0 \leftarrow R_0 + R_1$ 
6:   end if
7: end for
8:  $Q \leftarrow R_0$ 

```

In this algorithm P is the base point on the curve, which is being multiplied with the scalar k , and Q is the resulting point on the curve. t is the bit length of k . What Algorithm 1 does is to iterate through all the bits in k , starting to the left (most significant bit). First R_0 is set to the point at infinity, and R_1 to the base point P . For each iteration it performs point doubling of R_0 (doubling of point at infinity returns the point at infinity), and if the current bit i is 1 then the point addition of R_0 and R_1 is stored in R_0 (addition of a point at infinity and a point P returns the point P).

This algorithm will perform t point doublings and, in worst case, t point additions.

2.4 Coordinate Systems

Elliptic Curves are often represented using affine coordinates, (x, y) , as we have done so far, but there are several different coordinate systems with different attributes available. The purpose for using different coordinate systems is usually to increase performance. The way computation time is compared between coordinate systems is by calculating how many inversions (I), multiplications (M), and squarings (S) an addition or doubling operation require. From equations 2.10, 2.11 and 2.12 we see that in affine coordinates (\mathcal{A}) the computation times are $t(\mathcal{A} + \mathcal{A}) = I + 2M + S$ and $t(2\mathcal{A}) = I + 2M + 2S$. [18]

An alternative coordinate representation often used in practice is projective coordinates (\mathcal{P}). Here a point P is represented by a tuple (X, Y, Z) , where $x = \frac{X}{Z}$ and $y = \frac{Y}{Z}$. Using projective coordinates the computation time is $t(\mathcal{P} + \mathcal{P}) = 12M + 2S$ and $t(2\mathcal{P}) = 7M + 5S$. [18] The main motivation for using projective coordinates is reduced computation time since there is no inversion using projective coordinates, which is an expensive operation, as noted in Chapter 2.2.

There are other common alternatives for coordinates, as described in [3, p.86] and [18], but they will not be discussed here.

2.5 ECC Algorithms

Elliptic curve cryptography is commonly used for handshakes and digital signatures, such as in the Transport Layer Security (TLS) protocol 1.3 [7]. To add some perspective as to how the scalar multiplication is used in ECC this section will outline the Elliptic Curve Digital Signature Algorithm (ECDSA) [19].

The two parties involved will be referred to as *Alice* and *Bob* [20], where Alices private and public key are d_A and Q_A , respectively. Same for Bob, d_B and Q_B . For all ECC algorithms Alice and Bob have to agree on a set of parameters, D . In the case of \mathbb{F}_p these parameters are $D = (q, a, b, G, n, h)$, where:

q Are the field order (Number of elements in the field. See Chapter 2.1)

a, b Are the elliptic curve coefficients (See Equation 2.8)

G Is the base point on the curve.

n Is the order of G ; The smallest positive number such that $n \cdot G = \mathcal{O}$

h Is a number such that $h = \frac{n}{q}$

For \mathbb{F}_{2^m} the parameters are $D = (m, f(x), a, b, G, n, h)$, where $f(x)$ is an irreducible binary polynomial of degree m specifying the representation of \mathbb{F}_{2^m} .

Algorithm 2 ECDSA signature generation [19]INPUT: Domain parameters D , private key d and message m OUTPUT: Signature (r, s)

- 1: Select $k \in [1, n - 1]$
- 2: Compute $kG = (x, y)$
- 3: Compute $r = x \bmod n$. If $r = 0$ then go to step 1
- 4: Compute $e = H(m)$
- 5: Compute $s = k^{-1}(e + dr) \bmod n$. If $s = 0$ then go to step 1
- 6: Return (r, s)

If Alice wants to send a message to Bob with a digital signature to verify that the message has not been corrupted during sending, she can use ECDSA, as shown in Algorithm 2. First, a random number k are multiplied with the base point G , and the resulting x value are used to compute r , one of the two parts of the signature. Then, a hash function $H(m)$ are used to produce a hash from the message. A hash function is a one-way function, where the message is very difficult to guess for anyone who knows the hash value. The hash and Alices private key is used to produce the second part of the signature s .

Algorithm 3 ECDSA signature verification [19]INPUT: Domain parameters D , public key Q , message m and signature (r, s)

OUTPUT: Acceptance or rejection of the signature

- 1: Verify that r and s are integers in the interval $[1, n - 1]$ If any verification fails then return("Reject the signature").
- 2: Compute $e = H(m)$
- 3: Compute $w = s^{-1} \bmod n$
- 4: Compute $u_1 = ew \bmod n$ and $u_2 = rw \bmod n$
- 5: Compute $X = u_1G + u_2Q$.
- 6: If $X = \infty$ then reject the signature
- 7: Convert the x-coordinate x of X to an integer \bar{x} compute $v = \bar{x} \bmod n$
- 8: If $v = r$ then accept the signature

When Bob then receives the message and the signature from Alice he can use Algorithm 3 to verify that the message has not been corrupted during sending, and be sure that it is the exact same message as Alice sent. The proof of the verification is out of scope for this thesis, but note that the verification requires two scalar multiplications.

Relating to the TLS 1.3 [7] standard: ECDH [4] [21] is often used to pass a symmetric key between Alice and Bob, along with an ECDSA-signature which verifies that the symmetric key has not been corrupted during transmission.

2.6 Tools

For simulation and synthesis the tool Questasim [22] is used. Questasim is developed by Mentor [23]. It is a high-performance tool supporting simulation, debugging and functional coverage using HDL languages such as VHDL [24], Verilog [25], and SystemVerilog [26], including SystemVerilogs object oriented features and SVA.

2.7 ARM Cortex M33

The Cortex-M33 [27] (CM33) is a processor developed by ARM [28]. It uses the ARMv8-M [29] instruction set architecture and is developed for embedded applications, allowing low power consumption while still providing efficient security and debug capabilities. It contains features such as an FPU and DSP with SIMD instructions.

The CM33 also features a coprocessor interface, which allows for tight integration of coprocessors and accelerators with the CM33. The coprocessors are accessible from software using assembly instructions provided in the ARMv8-M instruction set [29]:

CPD, CPD2 Coprocessor data processing instructions.

MCR, MCR2 32-bit data transfer to the coprocessor.

MRC, MRC2 32-bit data transfer to the CM33.

MCRR, MCRR2 64-bit data transfer to the coprocessor.

MRRC, MRRC2 64-bit data transfer to the CM33.

2.8 Hardware Acceleration

Hardware acceleration is commonly known as a method to speed up calculations by using specialized hardware, designed for a specific task, which often supplements a general purpose CPU [30]. A very common application of hardware acceleration is graphical processing units (GPUs), which are used in virtually every desktop. Other areas where hardware acceleration is common is in the field of AI and neural networks, and relevant to this thesis: cryptography. The security of cryptosystems are based on mathematics which often require heavy computations, which usually can greatly benefit from dedicated hardware.

2.9 libecc

libecc [31] is a library implementing EC mathematics hierarchically, as illustrated in Figure 2.4. The library provides separate modules which provides natural numbers arithmetics, field arithmetics (Chapter 2.1), elliptic curve

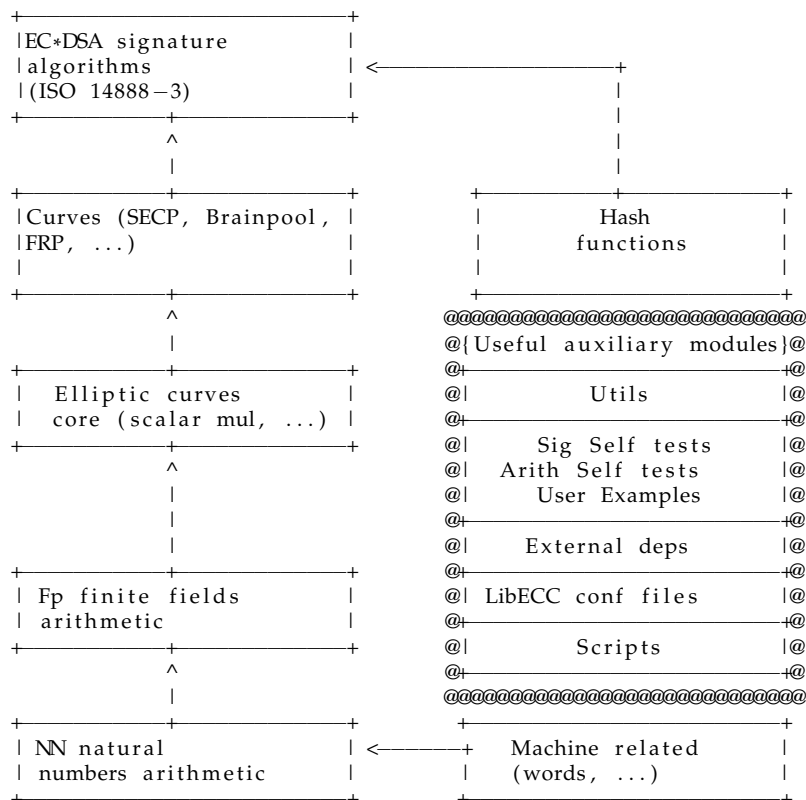


FIGURE 2.4: libecc architecture [31]

operations (Chapter 2.2), hardcoded values for curves, and implementation of the ECDSA algorithm (Chapter 2.5). Also, as seen in Figure 2.4, it provides implementation of some required hash function, self tests and some utilities, which will not be described here (see [31] for details).

Libecc does not actually implement multiple precision arithmetics but implements finite field and point arithmetics on big numbers up to a maximum integer width, which is determined at compile time. It uses projective coordinates, no dynamic memory allocation and is written without any dependencies, including the standard libc library.

2.10 Python

Python [32] is an interpreted, general-purpose programming language with dynamic type checking. Python has several interesting features which makes it flexible and easy to use, e.g. Python integers have an unlimited range [33] which makes handling of big numbers trivial. Internally Python represents big numbers as an array of fixed sized integers, but it is hidden when working with Python. Python also supports object oriented programming.

Chapter 3

Previous Work

In this chapter, existing algorithms for hardware implementations of modular addition and modular multiplication is presented. A thorough explanation and proof of correctness for these algorithms are not provided, see their respective references for more details.

An FPGA implementation of ECC coprocessors are presented, and finally the results from the pre-study is presented.

3.1 Modular Addition Implementation

Modular addition (MA) is the operation of calculating $S = X + Y \pmod{n}$, and is in effect the same operation for both addition and subtraction, if using 2's complement to represent signed numbers.

A straight forward way of implementing MA is to assume that $0 \leq A, B < n$ and do Algorithm 4 [34]. This algorithm may be performed in a single cycle with minimal control logic, depending on the timing constraints and the critical path through the additions on line 1 and 2.

Algorithm 4 Modular Addition Algorithm

INPUT: Adds A & B , modulo n

OUTPUT: Sum S

- 1: Compute $S' = A + B$
 - 2: Compute $S'' = S' - n$
 - 3: **if** $S'' \geq 0$ **then**
 - 4: $S = S''$
 - 5: **else**
 - 6: $S = S'$
 - 7: **end if**
-

The operations on lines 1 and 2 are normal addition and subtraction, and the subtraction will require the 2's complement of n to either be calculated during operation or precomputed and be an input to the HW module. Algorithm 4 is restricted to positive numbers smaller than n .

Another method was proposed in [35]. Let $n < 2^k$ and $m = 2^k - n$, where k may be the word size of the system. It is assumed that $A, B < 2^k$. Modular addition can be computed as in Algorithm 5.

Algorithm 5 Omura's Method, Modular Addition Algorithm

INPUT: Addends A & B OUTPUT: Sum S

- 1: Compute $S' = A + B$
 - 2: **if** there is a carry **then**
 - 3: $S = S' + m$
 - 4: **else**
 - 5: $S = S'$
 - 6: **end if**
-

The value of m will need to either be computed during operation or pre-computed and be an input to the HW module. Here the additions in line 1 and 3 are normal additions. If there is no carry the result is $A + B$, which may be larger than n , in which case it will be reduced later. However, if there is a carry it will be ignored, which implies that $S' = A + B - 2^k$. And the correctness of the algorithm is given by:

$$\begin{aligned}
 S &= S' + m \\
 &= (A + B - 2^k) + (2^k - n) \\
 &= A + B - n
 \end{aligned}$$

Omura's algorithm is still restricted to positive numbers, but accepts addends greater than the modulo.

3.2 Modular Multiplication Implementation

Modular multiplication (MM) is the operation of calculating $P = A \cdot B \pmod{n}$. There are many algorithms for performing MM, many of which relies on alternative number representations for higher efficiency, such as the Montgomery modular multiplication [34]

An intuitive way of calculating MM is the multiply-and-divide method [34], illustrated in Algorithm 6.

Algorithm 6 Multiply and Divide Algorithm

INPUT: Multiplicand A , multiplier B , modulo n OUTPUT: Product P

- 1: $P' = A \cdot B$
 - 2: $P = P' \% n$
 - 3: **return** P
-

This is, however, not an efficient implementation. The word size of P' will have to be twice that of A and B in order to avoid overflow, and the need to optimize the modulo reduction $\%$ will introduce unnecessary complexity to the design. Unless the product P' is needed an interleaving algorithm is usually to be preferred.

A basic interleaving algorithm is presented in Algorithm 7, where A and B are k -bit numbers between $0 \leq A, B < n$ of which A_i and B_i represents the i th bit.

Algorithm 7 Modular Multiplication Interleaving Algorithm

 INPUT: Multiplicand A , multiplier B , modulo n

 OUTPUT: Product P

```

1:  $P = 0$ 
2: for  $i = 0$  to  $k - 1$  do
3:    $P = 2 \cdot P + A \cdot B_{k-1-i}$ 
4:    $P = P \% n$ 
5: end for
6: return  $P$ 

```

Since $A, B, P < n$ it follows that

$$2P + A \cdot B_j \leq 2(n - 1) + (n - 1) = 3n - 3$$

Thus, maximum two subtractions are needed to reduce P to $0 \leq P < n$, which means the modulo operation in line 4 may be implemented as conditional subtractions.

Another efficient modular multiplication algorithm was proposed by Peter Montgomery in [36]. The result from the Montgomery algorithm is

$$P = A \cdot B \cdot r^{-1} \pmod{n}$$

where $A, B < n$ and $\gcd(n, r) = 1$. This adds overhead by requiring conversion of the result. The number of bits in A or B is less than k , and we take $r = 2^k$ [34]. The multiplication is shown in Algorithm 8.

Algorithm 8 Montgomery Modular Multiplication Algorithm

 INPUT: Multiplicand A , multiplier B , modulo n

 OUTPUT: Product $P = A \cdot B \cdot r^{-1} \pmod{n}$

```

1:  $P = 0$ 
2: for  $i = 0$  to  $k - 1$  do
3:    $P = P + A_i \cdot B$ 
4:   if  $P$  is odd then
5:      $P = P + n$ 
6:   end if
7:    $P = P / 2$ 
8: end for
9: return  $P$ 

```

Here, the division on line 7 is just a right shift, and the operations on line 3 and 5 can be combined: the LSB of P can be calculated before computing the sum on line 3.

| Coprocessor | Modular Multiplication | Modular Addition | Modular Subtraction | Point Doubling | Point Addition | Scalar Multiplication |
|-------------|------------------------|------------------|---------------------|----------------|----------------|-----------------------|
| CP 1 | 100 | - | - | - | - | - |
| CP 2 | 100 | 99 | 99 | - | - | - |
| CP 3 | 147 | 146 | 146 | 899 | 801 | - |
| CP 4 | 147 | 146 | 146 | 899 | 801 | 240000 |

TABLE 3.2: Execution times of coprocessors, in clock cycles.

3.3 FPGA Elliptic Curve Coprocessor

In [17] four different EC coprocessors were implemented and tested on an FPGA, each one implementing different arithmetic operations: CP 1 implemented modular multiplication (Chapter 2.1.1); CP 2 implemented modular multiplication, addition and subtraction (Chapter 2.1.1); CP 3 also implemented point doubling and addition (Chapter 2.2.3); and CP 4 implemented SM in addition to the arithmetic operations (Chapter 2.3).

The execution time of the implemented operations in each CP is listed in Table 3.2. The execution time is displayed in clock cycles.

The tests were performed using 256-bit values. The connected microcontroller used 8-bit word width, and the coprocessors were connected to and read the operands from RAM. Execution times includes reading operands and writing results.

3.4 Pre-Study

In the pre-study [11] possible partitioning between hardware and software for an ECC accelerator was explored. Using a pure software implementation of ECC profiling results were analyzed, trying to determine which parts of the software implementation could benefit the most from hardware acceleration.

The results showed that roughly 18.8% of execution time during testing was spent on managing the software implementation of big numbers: initialization, checking correct behavior, and handling number meta data. The conclusion was that as much as possible of an EC cryptosystem, in particular the scalar multiplication, should be performed by a coprocessor to reduce the overhead of dealing with big numbers in software.

Chapter 4

Methodology and Architecture Design

The main goal for this thesis is to implement an Elliptic Curve Cryptography Coprocessor (ECCo) which primary purpose is to accelerate the scalar multiplication in EC cryptosystems, as was the conclusion of the pre-study [11]. To perform the scalar multiplication the fundamental mathematical operations needed are modular multiplication and modular addition (Chapter 2.1.1), and integer division, when using affine coordinates (Chapter 2.4). These operations are enough to perform point doubling and point addition (Chapter 2.2.3), which allows implementation of an entire scalar multiplication (SM). The primary goal when designing the ECCo is therefore to implement the modular arithmetic operations.

The design of a coprocessor are potentially a complex and lengthy process. In the design process of the ECCo, to try to simplify this process, reusable design patterns was actively used: communication between sub-modules in the ECCo was generalized with clearly defined protocols; test data for all arithmetic operations was generated with a single Python script, utilizing Python's OOP features; and a common testbench setup was used for all modules. These design patterns are further explained in their respective methodology and implementation chapters.

This chapter discusses which choices were made during the design and testing of the ECCo, and why these choices were made. Further, it highlights important aspects of the design process, specifically where and why reusable design patterns were used.

4.1 ECCo Design

The goal of the ECCo is to be able to perform scalar multiplication. Without any restrictions from any specific systems this allows for a number of different implementations.

1. It may be designed as a SM module which only performs the SM, similar to familiar division and multiplication modules. This module could be integrated in a processor, or connected to a bus, possibly using DMA to fetch operands.

2. It may be designed as a collection of modules, each implementing an atomic operation (i.e. modular addition or modular multiplication, see Chapters 3.1 - 3.2), similar to an FPU. This would be particularly suited for tight integration with a processor, and provide a flexible design which could be used for non-EC cryptosystems which also rely on finite field arithmetic, like RSA.
3. It may be designed as a combination of the previous solutions: Providing both the atomic operations and the SM operation. This could provide both a flexible design and an optimized SM, and would also be very well suited for tight integration with a processor.

The ECCo design in this thesis will interface with the ARM Cortex M33 (Chapter 2.7) for use from software. The CM33 provides a coprocessor interface which allows for tight integration of coprocessors and issuing opcodes to the coprocessor from software. Because of this, Solutions 2. and 3. are good choices. Ideally, Solution 3. would be chosen, but due to time limitations Solution 2. is the choice for this thesis. Allowing for estimates of SM speedup with and without the coprocessor by comparing speed of atomic operations in hardware and software. This minimal implementation will also be able to give an indication on how the size of the coprocessor will compare to that of the CM33 core itself.

Since the ECCo will be controlled from software through the coprocessor interface an instruction set has to be defined for the ECCo. The instruction set proposed in this thesis is presented in Chapter 5.1. The proposed instruction set includes more than the atomic operations and data transfer; It also includes logical, comparison, and shift operations. The pre-study concluded that an entire SM should be performed in the coprocessor in order to maximize the benefit of the coprocessor. By including these flow-control and common operations the ECCo will be able to perform an entire SM without data transfer between the ECCo and CM33 during execution, even though it is being controlled from SW.

4.2 Choice of Algorithms

The two essential atomic operations are modular addition and modular multiplication, both of which can be implemented with multiple different algorithms (as described in Chapters 3.1 - 3.2). When choosing which algorithms to implement, this thesis chose the simplest algorithms in order to reduce time spent on implementation. Optimizations of the algorithms will be left for future work.

The modular multiplication algorithm implemented is the *modular multiplication interleaving algorithm* (Algorithm 7), which is described in Chapter 3.2. This algorithm requires no overhead or added complexity from number conversion, but is not the most efficient algorithm and is not designed for security.

For the modular addition Algorithm 4 is the simplest presented algorithm, but it does not support negative numbers (i.e. no subtraction) nor intermediate sums greater than $2n$. To address these limitations an improved, generic version of the algorithm was designed. The new algorithm is described in Algorithm 9.

Algorithm 9 Generic Modular Addition Algorithm

INPUT: Addends A & B , modulo n OUTPUT: Sum S

```
1: Compute  $S' = A + B$ 
2: while  $S' \geq n$  do
3:    $S' = S' - n$ 
4: end while
5: while  $S' < 0$  do
6:    $S' = S' + n$ 
7: end while
8:  $S = S'$ 
```

This algorithm can handle both positive and negative numbers, and intermediate sums larger than $2n$. Notice that the **while** loops are mutually exclusive; After the intermediate sum, $S' = A + B$, has been calculated, S' will either be reduced or increased. Clearly, the **while** loops are not synthesizable. Details on the interpretation of this algorithm are presented in Chapter 5.

4.3 Interpretation of Algorithms

The mathematical foundation of ECC requires several abstract concepts and algorithms to be "translated" into hardware, i.e. the modulo operator; multiplication over a finite field (see Chapters 2.1.1 and 3); EC point addition (Chapter 2.2.3 and 3). There are often many ways of doing this, depending on the algorithm being implemented and system requirements. A significant decision when designing the implementation is the choice between sequential or combinatorial. Combinatorial designs are much more restricted by the clock frequency of the system, and can make it harder to meet timing requirements. For this thesis the sequential approach is preferred, and state machines has been designed to implement the chosen algorithms. The reason being that a sequential implementation is more similar to a state machine representation of the system, which makes it easier to reason about the behavior of the system.

4.4 Test Data

In order to verify the results from the implementations of arithmetic operations a set of known test data is required. In the pre-study [11] test data for the scalar multiplication and point arithmetic from reliable sources was

used. This test data will be reused in this thesis. Test data for simpler operations (i.e. modular addition, division, etc.) is easy to generate using a Python script. Using a Python script will also allow generating more test data for SM and point arithmetic, since a Python implementation of these operations was written for the pre-study. The details of this script are described in Chapter 5, and full source code is listed in Appendix A.

Generation of test data contains a repeating pattern, regardless of what data is being generated: reading data from file, and writing properly formatted data to file. This can be handled by Python's OOP features (see Chapter 5.5.5 and 2.10).

4.5 Verification

In order to both verify correct behavior and to speed up the development process, the entire ECCo and each sub-module are separately tested with a testbench verifying correct behavior. In the case of the arithmetic operations this includes checking results with test data, previously mentioned in Chapter 4.4.

Design of testbenches are a repeating process, which can be simplified by following a design pattern. During the development of ECCo the chosen pattern was:

- Each testbench consisted of a module, for instantiating and connecting the design under test (DUT); An interface connected to the DUT; A package with module specific parameters; A test program.
- All signals in the DUTs interface are connected to, and controlled by, the testbench. Allowing independent testing of all sub-modules.
- The testbench uses drivers and dummy implementation of modules to control the DUT. These dummies and driver can be reused between testbenches, and can utilize system verilog's OOP features.

4.6 Internal Interfaces

During design of the ECCo a repeating design question is how to communicate between sub-modules. The sub-modules of the system are primarily modules implementing the operations defined by the instruction set, all of which may share a common communication protocol. Because of this all communication between sub-modules have been clearly defined using two interfaces: one for all communication with the register bank, another for all communication with the ECCo controller module. See Chapter 5.3 for further details.

4.7 Area Measurement

To acquire the results for area measurement the design was synthesized. The results presented are relative values, compared between synthesis of the CM33+ECCo and the CM33 only.

The speed results were measured during simulation, counting clock cycles used to execute benchmarking code of modular addition and modular multiplication, for both software and hardware implementations of those operations. Further details in Chapter 5.8.3.

Chapter 5

Implementation

This chapter describes implementation details about the work done for this thesis: proposed instruction set for the ECCo; the implementation of the ECCo and its integration with the CM33; testbench architecture and verification of the ECCo and its sub-modules; test data generation using a Python script; C implementation of the big numbers library, and the ECCo software wrapper; benchmarking of modular arithmetic operations, using the ECCo and a pure software implementation.

The logical, shift and comparison operations mentioned are not implemented in the ECCo for this thesis. The proposed instruction set includes these instructions, and discusses why they should be included in a future implementation of an elliptic curve coprocessor.

5.1 ECCo Instruction Set

The ECCo instruction set was aimed at allowing software controlled implementations of SM, while reducing data transfer between between CM33 and ECCo. The instruction set designed in this thesis is listed in Table 5.2.

The connection between these instructions and the coprocessor instructions of the ARMv8-M instruction set (Chapter 2.7) is: the **MCRR** and **MRRC** are used to for the *Load* and *Store* instructions; the **CPD** and **CPD2** instructions are used for all other instructions, where the *opc1* and *opc2* arguments are opcodes for the issued operation (see [29] for description of assembly instructions).

In the instruction set the conditional operations are not explicitly listed, the reason being that all operations has a conditional counterpart, using the **CPD2** instruction.

While further evaluation about the necessity of all instructions are required, the instruction set proposed in this thesis are based on the following reasoning:

- The arithmetic instructions are fundamental for the SM (as discussed in Chapter 4).
- The logical instructions allows functionality like masking and setting registers to zero.
- Shift instructions allows efficient divide/multiply by 2, as required in algorithms like Montgomery (Algorithm 8)

| Operation | Parameter 1 (register) | Parameter 2 (register) | Parameter 3 (register) |
|------------------------|-----------------------------------|-----------------------------------|-----------------------------------|
| Modular Multiplication | <i>Multiplicand</i> | <i>Multiplier</i> | <i>Product</i> |
| Modular Addition | <i>Addend</i> | <i>Addend</i> | <i>Sum</i> |
| Integer division | <i>Dividend</i> | <i>Divisor</i> | <i>Quotient</i> |
| Negate 2's complement | <i>Operand</i> | | <i>Result</i> |
| or | <i>Operand 1</i> | <i>Operand 2</i> | <i>Result</i> |
| and | <i>Operand 1</i> | <i>Operand 2</i> | <i>Result</i> |
| xor | <i>Operand 1</i> | <i>Operand 2</i> | <i>Result</i> |
| not | <i>Operand</i> | | <i>Result</i> |
| Left shift | <i>Operand</i> | <i>Shift size</i> | <i>Result</i> |
| Logic right shift | <i>Operand</i> | <i>Shift size</i> | <i>Result</i> |
| Arithmetic right shift | <i>Operand</i> | <i>Shift size</i> | <i>Result</i> |
| Is zero | <i>Operand</i> | | |
| Is equal | <i>Operand 1</i> | <i>Operand 2</i> | |
| Less than | <i>Operand 1</i> | <i>Operand 2</i> | |
| Greater than | <i>Operand 1</i> | <i>Operand 2</i> | |
| Load | <i>Offset</i> | | <i>Index</i> |
| Store | <i>Offset</i> | | <i>Index</i> |
| Increment | <i>Operand</i> | | <i>Result</i> |
| Decrement | <i>Operand</i> | | <i>Result</i> |
| Invert comparison | | | |
| Set signed bit | <i>Index</i> | | |
| Unset signed bit | <i>Index</i> | | |

TABLE 5.2: Instruction set for elliptic curve coprocessor.

- Comparison and conditional instructions allow control flow.
- Increment and decrement are common operations. Since immediate values are not available for the coprocessor instructions this avoids the need of using a register for increment/decrement value.
- Inverting comparison allows for comparisons like *greater or equal to*, by inverting *Less than*.
- Set/Unset are required because the signed bit is not accessible through the data transfer instructions (see Chapter 5.4 for details).

An implementation of this instruction set will therefore allow an entire scalar multiplication to be performed in the ECCo, without data transfer during execution, while still being controlled by the CM33.

5.2 ECCo Architecture

The architecture of the ECCo were based on Solution 2 in Chapter 4.1. The architecture is illustrated in Figure 5.1.

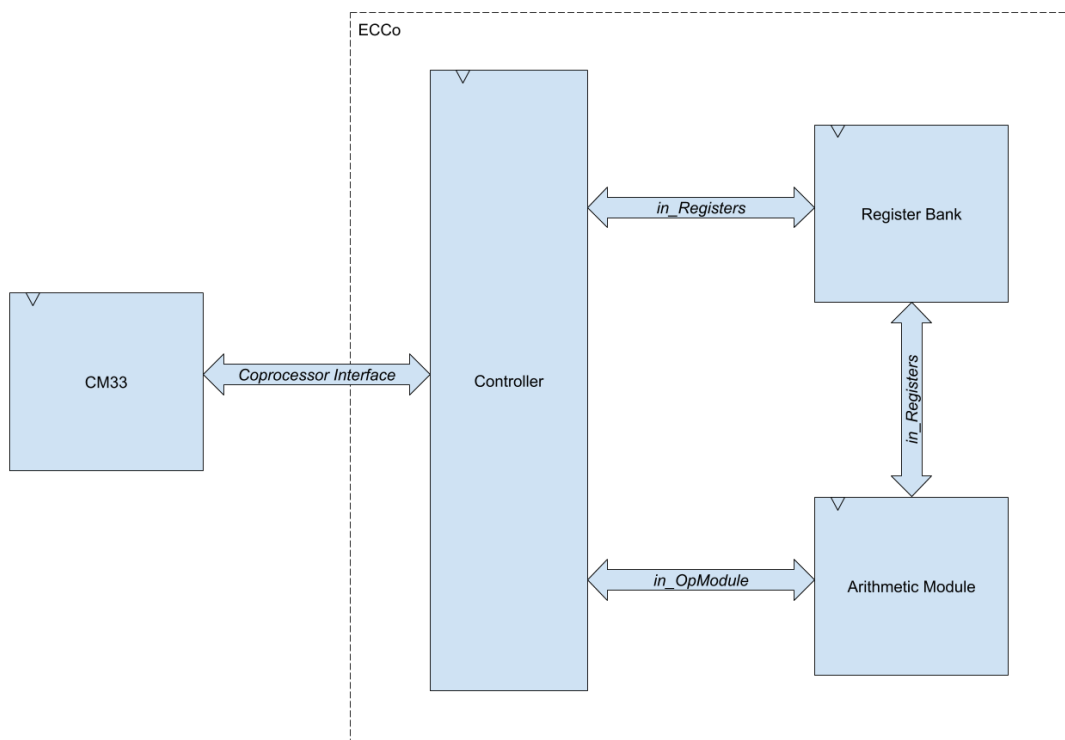


FIGURE 5.1: Architecture of ECCo, connected to the CM33 processor through the coprocessor interface.

The ECCo is connected to the CM33 through the coprocessor interface. Internally the sub-modules are connected through two interfaces, as discussed in Chapter 4.6. These interfaces are described in Chapter 5.3.

5.3 Internal Interfaces

There were used two internal interfaces in the design: *in_OpModule* which defines the protocol for issuing an operation to one of the operation-modules (a sub-module implementing one or more of the operations in the instruction set), and *in_Registers* which defines the protocol for reading from and writing to the register bank of the ECCo.

The *in_OpModule* interface uses a valid-ready protocol: when the sub-module is ready to accept a new operation a *ready* signal is asserted. An operation is issued by raising the *valid* signal, and it is accepted on the first clock cycle where *valid* and *ready* are both asserted. As long as *valid* is asserted all parameter values of the interface must be valid and stable. The interface also defines an *error* signal, which is asserted whenever an operation fails. The parameters of *in_OpModule* are:

- op1Reg** Register index of operand 1
- op2Reg** Register index of operand 2
- resReg** Register index of result
- opcode** Opcode for the requested operation

Figure 5.2 illustrates the protocol of the *in_Opmodule* interface. At t_3 an operation is accepted. The controller issues another operation at t_6 , and has to wait, while keeping the parameters valid, until the previous operation has completed. At t_9 the operation completed successfully, and the second operation is accepted. The second operation fails, as indicated by the *error* signal at t_{11} . When the following, third, operation is accepted at t_{13} , both the *ready* and *error* signals are deasserted. The SV interface implementation of *in_OpModules* is listed in Appendix B.

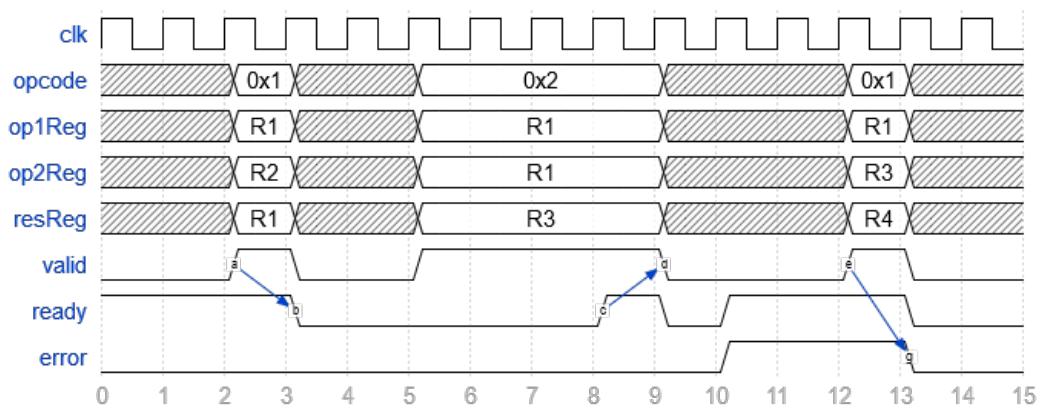


FIGURE 5.2: Illustration of *in_OpModule* communication protocol.

Because of this generalization of communication with all operation sub-modules, a common state machine is implemented as the controller in all of them, which is illustrated in Figure 5.3.

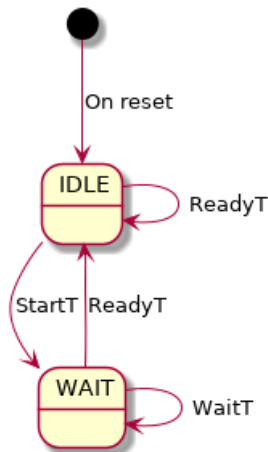


FIGURE 5.3: Illustration of FSM implementing the *in_OpModule* communication protocol.

In the state machine in Figure 5.3 **StartT**, **ReadyT**, and **WaitT** are names of possible transitions. This is because the output of the state machine are determined by both state and input. In *IDLE* the *ready* signal is asserted, and the value of *error* may be either 0 or 1. In *WAIT* both *ready* and *error* is always 0.

The *in_Registers* interface exposes all the registers directly, for reading. To write, the signals *enable*, *register*, and *data* are used, indicating when to enable writing, which register to write to, and the write data, respectively. The SV interface implementation of *in_Registers* are listed in Appendix B.

5.4 Register Bank

The register bank is a module containing 16 registers, which may be read from and written to. The choice of 16 registers was done based on a limitation from the CM33 which required the indexing of register using no more than 4 bits. However, it may not be necessary with these many registers to perform the SM. An evaluation of necessary number of registers are left for future work, considering both the area usage of the register bank and required number of registers for the SM implementation. All 16 registers are exposed for reading through the *in_Registers* interface. Writing is implemented following the *in_Registers* protocol.

The registers are of width $WORD_WIDTH + 1$, e.g. if the ECCo is instantiated with a word width of 256-bit the word width of the registers will be 257-bit. The reason for this is that parameter values from standards such as [37] and [38] require $WORD_WIDTH$ -bits to represent positive values. Because of this the signed bit of registers are manipulated through dedicated instructions, to avoid using a 64-bit data transfer to access the signed bit.

| Register Name | Register Index | Writable | Readable |
|-----------------|----------------|----------|----------|
| CR0 | 0 | X | X |
| CR1 | 1 | X | X |
| ... | ... | ... | ... |
| CR13 | 13 | X | X |
| Modulo Register | 14 | X | X |
| Status Register | 15 | | X |

TABLE 5.4: List of ECCo registers.

Table 5.4 lists all registers in the register bank. There is only two non-general registers: the modulo register and the status register. The modulo register is used for storing the modulo during modular arithmetic operations. The status register is read-only (all writing to it is done inside the register bank) and contains information about the current status of the ECCo:

Bit 0 Comparison result bit.

Bit 1-15 Active bits. These are reserved for future use in an asynchronous design, for indicating which operation modules are currently working and which are idle.

Bit 16-30 Signed bits. The signed bits of register 0-14, respectively.

Bit 31- Unused.

5.5 Arithmetic Module

The arithmetic operations sub-module is implemented as a controller implementing the *in_OpModule* protocol and wrapping the modules implementing each individual arithmetic operation: negation, integer division, modular addition, and modular multiplication. In Figure 5.4 the block diagram of the arithmetic module are shown. The arithmetic controller implements the *in_OpModule* FSM, as illustrated in Figure 5.3.

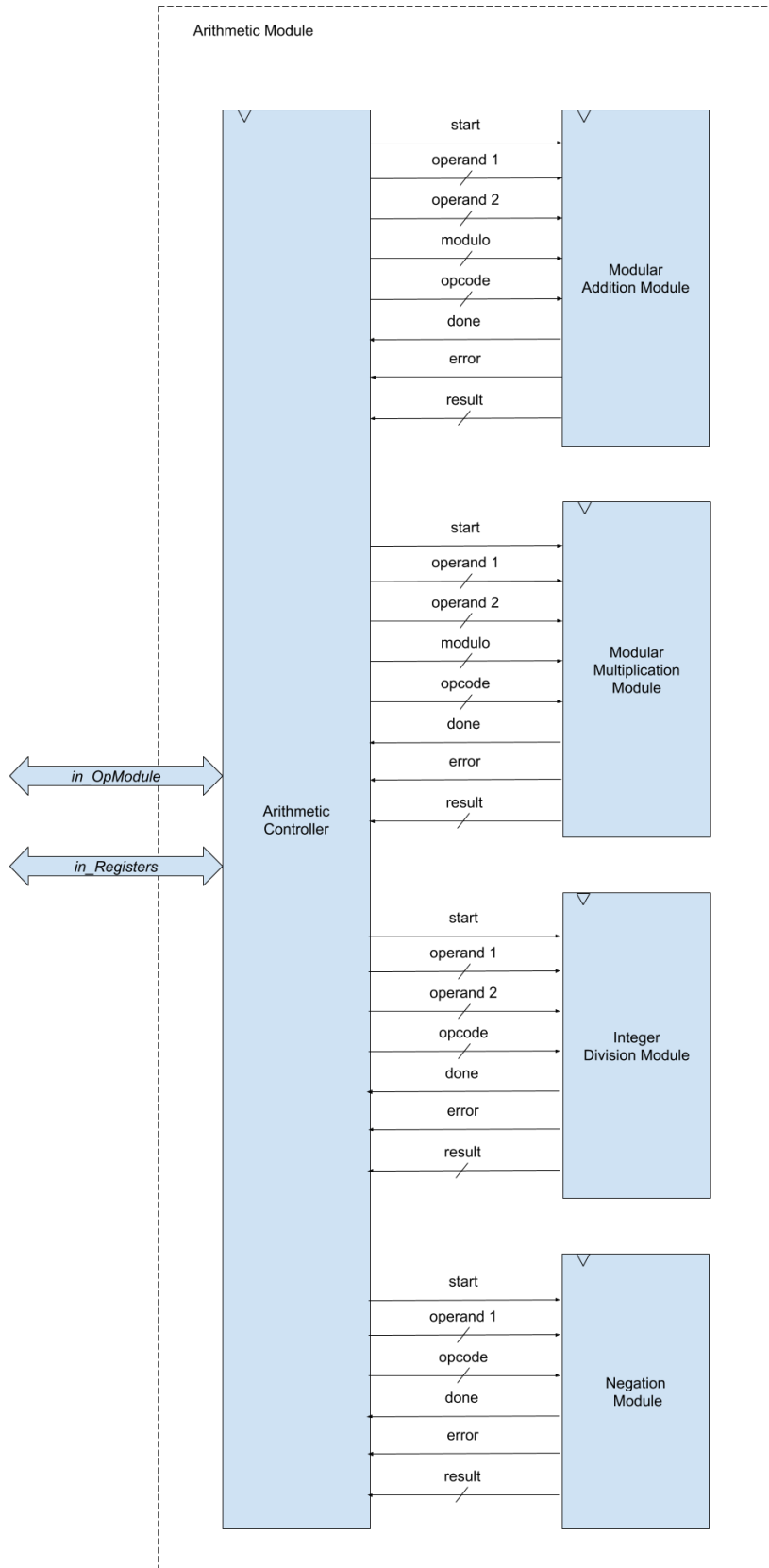


FIGURE 5.4: Block diagram of arithmetic module.

5.5.1 Negation

The negation operation is a single cycle operation which is straight forward to implement, and performs a 2's complement negation of the operand. It is continually calculated:

```
1      assign res = ~(operand) + 1;
```

5.5.2 Integer Division

The integer division is a necessary operation when using Affine coordinates, but its implementation is not very interesting in regards to the ECCo. Therefore, it was initially implemented using an opensource design from OpenCores [39]. However, this design did not function properly and instead integer division was implemented using the SystemVerilog division operator, "/".

It is also a single cycle operation, but requires divide-by-zero detection and handling of negative numbers: If the divisor and/or dividend is negative its positive 2's complement is used in the division and the sign of the result is calculated using basic algebra rules, as shown in Listing 5.1.

```
1 // MSB of dividend (op1) and divisor (op2)
2 logic msbOp1, msbOp2;
3 // Internal signals
4 logic [WORD_WIDTH:0] intOp1;
5 logic [WORD_WIDTH:0] intOp2;
6 logic [WORD_WIDTH:0] intRes;
7
8 // The division is continuously calculated.
9 assign divideByZero = (op2 == 0);
10 assign intRes = intOp1 / intOp2;
11 assign msbOp1 = op1[WORD_WIDTH];
12 assign msbOp2 = op2[WORD_WIDTH];
13
14 always_comb begin
15     intOp1 = op1;
16     intOp2 = op2;
17     if ( msbOp1 && msbOp2 ) begin
18         intOp1 = (~op1) + 1;
19         intOp2 = (~op2) + 1;
20     end
21     else if ( msbOp1 )
22         intOp1 = (~op1) + 1;
23     else if ( msbOp2 )
24         intOp2 = (~op2) + 1;
25 end
26
27 always_ff @(posedge ck)
28     res <= (msbOp1 ^ msbOp2) ? (~intRes) + 1 : intRes;
```

LISTING 5.1: Division SV implementation.

5.5.3 Modular Addition

The modular addition is implemented using Algorithm 9, designed for this thesis, as discussed in Chapter 4.2. This algorithm is interpreted as illustrated by the FSM in Figure 5.5, and the datapath in Figure 5.6. The transitions in the illustration are referred to by name.

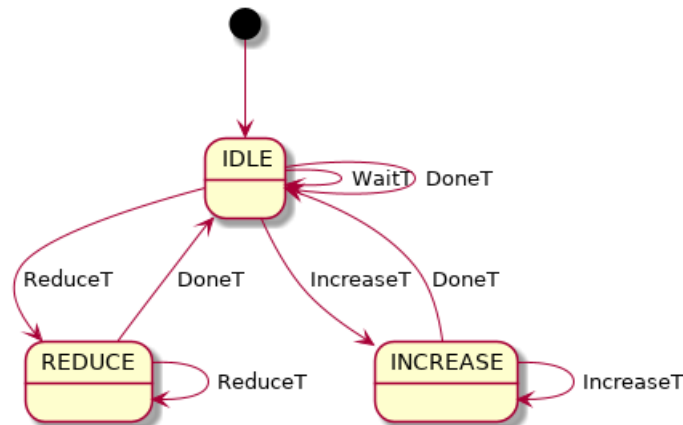


FIGURE 5.5: FSM interpretation of Generic Modular Addition Algorithm.

DoneT Transition to *IDLE* when an addition has finished. Asserting *done* for one cycle.

WaitT Transition in *IDLE* when not performing an operation.

ReduceT Transition to *REDUCE* when the intermediate sum is greater than the modulo, and need to be reduced to $0 \leq Sum < Modulo$.

IncreaseT Transition to *INCREASE* when the intermediate sum is less than 0, and need to be increased to $0 \leq Sum < Modulo$.

If initially: $op1 + op2 < mod$ then the calculation only takes one cycle to complete, or else *op1 mux* selects the intermediate result as operand 1 and *op2 mux* selects either mod or $-mod$ as operand 2, depending on if the state is *INCREASE* or *REDUCE*, respectively. In worst case the addition could take $2^{WORD_WIDTH} - 1$ cycles to perform, calculating $((2^{WORD_WIDTH} - 1) + 0) \% 1$.

5.5.4 Modular Multiplication

The modular multiplication is implemented using the Algorithm 7, as discussed in Chapter 4.2. This algorithm is interpreted as illustrated by the FSM in Figure 5.7, and the datapath in Figure 5.8. The transitions in the illustration are referred to by name.

DoneT Transition to *IDLE* when an multiplication has finished. Asserting *done* for one cycle.

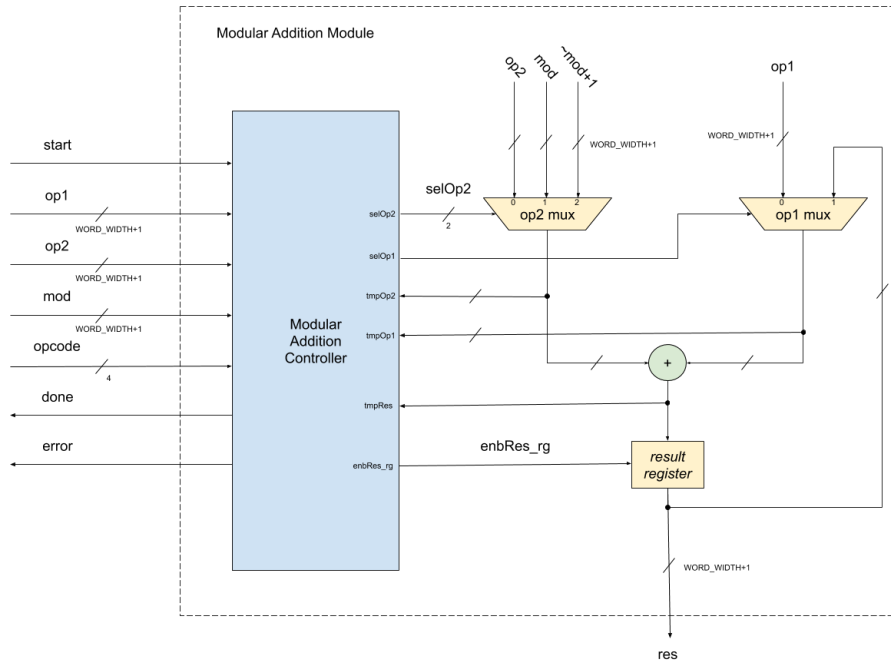


FIGURE 5.6: Block diagram of modular addition module.

WaitT Transition in *IDLE* when not performing an operation.

AddT Transition to *ADD* when calculating the sum of $2 \cdot P + A \cdot B_{k-1-i}$ (as described in Chapter 3.2).

ReduceT Transition to *REDUCE* when the intermediate sum is greater than the modulo, and need to be reduced to $0 \leq Sum < Modulo$.

ReduceDoneT Transition to *REDUCE_DONE* when the intermediate sum is greater than the modulo, and need to be reduced to $0 \leq Sum < Modulo$, before finishing to operation.

The modular multiplication always has an execution time of at least *WORD_WIDTH* cycles since it has to iterate through all bits of *op2*, except the signed bit. None of *op1*, *op2*, or *mod* are allowed to be negative. The emphartial product mux selects the current value of $A \cdot B_{k-1-i}$. *op1 mux* and *op2 mux* selects whether to calculate $2 \cdot P + A \cdot B_{k-1-i}$ or to reduce the intermediate result.

5.5.5 Test Data

Test data was generated using a python script, which was written with an architecture as illustrated in Figure 5.9. The test data solutions are created by python operators, as shown in Listing 5.2.

```

1 def modular_addition(op1: int, op2: int, mod: int) -> int:
2     return (op1 + op2) % mod
3
4 def modular_multiplication(op1: int, op2: int, mod: int) ->
   int:

```

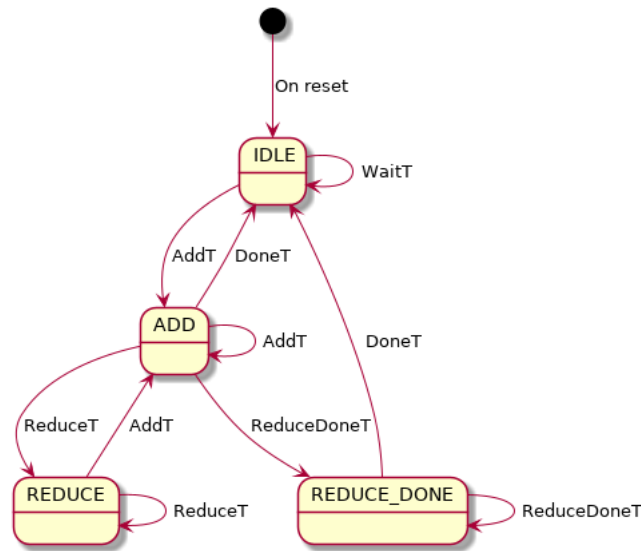



FIGURE 5.7: FSM interpretation of Multiply and Divide Algorithm.

```

5     return (op1 * op2) % mod
6
7     def integer_division(op1: int, op2: int) -> int:
8         if op1 < 0 and op2 < 0:
9             res = abs(op1) // abs(op2)
10        elif op1 < 0:
11            res = -(abs(op1) // op2)
12        elif op2 < 0:
13            res = -(op1 // abs(op2))
14        else:
15            res = op1 // op2
16        return res
  
```

LISTING 5.2: Test data solution calculations.

Notice the integer division `//` does not handle division of negative numbers correctly. Instead any negative numbers are negated, and basic algebra rules are used to determine the sign of the result, just as it is implemented in hardware.

The script source code is listed in Appendix A. Test data values used for verification are listed in Appendix C.

5.5.6 Verification - Arithmetic Module

The arithmetic module was tested using a TB design as illustrated in Figure 5.10. The test program communicates with the arithmetic module through an *in_OpModule* driver, and controls and verifies the register content during testing through a dummy register bank, connected to the arithmetic module.

During testing the values listed in Appendix C were used to verify correct results from arithmetic operations.

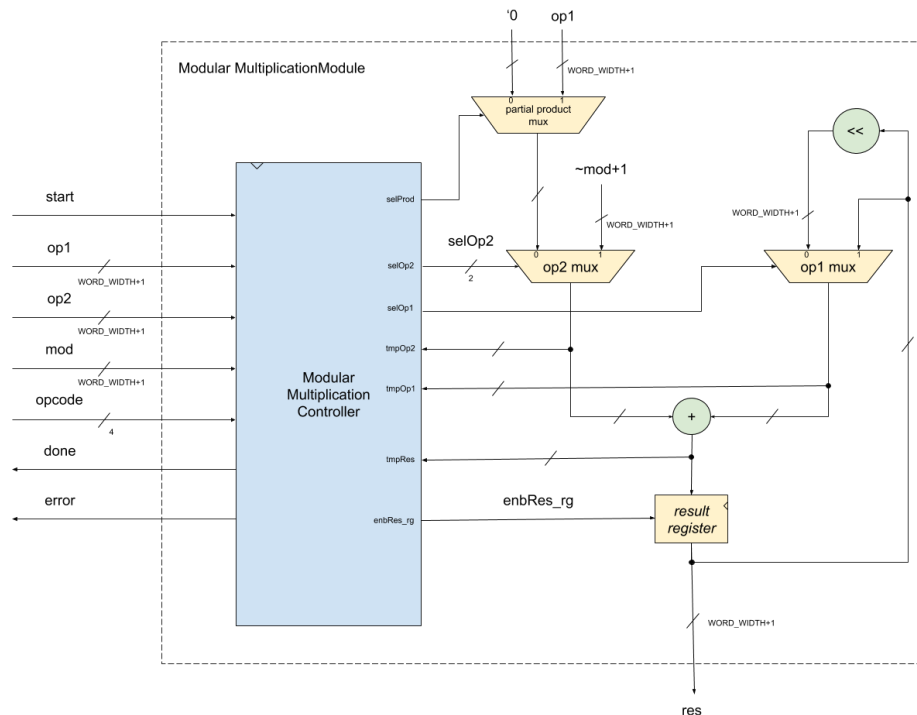


FIGURE 5.8: Block diagram of modular multiplication module.

5.6 Controller Module

The controller's primary purpose is to handle communication with the CM33 using the coprocessor interface, the FSM in Figure 5.11 illustrates the implemented state machine which does this. This is a synchronous design: the controller will wait for any multicycle operation to finish before signaling to the CM33 that it is ready to accept further instructions.

The outputs of the FSM are the coprocessor interface signals *valid* and *error*, and an internal *valid*, which are used in the *in_OpModule* interface. The transitions in the illustration are referred to by name. The output signals of the FSM are determined by both state and input, easiest described as the set of all possible transitions:

RyT - ready transition Transition to *READY*, with *ready* asserted and *error* deasserted, waiting for an instruction to be issued.

ET - error transition Transition to *READY*, with both *ready* and *error* asserted. May be from a write error, read error, data processing error or an invalid instruction being issued.

WaT - wait transition Transition to *WAIT* when *valid* is asserted and a data processing operation is issued.

WaWT - wait wait transition Transition to *WAIT*, from *WAIT*, while current data processing operation is not yet finished.

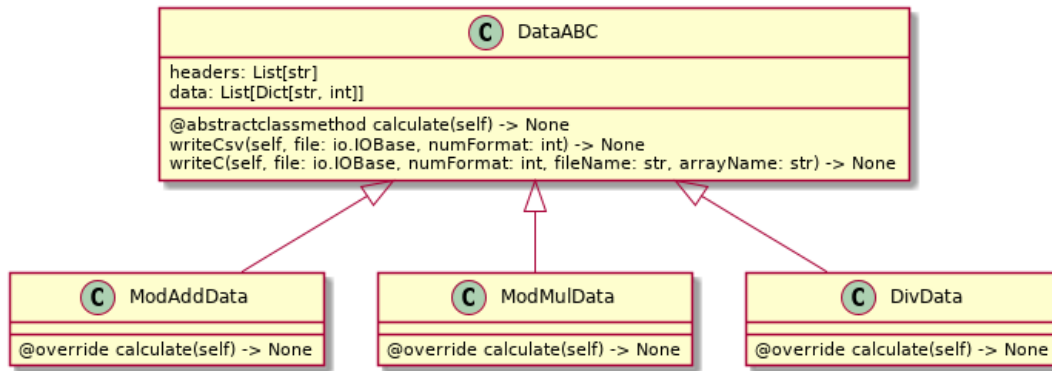


FIGURE 5.9: Class diagram of python script generating test data.

WaRT - wait ready transition Transition to *WAIT*, from *WAIT*, when a data processing operation finished successfully and *valid* is asserted, requesting a new data processing operation immediately.

WaET - wait error transition Transition to *WAIT*, from *WAIT*, when a data processing operation finished with error and *valid* is asserted, requesting a new data processing operation immediately.

ReT - read transition Transition to *READ*, when the processor wants to read from a coprocessor register.

ReRT - read ready transition Transition to *READ*, from *WAIT*, when a data processing operation finished successfully and *valid* is asserted, requesting a data transfer operation (read) immediately.

ReET - read error transition Transition to *READ*, from *WAIT*, when a data processing operation finished with error and *valid* is asserted, requesting a data transfer operation (read) immediately.

WrT - write transition Transition to *WRITE*, when the processor wants to write to a coprocessor register.

WrRT - write ready transition Transition to *WRITE*, from *WAIT*, when a data processing operation finished successfully and *valid* is asserted, requesting a data transfer operation (write) immediately.

WrET - write error transition Transition to *WRITE*, from *WAIT*, when a data processing operation finished with error and *valid* is asserted, requesting a data transfer operation (write) immediately.

5.6.1 Verification - Controller Module

The testbench setup for the verification of the controller module is illustrated in Figure 5.12.

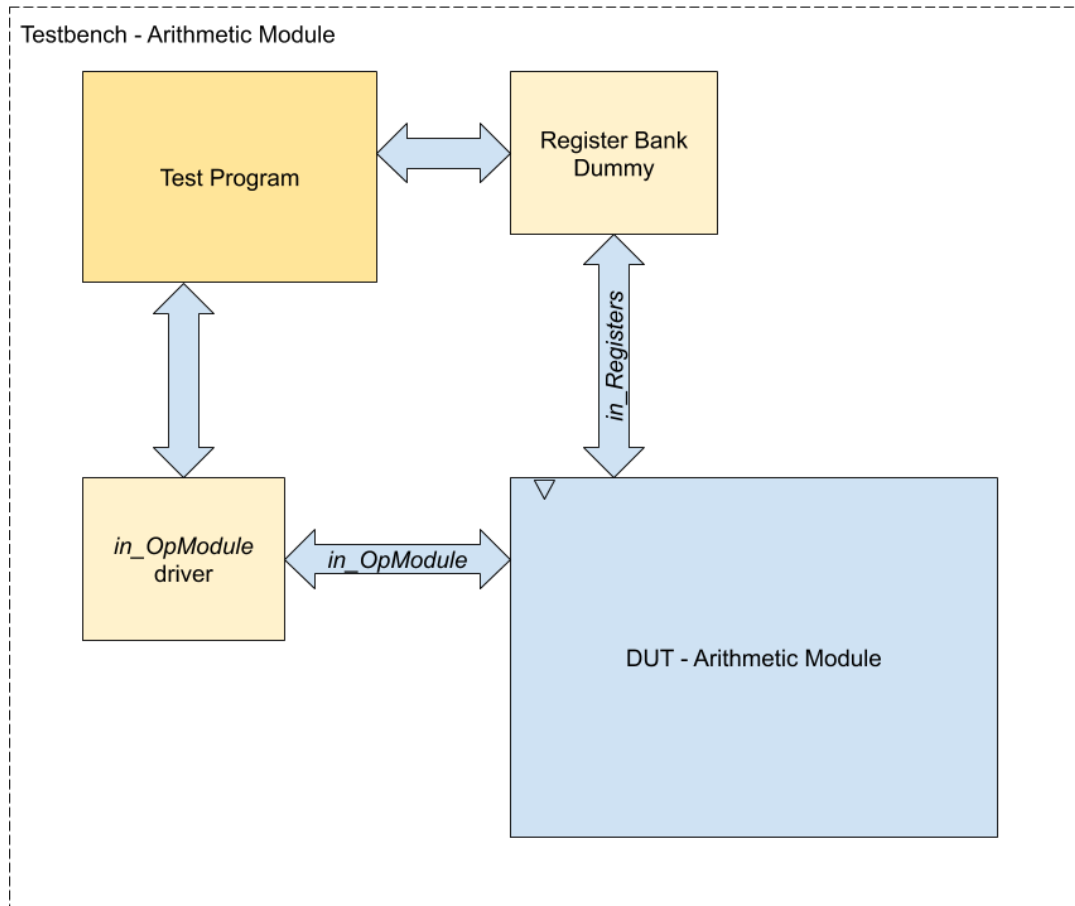


FIGURE 5.10: Block diagram of Arithmetic Module TB.

Operation module dummies for the arithmetic, logical, comparison and shift modules are connected to the controller, and controlled by the test program. A dummy register bank is connected to the controller, and the controller is tested using a coprocessor interface driver for communication.

5.7 Verification - ECCo

The testbench setup for verification of the entire ECCo is illustrated in Figure 5.13.

A coprocessor interface driver is used to communicate with the ECCo, and the test values from Appendix C are used to check for correct behavior of the implemented operations.

5.8 Software

For this thesis three software components were implemented: a wrapper for the coprocessor interface instructions; a big number library for use with the ECCo; and a benchmarking program.

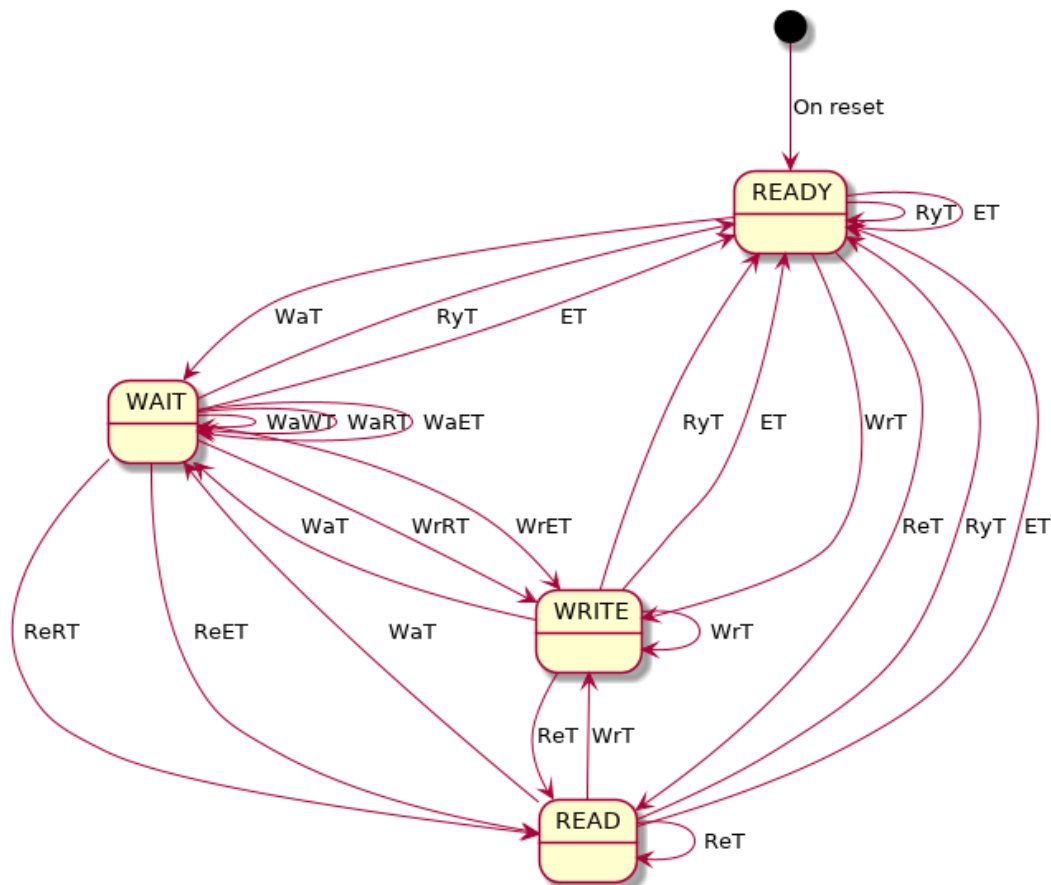


FIGURE 5.11: FSM of ECCo controller module.

The big number library and ECCo wrapper were used to verify that communication with the ECCo using the coprocessor interface was working as expected. To verify correct behavior of the ECCo controller and the implemented operations the test data from Appendix C were used. The source code of the test programs used for verification are listed in Appendix F.

5.8.1 ECCo Wrapper

The ECCo wrapper was implemented to simplify calling the ECCo from C using the coprocessor interface. The coprocessor instructions of the ARMv8-M instruction set have to be called from assembly, using string literals to refer to coprocessor registers and opcodes. Therefore a series of macros were created for all the instructions in the proposed instruction set (Table 5.2). The code for the wrapper is listed in Appendix D.

5.8.2 Big Number library

When using the ECCo some minor handling of big numbers in software are still required. For this a big number library was implemented for use with the ECCo. The functionality it provided was:

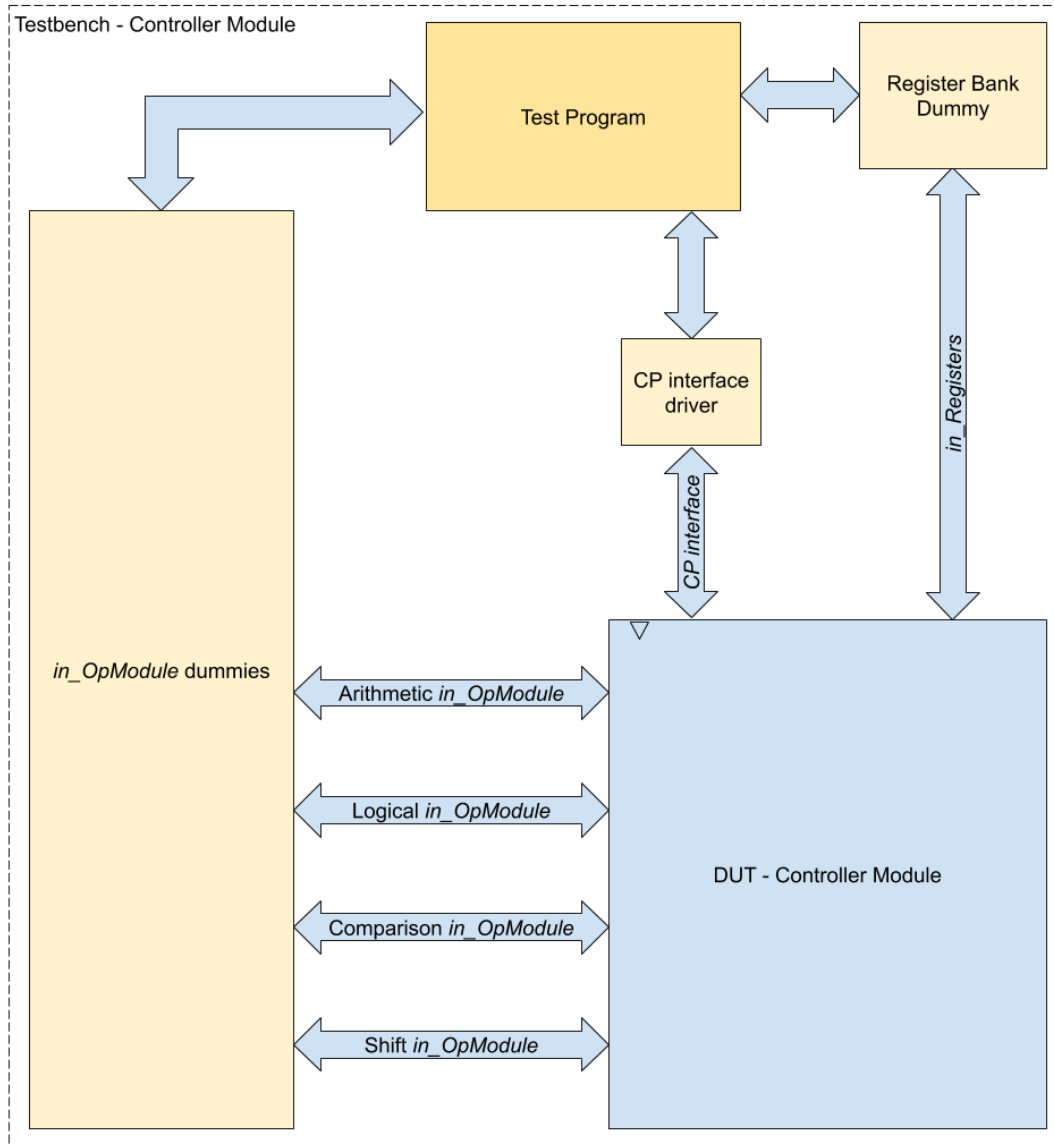


FIGURE 5.12: Testbench setup for verification of the controller module.

- Converting to and from number strings on hexadecimal format.
- Comparing two numbers.
- Loading a number to an ECCo register.
- Storing a number from an ECCo register.
- Some other convenient functionality.

The source code for the big number library is listed in Appendix E.

5.8.3 Benchmark Software

For benchmarking the pure software implementation of ECC, ANSSI libecc (Chapter 2.9), were compared to the ECCo. The benchmarked operations

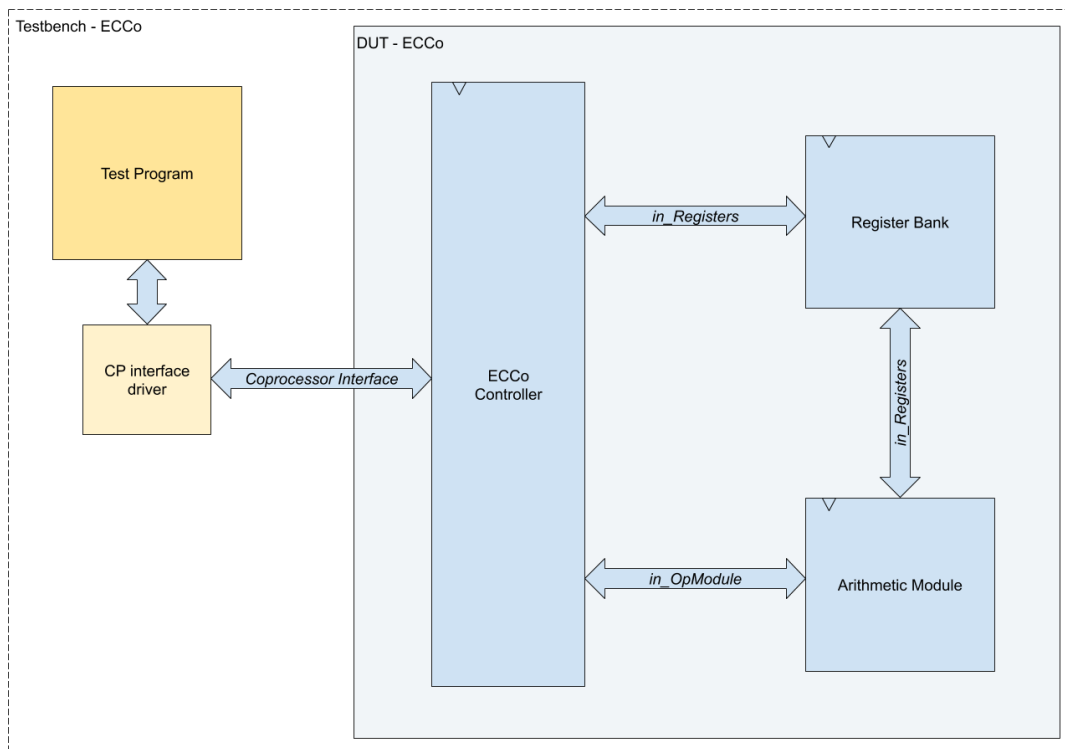


FIGURE 5.13: Testbench setup for verification of ECCo.

were the modular multiplication and modular addition. As these are the fundamental operations of SM the execution time of these will give an indication of the possible speedup. The benchmarking was performed by doing the setup of parameters once, instantiating operand 1 ($OP1$), operand 2 ($OP2$), and modulo (MOD) to large 256-bit values. The same values were used for the libecc and ECCo benchmarks. Then the operation $OP1 = OP1 + OP2 \% MOD$ were performed for the modular addition benchmark, and $OP1 = OP1 * OP2 \% MOD$ for the modular multiplication benchmark.

The benchmarks were performed doing runs of 10 and 100 iterations, i.e. performing the operation 10 or 100 times, updating the $OP1$ value each time. The test values were large 256-bit values, making them similar to values used during 256-bit SM. These benchmarks does, however, not include tests of edge cases, such as when $MOD \ll OP1 + OP2$ in which case the ECCo will have a very long execution time, nor does it guarantee coverage of the case when $MOD > OP1 + OP2$ or $MOD > OP1 * OP2$.

The source code for the benchmarking programs are listed in Appendix [F](#).

Chapter 6

Results

The simulation tests described in Chapter 5, verifying correct behavior of all sub-modules and correct results from implemented arithmetic operations, all succeeded.

This chapter presents the results from the benchmark, comparing the execution time between the modular arithmetic software implementation by libecc and the ECCo implementation. Lastly, the area estimates from synthesis are presented.

6.1 Speed

The execution time of modular addition and modular multiplication is compared between benchmark code running the operations on ECCo and using the software implementation from libecc. Table 6.2 summarizes the benchmarking results. The execution time is measured in clock cycles. As a reference, a simulation run without any operation was performed in order to measure the setup time of the system. This empty run had an execution time of 36,790 cycles (this is included in the results presented in Table 6.2).

The results show that the ECCo performed 3.8 times faster for modular addition at 10 iterations, and 8 times faster at 100 iterations. As for the modular multiplication the ECCo performed 7.8 times faster at 10 and 27 times faster at 100 iterations.

While the ECCo is significantly faster than the compared software implementation another notable result is how the ECCo and software implementation scales differently: From 10 to 100 iterations the ECCo had an increase

| Operation | Exec. Time - 10 Iterations | Exec. Time - 100 Iterations |
|---------------------------------|----------------------------|-----------------------------|
| Modular Addition - ECCo | 42,818 | 43,294 |
| Modular Addition - libecc | 164,906 | 347,966 |
| Modular Multiplication - ECCo | 46,840 | 87,864 |
| Modular Multiplication - libecc | 367,664 | 2,375,744 |

TABLE 6.2: Execution time of atomic operations. Measured in clock cycles.

| Measurement | Increase |
|-----------------------|----------|
| Combinational Area | 3.12x |
| Noncombinational Area | 1.36x |
| Total Area | 1.83x |

TABLE 6.4: Area increase for design when adding ECCo.

| Module | Sub-Module | ECCo Acc. Area | Comb. Area | Noncomb. Area |
|---------------|-----------------|----------------|------------|---------------|
| Arithmetic | | 84.63% | 5.80% | 13.61% |
| | Multiplication* | 1.97% | 1.56% | 4.81% |
| | Addition* | 1.92% | 1.53% | 4.61% |
| | Negation | 0.78% | 0.25% | 4.49% |
| | Division | 73.18% | 83.02% | 4.50% |
| Controller | | 4.65% | 5.25% | 0.42% |
| Register Bank | | 10.72% | 2.59% | 67.31% |

TABLE 6.6: Area distribution of ECCo modules. (**modular*)

in execution time of 1.01x (addition) and 1.8x (multiplication), while the software implementation had an increase of 2.1x (addition) and 6.5x (multiplication). This gives an indication on the benefit of having a coprocessor which allows an extensive amount of operations to be performed without the need for data transfer between processor and coprocessor.

6.2 Area

The design of the CM33 with the ECCo was synthesizable, and did not have any negative slack. It was synthesized without any optimization, at a frequency of 128MHz. The area results are presented as a comparison between synthesis estimates of the design with and without the ECCo included (Table 6.4), and a area distribution between the sub-modules of the ECCo (Table 6.6).

The values shown in Table 6.4 are percentage increase in area when synthesizing the CM33 and CM33+ECCo. Clearly, the ECCo contains a great deal of combinatorial logic, increasing area of combinatorial cell area by 312%. In total the ECCo's area equals 83% of existing design.

The values shown in Table 6.6 are the area distribution of the ECCo sub-modules.

ECCo Accumulative Area The area percentage of the ECCo occupied by this module, included its sub-modules. The percentages of *Arithmetic*, *Controller*, and *Register Bank* modules add up to 100%, being all the sub-modules of the ECCo. The percentages of *Multiplication*, *Addition*, *Negation*, and *Division* are included in the *Arithmetic* percentage, but they do not sum up to 84.63% since the *Arithmetic* module contains some logic of its own.

Combinatorial Area The area percentage of combinatorial cells for only this module, not including any of its sub-modules. E.g. the *Arithmetic* module uses 5.8% of the total area of combinatorial cells in the ECCo, excluded its sub-modules, and the *Division* module uses 83.02% of the total combinatorial area of the ECCo.

Noncombinatorial Area Same as for combinatorial.

Not surprisingly, a majority of the noncombinatorial area are occupied by the register bank. However, most of the area of the ECCo are occupied by the divider, which were synthesized using the SV division operator "/" without any optimization from the synthesizer.

The implementation of the most essential modules, *Modular Multiplication* and *Modular Addition*, only occupied 1.97% and 1.92%, respectively. Combined with the benchmark results, this gives an indication of the advantages of using the ECCo: Significant speedup, with only a small area increase, assuming the divisor can be more efficiently implemented. Assuming a more efficient divisor implementation: the register bank may be the module occupying the largest area, currently being 5x the size of the *Modular Multiplication* and *Modular Addition* modules, and 2x the size of the controller.

Chapter 7

Future Work

The ECCo implementation in this thesis has only included a small subset of necessary operations and features for the suggested design of a complete elliptic curve coprocessor. This chapter discusses possible changes and considerations for future work on the coprocessor proposed in this thesis.

7.1 Instruction Set Architecture

The instruction set proposed in Table 5.2 is intended for a design aimed for solution 2 in Chapter 4.1. The desired solution, however, is solution 3, which requires some additional, higher level operations to be included in the instruction set. More specifically point arithmetic (Chapter 2.2.3) and/or scalar multiplication (Chapter 2.3).

Also, another desirable functionality would be to have a way of generating random numbers of the coprocessors word size. This is because random numbers used in many cryptography algorithms, like ECDSA (Chapter 2.5).

The currently implemented arithmetic operations of modular addition and modular multiplication are also the fundamental operations of common, non-EC crypto systems, like RSA [20] and Diffie-Hellman [4]. Adding instructions for these common algorithms could be usefull, but would require the possibility of working with numbers of bit sizes up to 4096-bit to provide acceptable security.

7.2 Security

An issue which has not been addressed in this thesis, but which must be considered for future work, is security of the implementation against attacks such as side-channel attacks. A way of trying to defend against side-channel attacks is by using constant time algorithms for calculations, which should be considered both for the finite-field arithmetic, point operations and the scalar multiplication algorithm.

7.3 Algorithms

While the implemented algorithms for modular addition and modular multiplication are simple, with more complex and efficient methods available

(Chapters 3.1 and 3.2), the current implementation already provides significant speedup over pure software implementation. A future change in choice of algorithms is necessary for further development, a decision in which a compromise between security and efficiency surely is needed.

The integer division will, however, need a more area efficient implementation. Reducing the area consumption of the divisor module could, potentially, significantly reduce the total area of the ECCo.

Chapter 8

Conclusion

This thesis has explored how to design a coprocessor for accelerating elliptic curve cryptography, based on the results from the prestudy [11]. The coprocessor designed in the thesis, ECCo, was designed for use with the ARM CM33 processor. The CM33 provides a coprocessor interface for tight integration of coprocessors, which allows the instructions to be issued to connected coprocessors from software.

This led to the ECCo being designed with an instruction set providing the atomic mathematical operations for ECC, with the possibility of adding implementations of scalar multiplication to the instruction set in a future work.

As time did not allow for the entire proposed instruction set to be implemented only the atomic arithmetic operations were implemented, and an ECCo design with a controller, register bank and arithmetic module were used to compare execution time with an ECC software implementation, and to estimate area usage by synthesis. The ECCo accounted for 45% of the area when synthesizing ECCo+CM33. The estimates showed that the ECCo area consumption was largely dominated by the divisor (73.18% of the total ECCo area), which was implemented using the SystemVerilog division operator, "/", and no optimization in synthesis. However, the atomic operations of ECC, Modular Multiplication and Modular Addition, only occupied 1.97% and 1.92%, respectively. These modules also performed $3.8x - 27x$ faster than a pure software implementation of ECC.

While the implemented algorithms for modular addition and modular multiplication are simple, with more complex and efficient methods available (Chapters 3.1 and 3.2), the current implementation already provides significant speedup over pure software implementation. Providing a complete system which allows efficiency to be achieved through several methods: reducing data transfers, optimizing implementation of mathematical operations and flexibility and ease-of-use.

Appendix A

Test Data Python script

```

1  import argparse
2  import csv
3  import io
4  import os
5  import re
6  import shutil
7  import sys
8  from abc import ABC, abstractclassmethod
9  from typing import *
10
11
12 # Exception class used to differentiate between known and unknown errors.
13 class DataError(Exception):
14     pass
15
16
17 #####
18 #
19 #                                     Baseclass
20 #
21 #####
22
23 class DataABC(ABC):
24     """DataABC is the baseclass for all calculations. It handles reading from
25     and writing to csv data files, writing to C files, and number formatting
26     (decimal, hex & binary).
27     """
28     headers = []
29     data = []
30
31     def __init__(self, headers, file: io.IOBase, numBase: int) -> None:
32         self.headers = headers
33         rd = csv.reader(file)
34         # First line of the file must be the headers
35         fileHeaders = rd.__next__()
36         if self.headers != fileHeaders:
37             raise DataError(f'!!!DataABC, __init__: Invalid headers! Want_{self.headers} got_
38             ↪ {fileHeaders}')
39
40         # Read all data
41         for j, cols in enumerate(rd):
42             # Report and skip empty lines
43             if not cols:
44                 print(f'[_]DataABC, __init__: Reading_{file}: Found empty line_{(j+2)}.
45                 ↪ Ignoring...')
46                 continue
47             # Represent the data as a dict, indexed by header names
48             tmp = dict()
49             for i, h in enumerate(self.headers):
50                 # Sanitychecks to avoid decimal interpreted as hex etc.
51                 if not re.match(r'^~\d+$', cols[i]) and numBase == 10:
52                     raise DataError(f'DataABC, __init__: Reading_{file}: Tried interpreting_
53                     ↪ non-decimal_number_as_decimal: "{cols[i]}"')
54                 elif not re.match(r'^~?x[0-9a-fA-F]+$', cols[i]) and numBase == 16:
55                     raise DataError(f'DataABC, __init__: Reading_{file}: Tried interpreting_non-hex_
56                     ↪ number_as_hexadecimal: "{cols[i]}"')
57                 elif not re.match(r'^~?b[01]+$', cols[i]) and numBase == 2:
58                     raise DataError(f'DataABC, __init__: Reading_{file}: Tried interpreting_
59                     ↪ non-binary_number_as_binary: "{cols[i]}"')
60                 tmp[h] = int(cols[i], numBase)
61             self.data.append(tmp)
62
63     @abstractclassmethod
64     def calculate(self) -> None:
65         pass
66
67     @staticmethod
68     def _formatNumber(num: int, numFormat: int) -> str:
69         # Determine number format string
70         if numFormat == 16:
71             return f'0x{num:x}' if num >= 0 else f'-0x{abs(num):x}'
72         elif numFormat == 2:
73             return f'0b{num:b}' if num >= 0 else f'-0b{abs(num):b}'

```

```

69         else:
70             return f'{num}'
71
72
73     def _formatDataCsv(self, numFormat: int) -> Generator[Dict[str, str], None, None]:
74         # Iterate through data values, yield dictionaries with strings of formatted numbers
75         for d in self.data:
76             tmp = dict()
77             for k, v in d.items():
78                 tmp[k] = self._formatNumber(v, numFormat)
79             yield tmp
80
81     def writeCsv(self, file: io.IOBase, numFormat: int) -> None:
82         wr = csv.DictWriter(file, fieldnames=self.headers)
83         # First writeCsv the header line
84         wr.writeheader()
85         # Write all data to the file
86         for d in self._formatDataCsv(numFormat):
87             wr.writerow(d)
88
89     def _formatDataC(self, numFormat: int) -> Generator[List[str], None, None]:
90         for d in self.data:
91             tmp = list()
92             for v in d.values():
93                 tmp.append(self._formatNumber(v, numFormat))
94             yield tmp
95
96     def writeC(self, file: io.IOBase, numFormat: int, fileName: str, arrayName: str) -> None:
97         # Need to know size of all the arrays dimensions
98         numEntries = len(self.data) + 1 # Zero terminated
99         numHeaders = len(self.headers)
100         numChars = 0
101         # Iterate through all values and find the longest string
102         for d in self.data:
103             for v in d.values():
104                 l = len(self._formatNumber(v, numFormat))
105                 if l > numChars:
106                     numChars = l
107         numChars += 1 # One extra, for terminating zero
108
109         # Print some general information comments
110         print(f'//_Created_by_{sys.argv[0]}_with_data_from_{fileName}\n//_Number_base:_{numFormat}',
111               ↪ file=file, end='\n\n')
112         # Print some macros with meta data
113         print(f'#define_{arrayName.upper()}_NUM_ENTRIES_{numEntries-1}', file=file)
114         print(f'#define_{arrayName.upper()}_NUM_HEADERS_{numHeaders}', file=file)
115         print(f'#define_{arrayName.upper()}_NUM_CHARS_{numChars-1}', file=file, end='\n\n')
116         # Print a comment with the headers
117         print(f'//_{",".join(self.headers)}', file=file)
118         # Write the actual data
119         print(f'char_{arrayName}[_{numEntries}][[_{numHeaders}][[_{numChars}]]=', file=file)
120         for data in self._formatDataC(numFormat):
121             print(f"          {",".join(data)}", file=file)
122         # End with zero termination
123         print('          {0}\n';', file=file)
124
125 #####
126 #
127 #
128 #           Addition
129 #
130 #####
131
132 class ModAddData(DataABC):
133     def __init__(self, file: io.IOBase, numBase: int):
134         super().__init__(['modulo', 'operand1', 'operand2', 'result'], file, numBase)
135
136     def calculate(self):
137         # For each entry calculate op1+op2 % mod
138         for i, d in enumerate(self.data):
139             self.data[i]['result'] = (d['operand1'] + d['operand2']) % d['modulo']
140
141 #####
142 #
143 #
144 #           Multiplication
145 #
146 #####
147
148 class ModMulData(DataABC):
149     def __init__(self, file: io.IOBase, numBase: int):
150         super().__init__(['modulo', 'operand1', 'operand2', 'result'], file, numBase)
151
152     def calculate(self):
153         # For each entry calculate op1*op2 % mod
154         for i, d in enumerate(self.data):
155             self.data[i]['result'] = (d['operand1'] * d['operand2']) % d['modulo']
156
157 #####
158 #
159 #
160 #           Division
161 #
162 #####
163
164 class DivData(DataABC):

```

```

165 def __init__(self, file: io.IOBase, numBase: int):
166     super().__init__(['operand1', 'operand2', 'result'], file, numBase)
167
168 def calculate(self):
169     # For each entry calculate op1/op2, integer division
170     for i, d in enumerate(self.data):
171         op1 = d['operand1']
172         op2 = d['operand2']
173         # Integer division doesn't behave as expected when dealing with
174         # negative numbers (e.g. it thinks 3// -4 = -1) so just give it
175         # positive numbers instead and use basic arithmetic rules for
176         # determining result sign.
177         if op1 < 0 and op2 < 0:
178             self.data[i]['result'] = abs(op1) // abs(op2)
179         elif op1 < 0:
180             self.data[i]['result'] = -(abs(op1) // op2)
181         elif op2 < 0:
182             self.data[i]['result'] = -(op1 // abs(op2))
183         else:
184             self.data[i]['result'] = op1 // op2
185
186
187 #####
188 #
189 #                               Main code
190 #
191 #####
192
193 if __name__ == "__main__":
194     # Setup argparse
195     par = argparse.ArgumentParser()
196     par.add_argument('FILE', type=str, help='data_file_on_either_hexa,_binary_or_decimal_format.')
197     par.add_argument('-o', metavar="FILE", type=str, help='optional_output_file')
198     par.add_argument('-c', action='store_true', help='output_the_data_as_C-array_instead_of_CSV')
199     par.add_argument('-b', action='store_true', help='create_a_backup_file')
200     # Use a mutually exclusive group for selecting number format
201     formatGroup = par.add_mutually_exclusive_group(required=True)
202     formatGroup.add_argument('--dec', action='store_true', help='input_data_is_on_decimal_format.')
203     formatGroup.add_argument('--hex', action='store_true', help='input_data_is_on_hexadecimal_
204     ↪ format.')
204     formatGroup.add_argument('--bin', action='store_true', help='input_data_is_on_binary_format.')
205     # Use a mutually exclusive group for selecting output number format
206     formatGroup = par.add_mutually_exclusive_group(required=False)
207     formatGroup.add_argument('--outDec', action='store_true', help='output_data_is_on_decimal_
208     ↪ format.')
208     formatGroup.add_argument('--outHex', action='store_true', help='output_data_is_on_hexadecimal_
209     ↪ format.')
209     formatGroup.add_argument('--outBin', action='store_true', help='output_data_is_on_binary_
210     ↪ format.')
211     # Use a mutually exclusive group for selecting operation
212     operationGroup = par.add_mutually_exclusive_group(required=True)
213     operationGroup.add_argument('--add', action='store_true', help='calculate_data_for_modular_
214     ↪ addition.')
213     operationGroup.add_argument('--mul', action='store_true', help='calculate_data_for_modular_
214     ↪ multiplication.')
214     operationGroup.add_argument('--div', action='store_true', help='calculate_data_for_integer_
215     ↪ division.')
215
216     args = vars(par.parse_args())
217     dataFile = args['FILE']
218     bkupFile = f'{dataFile}.backup'
219     outFile = args['o'] if args['o'] else dataFile
220     csvOut = not args['c']
221
222     # Select data operation
223     if args['add']:
224         dataClass = ModAddData
225         cArrayName = 'dataAdd'
226     elif args['mul']:
227         dataClass = ModMulData
228         cArrayName = 'dataMul'
229     elif args['div']:
230         dataClass = DivData
231         cArrayName = 'dataDiv'
232
233     # Select input number base
234     if args['dec']:
235         inBase = 10
236     elif args['hex']:
237         inBase = 16
238     elif args['bin']:
239         inBase = 2
240     # Select output number base
241     if args['outDec']:
242         outBase = 10
243     elif args['outHex']:
244         outBase = 16
245     elif args['outBin']:
246         outBase = 2
247     else:
248         outBase = inBase
249     cArrayName = f'{cArrayName}{outBase}'
250
251     # Perform calculation
252     try:
253         with open(dataFile, 'r', newline='') as fin:
254             data = dataClass(fin, inBase)

```

```
255     data.calculate()
256     if args['b']:
257         shutil.copy(dataFile, bkupFile)
258     with open(outFile, 'w', newline='') as fout:
259         if csvOut:
260             data.writeCsv(fout, outBase)
261         else:
262             data.writeC(fout, outBase, outFile, cArrayName)
263     except DataError as e:
264         print(e, file=sys.stderr)
```

LISTING A.1: Python script for generating test data

Appendix B

Internal Interfaces SV Code

```
1 interface in_Registers;
2   logic [NUM_REGS-1:0][WORD_WIDTH:0] registers;
3   logic [WORD_WIDTH:0] wData;
4   logic [3:0] wReg;
5   logic wEnable;
6
7   modport slave (
8     output registers ,
9     input wData,
10    input wReg,
11    input wEnable
12  );
13  modport master (
14    input registers ,
15    output wData,
16    output wReg,
17    output wEnable
18  );
19  endinterface
20
21 interface in_OpModule;
22   logic ready;
23   logic error;
24   logic valid;
25   logic [3:0] opcode;
26   logic [3:0] op1Reg;
27   logic [3:0] op2Reg;
28   logic [3:0] resReg;
29
30   modport slave (
31     output ready ,
32     output error ,
33     input valid ,
34     input opcode ,
35     input op1Reg ,
36     input op2Reg ,
37     input resReg
38  );
39   modport master (
40     input ready ,
41     input error ,
42     output valid ,
43     output opcode ,
```

```
44     output op1Reg ,  
45     output op2Reg ,  
46     output resReg  
47 );  
48 endinterface
```

LISTING B.1: SystemVerilog code for the internal interfaces of ECCo.

Appendix C

Test Data

```
modulo, operand1, operand2, result
```

```
7,15,1,2
```

```
11,3,2,5
```

```
11,3,-4,10
```

```
233,75,77,152
```

```
233,567,895,64
```

```
233,567,-895,138
```

```
28657,16578,19504,7425
```

```
514229,546500,357980,390251
```

```
99194853094755497,98275954794755497,12457956214,98275967252711711
```

```
99194853094755497,98275954794755497,-12457956214,98275942336799283
```

```
92567853094755497,98275954794755497,92657924597654697,5798173202899200
```

```
92567853094755497,-98275954794755497,-92657924597654697,86769679891856297
```

```
75356465794755497,65245765798756497,70253759756423697,60143059760424697
```

```
74225698149877013133163669918490695756676765155849109751738796007550114900164,55228977
```

```
55228977394393414412853003502097247104908965897402951232160234933662925082798,45228977
```

```
74225698149877013133163669918490695756676765155849109751738796007550114900164,55228977
```

```
74225698149877013133163669918490695756676765155849109751738796007550114900164,65228977
```

```
74225698149877013133163669918490695756676765155849109751738796007550114900164,35289773
```

```
74225698149877013133163669918490695756676765155849109751738796007550114900164,95289773
```

```
74225698149877013133163669918490695756676765155849109751738796007550114900164,85289773
```

```
74225698149877013133163669918490695756676765155849109751738796007550114900164,45228977
```

LISTING C.1: Modular addition test data.

```
modulo, operand1, operand2, result
```

```
7,15,1,1
```

```
11,3,2,6
```

```
233,75,77,183
```

```
233,567,895,224
```

```

28657,16578,19504,381
514229,546500,357980,218095
99194853094755497,98275954794755497,12457956214,31017271154744113
92567853094755497,98275954794755497,92657924597654697,48036520782282743

75356465794755497,65245765798756497,70253759756423697,65782237743603078

74225698149877013133163669918490695756676765155849109751738796007550114900164,5522

55228977394393414412853003502097247104908965897402951232160234933662925082798,4522

74225698149877013133163669918490695756676765155849109751738796007550114900164,5522

74225698149877013133163669918490695756676765155849109751738796007550114900164,6522

74225698149877013133163669918490695756676765155849109751738796007550114900164,3522

74225698149877013133163669918490695756676765155849109751738796007550114900164,9522

74225698149877013133163669918490695756676765155849109751738796007550114900164,8522

74225698149877013133163669918490695756676765155849109751738796007550114900164,4522

```

LISTING C.2: Modular multiplication test data.

```

operand1 , operand2 , result
5,1,5
3,2,1
3,-4,0
75,77,0
567,895,0
567,-895,0
16578,19504,0
546500,357980,1
98275954794755497,12457956214,7888609
98275954794755497,-12457956214,-7888609
98275954794755497,92657924597654697,1
98275954794755497,97,1013154173141809
98275954794755497,-97,-1013154173141809
65245765798756497,70256423697,928680
55228977394654679572853003502097247104908965897402951232160234933662925082798,4128

65228977394654679572853003502097247104908965897402951232160234933662925082798,4128

3528977394654679572853003502097247104908965897402951232160234933662925082798,41285

9528977394654679572853003502097247104908965897402951232160234933662925082798,91285

8528977394654679572853003502097247104908965897402951232160234933662925082798,91285

45228977394393414412853003502097247104908965897402951232160234933662925082798,1329

```

LISTING C.3: Integer division test data.

Appendix D

ECCo C Wrapper

```

1  #ifndef ECC_H
2  #define ECC_H
3
4  /*****
5  *
6  *           Internal ecc.h macros
7  *
8  *****/
9
10 // Coprocessor number of the ECCo
11 #define __ECC_COPROC "p0"
12
13 /*****
14 * Opcodes *
15 *****/
16
17 // Arithmetic
18 #define __ECC_OPC1_MUL "0x0"
19 #define __ECC_OPC1_ADD "0x1"
20 #define __ECC_OPC1_DIV "0x2"
21 #define __ECC_OPC1_NEG "0x3"
22 // Logical
23 #define __ECC_OPC1_LOG "0xd"
24 #define __ECC_OPC2_OR "0x0"
25 #define __ECC_OPC2_AND "0x1"
26 #define __ECC_OPC2_XOR "0x2"
27 #define __ECC_OPC2_NOT "0x3"
28 // Shift
29 #define __ECC_OPC1_SFT "0xe"
30 #define __ECC_OPC2_LSL "0x0"
31 #define __ECC_OPC2_LSR "0x1"
32 #define __ECC_OPC2_ASR "0x2"
33 // Comparison
34 #define __ECC_OPC1_CMP "0xf"
35 #define __ECC_OPC2_ZR "0x0"
36 #define __ECC_OPC2_NZR "0x1"
37 #define __ECC_OPC2_EQ "0x2"
38 #define __ECC_OPC2_NEQ "0x3"
39 #define __ECC_OPC2_LT "0x4"
40 #define __ECC_OPC2_GT "0x5"
41 // Miscellaneous
42 #define __ECC_OPC1_INC "0xa"
43 #define __ECC_OPC1_DEC "0xb"
44 #define __ECC_OPC1_SSB "0xc"
45 #define __ECC_OPC2_SSB "0x0"
46 #define __ECC_OPC1_USB "0xc"
47 #define __ECC_OPC2_USB "0x1"
48
49
50 /*****
51 *
52 *           Exported ecc.h macros
53 *
54 *****/

```

```

55
56 #ifndef NULL
57 #define NULL ((void*)0)
58 #endif
59
60 /*****
61  * Coprocessor interface meta *
62  *****/
63
64 #define ECC_OP1_WIDTH      4
65 #define ECC_OP1_MAX       15
66 #define ECC_OP2_WIDTH     3
67 #define ECC_OP2_MAX       7
68 #define ECC_REG_IDX_WIDTH 4
69 #define ECC_REG_IDX_MAX   15
70 #define ECC_WORD_WIDTH    256
71 #define ECC_WORD_WIDTH_BYTE (ECC_WORD_WIDTH/8)
72 #define ECC_MODULO_REG     "14"
73 #define ECC_STATUS_REG    "15"
74
75 /*****
76  * Arithmetic operations *
77  *****/
78
79 // All arguments are coprocessor register indexes, which must be integers
80 // in double quotes.
81 #define ECC_MUL(op1Reg, op2Reg, resReg) asm volatile ("cdp_ _ECC_COPROC", \
82 # "_ECC_OPC1_MUL", \_cr" op2Reg", \_cr" op1Reg", \_cr" resReg", \_cr" #0")
83 #define ECC_ADD(op1Reg, op2Reg, resReg) asm volatile ("cdp_ _ECC_COPROC", \
84 # "_ECC_OPC1_ADD", \_cr" op2Reg", \_cr" op1Reg", \_cr" resReg", \_cr" #0")
85 #define ECC_DIV(op1Reg, op2Reg, resReg) asm volatile ("cdp_ _ECC_COPROC", \
86 # "_ECC_OPC1_DIV", \_cr" op2Reg", \_cr" op1Reg", \_cr" resReg", \_cr" #0")
87 #define ECC_NEG(opReg, resReg) asm volatile ("cdp_ _ECC_COPROC", \
88 # "_ECC_OPC1_NEG", \_cr0, \_cr" opReg", \_cr" resReg", \_cr" #0")
89
90 /*****
91  * Logical operations *
92  *****/
93
94 // All arguments are coprocessor register indexes, which must be integers
95 // in double quotes.
96 #define ECC_OR( op1Reg, op2Reg, resReg) asm volatile ("cdp_ _ECC_COPROC", \
97 # "_ECC_OPC1_LOG", \_cr" op2Reg", \_cr" op1Reg", \_cr" resReg", \_cr" #_ECC_OPC2_OR
98 )
99 #define ECC_AND(op1Reg, op2Reg, resReg) asm volatile ("cdp_ _ECC_COPROC", \
100 # "_ECC_OPC1_LOG", \_cr" op2Reg", \_cr" op1Reg", \_cr" resReg", \_cr" #_
101 _ECC_OPC2_AND)
102 #define ECC_XOR(op1Reg, op2Reg, resReg) asm volatile ("cdp_ _ECC_COPROC", \
103 # "_ECC_OPC1_LOG", \_cr" op2Reg", \_cr" op1Reg", \_cr" resReg", \_cr" #_
104 _ECC_OPC2_XOR)
105 #define ECC_NOT(opReg, resReg) asm volatile ("cdp_ _ECC_COPROC", \
106 # "_ECC_OPC1_LOG", \_cr0, \_cr" op1Reg", \_cr" resReg", \_cr" #_
107 _ECC_OPC2_NOT)
108
109 /*****
110  * Shift operations *
111  *****/
112
113 // All arguments are coprocessor register indexes, which must be integers
114 // in double quotes.
115 #define ECC_LSL(op1Reg, op2Reg, resReg) asm volatile ("cdp_ _ECC_COPROC", \
116 # "_ECC_OPC1_SFT", \_cr" op2Reg", \_cr" op1Reg", \_cr" resReg", \_cr" #_ECC_OPC2_LSL
117 )
118 #define ECC_LSR(op1Reg, op2Reg, resReg) asm volatile ("cdp_ _ECC_COPROC", \
119 # "_ECC_OPC1_SFT", \_cr" op2Reg", \_cr" op1Reg", \_cr" resReg", \_cr" #_ECC_OPC2_LSR
120 )
121 #define ECC_ASR(op1Reg, op2Reg, resReg) asm volatile ("cdp_ _ECC_COPROC", \
122 # "_ECC_OPC1_SFT", \_cr" op2Reg", \_cr" op1Reg", \_cr" resReg", \_cr" #_ECC_OPC2_ASR
123 )

```

```

106
107 /*****
108  * Comparison operations *
109  *****/
110
111 // All arguments are coprocessor register indexes, which must be integers
112   in double quotes.
113 #define ECC_ZR( reg)          asm volatile ("cdp_ _ECC_COPROC",_#
114   _ECC_OPC1_CMP ",_cr0, _cr" reg",_cr0,_# _ECC_OPC2_ZR)
115 #define ECC_NZR( reg)        asm volatile ("cdp_ _ECC_COPROC",_#
116   _ECC_OPC1_CMP ",_cr0, _cr" reg",_cr0,_# _ECC_OPC2_NZR)
117 #define ECC_EQ( op1Reg, op2Reg) asm volatile ("cdp_ _ECC_COPROC",_#
118   _ECC_OPC1_CMP ",_cr" op2Reg",_cr" op1Reg",_cr0,_# _ECC_OPC2_EQ)
119 #define ECC_NEQ( op1Reg, op2Reg) asm volatile ("cdp_ _ECC_COPROC",_#
120   _ECC_OPC1_CMP ",_cr" op2Reg",_cr" op1Reg",_cr0,_# _ECC_OPC2_NEQ)
121 #define ECC_LT( op1Reg, op2Reg) asm volatile ("cdp_ _ECC_COPROC",_#
122   _ECC_OPC1_CMP ",_cr" op2Reg",_cr" op1Reg",_cr0,_# _ECC_OPC2_LT)
123 #define ECC_GT( op1Reg, op2Reg) asm volatile ("cdp_ _ECC_COPROC",_#
124   _ECC_OPC1_CMP ",_cr" op2Reg",_cr" op1Reg",_cr0,_# _ECC_OPC2_GT)
125
126 /*****
127  * Miscellaneous operations *
128  *****/
129
130 // All arguments are coprocessor register indexes, which must be integers
131   in double quotes.
132 #define ECC_INC( opReg, resReg) asm volatile ("cdp_ _ECC_COPROC",_#
133   _ECC_OPC1_INC ",_cr0,_cr" opReg",_cr" resReg",_#0)
134 #define ECC_DEC( opReg, resReg) asm volatile ("cdp_ _ECC_COPROC",_#
135   _ECC_OPC1_DEC ",_cr0,_cr" opReg",_cr" resReg",_#0)
136 #define ECC_SSB( reg)          asm volatile ("cdp_ _ECC_COPROC",_#
137   _ECC_OPC1_SSB ",_cr0,_cr" reg",_cr0, _cr" _ECC_OPC2_SSB)
138 #define ECC_USB( reg)          asm volatile ("cdp_ _ECC_COPROC",_#
139   _ECC_OPC1_USB ",_cr0,_cr" reg",_cr0, _cr" _ECC_OPC2_USB)
140
141 /*****
142  * Data transfer macros *
143  *****/
144
145 /* Load coprocessor register macros. Offset is in hexa. 'reg' is a
146   coprocessor
147   register index and must be a decimal integer in double quotes. 'Rt' and
148   'Rt2' are
149   32-bit input variables. */
150 #define ECC_LOAD_0(Rt, Rt2, reg) asm volatile ("mcr_ _ECC_COPROC",_#0x0,
151   _%0,_%1,_cr" reg :: "m" (Rt), "m" (Rt2))
152 #if ECC_WORD_WIDTH > 64
153 #define ECC_LOAD_1(Rt, Rt2, reg) asm volatile ("mcr_ _ECC_COPROC",_#0x1,
154   _%0,_%1,_cr" reg :: "m" (Rt), "m" (Rt2))
155 #else
156 #define ECC_LOAD_1(Rt, Rt2, reg)
157 #endif
158 #if ECC_WORD_WIDTH > 128
159 #define ECC_LOAD_2(Rt, Rt2, reg) asm volatile ("mcr_ _ECC_COPROC",_#0x2,
160   _%0,_%1,_cr" reg :: "m" (Rt), "m" (Rt2))
161 #else
162 #define ECC_LOAD_2(Rt, Rt2, reg)
163 #endif
164 #if ECC_WORD_WIDTH > 192
165 #define ECC_LOAD_3(Rt, Rt2, reg) asm volatile ("mcr_ _ECC_COPROC",_#0x3,
166   _%0,_%1,_cr" reg :: "m" (Rt), "m" (Rt2))
167 #else
168 #define ECC_LOAD_3(Rt, Rt2, reg)
169 #endif
170 #if ECC_WORD_WIDTH > 256
171 #define ECC_LOAD_4(Rt, Rt2, reg) asm volatile ("mcr_ _ECC_COPROC",_#0x4,
172   _%0,_%1,_cr" reg :: "m" (Rt), "m" (Rt2))
173 #else
174 #define ECC_LOAD_4(Rt, Rt2, reg)
175 #endif
176 #endif

```

```

159 #if ECC_WORD_WIDTH > 320
160 #define ECC_LOAD_5(Rt, Rt2, reg) asm volatile ("mcrn_>_ECC_COPROC",_#0x5,
    _#0,_%1,_#cr" reg :: "rm" (Rt), "rm" (Rt2))
161 #else
162 #define ECC_LOAD_5(Rt, Rt2, reg)
163 #endif
164 #if ECC_WORD_WIDTH > 384
165 #define ECC_LOAD_6(Rt, Rt2, reg) asm volatile ("mcrn_>_ECC_COPROC",_#0x6,
    _#0,_%1,_#cr" reg :: "rm" (Rt), "rm" (Rt2))
166 #else
167 #define ECC_LOAD_6(Rt, Rt2, reg)
168 #endif
169 #if ECC_WORD_WIDTH > 448
170 #define ECC_LOAD_7(Rt, Rt2, reg) asm volatile ("mcrn_>_ECC_COPROC",_#0x7,
    _#0,_%1,_#cr" reg :: "rm" (Rt), "rm" (Rt2))
171 #else
172 #define ECC_LOAD_7(Rt, Rt2, reg)
173 #endif
174 #if ECC_WORD_WIDTH > 512
175 #define ECC_LOAD_8(Rt, Rt2, reg) asm volatile ("mcrn_>_ECC_COPROC",_#0x8,
    _#0,_%1,_#cr" reg :: "rm" (Rt), "rm" (Rt2))
176 #else
177 #define ECC_LOAD_8(Rt, Rt2, reg)
178 #endif
179 #if ECC_WORD_WIDTH > 576
180 #define ECC_LOAD_9(Rt, Rt2, reg) asm volatile ("mcrn_>_ECC_COPROC",_#0x9,
    _#0,_%1,_#cr" reg :: "rm" (Rt), "rm" (Rt2))
181 #else
182 #define ECC_LOAD_9(Rt, Rt2, reg)
183 #endif
184 #if ECC_WORD_WIDTH > 640
185 #define ECC_LOAD_10(Rt, Rt2, reg) asm volatile ("mcrn_>_ECC_COPROC",_#0xa,
    _#0,_%1,_#cr" reg :: "rm" (Rt), "rm" (Rt2))
186 #else
187 #define ECC_LOAD_10(Rt, Rt2, reg)
188 #endif
189 #if ECC_WORD_WIDTH > 704
190 #define ECC_LOAD_11(Rt, Rt2, reg) asm volatile ("mcrn_>_ECC_COPROC",_#0xb,
    _#0,_%1,_#cr" reg :: "rm" (Rt), "rm" (Rt2))
191 #else
192 #define ECC_LOAD_11(Rt, Rt2, reg)
193 #endif
194 #if ECC_WORD_WIDTH > 768
195 #define ECC_LOAD_12(Rt, Rt2, reg) asm volatile ("mcrn_>_ECC_COPROC",_#0xc,
    _#0,_%1,_#cr" reg :: "rm" (Rt), "rm" (Rt2))
196 #else
197 #define ECC_LOAD_12(Rt, Rt2, reg)
198 #endif
199 #if ECC_WORD_WIDTH > 832
200 #define ECC_LOAD_13(Rt, Rt2, reg) asm volatile ("mcrn_>_ECC_COPROC",_#0xd,
    _#0,_%1,_#cr" reg :: "rm" (Rt), "rm" (Rt2))
201 #else
202 #define ECC_LOAD_13(Rt, Rt2, reg)
203 #endif
204 #if ECC_WORD_WIDTH > 896
205 #define ECC_LOAD_14(Rt, Rt2, reg) asm volatile ("mcrn_>_ECC_COPROC",_#0xe,
    _#0,_%1,_#cr" reg :: "rm" (Rt), "rm" (Rt2))
206 #else
207 #define ECC_LOAD_14(Rt, Rt2, reg)
208 #endif
209 #if ECC_WORD_WIDTH > 960
210 #define ECC_LOAD_15(Rt, Rt2, reg) asm volatile ("mcrn_>_ECC_COPROC",_#0xf,
    _#0,_%1,_#cr" reg :: "rm" (Rt), "rm" (Rt2))
211 #else
212 #define ECC_LOAD_15(Rt, Rt2, reg)
213 #endif
214
215 /* Store coprocessor register macros. Offset is in hexa. 'reg' is a
    coprocessor
216 register index and must be a decimal integer in double quotes. 'Rt' and
    'Rt2' are
217 32-bit output variables. */

```

```

218 #define ECC_STORE_0(Rt, Rt2, reg) asm volatile ("mrrc_0__ECC_COPROC", _0x0,
    _0, _1, _cr" reg : "=rm" (Rt), "=rm" (Rt2))
219 #if ECC_WORD_WIDTH > 64
220 #define ECC_STORE_1(Rt, Rt2, reg) asm volatile ("mrrc_1__ECC_COPROC", _0x1
    _0, _1, _cr" reg : "=rm" (Rt), "=rm" (Rt2))
221 #else
222 #define ECC_STORE_1(Rt, Rt2, reg)
223 #endif
224 #if ECC_WORD_WIDTH > 128
225 #define ECC_STORE_2(Rt, Rt2, reg) asm volatile ("mrrc_2__ECC_COPROC", _0x2
    _0, _1, _cr" reg : "=rm" (Rt), "=rm" (Rt2))
226 #else
227 #define ECC_STORE_2(Rt, Rt2, reg)
228 #endif
229 #if ECC_WORD_WIDTH > 192
230 #define ECC_STORE_3(Rt, Rt2, reg) asm volatile ("mrrc_3__ECC_COPROC", _0x3
    _0, _1, _cr" reg : "=rm" (Rt), "=rm" (Rt2))
231 #else
232 #define ECC_STORE_3(Rt, Rt2, reg)
233 #endif
234 #if ECC_WORD_WIDTH > 256
235 #define ECC_STORE_4(Rt, Rt2, reg) asm volatile ("mrrc_4__ECC_COPROC", _0x4
    _0, _1, _cr" reg : "=rm" (Rt), "=rm" (Rt2))
236 #else
237 #define ECC_STORE_4(Rt, Rt2, reg)
238 #endif
239 #if ECC_WORD_WIDTH > 320
240 #define ECC_STORE_5(Rt, Rt2, reg) asm volatile ("mrrc_5__ECC_COPROC", _0x5
    _0, _1, _cr" reg : "=rm" (Rt), "=rm" (Rt2))
241 #else
242 #define ECC_STORE_5(Rt, Rt2, reg)
243 #endif
244 #if ECC_WORD_WIDTH > 384
245 #define ECC_STORE_6(Rt, Rt2, reg) asm volatile ("mrrc_6__ECC_COPROC", _0x6
    _0, _1, _cr" reg : "=rm" (Rt), "=rm" (Rt2))
246 #else
247 #define ECC_STORE_6(Rt, Rt2, reg)
248 #endif
249 #if ECC_WORD_WIDTH > 448
250 #define ECC_STORE_7(Rt, Rt2, reg) asm volatile ("mrrc_7__ECC_COPROC", _0x7
    _0, _1, _cr" reg : "=rm" (Rt), "=rm" (Rt2))
251 #else
252 #define ECC_STORE_7(Rt, Rt2, reg)
253 #endif
254 #if ECC_WORD_WIDTH > 512
255 #define ECC_STORE_8(Rt, Rt2, reg) asm volatile ("mrrc_8__ECC_COPROC", _0x8
    _0, _1, _cr" reg : "=rm" (Rt), "=rm" (Rt2))
256 #else
257 #define ECC_STORE_8(Rt, Rt2, reg)
258 #endif
259 #if ECC_WORD_WIDTH > 576
260 #define ECC_STORE_9(Rt, Rt2, reg) asm volatile ("mrrc_9__ECC_COPROC", _0x9
    _0, _1, _cr" reg : "=rm" (Rt), "=rm" (Rt2))
261 #else
262 #define ECC_STORE_9(Rt, Rt2, reg)
263 #endif
264 #if ECC_WORD_WIDTH > 640
265 #define ECC_STORE_10(Rt, Rt2, reg) asm volatile ("mrrc_10__ECC_COPROC", _0
    xa, _0, _1, _cr" reg : "=rm" (Rt), "=rm" (Rt2))
266 #else
267 #define ECC_STORE_10(Rt, Rt2, reg)
268 #endif
269 #if ECC_WORD_WIDTH > 704
270 #define ECC_STORE_11(Rt, Rt2, reg) asm volatile ("mrrc_11__ECC_COPROC", _0
    xb, _0, _1, _cr" reg : "=rm" (Rt), "=rm" (Rt2))
271 #else
272 #define ECC_STORE_11(Rt, Rt2, reg)
273 #endif
274 #if ECC_WORD_WIDTH > 768
275 #define ECC_STORE_12(Rt, Rt2, reg) asm volatile ("mrrc_12__ECC_COPROC", _0
    xc, _0, _1, _cr" reg : "=rm" (Rt), "=rm" (Rt2))
276 #else

```

```
277 #define ECC_STORE_12(Rt, Rt2, reg)
278 #endif
279 #if ECC_WORD_WIDTH > 832
280 #define ECC_STORE_13(Rt, Rt2, reg) asm volatile ("mrrc_ __ECC_COPROC" ,_#0
        xd,_#0,_#1,_#cr"reg : "=rm" (Rt), "=rm" (Rt2))
281 #else
282 #define ECC_STORE_13(Rt, Rt2, reg)
283 #endif
284 #if ECC_WORD_WIDTH > 896
285 #define ECC_STORE_14(Rt, Rt2, reg) asm volatile ("mrrc_ __ECC_COPROC" ,_#0
        xe,_#0,_#1,_#cr"reg : "=rm" (Rt), "=rm" (Rt2))
286 #else
287 #define ECC_STORE_14(Rt, Rt2, reg)
288 #endif
289 #if ECC_WORD_WIDTH > 960
290 #define ECC_STORE_15(Rt, Rt2, reg) asm volatile ("mrrc_ __ECC_COPROC" ,_#0
        xf,_#0,_#1,_#cr"reg : "=rm" (Rt), "=rm" (Rt2))
291 #else
292 #define ECC_STORE_15(Rt, Rt2, reg)
293 #endif
294
295 #endif // ECC_H
```

LISTING D.1: ECCo C wrapper source.

Appendix E

ECCo Big Number library

```

1  #ifndef ECC_WORD_H
2  #define ECC_WORD_H
3
4  #include <stdbool.h>
5
6  #include "ecc.h"
7
8  /* Length of array in word struct. Define here instead of ecc.h since it
9     depends
10    on array type. */
11 #define EW_LENGTH (ECC_WORD_WIDTH_BYTE/sizeof(int))
12 /* +4 to fit terminating '\0', leading '0b' and optional '-' sign. */
13 #define EW_STR_LENGTH ECC_WORD_WIDTH+4
14
15 /* ecc_word is the datatype to work with big numbers with the same width
16    as
17    the ECC coprocessors word size. */
18 typedef struct {
19     int word [EW_LENGTH];
20     bool is_zero;
21     bool is_negative;
22 } ecc_word_t;
23
24 /* String-type big enough to represent any number on either
25    binary, decimal or hexadecimal format. */
26 typedef char ew_str_t[EW_STR_LENGTH];
27
28 /* Initializes a ecc_word. Returns a pointer to the given word. */
29 ecc_word_t* ew_init(ecc_word_t*);
30
31 /* Creates a new copy of an ecc_word. Returns a pointer to dst. */
32 ecc_word_t* ew_copy(const ecc_word_t* restrict src, ecc_word_t* restrict
33                    dst);
34
35 /* *****
36    *
37    *           Content handlers
38    *
39    *****/
40
41 /* Sets the content of a ecc_word to 0. Returns a pointer to the given word
42    . */
43 ecc_word_t* ew_zero(ecc_word_t*);
44
45 /* Set the value to an integer value. */
46 ecc_word_t* ew_set_int(ecc_word_t*, int);
47
48 /* Set the value of a word to a number represented by a string in
49    hexadecimal
50    (0x prefix) format. Return a pointer to the word, or NULL on failure. */
51 ecc_word_t* ew_set_str(ecc_word_t*, const char []);
52

```

```

50 /* Set parts of the content of a word, based on the given offset. */
51 ecc_word_t* ew_set_offs(ecc_word_t* w, int offs, int r1, int r2);
52
53 /* Return a pointer to the hexadecimal formatted string of the number. */
54 char* ew_to_str(const ecc_word_t*, char[], int);
55
56
57 /*****
58 *
59 *           Comparison
60 *
61 *****/
62
63 /* Check if two words are equal. */
64 bool ew_eq(const ecc_word_t*, const ecc_word_t*);
65
66
67 /*****
68 *
69 *           Coprocessor interaction
70 *
71 *****/
72
73 /* Load the given word into a coprocessor register. */
74 void ew_load_cr0(const ecc_word_t*);
75 void ew_load_cr1(const ecc_word_t*);
76 void ew_load_cr2(const ecc_word_t*);
77 void ew_load_cr3(const ecc_word_t*);
78 void ew_load_cr4(const ecc_word_t*);
79 void ew_load_cr5(const ecc_word_t*);
80 void ew_load_cr6(const ecc_word_t*);
81 void ew_load_cr7(const ecc_word_t*);
82 void ew_load_cr8(const ecc_word_t*);
83 void ew_load_cr9(const ecc_word_t*);
84 void ew_load_cr10(const ecc_word_t*);
85 void ew_load_cr11(const ecc_word_t*);
86 void ew_load_cr12(const ecc_word_t*);
87 void ew_load_cr13(const ecc_word_t*);
88 void ew_load_cr14(const ecc_word_t*);
89 /* CP register 15 is status register and unwriteable */
90
91 /* Store the value of a coprocessors register in the given word. Takes
92    coprocessor register index as second argument. */
93 void ew_store_cr0(ecc_word_t*);
94 void ew_store_cr1(ecc_word_t*);
95 void ew_store_cr2(ecc_word_t*);
96 void ew_store_cr3(ecc_word_t*);
97 void ew_store_cr4(ecc_word_t*);
98 void ew_store_cr5(ecc_word_t*);
99 void ew_store_cr6(ecc_word_t*);
100 void ew_store_cr7(ecc_word_t*);
101 void ew_store_cr8(ecc_word_t*);
102 void ew_store_cr9(ecc_word_t*);
103 void ew_store_cr10(ecc_word_t*);
104 void ew_store_cr11(ecc_word_t*);
105 void ew_store_cr12(ecc_word_t*);
106 void ew_store_cr13(ecc_word_t*);
107 void ew_store_cr14(ecc_word_t*);
108 void ew_store_cr15(ecc_word_t*);
109
110 /* Convenience macros */
111 #define EW_LOAD_MOD(WORD) ew_load_cr14(WORD)
112 #define EW_STORE_MOD(WORD) ew_store_cr14(WORD)
113 #define EW_STORE_STATUS(WORD) ew_store_cr15(WORD)
114
115
116 /*****
117 *   Offset select macros
118 *****/
119
120 #define EW_GET_0(Rt, Rt2, W) Rt = W->word[0]; Rt2 = W->word[1]
121 #if ECC_WORD_WIDTH > 64

```



```
122 #define EW_GET_1(Rt, Rt2, W) Rt = W->word[2]; Rt2 = W->word[3]
123 #else
124 #define EW_GET_1(Rt, Rt2, W)
125 #endif
126 #if ECC_WORD_WIDTH > 128
127 #define EW_GET_2(Rt, Rt2, W) Rt = W->word[4]; Rt2 = W->word[5]
128 #else
129 #define EW_GET_2(Rt, Rt2, W)
130 #endif
131 #if ECC_WORD_WIDTH > 192
132 #define EW_GET_3(Rt, Rt2, W) Rt = W->word[6]; Rt2 = W->word[7]
133 #else
134 #define EW_GET_3(Rt, Rt2, W)
135 #endif
136 #if ECC_WORD_WIDTH > 256
137 #define EW_GET_4(Rt, Rt2, W) Rt = W->word[8]; Rt2 = W->word[9]
138 #else
139 #define EW_GET_4(Rt, Rt2, W)
140 #endif
141 #if ECC_WORD_WIDTH > 320
142 #define EW_GET_5(Rt, Rt2, W) Rt = W->word[10]; Rt2 = W->word[11]
143 #else
144 #define EW_GET_5(Rt, Rt2, W)
145 #endif
146 #if ECC_WORD_WIDTH > 384
147 #define EW_GET_6(Rt, Rt2, W) Rt = W->word[12]; Rt2 = W->word[13]
148 #else
149 #define EW_GET_6(Rt, Rt2, W)
150 #endif
151 #if ECC_WORD_WIDTH > 448
152 #define EW_GET_7(Rt, Rt2, W) Rt = W->word[14]; Rt2 = W->word[15]
153 #else
154 #define EW_GET_7(Rt, Rt2, W)
155 #endif
156 #if ECC_WORD_WIDTH > 512
157 #define EW_GET_8(Rt, Rt2, W) Rt = W->word[16]; Rt2 = W->word[17]
158 #else
159 #define EW_GET_8(Rt, Rt2, W)
160 #endif
161 #if ECC_WORD_WIDTH > 576
162 #define EW_GET_9(Rt, Rt2, W) Rt = W->word[18]; Rt2 = W->word[19]
163 #else
164 #define EW_GET_9(Rt, Rt2, W)
165 #endif
166 #if ECC_WORD_WIDTH > 640
167 #define EW_GET_10(Rt, Rt2, W) Rt = W->word[20]; Rt2 = W->word[21]
168 #else
169 #define EW_GET_10(Rt, Rt2, W)
170 #endif
171 #if ECC_WORD_WIDTH > 704
172 #define EW_GET_11(Rt, Rt2, W) Rt = W->word[22]; Rt2 = W->word[23]
173 #else
174 #define EW_GET_11(Rt, Rt2, W)
175 #endif
176 #if ECC_WORD_WIDTH > 768
177 #define EW_GET_12(Rt, Rt2, W) Rt = W->word[24]; Rt2 = W->word[25]
178 #else
179 #define EW_GET_12(Rt, Rt2, W)
180 #endif
181 #if ECC_WORD_WIDTH > 832
182 #define EW_GET_13(Rt, Rt2, W) Rt = W->word[26]; Rt2 = W->word[27]
183 #else
184 #define EW_GET_13(Rt, Rt2, W)
185 #endif
186 #if ECC_WORD_WIDTH > 896
187 #define EW_GET_14(Rt, Rt2, W) Rt = W->word[28]; Rt2 = W->word[29]
188 #else
189 #define EW_GET_14(Rt, Rt2, W)
190 #endif
191 #if ECC_WORD_WIDTH > 960
192 #define EW_GET_15(Rt, Rt2, W) Rt = W->word[30]; Rt2 = W->word[31]
193 #else
```

```

194 #define EW_GET_15(Rt, Rt2, W)
195 #endif
196
197 #define EW_SET_0(Rt, Rt2, W) ew_set_offs(W, 0, Rt, Rt2)
198 #if ECC_WORD_WIDTH > 64
199 #define EW_SET_1(Rt, Rt2, W) ew_set_offs(W, 1, Rt, Rt2)
200 #else
201 #define EW_SET_1(Rt, Rt2, W)
202 #endif
203 #if ECC_WORD_WIDTH > 128
204 #define EW_SET_2(Rt, Rt2, W) ew_set_offs(W, 2, Rt, Rt2)
205 #else
206 #define EW_SET_2(Rt, Rt2, W)
207 #endif
208 #if ECC_WORD_WIDTH > 192
209 #define EW_SET_3(Rt, Rt2, W) ew_set_offs(W, 3, Rt, Rt2)
210 #else
211 #define EW_SET_3(Rt, Rt2, W)
212 #endif
213 #if ECC_WORD_WIDTH > 256
214 #define EW_SET_4(Rt, Rt2, W) ew_set_offs(W, 4, Rt, Rt2)
215 #else
216 #define EW_SET_4(Rt, Rt2, W)
217 #endif
218 #if ECC_WORD_WIDTH > 320
219 #define EW_SET_5(Rt, Rt2, W) ew_set_offs(W, 5, Rt, Rt2)
220 #else
221 #define EW_SET_5(Rt, Rt2, W)
222 #endif
223 #if ECC_WORD_WIDTH > 384
224 #define EW_SET_6(Rt, Rt2, W) ew_set_offs(W, 6, Rt, Rt2)
225 #else
226 #define EW_SET_6(Rt, Rt2, W)
227 #endif
228 #if ECC_WORD_WIDTH > 448
229 #define EW_SET_7(Rt, Rt2, W) ew_set_offs(W, 7, Rt, Rt2)
230 #else
231 #define EW_SET_7(Rt, Rt2, W)
232 #endif
233 #if ECC_WORD_WIDTH > 512
234 #define EW_SET_8(Rt, Rt2, W) ew_set_offs(W, 8, Rt, Rt2)
235 #else
236 #define EW_SET_8(Rt, Rt2, W)
237 #endif
238 #if ECC_WORD_WIDTH > 576
239 #define EW_SET_9(Rt, Rt2, W) ew_set_offs(W, 9, Rt, Rt2)
240 #else
241 #define EW_SET_9(Rt, Rt2, W)
242 #endif
243 #if ECC_WORD_WIDTH > 640
244 #define EW_SET_10(Rt, Rt2, W) ew_set_offs(W, 10, Rt, Rt2)
245 #else
246 #define EW_SET_10(Rt, Rt2, W)
247 #endif
248 #if ECC_WORD_WIDTH > 704
249 #define EW_SET_11(Rt, Rt2, W) ew_set_offs(W, 11, Rt, Rt2)
250 #else
251 #define EW_SET_11(Rt, Rt2, W)
252 #endif
253 #if ECC_WORD_WIDTH > 768
254 #define EW_SET_12(Rt, Rt2, W) ew_set_offs(W, 12, Rt, Rt2)
255 #else
256 #define EW_SET_12(Rt, Rt2, W)
257 #endif
258 #if ECC_WORD_WIDTH > 832
259 #define EW_SET_13(Rt, Rt2, W) ew_set_offs(W, 13, Rt, Rt2)
260 #else
261 #define EW_SET_13(Rt, Rt2, W)
262 #endif
263 #if ECC_WORD_WIDTH > 896
264 #define EW_SET_14(Rt, Rt2, W) ew_set_offs(W, 14, Rt, Rt2)
265 #else

```

```

266 #define EW_SET_14(Rt, Rt2, W)
267 #endif
268 #if ECC_WORD_WIDTH > 960
269 #define EW_SET_15(Rt, Rt2, W) ew_set_offs(W, 15, Rt, Rt2)
270 #else
271 #define EW_SET_15(Rt, Rt2, W)
272 #endif
273
274 #endif // ECC_WORD_H

```

LISTING E.1: Header file for big number implementation of an ECCo word.

```

1 #include "ecc_word.h"
2
3 #include <ee_printf.h>
4 #include <stdbool.h>
5
6 #include "ecc.h"
7
8 ecc_word_t*
9 ew_init(ecc_word_t* w)
10 {
11     for ( int i = 0; i < EW_LENGTH; i++ )
12         w->word[i] = 0;
13     w->is_zero = true;
14     w->is_negative = false;
15     return w;
16 }
17
18 ecc_word_t*
19 ew_copy(const ecc_word_t* restrict src, ecc_word_t* restrict dst)
20 {
21     if ( !src->is_zero )
22         for ( int i = 0; i < EW_LENGTH; i++ )
23             dst->word[i] = src->word[i];
24     else
25         for ( int i = 0; i < EW_LENGTH; i++ )
26             dst->word[i] = 0;
27
28     dst->is_zero = src->is_zero;
29     dst->is_negative = src->is_negative;
30     return dst;
31 }
32
33
34 /*****
35 *
36 *           Content handlers
37 *
38 *****/
39
40 ecc_word_t*
41 ew_zero(ecc_word_t* w)
42 {
43     if ( !w->is_zero ) {
44         for ( int i = 0; i < EW_LENGTH; i++ )
45             w->word[i] = 0;
46         w->is_zero = 1;
47     }
48     return w;
49 }
50
51 ecc_word_t*
52 ew_set_int(ecc_word_t* w, int val)
53 {
54     ew_zero(w);
55     w->word[0] = val;

```

```

56     w->is_zero = false;
57     return w;
58 }
59
60 ecc_word_t*
61 ew_set_str(ecc_word_t* w, const char str[])
62 {
63     int  shift, tmp;
64     int* num = w->word;
65     const char* c;
66
67     for ( c = str ; *c != '\0' ; c++ )
68         ;
69
70     /* Check sign */
71     if ( *str == '-' ) {
72         w->is_negative = true;
73         str++;
74     }
75     else
76         w->is_negative = false;
77
78     /* Sanity checks */
79     if ( *str++ != '0' ) {
80         MSG(("ew_set_str:_badly_formatted_string,_must_start_with_'0'_'or_'
81         '-0x'\n"));
82         return NULL;
83     }
84     if ( *str != 'x' ) {
85         MSG(("ew_set_str:_badly_formatted_string,_must_start_with_'0x'_'or_'
86         '-0x'\n"));
87         return NULL;
88     }
89
90     /* Set word to zero if non-zero */
91     if ( !w->is_zero ) {
92         do
93             *num = 0;
94             while ( ++num != w->word+EW_LENGTH );
95         }
96
97     do {
98         tmp = 0;
99         for ( shift = 0; shift < 32 && --c != str; shift += 4 ) {
100             switch ( *c ) {
101                 case 'f': case 'F':
102                     tmp ^= 0xf << shift;
103                     break;
104                 case 'e': case 'E':
105                     tmp ^= 0xe << shift;
106                     break;
107                 case 'd': case 'D':
108                     tmp ^= 0xd << shift;
109                     break;
110                 case 'c': case 'C':
111                     tmp ^= 0xc << shift;
112                     break;
113                 case 'b': case 'B':
114                     tmp ^= 0xb << shift;
115                     break;
116                 case 'a': case 'A':
117                     tmp ^= 0xa << shift;
118                     break;
119                 default:
120                     if ( *c < '0' && *c > '9' ) {
121                         MSG(("ew_set_str:_invalid_character_in_string:_%c", *c)
122                     );
123                     }
124                     return NULL;
125                 }
126             tmp ^= (*c - '0') << shift;

```

```

125     }
126     }
127     if ( tmp && w->is_zero )
128         w->is_zero = false;
129     *num = tmp;
130 } while ( c != str && ++num != w->word+EW_LENGTH );
131
132 return w;
133 }
134
135 ecc_word_t*
136 ew_set_offs(ecc_word_t* w, int offs, int r1, int r2)
137 {
138     if ( w->is_zero )
139         if ( r1 || r2 )
140             w->is_zero = false;
141     offs *= 2;
142     w->word[offs] = r1;
143     w->word[offs+1] = r2;
144     return w;
145 }
146
147 char*
148 ew_to_str(const ecc_word_t* w, char s[], int sz)
149 {
150     int i = 0, shift;
151     const int* num = w->word+EW_LENGTH;
152     unsigned char tmp;
153
154     if ( sz < 4 ) {
155         MSG(("ew_to_str:_too_small_string:_sz_=%d\n", sz));
156         return NULL;
157     }
158     if ( w->is_negative )
159         s[i++] = '-';
160     s[i++] = '0';
161     s[i++] = 'x';
162
163     while ( i < sz && num-- != w->word )
164         for ( shift = 28; shift >= 0 && i < sz; shift -= 4, i++ )
165             switch ( (tmp = (*num >> shift) & 0xf) ) {
166                 case 0xf:
167                     s[i] = 'f';
168                     break;
169                 case 0xe:
170                     s[i] = 'e';
171                     break;
172                 case 0xd:
173                     s[i] = 'd';
174                     break;
175                 case 0xc:
176                     s[i] = 'c';
177                     break;
178                 case 0xb:
179                     s[i] = 'b';
180                     break;
181                 case 0xa:
182                     s[i] = 'a';
183                     break;
184                 default:
185                     s[i] = (tmp > 9) ? 'X' : tmp + '0';
186             }
187
188     if ( i < sz )
189         s[i] = '\\0';
190     else {
191         MSG(("ew_to_str:_too_small_string:_sz_=%d\n", sz));
192         return NULL;
193     }
194     return s;
195 }
196

```

```

197
198 /*****
199 *
200 *                               Comparison
201 *
202 *****/
203
204 bool
205 ew_eq(const ecc_word_t* lhs, const ecc_word_t* rhs)
206 {
207     const int* lw = lhs->word+EW_LENGTH;
208     const int* rw = rhs->word+EW_LENGTH;
209
210     if ( lhs->is_zero && rhs->is_zero )
211         return true;
212     while ( *--lw == *--rw )
213         if ( lw == lhs->word )
214             return true;
215     return false;
216 }
217
218 /*****
219 *
220 *                               Coprocessor load
221 *
222 *****/
223
224 #define EW_LOAD_CR(N) void ew_load_cr##N(const ecc_word_t* w) { \
225     volatile register int r1, r2; \
226     /* Offset 0 */ \
227     EW_GET_0(r1, r2, w); \
228     ECC_LOAD_0(r1, r2, #N); \
229     /* Offset 1 */ \
230     EW_GET_1(r1, r2, w); \
231     ECC_LOAD_1(r1, r2, #N); \
232     /* Offset 2 */ \
233     EW_GET_2(r1, r2, w); \
234     ECC_LOAD_2(r1, r2, #N); \
235     /* Offset 3 */ \
236     EW_GET_3(r1, r2, w); \
237     ECC_LOAD_3(r1, r2, #N); \
238     /* Offset 4 */ \
239     EW_GET_4(r1, r2, w); \
240     ECC_LOAD_4(r1, r2, #N); \
241     /* Offset 5 */ \
242     EW_GET_5(r1, r2, w); \
243     ECC_LOAD_5(r1, r2, #N); \
244     /* Offset 6 */ \
245     EW_GET_6(r1, r2, w); \
246     ECC_LOAD_6(r1, r2, #N); \
247     /* Offset 7 */ \
248     EW_GET_7(r1, r2, w); \
249     ECC_LOAD_7(r1, r2, #N); \
250     /* Offset 8 */ \
251     EW_GET_8(r1, r2, w); \
252     ECC_LOAD_8(r1, r2, #N); \
253     /* Offset 9 */ \
254     EW_GET_9(r1, r2, w); \
255     ECC_LOAD_9(r1, r2, #N); \
256     /* Offset a */ \
257     EW_GET_10(r1, r2, w); \
258     ECC_LOAD_10(r1, r2, #N); \
259     /* Offset b */ \
260     EW_GET_11(r1, r2, w); \
261     ECC_LOAD_11(r1, r2, #N); \
262     /* Offset c */ \
263     EW_GET_12(r1, r2, w); \
264     ECC_LOAD_12(r1, r2, #N); \
265     /* Offset d */ \
266     EW_GET_13(r1, r2, w); \
267     ECC_LOAD_13(r1, r2, #N); \
268     /* Offset e */ \

```

```

269     EW_GET_14(r1, r2, w); \
270     ECC_LOAD_14(r1, r2, #N); \
271     /* Offset f */ \
272     EW_GET_15(r1, r2, w); \
273     ECC_LOAD_15(r1, r2, #N); \
274     \
275     if ( w->is_negative ) /* Set signed bit if negative */ \
276         ECC_NEG(#N, #N); \
277     else /* Else make sure it's unset */ \
278         ECC_USB(#N); \
279 }
280
281 _EW_LOAD_CR(0)
282 _EW_LOAD_CR(1)
283 _EW_LOAD_CR(2)
284 _EW_LOAD_CR(3)
285 _EW_LOAD_CR(4)
286 _EW_LOAD_CR(5)
287 _EW_LOAD_CR(6)
288 _EW_LOAD_CR(7)
289 _EW_LOAD_CR(8)
290 _EW_LOAD_CR(9)
291 _EW_LOAD_CR(10)
292 _EW_LOAD_CR(11)
293 _EW_LOAD_CR(12)
294 _EW_LOAD_CR(13)
295 _EW_LOAD_CR(14)
296
297
298 /* *****
299 *
300 *                               Coprocessor store
301 *
302 * *****
303
304 #define _EW_STORE_CR(N) void ew_store_cr##N(ecc_word_t* w) { \
305     register int r1, r2; \
306     unsigned     mask; \
307     \
308     /* Check sign */ \
309     ECC_STORE_0(r1, r2, ECC_STATUS_REG); \
310     mask = 1 << (0x10 + N); \
311     if ( r1 & mask ) { \
312         w->is_negative = true; \
313         ECC_NEG(#N, #N); \
314     } \
315     else \
316         w->is_negative = false; \
317     \
318     w->is_zero = true; \
319     /* Offset 0 */ \
320     ECC_STORE_0(r1, r2, #N); \
321     EW_SET_0(r1, r2, w); \
322     /* Offset 1 */ \
323     ECC_STORE_1(r1, r2, #N); \
324     EW_SET_1(r1, r2, w); \
325     /* Offset 2 */ \
326     ECC_STORE_2(r1, r2, #N); \
327     EW_SET_2(r1, r2, w); \
328     /* Offset 3 */ \
329     ECC_STORE_3(r1, r2, #N); \
330     EW_SET_3(r1, r2, w); \
331     /* Offset 4 */ \
332     ECC_STORE_4(r1, r2, #N); \
333     EW_SET_4(r1, r2, w); \
334     /* Offset 5 */ \
335     ECC_STORE_5(r1, r2, #N); \
336     EW_SET_5(r1, r2, w); \
337     /* Offset 6 */ \
338     ECC_STORE_6(r1, r2, #N); \
339     EW_SET_6(r1, r2, w); \
340     /* Offset 7 */ \

```

```

341     ECC_STORE_7(r1, r2, #N); \
342     EW_SET_7(r1, r2, w); \
343     /* Offset 8 */ \
344     ECC_STORE_8(r1, r2, #N); \
345     EW_SET_8(r1, r2, w); \
346     /* Offset 9 */ \
347     ECC_STORE_9(r1, r2, #N); \
348     EW_SET_9(r1, r2, w); \
349     /* Offset 10 */ \
350     ECC_STORE_10(r1, r2, #N); \
351     EW_SET_10(r1, r2, w); \
352     /* Offset 11 */ \
353     ECC_STORE_11(r1, r2, #N); \
354     EW_SET_11(r1, r2, w); \
355     /* Offset 12 */ \
356     ECC_STORE_12(r1, r2, #N); \
357     EW_SET_12(r1, r2, w); \
358     /* Offset 13 */ \
359     ECC_STORE_13(r1, r2, #N); \
360     EW_SET_13(r1, r2, w); \
361     /* Offset 14 */ \
362     ECC_STORE_14(r1, r2, #N); \
363     EW_SET_14(r1, r2, w); \
364     /* Offset 15 */ \
365     ECC_STORE_15(r1, r2, #N); \
366     EW_SET_15(r1, r2, w); \
367 }
368     if ( w->is_negative ) \
369         ECC_NEG(#N, #N); \
370 }
371
372 _EW_STORE_CR(0)
373 _EW_STORE_CR(1)
374 _EW_STORE_CR(2)
375 _EW_STORE_CR(3)
376 _EW_STORE_CR(4)
377 _EW_STORE_CR(5)
378 _EW_STORE_CR(6)
379 _EW_STORE_CR(7)
380 _EW_STORE_CR(8)
381 _EW_STORE_CR(9)
382 _EW_STORE_CR(10)
383 _EW_STORE_CR(11)
384 _EW_STORE_CR(12)
385 _EW_STORE_CR(13)
386 _EW_STORE_CR(14)
387
388 /* Store word from CP register 15. Does not care about sign since it's
389    the status register */
390 void
391 ew_store_cr15(ecc_word_t* w)
392 {
393     register int r1, r2;
394     w->is_zero = true;
395     /* Offset 0 */
396     ECC_STORE_0(r1, r2, "15");
397     EW_SET_0(r1, r2, w);
398     /* Offset 1 */
399     ECC_STORE_1(r1, r2, "15");
400     EW_SET_1(r1, r2, w);
401     /* Offset 2 */
402     ECC_STORE_2(r1, r2, "15");
403     EW_SET_2(r1, r2, w);
404     /* Offset 3 */
405     ECC_STORE_3(r1, r2, "15");
406     EW_SET_3(r1, r2, w);
407     /* Offset 4 */
408     ECC_STORE_4(r1, r2, "15");
409     EW_SET_4(r1, r2, w);
410     /* Offset 5 */
411     ECC_STORE_5(r1, r2, "15");
412     EW_SET_5(r1, r2, w);

```



```
413     /* Offset 6 */
414     ECC_STORE_6(r1, r2, "15");
415     EW_SET_6(r1, r2, w);
416     /* Offset 7 */
417     ECC_STORE_7(r1, r2, "15");
418     EW_SET_7(r1, r2, w);
419     /* Offset 8 */
420     ECC_STORE_8(r1, r2, "15");
421     EW_SET_8(r1, r2, w);
422     /* Offset 9 */
423     ECC_STORE_9(r1, r2, "15");
424     EW_SET_9(r1, r2, w);
425     /* Offset 10 */
426     ECC_STORE_10(r1, r2, "15");
427     EW_SET_10(r1, r2, w);
428     /* Offset 11 */
429     ECC_STORE_11(r1, r2, "15");
430     EW_SET_11(r1, r2, w);
431     /* Offset 12 */
432     ECC_STORE_12(r1, r2, "15");
433     EW_SET_12(r1, r2, w);
434     /* Offset 13 */
435     ECC_STORE_13(r1, r2, "15");
436     EW_SET_13(r1, r2, w);
437     /* Offset 14 */
438     ECC_STORE_14(r1, r2, "15");
439     EW_SET_14(r1, r2, w);
440     /* Offset 15 */
441     ECC_STORE_15(r1, r2, "15");
442     EW_SET_15(r1, r2, w);
443 }
```

LISTING E.2: Source file for big number implementation of an ECCo word.

Appendix F

Benchmark & Test program

```

1
2  /******
3  *
4  *           Control macros
5  *
6  *****/
7
8  // #define ONLY_HELLO /* Only run a simple hello world */
9
10 /* Testing control macros */
11 // #define TEST_ARI /* Test arithmetic module */
12 // #define TEST_ARI_NOADD /* Skip addition during arithmetic testing */
13 // #define TEST_ARI_NOMOD /* Skip multiplication during arithmetic testing
14 */
15 // #define TEST_ARI_NODIV /* Skip division during arithmetic testing */
16 // #define TEST_ARI_NONEG /* Skip negation during arithmetic testing */
17 // #define TEST_REGS /* Test register bank reading/writing */
18
19 /* Benchmarking control macros */
20 #define BENCHMARK /* Disable anything but the
21 benchmarking code */
22 // #define BENCHMARK_ECC_ADDITION /* Perform additions with ECCo
23 with minimal extra code */
24 // #define BENCHMARK_ANSSI_ADDITION /* Perform additions with ANSSI
25 lib with minimal extra code */
26 // #define BENCHMARK_ECC_MULTIPLICATION /* Perform multiplication with
27 ECCo with minimal extra code */
28 #define BENCHMARK_ANSSI_MULTIPLICATION /* Perform multiplication with
29 ANSSI lib with minimal extra code */
30 // #define BENCHMARK_ITERATIONS 1 /* Number of iterations during
31 benchmarking */
32 // #define BENCHMARK_ITERATIONS 10 /* Number of iterations during
33 benchmarking */
34 #define BENCHMARK_ITERATIONS 100 /* Number of iterations during
35 benchmarking */
36
37 /* ANSSI libecc control macros */
38 #define ANSSI_LIBECC
39
40 /* Sanity checks of macros */
41 #if (defined(BENCHMARK_ECC_ADDITION) && (defined(
42 BENCHMARK_ANSSI_ADDITION) || defined(BENCHMARK_ECC_MULTIPLICATION) ||
43 defined(BENCHMARK_ANSSI_MULTIPLICATION))) || \
44 (defined(BENCHMARK_ANSSI_ADDITION) && (defined(
45 BENCHMARK_ECC_ADDITION) || defined(BENCHMARK_ECC_MULTIPLICATION) ||
46 defined(BENCHMARK_ANSSI_MULTIPLICATION))) || \
47 (defined(BENCHMARK_ECC_MULTIPLICATION) && (defined(
48 BENCHMARK_ANSSI_ADDITION) || defined(BENCHMARK_ECC_ADDITION) ||
49 defined(BENCHMARK_ANSSI_MULTIPLICATION))) || \
50 (defined(BENCHMARK_ANSSI_MULTIPLICATION) && (defined(
51 BENCHMARK_ANSSI_ADDITION) || defined(BENCHMARK_ECC_MULTIPLICATION) ||
52 defined(BENCHMARK_ECC_ADDITION))))
53 #error("Only one BENCHMARK_ macro can be defined at a time")
54 #endif

```

```

38
39 #if (defined(BENCHMARK_ANSSI_ADDITION) || defined(
    BENCHMARK_ANSSI_MULTIPLICATION)) && !defined(ANSSI_LIBECC)
40 #error("ANSSI_LIBECC_must_be_defined_for_ANSSI_benchmarks")
41 #endif
42
43
44 /*****
45 *
46 *                               Includes
47 *
48 *****/
49
50 /* ARM CM33 */
51 #include <arm_cmse.h>
52 #include <cm4ss.h>
53 #include <ee_printf.h>
54 #include <cm33/secure/trustzone_util.h>
55
56 /* stdlib */
57 #include <stdbool.h>
58 #include <string.h>
59
60 /* Coprocessor */
61 #include "ecc.h"
62 #include "ecc_word.h"
63 #include "division_data.h"
64 #include "modular_addition_data.h"
65 #include "modular_multiplication_data.h"
66
67 /* ANSSI libecc */
68 #ifdef ANSSI_LIBECC
69 #include "libarith.h"
70 #endif
71
72
73 /*****
74 *
75 *                               Globals/Macros
76 *
77 *****/
78
79 /* TZ_START_NS: Start address of non-secure application */
80 #ifndef TZ_START_NS
81 #define TZ_START_NS (0x80000U)
82 #endif
83
84 #define CPACR_ADDR ((unsigned*) 0xE000ED88U)
85
86
87 /*****
88 *
89 *                               Test setup
90 *
91 *****/
92
93 /* Arithmetic test functions */
94 bool test_ari_multiplication(char (*) [DATAMUL16_NUM_HEADERS][
    DATAMUL16_NUM_CHARS+1]);
95 bool test_ari_addition(char (*) [DATAADD16_NUM_HEADERS][DATAADD16_NUM_CHARS
    +1]);
96 bool test_ari_division(char (*) [DATADIV16_NUM_HEADERS][DATADIV16_NUM_CHARS
    +1]);
97
98 /* ANSSI libecc helpers */
99 #ifdef ANSSI_LIBECC
100 static void nn_import_from_hexbuf(nn_t out_nn, const char *hbuf, u32
    hbuflen);
101 #endif
102
103 /* Benchmark value strings */

```

```

104 char add_op1_str[] = "0
    x63feb1ab67e6b315a2dea87e6547ba17e0daa6009366d19f14dbb427faee50ae";
105 char add_op1_buf[] = {0x63, 0xfe, 0xb1, 0xab, 0x67, 0xe6, 0xb3, 0x15, 0xa2,
    0xde, 0xa8, 0x7e, 0x65, 0x47, 0xba, 0x17, 0xe0, 0xda, 0xa6, 0x00, 0x93
    , 0x66, 0xd1, 0x9f, 0x14, 0xdb, 0xb4, 0x27, 0xfa, 0xee, 0x50, 0xae};
106 char add_op2_str[] = "0
    x2f08337b7ae05e16b4fada1ebbb4c7bb56009e5c141dc5b487db427faee50ae0";
107 char add_op2_buf[] = {0x2f, 0x08, 0x33, 0x7b, 0x7a, 0xe0, 0x5e, 0x16, 0xb4,
    0xfa, 0xda, 0x1e, 0xbb, 0xb4, 0xc7, 0xbb, 0x56, 0x00, 0x9e, 0x5c, 0x14
    , 0x1d, 0xc5, 0xb4, 0x87, 0xdb, 0x42, 0x7f, 0xae, 0xe5, 0x0a, 0xe0};
108 char add_mod_str[] = "0
    xa41a41a12a799548211c410c65d8133afde34d28bdd542e4b680cf2899c8a8c4";
109 char add_mod_buf[] = {0xa4, 0x1a, 0x41, 0xa1, 0x2a, 0x79, 0x95, 0x48, 0x21,
    0x1c, 0x41, 0x0c, 0x65, 0xd8, 0x13, 0x3a, 0xfd, 0xe3, 0x4d, 0x28, 0xbd
    , 0xd5, 0x42, 0xe4, 0xb6, 0x80, 0xcf, 0x28, 0x99, 0xc8, 0xa8, 0xc4};
110 char mul_op1_str[] = "0
    x63feb1ab67e6b315a2dea87e6547ba17e0daa6009366d19f14dbb427faee50ae";
111 char mul_op1_buf[] = {0x63, 0xfe, 0xb1, 0xab, 0x67, 0xe6, 0xb3, 0x15, 0xa2,
    0xde, 0xa8, 0x7e, 0x65, 0x47, 0xba, 0x17, 0xe0, 0xda, 0xa6, 0x00, 0x93
    , 0x66, 0xd1, 0x9f, 0x14, 0xdb, 0xb4, 0x27, 0xfa, 0xee, 0x50, 0xae};
112 char mul_op2_str[] = "0
    x02f08337b7ae05e16b4fada1ebbb4c7bb56009e5c141dc5b487db427faee50ae";
113 char mul_op2_buf[] = {0x02, 0xf0, 0x83, 0x37, 0xb7, 0xae, 0x05, 0xe1, 0x6b,
    0x4f, 0xad, 0xa1, 0xeb, 0xbb, 0x4c, 0x7b, 0xb5, 0x60, 0x09, 0xe5, 0xc1
    , 0x41, 0xdc, 0x5b, 0x48, 0x7d, 0xb4, 0x27, 0xfa, 0xee, 0x50, 0xae};
114 char mul_mod_str[] = "0
    xa41a41a12a799548211c410c65d8133afde34d28bdd542e4b680cf2899c8a8c4";
115 char mul_mod_buf[] = {0xa4, 0x1a, 0x41, 0xa1, 0x2a, 0x79, 0x95, 0x48, 0x21,
    0x1c, 0x41, 0x0c, 0x65, 0xd8, 0x13, 0x3a, 0xfd, 0xe3, 0x4d, 0x28, 0xbd
    , 0xd5, 0x42, 0xe4, 0xb6, 0x80, 0xcf, 0x28, 0x99, 0xc8, 0xa8, 0xc4};

116
117 #define BM_STR_LEN 67
118 #define BM_BUF_LEN 32
119 #define BM_NN_LEN ((BM_STR_LEN / 2) / WORD_BYTES)
120
121
122 /* *****
123 *
124 *                               Secure main
125 *
126 * ***** */
127
128 int
129 main(void)
130 {
131     #ifndef BENCHMARK
132         MSG(("C-code: _Secure_firmware_booting\n"));
133         MSG((">>>>>> _Running_ECC_firmware_test.\n"));
134     #endif
135
136     /* Enable coprocessor */
137     *CPACR_ADDR ^= 0x01;
138
139     #ifdef ONLY_HELLO
140
141         MSG(("HELLO_EC_WORLD!\n"));
142
143     #else
144
145         /* *****
146          * Test arithmetic module *
147          * ***** */
148
149         #ifdef TEST_ARI
150             /* Modular addition */
151             #ifndef TEST_ARI_NOADD
152                 MSG((">>>> _Testing_addition\n"));
153                 if ( test_ari_addition(dataAdd16) )
154                     MSG(("Success!\n"));
155             #endif
156             /* Modular multiplication */
157             #ifndef TEST_ARI_NOMUL

```

```

158     MSG((">>>>_Testing_multiplication\n"));
159     if ( test_ari_multiplication(dataMul16) )
160         MSG("Success!\n");
161 #endif
162     /* Division */
163 #ifndef TEST_ARI_NODIV
164     MSG((">>>>_Testing_division\n"));
165     if ( test_ari_division(dataDiv16) )
166         MSG("Success!\n");
167 #endif
168 #endif
169
170     /* *****
171     * Benchmark modular addition w/CP *
172     * ***** */
173
174 #ifdef BENCHMARK_ECC_ADDITION
175     ecc_word_t op1, op2, mod;
176     /* Set parameter values */
177     ew_set_str(&op1, add_op1_str);
178     ew_set_str(&op2, add_op2_str);
179     ew_set_str(&mod, add_mod_str);
180     /* Load parameters to CP */
181     ew_load_cr0(&op1);
182     ew_load_cr1(&op2);
183     EW_LOAD_MOD(&mod);
184     /* Perform N number of additions */
185     for ( int i = 0; i < BENCHMARK_ITERATIONS; ++i )
186         ECC_ADD("0", "1", "0");
187 #endif
188
189     /* *****
190     * Benchmark modular addition in software *
191     * ***** */
192
193 #ifdef BENCHMARK_ANSSL_ADDITION
194     nn nn_op1, nn_op2, nn_mod;
195     fp fp_op1, fp_op2;
196     fp_ctx fp_ctx; /* Finite field context – size of field etc. */
197     /* Initialize and set parameter values */
198     nn_init_from_buf(&nn_op1, add_op1_buf, BM_BUF_LEN);
199     nn_init_from_buf(&nn_op2, add_op2_buf, BM_BUF_LEN);
200     nn_init_from_buf(&nn_mod, add_mod_buf, BM_BUF_LEN);
201     fp_ctx_init_from_p(&fp_ctx, &nn_mod);
202     fp_init(&fp_op1, &fp_ctx);
203     fp_init(&fp_op2, &fp_ctx);
204     fp_op1.fp_val = nn_op1;
205     fp_op2.fp_val = nn_op2;
206     /* Perform N number of additions */
207     for ( int i = 0; i < BENCHMARK_ITERATIONS; ++i )
208         fp_add(&fp_op1, &fp_op1, &fp_op2);
209 #endif
210
211     /* *****
212     * Benchmark modular multiplication w/CP *
213     * ***** */
214
215 #ifdef BENCHMARK_ECC_MULTIPLICATION
216     ecc_word_t op1, op2, mod;
217     /* Set parameter values */
218     ew_set_str(&op1, mul_op1_str);
219     ew_set_str(&op2, mul_op2_str);
220     ew_set_str(&mod, mul_mod_str);
221     /* Load parameters to CP */
222     ew_load_cr0(&op1);
223     ew_load_cr1(&op2);
224     EW_LOAD_MOD(&mod);
225     /* Perform N number of additions */
226     for ( int i = 0; i < BENCHMARK_ITERATIONS; ++i )
227         ECC_MUL("0", "1", "0");
228 #endif
229

```

```

230  /* *****
231  * Benchmark modular multiplication in software *
232  * *****
233
234  #ifdef BENCHMARK_ANSSI_MULTIPLICATION
235  nn nn_op1, nn_op2, nn_mod;
236  fp fp_op1, fp_op2;
237  fp_ctx fp_ctx; /* Finite field context - size of field etc. */
238  /* Initialize and set parameter values */
239  nn_init_from_buf(&nn_op1, mul_op1_buf, BM_BUF_LEN);
240  nn_init_from_buf(&nn_op2, mul_op2_buf, BM_BUF_LEN);
241  nn_init_from_buf(&nn_mod, mul_mod_buf, BM_BUF_LEN);
242  fp_ctx_init_from_p(&fp_ctx, &nn_mod);
243  fp_init(&fp_op1, &fp_ctx);
244  fp_init(&fp_op2, &fp_ctx);
245  fp_op1.fp_val = nn_op1;
246  fp_op2.fp_val = nn_op2;
247  /* Perform N number of additions */
248  for ( int i = 0; i < BENCHMARK_ITERATIONS; ++i )
249      fp_mul(&fp_op1, &fp_op1, &fp_op2);
250  #endif
251
252  #endif
253
254  #ifndef BENCHMARK
255      MSG(">>>>>>>_Finished_ECC_firmware_test.\n\n");
256  #endif
257
258  finish_test(TEST_PASS);
259  return 0; // This line will never execute as boot_nonsec_program never
        returns
260  }
261
262
263  /* *****
264  *
265  *                               Test functions
266  *
267  * *****
268
269  /* *****
270  * Arithmetic module *
271  * *****
272
273  /* Modular addition */
274  bool
275  test_ari_addition(char (*data)[DATAADD16_NUM_HEADERS][DATAADD16_NUM_CHARS
        +1])
276  {
277      int i = 0;
278      char (*entry)[DATAADD16_NUM_CHARS+1];
279      ew_str_t mod_s, op1_s, op2_s, sol_s, res_s;
280      ecc_word_t mod, op1, op2, sol, res;
281
282      while ( i++ < DATAADD16_NUM_ENTRIES ) {
283          entry = *data++;
284          /* Set parameter values from data strings */
285          if ( !ew_set_str(&mod, entry[0]) ) goto error;
286          if ( !ew_set_str(&op1, entry[1]) ) goto error;
287          if ( !ew_set_str(&op2, entry[2]) ) goto error;
288          if ( !ew_set_str(&sol, entry[3]) ) goto error;
289          /* Load parameters into CP registers */
290          ew_load_cr0(&op1);
291          ew_load_cr1(&op2);
292          EW_LOAD_MOD(&mod);
293          /* Perform addition */
294          ECC_ADD("0", "1", "2");
295          /* Verify result */
296          ew_store_cr2(&res);
297          if ( !ew_eq(&res, &sol) )
298              goto wrong;
299          MSG("Test_entry_%d_passed.\n", i);

```

```

300     }
301     return true;
302
303     wrong:
304     ew_to_str(&mod, mod_s, EW_STR_LENGTH);
305     ew_to_str(&op1, op1_s, EW_STR_LENGTH);
306     ew_to_str(&op2, op2_s, EW_STR_LENGTH);
307     ew_to_str(&res, res_s, EW_STR_LENGTH);
308     ew_to_str(&sol, sol_s, EW_STR_LENGTH);
309     MSG(("  _ _ _ _ %s\n"
310         "  _ _ + _ %s\n"
311         " (mod_ %s)\n"
312         "  _ _ = _ %s\n"
313         "  _ got _ %s\n",
314         op1_s, op2_s, mod_s, res_s, sol_s));
315     error:
316     MSG(("Failed ... \n"));
317     return false;
318 }
319
320 /* Modular addition */
321 bool
322 test_ari_multiplication(char (*data)[DATAMUL16_NUM_HEADERS][
323     DATAMUL16_NUM_CHARS+1])
324 {
325     int i = 0;
326     char (*entry)[DATAMUL16_NUM_CHARS+1];
327     ew_str_t mod_s, op1_s, op2_s, sol_s, res_s;
328     ecc_word_t mod, op1, op2, sol, res;
329
330     while ( i++ < DATAMUL16_NUM_ENTRIES ) {
331         entry = *data++;
332         /* Set parameter values from data strings */
333         if ( !ew_set_str(&mod, entry[0]) ) goto error;
334         if ( !ew_set_str(&op1, entry[1]) ) goto error;
335         if ( !ew_set_str(&op2, entry[2]) ) goto error;
336         if ( !ew_set_str(&sol, entry[3]) ) goto error;
337         /* Load parameters into CP registers */
338         ew_load_cr0(&op1);
339         ew_load_cr1(&op2);
340         EW_LOAD_MOD(&mod);
341         /* Perform addition */
342         ECC_MUL("0", "1", "2");
343         /* Verify result */
344         ew_store_cr2(&res);
345         if ( !ew_eq(&res, &sol) )
346             goto wrong;
347         MSG(("Test_entry_%d_passed.\n", i));
348     }
349     return true;
350
351     wrong:
352     ew_to_str(&mod, mod_s, EW_STR_LENGTH);
353     ew_to_str(&op1, op1_s, EW_STR_LENGTH);
354     ew_to_str(&op2, op2_s, EW_STR_LENGTH);
355     ew_to_str(&res, res_s, EW_STR_LENGTH);
356     ew_to_str(&sol, sol_s, EW_STR_LENGTH);
357     MSG(("  _ _ _ _ %s\n"
358         "  _ _ * _ %s\n"
359         " (mod_ %s)\n"
360         "  _ _ = _ %s\n"
361         "  _ got _ %s\n",
362         op1_s, op2_s, mod_s, res_s, sol_s));
363     error:
364     MSG(("Failed ... \n"));
365     return false;
366 }
367
368 /* Modular addition */
369 bool
370 test_ari_division(char (*data)[DATADIV16_NUM_HEADERS][DATADIV16_NUM_CHARS
371     +1])

```



```

370 {
371     int i = 0;
372     char (*entry)[DATADIV16_NUM_CHARS+1];
373     ew_str_t  op1_s, op2_s, sol_s, res_s;
374     ecc_word_t op1, op2, sol, res;
375
376     while ( i++ < DATADIV16_NUM_ENTRIES ) {
377         entry = *data++;
378         /* Set parameter values from data strings */
379         if ( !ew_set_str(&op1, entry[0]) ) goto error;
380         if ( !ew_set_str(&op2, entry[1]) ) goto error;
381         if ( !ew_set_str(&sol, entry[2]) ) goto error;
382         /* Load parameters into CP registers */
383         ew_load_cr0(&op1);
384         ew_load_cr1(&op2);
385         /* Perform addition */
386         ECC_DIV("0", "1", "2");
387         /* Verify result */
388         ew_store_cr2(&res);
389         if ( !ew_eq(&res, &sol) )
390             goto wrong;
391         MSG(("Test_entry_%d_passed.\n", i));
392     }
393     return true;
394
395 wrong:
396     ew_to_str(&op1, op1_s, EW_STR_LENGTH);
397     ew_to_str(&op2, op2_s, EW_STR_LENGTH);
398     ew_to_str(&res, res_s, EW_STR_LENGTH);
399     ew_to_str(&sol, sol_s, EW_STR_LENGTH);
400     MSG(("  ___\n"
401         "  __/\n"
402         "  ___=\n"
403         "  __got_\n",
404         op1_s, op2_s, res_s, sol_s));
405 error:
406     MSG(("Failed...\n"));
407     return false;
408 }

```

LISTING F.1: C main of test and benchmark program.

References

- [1] N. Koblitz, "Elliptic curve cryptosystems", *Math. Comp.*, vol. 48, pp. 203–209, 1987, ISSN: 0025-5718. DOI: [10.1090/S0025-5718-1987-0866109-5](https://doi.org/10.1090/S0025-5718-1987-0866109-5).
- [2] V. S. Miller, "Use of elliptic curves in cryptography", in *Advances in Cryptology — CRYPTO '85 Proceedings*, H. C. Williams, Ed., Berlin, Heidelberg: Springer Berlin Heidelberg, 1986, pp. 417–426, ISBN: 978-3-540-39799-1.
- [3] A. J. Menezes, S. A. Vanstone, and P. C. V. Oorschot, *Handbook of Applied Cryptography*, 1st. Boca Raton, FL, USA: CRC Press, Inc., 1996, ISBN: 0849385237.
- [4] W. Diffie and M. Hellman, "New directions in cryptography", *IEEE Transactions on Information Theory*, vol. 22, no. 6, pp. 644–654, Nov. 1976, ISSN: 0018-9448. DOI: [10.1109/TIT.1976.1055638](https://doi.org/10.1109/TIT.1976.1055638).
- [5] Y. Kumar, R. Munjal, and H. Sharma, "Comparison of symmetric and asymmetric cryptography with existing vulnerabilities and countermeasures", *International Journal of Computer Science and Management Studies*, vol. 11, no. 03, 2011.
- [6] R. Tripathi and S. Agrawal, "Comparative study of symmetric and asymmetric cryptography techniques", *International Journal of Advance Foundation and Research in Computer (IJAFRC)*, vol. 1, no. 6, pp. 68–76, 2014.
- [7] E. Rescorla. (2018). The transport layer security (tls) protocol version 1.3, [Online]. Available: <https://tools.ietf.org/html/rfc8446> (visited on 11/09/2018).
- [8] IEEE. (2017). Why we need low-power, low-latency devices, [Online]. Available: <https://innovationatwork.ieee.org/why-we-need-low-power-low-latency-devices/> (visited on 06/26/2019).
- [9] M. Guerra. (2017). The power of iot devices, [Online]. Available: <https://www.electronicdesign.com/power/power-iot-devices> (visited on 06/26/2019).
- [10] N. Shields. (2017). Here's how 5g will revolutionize the internet of things, [Online]. Available: <https://www.businessinsider.com/how-5g-will-revolutionize-the-internet-of-things-2017-6?r=US&IR=T> (visited on 06/26/2019).
- [11] M. Hirth, *Hardware acceleration of asymmetric elliptic curve cryptography*, 2018.
- [12] P. B. Bhattacharya, S. K. Jain, and S. Nagpaul, *Basic abstract algebra*, 2nd. Cambridge University Press, 1994, ISBN: 0521460816.

- [13] B. Lynn. (). Modular arithmetic, [Online]. Available: <https://crypto.stanford.edu/abc/notes/numbertheory/arith.html> (visited on 11/14/2018).
- [14] Wikipedia. (2018). Extended euclidaen algorithm, [Online]. Available: https://en.wikipedia.org/wiki/Extended_Euclidean_algorithm (visited on 11/14/2018).
- [15] —, (2018). Euclidaen algorithm, [Online]. Available: https://en.wikipedia.org/wiki/Euclidean_algorithm (visited on 11/14/2018).
- [16] S. for Efficient Cryptography. (2009). Sec 1: Elliptic curve cryptography, [Online]. Available: <http://www.secg.org/sec1-v2.pdf> (visited on 12/19/2018).
- [17] J. Balasch, B. Gierlichs, K. Järvinen, and I. Verbauwhede, “Hardware/-software co-design flavors of elliptic curve scalar multiplication”, in *2014 IEEE International Symposium on Electromagnetic Compatibility (EMC)*, Aug. 2014, pp. 758–763. DOI: [10.1109/ISEMC.2014.6899070](https://doi.org/10.1109/ISEMC.2014.6899070).
- [18] H. Cohen, A. Miyaji, and T. Ono, “Efficient elliptic curve exponentiation using mixed coordinates”, in *Advances in Cryptology — ASIACRYPT’98*, K. Ohta and D. Pei, Eds., Berlin, Heidelberg: Springer Berlin Heidelberg, 1998, pp. 51–65, ISBN: 978-3-540-49649-6.
- [19] D. Hankerson, A. J. Menezes, and S. Vanstone, *Guide to Elliptic Curve Cryptography*. Berlin, Heidelberg: Springer-Verlag, 2003, ISBN: 038795273X.
- [20] R. L. Rivest, A. Shamir, and L. Adleman, “A method for obtaining digital signatures and public-key cryptosystems”, *Commun. ACM*, vol. 21, no. 2, pp. 120–126, Feb. 1978, ISSN: 0001-0782. DOI: [10.1145/359340.359342](https://doi.org/10.1145/359340.359342). [Online]. Available: <http://doi.acm.org/10.1145/359340.359342>.
- [21] A. P. Fournaris, I. Zafeirakis, C. Koulamas, N. Sklavos, and O. Koufopavlou, “Designing efficient elliptic curve diffie-hellman accelerators for embedded systems”, in *2015 IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2015, pp. 2025–2028. DOI: [10.1109/ISCAS.2015.7169074](https://doi.org/10.1109/ISCAS.2015.7169074).
- [22] Mentor. (2019). Questa® advanced simulator, [Online]. Available: <https://www.mentor.com/products/fv/questa/> (visited on 06/19/2019).
- [23] —, (2019). Mentor, [Online]. Available: <https://www.mentor.com/> (visited on 06/19/2019).
- [24] “Ieee standard vhdl language reference manual”, *IEEE Std 1076-2008 (Revision of IEEE Std 1076-2002)*, pp. c1–626, Jan. 2009. DOI: [10.1109/IEEESTD.2009.4772740](https://doi.org/10.1109/IEEESTD.2009.4772740).
- [25] “Ieee standard for verilog hardware description language”, *IEEE Std 1364-2005 (Revision of IEEE Std 1364-2001)*, pp. 1–590, Apr. 2006. DOI: [10.1109/IEEESTD.2006.99495](https://doi.org/10.1109/IEEESTD.2006.99495).

- [26] “Ieee standard for systemverilog–unified hardware design, specification, and verification language”, *IEEE Std 1800-2017 (Revision of IEEE Std 1800-2012)*, pp. 1–1315, Feb. 2018. DOI: [10.1109/IEEESTD.2018.8299595](https://doi.org/10.1109/IEEESTD.2018.8299595).
- [27] ARM. (2019). Cortex-m33, [Online]. Available: <https://developer.arm.com/ip-products/processors/cortex-m/cortex-m33> (visited on 06/19/2019).
- [28] —, (2019). Arm, [Online]. Available: <https://www.arm.com/> (visited on 06/19/2019).
- [29] —, (2016). Armv8-m architecture reference manual, [Online]. Available: <http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.ddi0553a.d/index.html> (visited on 06/26/2019).
- [30] Wikipedia. (2019). Hardware acceleration, [Online]. Available: https://en.wikipedia.org/wiki/Hardware_acceleration (visited on 06/19/2019).
- [31] R. Benadjila, A. Ebalard, and J.-P. Flori. (2017). Libecc project, [Online]. Available: <https://github.com/ANSSI-FR/libecc> (visited on 10/11/2018).
- [32] Python Software Foundation. (2018). Python, [Online]. Available: <https://www.python.org/> (visited on 11/21/2018).
- [33] Python Docs. (2018). Python data model, [Online]. Available: <https://docs.python.org/3/reference/datamodel.html#the-standard-type-hierarchy> (visited on 11/20/2018).
- [34] C. Koc, *Rsa hardware implementation, rsa laboratories, rsa data security, inc. august 1995*.
- [35] J. K. Omura, “A public key cell design for smart card chips”, *ISITA’90*, pp. 983–985, 1990.
- [36] P. L. Montgomery, “Modular multiplication without trial division”, *Math. Comp*, vol. 44, pp. 519–521, 1985. DOI: [10.1090/S0025-5718-1985-0777282-X](https://doi.org/10.1090/S0025-5718-1985-0777282-X).
- [37] N. I. of Standards and Technology. (2013). Digital signature standards, [Online]. Available: <https://nvlpubs.nist.gov/nistpubs/FIPS/NIST.FIPS.186-4.pdf> (visited on 09/09/2018).
- [38] S. for Efficient Cryptography. (2010). Sec 2: Recommended elliptic curve domain parameters, [Online]. Available: <http://www.secg.org/sec2-v2.pdf> (visited on 09/09/2018).
- [39] OpenCores. (2019). Opencores, [Online]. Available: <https://opencores.org/> (visited on 07/01/2019).

