Master's thesis

NTNU
Norwegian University of Science and Technology
Faculty of Information Technology and Electrical Engineering
Department of Electronic Systems

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Behavioral Modelling and Design of Noise Shaping SAR ADC in 22nm FDSOI

Master's thesis in Electronic Systems Design
Supervisor: Trond Ytterdal
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30 ECTS
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Supervisor: Prof. Trond Ytterdal
Co-Supervisor: Carsten Wulff

Preface

This thesis has been written to fulfill the requirements of Masters program at Norges Teknisk-Naturvitenskaplige Universitet(NTNU), Trondheim. The basis for this research, carried out during the Spring semester of 2019, is to understand the design aspects of Noise Shaping SAR(Successive Approximation Register) ADC(Analog to Digital Converter).

I would like to thank my supervisor Professor Trond Ytterdal for the technical interaction and support through out the duration of the thesis. I would also like to thank Carsten Wulff, Nordic Semiconductor for counselling and discussions.

Problem Description

Analog to Digital Converters(ADCs) are key components in many wireless applications. Among the most critical specifications is the power dissipation. Successive Approximation Register(SAR) ADCs is of great popularity due to its power efficiency for medium resolution applications. The goal of the thesis is to design a Noise Shaping SAR ADC in 22-nm FDSOI process. The main specifications are:

- Input Bandwidth : 10 MHz.
- Accuracy : Close to 11 b ENOB.
- The ADC must use as low power as possible.

In the specialization project carried out in Autumn 2018, behavioral modelling was done to arrive at the specifications for a particular loop filter topology. The thesis work uses those specifications as basis. There have been some new topologies in Noise Shaped SAR ADC. The thesis work should compare the topologies in schematic level implementation in terms of energy efficiency for the required specifications.

The objective is to implement entire Noise shaped SAR ADC with one of the loop filter topologies and verify performance with simulations on post layout netlist in typical corner.

Abstract

Successive Approximation Registers(SAR) Analog to Digital Converters(ADCs) are very power efficient for Effective Number Of Bits(ENOB) below 9 bits. Above 9 bits, low noise comparator current could potentially limit the Figure of Merit(FOM). To achieve good power efficiency for higher ENOB, noise shaping is added to SAR ADC.

A key decision is the choice of loop filter for noise shaping. The main topologies for loop filter are cascaded FIR-IIR, fully passive and error feedback. During the course of the thesis, Noise Shaping SAR ADCs with different loop filters are modelled in Python and designed in schematic level. After comparison of Figure of Merit(FOM), it is found that the error feedback gives lower FOM for the given specifications. In addition to giving a sharp noise shaping, error feedback topology has comparator as the only analog component, making it scaling-friendly. The topology also decreases the loop filter capacitance area due to residue amplification before sampling at FIR filter, resulting in low core area. The input referred noise of comparator of approximately 500 μV is found to be sufficient to get 11b ENOB from model simulations, with 9 bit DAC. SAR ADC based on error feedback loop filter is designed and laid out. The FOM for the ADC on extracted netlist is 13 fJ/conv-step for an ENOB of 10.8 bits, and input frequency of 9.375 MHz. Operating at 160 MS/s, the SAR ADC consumes 509 μA from 0.85 V supply in 22-nm FDSOI process. The core area of the SAR ADC is 0.0045 mm^2.

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1 Introduction

Analog to digital converters(ADCs) are the vital link between the analog world and circuits performing the digital signal processing. The important metrics of ADCs for most systems are linearity, accuracy, input bandwidth and power consumption. The Successive Approximation Register(SAR) ADC is a popular architecture for medium resolution medium speed applications. For higher resolution, thermal noise of comparator limits the performance of the ADC. Noise shaping is used to solve this issue. More Effective Number Of Bits(ENOB) can be achieved using the same accuracy of DAC, thus improving energy efficiency.

There has been a lot of development as researchers try to attain better resolution for same power consumption. There are many types of ADCs such as Flash, SAR, sigma delta etc. each with its own merits and demerits. Some state of the art papers for 5-30MHz bandwidth published in ISSCC and VLSI conferences in the last 10 years show that SAR ADC is one of the best architectures to get best energy efficiency[1].

The objective of the thesis work is to design noise shaped SAR ADC which will give best Figure of Merit(FOM) for 10MHz bandwidth and 11 bit ENOB in 22nm FDSOI. To arrive at a system specification for best FOM for above requirements, a lot of investigation was necessary. The next few paragraphs highlights the flow of the investigations. At the end of this chapter, the contributions of the author to the project are described.

The energy efficiency of SAR ADC can be combined with noise shaping techniques of sigma-delta ADCs to get a better Figure of Merit for higher resolutions. In Chapter 2, noise shaping SAR ADC are introduced. Performance of some of the recent loop filters are presented.

Top level models need to be developed to check the impact of all parameters in the design. The simulation time must be short as well. Therefore, behavioral models are developed. In Chapter 3, the models developed for architectural decisions are described. The behavioral models are developed in Cadence environment and Python. Most of the observations are made based on Python models, while Cadence model was used to verify the results from the Python model. Also, the transistor level design is easily inserted into Cadence model simulations to verify block level functionality.

Noise shaping SAR ADC based on cascaded FIR-IIR filter, fully passive filters, and error feedback filters are designed in schematic level. The design aspects are discussed in Chapter 4. The chapter also includes DAC, and digital design.

The results from the parametric sweep of the Python and Cadence model are presented in in Chapter 5. The chapter also includes schematic simulation results from the different loop filters. A comparison of FOM is made by assuming same current for digital and DAC switching for all the topologies. For comparison purposes, the digital, switches and the CDAC are ideal. The digital and

DAC switching current consumption are taken from schematic simulations, and are assumed independent of loop filter topology. In addition, results from post layout simulations of error feedback noise shaping SAR ADC are also presented.

In Chapter 6, the salient points of the project are discussed based on results and observations. A comparison table with prior art is presented.

In Chapter 7, conclusions from the project are presented. The chapter includes a table with key specifications for each block in the design. A comparison with other recent publications are also included. This chapter includes discussion of what could be the future work.

ADC design optimization involves combination of many optimization techniques such as DAC switching techniques, optimal loop filters, choice of architectures for build hybrid ADC etc. All these techniques need to be investigated to get a good idea of where power efficiency can be maximized. The following section describes the contribution of the author to the project as a part of that investigation.

- *Background study*: State of the art research papers from ISSCC and VLSI in the past 10 years were studied to understand different aspects of SAR ADC design.
- *Loop filters Study*: Some of the loop filters in recent research papers were studied. A comparison of advantages and disadvantages of the loop filters is presented.
- *Python Model*: A behavioral time-domain model was built in Python for all the considered loop filters. The model can be simulated in very short time compared to the Cadence model and used extensively to arrive at the specifications of blocks.
- *Cadence Models*: A behavioral time-domain model in Cadence was built to study impact of additional top level parameters of the ADC such as thermal noise of sampling switches and filter, and settling time. The transistor level design could easily replace the model, thus verifying each block.
- *Circuit Implementation*:Schematic design was done for each of the loop filters. The loop filters could be easily integrated in the Cadence model to give an estimate of FOM. In addition, SAR ADC based on error feedback noise shaping is laid out and simulated with post layout netlist. The SAR ADC includes the comparator, CDAC, bootstrapped switch and asynchronous digital logic.

2 Background Theory

2.1 Introduction

In this chapter, noise shaped SAR ADC theory is discussed, followed by loop filter topologies. Some of the relevant works in the recent times will be discussed briefly. The loop filters are followed by DAC switching scheme theory. At the end of the chapter, the key component of SAR ADC, the Strong Arm Latch is introduced.

2.2 Noise shaping SAR ADC theory

One of the ways to improve the ENOB of SAR ADC is by oversampling. In a Nyquist ADC, an input signal of bandwidth f_{in} is sampled at frequency $f_s = 2 * f_{in}$. In an oversampled ADC, the sampling frequency can be written as $f_{sOV} = 2 * f_{in} * OSR$, where OSR is oversampling ratio. The bandwidth for integration of noise for ENOB calculation is $2f_{in}$. This bandwidth of interest can be seen as assuming ideal low pass filter after the ADC with bandwidth of $2f_{in}$. Assuming a constant power spectral density of thermal noise, it is easy to see that the integrated noise inside bandwidth $2f_{in}$ is noise inside bandwidth f_{sOV} divide by OSR. Thus, SNR of ADC can be written as:

$$SNR = 6.02N + 1.76 + 10log(OSR)dB \tag{2.1}$$

where SNR is signal to noise ratio in dB, N is effective number of bits in ADC, OSR is oversampling ratio. For a Nyquist ADC, OSR = 1. For an oversampled ADC, OSR > 1. From 2.1, it can be seen that doubling OSR results in 3dB improvement in SNR or ENOB increase of 0.5 bits.

Noise shaping improves the SNR by shaping the quantization noise spectral density. For a 1^{st} order noise shaper, the SNR can be written as:

$$SNR = 6.02N + 1.76 + 30log(OSR)dB \tag{2.2}$$

The equation 2.2 implies that the SNR improves by 9dB for doubling of OSR. A similar expression can be written for higher order noise shapers as well. In general, L^{th} order filter improves ENOB by $L + 0.5$ every doubling of OSR.

Noise shaping concepts have been used in Delta-Sigma modulators for a long time to get high resolution. Similar concept can be applied to oversampled SAR ADC as well to improve the resolution. The power efficiency of SAR ADC, when combined with ability to get better ENOB through noise shaping can potentially give ADC with high FOM. This is the focus of the noise shaping SAR ADC. There are many topologies for the loop filter in noise shaping SAR ADC, broadly divided into feed-forward and feedback topologies. In feed-forward noise shaping, the residue is sampled at the end of the bit cycling and fed to another pair of comparator inputs at the beginning of the next cycle. In feedback topology, the residue is sampled at the end of the bit cycling and fed back to CDAC. The comparator does not need one more input pair.

2.3 Cascaded FIR-IIR filters

A generic feed forward filter can be depicted as :

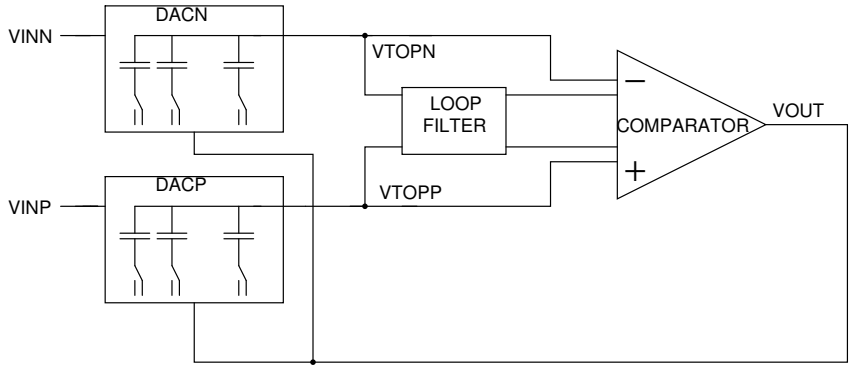

Figure 1: Error FeedForward Noise shaping Filter

A noise shaping SAR ADC based on cascaded FIR-IIR filter is proposed in [2]. In a cascaded FIR-IIR filter topology, the loop filter is an FIR filter followed by an active integrator as shown in Figure 2.

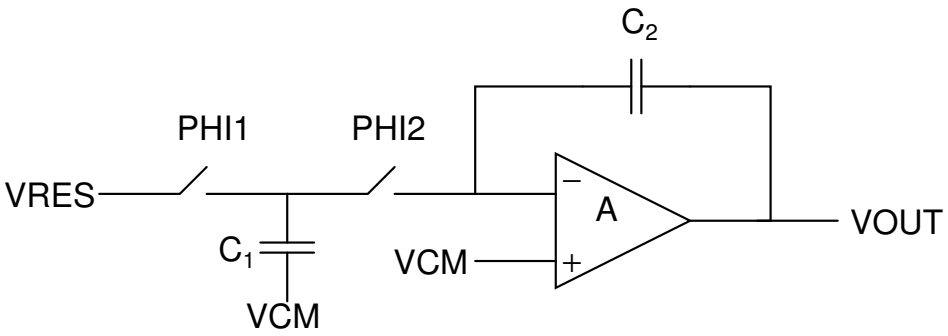

Figure 2: Cascaded FIR IIR Filter

A basic switched capacitor based integrator as a cascaded FIR IIR filter is shown in Figure 2 [3]. When PHI1 is high, the input is sampled in C_1. C_2 retains its previous output. When PHI2 is high, C_1 is discharged, assuming the top plate is made VCM by the virtual ground node of the op-amp. The charge stored in C_1 from the previous phase is transferred to C_2. If op-amp gain is infinitely large, the transfer function of integrator tends to:

$$\frac{VOUT(z)}{VRES(z)} = -\frac{C_1}{C_2}\frac{z^{-1}}{1-z^{-1}} \tag{2.3}$$

The FIR filter can be increased in order by storing residue from two cycles before. Thus, a better noise-shaping can be attained by adding more delays in the form of switches and capacitors.

The active integrator in cascaded FIR-IIR implementation is power-hungry. FIR capacitance is defined by the noise contribution. Thus, the capacitance is typically high. The integrator capacitor needs to be in ratio with the FIR for the required transfer function. For higher sampling frequency, the integrator could have high power consumption to match settling requirements.

A SAR ADC where an amplifier is used to amplify the residue before sampling at the FIR filter is proposed in [4]. The work achieves very low area, however the extra gain enhanced amplifier may not be very scaling friendly. In addition, it is an additional analog block, other than the comparator and the design and verification process could be longer.

2.4 Fully Passive Filters

Fully passive loop filters have been proposed to avoid active interators. A first order fully passive loop filter is proposed in the design[5]. Two cycles are needed for noise shaping in the proposed architecture. The architecture has a high filter area. In addition, there is attenuation during charge transfer after sampling, just before bit cycling. The comparator noise will limit the maximum ENOB that can be achieved. The first order noise shaping is sufficient for systems specification with lower ENOB, however achieving higher ENOB might need second order filter for the same OSR.

The location of zeros in NTF is vital since it leads to higher attenuation at lower frequency, at the cost of higher peaks near half sampling frequency. A passive 1^{st} loop filter with lower area is proposed[6], with zero of NTF closer to 1. This filter also may not suit the desired specification because of the first order noise shaping and comparator noise. The transfer function is set by increasing the gain of comparator for noise shaping inputs. This increases input referred noise for the inputs connected to DAC top nodes. The work has input bandwidth of $125KHz$, probably due to higher capacitance on comparator output nodes to lower noise, which restricts the maximum sampling frequency of the ADC.

A 2^{nd} loop filter passive error feedback topology is proposed in [7]. Integration is achieved by using another capacitor. Additionally, the gain to achieve the desired transfer function is achieved by using passive gain. The NTF is still shallow to achieve the desired transfer function as demonstrated in Chapter 5.

2.5 Error Feedback Filters

In [8], the residue error is amplified and fed back to the DAC, during bit cycling by charge sharing with the FIR filter. The architecture is shown in Figure 3. The residue is sampled at the end of the bit cycling and is amplified by the comparator. Since the residue is small, the comparator has sufficient linearity. The amplified residue is then sampled by FIR filter and the charge transferred to DAC by charge sharing between one of the bit cycles. The noise shaping is second order with a configurable zero in the transfer function based on the gain of the comparator during the amplification phase. The FIR filter capacitance acts as noise filter for comparator during gain phase, thus decreasing the noise at residue sampling. The filter capacitance can be potentially lowered by a factor equal to

gain of comparator. The main advantages are that the filter is passive, the ADC is potentially scaling friendly, the area can be reduced due to higher order noise shaping required lower resolution from DAC and smaller FIR filter.

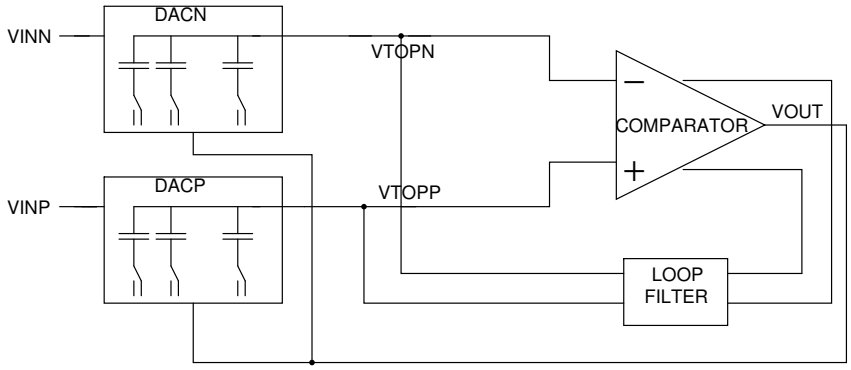

Figure 3: Error feedback filter

2.6 Switching Schemes

DAC switching energy can be lowered by choosing an appropriate switching scheme. Conventional scheme uses bottom plate sampling. The switching technique uses 2^B capacitors. During sampling phase, the input is at bottom plate and top plates are kept at common mode voltage. During hold phase, the common mode switch is open and the bottom plate is connected to ground. During bit cycling, the reference voltage is sampled by one capacitor per bit starting with the MSB capacitor. Based on the comparator decision, the chosen capacitor for the bit cycle is either connected to ground or left connected to VREF. The scheme does not reuse any charge, since charged capacitors are connected to ground for the '0' state, and capacitors are charged for the '1' state from the VREF again. The equation for average energy can be found in [9].

Monotonic switching technique uses $2^{(B-1)}$ capacitors. It uses top plate sampling. MSB is determined directly without switching any capacitor. During sampling phase, bottom plates of all capacitors are connected to ground, while the top plates are connected to input. Depending on the comparator decision, the capacitors from either of the differential DAC are connected to ground. Since only one of the differential DAC is shifted to ground every cycle, the common mode varies with bit cycling. The comparator has different offset and noise performance with common mode. This affects the linearity of the ADC.

VCM-based switching technique uses $2^{(B-1)}$ capacitors. It uses top plate sampling. MSB is determined directly without switching any capacitor. During sampling phase, bottom plates of all capacitors are connected to VCM(for example, VREF/2), while the top plates are connected to input. Depending on the comparator decision, the capacitor from one of the differential DAC are connected to ground and the corresponding capacitor on the other side connected to VREF. The

average energy consumption could be lower than monotonic since there is only charging till VCM in the sampling phase, and the discharge of this capacitor loses energy of 0.125· C· VREF^2 instead of 0.5· C· VREF^2 for the case of monotonic scheme.

From [9], VCM-based switching uses 12% energy compared to conventional switching. This is the basis for VCM switching to be used for SAR ADC.

2.7 Strong Arm Latch

The comparator is a key contributor to the overall current consumption of the SAR ADC. The comparator input referred noise and decision time is very critical to the SAR ADC performance. One of the most popular architectures for comparator is the Strong Arm Latch, first introduced in [10].

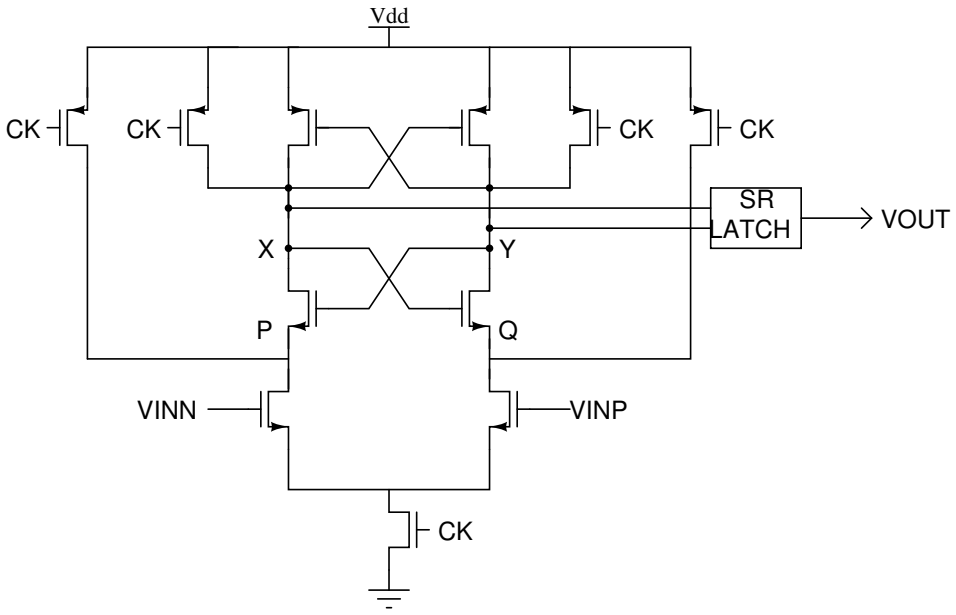

Figure 4: Strong Arm Latch

The basic latch is shown in Figure 4. The operation is explained further in brief. During the reset phase(CK is low), the nodes P,X,Y and Q are driven to supply voltage. When CK is high, the inputs create a voltage difference between the gate to source voltages of input transistors. This results in a differential current discharging P or Q. This is the amplification phase. The gain is proportional to the g_m of the input transistors. As the difference between P and Q exceeds VTH_n of NMOS transistors of the latch, voltage difference between X and Y begins to develop. Once the voltage difference exceeds VTH_p of PMOS latch transistors, the latch activates and resolves X, Y nodes to either ground or supply depending on the input voltage.

2.8 Figure of Merit

The Walden Figure of Merit(FOM) for ADC is defined as:

$$FOM_{Walden} = \frac{Power}{2 * BW.2^{ENOB}} J/conv - step \tag{2.4}$$

where Power is average power consumed by ADC, BW is input bandwidth and ENOB is effective number of bits in ADC. All future references of term 'FOM' pertains to Walden FOM. The goal is to obtain as low FOM as possible.

3 ADC Behavioral Model

3.1 Introduction

The behavioural models for the different topologies are built in Python and Cadence. The Python model is a time-domain model. Different system parameters are swept in Python model and expected ENOB is calculated. In [11], a Python and Cadence framework was built using cascaded FIR IIR filter. A current consumption model was built using initial simulation results. Model parameters were swept to get the parameters for best FOM. During the course of the thesis, it is further extended to include passive loop filter and error feedback filter. Since error feedback loop filter is fundamentally different from a feed-forward filter, some modifications needed to be done in Python model, which will be described in this chapter. All models are built using Python 3.7.1, released on 20^{th} October 2018.

3.2 Cascaded FIR IIR Filter Model

The model is described in [11]. The sampling frequency, number of bits in DAC, comparator noise were swept, and using a current consumption model, it was found that the best FOM can be achieved when number of bits in DAC is 9, sampling frequency is 160 MHz and comparator noise is 500 μV. The filter coefficients are same as [2]. Some key results from the model are described in Chapter 5.

3.3 Fully Passive Loop Filter Model

The loop filter model is modified to model the fully passive filter transfer function.

3.4 Error Feedback Loop Filter Model

The Python behavioral model can be described as in Figure 5. Parameters of the ADC like DAC LSB, number of bits in DAC(NUM_BITS), sampling frequency(FS), comparator noise during comparison(COMP NOISE) and residue amplification(COMP INT NOISE), gain of the residue amplification(COMP INT GAIN) can be swept. The ENOB is calculated from the spectrum. The passive filter noise and any settling effects are not included in the model. The DAC noise is included in the model.

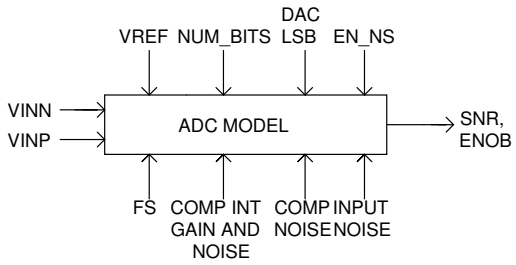

Figure 5: ADC Model Inputs and Outputs

The error feedback noise shaping ADC model is shown in Figure 6. The comparator model provides digital output during comparison phase and amplified residue. The residue is sampled when PHI_AMP is high. The loop filter consists of delays and gain blocks. Feedback of residue occurs by charge sharing when PHI_EF is high. The ADC clocks are synchronous. The DAC uses VCM switching scheme.

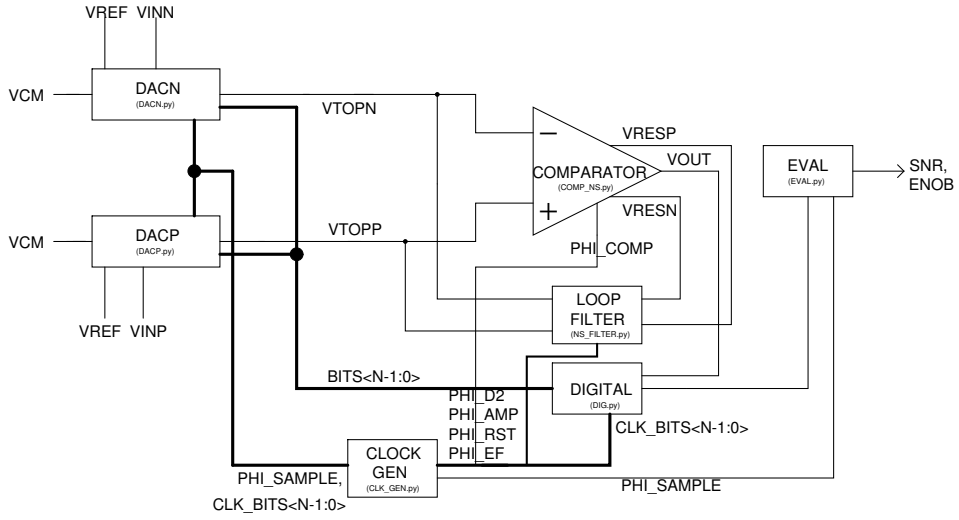

Figure 6: ADC EF Top Level

3.4.1 DAC model

DAC is modelled with VCM switching as shown in Figure 7. There are 3 states of DAC operations:

- *Sample State*: The inputs are sampled onto the top plate while the bottom plates are set to VCM.

- *Initial Bit Cycling State*:The comparison to decide the MSB is done immediately. Based on the comparator output, the capacitor bottom plates are switched from VCM to VREF or AVSS, and differentially on the other DAC. VCM is chosen as $VREF/2$. The expression for the top nodes after switching capacitor C, when VTOPP is less than VTOPN can be written as:

$$\begin{aligned} VTOPP(n) &= VTOPP(n-1) + VREF/2 * (C/C_{DAC}) \\ VTOPN(n) &= VINN(n-1) - VREF/2 * (C/C_{DAC}) \end{aligned} \tag{3.1}$$

  where C_{DAC} is total DAC capacitance on VTOPP or VTOPN respectively, and C is the capacitance that is switched for the bit cycle.
- *Error Feedback State*:The outputs from the loop filter is fed back after the 6^{th} bit is decided. The bit position to inject the feedback is configurable in the model. The expression for the top nodes after switching capacitor C for the feedback bit can be written as:

$$\begin{aligned} VTOPP(n) &= VTOPP(n-1) * C_{DAC}/C_{TOT} + VRESP_{EF}(n) \\ VRESP_{EF}(n) &= VRESP(n-1) * C_{RES}/C_{TOT} + 0.5 * VRESN(n-2) * C_{RES}/C_{TOT} \\ VTOPN(n) &= VTOPN(n-1) * C_{DAC}/C_{TOT} + VRESN_{EF}(n) \\ VRESN_{EF}(n) &= VRESN(n-1) * C_{RES}/C_{TOT} + 0.5 * VRESP(n-2) * C_{RES}/C_{TOT} \end{aligned} \tag{3.2}$$

where $C_{TOT} = C_{DAC} + 2 * C_{RES}$ is the total cap after the feedback switch is turned on, C_{RES} is the FIR filter capacitance, VRESN(n-1) and VRESP(n-1) are the sampled residues at the end of last sampling cycle, and VRESN(n-2) and VRESP(n-2) are the sampled residues at the end of two sampling cycles before. After the feedback filter is enabled, the TOP nodes has extra capacitance from the filter. The expression for the top nodes after the feedback bit till the LSB bit cycle, when VTOPP is less than VTOPN can be written as:

$$\begin{aligned} VTOPP(n) &= VTOPP(n-1) + VREF/2 * (C/C_{TOT}) \\ VTOPN(n) &= VTOPN(n-1) - VREF/2 * (C/C_{TOT}) \end{aligned} \tag{3.3}$$

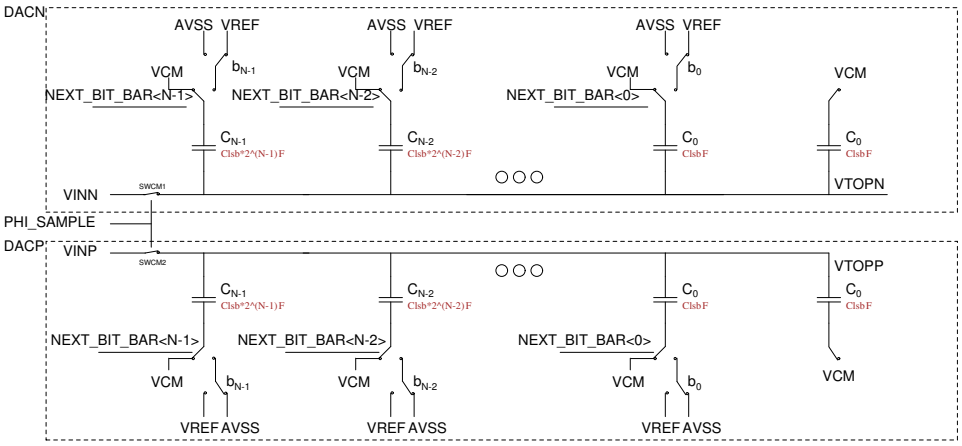

Figure 7: DAC model. The DAC is shown in sample state.

3.4.2 Comparator model

During the bit cycling phase, the comparator is modelled as a gain block followed by a limiter as shown in Figure 8. VTOPN and VTOPP nodes are at the top plates of capacitor array. The output of the comparator is reset to supply when PHI_COMP is low.The residue is always available from the comparator. It is sampled when PHI _AMP is high by the loop filter. VNOISE is input referred noise of comparator, that is swept during parametric sweep.

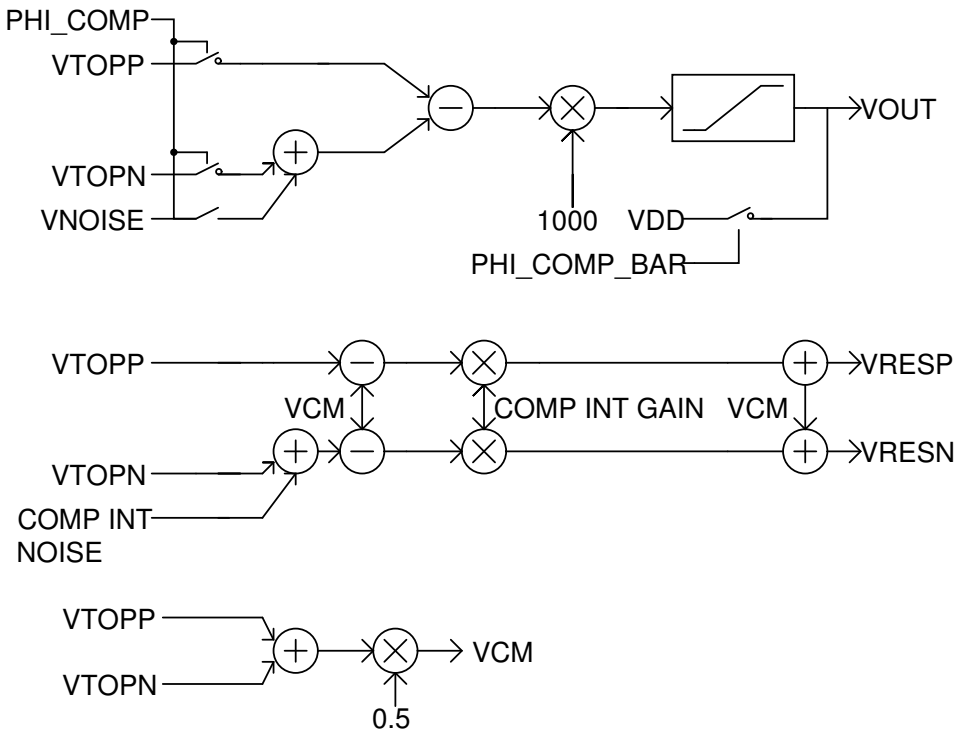

Figure 8: Comparator Model.

3.4.3 Loop Filter model

The filter model is simple FIR filter implementation as shown in Figure 9. The amplified residue from comparator is sampled when PHI_AMP is high and is fed back to the CDAC when PHI_EF is high.

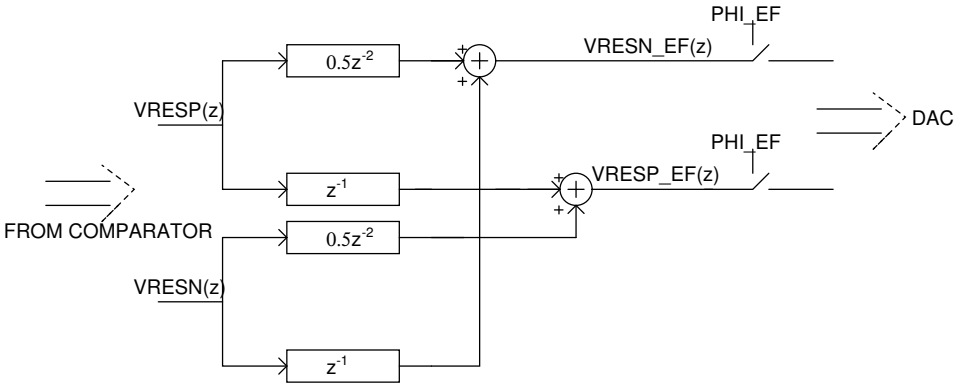

Figure 9: Loop Filter Model

3.4.4 Digital model

Synchronous clocks are used in the model for all simulations. A clip of the clock waveforms in Python simulation can be seen in Figure 10.

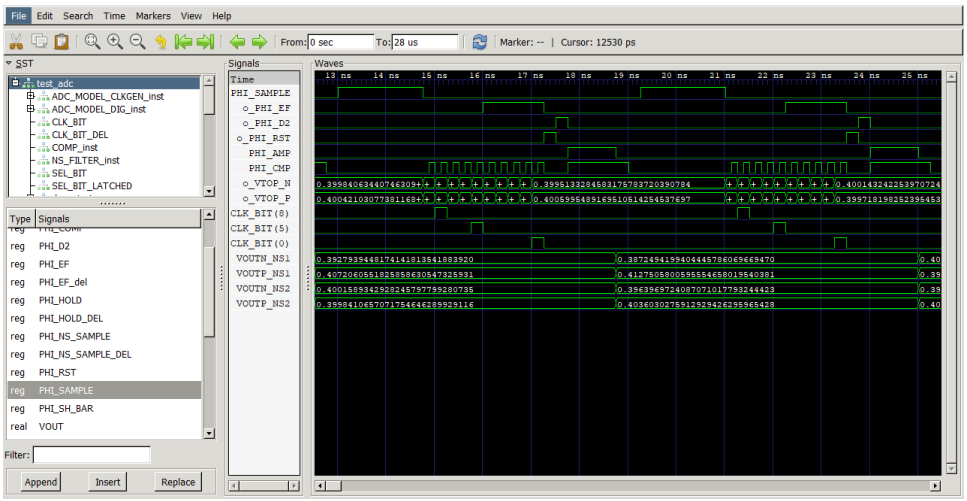

Figure 10: Loop Filter Model

3.4.5 Cadence model

The DAC and loop filter is built using ideal capacitors and ideal switches with configurable on and off resistance. The comparator is built in a similar way to the Python model. The clock generation is built using ideal sources. All block models are pin-compatible with schematic, so that the model can easily be replaced by schematic or extracted netlist for individual block verification. It was particularly useful to find out the required comparator gain for noise-shaping with DAC extracted netlist. It was also to verify the DAC linearity and filter performance with extracted netlist. The digital part is built using VerilogA model.

4 Noise Shaped SAR ADC Circuit Implementation

4.1 Introduction

This chapter describes the circuit implementation of noise-shaping ADC with three different topologies of loop filters, namely cascaded FIR-IIR filter, fully passive, and error feedback. The comparator for each of the topology is different due to the inherent nature of the noise-shaping topology. The DAC, digital, bootstrapping switch design, which are independent of the filter topology are described at the end of ths chapter. A comparison of the expected FOM is shown in Chapter 5. In addition, a brief discussion on the advantages and disadvantages of the three topologies can be found in Chapter 6.

4.2 Cascaded FIR-IIR Filter SAR ADC Design

The architecture from [2], has 2 critical analog blocks, namely the integrator and the comparator. The current consumption is determined by the comparator noise, and the settling time of comparator and integrator.

4.2.1 Comparator Design

The architecture chosen for investigation is based on Strong Arm Latch. It was first introduced in [10]. The circuit diagram is shown in Figure 11. The inputs VINN, VINP are from the CDAC top nodes, while the inputs VNSP, VNSN are the loop filter outputs. The critical specifications are the response time and input referred noise. The specification for input referred noise is derived from Python model. The response time is proportional to the sampling frequency and the time allotted for bit cycling.

The input referred noise can be seen to be proportional to[12]:

$$\bar{V_{n,in}^2} \propto \frac{V_{ov}}{C_{P,Q}} \tag{4.1}$$

where V_{ov} is $V_{GS} - V_t$ of input transitors and $C_{P,Q}$ is the capacitance at nodes P or Q. Thus, to reduce the noise, V_{ov} should be minimized which can be done by decreasing the common mode of NMOS input pair or adding capacitance at nodes P and Q. Both of the above measures increases decision time, which is proportional to $g_m/C_{P,Q}$. The common mode is half the supply voltage, so the capacitance is appropriately sized to give desired noise. To achieve the response time, the current consumption has to be increased.

The response time of comparator from schematic simulations is around 100 ps for an input of 1 LSB(around 3.5 mV). The differential input referred noise looking at VINN and VINP is 500 μV when VNSP and VNSN nodes are grounded. The noise increases to 1000 μV, when VNSP and VNSN

nodes are kept at common mode of half the supply voltage. This is because the transistors attached to VNSP and VNSN add noise current to output. The comparator schematic is simulated in Cadence model and the ENOB is similar to the Python model with only comparator noise included.

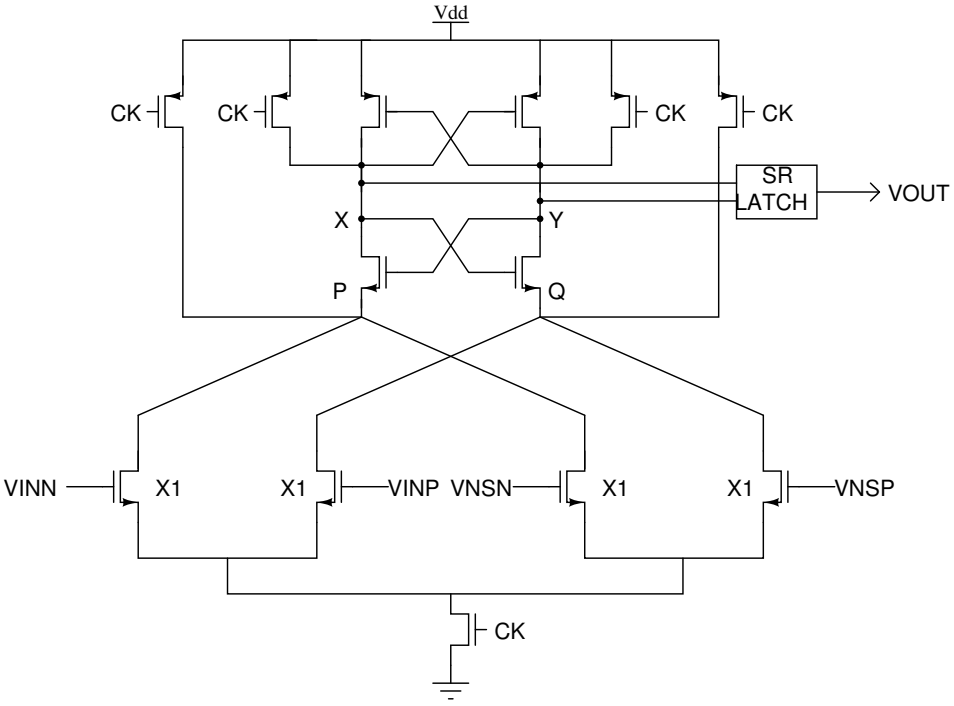

Figure 11: Strong Arm Latch

4.2.2 Filter Design

The filter comprises of interleaved passive filter followed by an active integrator. The interleaving is needed to store the residue for an extra clock period. The loop transfer function from residue to output is [2]:

$$LF(z) = \frac{K_{int} * (3z^{-1} + z^{-2})}{1 - K_{int}z^{-1}}; \tag{4.2}$$

where k_{int} is due to finite gain of op-amp.

The main current determining specification of the integrator is the settling time. Smaller the required settling time, more the current that needs to be spent on the integrator bias to increase the UGB. The sampling time is allotted 25% of the total time of conversion to allow for input settling. The integrator can be active during this time. Thus, for a sampling frequency of 160MHz, time for sampling is 1.56 ns. The integrator output must have a time constant of at least one-eighth sampling time to have good settling accuracy, to half LSB of 11 bits as given by:

$$\exp^{-T/\tau} < \frac{1}{2^{N+1}} \tag{4.3}$$

where T is charging time, τ is time constant, N is number of bits of accuracy. Thus the required τ for 160 MHz is 195 ps.

The transfer function of an integrator with a finite gain of op-amp can be written as:

$$\frac{Vout(z)}{Vin(z)} = -\frac{C_1}{C_2}\frac{z^{-1}}{1+(C_1/C_2)(1/A)-z^{-1}} \tag{4.4}$$

where A is gain of op-amp, C_1 is FIR capacitance that is reset during integration and C_2 is integrating capacitance across the op-amp. If op-amp gain is infinitely large, the transfer function of integrator tends to:

$$\frac{Vout(z)}{Vin(z)} = -\frac{C_1}{C_2}\frac{z^{-1}}{1-z^{-1}} \tag{4.5}$$

The integrator open loop gain has an impact on the noise shaping capability of the filter. Higher the gain, better the noise shaping as shown in [2]. The designed integrator has loop gain of 32 dB and UGB of 5.7 GHz. The results from stability analysis are shown in 12. Using Equation 4.4, and open loop gain of 40, the value of k_{int}=0.83 for $\frac{C_1}{C_2} = 8$ to achieve the desired transfer function. The simulated time constant is 147 ps. The current consumption is 180 μA.

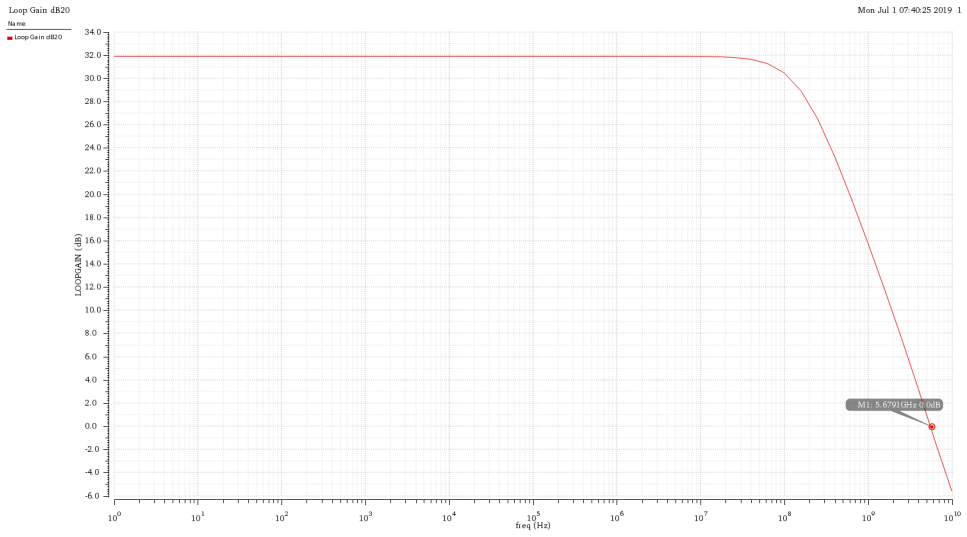

Figure 12: Integrator stability analysis Results

The output of the integrator needs a common mode feedback circuit, which is ideal for the ADC simulations. The capacitor ratios for the filter are derived from [2]. KT/C noise from a full DAC capacitance(164 fF) is around 168 μV. Unlike the comparator noise, this noise is not filtered. It is found through transient noise simulations that this capacitor is sufficient for the desired ENOB. The total FIR filter cap is kept at full DAC capacitance and the integrating cap is decided accordingly to get the correct ratio for the loop transfer function.

The architecture of the loop filter is shown in Figure 13.The states of the noise-shaping SAR ADC is shown in Figure 14. The sampling phase is also used for integration in the loop filter.

The loop filter is designed a similar way as in [2]. Only half the charge is transferred when sampling from DAC node to FIR filter. So the gain for residue transfer is 0.5. This is compensated by having a gain from the capacitor ratios during integration. The corresponding clock waveform is shown in Figure 15. PHI_SH1 and PHI_SH2 are sampling clocks with half the frequency of the input sampling clock. PHI_NS1 and PHI_NS2 are residue sampling clocks that are used to achieve the interleaving operation. In brief, when PHI_NS1 is high, residue is sampled onto C_{A1} and C_{B1}. When PHI_SH2 becomes high, the residue sampled on C_{A1} and C_{B2} is used for integration. The residue on C_{A1} is from previous cycle and residue on C_{B2} is from two cycles before. This achieves the 2-tap FIR filter. Similar activity occurs with other capacitors in the next sampling cycling.

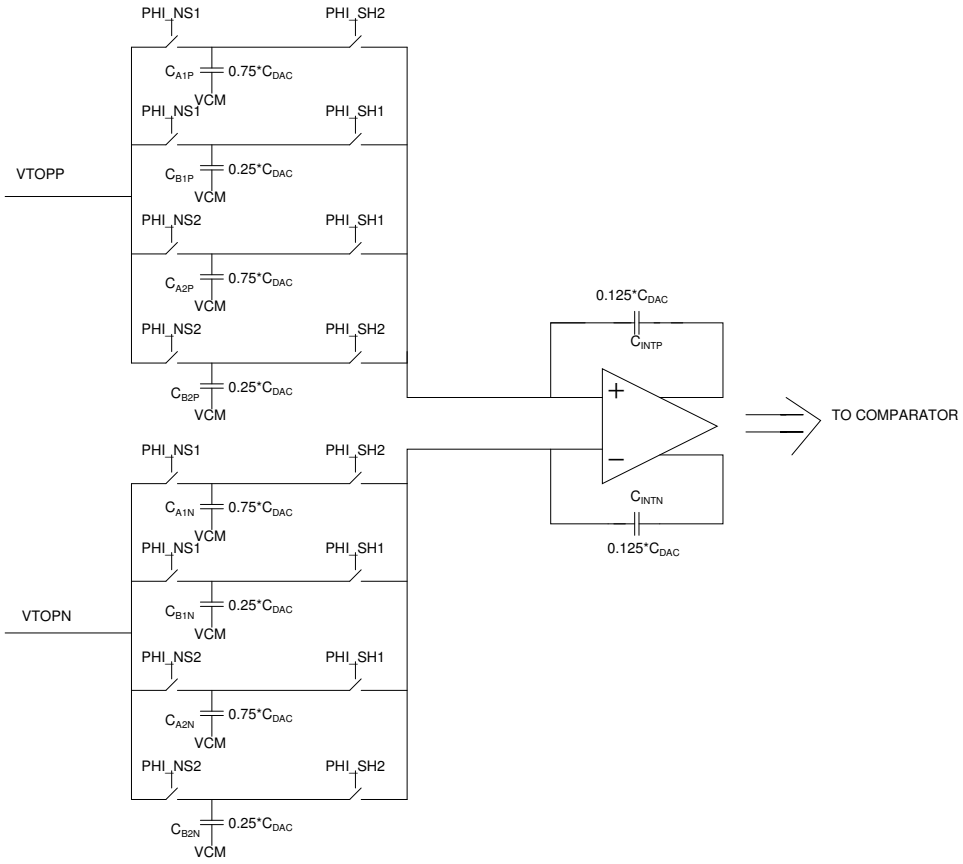

Figure 13: Interleaved FIR IIR loop filter

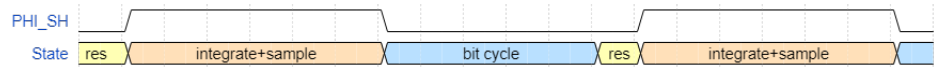

Figure 14: States of noise shaping

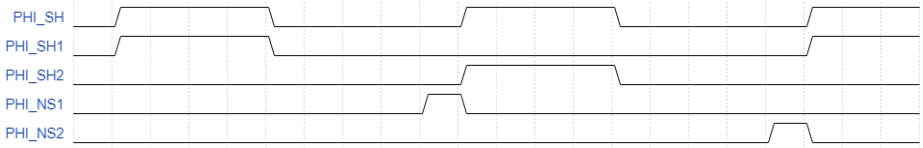

Figure 15: Waveforms for Interleaved FIR

4.3 Fully Passive Loop Filter SAR ADC Design First Order

The filter does not need any active integrator, thus saving power and design time. The filter values are from [6].

4.3.1 Comparator Design

The comparator needs to provide a gain for the residue path to place the zero at the desired location[6]. This is achieved by sizing the input transistors for residue inputs VNSN and VNSP. Those transistors are 4 times those with inputs VINN and VINP. The differential input referred noise looking at VINN and VINP is 500 μV when VNSP and VNSN nodes are grounded. The noise increases to 2000 μV when VNSP and VNSN nodes are kept at common mode of half the supply voltage.

4.3.2 Filter Design

The passive loop filter architecture is shown in Figure 16. During PHI_NS1, the residue is sampled onto capacitors C1P and C1N. During PHI_NS2, the sampled residue is integrated on capacitors C2P and C2N. The noise shaping transfer function achieved is:

$$LF(z) = 1 - 0.75z^{-1}; \tag{4.6}$$

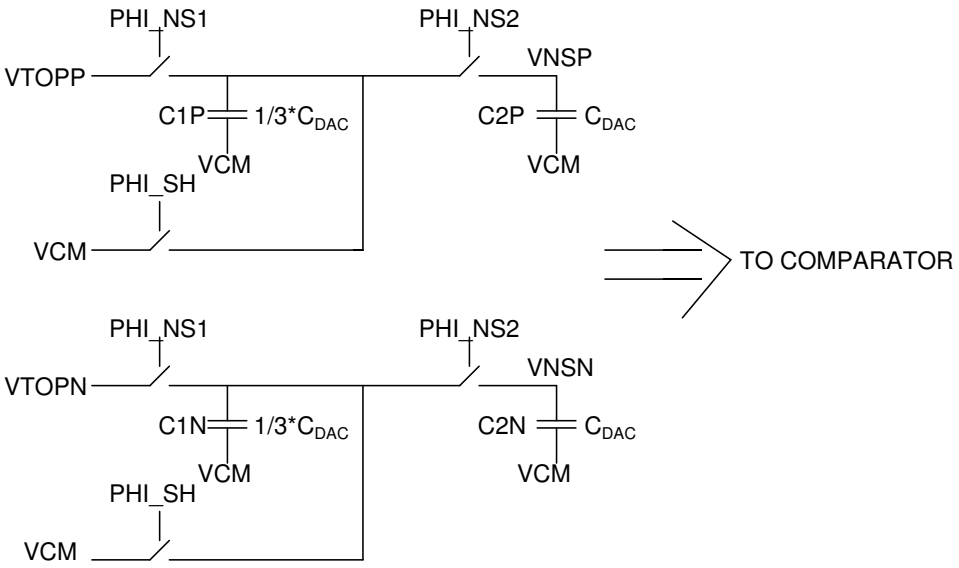

Figure 16: Fully Passive First Order Filter

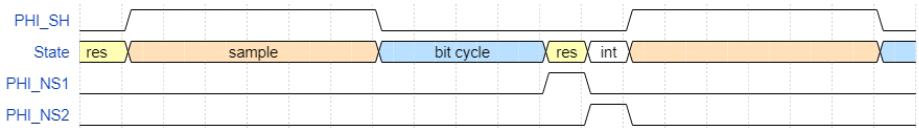

Figure 17: Fully Passive First Order Filter Clock Waveform

4.4 Fully Passive Loop Filter SAR ADC Design Second Order

The noise shaping from a first order fully passive filter is weak. Thus, to achieve a higher ENOB, more bits in DAC are needed. The second order provides more noise shaping and thus, potentially better FOM. The architecture can be extended to second order[13], but the noise of the comparator will be difficult to reduce for the desired ENOB and the desired bandwidth. Another architecture uses a 2 zero, 1 pole in filter with passive gain[7].

4.4.1 Comparator Design

The comparator is same as for cascaded FIR-IIR filter.

4.4.2 Filter Design

The filter is shown in Figure 18. The filter operation is not broken into distinct states as the first order filter. The clock waveform can be seen in Figure 19.

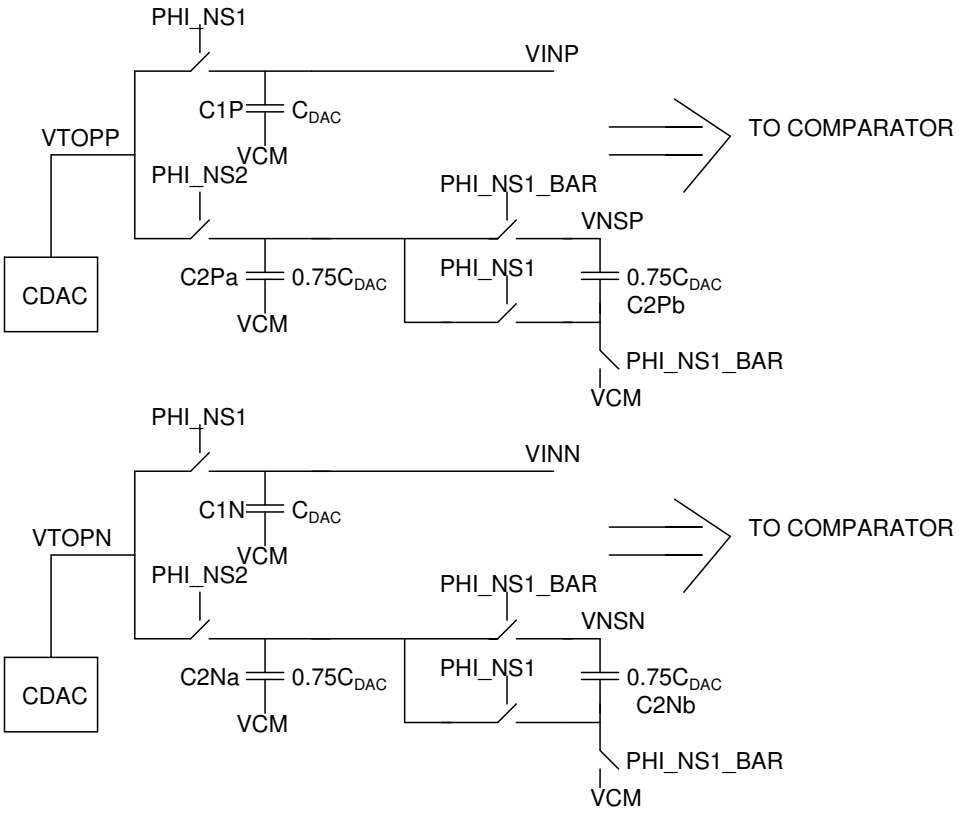

Figure 18: Fully passive second order filter with passive gain

During sampling time, the inputs are sampled onto DAC nodes. The capacitors C1P and C1N contain the residue from the previous sample conversion. During PHI_NS1, the inputs are sampled onto C1P and C1N, while the residue is also added to the inputs. After conversion, the residue from DAC capacitors are sampled onto capacitors C2P. The loss in residue due to sampling onto filter is compensated by passive gain. When PHI_NS1 is high, at the beginning of the bit cycle for the next sample, C2Pa and C2Pb(C2Na and C2Nb) are in series, giving a gain of 2. The transfer function including two zeros and a pole can be seen in [13].

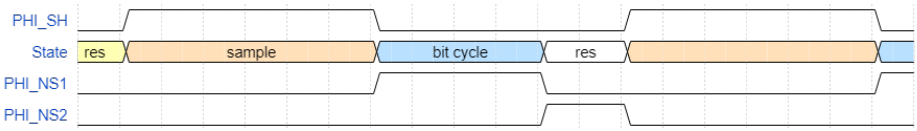

Figure 19: Fully passive second order filter with passive gain

4.5 Error Feedback SAR ADC Design

The architecture feeds back the residue to the CDAC instead of feeding the residue forward to the comparator. The residue is amplified by the comparator after the bit cycling. The residue is stored in a capacitor to be fed back to CDAC by charge sharing between the FIR capacitor and the CDAC. The comparator is the only analog component in the filter.

4.5.1 Comparator Design

The comparator needs to provide the residue gain during the integration time. The gain needs to be accurately controlled. So a bias current is used during the integration phase. The comparator is as shown in Figure 20. The input referred noise during bit cycling phase is 500 μV. The input referred noise during integration phase is 250 μV. VCOMP_RDY_BAR is high when comparator is in reset state and low when comparators have flipped. This signal is used in the asynchronous engine.

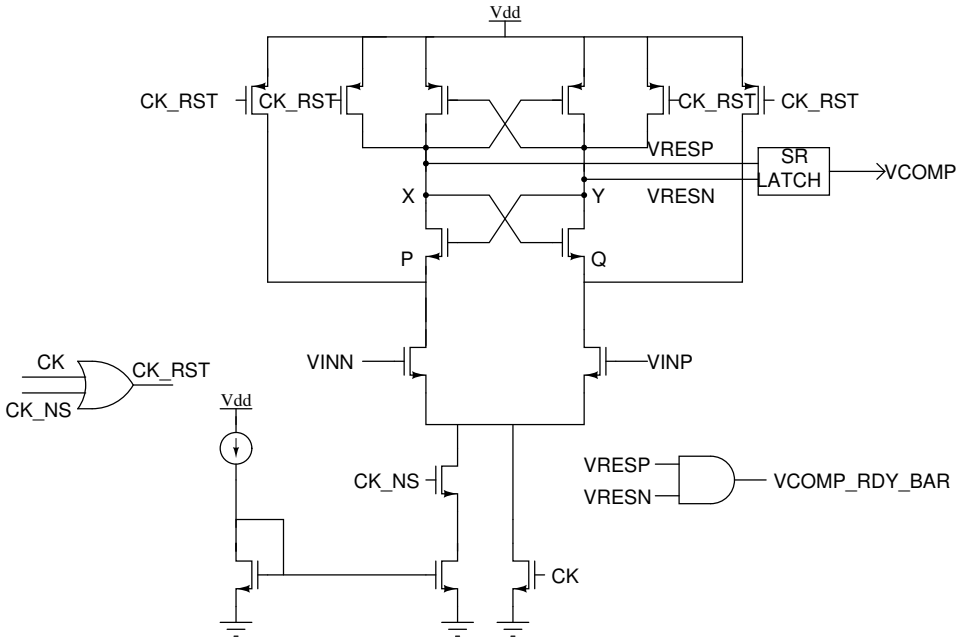

Figure 20: Comparator for Error Feedback Noise Shaping Filter

4.5.2 Filter Design

The filter architecture is shown in Figure 21. The clock waveform is shown in Figure 22. PHI_RST resets the capacitors C_{B2N} and C_{B2P}. During PHI_D2, the charge from $C_{B1P}(C_{B1N})$ is shared with $C_{B2P}(C_{B2N})$. During PHI_AMP, the amplified residue from the comparator is sampled by $C_{B1P}(C_{B1N})$ and $C_{AP}(C_{B1N})$. The output of the FIR filter is fed back to CDAC when PHI_EF is high.

The noise shaping transfer function can be written as:

$$LF(z) = 1 - GA_{CS}z^{-1} + 0.5 \cdot GA_{CS}z^{-2}; \tag{4.7}$$

where G is gain of comparator during residue amplification, and $A_{CS} = C_{RES}/(C_{DAC} + 2C_{RES})$.

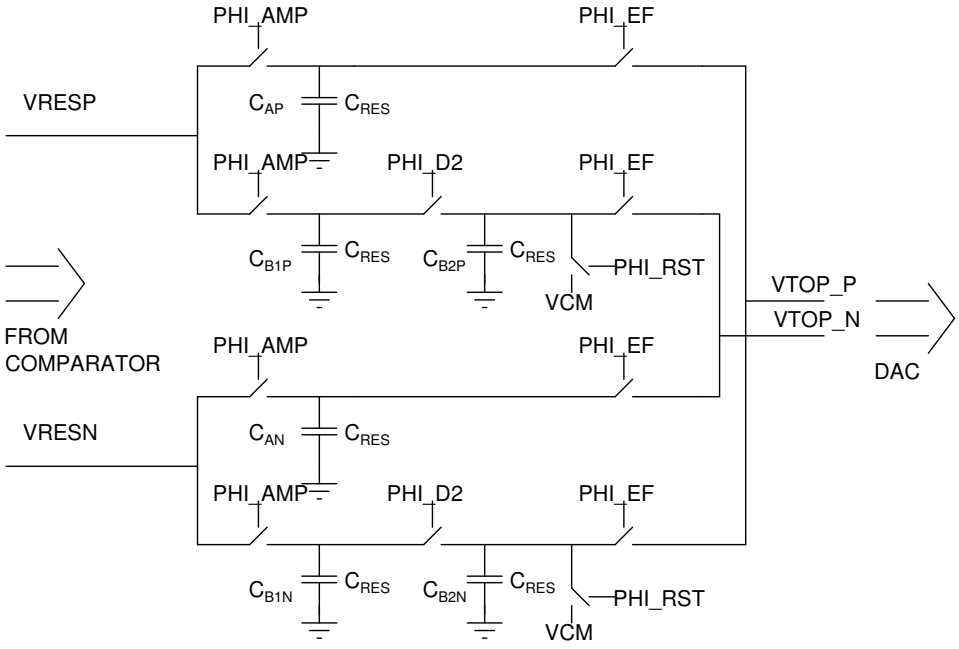

Figure 21: Filter for Error Feedback Noise Shaping Filter

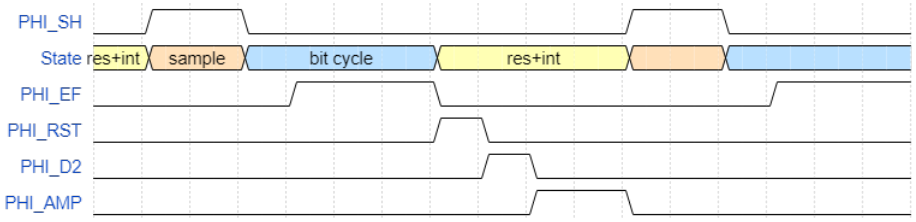

Figure 22: Clock Waveform for Error Feedback Noise Shaping Filter.

4.5.3 Timer Design

The integration gain needs to be accurately controlled to get the desired NTF. The gain is controlled using a common mode detection circuit, which shuts the switches from the comparator to the noise shaping filter when the common mode is reached. The circuit diagram is shown in Figure 23. The gain increases as the comparator proceeds through the integration phase and into the regeneration

phase. The gain is dependent on the current bias of the comparator and the filter capacitance. When the outputs of the comparator is below a certain common mode, PHI_INT_STOP_BAR goes low. This is used to pull down PHI_AMP which stops the integration operation. NEXT_BIT_<0> signal is used to prevent unnecessary toggling of the output signal. The output can only toggle low after the bit cycling is completed when it meets the condition stated above.

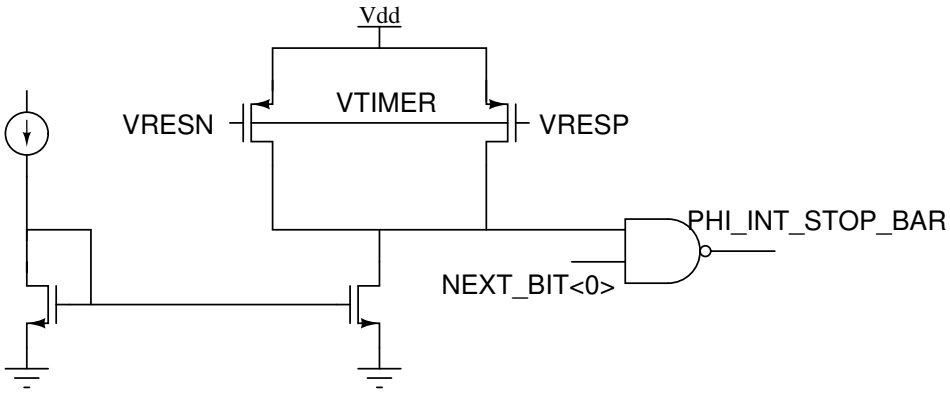

Figure 23: Timer Circuit Diagram

4.5.4 Choice of Filter Capacitance

The FIR capacitor should be high enough to lower the comparator noise after amplification. Higher FIR capacitance implies larger charge sharing from FIR capacitance to CDAC, implies lower A_{CS}, so the gain of the comparator has to be increased. Since the common mode to get a desired gain from the comparator is not the same as the DAC common mode(set by the input signal), any mismatch in capacitance between the DAC nodes or between the FIR filter output nodes will lead to wrong charge transfer to the CDAC. This will result in corruption in noise shaping. So, a small FIR filter is good as long as its noise contribution is lower than the output referred noise of the comparator. Care should be taken for systematic mismatch in layout as it can corrupt the coefficient in filter transfer function. The filter capacitance of 17 fF for this design was found to be sufficient. The input referred noise of the comparator is simulated using PSS/PNOISE analysis. The noise is modelled in the Python model and the impact is checked.

4.5.5 DAC Design

VCM switching is used to reduce the switching energy compared to the conventional DAC. Top plate sampling allows MSB decision to be made immediately after the sampling phase, and does not need hold phase like in the conventional switching scheme. The voltage change after decision is from VCM(half supply voltage) to either ground or supply. Thus the switching scheme is more energy efficient than the conventional scheme, where the plates change from VREF(supply voltage) to ground or vice-versa.

The layout of a part of DAC is shown in Figure 24. The capacitance is based on capacitance

between the side surfaces of the metals. CTOP and AVSS lines are regularly placed. The bottom plates of capacitors are uniformly picked up at the left in Figure 24.

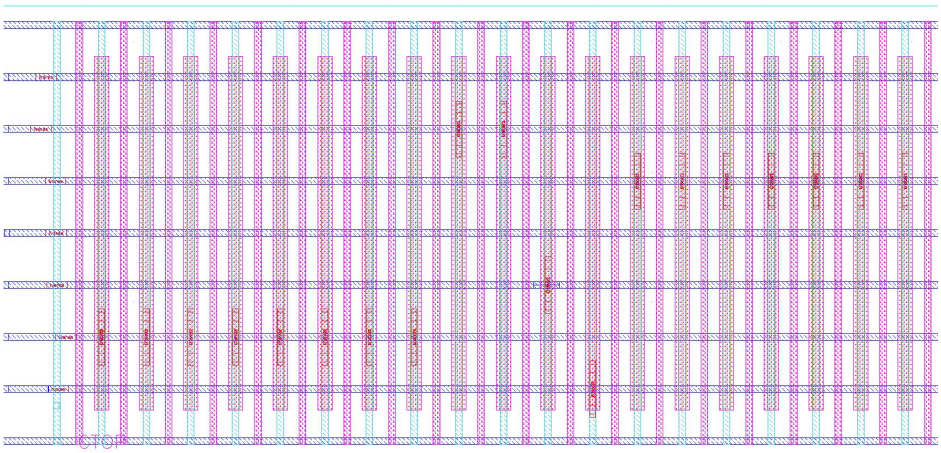

Figure 24: Several DAC unit cells

4.5.6 Bootstrapped Switch Design

The bootstrapped switch design is based on [14]. The circuit is shown in Figure 25. PHI1 and PHI2 are non-overlapping clocks. In the design, PHI1 is buffered version of sample clock, PHI_SH and PHI2 is the pulse for residue amplification, PHI_BAR, inverted version of PHI1. When PHI2 is low and PHI2 is high, capacitor C1 is charged to AVDD and VG is set low. When PHI1 turns high, MP3 switches on due to MN6, and VG starts charging towards supply. MN2 turns on once VG is sufficiently high, and VCB equals VIN. Due to charge conservation, it can be seen that VG equals VDD + VIN. Gate-source voltage of MNSWITCH is then kept constant at VDD. In addition, MNSWITCH is a slvtnfet transistor, which means increasing the body bias reduces the threshold, reducing the on resistance. Therefore, VG is used as the body voltage of MNSWITCH. MNSWITCH is a NMOS in NWELL transistor, so its NWELL tap is connected to VG.

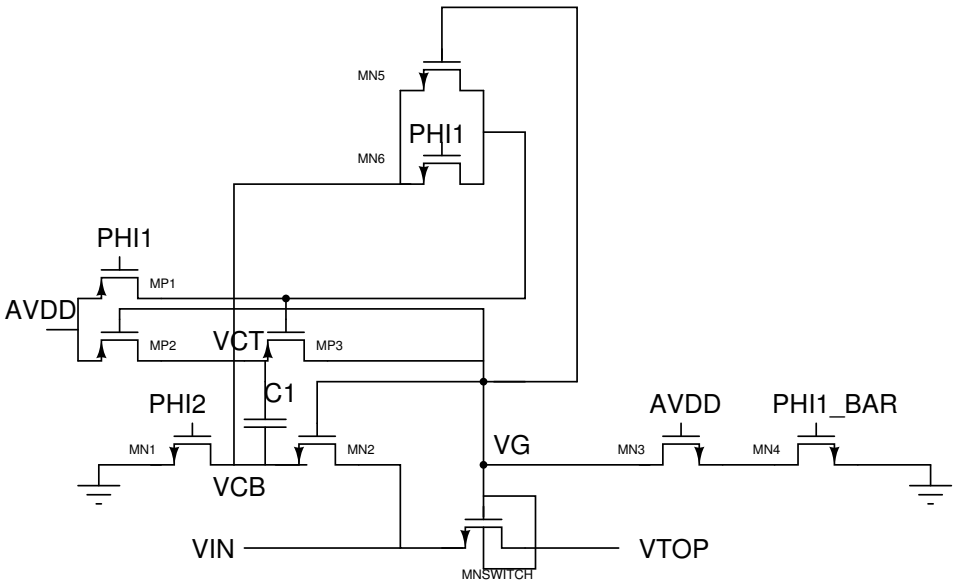

Figure 25: Boot Strapped Switch for sampling input

4.5.7 Digital Design

The SAR logic derived from [15] is modified to include VCM switching. The waveforms are shown in Figure 26. In brief, when BIT_SET is high, BIT_INT is set high. VCOMP_RDY_BAR is high during the reset state of comparator. COMPARE_BAR is pulled low, which sets the comparator clock, VCLK high. Once the comparator has decided, VCOMP_RDY_BAR is pulled low. The comparator decison, VCOMP is sampled on the falling edge of VCOMP_RDY_BAR. Meanwhile, NEXT_BIT_SET is set high which pulls VCLK low. The result of the decision is passed to the DAC bottom modes when NEXT_BIT_SET is set high. The DAC bottom plates are set at VCM when NEXT_BIT_SET is low.

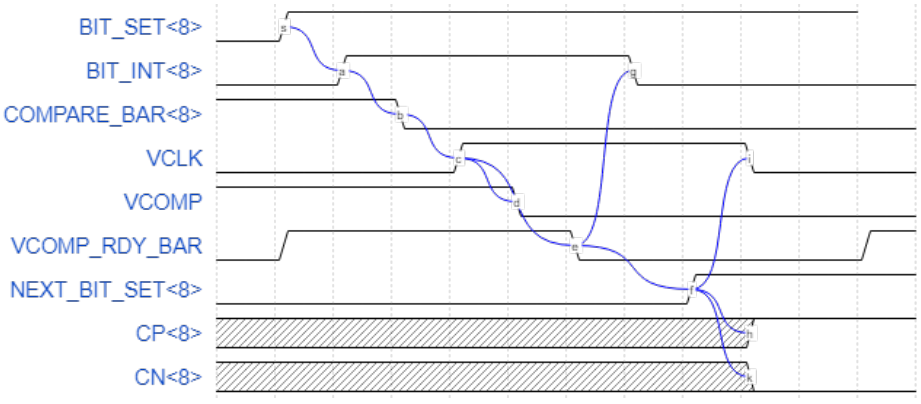

Figure 26: SAR logic

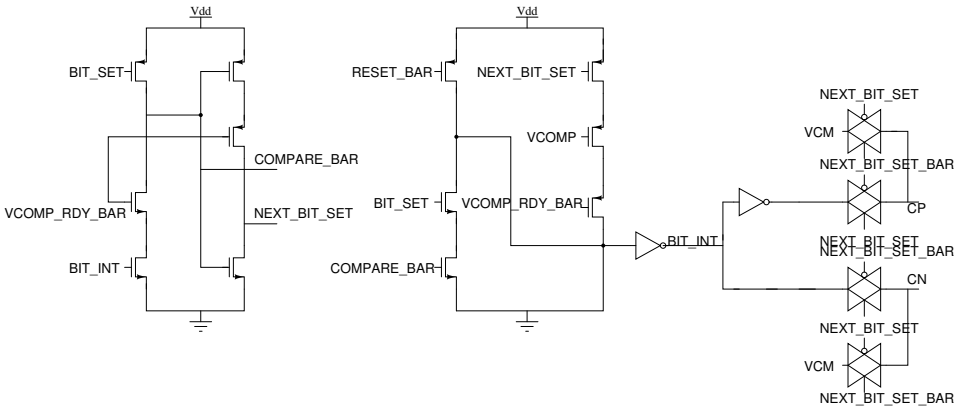

Figure 27: SAR logic circuit

The circuit level implementation is shown in Figure 27.

4.5.8 Discussion

A comparison of achievable FOM and ENOB is in Chapter 5. A discussion about the ease of design and challenges for the different filters can be found in Chapter 6.

4.5.9 Toplevel Layout

The layout of the error feedback noise shaping filter based ADC is as shown in Figure 28. The dimensions are 50X90, making a total area of 0.0045 mm^2.

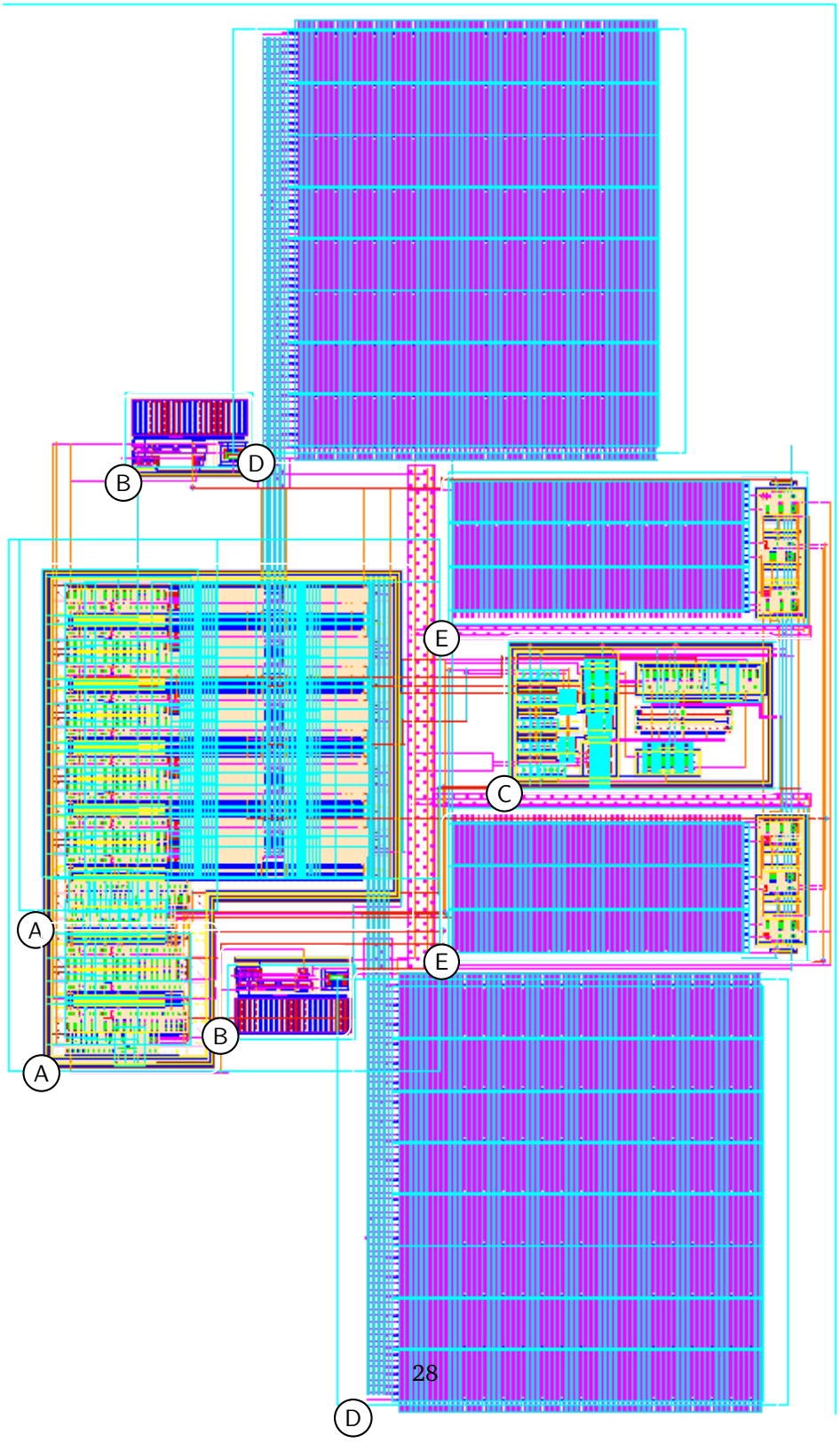

Figure 28: Top Level Layout – Digital (A), Bootstrapped Switch (B), Comparator (C), CDAC (D),FIR filter(E).

5 Results

5.1 Introduction

The impact of various parameters like number of bits in DAC, sampling frequency, comparator noise etc. were investigated to arrive at an optimum FOM in [11] using cascaded FIR-IIR filter structure. In this chapter, the results from the Python and Cadence model for each of the three types of noise shaping filters are presented. The Python models contain only the noise from the comparator and DAC. The filter noise and settling effects are not considered, but the comparator noise during the integration phase in error feedback(EF) SAR ADC is included in model. So, Python models are used as sanity checks and specification drivers. The models are then built in Cadence. The comparator and the filter are implemented in circuit level. For the case of the cascaded FIR-IIR and fully passive filters, the switches in filter are still ideal with an on resistance that generates noise, while for the Error Feedback the switches are in transistor level. The transient noise results from Cadence simulations include all the above noise sources and settling effects. So, the Cadence model results are expected to be worse than the Python results. The results from fully passive and cascaded FIR-IIR filters are from schematic implementation. The results from error feedback filter are from schematic and post layout simulations.

The input frequency for all results is 9.375MHz, which is so chosen to get an ENOB slightly better than 11 in Python simulations. From [11], the required sampling frequency for the final design is 160MHz and 9 b DAC with LSB of 320aF. All the schematic simulations are with ideal DAC and no parasitic to ground. Only the error feedback noise-shaping ADC is simulated in post layout C extracted netlist. The bandwidth for SNR extraction is twice the input bandwidth. The Fmax for transient noise analysis is 30GHz. The lower bound is set by the simulation time, set by the number of points of FFT. All Cadence simulation results are with 512 point-FFT, and all Python simulation results are with 4096 point-FFT. The input amplitude for all schematic simulations is 0.4V. It is changed to 0.28V when the CDAC is included as extracted netlist.

5.2 Python Model Results

The results from Python models that were used to arrive at specifications for the design are presented. In addition, in each section, the corresponding value achieved in design is also reported, wherever applicable.

5.2.1 ENOB vs Comparator Noise for different loop filters

The comparator input referred noise is swept to find the specification to achieve the desired ENOB. It is clear that the first order fully passive filter will not fulfill the requirements because the noise shaping is too weak. FIR IIR filter gives better ENOB for the same comparator noise. In reality, since

FIR IIR filters has two pairs of inputs one for the noise-shaping, and one for the DAC nodes, the effective load capacitance is higher to achieve the same input referred noise as for the EF case. The differential input referred noise looking at VINN and VINP is 500 μV when VNSP and VNSN nodes are grounded. The noise increases to 1000 μV when VNSP and VNSN nodes are kept at common mode of half the supply voltage. The ENOB with 1000 μV for FIR IIR filter is almost same as EF filter with 500 μV. It can be seen from Figure 29, that input referred noise of 500 μV is sufficient for Error Feedback(EF) Filter and about 1000 μV for cascaded FIR-IIR filter. Note that for the purpose of this simulation, the noise of comparator during amplification in EF structure is kept at 250 μV.

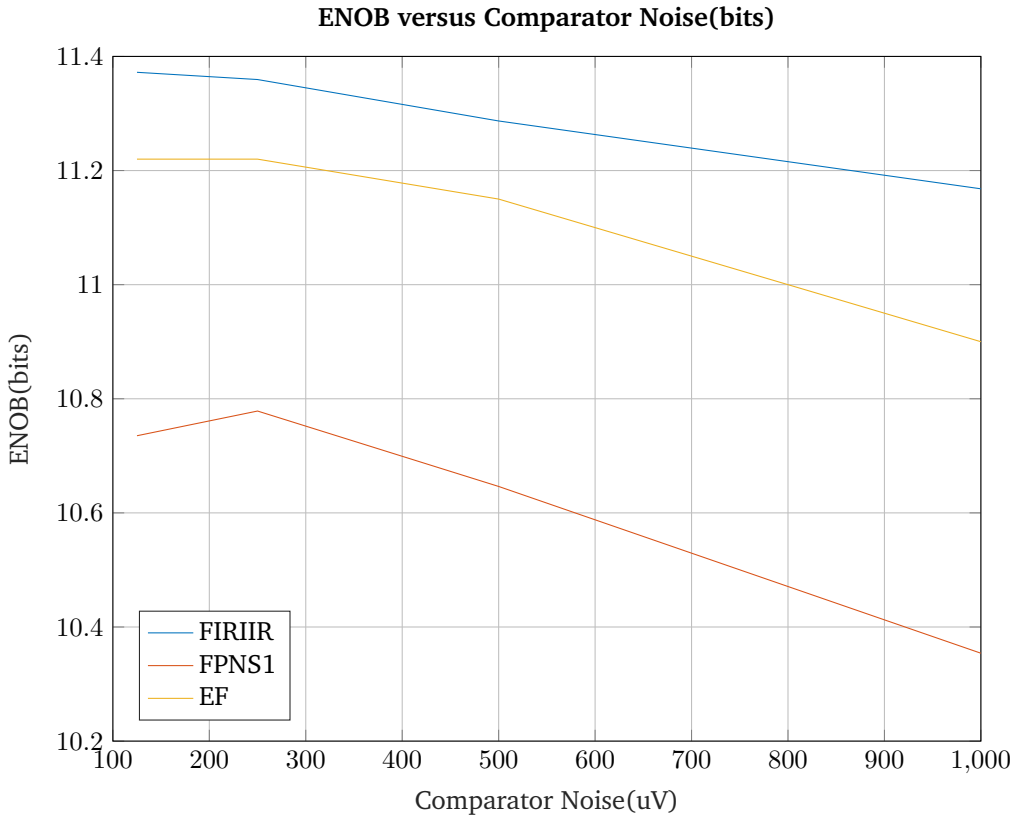

Figure 29: ENOB with comparator noise for the different loop filters. Sampling frequency is 160MHz. Input frequency is 9.375MHz. DAC LSB is 320aF.

5.2.2 Choice of DAC LSB

The LSB of DAC is swept to check the minimum LSB needed to get the desired ENOB. The sweep is only done for the cascaded FIR IIR filter, but the result applies for the EF filter case as well. The minimum LSB needed is around 150 aF for ENOB of 11 bits. The DAC LSB is chosen as 320 aF. With

that value, the DAC no longer affects the ENOB. It was also a convenient LSB from layout point of view. The DAC unit is made of 64 unit cells. The size of vias dictate the height of the DAC unit. Once the height of the unit cell is fixed, the LSB is fixed for the given structure. This is clearer in Chapter A.10, where the layout of CDAC is presented.

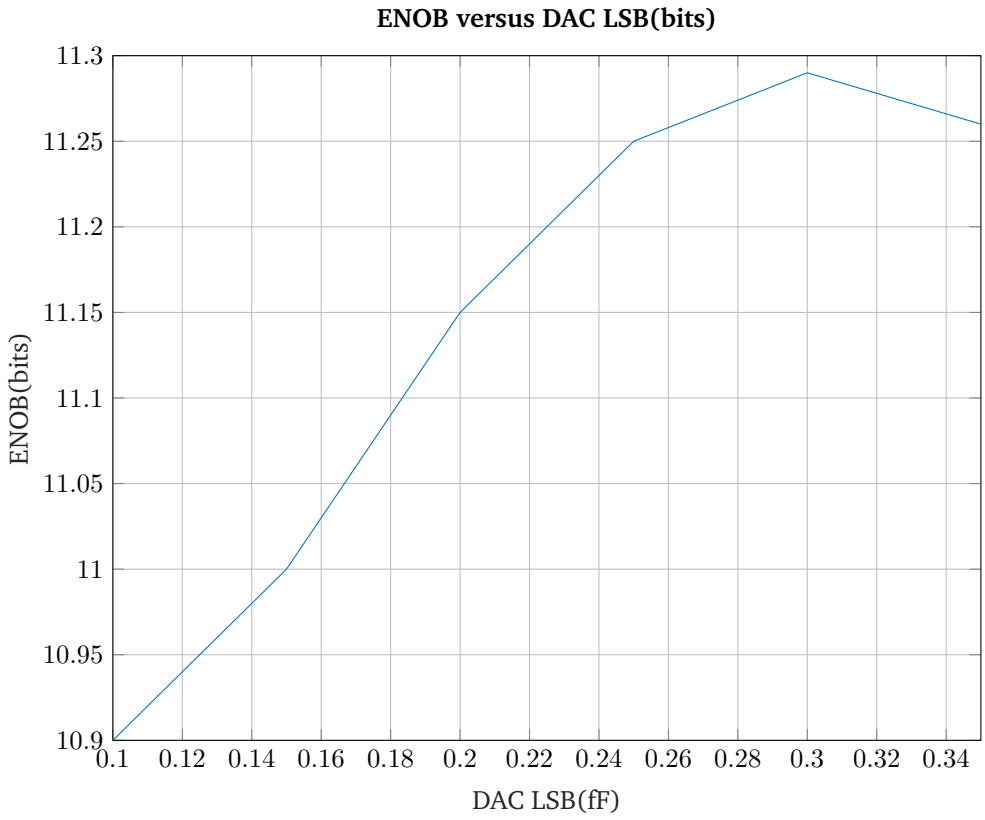

Figure 30: ENOB with DAC LSB for cascaded FIR IIR filter. Comparator input referred noise is 1000 μV.

5.2.3 ENOB vs Comparator Gain for Error Feedback Filter

The gain for the residue from the comparator needs to be accurate to get the best noise-shaping for the EF filter. It should be noted that the required gain changes with capacitor ratio between FIR filter and CDAC as can be interpreted from the transfer function in Section 4. Higher the CRES, lower the A_{CS} and thus, lower the gain. This means that the gain needs to be changed whenever parasitic capacitors change significantly. Figure 31 shows that gain of around 18 gives the best results when CRES = 17 fF and gain of around 12 gives best results for CRES = 25 fF. It can be seen that ENOB of 11 can be achieved with EF structure with the correct gain. For a CRES of 10 fF, the gain for peak ENOB is 30.

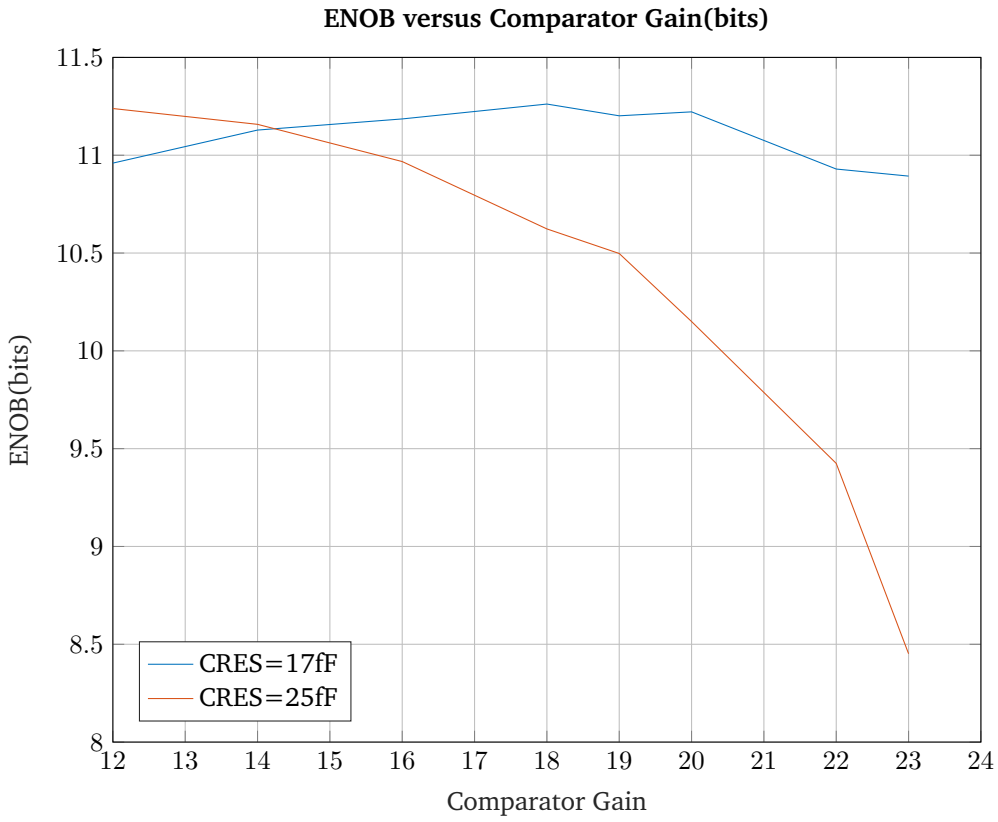

Figure 31: ENOB with gain of comparator during the residue amplification time. The comparator noise is 500 μV during the comparison phase and 250 μV during the residue amplification phase. CRES=17 fF and 25 fF.

5.2.4 ENOB vs Comparator Noise During Integration Phase for Error Feedback Filter

The specification for the input referred noise during residue amplification is obtained by sweeping the noise for the same gain and filter capacitance. It can be seen from Figure 32, that the required noise is at least around 350 μV. From design, the noise is around 250 μV.

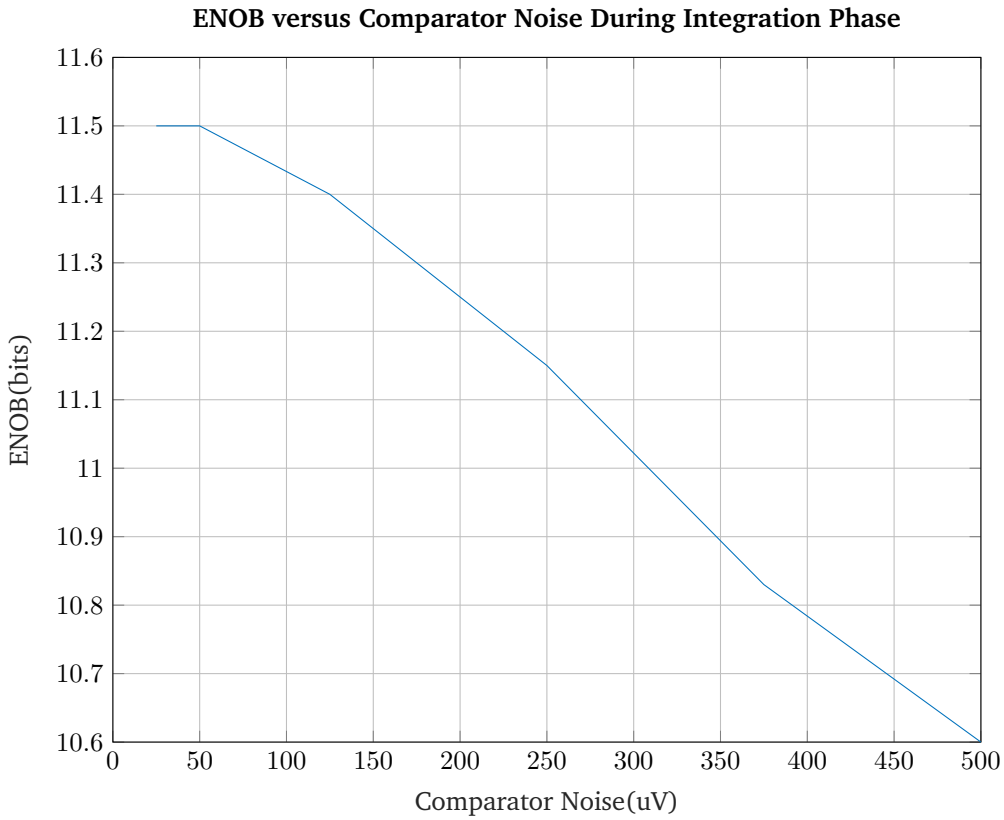

Figure 32: ENOB with input referred noise of comparator during the residue amplification time. The comparator noise is 500 μV during the comparison phase. CRES = 17 fF, gain of comparator is 18 for best ENOB.

5.2.5 Spectrum

The FFT plots for the different loop filters are presented. It can be seen that cascaded FIR IIR and EF filter give better noise shaping than the fully passive first order filter. A small notch around 15MHz can be seen in Figure 36, signifying the zero in the residue transfer function. The comparator noise and achievable ENOB are reported with the figures.

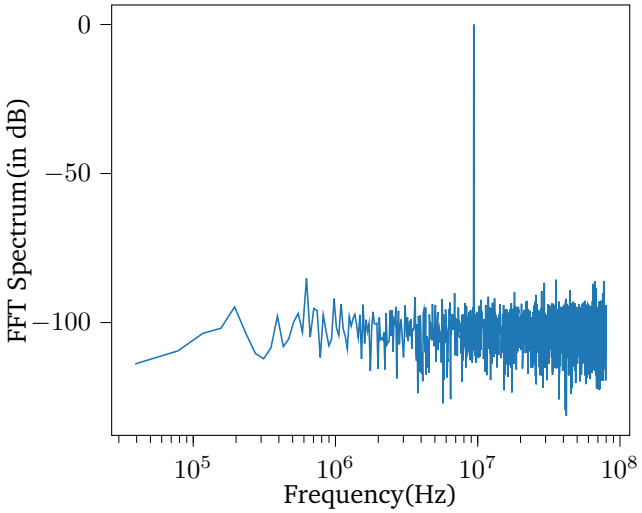

Figure 33: 4096 point FFT for ADC with no noise shaping. The input referred comparator noise is 500 μV. ENOB is 9.7 bits.

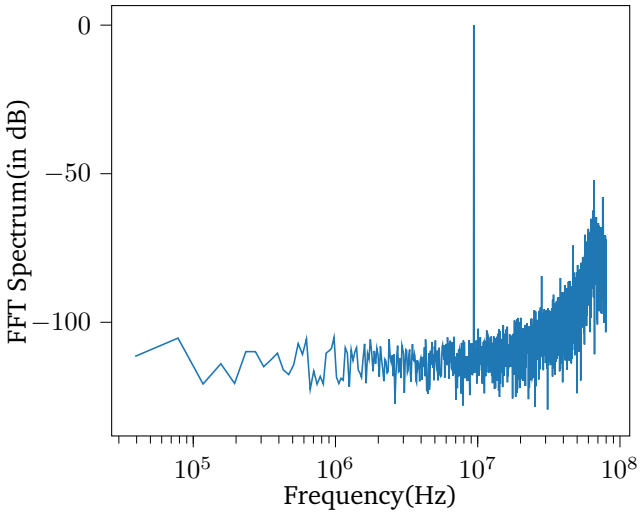

Figure 34: 4096 point FFT for ADC with cascaded FIR IIR loop filter. The input referred comparator noise is 1000 μV. ENOB is 11.2 bits.

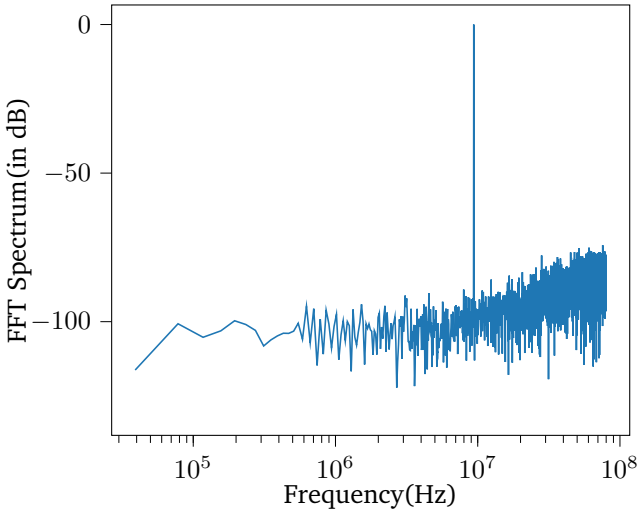

Figure 35: 4096 point FFT for ADC with Fully Passive First Order Filter. The input referred comparator noise is 2000 μV for DAC side and 500 μV for loop filter side. ENOB is 9.3 bits.

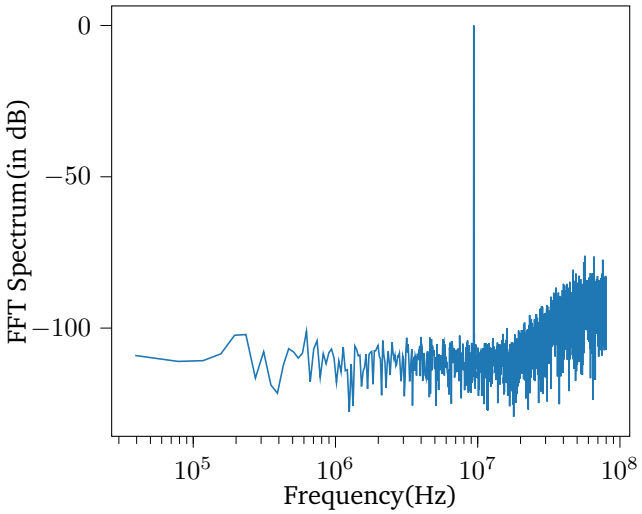

Figure 36: 4096 point FFT for ADC with Error Feedback Noise Shaping Filter. The comparator noise is 500 μV during comparison and 250 μV during residue amplification. ENOB is 11.15 bits.

5.3 Circuit Implementation Results

5.3.1 Schematic vs Python Model Results

The Cadence model is built so that the ideal models can be easily replaced by schematic netlist to verify block performance. The transistor level design is built for the comparator and loop filter

to replace the ideal components. The results from the Cadence schematic simulations and Python models are presented here. The results agree well for the different loop filters, except the cases of no noise of cascaded FIR-IIR and FPNS, possibly due to settling issues in schematic. But the schematic simulations agree well for noise-enabled cases for all the loop filters. The EF and FIR-IIR provide similar ENOB as expected from the Python simulations.

Filter	Type	Noise Enabled	Max ENOB(bits)
FIRIIR	Python	No	12.4
FIRIIR	Schematic	No	11.9
FIRIIR	Python	Yes	11.2
FIRIIR	Schematic	Yes	11.03
FPNS 1^{st} Order	Python	No	11.5
FPNS 1^{st} Order	Schematic	No	11
FPNS 1^{st} Order	Python	Yes	9.3
FPNS 1^{st} Order	Schematic	Yes	9.4
EF	Python	No	12.1
EF	Schematic	No	12.1
EF	Python	Yes	11.15
EF	Schematic	Yes	11.1

Table 1: Comparison of Filter performance from Schematic and Python Simulations

5.3.2 Cascaded FIR-IIR Filter Schematic Simulation Results

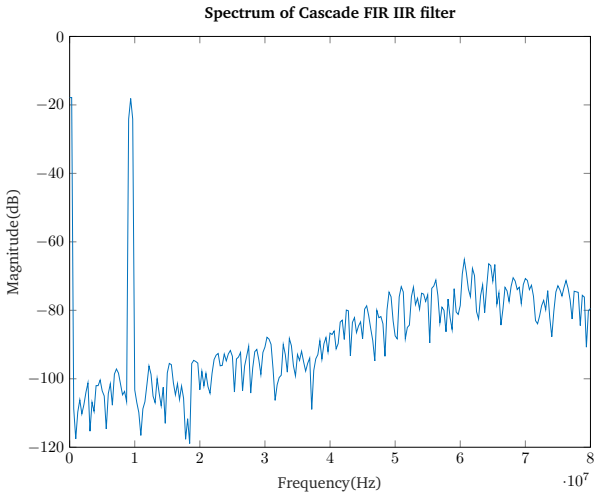

Figure 37: 512 point FFT for ADC with cascaded FIR IIR loop filter. The input referred comparator noise is 1000 μV from simulation. ENOB is 11.03 bits.

5.3.3 Fully Passive Filter Schematic Simulation Results

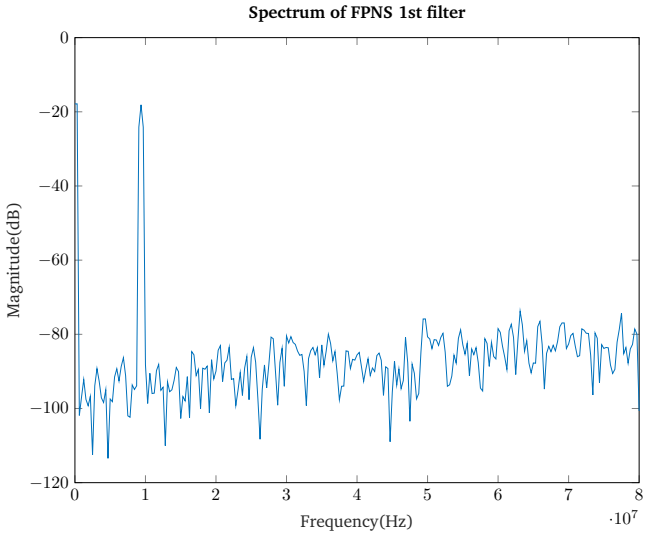

Figure 38: 512 point FFT for ADC with Fully Passive First Order filter. The input referred comparator noise is 2000 μV from VINN, VINP and 500 μV from VNSN, VNSP. ENOB is 9.4 bits.

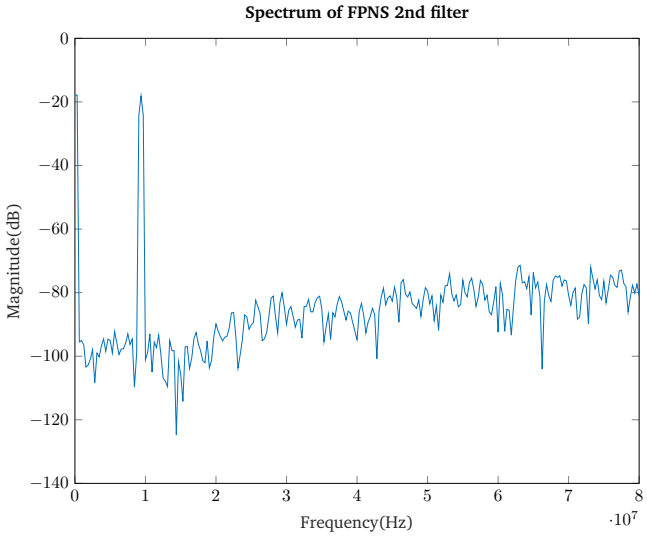

Figure 39: 512 point FFT for ADC with Fully Passive Second Order filter. The input referred comparator noise is 1000 μV. ENOB is 10.2 bits.

5.3.4 Error Feedback Filter Schematic Simulation Results

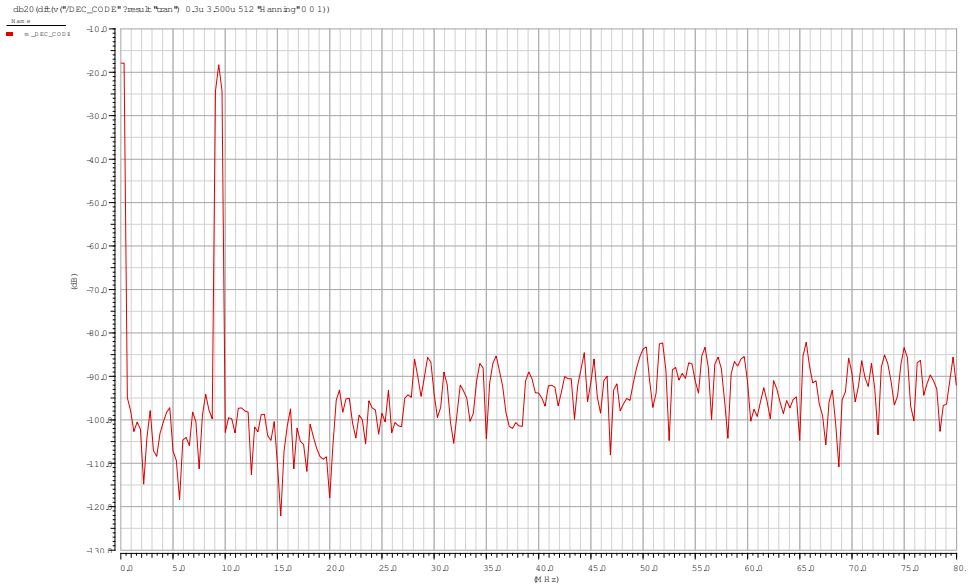

Figure 40: 512 point FFT for ADC with Error Feedback Noise Shaping Filter. The comparator noise is 500 μV. ENOB is 11.1 bits.

5.3.5 Expected FOM for different loop filters

LF	Max ENOB(bits)	LF Current(uA)	Total Current(uA)	FOM(fJ/step)
FIRIIR	11.03	278	478	9.7
FPNS 1^{st} Order	9.42	168	368	22.9
FPNS 2^{nd} Order	10.2	104	304	11.0
EF	11.13	160	360	6.8

Table 2: Comparison of FOM from Schematic Simulations

From Table 2, it is observed that EF filter is the most energy efficient for the given specifications.

5.3.6 Error Feedback Filter Post Layout Simulation Results

The ENOB in schematic simulations without DAC parasitic capacitors on top nodes is 11.1 bits. The parasitic capacitors degrade the SNR because the effective LSB is decreased by the ratio of the parasitic capacitors to CDAC capacitor, but the input referred noise remains the same. This is reflected as a decrease in ENOB. The ENOB vs input differential amplitude is shown in Figure 41. The input amplitude of 0.28V is used for all layout extracted simulations. With that amplitude, the digital output codes are almost full scale. The simulated max ENOB is 10.8 bits.

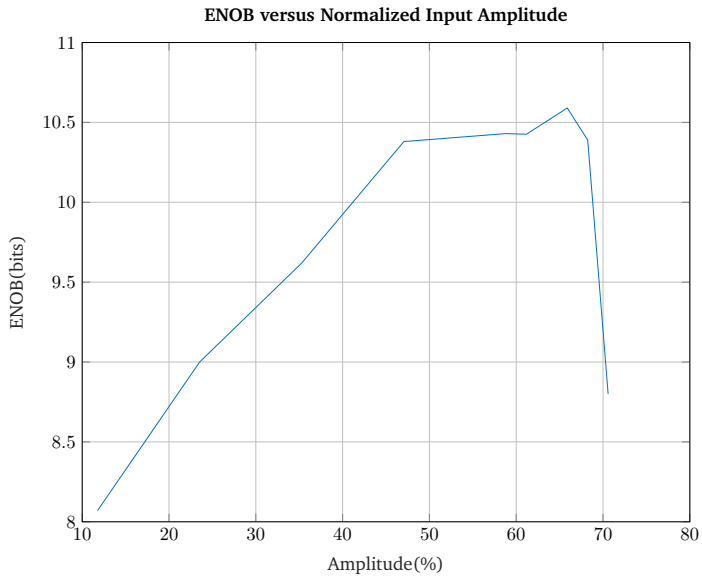

Figure 41: ENOB vs input differential amplitude. The supply voltage is 0.85 V.

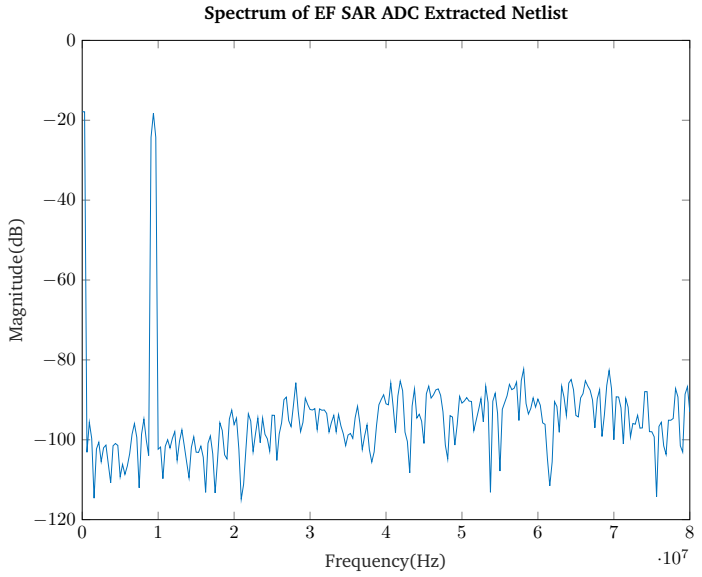

Figure 42: 512 point FFT for ADC with Error Feedback Noise Shaping Filter. ENOB is 10.8 bits. The input signal has an amplitude of 0.28 V. The supply voltage is 0.85 V.

5.3.7 DAC Post Layout Simulation Results

The DAC is simulated using AC analysis. The LSB is 320 aF. The total DAC capacitance is about 163 fF. The capacitance from CTOP to ground is 67 fF. Thus, the parasitic capacitance ratio is about 29%.

5.3.8 DAC and Filter Post Layout Simulation Results

The DAC and filter extracted netlist is inserted into Cadence model to check the impact on non-linearity and ENOB. In Figure 43, ENOB vs comporator gain is plotted from the Python model, Cadence model with DAC ideal and filter in extracted view, as well as Cadence model with DAC and filter in extracted view. It can be seen that the peak of ENOB is slightly shifted due to difference in ideal parasitics value and the value from the extracted netlist. Since the peak is for a narrow range of gain, the peak from the extracted simulation is missing in the figure. A finer sweep was run and presented in Figure 44, and it can be seen that the peak of the ENOB is similar. The results show that the DAC and filter nonlinearity should not decrease the ENOB of the ADC. In addition, a noise simulation was run, still keeping an ideal comparator. The peak ENOB was found to be 11.3 bits. This is the impact of DAC and filter noise. The need for accurate gain for comparator can be seen clearly from the above two figures. Since background calibration is not included for the simulations, a fine sweep is needed to get the results in case of schematic and layout simulations. This adds considerable design time for this case.

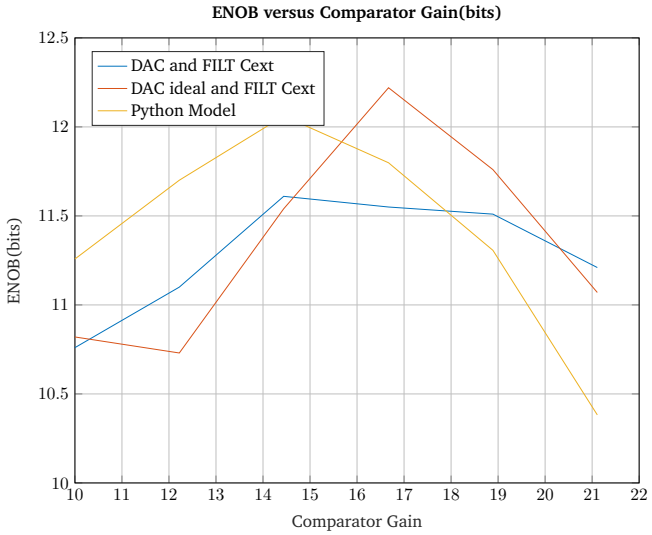

Figure 43: Comparison of ENOB vs gain for ideal model of DAC and filter and extracted view of DAC and filter.

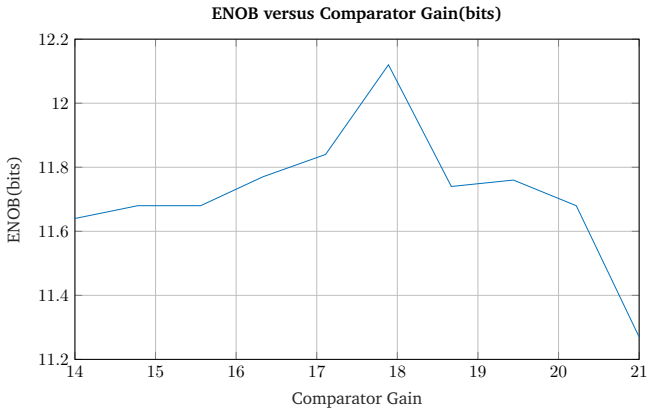

Figure 44: Comparison of ENOB vs gain for extracted view of DAC and filter. The gain is finely swept.

5.3.9 Boot Strapped Switch Post Layout Simulation Results

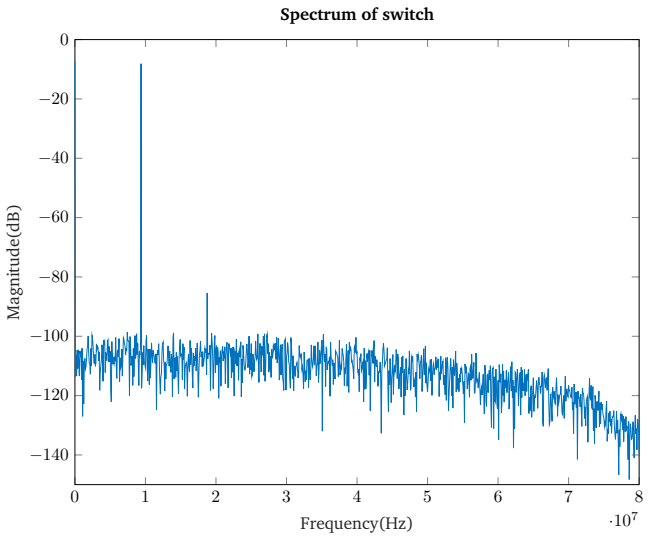

Figure 45: FFT of output with sample pulse width of 500ps.

The switch on resistance is 208 ohms, giving a time constant of 52 ps with 250 fF capacitance. Thus, for 11 bit accuracy, the required sampling pulse width is 432 ps. The sampling pulse width is set to 625 ps to allow for DAC and switch settling. Figure 45 is plotted assuming a sample pulse

width of 500 ps. The second harmonic is at -77 dBc, which is sufficient for 11 bit ENOB. The ENOB is 11.7 bits with input amplitude of 0.28 V in transient noise simulations.

5.3.10 Asynchronous Logic Post Layout Simulation Results

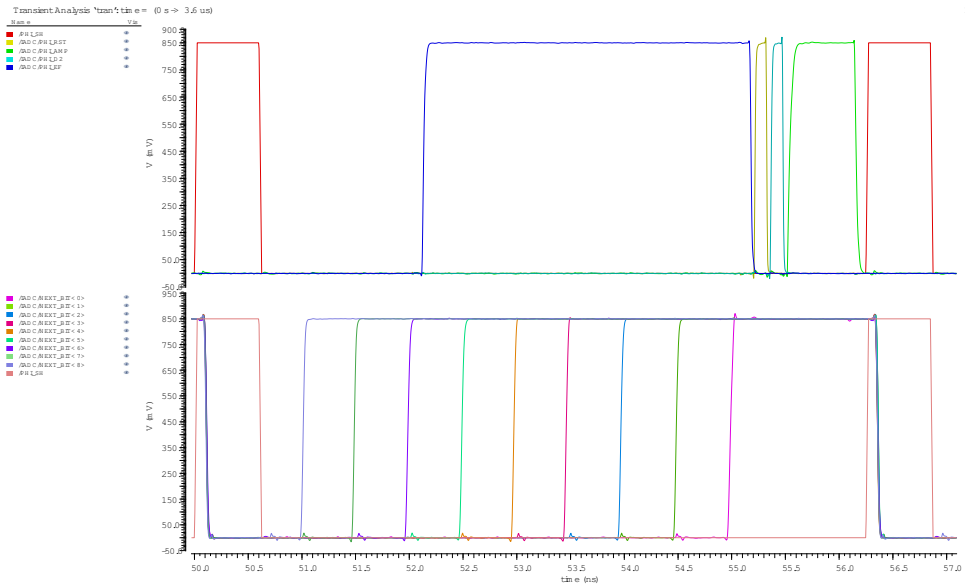

Figure 46: Digital signals. The top row is noise shaping related. The bottom row is bit cycle related.

It can be seen from Figure 46 that sampling time is approximately 600 ps, bit cycling takes about 4.5 ns. FIR filter operations and residue amplification takes the rest of the time, from the total time of 6.25 ns.

5.3.11 Comparator Gain vs Vtimer Post Layout Simulation Results

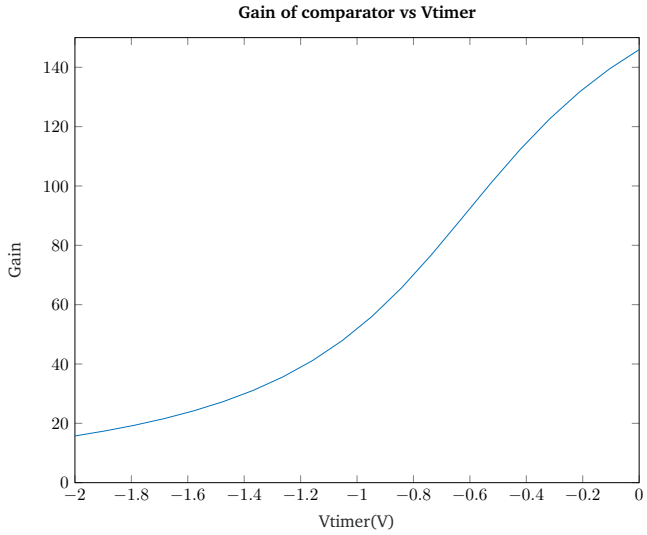

Figure 47: Comparator Gain vs vtimer.

A sweep of comparator gain vs Vtimer is plotted in Figure 47. Vtimer is the body bias potential of PMOS in timer circuit.

5.3.12 ENOB vs Comparator Gain Post Layout Simulation Results

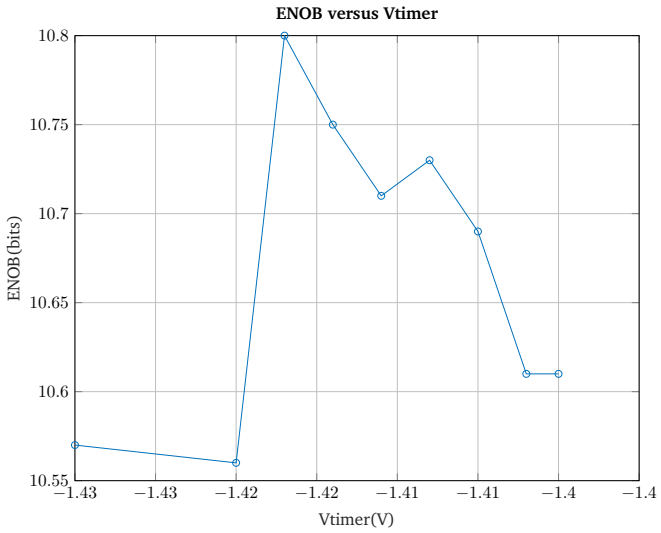

Figure 48: Comparator Gain vs vtimer from C Layout Extracted Simulations.

It can be seen from Figure 48 that the peak of the ENOB is 10.8. It is a bit sensitive to the window as Hanning window gives 10.8 bits and Rectangular window gives 10.9 bits. Since all other results are reported with Hanning window, the results with that window are used.

5.3.13 Power Consumption Breakdown

Table 3 summarizes the current consumption for each block for FOM for the error feedback ADC.

Block	Current Consumption(uA)	% of total
Clock Generation	163	32
Comparator(Bit cycling)	144	28.3
Comparator(Amplification)	90	17.7
DAC	112	22
Total	509	100

Table 3: Simulated Current Consumption Table

6 Discussion

6.1 Comparison of different loop Filters

There were three topologies studied during the course of the work. Based on the design work and results, the loop filter topologies can be compared in terms of ease of design, achievable FOM and merits and demerits. The error feedback filter provides the best FOM among the considered filters for the case of 11b ENOB in schematic level simulation. In addition, the absence of active integrator makes it easier to design. The topology needs calibration of gain for best ENOB. The linearity is difficult to achieve without first calibrating any offset capacitance on the output nodes of the comparator, followed by gain calibration for best noise shaping transfer function. The passive loop filters are power efficient for lower ENOB, but since noise-shaping is not very sharp, higher ENOB cannot be achieved in a power efficient way. The comparator noise dominates after around 10 bit ENOB due to shallow noise-shaping. The cascaded FIR-IIR filter has higher power consumption than error feedback filter for the given target specification, mainly due to additional power consumption in active integrator. An advantage over error feedback filter is the integration can be done during the sampling phase, while in error feedback topology, additional time needs to be given.

About the ease of design, the error feedback amplifiers without calibration takes a lot of simulation time to find the best gain, since a fine sweep is needed. The linearity of gain in loop is also sensitive to capacitance mismatch between the output nodes of the comparator as well as mismatch in capacitance between CTOP nodes of DAC. The ENOB is sensitive to setting the right gain and linearity. This makes top level simulations time consuming. A calibration loop for output capacitance of comparator and for gain is needed along with careful layout. The design becomes very robust, once calibration is added. Cascaded FIR-IIR filter has 2 critical blocks, comparator and integrator. They take longer to design, but are probably more robust, since the gain in filter is set by ratio of capacitors. The fully passive filters are the easiest to design, but noise shaping is not as good as the other filters. So they need more bits in DAC to achieve the same ENOB, which increases the current consumption in the DAC switching.

An additional advantage with the error feedback scheme is the ability to change the location of noise transfer function zeros by changing gain of comparator during integration. This is important if wide range on input bandwidths are targeted for the same sampling frequency, as well to adjust for mismatch. For cascaded FIR-IIR filter topology, the transfer function can only be changed by changing the ratio of the capacitors, which is not as easy. The same applies for the fully passive loop filters.

Sample clock pulse width should be large enough to decrease power consumption of the input buffers driving the ADC by allowing more settling time. The integration of error in noise shaping could take a good portion of the clock period to lower the power consumption. Since the sampling

frequency is high and the bit cycling time is finite for a given digital current budget, the sample clock pulse width time needs to be lowered for the error feedback filter. In case of cascaded FIR-IIR filters, the integration is done during the sampling time. So this allows lesser power consumption for the input buffers in the case of cascaded FIR-IIR filters.

VCM based switching scheme is used to reduce the power consumption of switching. In addition, with top sampling, the MSB decision can be made immediately made after sampling, which helps to operated at high sampling frequency. The voltage VCM is easily generated from a resistive divider from supply. Since the DAC is differentially switched, CDACP and CDACN hold charges of opposite polarity at the end of the cycle. During the sampling phase, when the bottom plates need to be charged to VCM, there could be a scheme to allow recirculation of charge between capacitors of opposite polarities. This saves power consumption in the VCM generation unit.

6.2 Gain Calibration of Error Feedback Loop Filter

A scheme for background calibration of gain can be seen in [8]. In brief, the calibration scheme injects a random residue voltage at the end of the bit cycle operation, by changing a bit randomly in the CDAC at the end of the conversion cycle. The residue is then sampled by the noise-shaping filter and is fed to the ADC loop in the next cycle. The binary code is also fed through a desired filter. The output codes of the ADC and the ideal path are then sent to an LMS algorithm engine. The output is converted to an analog value with another DAC, which needs moderate resolution(around 7 bits) and fed into the bulk voltage of the timer block to adjust the gain.

6.3 Back Bias

All the transistors in digital, comparator and filter are of SLVT(super low threshold) to design for the high sampling frequency. The body of SLVT transistors can be forward biased to meet settling constraints. In particular, it was useful when parasitic capacitors slow down transistions after layout. The schematic design was done without forward biasing, so there was a possibility to adjust the back bias by changing the bias voltage inputs at the testbench level, rather than re-laying out. The filter and comparator digital logic are fully forward biased to meet the sampling frequency requirement. The digital logic PMOS is forward biased, but not maximum, but the NMOS is not. The reason for that was the charge accumulation in asynchronous logic. The used asynchronous logic uses dynamic logic, which means there are chances for charge injection due to switching to integrate and flip the stored decision values. This was observed when the transistors became faster by forward biasing. There could be a more optimum point than current design, by adding more capacitance on the nodes to make sure that the decisions do not flip by applying more forward biasing. In that case, the supply voltage could be lowered potentially consuming less power and thus, better FOM.

6.4 Linearity

The mismatch of capacitance in the output nodes of comparator causes non-linearity in gain. This caused distortion, resulting in worse ENOB. For the current design, it is solved by manually adding a tiny output capacitor so that the gain value is same for negative and positive input voltage differ-

ence.

6.5 Kickback

Residue voltage in filter changes whenever output of comparator toggles because of coupling from source to grain node of transistors inside filter. The error feedback must be applied after the output of comparators have been reset to make sure the residue value are correct.

6.6 Sampling Frequency

Due to the fact that the digital could not be made faster by forward biasing due to the problem discussed above, and integration time allotment of around 800 ps to optimize power consumption, the sampling frequency was difficult to meet. As stated above, the input sampling phase had to be shortened. In addition, higher supply voltage needed to be used for digital than desired. The supply voltage used is 0.85 V for the entire ADC, about 6% more than the initial supply voltage of 0.8V used during schematic design.

6.7 Jitter requirement

The jitter requirement on sampling clock is given by equation 6.1.

$$SNR = 20\log_{10}(1/2\pi f t_j) \tag{6.1}$$

where SNR is achievable SNR due to aperture jitter alone, f is input frequency and t_j is rms aperture jitter. For ENOB of 11 bits and input frequency of 10MHz, the SNR needed is approximately 68dB. Using (6.1), $t_j = 6.3ps$. In addition to that, the input signal might have higher harmonics due to insufficient out of band filtering by anti-aliasing filter at the input. Assuming a jitter of 1ps, gives SNR of 70dB for 50MHz input frequency, 5^{th} harmonic of 10MHz. This is an achievable number on silicon for 160MHz clock without much circuit complexity.

6.8 Noise Contribution

Block	Percentage Contribution(%)
Quantization	27.5
Sampling	27.5
Comparator	45

Table 4: Percentage contribution of blocks to total noise

From Python simulations, individual noise contributions from DAC and Comparator can be switched off to determine the contribution of each of the main contributors to the total noise. The DAC capacitance is 164fF and comparator input referred noise during comparison is 500 μV and during integration is 250 μV.

6.9 Layout Optimization

The DAC parasitics from TOP nodes to ground is around 29%. The reference step and the inputs are attenuated in the same ratio. But, the comparator input referred noise is the same as before, thus decreasing the SNR of the ADC. The layout of the DAC needs to be optimized for lower parasitics on the TOP nodes. The layout could have been done with more symmetry than current layout. The mismatch on CTOP nodes is about 0.5%, which is compensated by dummy routing. The margin of achievable ENOB from required ENOB should have been higher to compensate for the loss in SNR. The layout floorplan could have been optimized more to get lower area. The filter has some extra area to add more capacitance later, which could be optimized.

6.9.1 Comparison to Prior Art

Table 5 compares the key results of the current work to some of the prior art published in ISSCC and VLSI Symposium. Predictive ADC is used for coarse bits in [4], which means 4 MSBs are switched immediately after sampling using prediction logic, decreasing conversion time. In addition, a dynamic amplifier is used to amplify residue before sampling at FIR filter. The input bandwidth is lower than this work in [8], which means comparator noise could be lowered by adding more capacitance to get better ENOB. The Fully Passive Noise Shaping in [5], has weak noise shaping, which results in low ENOB, even though the FOMW is good. Compared with [2], the power is lower in this work partly due to effect of scaling on digital current and partly due to absence of active integrator.

Specifications	[2]	[4]	[5]	[8]	This work
Architecture	CIFF	CIFF	FPNS	EF	EF
Opamp	Yes	No	No	No	No
Technology[nm]	65	28	65	40	22
Active Area[mm^2]	0.03	0.0049	0.012	0.024	0.0045
Supply[V]	1.2	1	0.8	1.1	0.85
Fs[MS/s]	90	132	50	10	160
Bandwidth[MHz]	11	5	6.25	0.625	9.375
OSR	4	13.2	4	8	8
ENOB	10	13	9.35	13	10.8
Power[μW]	806	460	121	84	433
FOM[fJ/step]	36	5.8	15	9	13

Table 5: Comparison to Prior Art

7 Conclusion

This thesis presented the modelling and transistor level design of noise shaped SAR ADC based on cascaded FIR-IIR, fully passive and error feedback loop filter topologies. The block specifications were derived from Python model, and the blocks designed to achieve the specification. The work compared the performance of the SAR ADCs with the loop filters from schematic simulations for the required specification, which is achieving as low FOM as possible for SAR ADC with close to 10 MHz bandwidth. Error feedback loop filter was found to be most energy efficient among the selected filters. A SAR ADC based on error feedback loop filter topology was laid out and simulations were carried out with extracted netlist. With input referred noise of comparator of 500 μV and 9 bit DAC, 10.8 bits could be achieved by error feedback noise shaping. The FOM for the designed ADC is 13fJ/conv-step with input frequency of 9.375 MHz. Operating at 160 MS/s, the SAR ADC consumes 509 μA from 0.85 V supply. The design was done in 22 nm FDSOI process, and the core area is 0.0045 mm^2. The performance of the SAR ADC is sufficient for the target application.

Table 6 summarizes the top level parameters of SAR ADC to achieve 10.8b ENOB with error feedback loop filter.

Key Top Level Specification	Value
DAC NBITS	9
DAC LSB	0.32fF
Input Differential Amplitude	560mV
Input Frequency	9.375MHz
Sampling Frequency	160MHz
Comparator Noise	500uV
Comparator Noise(Amplification)	250uV
Noise shaping	Error Feedback
Aperture Jitter	1ps

Table 6: Specification Table

7.1 Future Work

- Calibration: Calibration of DAC might be required to cancel non linearity and mismatch in DAC to achieve 11b ENOB across process. In addition, offset calibration for the comparator could be necessary to limit non-linearity in gain. Gain calibration is required to achieve the correct gain for the required noise transfer function.
- Digital: The digital circuit could be optimized further by using higher back bias voltage and decreasing the supply voltage.

- Conversion Time: Multi-bit SAR ADC decreases the conversion time. So the power efficiency can be improved.

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A Appendix

A.1 Matlab Code for Comparator Noise Post Processing

```
digout=load('digout1.matlab');

vin = digout(:,1);
avg = digout(:,2);

size_vin = length(vin);

% (2) inverse erf for rising slope only
% y(1:21) is this case contains the data
% for the rising slope
v = sqrt(2)*erfinv(avg(1:size_vin)*2-1);
% select values within  2 .5 ... 2.5 sigma
i=find(v>-2.5 & v<2.5)
% fit line through selected values
% Figure 5
[p,s]=polyfit(vin(i), v(i), 1);
plot(vin(i), v(i), vin(i), polyval(p,vin(i)))
% (4) compute mu and sigma
sigma = 1/p(1)
mu = -p(2)/p(1)
```

A.2 ADC EF Schematics

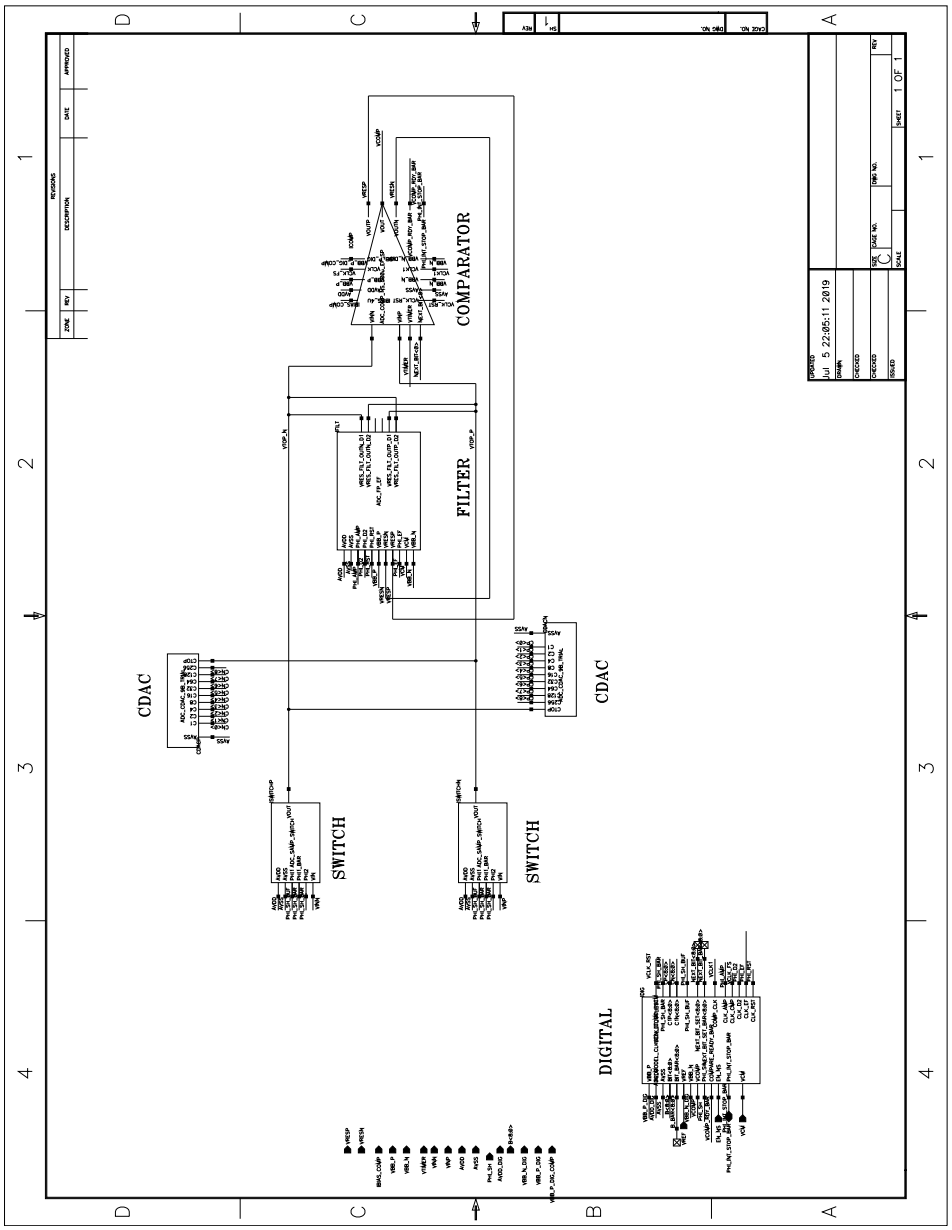


Figure 1: Top Level Schematic for Error Feedback Noise Shaping SAR ADC

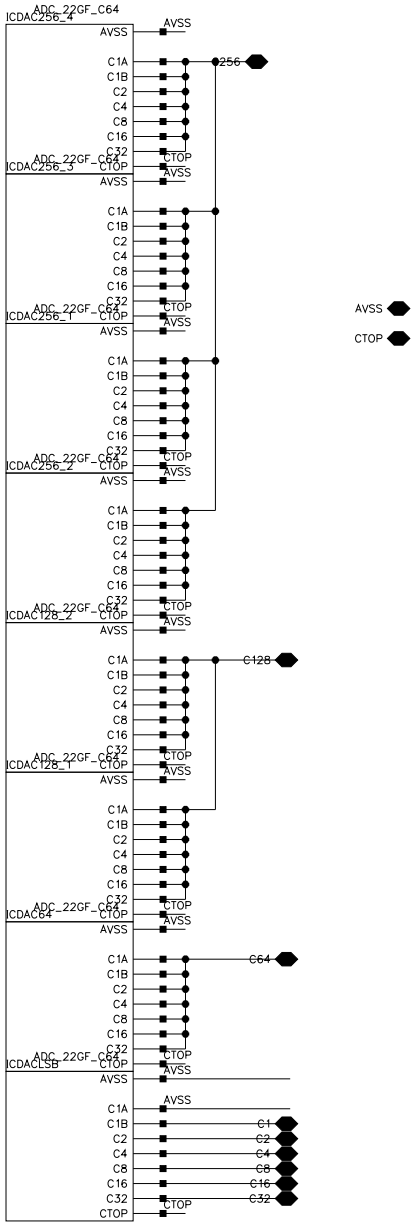


Figure 2: 9bit CDAC

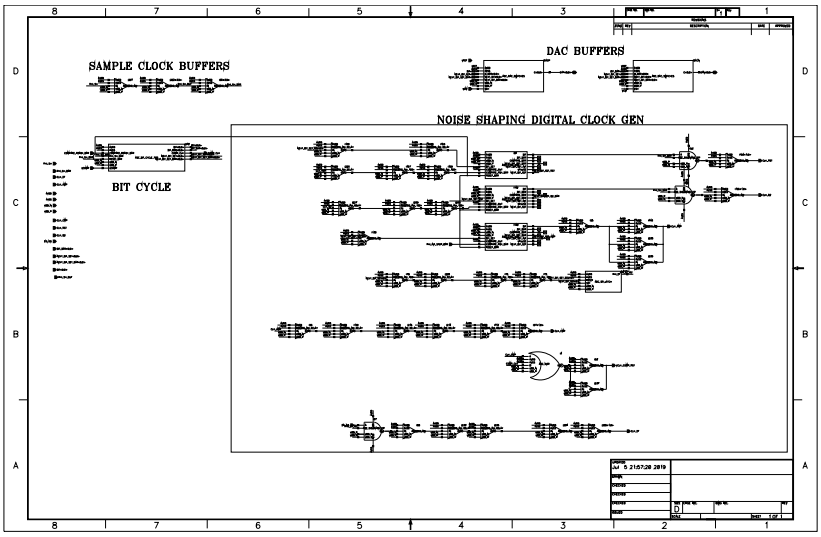


Figure 3: Digital Top

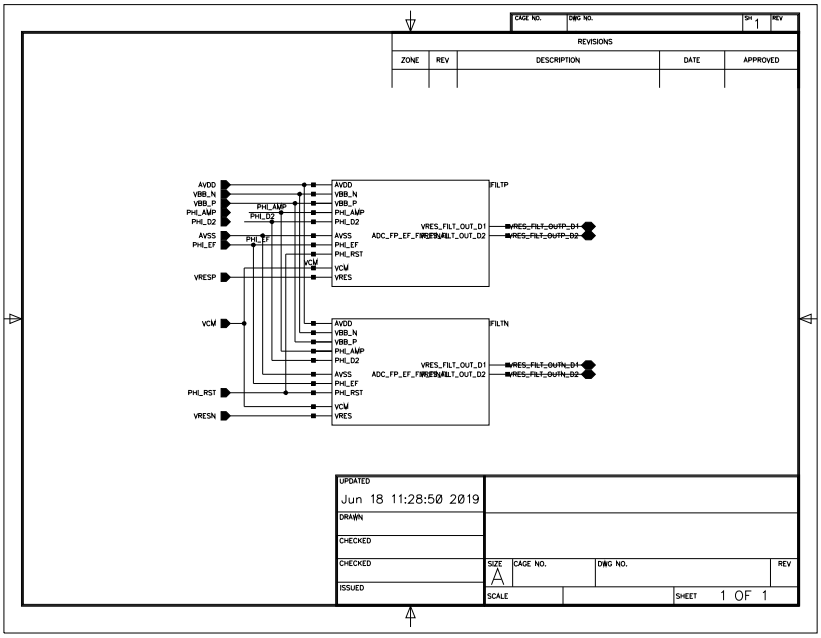


Figure 4: Filter Top

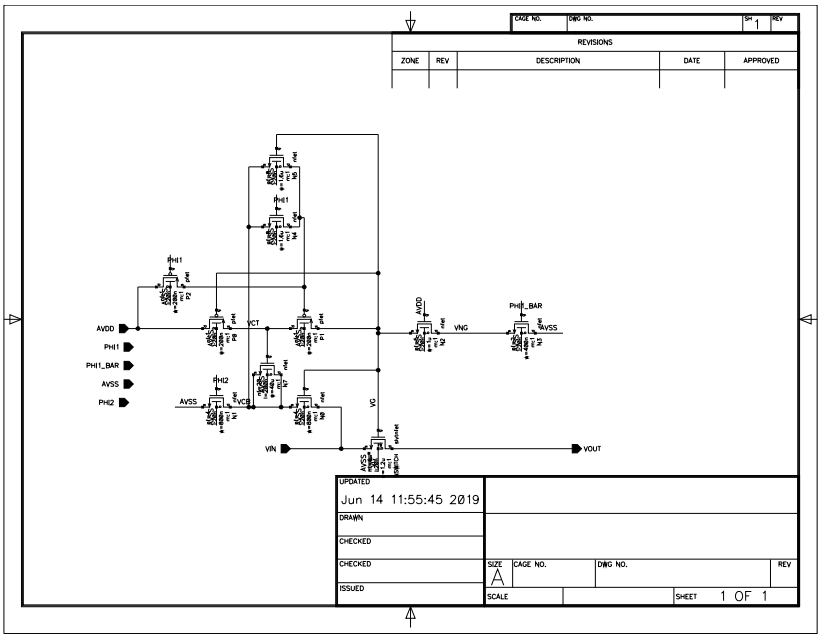


Figure 5: Bootstrapped Switch

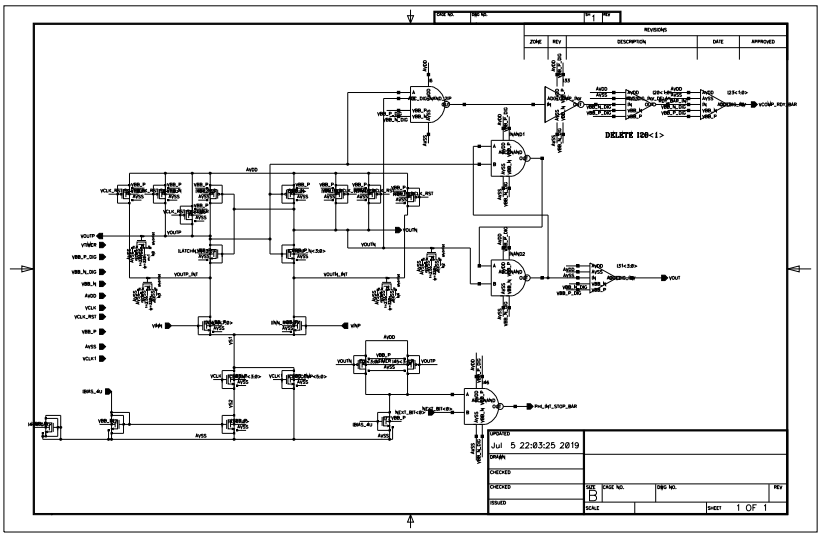


Figure 6: Comparator

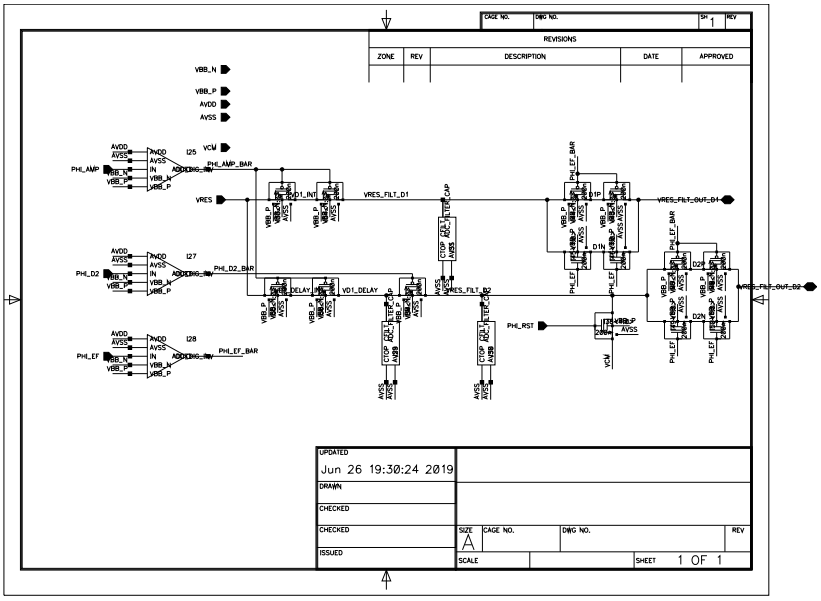


Figure 7: FIR filter

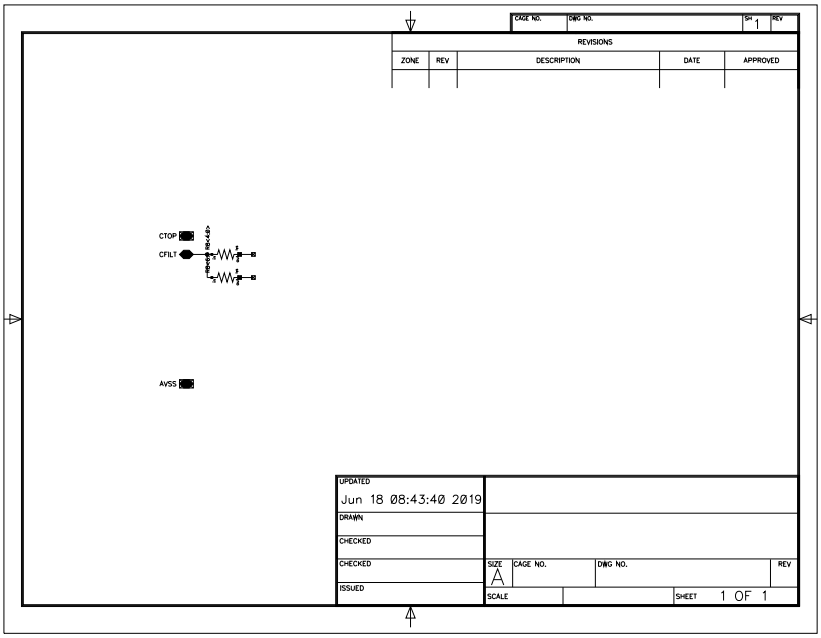


Figure 8: FIR filter cap

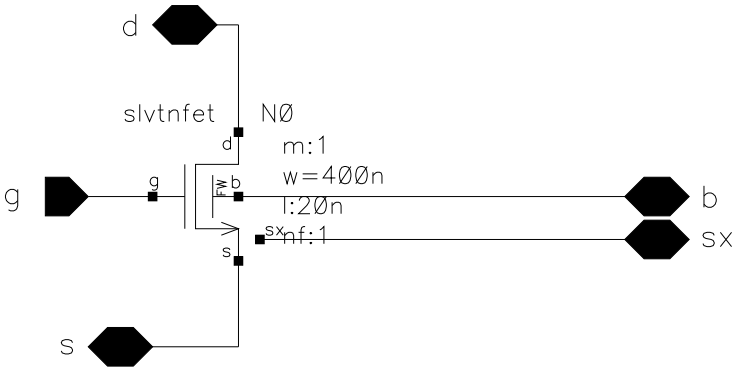


Figure 9: Comparator NMOS

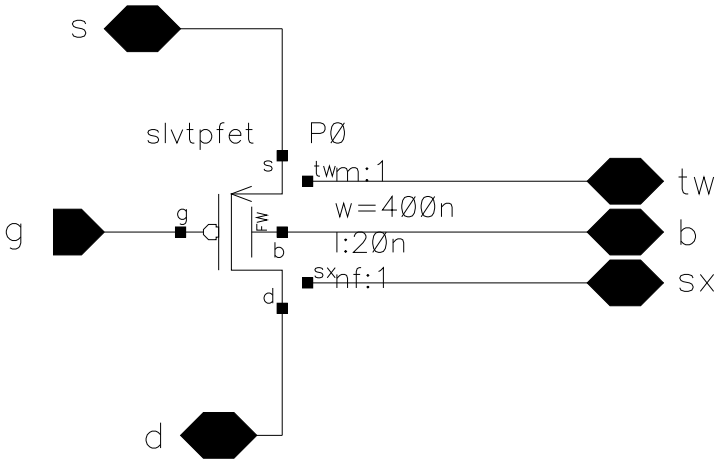


Figure 10: Comparator PMOS

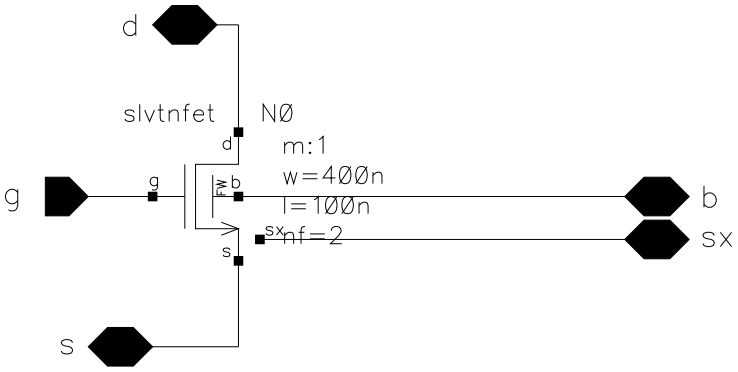


Figure 11: Comparator NMOS in the Current Mirror

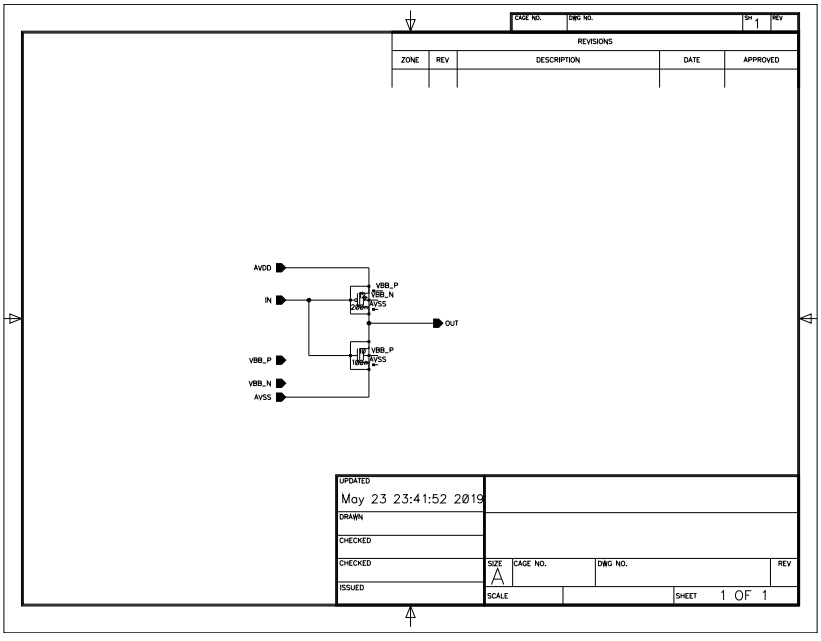


Figure 12: Inverter in comparator

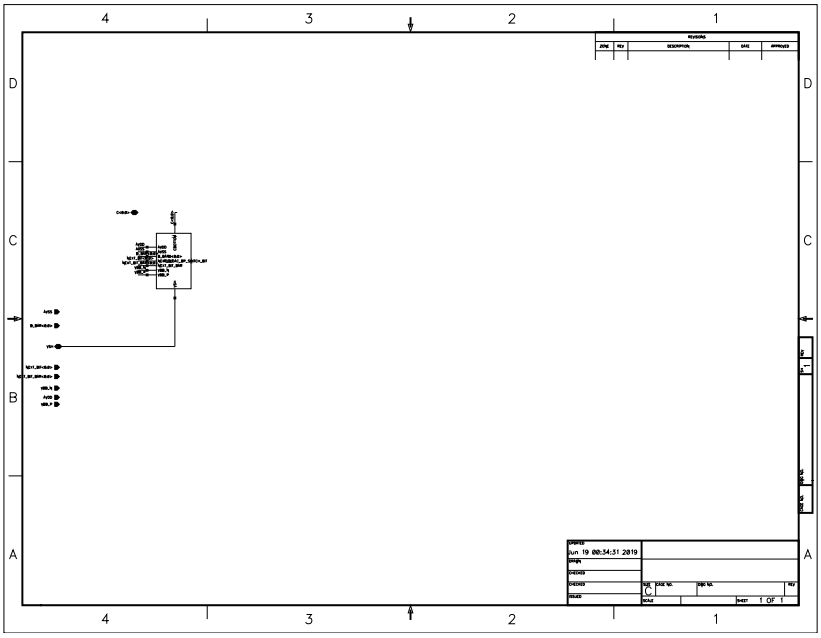


Figure 13: DAC bottom plate drivers top schematic

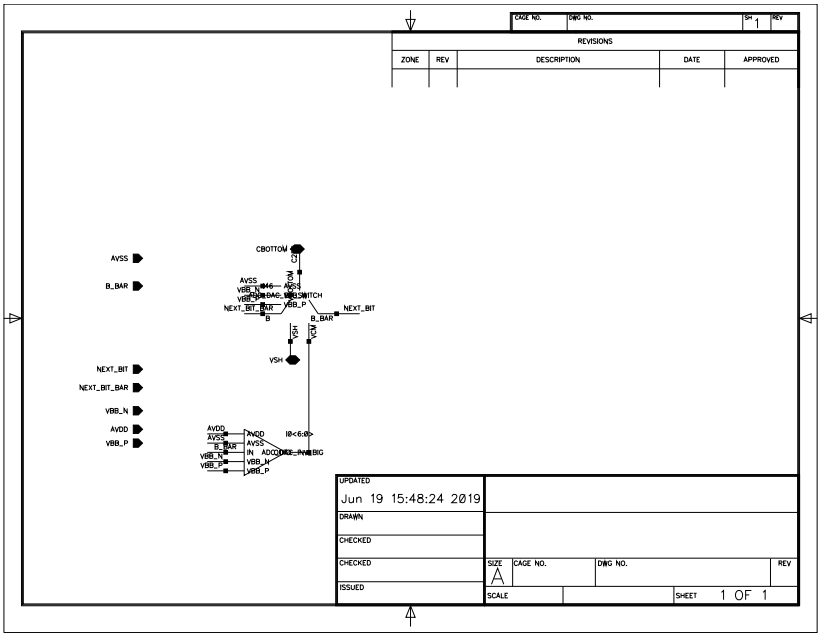


Figure 14: DAC bottom plate drivers bit schematic

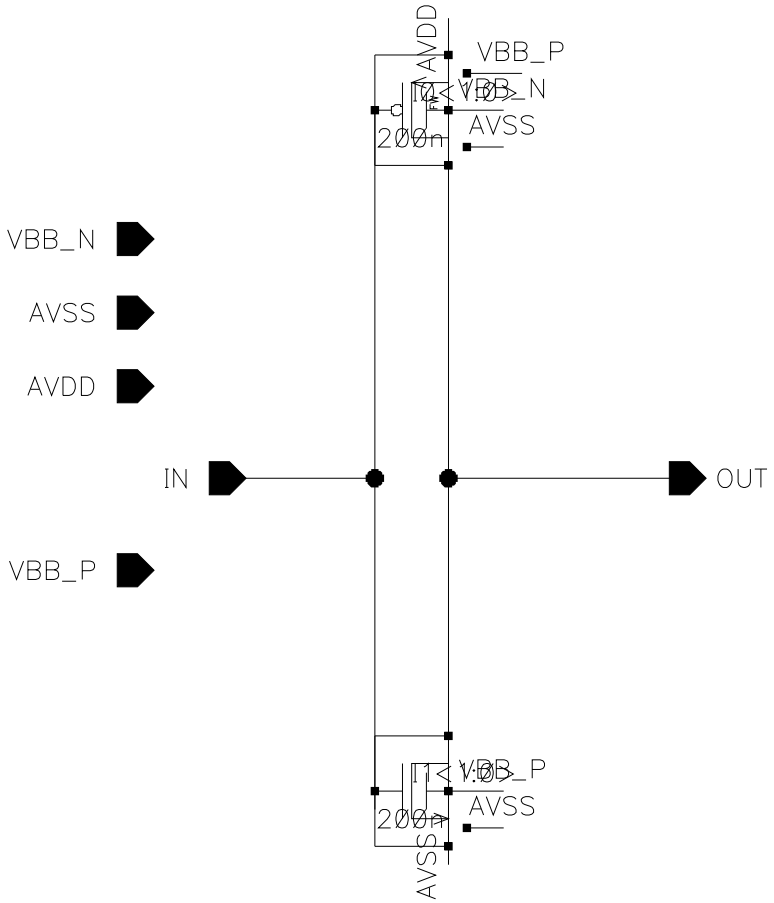


Figure 15: Inverters for driving bottom plate of DAC

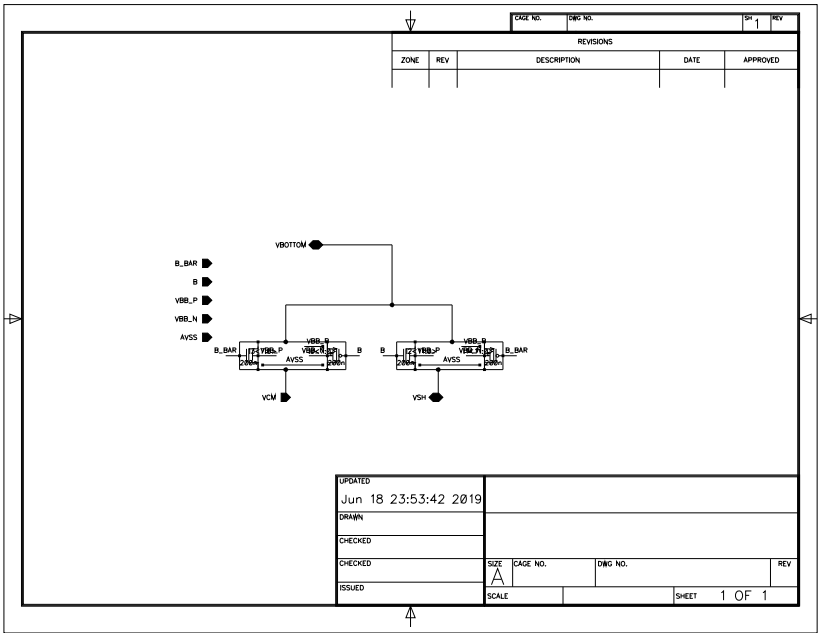


Figure 16: Switches on the bottom plate of DAC

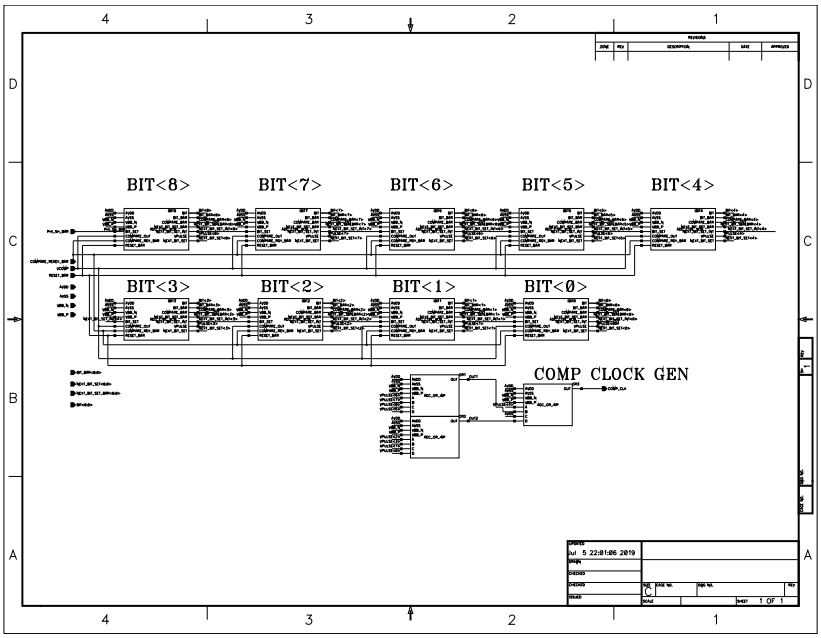


Figure 17: Bit Cycling digital circuit top

63

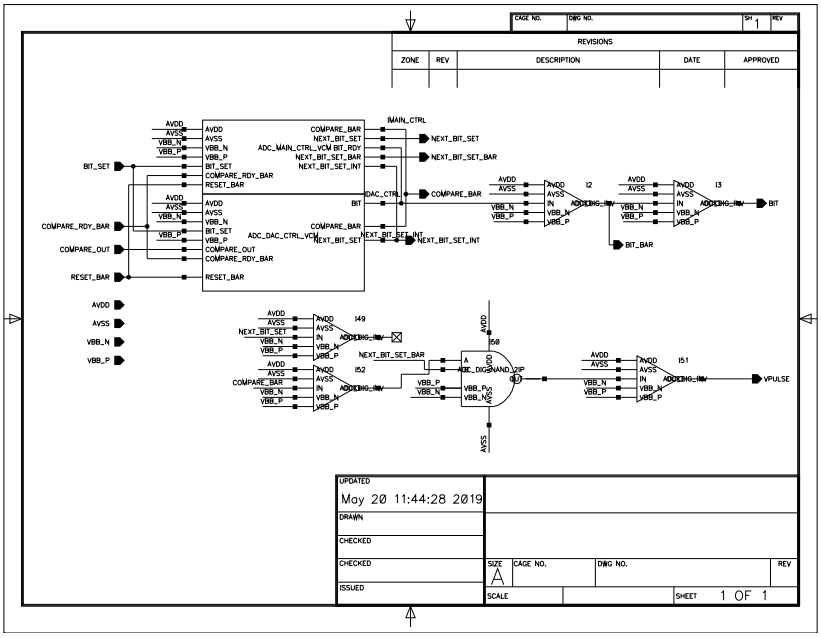


Figure 18: Bit Cycling digital circuit at bit level

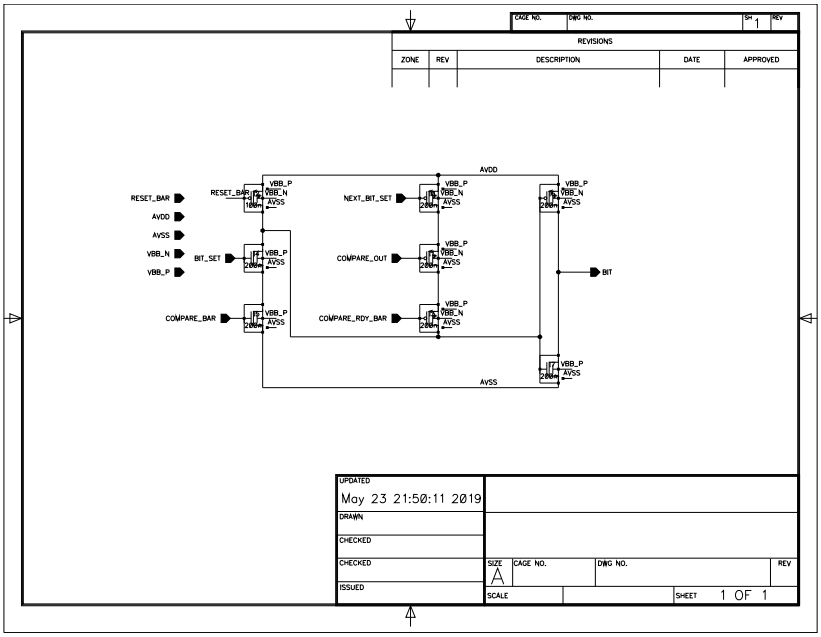


Figure 19: DAC control

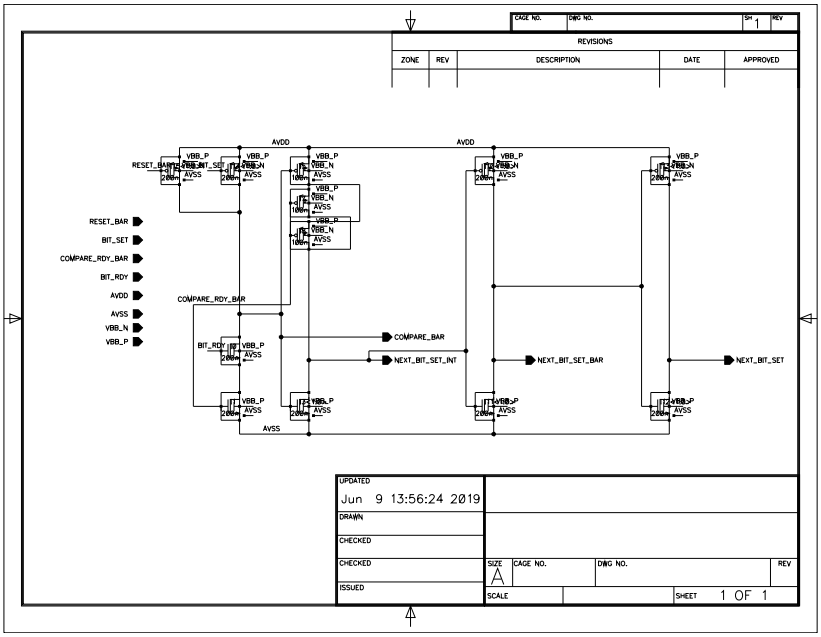


Figure 20: Main control

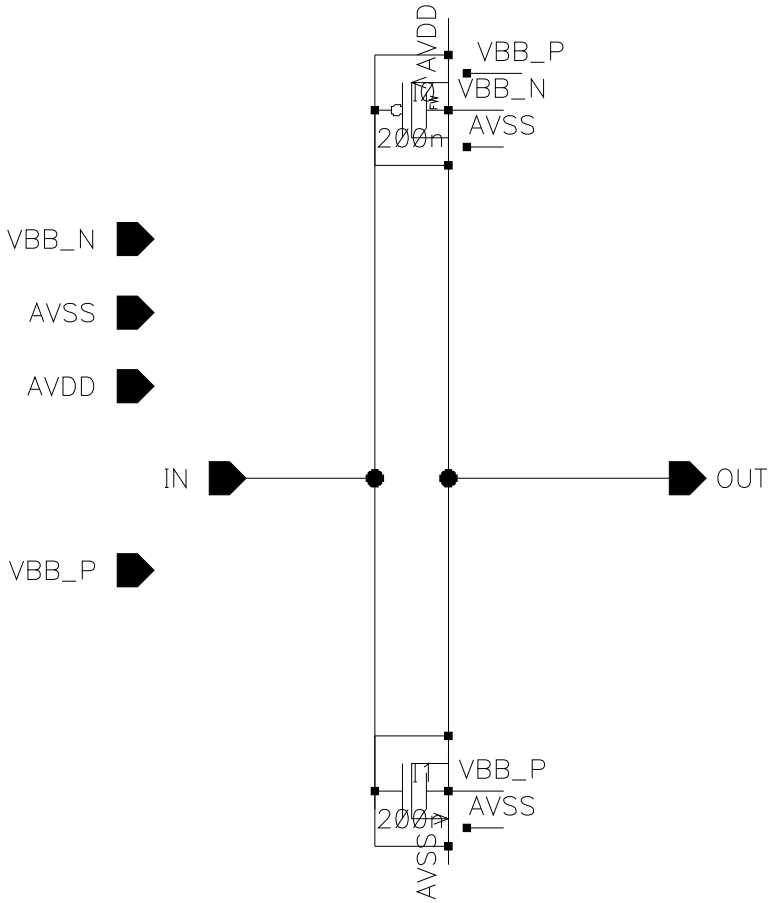


Figure 21: Inverter

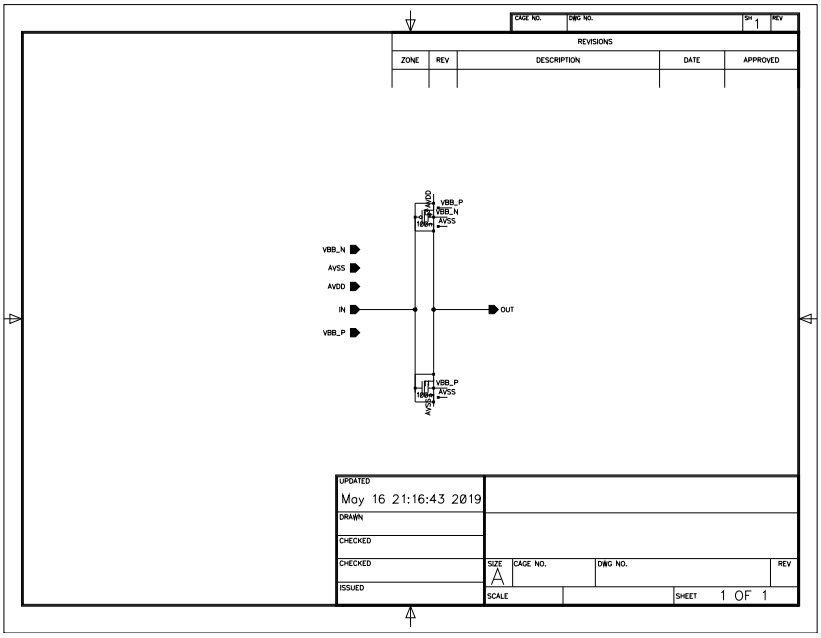


Figure 22: Inverter with 100nm width

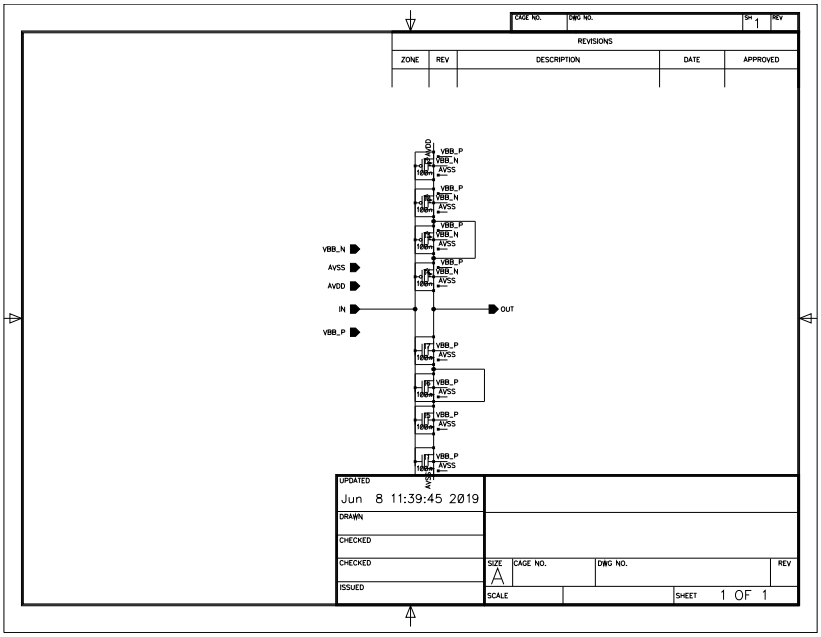


Figure 23: Inverter for creating delay

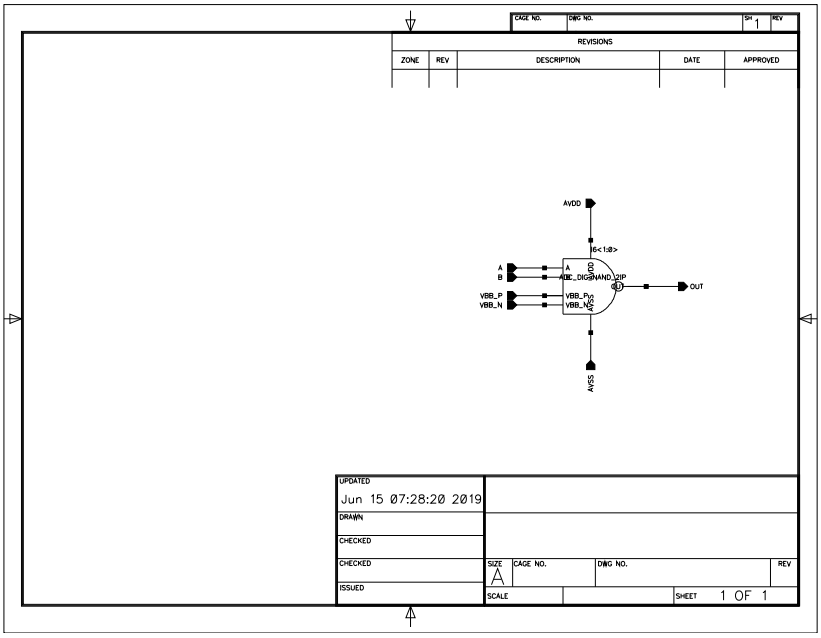


Figure 24: NAND gate in comparator

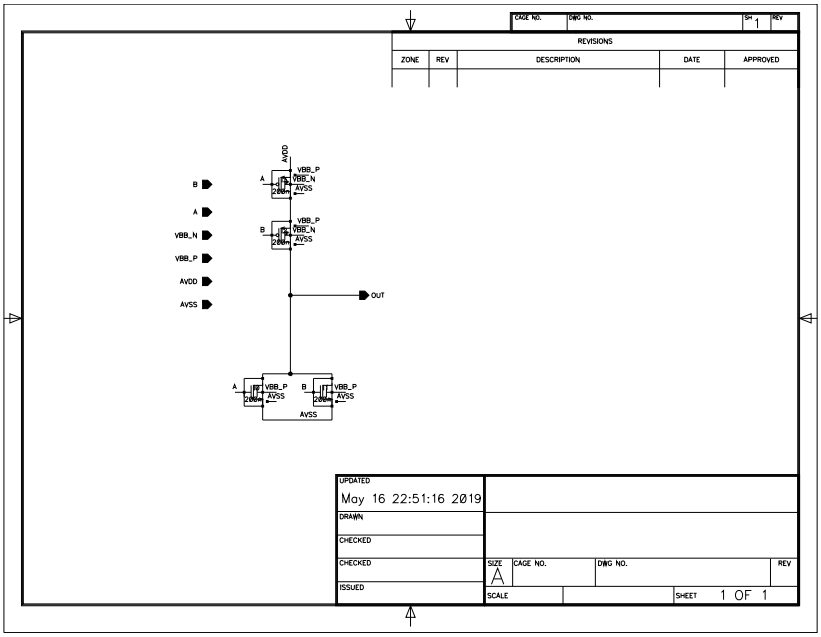


Figure 25: NOR gate

68

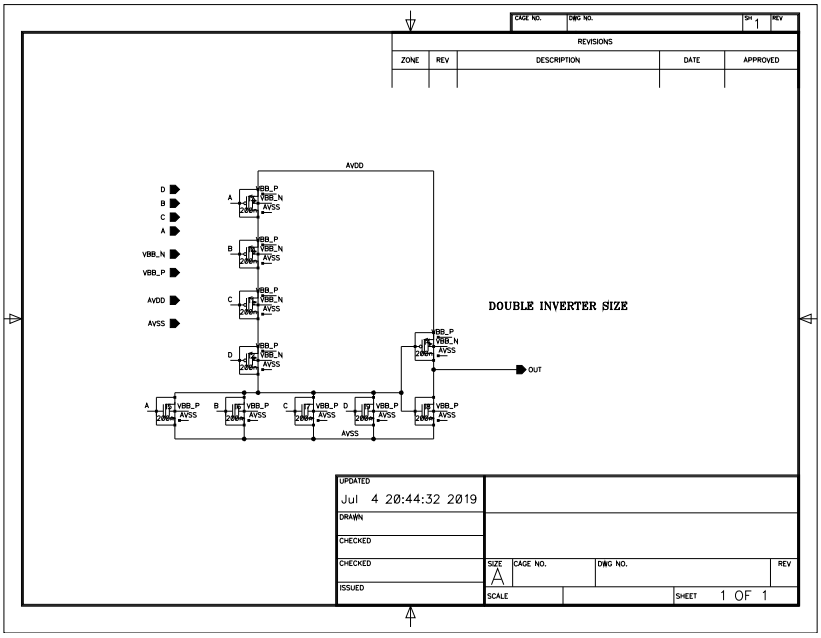


Figure 26: 4 input OR gate

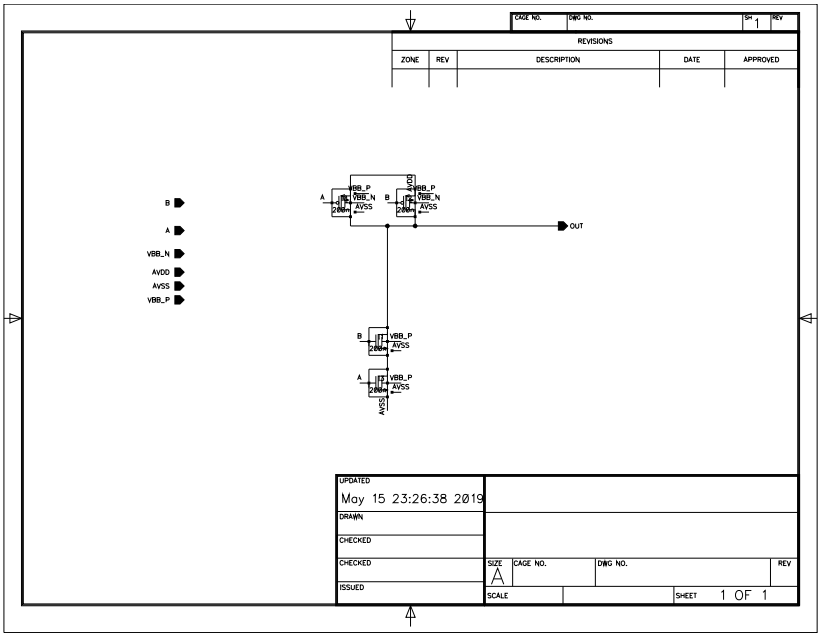


Figure 27: NAND gate in digial part

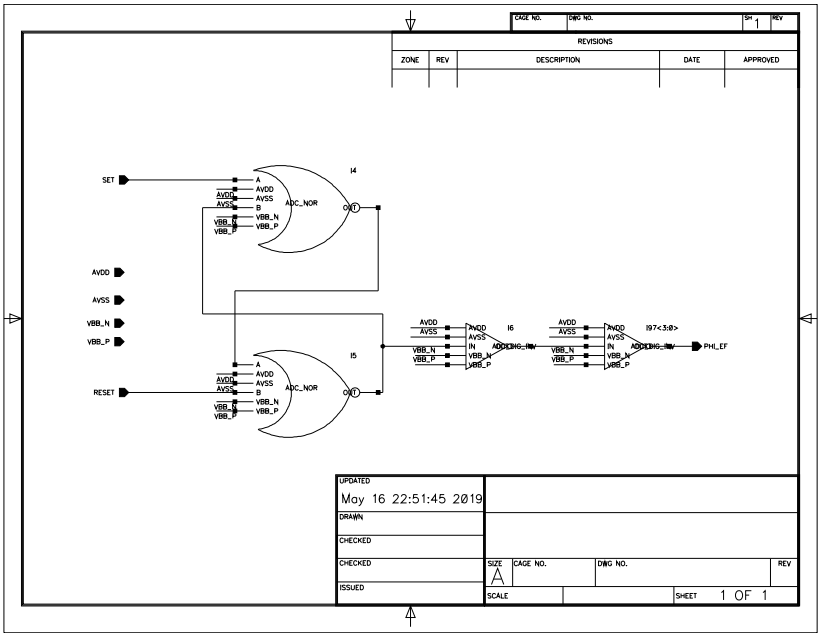


Figure 28: Latch to generate error feedback signal

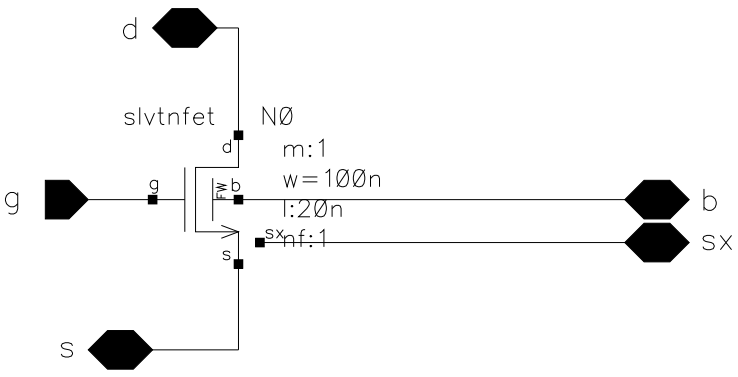


Figure 29: 100nm NMOS for digital logic

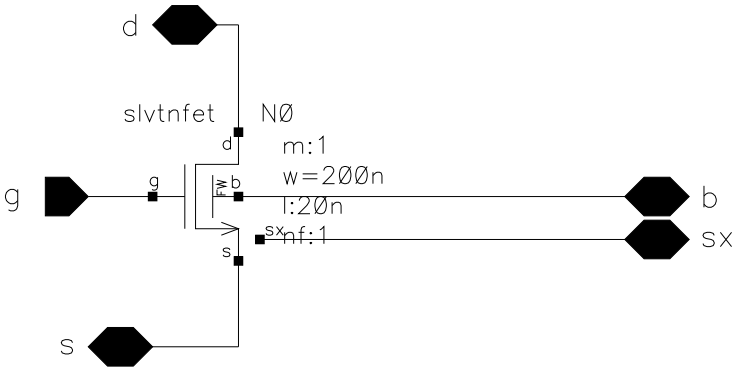


Figure 30: 200nm NMOS for digital logic

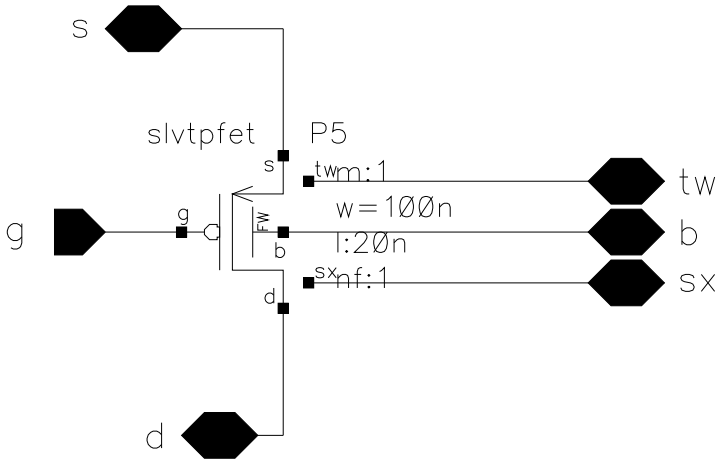


Figure 31: 100nm PMOS for digital logic

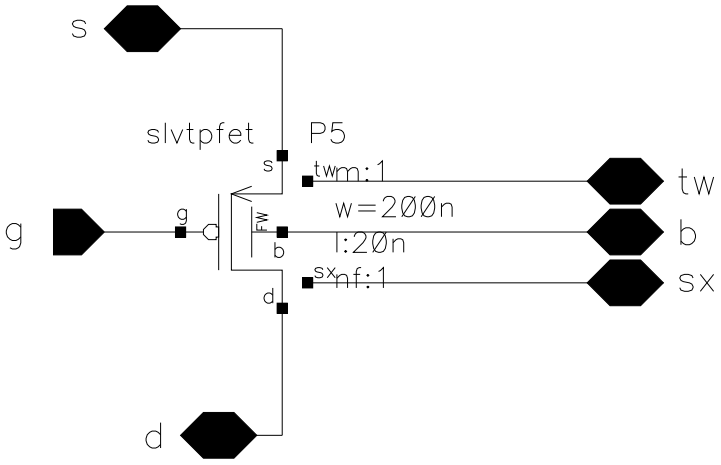


Figure 32: 200nm PMOS for digital logic

A.3 Switch Testbench

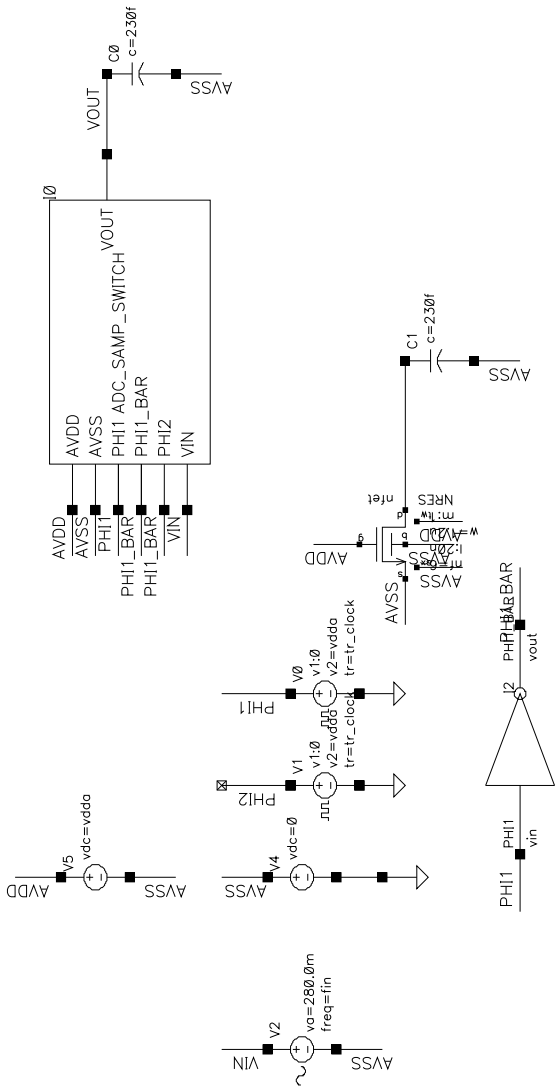


Figure 1: Testbench for sampling switch to check noise and linearity.

A.4 ADC EF Model

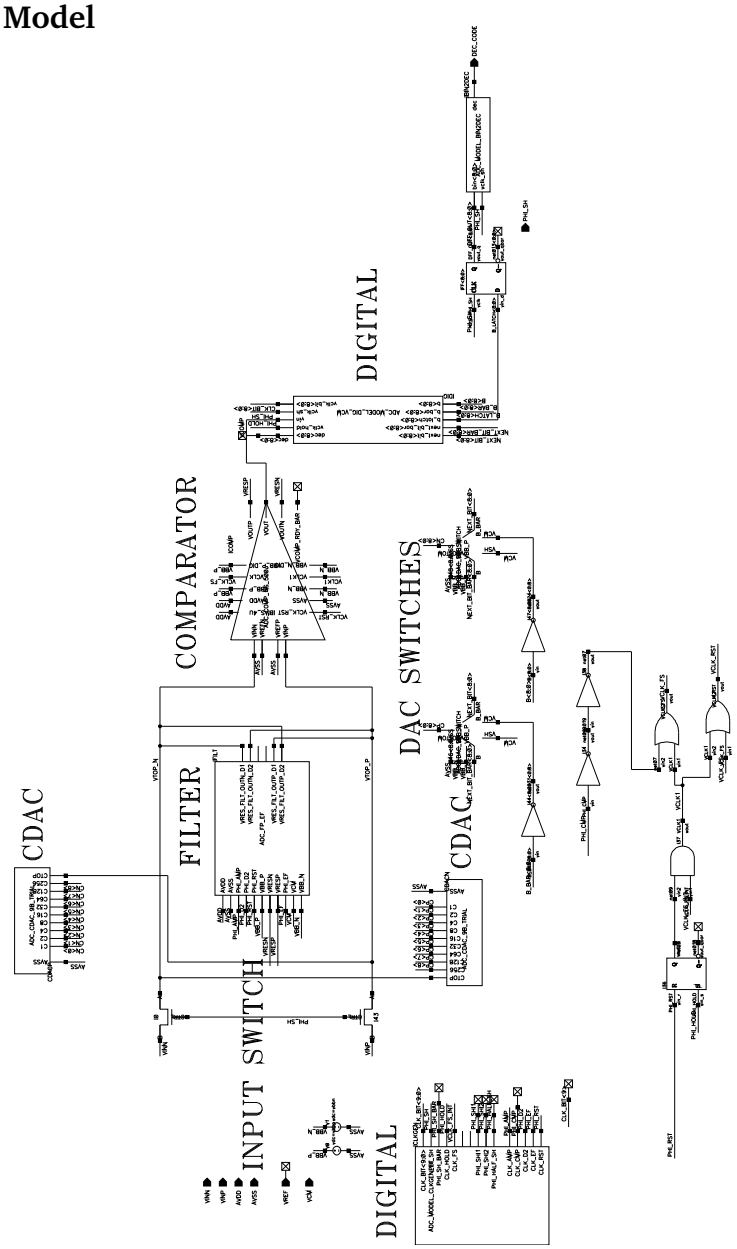


Figure 1: Top Level Schematic for Error Feedback Noise Shaping SAR ADC Model

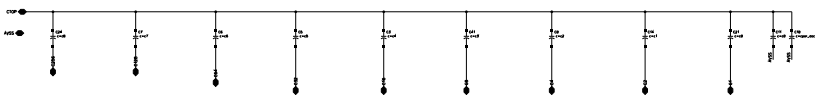


Figure 2: 9bit CDAC Model

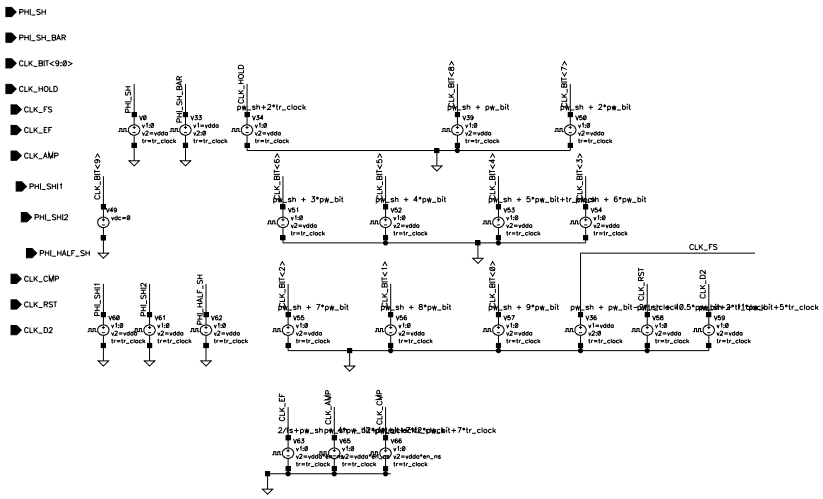


Figure 3: Clock Generator Model

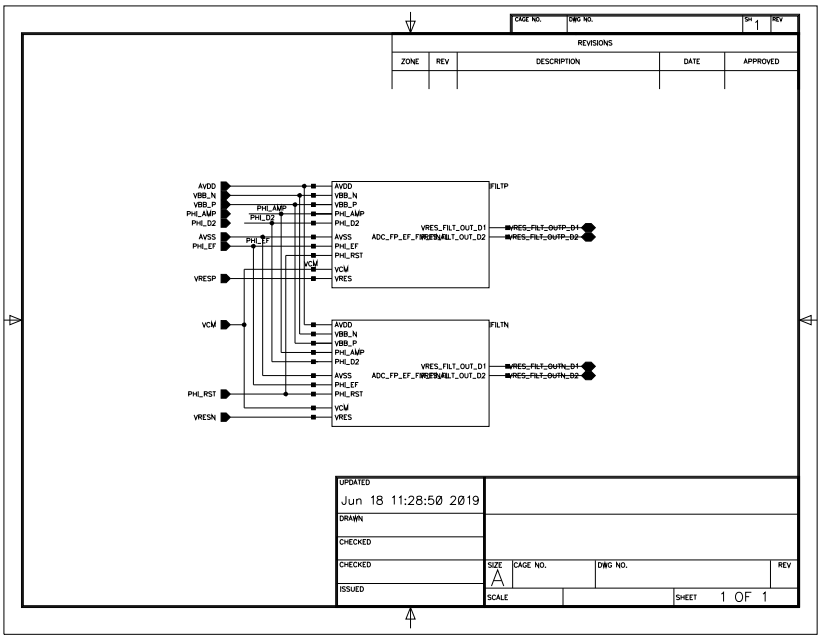


Figure 4: Filter Top Model

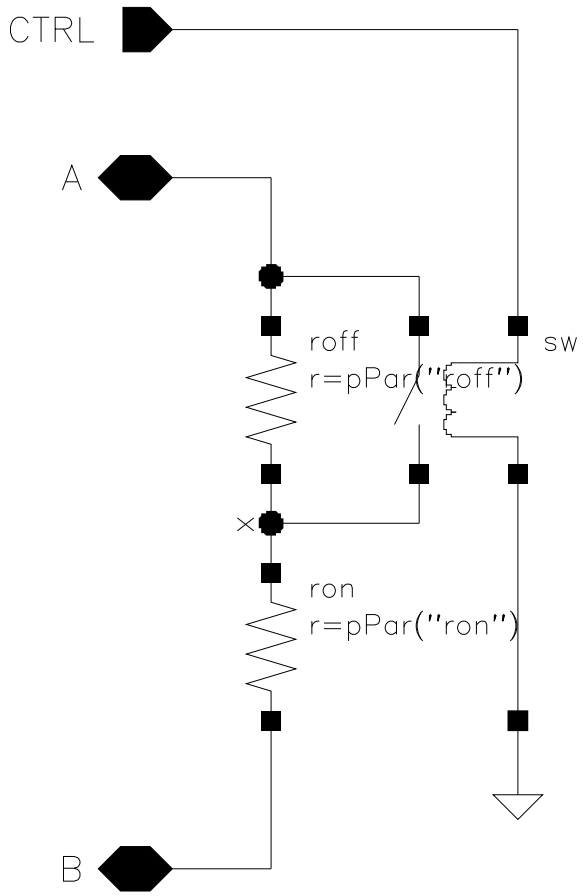


Figure 5: Switch Model

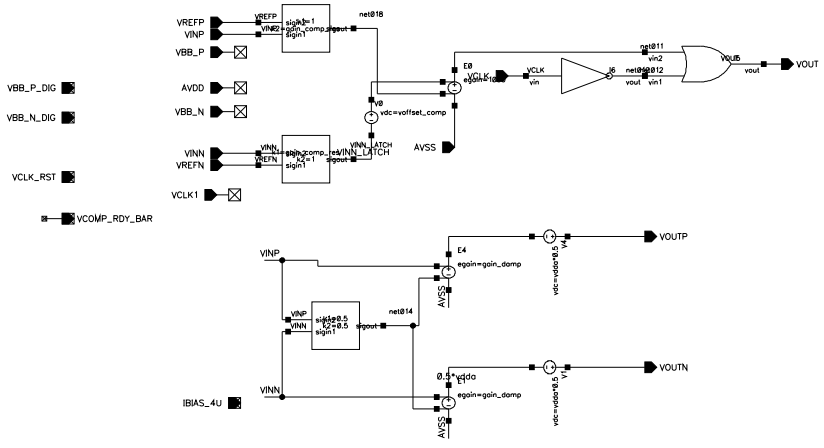


Figure 6: Comparator Model

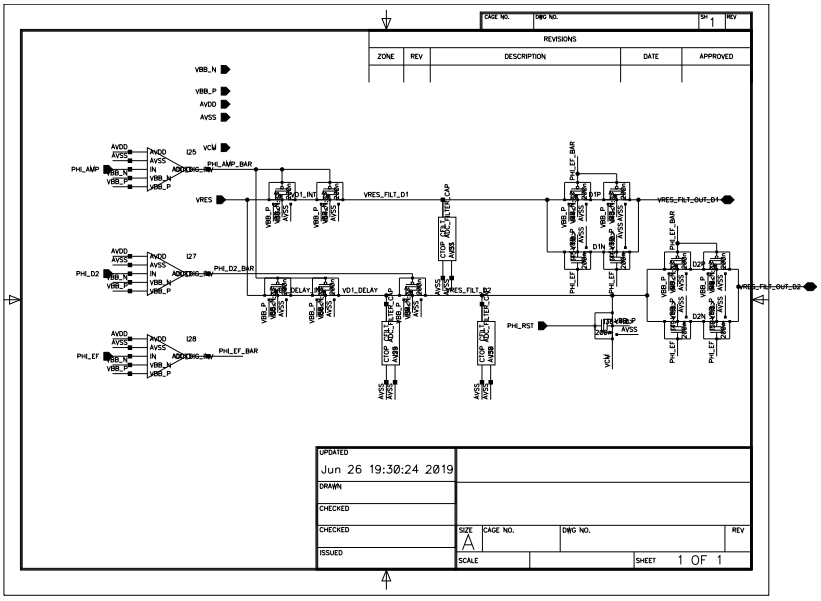


Figure 7: FIR filter Model

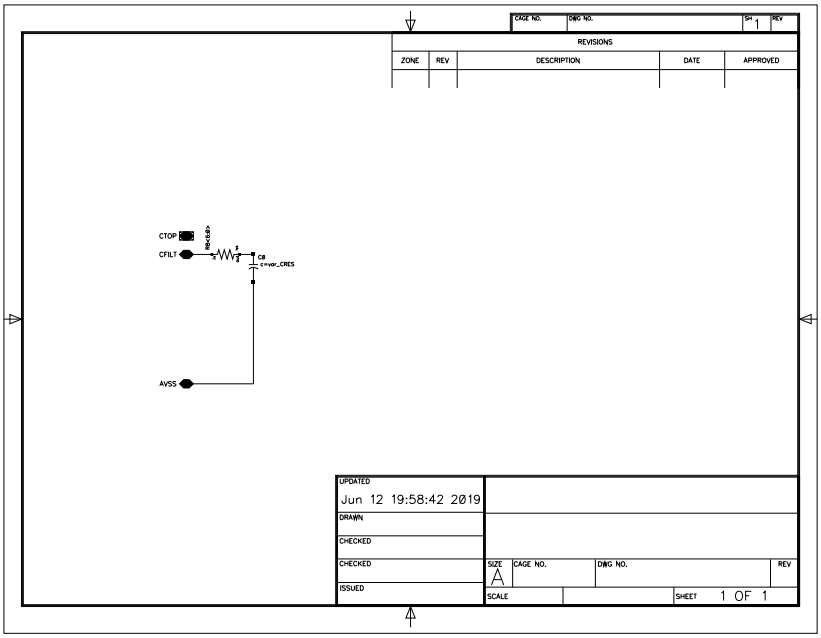


Figure 8: FIR filter cap

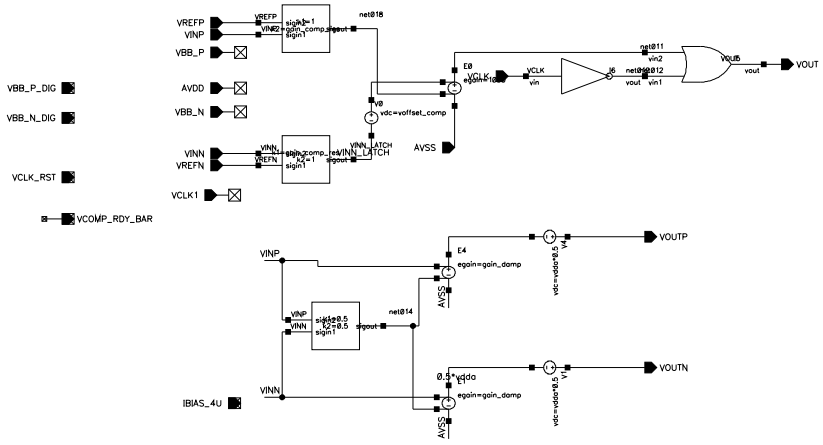


Figure 9: Comparator Model

A.5 ADC EF Testbench

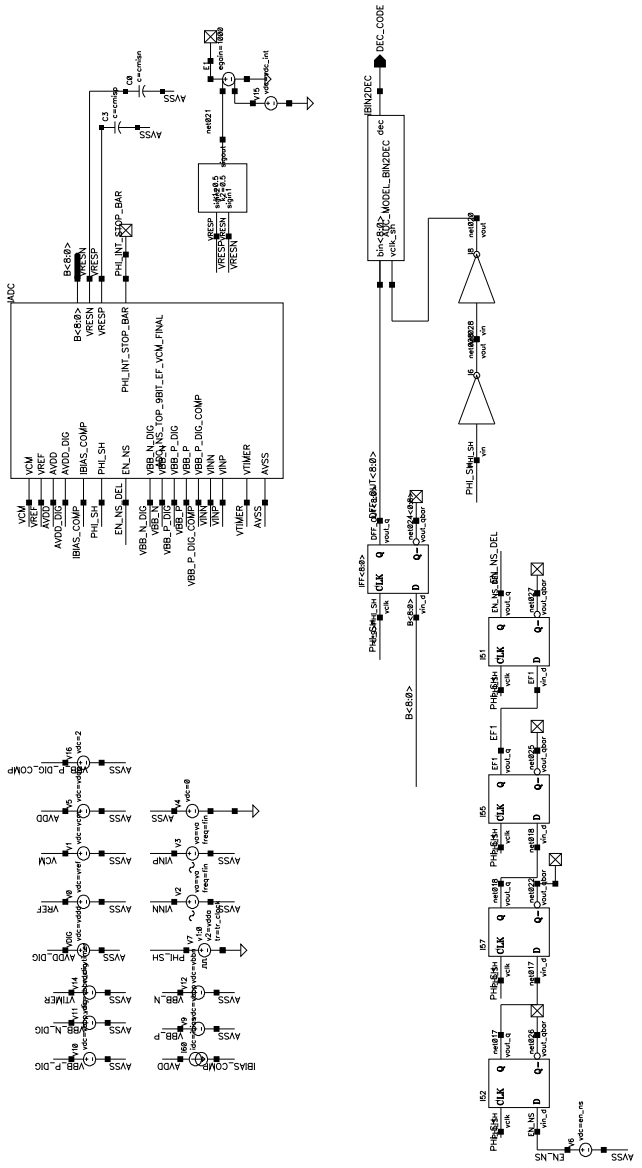


Figure 1: Top Level Testbench for Error Feedback Noise Shaping SAR ADC

A.6 Cascaded FIR IIR Schematics

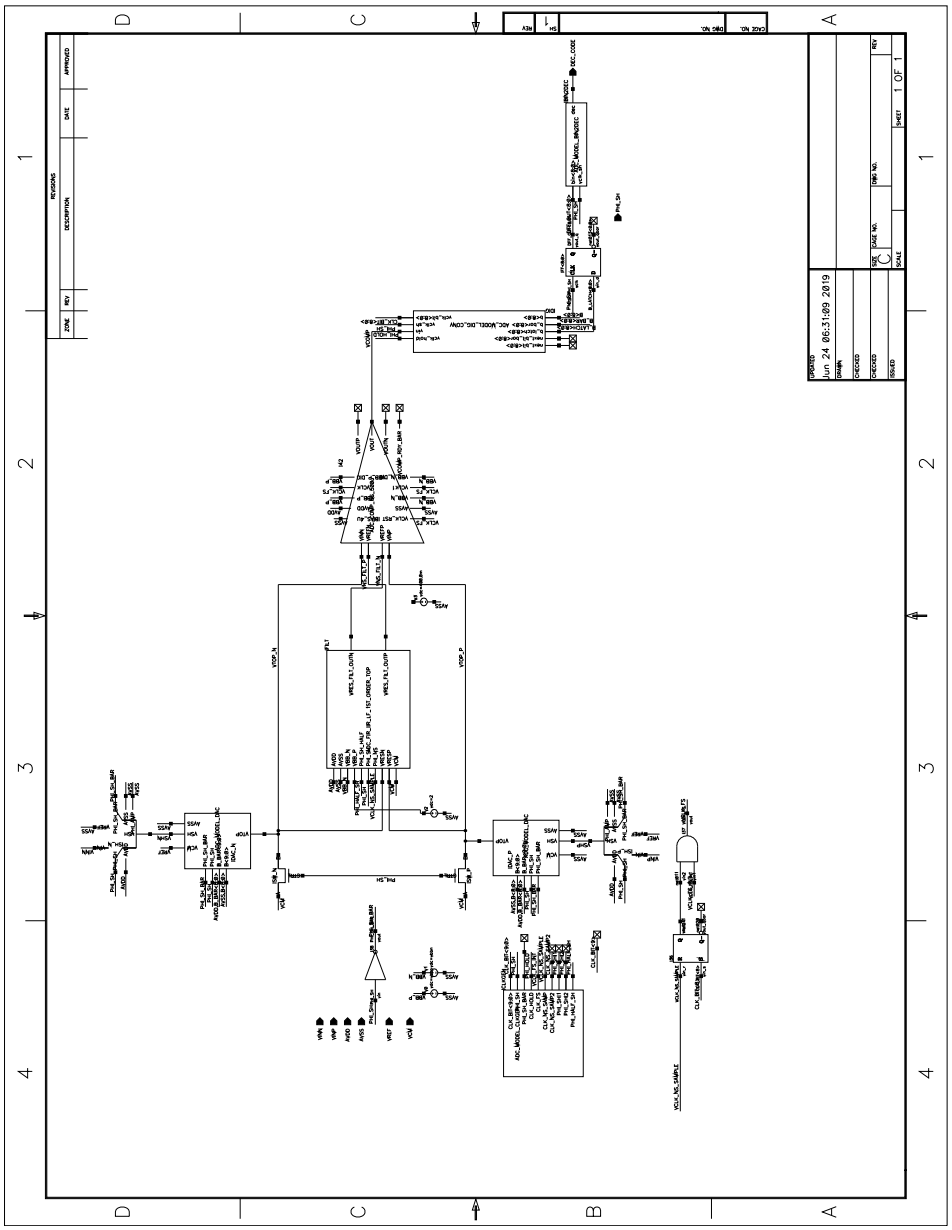


Figure 1: Top Level Schematic for Cascaded FIR IIR SAR ADC

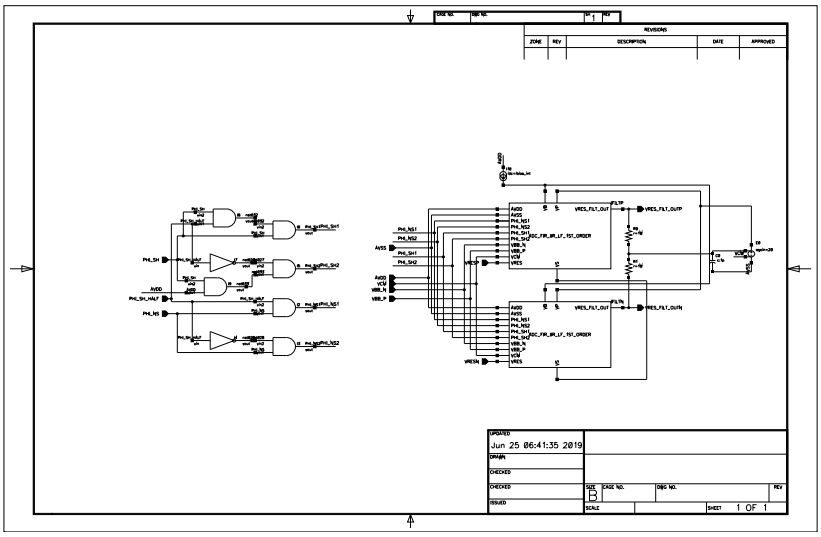


Figure 2: Filter Top

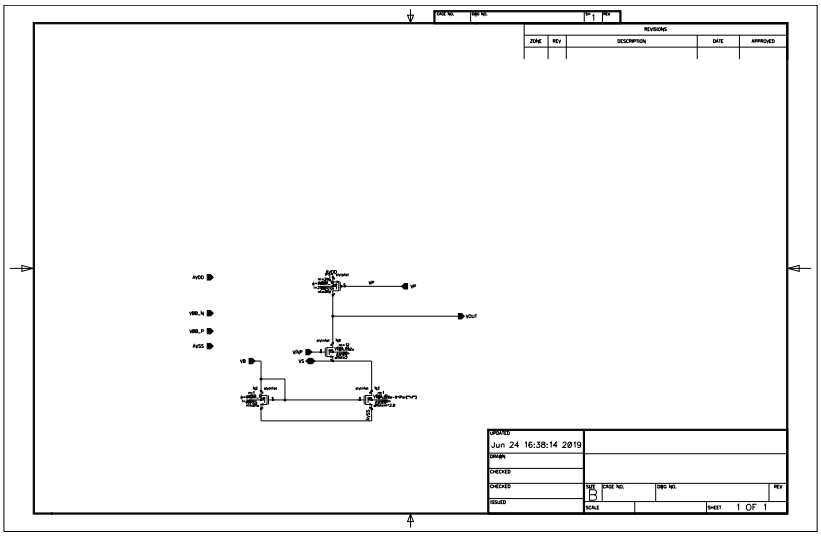


Figure 3: Integrator Half Cell

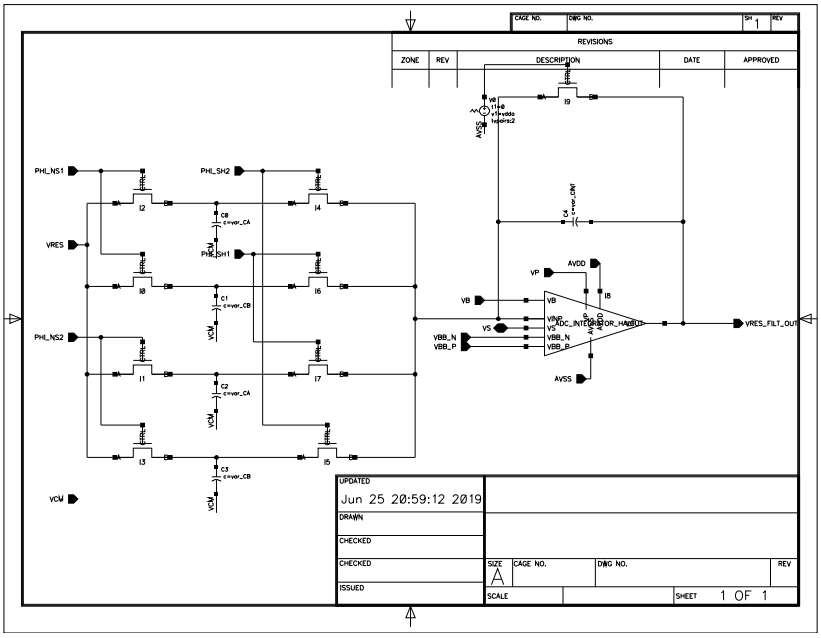


Figure 4: FIR-IIR Filter

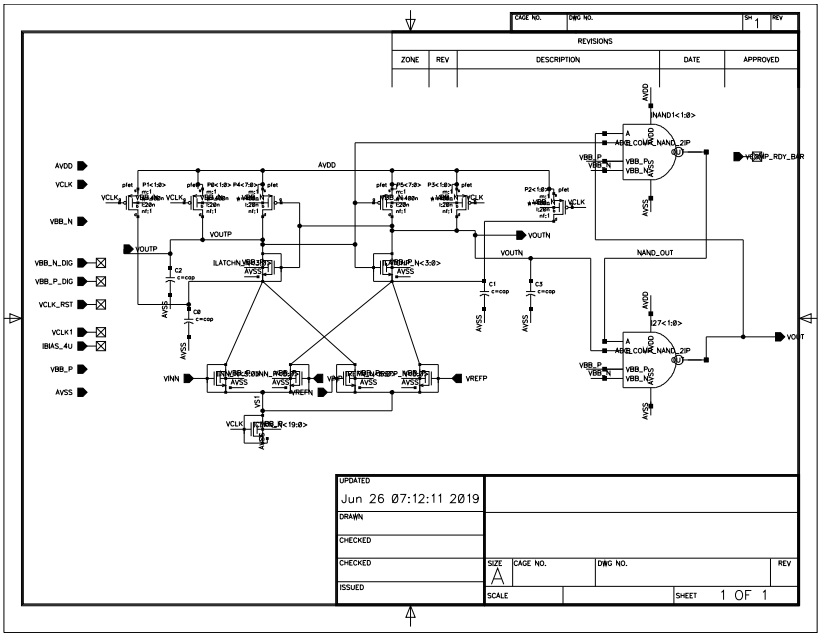


Figure 5: Comparator

A.7 Fully Passive First Order Schematics

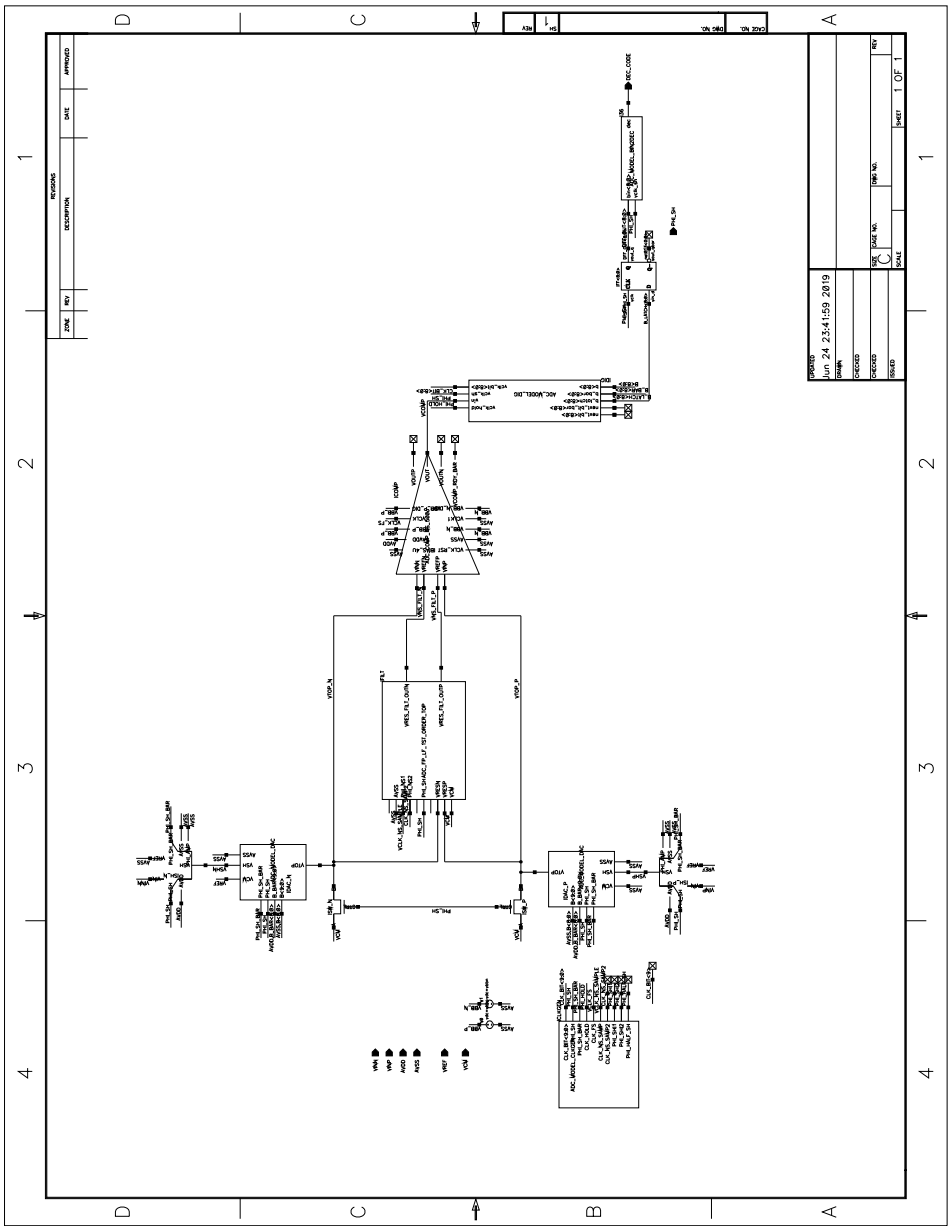


Figure 1: Top Level Schematic for FPNS 1st Order ADC

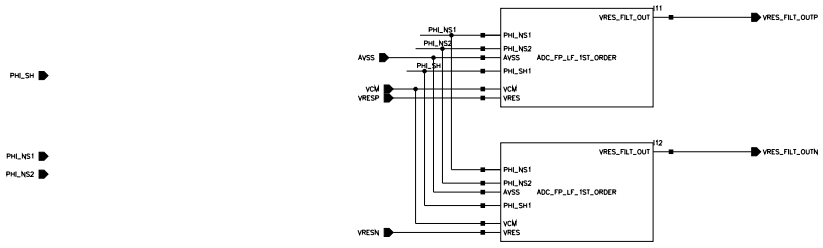


Figure 2: Filter Top

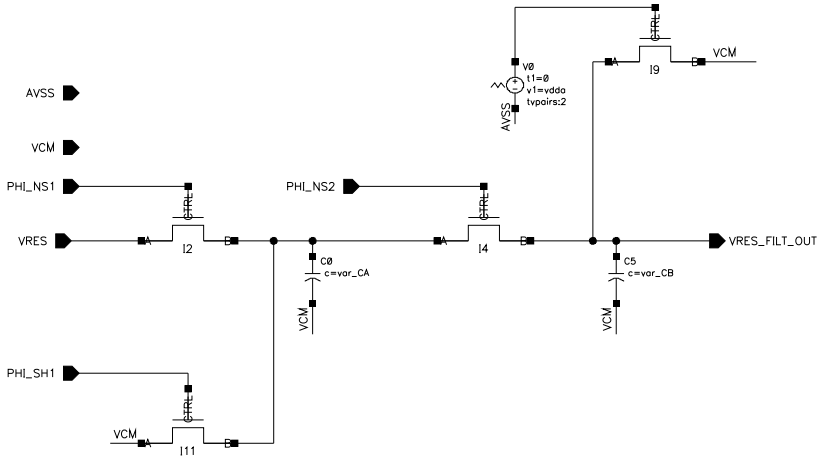


Figure 3: Filter

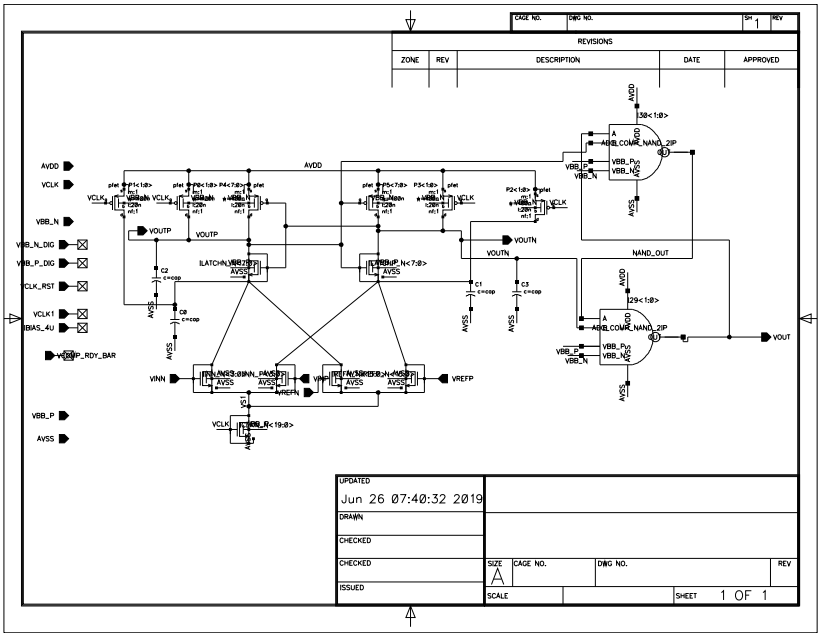


Figure 4: Comparator

A.8 Fully Passive Second Order Schematics

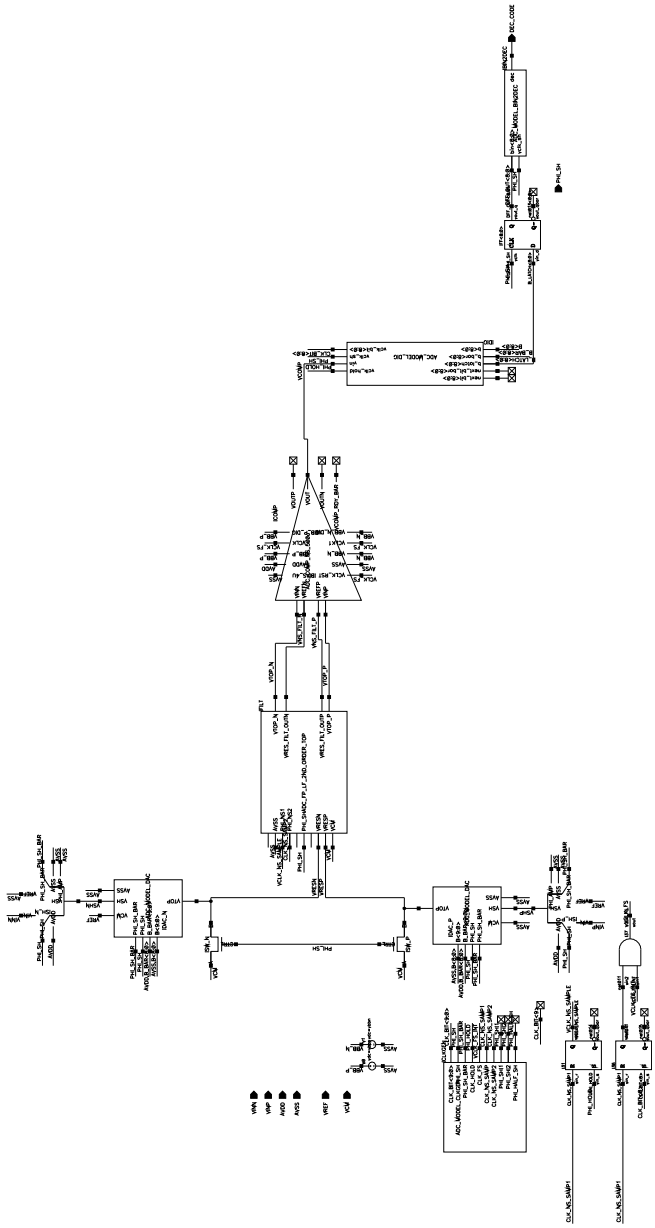


Figure 1: Top Level Schematic for FPNS 2nd Order ADC

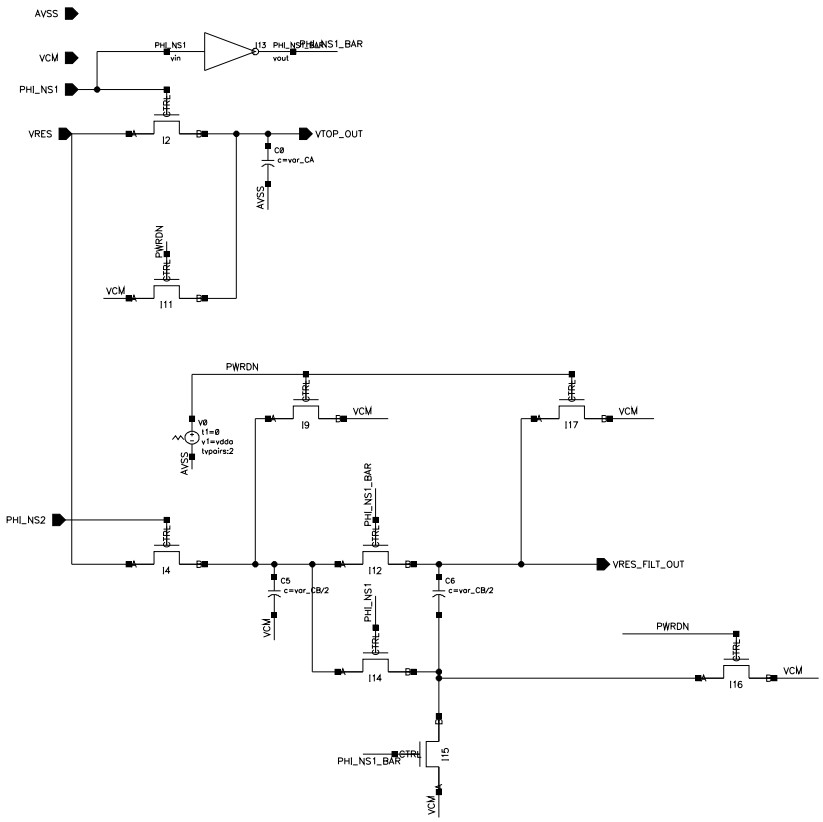


Figure 2: Filter Top

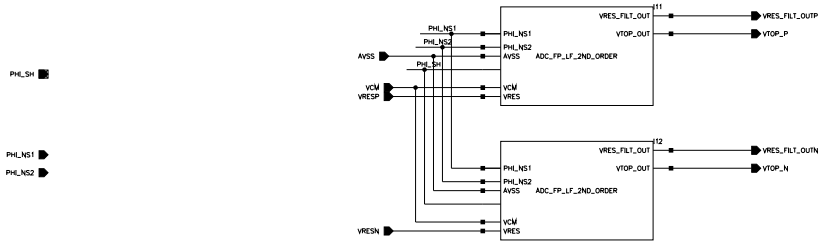


Figure 3: Filter

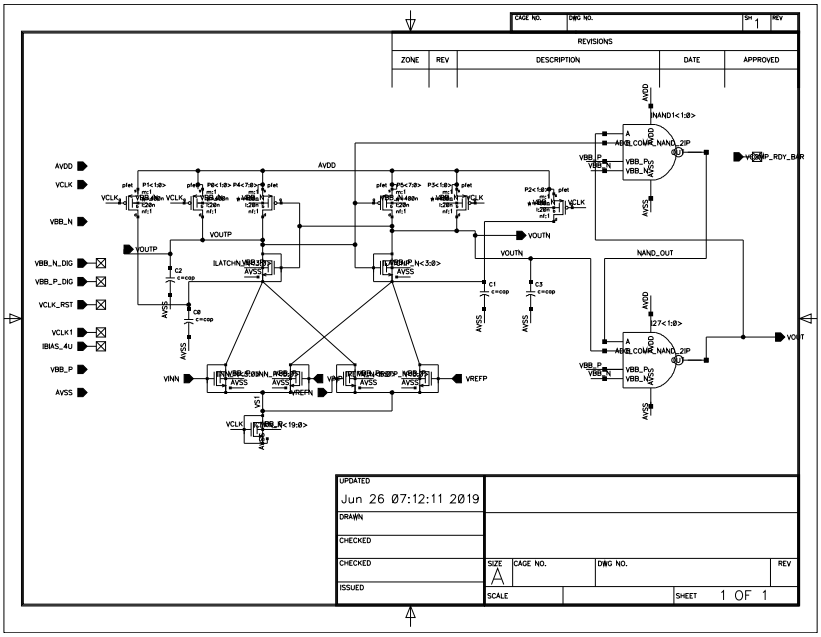


Figure 4: Comparator

A.9 Loop Filter VerilogA

```
// VerilogA for ADC_GF22N, ADC_MODEL_NS_FILTER, veriloga

`include "constants.vams"
`include "disciplines.vams"

module ADC_MODEL_NS_FILTER (vin,vclk_bit,phi_hold, phi_sh,vout);
input vin,vclk_bit,phi_sh,phi_hold;
electrical vin,vclk_bit,phi_sh,phi_hold;

output vout;
electrical vout;

real vin_del1=0;
real vin_del2=0;
parameter real Kint=0.6;
parameter real Ka1 = 3;
parameter real Ka2 = 1;
parameter real vlogic_high = 0.8;
parameter real vlogic_low  = 0;
parameter real vtrans_clk     = 0.4;
parameter tdel=100e-12;
parameter trise=100e-12;
parameter tfall=100e-12;
parameter ttol=1e-12;
real vout_int_fir=0;
real vout_int=0;
analog begin

        @( initial_step ) begin
                vin_del1 = 0;
                vin_del2 = 0;
                vout_int = 0;
                vout_int_fir=0;
        end

        @(cross(V(vclk_bit) - vtrans_clk, 1,ttol , vclk_bit.potential.abstol)) begin
                vin_del2=vin_del1;
                vin_del1=V(vin);
        end

        @(cross(V(phi_sh) - vtrans_clk, 1,ttol , vclk_bit.potential.abstol)) begin
                vout_int_fir = Ka1*vin_del1 + Ka2*vin_del2;
        end

        @(cross(V(phi_hold) - vtrans_clk, 1,ttol , vclk_bit.potential.abstol)) begin
                vout_int = (vout_int + vout_int_fir)*Kint;
        end
        V(vout) <+vout_int;
end

endmodule
```

A.10 DAC Layout

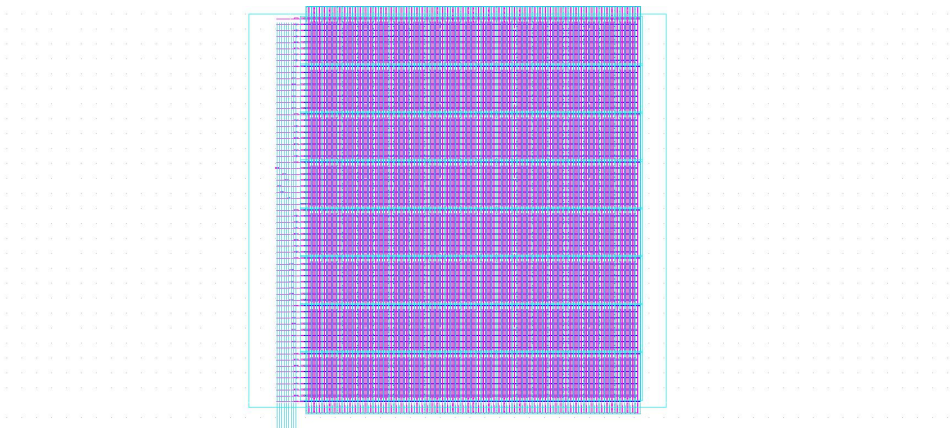


Figure 49: CDAC

A.11 Digital Layout

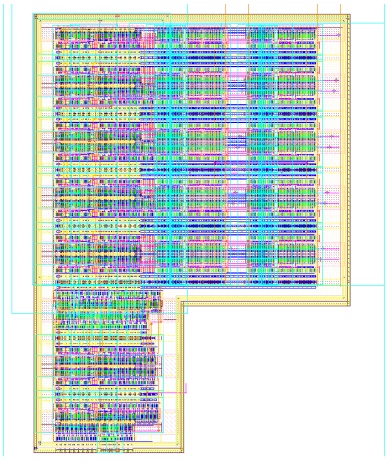


Figure 50: Digital Layout

A.12 Compararator Layout

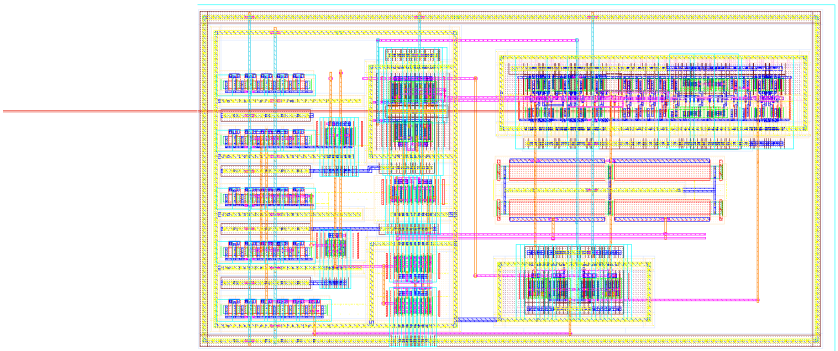


Figure 51: Comparator Layout

A.13 Filter Layout

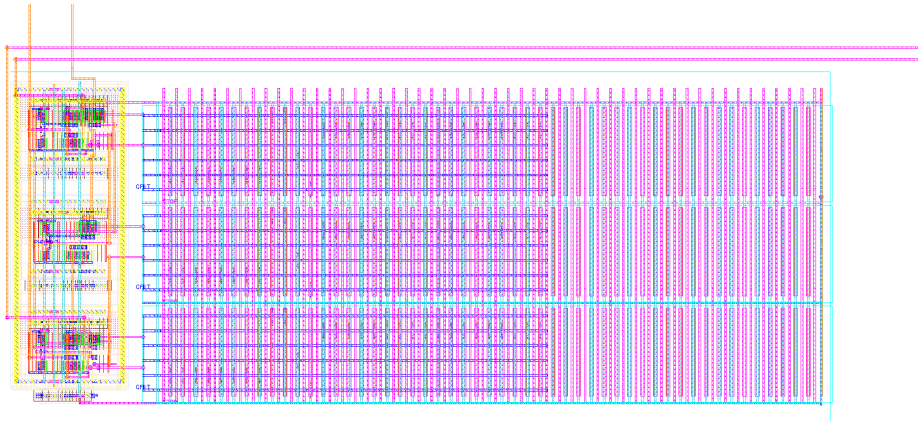


Figure 52: Filter Layout

A.14 Digital VerilogA

```
// VerilogA for ADC_GF22N, ADC_MODEL_DIG, veriloga

`include "constants.vams"
`include "disciplines.vams"

module ADC_MODEL_DIG (vin,b,vclk_sh,vclk_bit,b_latch,b_bar,vclk_hold);
localparam integer  num_bits=10;
input vin,vclk_sh,vclk_hold;
input [num_bits-1:0] vclk_bit;

electrical vin,vclk_sh,vclk_hold;
electrical [num_bits-1:0] vclk_bit;

output [num_bits-1:0] b;
output [num_bits-1:0] b_bar;
output [num_bits-1:0] b_latch;
electrical [num_bits-1:0] b;
electrical [num_bits-1:0] b_bar;
electrical [num_bits-1:0] b_latch;
integer b_int[num_bits-1:0];
integer b_bar_int[num_bits-1:0];
integer b_int_latch[num_bits-1:0];
parameter real vlogic_high = 0.8;
parameter real vlogic_low  = 0;
parameter real vtrans_clk     = 0.4;
parameter tdel=100e-12;
parameter trise=100e-12;
parameter tfall=100e-12;
parameter ttol=1e-12;
integer j=0;
genvar i;

analog begin

        @( initial_step ) begin
                for ( j = 0 ; j < num_bits ; j=j+1 ) begin
                        b_int[j]=1;
                        b_bar_int[j]=0;
                        b_int_latch[j]=1;
        end
        end

        @(cross(V(vclk_bit[0]) - vtrans_clk, -1,ttol , vclk_sh.potential.abstol)) begin
                if (V(vin)>vtrans_clk) begin
                        b_int[0] = 0;
                        b_bar_int[0]=1;
                end
                for ( j = 0 ; j < num_bits ; j=j+1 ) begin
                        b_int_latch[j]=b_int[j];
```

```
        end


        end
        @ (cross(V(vclk_sh) - vtrans_clk, 1, ttol, vclk_sh.potential.abstol)) begin
                for ( j = 0 ; j < num_bits ; j=j+1 ) begin
                        b_int[j]=1;
                        b_bar_int[j]=0;
        end
        end

        @ (cross(V(vclk_hold) - vtrans_clk, 1, ttol, vclk_sh.potential.abstol)) begin
                for ( j = 0 ; j < num_bits-1 ; j=j+1 ) begin
                        b_int[j]=0;
                        b_bar_int[j]=1;
        end
        end

        @ (cross(V(vclk_hold) - vtrans_clk, -1, ttol, vclk_sh.potential.abstol)) begin
                        b_int[num_bits-1]=1;
                        b_bar_int[num_bits-1]=0;
        end

        @ (cross(V(vclk_sh) - vtrans_clk, -1, ttol, vclk_sh.potential.abstol)) begin
                for ( j = 0 ; j < num_bits ; j=j+1 ) begin
                        b_int[j]=0;
                        b_bar_int[j]=1;
        end
        end

        for ( i = num_bits-1 ; i > 0 ; i=i-1 ) begin
                @ (cross(V(vclk_bit[i]) - vtrans_clk, -1, ttol, vclk_sh.potential.abstol)) begin
                        if (V(vin)>vtrans_clk) begin
                                b_int[i] = 0;
                                b_bar_int[i]=1;
                        end
                        b_int[i-1] = 1;
                        b_bar_int[i-1] = 0;
                end
        end

        for ( i = 0 ; i < num_bits ; i=i+1 ) begin
         V(b[i]) <+ transition( b_int[i]*vlogic_high, tdel, trise, tfall );
         V(b_bar[i]) <+ transition( b_bar_int[i]*vlogic_high, tdel, trise, tfall );
                 V(b_latch[i]) <+ transition( b_int_latch[i]*vlogic_high, tdel, trise, tfall );
        end
end

endmodule
```

A.15 Comparator Testbench

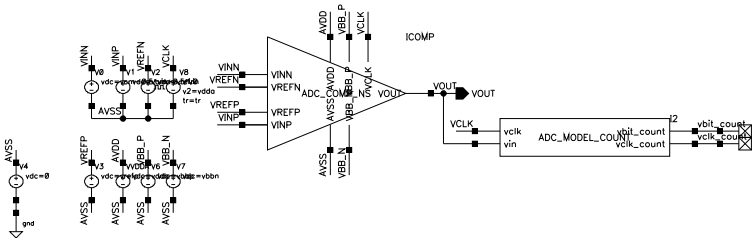


Figure 1: Testbench

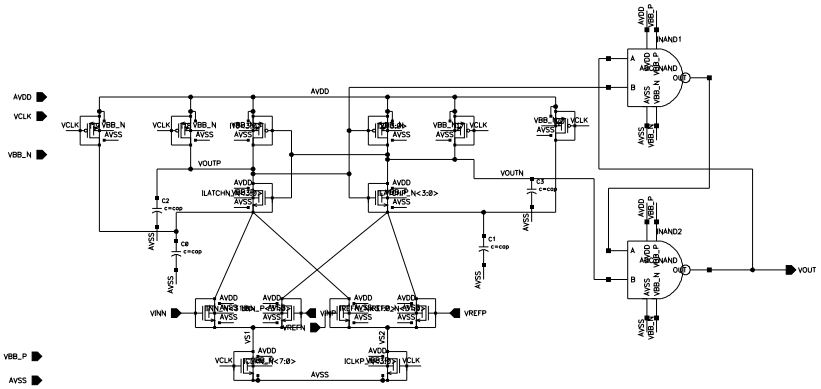


Figure 2: Comparator

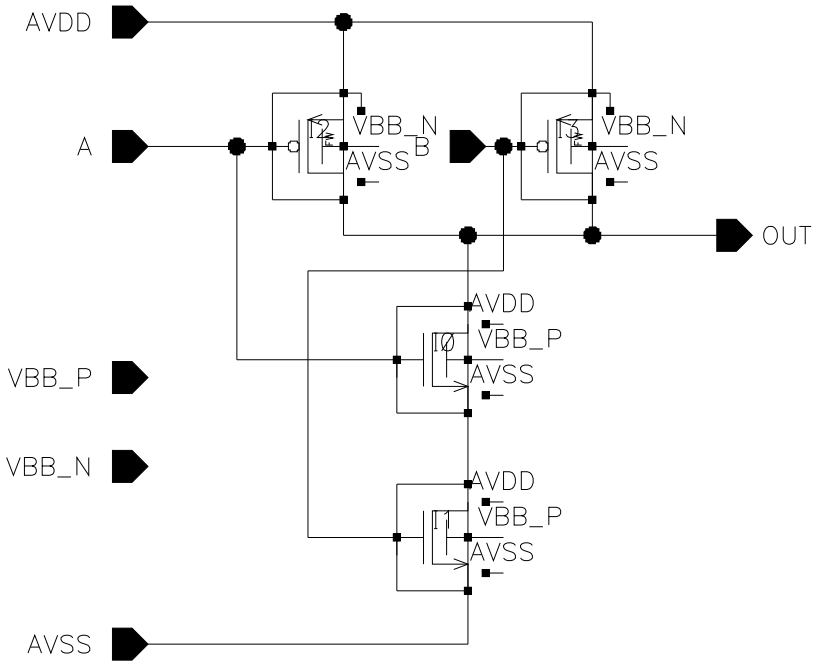


Figure 3: NAND gate

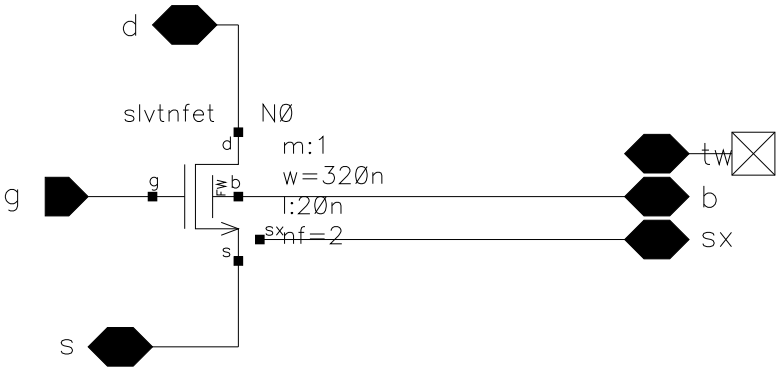


Figure 4: NMOS cell used in comparator circuit

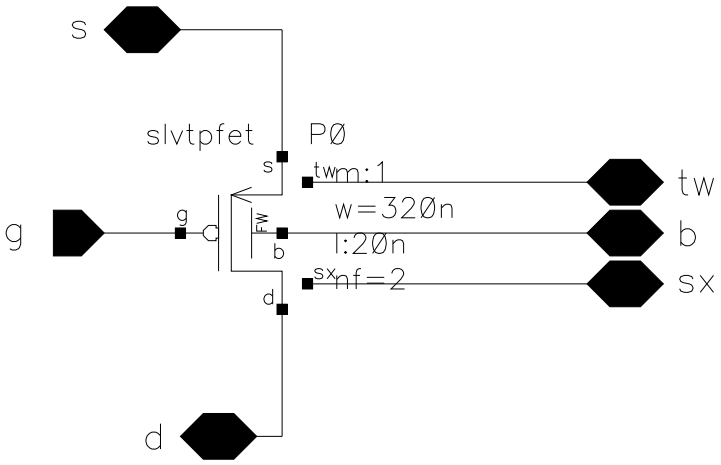


Figure 5: PMOS cell used in comparator circuit

A.16 Integrator Testbench

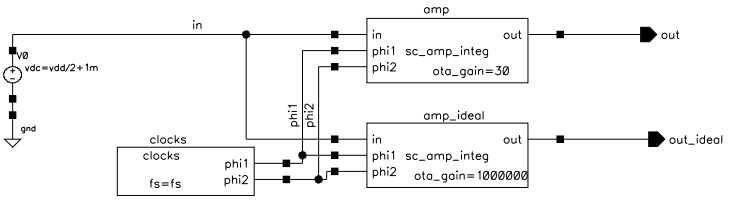


Figure 1: Testbench

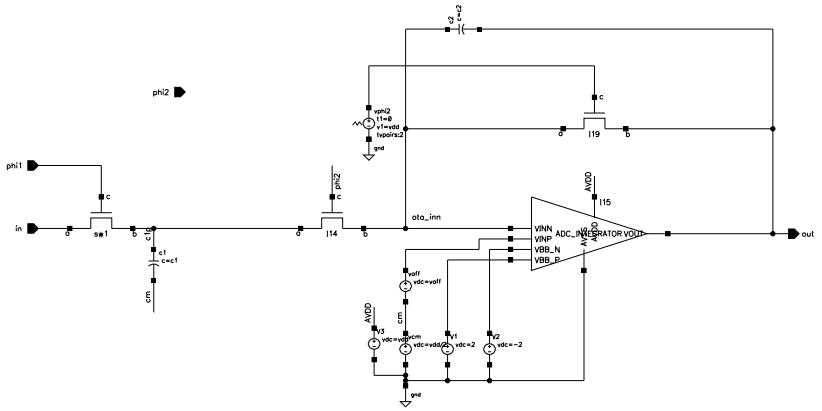


Figure 2: Integrator Top Level

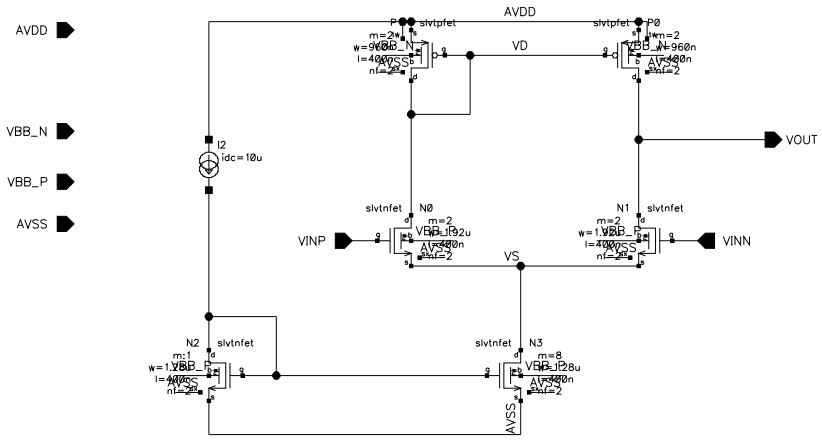
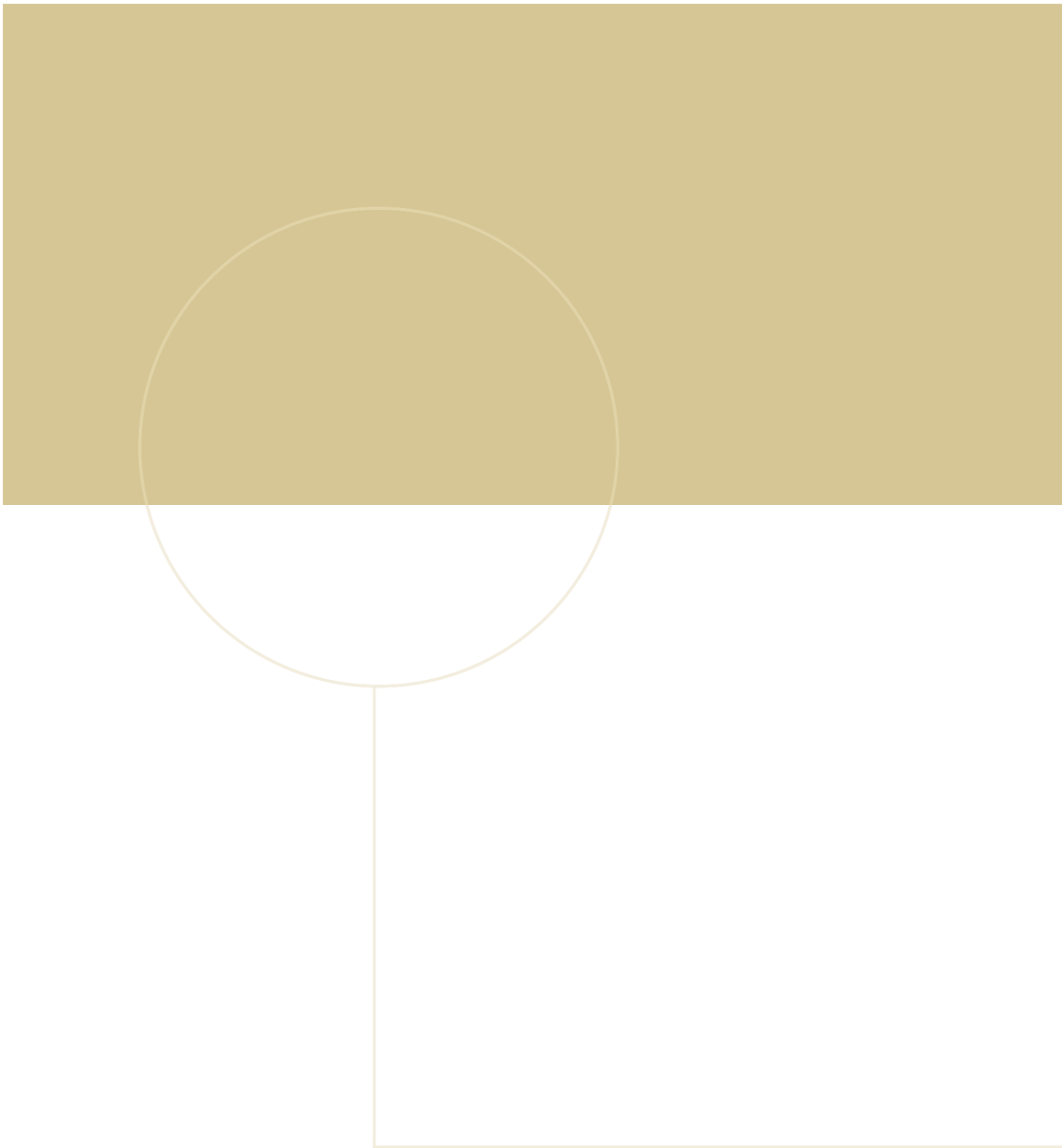


Figure 3: Integrator Amplifier



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