Selective output impedance based control for grid-connected inverters

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Keywords

≪Converter control≫, ≪Harmonics≫, ≪Power quality≫, ≪Voltage Source Inverters (VSI)≫.

Abstract

This paper proposes a power control loop strategy for Voltage-Source Inverters (VSIs), based on the use of abc frame PI controllers. Its physical behaviour and mathematical model are presented in detail and the inverter output impedance is derived to analyze the obtained disturbance rejection performance. The results show that the proposed scheme is capable of effectively rejecting disturbances originating from the grid voltage, achieving current THD as low as 2.45% even with a voltage THD of 28.3%.

Introduction

Renewable power sources are usually interfaced with the electrical grid through power converters that must comply with standards, such as the IEEE Std 1547-2018 [1], that establish requirements for the connection of the distributed generators (DGs) to the grid, also in terms of power quality. The current THD is an important index which should be kept below specific limits and is affected by both the converter control and preexisting distortions in the voltage of the Point of Common Coupling (PCC). To ensure a suitable operation, complying with the standards requirements, a grid-connected converter must be equipped with a control system that presents an adequate performance even under non-ideal conditions and is capable of rejecting disturbances coming from the grid voltage.

A number of works discuss and evaluate strategies for current control in grid-connected VSIs. The most common controllers are the Proportional-Integral (PI), implemented in natural or synchronous reference frames, the Proportional-Resonant (PR) or Proportional-Integral-Resonant (PI-R) [2, 3], and the Dead-Beat (DB) [4, 5]. For the natural frame PI, the biggest constraint is its inherent bandwidth limitation, which causes steady-state error when tracking time-varying references. To overcome this limitation, the Park transformation is widely used, since it allows to represent the error signals as DC values in the dq synchronous frame, where PI controllers ensure zero steady-state error. Still, it does not allow the elimination of oscillations that appear in the dq signals under unbalanced grid conditions, requiring the use of two controllers to independently regulate the positive and negative sequence components [6]. Similarly, for harmonic compensation, a reference frame has to be used for each frequency. However, in case of single-phase applications, the Park transformation cannot be directly applied, so a quadrature voltage signal has to be synthesized, which is typically done by displacing the measured voltage by a

quarter fundamental period. In [7] a simplified method to calculate the dq components is proposed, improving the system dynamics, but the other aforementioned problems remain unaddressed.

PR and PI-R controllers solve the drawbacks of the natural frame PI. Their high gain at selected frequencies leads to an increase of the Dynamic Stiffness (DS) [8, 9] of the system, which is a measure of its disturbances rejection capability. Thus, these types of controllers provide good results, even in very adverse grid conditions, and can be used for selective harmonic compensation [10]. The drawback with respect to the PI is an increased complexity and implementation difficulty, especially when the control of multiple harmonic components is required.

Finally, there are several works reporting good results with the use of Dead-Beat controllers. This type of controller is relatively simple and capable of regulating harmonic components without the need for several parallel units, which is an advantage over the resonant controllers. However, its optimum performance requires a fairly good knowledge of the controlled system's parameters, posing an additional requirement with respect to the PI implementations.

This paper presents a power control method for single-phase grid-connected inverters, whose objective is to regulate the active and reactive power flow supplied by the DG, while guaranteeing the low current harmonic distortion. This method is based on a double-loop system in which the outer loop tracks the disturbance current and changes the inner loop reference signal to eliminate the circulation of harmonics.

System configuration

The system studied in this paper is composed of a single-phase VSI, supplied by a Renewable Energy Source (RES). As this paper focuses on the connection between the inverter and the grid, for simplicity, the RES and any conditioning circuits, such as DC-DC or AC-DC converters, are simplified and, thus, represented as a DC voltage source. The grid is modelled as a Thèvenin equivalent and the inverter is connected to it through an LC filter. Since DGs are connected mainly in distribution networks, whose capacitive component is normally negligible, its effects are not considered.

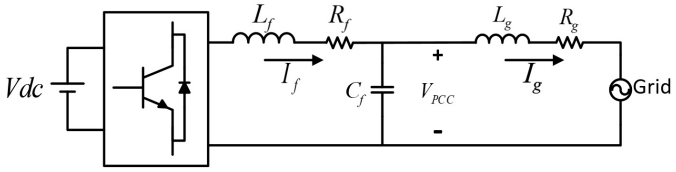

Fig. 1: Circuit of the grid-connected VSI

Current control

The inverter-side current control loop is shown in Fig. 2, where $C_i(s)$ represents the current controller, $G_d(s) = e^{-s\lambda T_s}$, where T_s is the sampling period, represents the computational delay resulting from the analog-to-digital conversion and control algorithm calculation.In real applications, λ is typically either 0.5 or 1 [12], but, because of the modulation used, λ is considered equal to 1 herein. C_{pk} is the PWM carrier peak-to-peak amplitude, $DPWM$ is the digital PWM model, $G_{conv}(s) = 2V_{DC}$ is the converter transfer function (TF) for three-level PWM, H_i is the current transducer gain and v_{pcc} is the voltage at the Point of Common Coupling (PCC). Given that the filter capacitor value is small, the output impedance, $Z_f = sL_f + R_f$, can be approximated by a RL system, except near the resonance between C_f and L_g.

The model of the digital PWM is thoroughly discussed in [11] and, thus, its derivation is not presented herein. In this paper, it is assumed the use of a uniformly sampled PWM with double update and triangular carrier whose amplitude goes from 0 to 1 ($C_{pk} = 1$). Its TF and simplification by means of the Padé approximation are shown in (1). From this analysis, it is possible to see that there are two different sources of delay in the system, the PWM and the computational time. To simplify the system representation, it is possible to consider a single delay, whose value is equal to their sum, by increasing the PWM

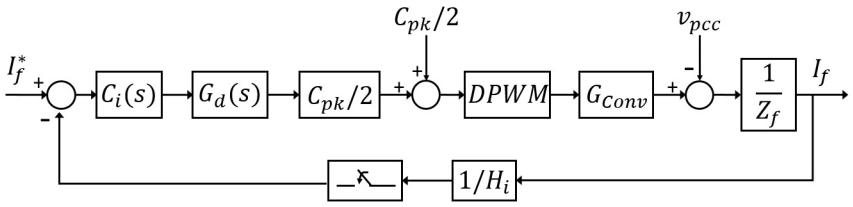

Fig. 2: Inverter-side current control loop

sampling time by λT_s, as shown in (2). Considering all those definitions, the open-loop TF of the current control loop can be determined as shown in (3):

$$DPWM = \frac{1}{C_{pk}} \cdot \frac{1+e^{-sT_s}}{2} = \frac{1}{C_{pk}} \cdot \frac{1}{1+\frac{sT_s}{2}} \tag{1}$$

$$DPWM = \frac{1}{C_{pk}} \cdot \frac{1}{1+s\frac{(1+\lambda)T_s}{2}} \tag{2}$$

$$G_{OL}^{I}(s) = \frac{K_p s + Ki}{s} \cdot \frac{V_{DC}}{H_i Z_f (1+s\frac{(1+\lambda)T_s}{2})} \tag{3}$$

Dynamic Stiffness

To evaluate the disturbance rejection capability of the system, the concept of DS, as defined in [8], is used. This quantity is defined as the capability of a system to reject a determined disturbance and quantified as the amplitude of the perturbation needed to produce a unit variation in the output. This concept can be used to analyze any system, but, in this particular case, the system's DS is equal to the output impedance of the inverter (Z_{out}) and, thus, has unit of [Ω]. It can be derived from the current control loop block diagram in Fig. 2 as the inverse of the TF between I_f and v_{pcc}. This diagram is redrawn in Fig. 3 to clearly show its derivation and the resulting expression is shown in (4). It is straightforward that a higher impedance makes the system less susceptible to perturbations in the grid voltage.

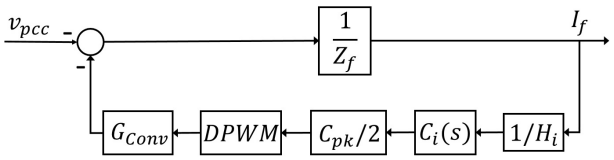

Fig. 3: Block diagram for determination of the output impedance

$$Z_{out}(s) = \frac{v_{pcc}}{I_f}(s) = -\left(\frac{V_{DC} \cdot DPWM(s) \cdot C_i(s)}{H_i} + Z_f\right) \tag{4}$$

Equation (4) shows that the magnitude of Z_{out} is directly proportional to the controller TF and, thus, explains why high-gain controller configurations have better disturbance rejection capability.

It is well known that the Proportional-Resonant has high gain on specific harmonics, which leads to a high output impedance at those frequencies. The Dead-Beat has a high gain and, thus, yields a very high output impedance in a wide range of frequencies [5]. As such, the disturbance rejection capability of the current control loop is very high when these kinds of controllers are used. The traditional PI controllers, however, have poor disturbance rejection capability due to its low gain in high frequencies. This leads to a poor performance when the inverter is connected to a grid with highly distorted voltage.

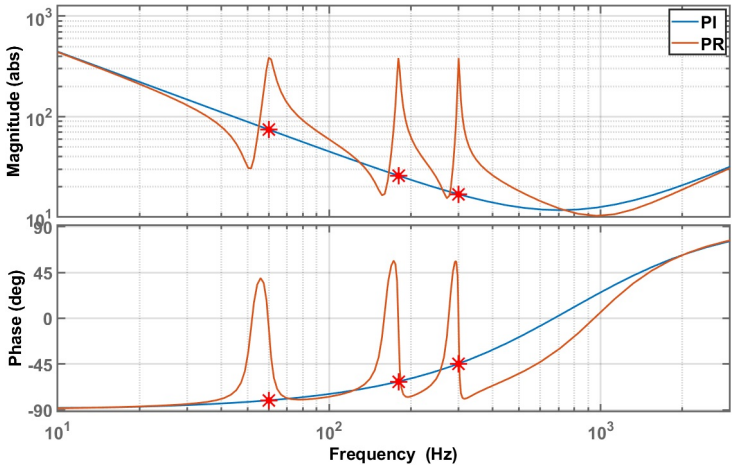

Fig. 4: Z_{out} for the current loop with PI and PR controllers

Table I: Data Points of Fig. 4

Freq [Hz]	Mag [Ω]	Ph [deg]
60	74.3	-80.6
180	25.9	-62.1
300	16.9	-44.5

Proposed control strategy

In the last section, it was discussed that using a PI as current controller may render the system susceptible to the circulation of disturbance currents due to its low resulting output impedance. However, this section demonstrates that this type of controller can achieve better results as long as an outer control loop is responsible for rejecting disturbances, as is the case of the strategy proposed herein.

Fig. 4 shows the Bode diagram of (4), with $C_i(s)$ being a PI controller. The fundamental grid frequency (60 Hz) and the third and fifth harmonics are highlighted. It can be seen that the impedance drops when the frequency increases, following the behaviour of the PI controller gain, yielding a low value in middle-range frequencies. Since the most significant voltage harmonics are usually located in the range between 180-900Hz, this deteriorates the system performance when the grid voltage is distorted. In higher frequencies, however, the impedance magnitude starts to rise again, due to the natural behaviour of the filter inductors. For comparison, the output impedance for the PR controller is also shown. It can be seen that, as expected, the output impedance is much higher on the selected frequencies.

Having determined the output impedance frequency response, it is possible to analytically determine the disturbance currents if the respective voltage harmonic are measured, as shown in (5), where ω_0 is the fundamental frequency in [*rad/s*]. This suggests that the disturbances can be completely eliminated if the system imposes an opposite current through the filter. However, to achieve this, it is not sufficient to use the opposite of I_h as reference for the current control loop. While for low frequencies this may yield good results, at high frequencies it is necessary to account for the current loop dynamics. Thus, to completely eliminate the disturbance currents, the reference has to be defined as shown in (6), where $G_i(s) = I_f(s)/I_f^*(s)$ represents the closed-loop TF of the current control.

$$I_h(jh\omega_0) = \frac{V_{PCC}(jh\omega_0)}{Z_{out}(jh\omega_0)} \tag{5}$$

$$I_h^*(jh\omega_0) = -\frac{V_g(jh\omega_0)}{G_i(jh\omega_0) \cdot Z_{out}(jh\omega_0)} \tag{6}$$

To test this assumption, a current-controlled grid-connected single-phase inverter is simulated in MATLAB/Simulink. In this simulation, the grid voltage had a fundamental magnitude of 127V RMS and 20% of both third and fifth harmonic components. Even though such a heavy distortion almost never occurs in real applications due to stringent grid codes, this severe condition is considered to test the controller's performance in an extreme situation. Additionally, for simplicity, all components are set with zero phase-shift; however, this assumption does not cause a loss of generality.

First, the current reference is set to zero and I_f is measured to determine the disturbance current. Fig. 5 shows the resulting waveform and Table II shows the magnitudes of each harmonic component, determined with the use of an FFT. It can be seen that these components are equal to the result of (5) if the impedance values shown in Fig. 4 and the respective voltage amplitudes are considered. In a following test, a reference signal composed of the fundamental, third and fifth harmonics, each one calculated according to (6), is applied as reference to the current control in an open-loop configuration and I_f is measured again. The result of this test is also shown in Table II and Fig. 5. It is evident that the compensation yielded very good results, almost eliminating the disturbance completely. Even better results can be achieved by considering the grid impedance in the output impedance calculation. However, as this is a parameter that is not usually known in real situations, it is not considered in this analysis. Nonetheless, the obtained results are sufficient to validate this equation.

Table II: Disturbance and compensated current components

Signal	**Harmonic Component**		
	1^{st}	3^{rd}	5^{th}
Grid Voltage (V_{pk})	180	36	36
Disturbance Current (A_{pk})	2.42	1.39	2.11
Compensated Current (A_{pk})	0.05	0.09	0.27

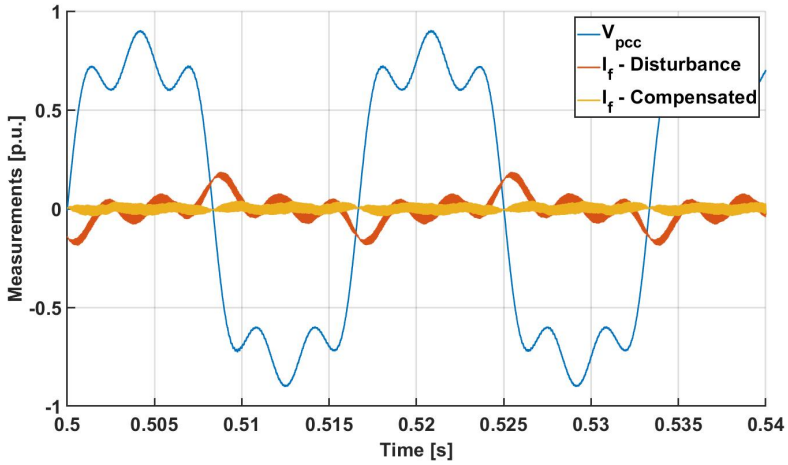

Fig. 5: Open-loop disturbance compensation

In conclusion, these tests proved that it is possible to reject the disturbance by manipulating the current loop reference, even if a PI is used as current controller. Nonetheless, as is rather obvious, the open-loop strategy shown is not feasible for a real application. Thus, it is necessary to develop a more robust system that behaves in a similar way, but is capable of compensating parameter variations such as deviations in the measured voltage magnitude and changes in the values of the output filter due to temperature fluctuations or wear and tear. Hence, the structure shown in Fig. 7 is proposed.

In this structure, a pair of PI controllers, $C_p(s)$ and $C_q(s)$, is responsible for regulating the flow of active (P) and reactive (Q) power. The output of each one of these controllers is then multiplied by purely sinusoidal signals, x_1 and $\hat{x}_1$, whose frequency is equal to the grid voltage fundamental component, being the first in-phase with the grid voltage and the second -90 degrees phase-shifted. These signals are generated by a PLL system, normally used in grid-connected inverters to synchronize the inverter with the grid voltage. The resulting signals, I_a^* and I_r^*, are then added, enabling the control of the magnitude and phase of the fundamental component of the output current. Fig. 6 shows the calculation method for all quantities and waveforms necessary for the control algorithm. The calculation of the active and reactive power is done in accordance to (7) [16], where $\widehat{v}_{pcc}$ is the integral of the PCC voltage without its average value, calculated as shown in (8).

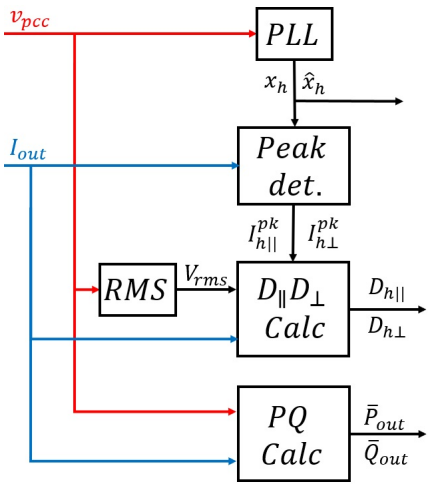

Fig. 6: Signal generation algorithm

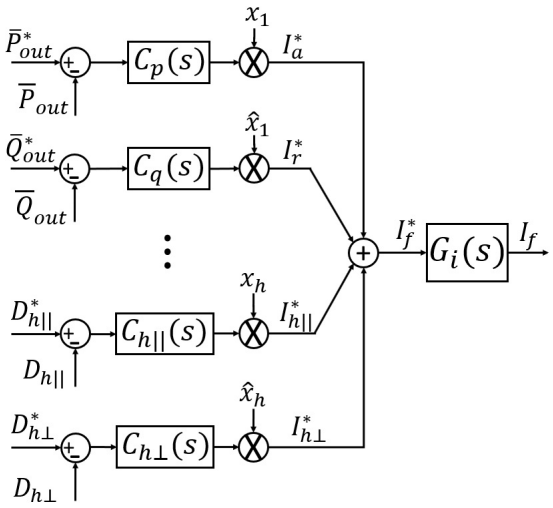

Fig. 7: Proposed control strategy diagram

$$P = \frac{1}{T_s}\int_{T_s} v_{pcc}\cdot i_f\, dt \qquad Q = \frac{1}{T_s}\int_{T_s} \hat{v}_{pcc}\cdot i_f\, dt \tag{7}$$

$$\hat{v}_{pcc} = \omega\int_0^t v_{pcc}\, d\tau - \frac{\omega}{T_s}\int_{T_s} v_{pcc}\, dt \tag{8}$$

Besides the active and reactive power control loops, this strategy is composed of N other controller pairs, being each one responsible for the regulation of one harmonic frequency. The behaviour of these loops is similar to the fundamental component loop. However, the harmonic distortion associated to each component is quantified differently. The quantities $D_{h\|}$ and $D_{h\perp}$ are calculated for each individual frequency as shown in (9) for the in-phase and quadrature components.

$$D_{h\|} = V_{RMS}\cdot\frac{I_{h\|}^{pk}}{\sqrt{2}} \qquad D_{h\perp} = V_{RMS}\cdot\frac{I_{h\perp}^{pk}}{\sqrt{2}} \tag{9}$$

This topology behaves similarly to what was presented in the test of Fig. 5, in the sense that the current reference signal is the sum of harmonic currents determined by the grid voltage and output impedance, corrected by the current loop dynamics. To demonstrate this behaviour, Fig. 8 shows the reference generated by the analytical calculation of (6) and the power control loop output (I_f^*) of Fig. 7, with all references set to zero. The box in Fig. 8 details the region around 0.5s. Since all parameters are known, the analytical derivation is very accurate and the signals are almost identical. If there are parameter deviations, the power control loop automatically corrects the current reference.

Power controller tuning

To size the power controllers, the open-loop TF of the power loop has to be derived. Even tough the system is non-linear due to the power calculation algorithm, in which signals are multiplied on the time-domain, an approximation can be derived. Fig. 6 and Fig. 7 show that the feedback of the power control loop is done through the PQ calculation algorithm, whose dynamic is slow as the implementation of (7) is usually done by a Moving-Average Filter (MAF), whose frequency response is complex, but can be reasonably approximated by a Low-Pass Filter (LPF) [17]. Here, the cutoff frequency of the equivalent LPF (ω_c) is equal to $2\pi\cdot 15$ *rad/s*.

Fig. 9 illustrates the control loop as a single entity, where $H_p = H_v\cdot H_i$ is the power base, equal to the product of the current and voltage sensor gains. In this figure, the regulated quantity is the active power, however, this structure remains nearly unchanged if a different quantity (Q, $D_{h\|}$ or $D_{h\perp}$) is to be

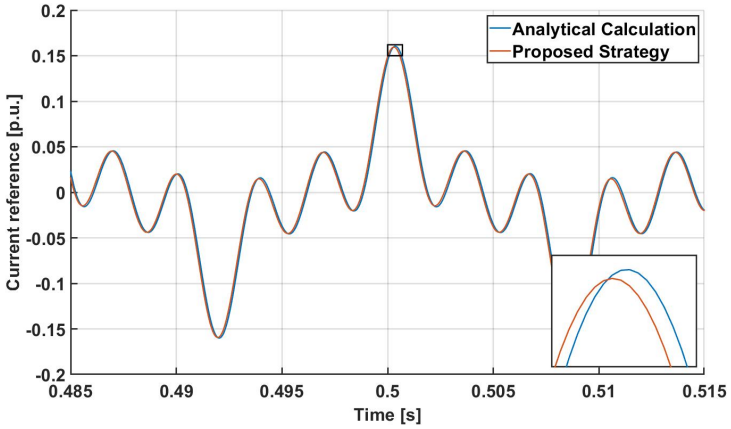

Fig. 8: Current references generated by the analytical calculation and proposed strategy

controlled, as only the frequency and phase of signal x_1 have to be changed. Hence, the power controller's tuning is independent of the frequency and the same K_p and K_i gains can be used for all controllers.

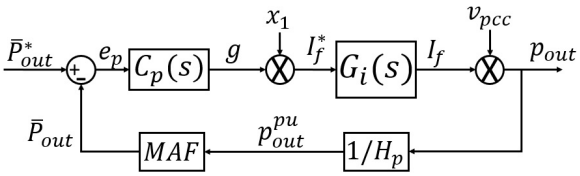

Fig. 9: Active power control loop

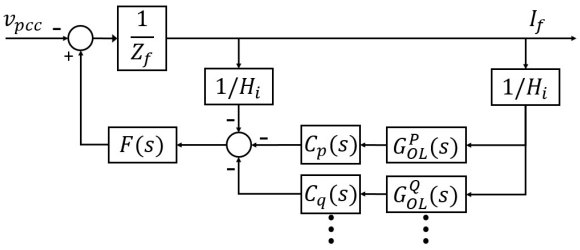

Fig. 10: Z_{out} considering the power control loop

The instantaneous active power signal, p_{out}, can be calculated as shown in (10). Because of the slow dynamic of the power control, the current loop, $G_i(s)$, can be approximated as a static gain, H_i. In here, this approximation is valid for frequencies up to 100Hz. Additionally, because of its low bandwidth, it is reasonable to assume that the MAF completely rejects the high-frequency component of p_{out}. Thus, only the average signal value has to be considered for tuning the controller [18]. The open-loop TF is shown on (11). From this equation, the PI can be tuned by any desired method.

$$p_{out} = g \cdot x_h \cdot H_i \cdot v = g \cdot H_i \cdot V_{pk} \cdot sin^2(h\omega_0 t) = \frac{g \cdot V_{pk} \cdot H_i}{2}\left[1 - cos(2h\omega_0 t)\right] \tag{10}$$

$$G^{P,Q,D}_{OL} = \frac{V_{pk}}{2H_v}\frac{\omega_c}{s+\omega_c} \tag{11}$$

Output impedance analysis

The use of the power controller as an external loop increases the inverter's output impedance at the selected frequencies. However, since the model derived to tune the PI is simplified, it is necessary to derive a more complete TF of the system in order to illustrate this behavior.

The PI output is constant in time when in steady-state and I^*_f may be either a sine or cosine. The multiplication by x_h can be represented by the division of both signals' Laplace transforms. Thus:

$$\frac{I^*_{f,h\parallel}}{g}(s) = \frac{sh\omega_0}{s^2 + (h\omega_0)^2} \qquad \frac{I^*_{f,h\perp}}{g}(s) = \frac{s^2}{s^2 + (h\omega_0)^2} \tag{12}$$

Regarding the second multiplication, because of how the current reference is generated, I_f can be considered a purely sinusoidal signal. However, the PCC voltage may have an undetermined number of

harmonic components. Nonetheless, since the strategy controls the average value of the power quantities, and the average value of the multiplication between signals of different frequencies is always equal to zero, these components can be disregarded when analyzing a single harmonic. Treating the power calculation in the time-domain as a phasor multiplication in the frequency domain and assuming that the current angle will be either zero or 90°, the average active power can be defined as shown in (13). An analogous derivation can be done for all other controlled quantities. Finally, it is necessary to consider the dynamics of the MAF. Hence, it is possible to determine the open-loop transfer function of the in-phase and quadrature loops, shown on (14).

$$\overline{P}_{out} = |I_a|\angle\Theta_a \cdot |v_{pcc}|\angle 0^\circ = |I_a|\angle 0^\circ \cdot |v_{pcc}|\angle 0^\circ = \frac{I_{a,pk} \cdot V_{pk}}{2} \tag{13}$$

$$G_{OL}^{\parallel}(s) = \frac{V_{pk}(h\omega_0)}{2H_v} \frac{\omega_c}{s+\omega_c} \frac{s}{s^2+(h\omega_0)^2} \qquad G_{OL}^{\perp}(s) = \frac{V_{pk}}{2H_v} \frac{\omega_c}{s+\omega_c} \frac{s^2}{s^2+(h\omega_0)^2} \tag{14}$$

Expanding the current loop on Fig. 9, as shown on Fig. 2, and rearranging the diagram to obtain the TF between the output current and grid voltage, the system shown on Fig. 10 is obtained. For simplicity, this diagram is shown with only the P loop, but can easily include as many loops as needed, being all in parallel with the ones shown. Equation (15), where $F(s) = DPWM(s) \cdot G_{conv} \cdot C_i(s)$, shows the complete equation for the output impedance of the system. Its Bode diagram is shown on Fig. 11, where it can be seen that there is a peak at the selected frequencies, like the ones in Fig. 4. However, these peaks are narrower and their magnitude is bigger, approximating the behaviour of an ideal PR. However, the proposed topology does not face the same stability issues.

$$Z_{out}(s) = -\left[Z_f(s) + \frac{F(s)}{H_i}\left(1 + \sum C_{P,Q,D}(s) \cdot G_{OL}^{P,Q,D}(s)\right)\right] \tag{15}$$

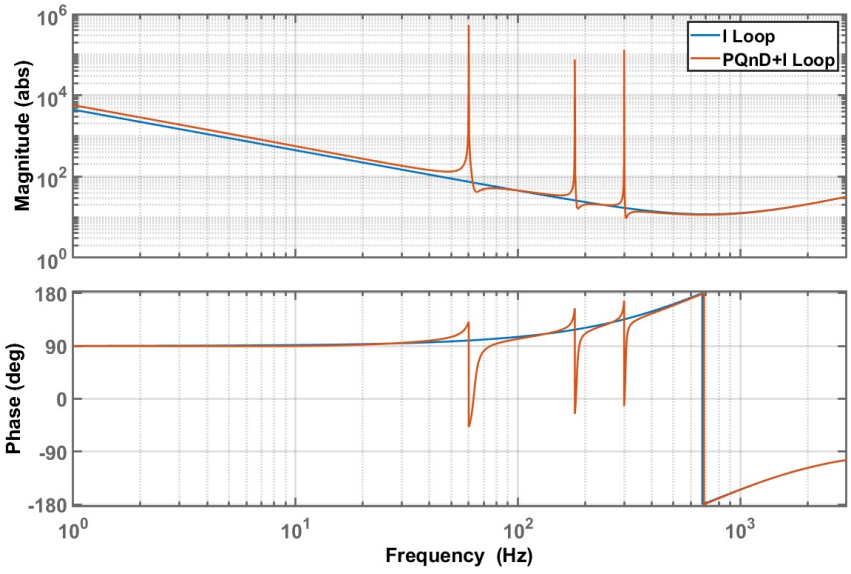

Fig. 11: Output impedance when applying the power control loops

Simulation Results

To evaluate the proposed strategy, simulations are devised in MATLAB/Simulink. Table III and Table IV show its parameters. In terms of steady-state performance, it can be seen from Fig. 12 that the system has a satisfactory behaviour, since the active and reactive power track the reference signals and stabilize in less than 0.1 seconds. Fig. 13 shows the PCC voltage and filter current waveforms during the steps in the

references. It is evident that the output current has low THD despite the heavily distorted grid voltage. In fact, an FFT shows that the THD is equal to 3.36% in Fig. 13(a) and 2.43% in Fig. 13(b), being the present harmonic components associated to the PWM switching. Finally, the figures show that the current increase is smooth during the transients, avoiding dangerous overcurrents or angle differences.

Table III: System parameters

Parameter	Symbol	Value	
Filter inductance	L_f	1.0	mH
Filter ESR	R_f	0.5	Ω
Filter capacitor	C_f	6.6	μF
Capacitor ESR	R_c	1.0	mΩ
Grid inductance	L_g	60	μH
Grid resistance	R_g	0.12	Ω
DC bus voltage	V_{dc}	400	V
Switching frequency	f_{sw}	12	kHz
Sampling frequency	f_s	24	kHz

Table IV: Controller parameters

Parameter	Symbol	Value	
P Gain - Current	K_{pi}	1.0723	Ω
I Gain - Current	K_{ii}	0.1015	F^{-1}
P Gain - Power	K_{pp}	0.8577	V^{-1}
I Gain - Power	K_{ip}	0.0066	

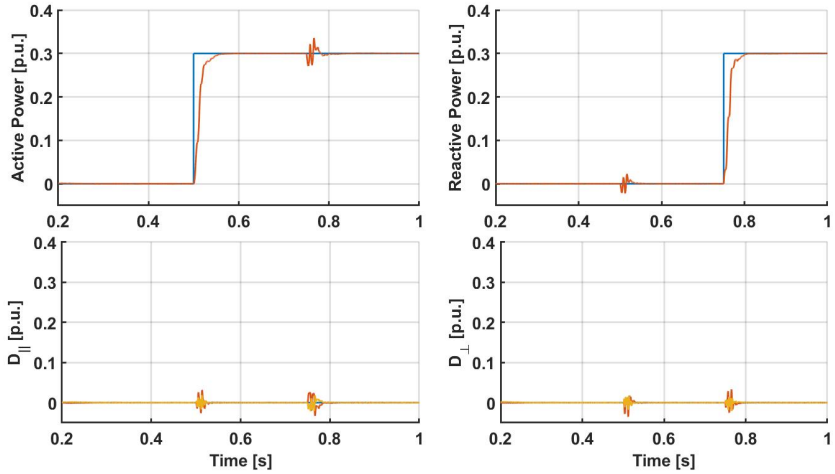

Fig. 12: Simulation results - Calculated power terms

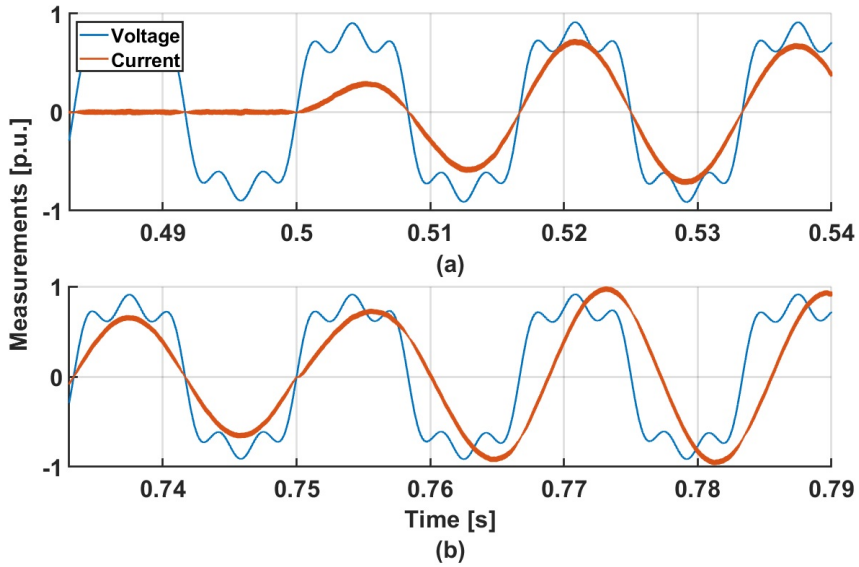

Fig. 13: Simulation results - PCC voltage and filter current ($THD_v = 28.3\%$, $THD_i = 3.36\%/2.43\%$)

Conclusion

This paper presented a scheme to implement the power and current control loops for a grid-connected inverter. Its physical behaviour was explained in-depth and simulation results were presented to evaluate its performance. It was shown that low current THD can be achieved even when highly distorted grid voltage is considered.

The proposed control scheme has the advantage over traditionally used methods such as the Proportional-Resonant because it is not as complex and can be more easily implemented. Compared to the Dead-Beat controller, this topology is not as sensitive to parameter variations.

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