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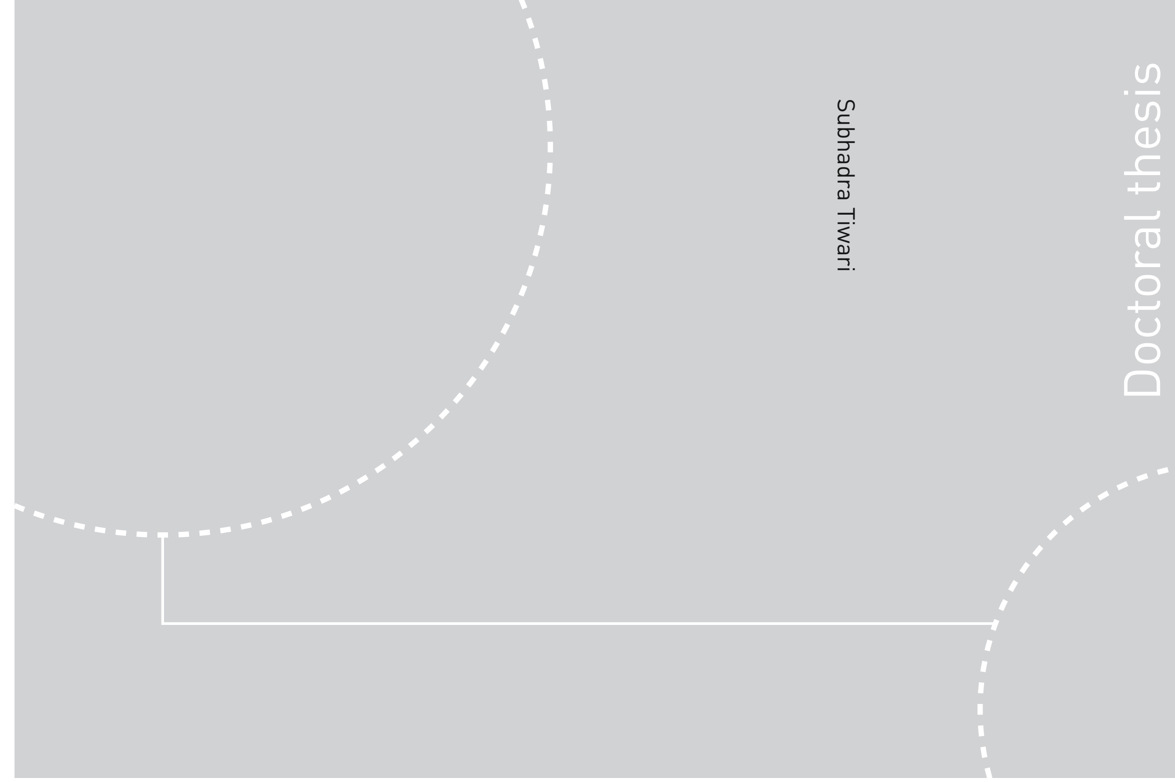

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To my parents

Preface

This thesis is submitted to the Norwegian University of Science and Technology (NTNU) in partial fulfillment of the requirements for the degree of philosophiae doctor (PhD).

The research is carried out at the Department of Electric Power Engineering, Faculty of Information Technology and Electrical Engineering, NTNU, Norway. The PhD work is sponsored by The Research Council of Norway, and six industry partners: EFD Induction, Siemens, Eltek, Norwegian Electric Systems, and Vacon.

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Subhadra Tiwari

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Subhadra Tiwari

Abstract

The future power electronic system trends are: higher efficiency, higher power density, higher operating temperature and lower operation cost of power electronic converters. The emerging wide-bandgap (WBG) semiconductor material, especially silicon carbide (SiC), exhibits outstanding inherent properties that promise the potential to meet the subsequent growing demands. SiC enables the development of power devices capable of switching efficiently even at higher voltages and temperatures compared to the matured and well-established Si technology of today. Nonetheless, parasitic inductance and capacitance in the switching circuit are limitations for fully unleashing the fast-switching potential of these devices. The objective of this research is to evaluate what the state-of-the-art SiC devices, particularly SiC MOSFETs, offer at present and what can be done for better realizing their high switching-speed capability.

First, to assess the fast dynamic characteristics of SiC devices with a high degree of accuracy, measurement probes and oscilloscope with adequate bandwidth along with low-inductive connections are adopted. Switching characterization was conducted via double-pulse test in hard-switched as well as in resonant topology. Based on the measurement results, it is recommended to use a realistic topology for the precise assessment of switching losses in SiC devices.

Second, the state-of-the-art SiC MOSFET modules are examined to determine how fast they switch compared to the class-leading IGBT modules, given that they are packaged in the standard plastic housing. Measurement results revealed that the maximum dv/dt and di/dt rates that SiC MOSFET achieves are: 20 V/ns and 11 A/ns at 600 V bus voltage and 120 A load current. Si IGBT, on the other hand, achieved 17 V/ns and 12 A/ns when switched at similar conditions. According to this result, it can be inferred that dv/dt and di/dt rates that SiC MOSFET reaches are not as revolutionary as its intrinsic properties can potentially offer. In fact, this outcome can be attributed to the higher internal gate resistance that manufacturers use for avoiding oscillation during turn-off and the higher package inductance. In order to know what else can be achieved using SiC MOSFET, the body-diodes of the state-of-the-art SiC MOSFETs (both planar and trench technologies) were inspected. A particular focus was put on di/dt during the second-half of the recovery, keeping di/dt on the first-half of the recovery constant for all the devices being tested. Experimental outcomes revealed that the body-diodes in new generation SiC MOSFETs are as good as SiC junction barrier Schottky (JBS) diodes from the switching point of view. Nonetheless, the forward voltage drop is higher approximately by a factor of 3 compared to unipolar SiC Schottky diodes. Based on this information and the research conducted by another team, which confirmed that the body-diodes in new SiC MOSFETs do not create reliability issues anymore like those seen in the initial generation SiC MOSFETs, it is concluded that the body-diodes in SiC MOSFETs work effectively as freewheeling diodes.

Third, SiC MOSFETs are evaluated in three different key applications. One of those applications is a 240 kW back-to-back connected three-phase, two-level voltage source converter for motor drive, which disclosed that, for the same converter power loss, the switching frequency in an all-SiC-based converter can be increased by six times compared to that of an all-Si-based converter. Another application is an 80 kW single-phase, full-bridge inverter for induction heating applications, which proved an efficiency of 99.3% when switched at 200 kHz. SiC DioMOS, where MOSFET and diode are fabricated in a single chip, was the device under test and the inverter loss was measured via calorimetric method in this case. Finally, a 1 kW power factor correction rectifier is evaluated employing SiC MOSFET and SiC JBS diode in boost stage. A peak efficiency of 97.2% was achieved when switched at 250 kHz satisfying the 80 PLUS regulation throughout the entire load range. Moreover, EMI measurements revealed that the rectifier satisfies CISPR 11 Class B limits. Furthermore, when the switching frequency was increased from 66 to 250 kHz, the size of boost inductor was reduced drastically, while the emissions were increased by roughly 10 dB throughout the entire conducted spectra for the identical size of EMI filter.

To further unlock the fast switching potential of SiC devices, low-inductive converter design guidelines are proposed, such as the selection of DC-clamping capacitors with low internal inductance and their appropriate orientation and stripline layouts whenever possible maintaining width to length ratio larger than unity. Two design examples for further achieving low switching loop inductance with SiC modules and discrete SiC devices are provided. For the SiC modules, multiple DC-source busbars for multiple screw hole modules are recommended. As internal inductance of the standard module is larger, an example of layout employing seven-pin discrete SiC MOSFETs and Ceralink capacitors is designed, the switching loop inductance of which is estimated to be 5 nH via 3D FEM simulations.

Keywords: Silicon Carbide (SiC), Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET), Junction Barrier Schottky (JBS) diodes, High-Efficiency Converters, Low inductance designs.

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List of Symbols

Acronyms

3L-NPC	Three-Level Neutral Point Clamped
3D	Three-Dimensional
AC	Alternating Current
Al_2O_3	Aluminum Oxide (DBC substrate)
AlN	Aluminum Nitride (DBC substrate)
BJT	Bipolar Junction Transistor
BW	Bandwidth
CCM	Continuous Conduction Mode
CISPR	International Special Committee on Radio Interference (original french abbreviation)
CM	Common Mode
CoolMOS	Trade mark of Infineons charge compensated silicon MOSFET
CVR	Current viewing resistor (resistive current shunt)
DBC	Direct Bonded Copper
DC	Direct Current
DM	Differential Mode
DPT	Double-Pulse Test
DUT	Device Under Test
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
FEA	Finite Element Analysis
FEM	Finite Element Method
FOM	Figure-of-Merit
FS	Field-Stop
GaN	Gallium Nitride
GTO	Gate Turn-off Thyristor
HEV	Hybrid Electric Vehicle
IEC	International Electrotechnical Commission
IGBT	Insulated-Gate Bipolar Transistor
IGCT	Insulated Gate Commutated Thyristor
JBS	Junction Barrier Schottky (diode)
JFET	Junction Field Effect Transistor
LISN	Line Impedance Stabilizing Network
MEA	More Electric Aircraft
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MPS	Merged PiN Schottky (diode)

NPT	Non-Punch-Through
PCB	Printed Circuit Board
PCC	Point of Common Coupling
PFC	Power Factor Correction
PWM	Pulse Width Modulation
Q3D	Quick Three Dimension
QP	Quasi-Peak (used for EMC measurements)
SBD	Schottky Barrier Diode
Si	Silicon
Si_3N_4	Silicon Nitride (DBC substrate)
SiC	Silicon Carbide
SJT	Super Junction Transistor
SPT	Soft-Punch-Through
SVPWM	Space Vector Pulse Width Modulation
THD	Total Harmonic Distortion
VMOS	Vertical Metal-Oxide-Semiconductor (structure)
VSC	Voltage Source Converter
VSD	Variable Speed Drive
WBG	Wide-Bandgap
ZVS	Zero Voltage Switching

Abbreviations (Sub-script)

ac	Alternating current
avg	Average
dc	Direct current
inp	Input
max	Maximum or maximal
min	Minimum or minimal
n	Electron, negative charge carrier
out	Output
p	Hole, positive charge carrier
pp	Peak-to-peak
res	Resonance
rms	Root mean square
tot	Total

Variables

C_{DC}	DC-link capacitance
C_{ds}	Drain-source capacitance of a transistor
C_{gd}	Gate-drain capacitance of a transistor
C_{gs}	Gate-source capacitance of a transistor
C_{iss}	Input capacitance of a transistor
C_L	Parasitic capacitance of inductor
C_{oss}	Output capacitance of a transistor
C_{rss}	Miller capacitance of a transistor
E_{crit}	Critical electric field
E_g	Band gap energy
E_{off}	Transistor turn-off energy loss
$E_{off-spec}$	Specific turn-off energy loss of a transistor
$E_{off-spec-elec}$	Specific turn-off energy loss of a transistor measured via electrical method
$E_{off-spec-calori}$	Specific turn-off energy loss of a transistor measured via calorimetric method
E_{on}	Transistor turn-on energy loss
$E_{on-spec}$	Specific turn-on energy loss of a transistor
E_{rr}	Diode reverse-recovery energy loss
$E_{rr-spec}$	Specific reverse energy loss of a diode
ESL	Equivalent series inductance
ESR	Equivalent series resistance
E_{tot}	Transistor total switching energy loss
f_{line}	Line frequency
f_{osc}	Frequency of oscillation
f_{res}	Resonant frequency
f_{sw}	Switching frequency
G_{lower}	Gate signal to lower transistor in a phase-leg
G_{upper}	Gate signal to upper transistor in a phase-leg
I_{ce}	Collector-emitter current
I_{DC}	DC-link current
I_{ds}	Drain-source current
I_F	Diode forward current
I_L	Load current
I_{os}	Current overshoot of a transistor
I_{out}	Peak output current
$I_{out,rms}$	rms output current
I_{ref}	Reference current
I_{rrm}	Peak reverse-recovery current
J	Current density
$L_{byp-con}$	Parasitic inductance of a bypass capacitor connection
$L_{byp-ESL}$	Internal parasitic inductance of a bypass capacitor
$L_{stray,tot}$	Total parasitic inductance of a switching loop
$L_{trans-module}$	Internal parasitic inductance of a transistor module
$L_{trans-module-con}$	Parasitic inductance of a transistor module connection
m	Modulation index

P_{cond}	Conduction losses
P_{sw}	Switching losses
P_{sw-off}	Transistor turn-off switching power loss
P_{sw-on}	Transistor turn-on switching power loss
Q_c	Transistor capacitive charge
Q_g	Transistor gate charge
Q_{rr}	Transistor reverse-recovery charge
$R_{CE,on}$	Collector-emitter on-resistance
R_d	Diode on-resistance
$R_{DS,on}$	Drain-source on-resistance
$R_{g,ext}$	External gate resistance
$R_{g,int}$	Transistor internal gate resistance
$R_{g,off}$	Transistor turn-off gate resistance
$R_{g,on}$	Transistor turn-on gate resistance
f_{sw}	Switching frequency
$R_{th,jc}$	Thermal resistance between junction and case
T_{in}	Input temperature
T_j	Junction temperature
T_{out}	Output temperature
V_{ce}	Collector-emitter voltage
V_{CEO}	Transistor knee voltage
V_{DC}	DC-link voltage
V_{ds}	Drain-source voltage
V_F	Forward voltage (drop)
V_{F0}	Diode knee voltage
V_{gs}	Gate-source voltage
V_{gs-L}	Gate-source voltage of lower transistor in a phase-leg
V_{gs-H}	Gate-source voltage of higher transistor in a phase-leg
$V_{gs,th}$	Gate-source threshold voltage
V_{os}	Voltage overshoot of a transistor
V_{pp}	Peak-to-peak voltage
V_{ref}	Reference voltage
η_i	Intrinsic carrier density
i_L	Inductor instantaneous current
i_{ds}	Instantaneous drain-source current
i_d	Diode instantaneous current
p_{inst}	Instantaneous power loss
p_{avg}	Average power loss
t_b	Blanking time
t_d	Delay time
t_{fall}	Fall time
t_{hold}	Hold-up-time
t_{rise}	Rise time
t_{rr}	Diode reverse-recovery time
ϕ	Output current-to-voltage displacement angle
ϵ	Permittivity
ϵ_r	Relative permittivity

η	Efficiency
λ_{th}	Thermal conductivity
μ_n	Electron mobility
μ_p	Hole mobility
$v_{s,min}$	Minimum input voltage
$v_{s,max}$	Maximum input voltage
v_{out}	Output voltage

Constants

$\epsilon_0 = 8.854 \cdot 10^{-12}$ F/m	Permittivity of free space
$\mu_0 = 1.257 \cdot 10^{-6}$ H/m	Permeability of free space

Chapter 1

Introduction

This chapter starts with the background and motivation behind this doctoral dissertation. In the next section, the scope of the work and the structure of the thesis are presented. This is then followed by the methodology adopted. Finally, the chapter is concluded, giving a brief overview of the main scientific contributions and the publications.

1.1 Background and motivation

Power electronics is associated with the efficient conversion, control and conditioning of electric energy to supply a wide range of loads at various voltages, currents and frequencies [1]. This technology has enabled applications, such as variable-speed motor drives, renewable energy integration, transportation electrification, and more-efficient data centers [1–7]. In this way, problems of the increasingly growing demand for energy, the limited availability of fossil fuels and the need for carbon footprint reduction can be overcome by a considerable degree.

The continuous development of an improved power semiconductor device has always been an impulsive force for power electronic converters, which is the heart of power electronics. Currently, low power systems use silicon (Si) metal-oxide-semiconductor field-effect transistors (MOSFETs) in planar and super junction technologies, and silicon insulated-gate bipolar transistors (IGBTs). Furthermore, medium-and high-power systems are greatly dominated by Si IGBTs, Si integrated gate-commutated thyristors (IGCTs), or Si gate turn-off thyristors (GTOs) [7]. Si-based power semiconductor devices are matured and well-established in today's power converters. However, they are approaching their material theoretical limits in terms of blocking voltage capability ($\leq$ 6.5 kV) [8], which requires the series connection of devices or multilevel converter topologies. It is worth noting that the series connections lead to voltage imbalance issues and multilevel converters require complex control. In addition, both of these solutions increase the component count. Another constraint is the reliable maximum operating temperature (125–150°C), which potentially impedes the high temperature applications, for example, deep-well drilling, automotives and avionics [9–13]. In addition, unipolar devices (e.g., MOSFETs and Schottky diodes) are limited with regard to conduction losses and bipolar devices (e.g., IGBTs, IGCTs, and GTOs) are constrained with respect to switching performances. Accordingly, efficiency and switching frequency of the high-voltage power converters are limited.

The future power electronic system trends are higher power, higher temperature, higher efficiency, higher power density, higher reliability, and lower operational cost of power electronic converters, which can potentially be met by emerging wide-bandgap (WBG) semiconductors. Amongst the various WBG semiconductors, silicon carbide (SiC) and gallium nitride (GaN) are the most promising candidates because of their superior inherent material properties compared to Si, leading to ideal solid-state components. However, due to the lack of good quality bulk substrates needed for vertical devices and the low thermal conductivity, GaN is primarily anticipated to cover low-voltage, low-power (600 V, kW or below) applications, while SiC favors high-voltage, high-power (600V, kW or above) areas [2, 14]. This thesis essentially concentrates on SiC power devices. Section 1.2 presents the scope of the work.

1.2 Scope of the work

The main objective of this work is to evaluate state-of-the art SiC power devices, particularly SiC MOSFET modules, in a low-inductive system setup and connections. Then implement a prototype converter based on one of the new devices along with the ancillary systems and components. The defined tasks are itemized as follows:

- Review of the available SiC diodes and SiC transistors in order to understand the benefits and challenges associated with this new technology. *This is covered in Chapter 2.*
- Investigate state-of-the-art measurement techniques capable of assessing the potential fast dynamic characteristics of SiC devices with high fidelity. Implement a practical method to accurately evaluate the switching loss of SiC devices. *Key contributions are presented in Chapter 3.*
- Characterize and understand state-of-the-art SiC MOSFET modules via laboratory measurements and circuit simulations. *Key contributions are presented in Chapters 4 and 5.*
- Implement a prototype of a converter based on one of the new devices along with the ancillary systems and components. *Key contributions are presented in Chapter 6.*
- Quantify the benefit of employing state-of-the-art SiC devices over their Si counterparts in power electronic converters through hardware measurements. *Key contributions are presented in Chapter 6.*
- Develop the design guidelines for the optimal use of SiC devices in power electronic converters. *Key contributions are presented in Chapter 7.*

1.3 Structure of the thesis

Chapter 1. includes an introduction and a brief background of the topic, and states the scope of the work as well as the methodology. Moreover, it describes the main scientific contributions.

Chapter 2. provides a short overview of the development of SiC power devices in the last two decades. A brief summary of state-of-the-art, commercially available SiC devices as well as those still in research is presented. Finally, a brief description of the packages employed by commercialized SiC devices and the challenges associated in adopting these devices follows.

Chapter 3. describes the prerequisites for accurate assessment of switching loss by electrical method and delineates the importance of employing an appropriate converter configuration for correct evaluation of switching loss.

Chapter 4. characterizes state-of-the-art SiC MOSFET modules to answer how fast these devices switch compared to class-leading Si IGBT modules and how their switching performances differ from each other, which are also the key research questions in the thesis.

Chapter 5. shows the experimental investigation of body-diodes in state-of-the-art SiC MOSFETs to be able to answer if these intrinsic/parasitic diodes are sufficiently effective as freewheeling diodes.

Chapter 6. presents three potential applications of SiC MOSFETs: motor drive, induction heating, and power factor correction.

Chapter 7. includes low-inductive converter design considerations and exemplifies layouts for the optimal use of fast switching potential of SiC devices.

Chapter 8. summarizes the work done in this thesis along with the main contributions and gives an outlook on possible future work.

Appendices present the supporting texts and figures for the thesis.

1.4 Methodology

The results of this work are primarily based on laboratory experiments. However, theoretical and mathematical analysis along with circuit simulations are also employed for clarifying the results obtained from the hardware. Measuring the voltage and current waveforms via high-bandwidth voltage probes, such as single-ended passive probes and differential probes, and current probes, namely coaxial shunts, the experimental verifications are performed. Moreover, high precision digital multi-meters are also used for monitoring the voltages and currents while an impedance analyzer is used for measuring the passive components values. In addition, the passive elements of the busbar are simulated via an Ansys Q3D extractor. Furthermore, the converter loss is measured via calorimetric and electrical approaches. In the electrical approach, a widely accepted double-pulse test methodology and Yokogawa WT3000 power analyzer are adopted. Moreover, for EMI measurement, a standard line impedance stabilizing network (LISN) and an EMC analyzer (Agilent E7401A) are used.

1.5 Main scientific contributions

This thesis has resulted in the following main contributions to research:

- **Significance of a realistic inverter topology:** SiC MOSFET has been evaluated in this thesis via a double-pulse test methodology in two different circuit configurations: hard- versus resonant-switched topologies. Turn-off switching losses imposed in the SiC MOSFET by two chosen topologies are compared. The results reveal two clear messages: first, even at the same switching current, the resonant converter has significant advantages over the hard-switched one, from a switching loss viewpoint. Second, an appropriate inverter topology must be adopted for the correct assessment of switching loss. These outcomes were presented in [15] and are amongst the key contributions of this thesis.

- **Experimental evaluation of state-of-the-art SiC MOSFET modules:** Switching performances of SiC MOSFET modules have previously been evaluated by other research teams, for instance, SiC MOSFET modules were compared with SiC IGBT modules under similar dv/dt conditions in [16]. However, this thesis extends the research by comparing SiC MOSFET modules under a series of different conditions, such as similar dv/dt per chip size, similar di/dt per chip size, similar voltage overshoot and similar current overshoot. Most importantly, the main intention of this work is to answer how fast state-of-the-art commercially available SiC MOSFET modules switch compared to class-leading Si IGBT modules, given the same packages. These results were published in [17, 18].

- **Experimental evaluation of the body-diodes in state-of-the-art planar and double-trench SiC MOSFETs:** The switching characterization of body-diodes in state-of-the-art discrete SiC MOSFETs and discrete cascode SiC JFET are experimentally investigated and compared with Schottky diodes with the aim of answering if these intrinsic diodes are suitably effective as freewheeling diodes. A number of key electrical parameters, such as peak reverse-recovery current, and recovery time, are measured under similar dv/dt, and di/dt conditions during the first-half of reverse-recovery. To the best of the author's knowledge, di/dt during the second-half of the reverse-recovery and dv/dt are not provided in the manufacturers' data sheets and are barely discussed in the literature. The results were reported in [19].

- **Quantification of the performance gain using SiC MOSFETs over Si IGBTs:** A 240 kW, back-to-back connected, two-level, three-phase, voltage source converter (VSC) for wind power application is evaluated, from an efficiency standpoint, with the objective of quantifying the benefit of using SiC MOSFET over best-in-class Si IGBT using a space vector pulse width modulation (SVPWM) technique. Through the combination of experimental and simulation results, the converter efficiency is quantified, which revealed that the solution with SiC MOSFET entails lower losses compared to that with Si IGBT over all the switching frequency ranges; the advantages of SiC being more pronounced at higher frequencies and higher temperatures. Furthermore, it is also illustrated that for the same output power the inverter switching frequency can be increased by approximately six times in the SiC MOSFET compared to that in the Si IGBT with a similar total power

loss. Despite the large number of recent publications quantifying the benefits of SiC over Si [20, 21], very few have compared the state-of-the-art devices with same voltage and current ratings. This work, in addition to comparing the performance of similar rated devices, also verifies the methodology employed. For example, the simulation results are compared with the analytical and the numerical solutions. The results are found to be within 10% accuracy and was published in [22].

- **Evaluation of SiC DioMOS in a continuous converter operation:** A 78 kW, low-inductive, full-bridge, resonant inverter is built adopting SiC DioMOS for an induction heating application with the aim of quantifying the soft switching loss with a calorimetric loss measurement method. By switching the device just above the zero-crossing of the current during turn-off and at perfect zero voltage during turn-on, an efficiency of 99.3% is demonstrated at full-rated power. The results were published in [15]. Note that this device has both MOSFET and diode fabricated in a single chip; however, in a standard SiC MOSFET module, each of them are fabricated separately. This work was the basis for making a 1.85 MW, 300 kHz welder put into operation approximately one year later. To the best of the author's knowledge, this is the biggest SiC welder still in operation [23].

- **Conducted EMI evaluation of a single-phase boost converter:** SiC-based diodes and MOSFETs switch extremely quickly with low conduction losses. Thus, from the perspective of efficiency, such devices are ideal for a continuous conduction mode (CCM) boost power factor correction (PFC) converter. However, the circuit parasitic becomes alive while switching with high dv/dt and di/dt values, which necessitates the need for EMC compliance measurements. In this study, a 1 kW PFC boost converter prototype was designed, developed, and evaluated with the objective of quantifying the efficiency and electromagnetic compatibility signature. To maximize the efficiency, a fast, clean switching of the SiC is necessary. Utilizing a low-parasitic printed circuit board design approach and switching the selected low-loss SiC devices with a 0 Ω external gate drive resistance, this PFC boost yields a peak efficiency of 97.2% at full rated power when switched at 250 kHz. Furthermore, the EMI noise was measured at 66 and 250 kHz. It was found that the same EMI filter size satisfies the CISPR 11 Class B conducted EMI limit at both switching frequencies with a noise of approximately 10 dB higher at 250 kHz. Evaluation of the best case efficiency and worst case EMI is the main contribution of the present study. The results are included in article [24].

- **Low-inductive converter design considerations:** Low-inductive transistor case [25, 26] and busbars [27, 28] have recently received considerable attention. Employing low stray inductance DC-link capacitors is essential for realizing the low stray inductance designs. The interface methods used to connect the DC-link capacitors to the system, such as the busbar, are equally important. Reviewing the commercially available low inductance DC-link capacitors with different physical sizes and terminations, this work presents the design of a DC-link for a 100 kW full-bridge AC-DC-AC converter. Further investigating the geometry and orientation of the DC-clamping capacitor, this thesis provides guidelines on mounting these capacitors for reducing the SiC transistor turn-off over voltages. A few design examples for further minimizing the switching loop stray inductance when used SiC modules and discrete SiC packages are also provided in [29, 30].

1.6 Overview of publications

This section presents an overview of publications resulting from the PhD research and which have been published and presented in various peer-reviewed conferences, journals and tutorials. Section 1.6.1 includes a list of journal publications. Section 1.6.2 lists conference publications. Among the listed conference papers, parts of **C10** and **C11** are extended and included in journal paper **J2**. Papers **C7** and **C8** are the initial-phase publications, which helped to define the problem and to develop ideas during the research. In addition, a part of the PhD work is disseminated in relevant workshop and conference tutorials, which are listed in Section 1.6.3.

1.6.1 List of journal papers

J1. **S. Tiwari**, T. M. Undeland, O.-M. Midtgård, and R. Nilsen, "SiC MOSFETs for Offshore Wind Applications," in *Journal of Physics: Conference Series*, 1104(1):012032, 2018.

J2. **S. Tiwari**, J. K. Langelid, T. M. Undeland, and O.-M. Midtgård, "Merits of SiC MOSFETs for high-frequency soft-switched converters, measurement verifications by both electrical and calorimetric methods," in EPE Journal, 2019, DOI: 10.1080/09398368.2019.1586375.

J3. **S. Tiwari**, S. Basu, T. M. Undeland, O.-M. Midtgård, "Efficiency and Conducted EMI evaluation of a single-phase power factor correction boost converter using state-of-the-art SiC MOSFET and SiC diode," in IEEE Transactions on Industry Applications, May 2019, DOI: 10.1109/TIA.2019.2919266.

1.6.2 List of conference papers

C1. **S. Tiwari**, O.-M. Midtgård, and T. M. Undeland, "SiC MOSFETs for future motor drive applications," in *18th European Conference on Power Electronics and Applications (EPE'16 ECCE Europe)*, Karlsruhe, 2016, pp. 1-10.

C2. **S. Tiwari**, O.-M. Midtgård, and T. M. Undeland, "Experimental performance evaluation of two commercially available, 1.2 kV half-bridge SiC MOSFET modules," in *IECON 2016 - 42nd Annual Conference of the IEEE Industrial Electronics Society*, Florence, 2016, pp. 1106-1111.

C3. **S. Tiwari**, O.-M. Midtgård, and T. M. Undeland, "Comparative evaluation of a commercially available 1.2 kV SiC MOSFET module and a 1.2 kV Si IGBT module," in *IECON 2016 - 42nd Annual Conference of the IEEE Industrial Electronics Society*, Florence, 2016, pp. 1093-1098.

C4. **S. Tiwari**, O.-M. Midtgård, and T. M. Undeland, "Design of low inductive busbar for fast switching SiC modules verified by 3D FEM calculations and laboratory measurements," in *IEEE 17th Workshop on Control and Modeling for Power Electronics (COMPEL)*, Trondheim, 2016, pp. 1-8.

C5. **S. Tiwari**, T. M. Undeland, and O.-M. Midtgård, "An insight into geometry and orientation of capacitors for high-speed power circuits," in *IEEE 19th Workshop on Control and Modeling for Power Electronics (COMPEL)*, Padua, 2018, pp. 1-8.

C6. **S. Tiwari**, I. Abuishmais, J. K. Langelid, R. Lund, O.-M. Midtgård, and T. M. Undeland, "Characterization of body diodes in the state-of-the-art SiC FETs -Are they good enough as freewheeling diodes?," in *18th European Conference on Power Electronics and Applications (EPE'18 ECCE-Europe)*, Riga, Latvia, 2018, pp. 1-10.

C7. **S. Tiwari**, A. Rabiei, P. Shrestha, O.-M. Midtgård, T. M. Undeland, R. Lund, and A. Gytri, "Design considerations and laboratory testing of power circuits for parallel operation of silicon carbide MOSFETs," in *17th European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe)*, Geneva, 2015, pp. 1-10.

C8. **S. Tiwari**, O.-M. Midtgård, T. M. Undeland, and R. Lund, "Experimental performance comparison of six-pack SiC MOSFET and Si IGBT modules paralleled in a half-bridge configuration for high temperature applications," in *IEEE 3rd Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Blacksburg, VA, 2015, pp. 135-140.

C9. **S. Tiwari**, O.-M. Midtgård, T. M. Undeland, and R. Lund, "Parasitic capacitances and inductances hindering utilization of the fast switching potential of SiC power modules. Simulation model verified by experiment," in *19th European Conference on Power Electronics and Applications (EPE'17 ECCE Europe)*, Warsaw, 2017, pp. P.1-P.10.

C10. **S. Tiwari**, J. K. Langelid, O.-M. Midtgård, and T. M. Undeland, "Soft switching loss measurements of a 1.2 kV SiC MOSFET module by both electrical and calorimetric methods for high frequency applications," in *19th European Conference on Power Electronics and Applications (EPE'17 ECCE Europe)*, Warsaw, 2017, pp. P.1-P.10.

C11. **S. Tiwari**, J. K. Langelid, O.-M. Midtgård, and T. M. Undeland, "Hard and soft switching losses of a SiC MOSFET module under realistic topology and loading conditions," in *19th European Conference on Power Electronics and Applications (EPE'17 ECCE Europe)*, Warsaw, 2017, pp. P.1-P.10.

1.6.3 List of tutorial presentations

T1. T. M. Undeland, S. Basu, and **S. Tiwari**, "Comparisons & Measurements on Converters using Si and SiC," *International Wide-Bandgap Power Electronics Applications Workshop SCAPE 2018*, June 10-12, 2018.

T2. S. Basu, T. M. Undeland, **S. Tiwari**, J. Kyyrä, and B. Ahmad "Designing with SiC & GaN Devices With Emphasis on EMC & Safety Considerations," *18th European Conference on Power Electronics and Applications EPE18*, Sept. 17-21, 2018.

Chapter 2

Silicon carbide power devices and key advantages and challenges

This chapter begins with a comparison of key semiconductor material properties. Following this, it primarily concentrates on silicon carbide (SiC) material and the benefits it brings to power devices and applications. Thereafter, an overview of various SiC power devices, both commercially available and currently in research, is provided. To address the scope of the thesis, this chapter further focuses upon the details of SiC MOSFET and SiC diode structures. In addition, a comparison of state-of-the-art SiC MOSFET and class-leading super junction (SJ) Si MOSFET is performed. Simultaneously, the SiC junction barrier Schottky (JBS) diode is compared with the Si diode. The central objective of the above two comparisons is to delineate what SiC devices offer compared to their Si contenders to date. Moreover, the packaging of the commercially available SiC devices is discussed. Then, the critical challenges to unleash the full potential of SiC devices are addressed. Finally, the chapter closes with a summary of the findings.

2.1 Material properties

The fundamental properties of semiconductors are addressed in this section. Of the various compound semiconductors, gallium arsenide (GaAs), gallium nitride (GaN) and silicon carbide (SiC) are the most promising candidates. Table 2.1 highlights some of the key material properties of the above mentioned compound semiconductors and the currently well-established and matured technology, silicon (Si) [31]. As can be seen, GaAs exhibits

Table 2.1: Key material properties of Si, GaAs, SiC and GaN [14, 31].

Material properties	Si	GaAs	4H-SiC	2H-GaN
Bandgap energy, E_g (eV)	1.1	1.4	3.2	3.4
Breakdown electric field, E_{crit} (MV/cm)	0.3	0.4	3.5	5
Electron mobility, μ_n (cm^2/V·s)	1500	8500	900	900-2000
Hole mobility, μ_p (cm^2/V·s)	480	400	120	1600
Electron saturation velocity, v_{sat} (cm/s) $\times$ 10^7	1.0	2.0	2.2	2.5
Thermal conductivity, λ_{th} (W/cm·K)	1.5	0.5	5	1.3
Dielectric constant, ϵ	11.9	13.1	10	8.9

the highest electron mobility (μ_n) and the lowest thermal conductivity (λ_{th}) amongst all. GaN and SiC have a remarkably wider bandgap compared to Si and GaAs, and are referred as wide-bandgap (WBG) semiconductors. Notable are the higher breakdown electric field (E_{crit}), higher μ_n and higher electron saturation drift velocity (v_{sat}) of GaN compared to SiC, which favor development of higher frequency and higher voltage devices compared to those with SiC. However, due to the lack of good quality bulk substrates needed for vertical devices and the low thermal conductivity, GaN is mainly foreseeable as covering low-voltage applications, SiC, on the other hand, is best suited to covering high-voltage areas [14]. The remainder of the chapter deals only with SiC versus Si as GaN and GaAs are not in the scope of this thesis.

2.2 Fundamentals and potential advantages of SiC

This section addresses the fundamentals of SiC and describes how their physical properties benefit power devices and converters.

2.2.1 Fundamental properties of SiC

SiC is a compound semiconductor composed of elements from group IV of the periodic table. It is made up of equal parts of Si and carbon (C) with the highly covalent nature of crystalline bonds raising the resistance to dislocation glide. Therefore, it is one of the hardest materials in nature [32]. As can be seen from Table 2.1, the bandgap energy, E_g, is 3.2 eV, which is three times greater than that of Si. Wider bandgap is attributable to the larger amount of energy required for an electron to jump from the top of the valence band to the bottom of the conduction band [33]. The most common way to pack the SiC is in hexagonal fashion, in crystallographic term, called hexagonal close packing. Larger wafers can be made with 4H and 6H structures so that they are attractive for device production. In particular, the 4H poly-type possesses higher electron mobility compared to 6H type (450 $cm^2/V \cdot s$), this leads to power devices with a higher switching speed, and which are particularly suitable for vertical devices. This is the reason why all commercial SiC power devices are made of 4H structures. It is worth noting that 4H indicates four layers before repeating and H represents a hexagonal structure in 4H-SiC, as specified in Table 2.1. Stronger bonds, higher radiation resistance and chemical inertness are amongst the other key properties of SiC compared to Si, which leads to a wide range of applications where wear and corrosion resistance are primary performance requirements. Currently, 150 mm or 6 inch SiC wafers are commercially available [34]

2.2.2 Potential advantages of SiC

This section explains how different material properties of SiC can be translated to develop better power devices compared to Si. Moreover, the key applications benefiting from these devices are described. Before going into detail, it is important to know that there are certain features that a better semiconductor switching device should exhibit. For instance, during the on-state, the on-state voltage drop or forward voltage drop and on-state resistance should be as low as possible to reduce the conduction losses. Simultaneously, it should be capable of conducting sufficiently high currents. During the off-state, the power semiconductor should provide an adequate blocking voltage capability to ensure

safe operation. Moreover, the switching losses should be minimal. Minimal degradation effects and capable of handling high irradiation levels are among other important factors. Fig. 2.1 summarizes the key advantages of SiC power devices for different applications, the details of which are explained in the following paragraphs.

First, SiC offers a ten times higher breakdown electric field compared to Si, allowing the use of thinner and shorter drift layers with higher doping concentration, yielding lower specific on-resistance and junction capacitances at the same blocking voltage. Consequently, SiC power devices with higher voltage capability, and lower conduction and switching (faster switching speed) losses are achieved [35]. Second, with three times higher saturation electron drift velocity of SiC compared to Si, minority carriers are swept out of the depletion region faster during the turn-off transient, which further leads to an increased switching speed of SiC devices. Both of these aforementioned features of SiC enable the viability of **high switching frequency**, which can lead to better dynamics and reduced filter and passive components. SiC MOSFETs are now already commercially available from 650 V to 1.7 kV demonstrating the potential to replace Si IGBTs in the applications, such as solar photovoltaic (PV), hybrid or electric vehicle (H/EV), telecommunication and process heating.

Moreover, considerable research is taking place regarding 10–20 kV SiC devices. When these devices are available, **medium- and high-voltage** applications will have a simplified topology, reducing the number and size of active and passive components, and eventually leading to higher density, higher reliability and lower cost. Applications, for instance, wind power, more- and all-electric ships, more- and all-electric aircraft, in which space and weight savings are valuable, could greatly benefit from the use of SiC. Another interesting high-voltage application would be transformer-less intelligent power stations [36, 37]. In addition, using 10–20 kV SiC devices in a medium-frequency power converter, the large, heavy, line frequency classical power transformer can be replaced by a smaller, lighter, high-frequency solid-state-transformer (SST). SST is important in smart grid, traction drive, renewable energy systems, among others [37–40].

Bandgap energy and thermal conductivity of SiC are roughly three times larger than

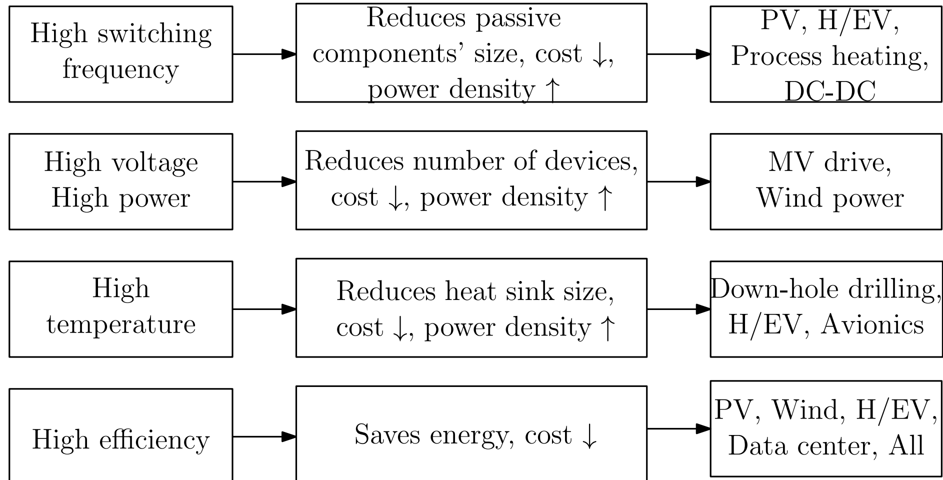


Figure 2.1: Key applications benefiting from SiC power devices.

that of Si. The former results in a remarkably lower concentration of intrinsic carriers at any given temperature [35],[1] enabling the SiC devices to operate at a higher junction temperature. In addition, wider bandgap empowers the device to exhibit lower leakage current in the blocking mode because the carriers need higher energy to cross the greater energy gap. The latter translates into reduced thermal resistance and improved heat extraction from the device. As a result, cooling requirements are reduced, and thereby high power density can be acquired. For the oil and gas industry, **high-temperature** electronics are essential for deep-well drilling application. Ambient temperatures in such deep oil wells can reach over 200 °C, which is far beyond the limits of the current Si devices [2]. Further transportation electrification, especially the aerospace and automotive industries demands high-temperature electronics [43]. Thus, WBG power electronics is greatly attractive for applications requiring high-temperature and high-power simultaneously. Once the high-temperature packaging technology and ancillary components are sufficiently developed WBG plays a critical role in realizing such applications.

2.3 Overview of SiC power devices

Most of the devices available with Si are also made with SiC; some are commercially available products and some are in research. Fig. 2.2 shows an overview of SiC power devices divided into two main groups: diodes and switches. The function of the first group is to control the direction of current flow, while that of the second group is to regulate the duration of current flow. Moreover, each group has unipolar (U) components, where the current conduction is governed only by the majority carriers (electrons); and bipolar (B) components, where both the majority and minority (holes) carriers are involved in the current conduction.

2.3.1 SiC power diodes

Essentially, SiC power diodes can be classified into three types: SiC Schottky barrier diodes (SBDs); SiC PiN diodes; and SiC junction barrier Schottky (JBS) diodes, also called merged PN-Schottky diodes (MPS). The SiC SBD was commercially introduced by Infineon Technologies and Wolfspeed Inc. (formerly Cree Inc.) in 2001 and 2002, respectively [44]. Initially, these diodes have primarily been used in high-end applications like servers or telecom power supplies because of their high cost. Subsequently, they were introduced in performance-driven applications, such as solar PV. Lately, because of the availability and cost reduction, other applications such as industrial motor drives use SiC JBS diodes as anti-parallel diodes in IGBTs or MOSFETs to handle the current in the reverse direction.

[1] What is the theoretical high-temperature limit of SiC compared to Si? When the intrinsic carrier concentration, η_i, becomes $> 10^{15}$ cm^{-3} (a typical doping concentration), the semiconductor behaves as a bulk resistor (intrinsic conduction starts) and fails to operate in a normal semiconductor fashion. Using relation $\eta_i = C \cdot e^{\frac{-E_g}{2kT}}$ [35], it can be derived that 4H-SiC does not approach this critical η_i until temperatures exceed 1000 °C while the boundary for Si is 247 °C. Consequently, the wide-bandgap is the reason that SiC power semiconductors can potentially be operated at much higher junction temperatures than power semiconductors made of Si [35, 41, 42].

[2] When the ambient temperature is above 200 °C, self-heating in high-power Si devices entails high internal junction temperatures and leakages.

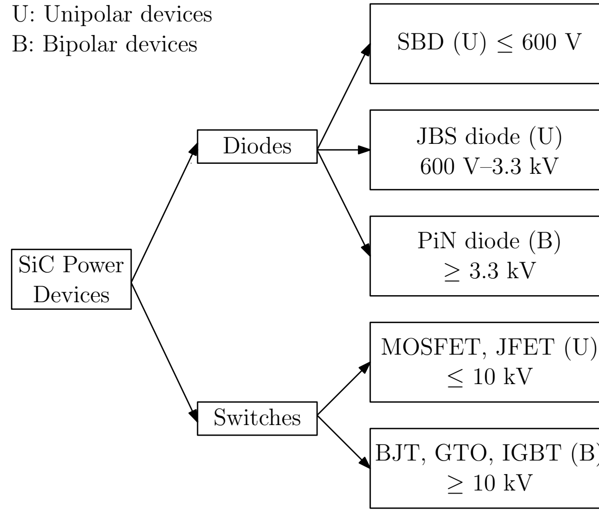


Figure 2.2: An overview of SiC power devices.

2.3.1.1 SiC Schottky barrier diode

Schottky barrier diodes (SBDs) are unipolar devices. In SBD, the forward voltage drop is determined by the metal semiconductor barrier height plus the resistance imposed by the drift layer and the substrate. However, as the temperature increases, the Schottky barrier height lowers, leading to an increase in the reverse leakage current [45]; thus the blocking voltage of commercially available SiC SBD is limited to 600 V. In order to further improve the static performance of the Schottky diode (reduce forward voltage drop), and reduce the leakage current, the SiC trench SBD is under development [46, 47].

2.3.1.2 SiC PiN diode

A SiC PiN diode is a bipolar device and has lower drift resistance; acquired via conductivity modulation, and lower reverse leakage current compared to SiC SBD. However, it has higher knee voltage $\approx$ 3 V, determined by SiC material; i.e., SiC has a wider bandgap energy ($\approx$ 3 eV) compared to Si ($\approx$ 1.2 eV). Additionally, it suffers from significant reverse-recovery current at turn-off as the drift region stored charges need to be removed. This is essentially undesirable because it causes additional turn-on loss in the active switch. Thus, the 4H-SiC PiN diode is attractive when the blocking voltage is higher than 3.3 kV. At 10–20 kV ratings, SiC PiN diode offers the best trade-off between on-state voltage drop, switching loss and high-temperature performance compared with Si PiN and SiC JBS diodes [48].

2.3.1.3 SiC Junction barrier Schottky diode

A junction barrier Schottky (JBS) diode (hybrid diode) combines SBD-like on-state and switching characteristics and PiN-like blocking characteristics. This diode is also often referred to as a merged PiN Schottky (MPS) diode. However, this concept was first demonstrated in Si in 1983 [49]. Thus far, SiC JBS diodes are commercially available

with the maximum voltage and current ratings of 1.7 kV and 100 A per die at room temperature and are anticipated to cover the voltage range up to 3.3 kV.

2.3.2 SiC switches

To date, low-voltage (up to 1.7 kV ratings) MOSFETs, JFETs, and BJTs (also called SJTs, super junction transistors) are the most common commercially available SiC switches, while high-voltage MOSFETs, JFETs, BJTs, IGBTs, GTOs and ETOs are available as engineering samples for research purposes. The following sections outline only the transistors' part as thyristors (GTOs, ETOs) are not in the scope of the thesis.

2.3.2.1 SiC MOSFET

At low-voltage, < 200 V, vertical diffused Si MOSFETs (VDMOSFET) possess low conduction losses, are capable of switching extremely fast and carrying a high current. As the blocking voltage increases, the drift region (epilayer) thickness increases. As a consequence, the on-state resistance increases significantly, and, thus, the current carrying capacity of Si MOSFET has to be reduced to limit the on-state power dissipation [1]. This is the reason why VDMOSFETs are not available with high blocking voltage. The emergence of the super junction MOSFET (SJ-MOSFET, also called CoolMOS by Infineon Technologies) technologies enabled Si unipolar transistors to compete up to 900 V.

Alternatively, the remarkably lower drift region resistance in SiC allows the development of power MOSFETs with higher breakdown voltages and smaller conduction losses. The first SiC power double diffusion MOSFET [3] (DMOSFET) was introduced in 1996 [50]. Since then different devices have been designed, characterized and studied, aiming to improve their performance. In 2010, the first power SiC DMOSFET was commercialized by Wolfspeed Inc., which was a vertical device with a planar gate. SiC MOSFETs are the highly-developed devices thus far. As it is both voltage controlled and normally-off, it is the most preferable power switch. Currently, these devices are available at different rated voltages from 650 V to 1.7 kV. With VDMOS structure, the maximum available current rating per chip at 25 °C is 90 A (25 mΩ, C2M0025120D from Wolfspeed) and with UMOS structure[4], it is 118 A (17 mΩ, SCT3017AL from Rohm). Currently, Rohm and Infineon Technologies manufacture SiC MOSFET based on trench technology. SiC MOSFETs up to 15 kV have been reported so far [51–53]. New high-voltage (>3.3 kV) third generation SiC MOSFETs from Wolfspeed are demonstrated with short-circuit currents up to 13 μs [54]. Primarily, there have been three reliability related challenges associated with SiC MOSFET. The first concerns threshold voltage stability of SiC MOSFET, i.e., positive shift with positive gate bias and negative shift with negative gate bias [55]. The second relates to the bipolar degradation of body-diode in SiC MOSFET, i.e., positive shifts in forward voltage of body-diode and on-state loss of SiC MOSFET [56, 57]. The final concerns to the gate-oxide reliability, particularly on the long term operations, high-temperatures and short circuit conditions [58–60]. All of these issues have been experimentally verified to be within the safe limit for new-generation SiC MOSFETs [56, 61–63].

[3] Double diffusion MOS (DMOS): the name is taken from the fabrication technique that involves double diffusion through the same opening: first to create the P region and second for the N source.

[4] Double trench, gate and source trench MOSFET is called UMOS: the name of the structure comes from the U-shapes of the trenches.

2.3.2.2 SiC JFET

The first commercialized SiC JFET was a lateral channel JFET (LCJFET) from SiCED (Infineon Technologies). This SiC JFET is a normally-on device. One of the key advantages of this device was the easiness for implementation because there were no reliability issues with gate-oxide as that with SiC MOSFETs. In fact, there is no surface conduction path to gate. The second commercially available SiC JFET was the vertical trench JFET (VTJFET), released by SemiSouth Laboratories in 2008. The SiC VTJFET can be produced either as a normally-on (depletion-mode vertical trench JFET, DMVTJFET) or as a normally-off (enhancement-mode vertical trench JFET, EMVTJFET) type. DMVTJFET and EMVTJFET, that is, normally-on and normally-off characteristic is determined by regulating the vertical channel thickness and the doping levels of the structures. Since a gate-source voltage has to be applied to stop conduction, the normally-on JFET requires additional protection circuitry to prevent short circuiting of DC-bus in case of the potential gate signals failure. This is the reason why the normally-on JFET is not the preferred option from an application standpoint.

Presently, United Silicon carbide Inc. produces vertical channel JFETs, including normally-on, normally-off and cascode types. A cascode configuration comprises of a normally-on SiC JFET and a series-connected low-voltage Si MOSFET. This solution overcomes the normally-on problem and makes a normally-on JFET behave similarly to a classical MOSFET. As low-voltage Si MOSFET has a relatively higher threshold voltage compared to that of SiC MOSFET, the cascode configuration is regarded as being safer from an application viewpoint. Moreover, an off-the-shelf Si MOSFET driver can be adopted for driving cascode JFET. However, the high-temperature potential of SiC JFET is limited by a co-packed Si MOSFET. Currently, these devices are available at different rated voltages from 650 V to 1.2 kV. SiC JFETs with 6.5 kV have been reported thus far [64].

2.3.2.3 SiC BJT

Si-based BJT does not favor high-voltage applications for a number of reasons. First, the current gain (β: the ratio of collector current to the base current) was low in Si BJT, which produced high driving losses. For higher current ratings, the gain would be reduced, and thus the losses would increase. Second, minority carrier injection slowed down Si BJT and caused higher switching losses, which, in turn, generated high dynamic resistance within the device. Third, the BJTs experienced the following reliability issues. (a) Current crowding created high-temperature filaments in the forward-biased mode, which eventually led to device failure. (b) Electrical field stress could be stretched beyond the drift region due to the voltage and current stresses during the inductive load switching, which could result in reverse-biased breakdown. Accordingly, stringent limits were placed on the Reverse Safe Operation area (RSOA) of the Si BJTs. This indicates that they did not have short-circuit capability [65].

The implementation of BJTs in SiC, on the other hand, revived this technology because the wider bandgap of SiC enabled higher current gain and thereby minimized the driving losses and improved the efficiency. SiC BJTs were less susceptible to thermal runaway, which is attributed to the higher breakdown field of SiC. As a consequence, reliability was greatly increased [65]. The key characterizing parameters that should be accounted for while choosing SiC BJT are: β, also called common-emitter gain; the spe-

cific on-resistance, and the open-base breakdown voltage, BV_{CEO} [66]. SiC BJT has been profoundly investigated, designed, and fabricated by TranSiC. As low current gain has been the main challenge in SiC BJT, considerable work has been done to improve the device performance in this regard: (a) Optimization of surface passivation for reducing the surface recombination current. (b) Increasing of minority carrier lifetime in the base and emitter regions [67]. (c) Darlington pair connection of SiC BJT. SiC BJTs from 100 V to 1.7 kV are commercially available today [68]. Table 2.2 lists some of the reported SiC BJTs in the literature by different groups. The highest value of β that has been reported so far is 335 for a SiC BJT with 600 V [69]. Likewise, the maximum BV_{CEO} for a SiC BJT was reported to be 6 kV exhibiting specific on-resistance of 28 m$\Omega \cdot$ cm^2 in [70][5], however, the β was 3. There is extensive research ongoing with the goal of achieving higher BV_{CEO} without sacrificing the β of the transistor.

Table 2.2: A list of reported SiC BJTs.

Current gain (β)	$R_{DS,on-spec}$ (m$\Omega \cdot$ cm^2)	BV_{CEO} (kV)	$V_B^2/R_{DS,on-spec}$ (MW/cm^2)	Group	Year	Ref.
34	35	4	457	RPI + ARL + Cree	2006	[71]
3	28	6	1272	IR + GE + RPI	2007	[70]
28	130	10	769	Cree + ARL	2010	[72]
75	110	10	909	GeneSiC	2015	[73]
139	534	15	421	KTH	2018	[74]

Note: The variables used in Table 2.2 are: current gain, β; specific on-resistance, $R_{DS,on-spec}$; and open-base breakdown voltage, BV_{CEO} or V_B. The abbreviations are: Rensselaer Polytech Institute (RPI), Army Research Lab (ARL), International Rectifier (IR) and General Electric (GE).

2.3.2.4 SiC IGBT

Because of the conductivity modulation, Si IGBT has lower on-state losses than high-voltage Si MOSFET, but it experiences a slow switching speed due to the minority carrier injection and thus suffers from high switching losses. Currently, medium- and high-voltage converters predominantly use Si IGBTs, and Si injection enhanced gate transistor (IEGTs)[6]. These devices are well-established, have proven reliability and ruggedness and are available with a blocking voltage of typically 6.5 kV or less. Today, multilevel converter topologies or series connection of these devices are considered in high-voltage applications. The former solution requires complex control, while the latter raises the voltage imbalance issues. Worth noting is the maximum junction temperature of these devices, which is typically in the range of 125–150 °C.

Significant research is taking place in the development of both p-type and n-type IGBTs. Table 2.3 lists some of the reported SiC IGBTs up to 20 kV ratings [75–77]. In general, SiC n-channel IGBTs have a higher switching speed than SiC p-channel ones. This is primarily due to a higher mobility of electrons than holes in 4H-SiC, a factor of 7.5

[5]SiC BJT has extremely low on-state losses, which are in the order of SiC unipolar devices. This is principally because the two built-in pn-junctions (even number of pn-junctions) cancel each other out; hence the on-state losses are principally determined by the drift layer resistance and the substrate resistance.

[6]IEGT has IGBT-like structure with deep trench gates and wider cell widths. Hole concentration in the P layer is enhanced for lowering the on-state voltage, specially in high-voltage devices.

times higher, as listed in Table 2.1. The fabrication of a SiC n-channel IGBT, however, starts on a p-type SiC substrate, which is greatly resistive compared to an n-type one. As a consequence, the former type is anticipated to exhibit a relatively high specific on-state resistance compared to the latter one. Other challenges regarding the high-voltage SiC IGBTs are the stability of the gate-oxide layer and the parameter degradation due to the stacking faults.

Table 2.3: A list of reported SiC IGBTs.

SiC IGBT types	$R_{DS,on-spec}$ (m$\Omega \cdot$ cm^2)	BV_{CEO} (kV)	$V_B^2/R_{DS,on-spec}$ (MW/cm^2)	Group	Year	Ref.
p-IGBT	18	12	8000	DRAPA + Cree	2008	[78]
n-IGBT	22	13	7681	Cree	2009	[79]
p-IGBT	130	20	3076	Purdue	2009	[80]

Note: The variables used in Table 2.3 are: specific on-resistance, $R_{DS,on-spec}$; and open-base breakdown voltage, BV_{CEO} or V_B. The abbreviation is: Defence Advanced Research Projects Agency (DRAPA).

2.4 Comparison of SiC MOSFETs/SiC diodes with Si MOSFETs/Si diodes

As this thesis aims for an evaluation of the latest generations of SiC MOSFETs and SiC diodes, the focus here onwards will primarily be on these devices.

2.4.1 Structures of MOSFET

Before exploring the details of state-of-the-art MOSFET devices, it is vital to briefly consider their structures and the purposes behind them. Overall, there are three major structures of MOSFET: vertical diffused MOS (VDMOS) structure, UMOS structure (also called trench-MOS structure), and super junction (SJ) structure. The total on-resistance, $R_{DS,on}$, consists of the sum of the channel resistance, the JFET resistance and the substrate resistance. In low-voltage devices, the channel-resistance is the predominant, while in high-voltage devices, the drift resistance is the dominant resistive component [56]. As the blocking voltage of Si MOSFETs exceeds 200 V, $R_{DS,on}$ increases. To cope with this challenge, other structures, such as the UMOS structure, where the gate electrode is buried in a trench and the SJ structure, where a charge compensation principle is used, have been introduced. The former structure provides the potential to reduce the channel resistance and eliminate the JFET resistance, which makes the trench MOSFET very attractive for the lower voltage ratings [56]. The latter structure minimizes the drift layer resistance. Fig. 2.3 shows the structures of SiC MOSFET with planar versus trench technology [46, 47].

2.4.2 Comparison of SiC MOSFETs with Si MOSFETs

Table 2.4 compares the most significant parameters, in particular, the maximum breakdown voltage (V_{DS}), current (I_D), on-state resistance ($R_{DS,on}$), internal gate resistance ($R_{g,int}$), total gate charge (Q_g), gate-drain charge (Q_{gd}), input capacitance (C_{iss}), output

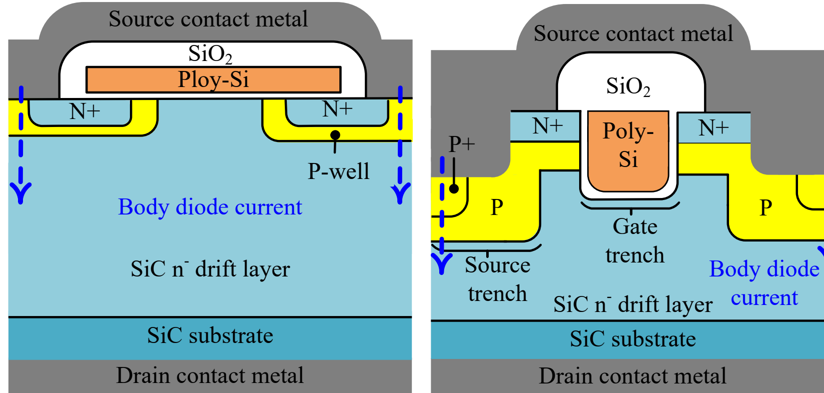


Figure 2.3: Structures of planar (left) and double-trench, gate-source-trench (right), MOSFETs. Note that trench structures improve the static performances in MOSFETs [46, 47].

Table 2.4: Comparison of key parameters for Si versus SiC MOSFETs in TO247 package.

Manufacturer	Wolfspeed (Planar) (SiC MOSFET)		Infineon (Super Junction) (Si MOSFET-CoolMOS)	
Data sheet	[81]	[82]	[83]	[84]
Device	C2M0040120D	C3M0065090D	IPW60R045CP	IPW90R120C3
V_{DS} (V)	1200	900	650	900
I_D (A)	60 @25 °C 40 @100 °C	36 @25 °C 23 @100 °C	60 @25 °C 38 @100 °C	36 @25 °C 23 @100 °C
$R_{DS,on}$ (mΩ)	40 @25 °C 84 @150 °C	65 @25 °C 90 @150 °C	40 @25 °C 110 @150 °C	120 @25 °C 270 @150 °C
$R_{g,int}$ (Ω)	1.8	4.7	1.3	0.9
Q_g (nC)	115 @800 V	30 @400 V	150 @400 V	270 @400 V
Q_{gd}(nC)	37 @800 V	12 @400 V	51 @400 V	115 @400 V
C_{iss}(pF)	1893 @1000V	660 @600	6800 @400	6800 @100
C_{oss}(pF)	150 @1000V	60 @600	220 @400	330 @100
C_{rss}(pF)	10 @1000V	4 @600	9.4 @400	-
$R_{th,jc}$(°C/W)	0.34	1	0.29	0.3

Note: All data are from manufacturer's data sheet.

capacitance (C_{oss}), Miller capacitance (C_{rss}), and thermal resistance from junction to case ($R_{th,jc}$), based on both Si and SiC. As seen in Table 2.4, the SJ MOSFET (referred as CoolMOS by Infineon Technologies), IPW60R045CPA, has relatively low $R_{DS,on}$ (in the same order as the planar SiC MOSFET, C2M0040120D) at 25 °C. Nonetheless, this parameter increases by 175% at 150 °C compared to that at 25 °C. This result indicates that when using the Si MOSFET, the efficiency will degrade substantially when the junction temperature is high, which will limit the power density and the operating frequency of the converter.

When this research is conducted, Rohm and Infineon Technologies are only manufacturers of SiC MOSFET based on trench technology. From the data sheet of the same chip size devices (SCT2080KE, planar, versus SCT3040KL, trench), a 50% reduction in

$R_{DS,on}$ and a 35% reduction in C_{iss} are achieved by switching the technology from the planar to the trench type [85]. As per $R_{DS,on}$, SCT3017AL and SCT3022KL with trench structures are the most interesting DUT candidates today. Note that the $R_{g,int}$ of the MOSFET depends on the sheet resistance of the gate electrode material and the chip size. Specifically, $R_{g,int}$ is inversely proportional to the chip size [85]. The chip size of the SiC MOSFET is smaller than that of the Si MOSFET, leading to a larger $R_{g,int}$ and a smaller gate capacitance in SiC, provided that the ratings are the same, which can be explicitly seen from the comparison shown in Table 2.4. Note that a higher value of $R_{g,int}$ limits the switching speed of the SiC MOSFET. It should be mentioned that a trade-off exists between the conduction and switching losses for a device. A device with a larger die size (A) exhibits reduced conduction loss ($R_{DS,on} \sim 1/\mathrm{A}$), but leads to increased switching loss ($C_{iss} \sim \mathrm{A}$).

2.4.3 Structures of diode

There are basically two types of diodes: the PiN diode and the Schottky diode. This thesis centers on the Schottky type only. Fig. 2.4 shows the two major structures of the Schottky diode, namely, planar and trench.

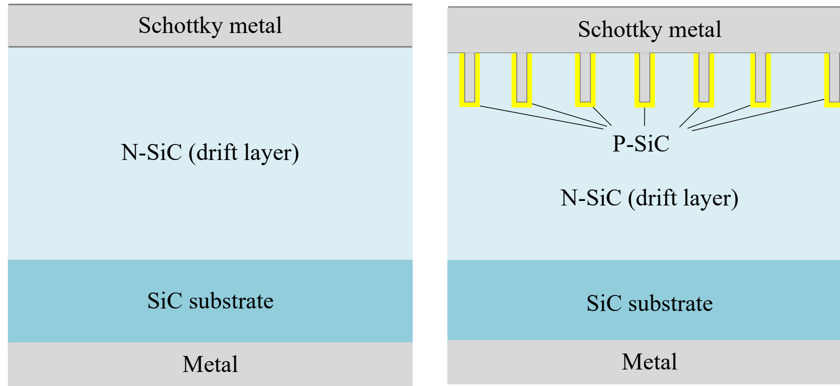


Figure 2.4: Structures of planar (left) and trench (right) SBD.

2.4.4 Comparison of SiC diodes with Si diodes

Table 2.5 documents the key electrical parameters, including the maximum breakdown voltage (V_{DS}), forward current (I_F), forward voltage drop (V_F), reverse-recovery charge of a Si diode (Q_{rr}), and capacitive charge of a SiC diode (Q_c), for state-of-the-art diodes, based on both Si and SiC with two different voltage ratings: 650 V and 1200 V. In particular, V_F and Q_{rr} or Q_c are desired to be the lowest to achieve the highest efficiency. Schottky barrier diodes exhibit both of these features compared to other diode technologies, for instance, the fast recovery epitaxial diode (FRED) [88, 89]. Nevertheless, the narrow bandgap of Si limits its use to a maximum voltage of approximately 200 V, i.e., Si SBDs that operate above 200 V have higher V_F and Q_{rr}.

Before the advent of SiC Schottky diodes, bipolar pn-junction FREDs were the only solutions for applications requiring diodes with blocking voltages in excess of 200 V. It is

Table 2.5: Comparison of key parameters for Si- versus SiC Schottky diodes in TO247 package.

Manufacturer	ROHM (Planar) (SiC JBS diode)		Vishay (FRED PT) (Si diode)	IXYS (FRED) (Si diode)
Data sheet	[86]	[87]	[88]	[89]
Device	SCS220AE2	SCS220KE2	VS-EPH3007L-N3	DSEI30-12A
V_{DS} (V)	650	1200	650	1200
I_F (A)	20 @135 °C	20 @145 °C	30 @100 °C	30 @100 °C
V_F (V)	1.35 @25 °C 1.55 @150 °C	1.4 @25 °C 1.8 @125 °C	1.8 @25 °C 1.4 @150 °C	2.55 @25 °C 2.2 @150 °C
Q_{rr}/ Q_c (nC)	30 @400 V	68 @800 V	1350 @400 V, 125 °C	3000 @540 V, 100 °C
$R_{th,jc}$ (°C/W)	0.8	0.45	0.7	0.25

Note: All data are from manufacturer's data sheet.

worth mentioning that SiC SBDs or SiC JBS diodes maintain a constant recovery charge regardless of temperature and forward current, but this charge significantly increases in the similar rating Si FRED [90]. There are two main explanations for this behavior. First, SiC SBDs and SiC JBS diodes are majority carrier devices, and there is no minority carrier injection as in the Si FRED. Second, SiC has a significantly smaller chip size compared to Si, and, consequently, little or no charge storage mechanism exists in SiC. As seen in Table 2.5, the Q_{rr} of Si diodes also contains information about the temperature, but this information is not provided for SiC diodes because the Q_c of SiC is temperature independent. Another interesting observation from Table 2.5 is that the V_F in Si FRED has a negative temperate coefficient, whereas the opposite is true in SiC JBS diodes. In Si FREDs, as the temperature rises, the Fermi level moves, and, then, the barrier height lowers, leading to a decrease in V_F. In contrast, in SiC JBS diodes, as the temperature increases, the lattice vibration increases and the mobility decreases, resulting in higher resistance [45].

2.5 Packaging

This section provides a brief overview of the commercially available packages of SiC devices. Low-power discrete SiC devices are available in different packages, such as TO247-3, TO247-4, TO263-7. All of these devices showed outstanding static and dynamic performance compared to their Si contenders. It is obvious that the chip size determines the current rating of a device; however, the low yield of SiC wafer and thermal mechanical stress restrict the device area. As a consequence the current capability of a single chip is limited. Therefore, for high current power modules, multiple chips are paralleled to form a single switch. Several features, including electrical connections, thermal conduction to heat sink, electrical insulation, and mechanical support are contained in a standard power module package. This consists of a chip, wire bond, solder, Cu, Ceramic, Cu, (Cu-Ceramic-Cu is often called DBC, direct bonded copper substrate) solder, baseplate, thermal grease and heat sink or cold plate arranged from top to bottom. Al_2O_3, AlN, Si_3N_4 are the most common ceramic materials. DBC substrate conducts the heat generated by the chip to the cooling system and provides an insulation layer between the chip

Table 2.6: Commercially available SiC modules and their package inductance.

Manufacturer	L_{module} (nH)	Remarks
Wolfspeed-45 mm	30	Standard module
Wolfspeed-62 mm	15	Standard module
Wolfspeed-62 mm	5	High performance
Sanrex	15	Solder bonding
Rohm type C	25	Standard module
Vincotech	7	Additional low-inductive current path

and the baseplate. Wire bond functions as the electrical connection between the top side of one chip and the other chips [91].

Table 2.6 lists the commercially available power module packages with their internal inductances. They are packaged in similar standard module packages as those used for Si devices. Wire bond interconnection is used in all of them except in Sanrex module, where a solder bond technique is employed. At high power level, the dynamic performance of SiC devices is limited by the parasitics in the module housing, as well as in the external busbar and gate drive circuitry. This is primarily a result of the parasitics becoming alive with higher dv/dt and di/dt.

To bridge the gap between SiC devices and their applications, manufacturers have started to look into improved and advanced packaging techniques. One example is the module from Vincotech, which uses a separate RC (resistance and capacitance) loop close to the power module, apart from the main DC-link capacitor. The former is active during switching when di/dt is high. The capacitor is realized via PCB or foil [26]. Another example is the Semikron SKiN technology introduced in 2011 for Si IGBTs, where all soldering and bonding connections of standard power module designs are replaced by silver diffusion sintering joints; i.e., the thin flexible layer takes over the function of bond wires. This resulted in a significant reduction in commutation inductance (3.2 nH) [25].

2.6 Critical thinking or challenges

Critical thinking is indispensable whenever new devices come onto the market. Here, some of the key challenges associated in unlocking the full-potential offered by SiC are discussed.

First, SiC allows fast switching speed enabling extremely high ($>$ 200 kHz) switching frequencies in SMPS applications (in the kW range). However, its **dynamic performance is hindered by the parasitics** in the transistor casing and in the external busbar and gate drive circuitry. Furthermore, various phenomena like parasitic ringings and electromagnetic interference (EMI) are augmented as dv/dt and di/dt increase. Thus, significant research efforts are ongoing regarding low-inductive packaging and busbar design as reported in [25–28, 92–97].

Second, although the physics of SiC permit maximum junction temperatures well above 200 °C, constraints are placed on other parts of the system, such as **high-temperature packaging technology**. Numerous research projects have been conducted in this direction and some interesting examples of these can be found in [95, 96, 98].

Third, SiC is an emerging technology, **special gate drivers** that are fast enough

to operate gates in the nanoseconds range (high charge and discharge pulse current) are required for switching the devices to their fast-switching potential. Further, unique gate drive voltages are needed as per the device technology. For instance, manufacturers recommend +20 V/-5 V gate voltages for most of the SiC MOSFETs [81,99], while third-generation SiC MOSFET from Wolfspeed requires +15 V/-4 V [82]. Similarly, Infineon Technologies recommend selecting lower limit of turn-off voltage depending on the turn-on voltage in their trench MOSFETs [100]. This aims in keeping the drift in gate-threshold voltage within the acceptable limits. There has been a wealth of discussion and research in the direction of gate driver design suitable for a high-temperature and high-frequency environment, some of which are reported in [101–106].

Finally, SiC is not only a part in a converter, the neighbouring components should also be able to sustain the same environment without deteriorating the mechanical, electrical, thermal and electromagnetic properties. Currently, **the availability of such ancillary components**, such as capacitors and inductors, capable of living in the same environment as SiC, is a serious impediment for harvesting the benefits offered by SiC. In addition, the insulation requirement when a single-device blocking voltage is in the tens of kilovolts should also be borne in mind. Therefore, advancements in semiconductors should go hand in hand with the complementing bodies. To overcome some of these challenges, a similar concept as used in Si technology, referred to as an intelligent power module (IPM), where the drive and protection circuitry are integrated along with a semiconductor [107], is being leveraged in SiC. SiC-based IPMs [108, 109], optimized gate drives for the commercial SiC modules [110, 111] are already released. Other efforts in this direction are reported in [101, 112–114].

Thus, to develop converters with unprecedented efficiency and power density, the next landmark would be the integration of passives, WBG semiconductors, gate driver, control, protection, communication and thermal management to the extent it makes meaning [112,115,116]. Texas instruments and Vicor have lunched several such products [115,116], for instance, 10 kW, three-phase AC to 48 V converter power-on-package solution was introduced by Vicor in 2018 [117].

2.7 Summary

This chapter started with a comparison of material properties of the most interesting semiconductors. With the special attention directed to the SiC devices, the chapter discussed various SiC devices that are commercially available and in research along with the benefits and challenges associated with each of them. Next, particular focus was paid to SiC MOSFETs and SiC diodes, together with the detailed comparison of state-of-the-art SiC versus Si devices and the packages they come with. Finally, the challenges in adopting this technology were addressed.

Chapter 3

Prerequisites for accurate assessment of switching loss by electrical method

The information presented in this chapter is based on publications J2 and C11, the main aim of which is to answer the following research questions.

Q 1. What are the prerequisites for accurate assessment of switching losses of SiC devices?

Q 2. Can the electrical loss measurement via a widely accepted double-pulse test (DPT) methodology with inductive clamped load be used for estimating the losses that occur in a resonant (sine wave current) inverter?

3.1 Introduction

The results of this work are primarily based on laboratory experiments. This chapter is divided into two parts. The first part concerns the provisos for evaluating the switching performance of SiC devices, which covers appropriate probes and oscilloscope for accurately tracking the fast switching transients of these devices. Following this, the low-inductive connection techniques and characteristics of load which are imperative for capturing the true switching waveforms of device under test (DUT) are exemplified. Finally, the importance of accuracy in post processing of the measured data is included.

The second part, on the other hand, is related to the significance of realistic topology for an accurate assessment of switching losses, where a widely accepted DPT methodology is employed. For representing the hard-switched application, a clamped inductive load is used, while for portraying the resonant-switched application, split DC-link capacitors with series connection of inductance and capacitance (LC) as load are used. Comparison of the turn-off loss measured between these two configurations revealed that the resonant (sine wave current) switching technique achieved considerably lower losses compared to the hard (square wave current) switching operation. Thus, this chapter primarily recommends using an appropriate circuit topology for the correct assessment of switching loss. Apart from reducing switching losses, the resonant inverter topology also entailed in mitigating the oscillations, which can subsequently alleviate electromagnetic interference (EMI). Based on this outcome, the author suggests adopting the sine wave switching technique whenever possible (as per the application).

3.2 Prerequisites for accurate measurement of high-speed switching signals

3.2.1 Bandwidth of measuring probes and oscilloscope

In order to capture the fast rising and falling current and voltage signals of switching devices, the probes and oscilloscope should have adequate bandwidth (BW) or rise time (t_{rise}) and fall time (t_{fall}). If not, the harmonics which are above the cut-off frequency of probe will be filtered out and the measured di/dt and dv/dt will be lower than the real slopes leading to inaccurate results. In [118], it is recommended to have five times greater BW of the probe and oscilloscope compared to the frequency of the waveform being measured. Moreover, it is also suggested that, for accurately tracking t_{rise} and t_{fall} of the waveform, the BW of equipment should satisfy the relation given by (3.1). As an illustration, Fig. 3.1 is presented where the t_{rise} of drain-source voltage (V_{ds}) is 20 ns for an external gate resistance ($R_{g,ext}$) of 0 Ω. Based on (3.1), BW is computed to be 87.5 MHz, indicating that the oscilloscope and probes with higher BW than 87.5 MHz are of sufficient quality to track the transient waveforms of that particular device. In addition, frequency of oscillations (f_{osc}) is measured to be 30 MHz, therefore, 150 MHz of BW is enough for tracking these oscillations. It is worth mentioning that the oscilloscope is calibrated in order to adjust its parameters according to surrounding environmental conditions, such as temperature, pressure, and humidity, each time the measurement is taken.

$$BW = 5 \cdot \frac{0.35}{t_{rise}\ [ns]} = 5 \cdot \frac{0.35}{20} = 87.5 \text{ MHz} \tag{3.1}$$

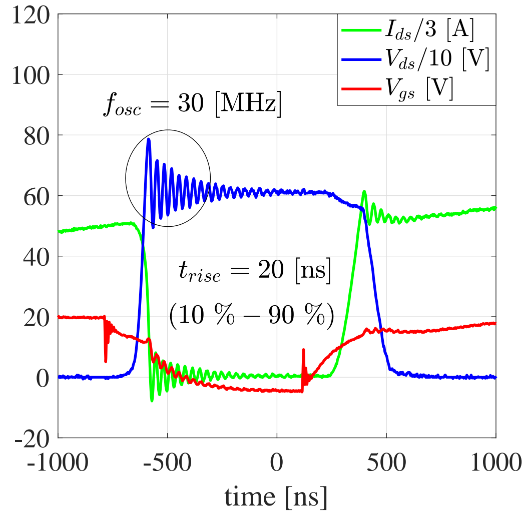


Figure 3.1: For $R_{g,ext} = 0$ Ω, the t_{rise} and t_{fall} are in the range of 20 ns and the ringing frequency (f_{osc}) is 30 MHz, thus the probes and oscilloscope bandwidth of ≥ 150 MHz are adequate for tracking these switching transients. The legends used in Fig. 3.1 are: V_{ds}, drain-source voltage; I_{ds}, drain-source current; and V_{gs}, gate-source voltage.

3.2.1.1 Voltage measurement

High BW and sufficient dynamic range are two important requirements of voltage probes. Table 3.1 summarizes the probes considered in this work. Passive probes are used for measuring low-side V_{gs} and V_{ds} in the phase-leg configuration. Differential probes are used for high-side V_{gs} and V_{ds} measurements because they also have galvanic isolation, while the passive probes do not. Moreover, common mode (CM) input voltage range and CM rejection ratio are also critical for high-side voltage measurements. All of these probes have their own propagation delays and have to be individually dealt with while computing the switching losses. Furthermore, the voltage probes are compensated to adjust their capacitances according to the input capacitance of the oscilloscope channel.

Table 3.1: Data sheet readings of voltage measurement probes used in the thesis.

Types	Models	Max. voltage	Bandwidth	Rise time[1]	Delay
Differential probe	THDPO200	± 1500 V	200 MHz	8.75 ns	14 ns
Passive probe	P5100A	2500 V	500 MHz	3.50 ns	6.1 ns
	TPP1000	750 V	1000 MHz	1.75 ns	5.67 ns

[1]Rise-time is calculated based on (3.1) with five times margin (i.e., 5 × 0.35/Bandwidth).

3.2.1.2 Current measurement

Current measurement techniques, such as coaxial shunt, split-core current probe, and Rogowski coil are adopted in this thesis, the specifications of which are summarized in Table 3.2. All of these probes have their own pros and cons. Although the Rogowski coil features galvanic isolation, and can be easily connected to the device, it has limitations regarding the BW and DC-component measurement. Therefore, it is not sufficiently accurate for measuring the high-speed switching current. The coaxial shunt, on the other hand, has high BW and high accuracy, but does not feature galvanic isolation. Moreover, it cannot be used for measuring current in continuous operation.

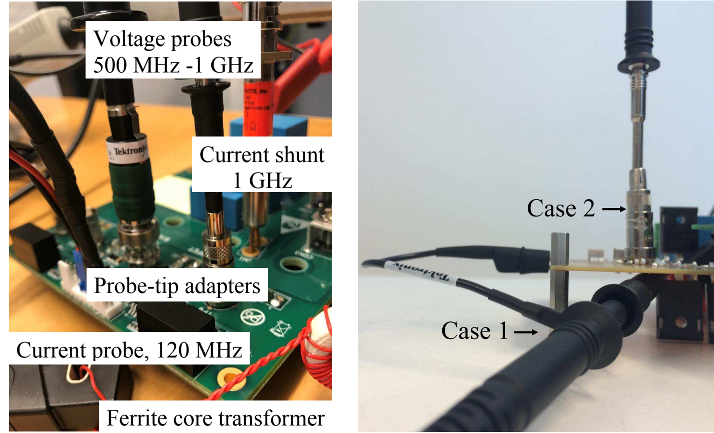
Table 3.2: Current measurement techniques and their specifications as per data sheet.

Types	Models	Current type	Bandwidth	Rise time[1]
Coaxial shunt	SDN - 25, 250 $m\Omega$	dc/ac	1000 MHz	1.75 ns
	SSDN - 414 - 01, 10 $m\Omega$	dc/ac	400 MHz	4.37 ns
Split-core	TCP0030A	dc/ac	120 MHz	14.58 ns
Rogowski coil	CWT6B	ac	30 MHz	58.3 ns

[1]Rise-time is calculated based on (3.1) with five times margin (i.e., 5 × 0.35/Bandwidth).

3.2.2 Low-inductive measurement connections

Ground-lead inductance is another factor impacting the measurement accuracy of switching waveforms, as discussed in [118, 119], because the typical ground-lead associated with the voltage probe has an inductance and forms a series-resonant network with the input capacitance of the probe. Therefore, a PCB probe-tip adapter is employed in order to reduce the ground-lead inductance, as shown in Fig. 3.2 (a) and (b).



(a) Probe-tip adapters connections. (b) Ground-lead of a voltage probe.

Figure 3.2: (a) Laboratory setup showing the arrangement for low-inductive connections for current and voltage measurements of the device under test. The current is measured by a high-bandwidth, low-inductive current shunt, and the voltage is measured by a high-bandwidth single-ended probe with probe-tip adapter as displayed. (b) Illustration of a typical ground-lead of a voltage probe (Case 1) versus probe-tip adapter connection (Case 2). Load current is measured by a dc/ac current probe out of a 40-turn ferrite core transformer.

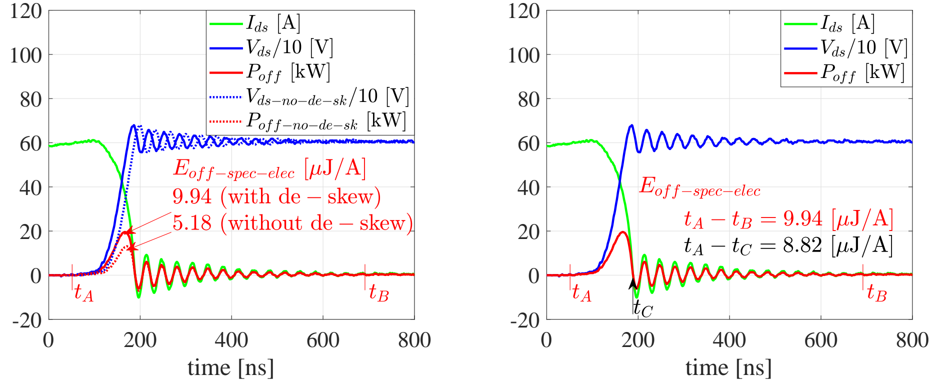
3.2.3 Load inductor characteristics

Two single-layer winding air core inductors are connected in series as an inductive load. The air core avoids saturation, single-layer winding provides small stray capacitance (C_L), and the series connection further reduces C_L, and subsequently the true switching waveforms of the DUT are reflected. The equivalent C_L of the load inductor is measured by an impedance analyzer, E4990, and is found to be 1 pF.

3.2.4 Post processing of measured data

3.2.4.1 De-skewing of voltage probes

Generally, the data sheet of the voltage probe provides information about probe delay, which is 14 ns for the selected probe. In order to analyze the influence of the probe delay on the accuracy of measurement, the voltage waveform is de-skewed, i.e., subtracting the probe delay from the originally measured voltage waveform, as shown in Fig. 3.3 (a). The originally measured voltage waveform is in dotted blue and the one with de-skewed is indicated by solid blue. As the current waveform is measured by a shunt resistor, there is no need to de-skew the current waveform. Thereafter, the current and voltage waveforms are multiplied to obtain the power loss indicated by the dotted red line for the original and the solid red line for the de-skewed. Then, the switching energy loss is calculated for the case with and without probe de-skew. With the former, the specific energy loss ($E_{off-spec-elec}$) is computed to be 9.94 μJ/A, whereas the same with the latter is calculated to be 5.18 μJ/A; lower by a factor of 1.91.



(a) Turn-off event with and without probe de-skew. (b) Turn-off event with different integration time.

Figure 3.3: Turn-off transients during hard-switching together with the power waveforms. Fig. (a) illustrates the influence of probe delay. With 14 ns of voltage probe delay with respect to current measured by shunt, there is a significant difference in the computed energy loss. Fig. (b) exposes the influence of integration limits on the power curve. Given that there are oscillations, the choice of the end of the integration time is not clear. t_A denotes the start of the integration time, while t_B and t_C are two options to select the end of the integration time.

3.2.4.2 Choosing the time interval for power integration

The selection of an appropriate time interval is crucial for integrating the measured power in order to extract the correct switching energy loss, an example of which is illustrated in Fig. 3.3 (b). Both current and voltage waveforms exhibit oscillations at the end of each switching transient and so do the power curves possessed. There are two possible integration time limits. The first is the initial zero crossing of power curve, indicated by t_C, the second is t_B, where the low and high-frequency oscillations have decayed. While integrating the power waveform from t_A to t_B, $E_{off-spec-elec}$ is computed to be 9.94 μJ/A, whereas when integrating the power waveform from t_A to t_C, the same is computed to be 8.82 μJ/A; lower by 11.26%. In this work, the former integration limit where all the oscillations are decayed is considered.

3.3 Importance of realistic circuits for loss evaluation

In this section, the significance of using an appropriate inverter topology for the correct assessment of the switching loss is investigated. Two different topologies studied involve a half-bridge inductive clamped load without split DC-link capacitors, which has a square wave output current; and a half-bridge series-resonant inverter with split DC-link capacitors and an LC load, which has a sine wave output current. For realizing a low switching loop stray inductance, the DC-link is made with a planar busbar, except for the termination parts needed to facilitate the module connection. A current viewing resistor (CVR), also called a shunt resistor, SSDN-414-01 (400 MHz, 10 mΩ) from T & M research, is used for measuring the drain current. The CVR is mounted directly on one of the screw terminals of the SiC MOSFET module, as illustrated in Fig. 3.4.

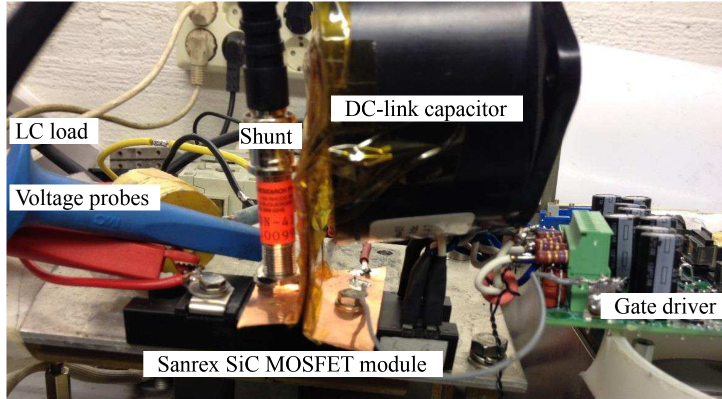
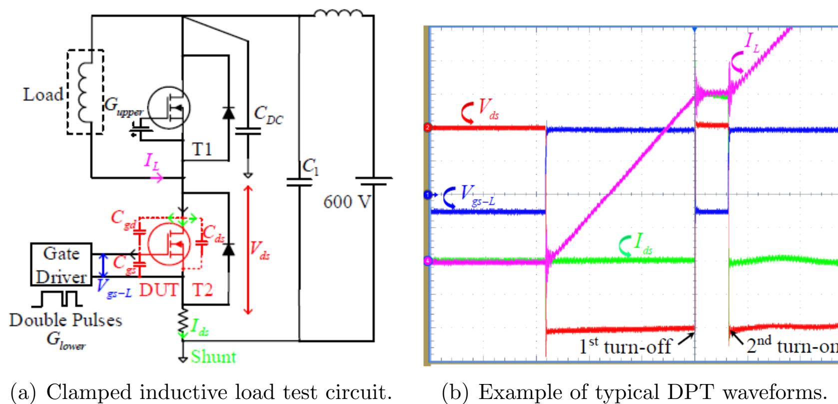


Figure 3.4: Laboratory setup with a low-inductive DC-link. The drain-source current is measured by a high-bandwidth, low-inductive shunt, and the drain voltage is measured by a high-bandwidth differential probe.

3.3.1 Hard-switched topology

Fig. 3.5 (a) shows a schematic diagram of a hard-switched inverter topology, where a lower transistor (T2) is used to switch a diode-clamped inductive load, primarily as a step-down DC-DC converter. An example of a DPT waveform is shown in Fig. 3.5 (b), where the main areas of concern are marked as the first turn-off event and the second turn-on event. For accessing the stress in the DUT, two pulses are sent, while the gate-source of an upper transistor (T1) is supplied with -5 V to ensure that it is turned off all the time. Fig. 3.5 (b) displays the typical DPT waveforms, where the first turn-off (at the end of the first pulse) and the second turn-on (at the beginning of the second pulse) are the key points of interest because the DUT switching transients can be captured under similar voltage and current conditions. The gate-source voltage (V_{gs-L}), the V_{ds}, the I_{ds} of transistor T2, and the current through the load inductor (I_L) are indicated in Fig. 3.5 (a)



(a) Clamped inductive load test circuit.

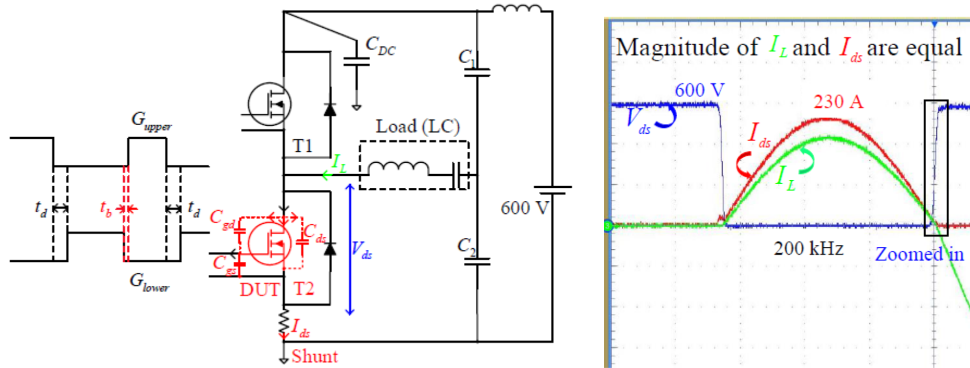
(b) Example of typical DPT waveforms.

Figure 3.5: Illustration of a circuit diagram for hard-switching loss measurement, and an example of a typical double-pulse test waveform.

and (b). The remaining abbreviations used in Fig. 3.5 are as follows. G_{upper} and G_{lower}: upper and lower gate pulses respectively, and C_{DC}: DC-link capacitance.

3.3.2 Resonant inverter topology

Fig. 3.6 (a) depicts a half-bridge resonant circuit with split DC-link capacitors and LC load for measuring soft-switching losses. The upper transistor (T1) is always in the on-state except for the period where the lower transistor (T2) is in the on-state, including some blanking time (t_b) and delay time (t_d). t_b refers to the time interval between the turn-off and turn-on switching of the transistors of the same leg. By adjusting the turn-on time, the switching current can be varied according to the value of interest. Noteworthy are the shapes of the V_{ds} and the I_L, which are square and sine waves, respectively, replicating those present in a real application circuit.

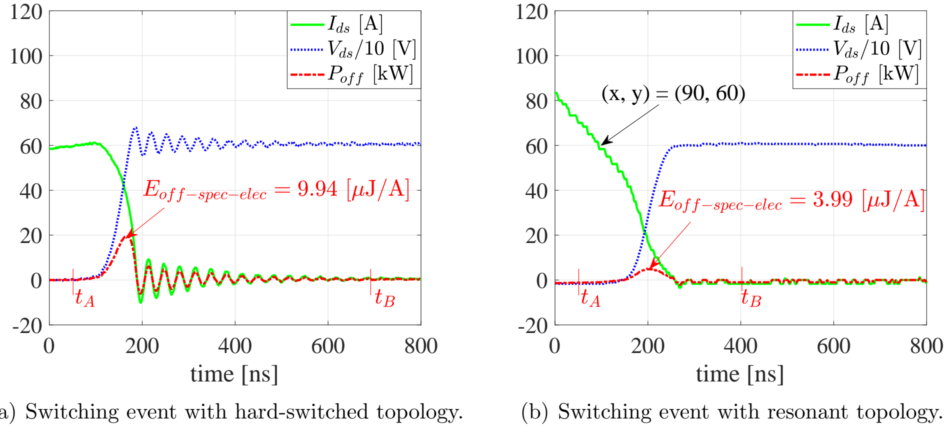


(a) Configuration with split DC-link capacitors and LC load. (b) Typical soft switched waveforms.

Figure 3.6: Illustration of a circuit diagram for series-resonant inverter topology, where a lower transistor (T2) is the DUT and the load is formed by a series inductor and capacitor in (a), and an example of a typical output waveform, where the turn-off instant is the key point of interest and is annotated by a rectangle in (b).

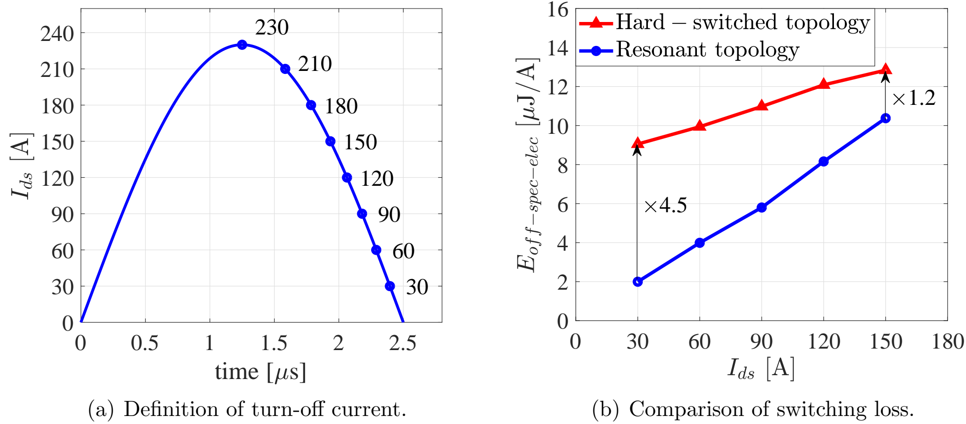
3.3.3 Experimental results for hard versus resonant topology

Fig. 3.7 shows example waveforms illustrating the difference between hard-switching and resonant switching. For a fair comparison, these waveforms are recorded at the same I_L (60 A), $R_{g,ext}$ (2.85 Ω) and V_{gs} (+ 20 V, - 5 V). It is clearly visible that the sinusoidal switching waveforms have lower ringing compared to those of the square wave switching. While comparing the switching losses, it is important to show how they are computed. Hence, in this work, the turn-off power (P_{off}) curve is integrated from t_A to t_B, as indicated in Fig. 3.7 (a) and (b), and the $E_{off-spec-elec}$ per switch are found to be 3.99 μJ/A for sine wave switching and 9.94 μJ/A for square wave switching at I_L of 60 A. In order to ensure a comprehensive overview of switching losses at different current levels with the two different topologies, the $E_{off-spec-elec}$ versus drain-source current is plotted in Fig. 3.8 (b).



(a) Switching event with hard-switched topology. (b) Switching event with resonant topology.

Figure 3.7: (a) Illustration of turn-off transients under hard versus resonant topology at the same load current. The former exhibits oscillations, while oscillations are absent in the latter. Specifically, the turn-off energy loss is 2.5 times lower for resonant topology than that of the hard-switched inverter, showing the ample benefit of the latter topology.



(a) Definition of turn-off current. (b) Comparison of switching loss.

Figure 3.8: (a) Illustration of the turn-off current in the resonant switching case. The peak value of the load current is set at 230 A, and the turn-off instants are varied. (b) Comparison of the switching loss between the hard (square wave current) and soft/resonant (sine wave current) switching. Switching with square wave current leads to higher turn-off losses, a factor of 1.2 (150 A) to 4.5 (30 A) depending on the load current, compared to that with sine wave current.

It is worth mentioning that, in either of the topologies, the required turn-off current level is acquired by adjusting the on-time and the DC-link voltage. To be more precise regarding the resonant switching, the peak value of the load current is fixed at 230 A, and, thereafter, the turn-off instants are varied (by adjusting the on-time), as defined in Fig. 3.8 (a). Aside from this, the switching frequency is set to 200 kHz according to the application requirements. Depending on I_{ds}, $E_{off-spec-elec}$ varies from 2 to 10.8 μJ/A

with the resonant topology and from 9 to 12.8 μJ/A with the hard-switched topology.

Thus, using the hard-switching loss for designing thermal management and estimating the power rating of the resonant inverter leads to a significant error, as the turn-off switching in the latter occurs at the minimum possible current (lower current regions). The difference in losses between the two topologies is more pronounced towards the lower currents, primarily for two reasons. First, at lower current, there is lower dv/dt, which causes the output capacitance of the MOSFET to work more effectively as a turn-off snubber compared to a higher current. Second, the MOSFET channel is closed to the current earlier in the turn-off process with lower dv/dt.

3.4 Summary

This chapter centred on accessing the true switching waveforms as in a real-world inverter circuit, and can be summarized as follows:

1. First a half-bridge configuration, a basic cell or a part of many topologies is considered for study, so that all the parasitics are involved during the switching events. Key issues impacting the high-speed measurements are discussed, and the measures for accurately tracking the fast switching transients and evaluating the switching losses by electrical method, such as selection of voltage probes, current probes, and oscilloscope with adequate BW; probe-tip adapter for minimizing connection inductances; adjustments of probe de-skew and possible post-processing errors are highlighted.

2. Keeping the gate driver stray inductance, resistance, voltage and location the same in hard versus resonant inverter topologies, the turn-off switching losses are compared. Measured results revealed that the resonant (sine wave current) switching technique causes remarkably lower loss compared to the hard (square wave current) switching operation, a factor of 2.5 times lower at 60 A. Thus, the author has two key recommendations.

    i. First, adopt resonant switching whenever feasible (as per the application) because this minimizes the switching losses and oscillations.

    ii. Second, consider an appropriate circuit topology for the correct assessment of switching loss, especially for a resonant inverter, where the turn-off is aimed towards the lower current region. Otherwise, estimation of loss for a sine wave switched inverter using the measurements from the hard-switched topology leads to significantly higher errors at lower currents compared to higher currents. This difference potentially entails considerable error in estimating the power rating of the inverter and sizing of the heat sink, and will be more pronounced, particularly at high switching frequency.

Chapter 4

Characterization of state-of-the-art SiC MOSFET modules

The information presented in this chapter is based on publications C1, C2, C3 and C9, the main aim of which is to answer the following research questions.

Q 1. How fast do state-of-the-art SiC MOSFET modules (those packaged in standard plastic housings) switch? How does the parasitic inductance and capacitance impact switching performance of SiC devices?

Q 2. How will the switching performances of high-voltage SiC MOSFETs differ from those of low-voltage types?

Q 3. How does the switching performance of SiC MOSFET modules differ with the class-leading IGBT modules?

4.1 Introduction

A number of publications have previously examined the switching performance of discrete SiC MOSFETs [120, 121] and SiC MOSFET modules [122]. A few of these have also compared high-voltage (15 kV) SiC MOSFET modules with SiC IGBT modules (15 kV) under similar dv/dt conditions [16]. Manufacturers are continuously improving the quality of these devices and new-generation types are available. However, none of them have compared SiC MOSFET modules against each other from the parasitic perspective nor have they compared them under a series of different conditions such as similar dv/dt per chip size, similar di/dt per chip size, similar voltage overshoot and similar current overshoot. This work extends the research in this regard. Apart from exploring the impact of stray inductance and stray capacitance in switching of these devices by means of both experiments and Spice simulations, this chapter also provides ideas on how the high-voltage SiC MOSFETs characterize compared to their low-voltage counterparts. Most importantly, the main objective of this work is to answer how fast the state-of-the-art commercially available SiC MOSFET modules switch compared to the leading-edge Si IGBT modules.

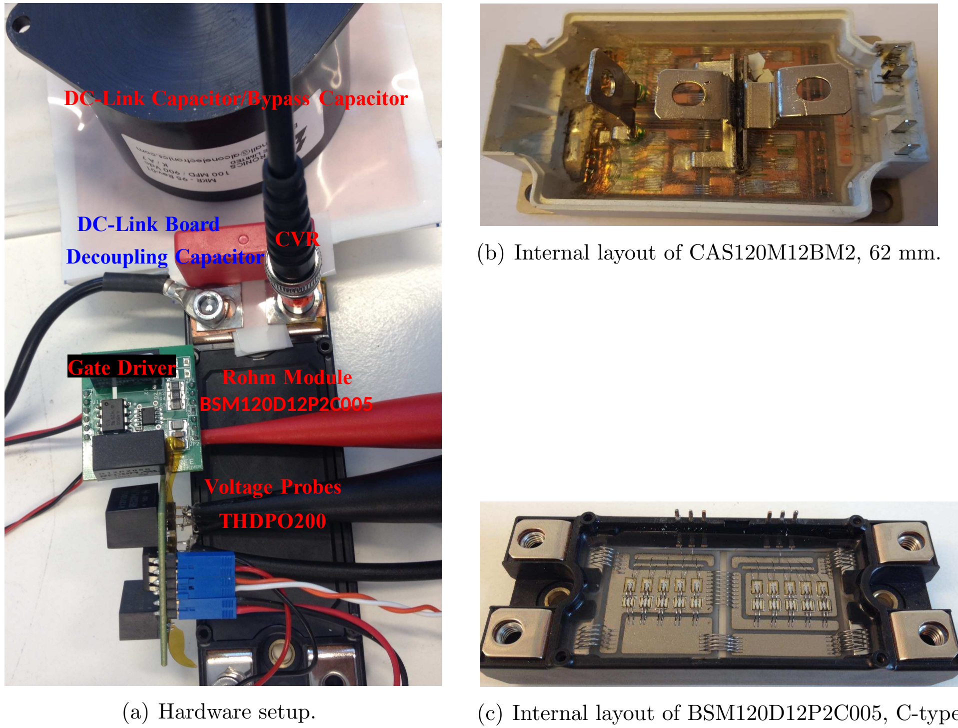
4.2 Comparison of SiC MOSFET modules

This section evaluates two sets of the state-of-the-art SiC MOSFET modules packaged in standard plastic housings. The first set has different internal stray inductance (L_{module}) and the second set has different internal stray capacitance (C_{stray} due to chip not via layout). This way, the impact of L_{module} and C_{stray} in the switching performance can be studied, thus the selection of these modules is a deliberate choice. The primary goal of the comparison is to address the first research question. A standard double pulse test (DPT) methodology is used for evaluating the stresses in these devices. A simulation model is developed in LTSpice for regenerating the laboratory results and providing further support to analyze the experimental results.

4.2.1 Modules with different stray inductance

4.2.1.1 Hardware setup and device under study

Fig. 4.1 shows photographs of the hardware setup and SiC MOSFET modules.



(a) Hardware setup.

(b) Internal layout of CAS120M12BM2, 62 mm.

(c) Internal layout of BSM120D12P2C005, C-type.

Figure 4.1: (a) Hardware setup showing a planar busbar, placement of current viewing resistor (CVR) instead of a screw, several parallel capacitors in the DC-link to reduce stray inductance associated with bypass capacitor and their connections (L_{byp}), and to realize an overall low stray inductance (L_{stray}) in the switching loop. (b) and (c) Pictures showing the internal layouts of two different modules under study.

To evaluate the true switching performance of these devices, the DC-link is realized with a planar busbar except the termination parts (needed to facilitate the module connection) so that the stray inductance in the switching loop can be kept as low as possible. A current viewing resistor (CVR) SSDN-414-01 (400 MHz, 10 mΩ) from T & M research is used for measuring the drain-source current (I_{ds}). The CVR replaces one of the screws in the SiC module as it is mounted directly on the screw terminal. This arrangement decreases the L_{stray} even further as one screw hole is eliminated. A picture illustrating the placement of the CVR in the laboratory setup is provided in Fig. 4.1. A detailed sketch for insertion of CVR between the busbar and the module is depicted in Fig. 4.2. The stray inductance of the bussing structure is calculated using Ansys Q3D extractor, and is 14 nH [29].

The on-state resistance ($R_{DS,on}$), the total die size, the input capacitance (C_{iss}) and the output capacitance (C_{oss}) of two different SiC MOSFET modules, from two different manufacturers, Wolfspeed and Rohm, are listed in Table 4.1 [123, 124]. Each of them has a voltage rating of 1.2 kV and a current rating of 120 A.

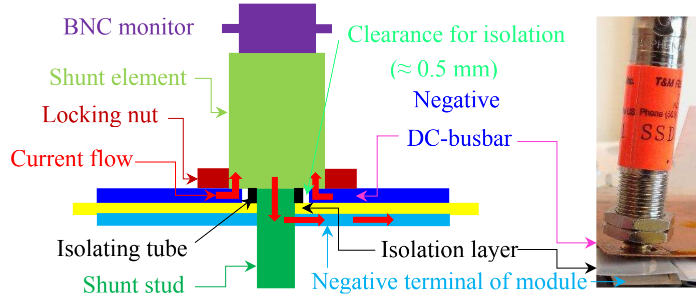


Figure 4.2: Detailed sketch of CVR insertion between the busbar and the module. A clearance of 0.5 mm is provided for shunt voltage drop on the DC-busbar.

Table 4.1: On-state resistance, total die size, C_{iss}, and C_{oss} of the modules under study.

Parts Half-bridge	$R_{DS,on}$ @25°C (mΩ)	Total die size (mm^2)	C_{iss} (nF)	C_{oss} (nF)
CAS120M12BM2 (Wolfspeed)	13	6 × 3.10 × 3.36	6.3	0.88
BSM120D12P2C005 (Rohm)	16	5 × 3.00 × 4.40	14	0.9

The variables used are: on-state resistance, $R_{DS,on}$; and input and output capacitances, C_{iss} and C_{oss}.

4.2.1.2 Experimental results

Summary of measurements with varying gate resistance: All the turn-on and turn-off switching transients are evaluated for a DC-link voltage of 600 V and a drain-source current of 120 A in each of the SiC MOSFET modules at 25 °C. Both the chosen SiC modules are evaluated with varying external gate resistance ($R_{g,ext}$). dv/dt and di/dt are measured at 50% of the drain voltage and current. A summary of the measurements taken during the experiments is provided in Table 4.2 for CAS120M12BM2 and Table 4.3 for BSM120D12P2C005. dv/dt and dv/dt^* are the voltage slew rate per module and

the voltage slew rate per chip area, respectively, during the turn-off events, while di/dt and di/dt^* are the current slew rate per module and the current slew rate per chip area, respectively, during the turn-on events. It is observed from the laboratory measurements that the variations in dv/dt with varying $R_{g,ext}$ are approximately in the same range for both modules, as shown in Table 4.2 and Table 4.3. Above all, **the comparison between the two modules shows that the highest achievable switching speed is roughly 35 V/ns and 10 A/ns with the state-of-the-art SiC modules using standard plastic packages, which provided an answer to one of the research questions.**

Table 4.2: Summary of laboratory measurements for CAS120M12BM2 (Wolfspeed, MOSFET).

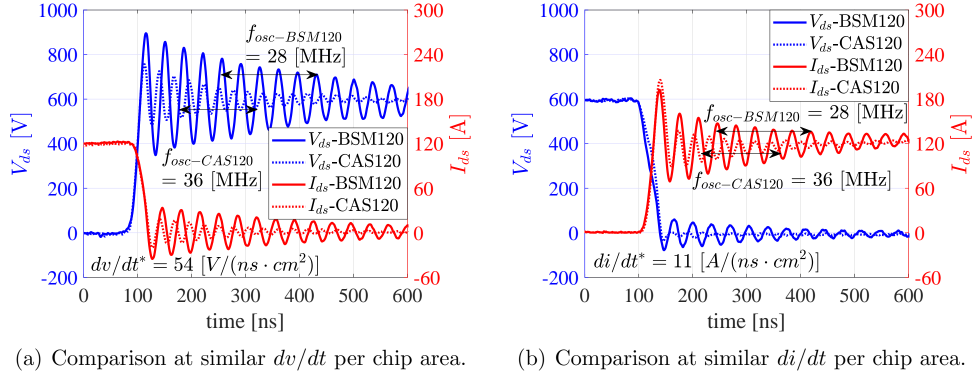
$R_{g,ext}$ (Ω)	dv/dt (V/ns)	di/dt (A/ns)	V_{os} (V)	I_{os} (A)	E_{on} (mJ)	E_{off} (mJ)	dv/dt^* (V/(ns · cm^2))	di/dt^* (A/(ns · cm^2))
0	34.2	9.8	215	134	0.52	0.53	54.7	15.6
1.95	26.3	7.3	185	101	0.76	1.17	42.0	11.6
3.9	19.7	5.9	156	79	1.46	1.62	31.5	9.4
6	14.8	5.8	139	67	2.08	1.67	23.6	9.2
10	10.4	3.5	106	45	3.10	2.52	16.6	5.6
12	9.4	3.1	90	43	3.83	2.90	15.0	4.9

Table 4.3: Summary of laboratory measurements for BSM120D12P2C005 (Rohm, MOSFET).

$R_{g,ext}$ (Ω)	dv/dt (V/ns)	di/dt (A/ns)	V_{os} (V)	I_{os} (A)	E_{on} (mJ)	E_{off} (mJ)	dv/dt^* (V/(ns · cm^2))	di/dt^* (A/(ns · cm^2))
0	35.2	7.01	295	87	0.4	1.04	53.3	10.6
1.95	23.4	3.57	264	49	2.0	1.52	35.4	5.4
3.9	17.5	2.34	212	36	3.7	1.80	26.5	3.5
6	14.26	1.92	183	31	5.0	2.17	21.6	2.9
10	10.4	1.32	147	23	7.4	3.2	15.7	2
12	9.4	1.15	135	21	8.6	3.6	14.2	1.7

Note: V_{os}, I_{os}, E_{on}, E_{off} are: voltage and current overshoots; and turn-on and turn-off energy losses.

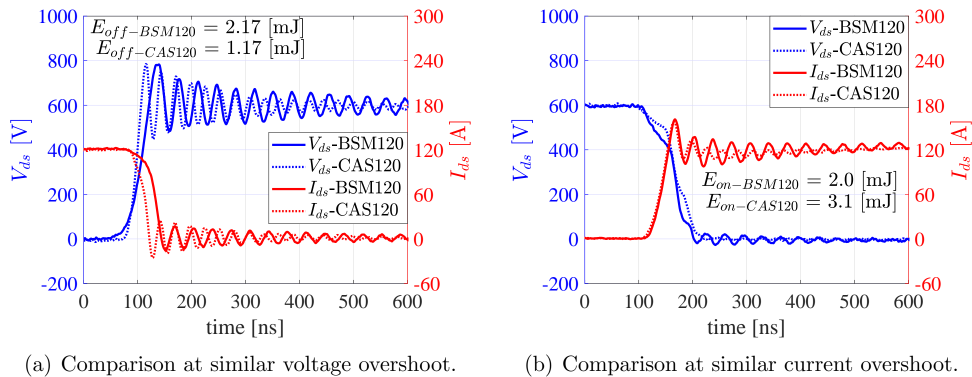
Comparison of switching at similar dv/dt and di/dt per chip area: Fig. 4.3 (a) and (b) show the measured switching transients of two different SiC MOSFET modules at similar dv/dt^* and di/dt^*, respectively. The frequency of oscillation in the Wolfspeed module is 36 MHz, while it is 28 MHz in the the Rohm module, which is indicated by f_{osc} in Fig. 4.3. The lower frequency of oscillation in the Rohm module is primarily due to higher L_{module}. Alternatively, the voltage overshoot (V_{os}) during turn-off is caused by switching loop inductance and di/dt at turn-off. L_{stray} can be estimated by, $V_{os} = L_{stray} \cdot di/dt$. As can be seen in Fig. 4.3 (a), di/dt is similar for each module, thus $V_{os} \propto L_{stray}$. Using this relation, L_{module} is computed to be 15 nH in CAS120, while it is 25.8 nH in BSM120. Moreover, as observed from Fig. 4.3 (b), dv/dt is roughly the same in each module; however, CAS120 has higher current overshoot (I_{os}) compared to BSM120, which is essentially because of higher effective junction capacitance of the MOSFETs and anti-parallel diodes in the former module. It is worth mentioning that L_{stray} oscillates with this effective capacitance.



(a) Comparison at similar dv/dt per chip area. (b) Comparison at similar di/dt per chip area.

Figure 4.3: Measurement of switching transients of two different SiC MOSFET modules at similar dv/dt per chip area during turn-off and similar di/dt per chip area during turn-on.

Comparison of switching at similar voltage and current overshoot: For comparing the cases with similar V_{os} and I_{os}, the events with the closest values are chosen from the summary provided in Table 4.2 and Table 4.3. Fig. 4.4 (a) compares the switching waveforms when these modules have similar V_{os}. The faster rising waveforms of the Wolfspeed module compared to the Rohm clearly indicate that the turn-off losses are higher in the Rohm module for this case. From laboratory measurements, the turn-off loss for Wolfspeed is 1.17 mJ and for Rohm it is 2.17 mJ, denoted by E_{off} in Fig. 4.4 (a). Thus, it is desirable to have a module with lower stray inductance, otherwise it suffers from higher turn-off switching loss. $R_{g,ext}$ of 10 Ω for Wolfspeed and 1.95 Ω for Rohm modules give almost similar I_{os}, as exemplified in Fig. 4.4 (b). Laboratory measurements show turn-on losses of 3.1 mJ for Wolfspeed and 2.0 mJ for Rohm, specified by E_{on} in Fig. 4.4 (b). Note that the stray inductance effectively works as a turn-on snubber, which is partly a reason for lower turn-on losses in the Rohm module.



(a) Comparison at similar voltage overshoot. (b) Comparison at similar current overshoot.

Figure 4.4: Measurement of switching transients of two different SiC MOSFET modules at similar voltage overshoot during turn-off and similar current overshoot during turn-on.

4.2.1.3 Analysis of impact of stray inductance by simulation in LTSpice

A simulation study is performed in a hard switching configuration, as shown in Fig. 4.5 for the Rohm MOSFET module. The aim of the simulation is to regenerate similar oscillations as in laboratory measurements and employ the model to study the influence of L_{stray}, as indicated in Fig. 4.5, in the switching transients. The simulated turn-off and turn-on switching transients for two different values of L_{stray} are shown in Fig. 4.6. With an L_{stray} of 12 nH, the frequency of oscillation is 36 MHz, while it is 28 MHz with an L_{stray} of 28 nH. V_{os} **and** I_{os} **are higher and oscillations are larger and longer with higher** L_{stray} conforming to the experimental results.

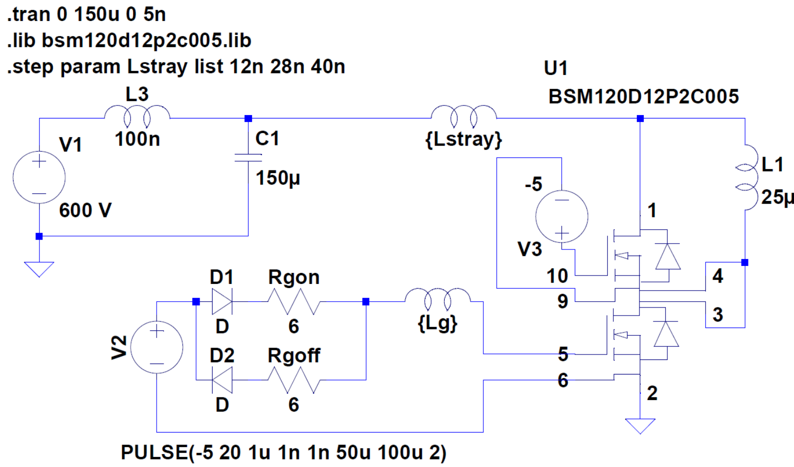
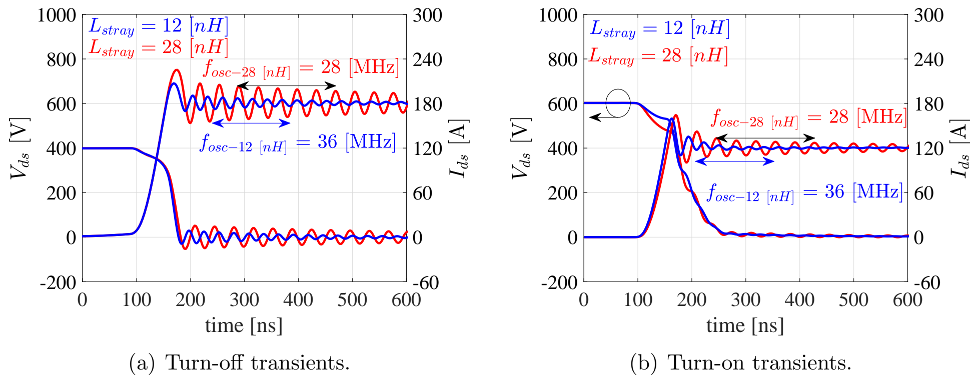


Figure 4.5: Simulation model in LTSpice for the study of impact of stray inductances.



(a) Turn-off transients.

(b) Turn-on transients.

Figure 4.6: LTSpice simulation of turn-off and turn-on switching transients with two different values of L_{stray}, provided $R_{g,ext} = 6\ \Omega$. Note that an LTSpice model of a half-bridge SiC MOSFET module, BSM120D12P2C005, is considered to investigate the effect of parasitic inductance. Clearly, the higher the L_{stray}, the higher the overshoot and the larger and longer the oscillations.

4.2.2 Modules with different stray capacitance

During the research work, it was of interest how the high-voltage SiC MOSFETs differ in switching compared to the low-voltage SiC MOSFETs. A closer look on the data sheet readings of SiC MOSFET dies with two different voltage ratings: 1.2 kV and 1.7 kV is provided in Table 4.4 [125, 126] as an example. Areas and thicknesses are different for these chips and so are the capacitances. Again, looking into the data sheet readings of two similarly rated SiC MOSFET modules in Table 4.5 [127, 128], it is clear that even the same rated devices can have different capacitances. Thus, this set of SiC MOSFET modules with 1.2 kV ratings has been evaluated in the laboratory for the sake of clarifying the issue.

Moreover, studying the impact of parasitic capacitances in the switching transients also provides an insight into the potential consequences of externally inserted parasitic capacitances, for instance: addition of a small capacitor or a voltage probe at gate-source; addition of an external anti-parallel diode across the drain-source, as it has a junction capacitance; and placement of the gate driver and module, as it can form a parallel trace between the gate and drain, and thereby form a capacitance across it.

Table 4.4: Data sheet readings of SiC MOSFET dies with different voltage ratings.

Parameters / Die	CPM2-1200-0040B	CPM2-1700-0045B
Voltage rating (kV)	1.2	1.7
Chip size (mm × mm)	3.10 × 5.90	4.08 × 7.35
Thickness (μm)	180 ± 40	380 ± 40
C_{iss} (pF) @ 1000 V	1893	3672
C_{oss} (pF) @ 1000 V	150	171
C_{rss} (pF) @ 1000 V	10	6.7

Table 4.5: Data sheet readings of SiC MOSFET modules with same voltage ratings.

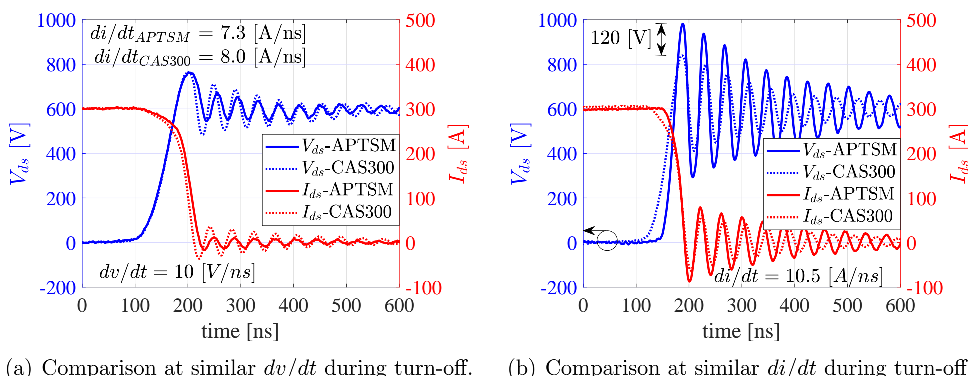
Parameters / Module	CAS300M12BM2 Wolfspeed (MOSFET)	APTSM120AM09CD3AG Microsemi (MOSFET)
Voltage rating (kV)	1.2	1.2
No. of chips × (mΩ)	6 × 25	9 × 80
C_{iss} (nF) @ 600 V	11.7	23
C_{oss} (nF) @ 600 V	2.55	1.1
C_{rss} (nF) @ 600 V	0.07	0.18
Q_c (nC) @ 600 V	3200	1080
Q_g (nC) @ 600 V	1025	1224
Q_{gd} (nC) @ 600 V	475	360
$\text{FOM}_1 = R_{DS,on} \times Q_g$	4270	10880
$\text{FOM}_2 = \sqrt{R_{DS,on} \times Q_{gd}}$	44	56

The variables used in Table 4.5 are: input capacitance, C_{iss}; output capacitance, C_{oss}; reverse transfer capacitance, C_{rss}; capacitive charge of SiC diode, Q_c; total gate charge, Q_g; and gate-drain charge, Q_{gd}. The conduction figure-of-merit, FOM_1; and the switching figure-of-merit, FOM_2 are defined in [129]. FOM_1 and FOM_2 are larger by a factor of 2.55 and 1.27, respectively, for APTSM120AM09CD3AG with regard to CAS300M12BM2. A smaller FOM indicates better device performance, i.e., lower device loss.

4.2.2.1 Experimental results

The same hardware setup as shown in Fig. 4.1 is used for examining the set of SiC MOSFET modules presented in Table 4.5.

Comparison of switching at similar dv/dt and di/dt during turn-off: Fig. 4.7 (a) illustrates the turn-off transients of two modules at similar dv/dt during turn-off. The frequency of oscillations in both the modules is approximately equal, even though the effective junction capacitance formed by the MOSFET output capacitance and junction capacitance of anti-parallel diode are smaller for Microsemi, indicating the presence of higher L_{module} in the Microsemi compared to the Wolfspeed. Furthermore, for this case, di/dt is smaller for the Microsemi (7.3 A/ns) compared to the Wolfspeed (8.0 A/ns), which is primarily influenced by two factors. First, higher L_{module}; and second, higher gate-source capacitance (C_{gs}). The simulation with varying L_{stray}, as presented in Section 4.2.1.3, supports the former reason and the latter is in accordance with the simulation presented with varying C_{gs} [see Appendix A.2.1, Fig. A.5 (c)]. Fig. 4.7 (b) compares two modules at similar di/dt during turn-off, the APTSM shows clearly higher voltage overshoot than the CAS300, further signifying the fact that the former module has higher L_{module}. It is worth mentioning that the V_{ds} of the lower side MOSFET in the half-bridge is measured across the sources of the upper and the lower MOSFETs. If it was measured across the power terminals, the oscillations would be almost invisible.



(a) Comparison at similar dv/dt during turn-off. (b) Comparison at similar di/dt during turn-off.

Figure 4.7: (a) APTSM has slightly lower di/dt compared to CAS300, indicating the presence of higher L_{module} in it. (b) At similar di/dt during turn-off, the APTSM shows noticeably higher overshoot than the CAS300, further clarifying the fact that it has higher L_{module}.

Comparison of switching at similar di/dt during turn-on: For the case with similar di/dt during turn-on, the switching signals are shown in Fig. 4.8. There are a number of reasons for the current overshoot being smaller in the APTSM compared to the CAS300: (a) Q_c of diode is 0.33 times smaller, (b) C_{iss} is 1.96 times larger, and (c) C_{ds} is 0.37 times smaller in APTSM. All of these data can be seen in Table 4.5. Simulation results with different C_{gs} and drain-source capacitance (C_{ds}); as presented in Appendix A.2.1, Fig. A.5 (d) and Appendix A.2.2, Fig. A.6 (d), respectively, further substantiate the above reasoning.

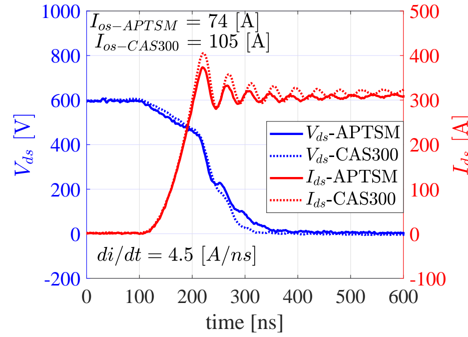
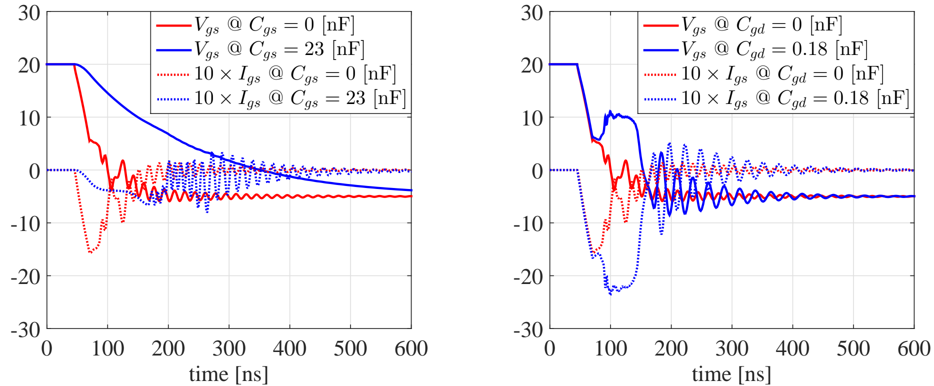


Figure 4.8: Measured turn-on transients of two modules at similar di/dt in the turn-on. Simulation results with different C_{gs} and C_{ds}, as presented in the Appendix, further confirm that the lower current overshoot in APTSM is due to smaller Q_c, smaller C_{ds} and larger C_{gs} in it compared to CAS300.

4.2.2.2 Analysis of the impact of stray capacitance by simulation in LTSpice

A simulation model is built in LTSpice for studying the impact of C_{gs}, C_{ds}, and C_{gd}. The values are chosen as per the data sheet of the chosen modules, as listed in Table 4.5. The simulated turn-off and turn-on transients of the currents and voltages in both the gate and drain sides with different C_{gs}, C_{ds}, and C_{gd} are elaborated in Appendix A.2. In particular, the comprehensive parametric study can be utilized to anticipate the relative performance differences between the devices with the same or different voltage ratings. Hence, this provides a guideline for choosing an appropriate SiC module. Fig. 4.9 (a) and (b) show the simulated turn-off signals: gate-source voltage, V_{gs}; and gate-source current, I_{gs}, with varying C_{gs} and C_{gd}; respectively. C_{gs} mainly determines the time constant of



(a) Gate signals with different C_{gs} during turn-off. (b) Gate signals with different C_{gd} during turn-off.

Figure 4.9: (a) Impact of different C_{gs} and C_{gd} on V_{gs} and I_{gs}. Higher C_{gs} leads to cleaner gate signals; whereas, higher C_{gd} results in noisier ones. Hence, higher ratio of C_{gs}/C_{gd} is preferable to avoid possible device malfunction.

gate circuit. Higher C_{gs} reduces the slew rates, mitigates the oscillations and prolongs the delay times of V_{gs}. In contrast, higher C_{gd} aggravates the oscillations. In fact, faster dv/dt of SiC MOSFET couples power circuit noise to gate side via C_{gd}. This noise can exceed the threshold voltage limit of SiC MOSFET and cause unwanted turn-on of the device. Hence, it is not only the absolute value of C_{gd} that endangers MOSFET, instead, it is more precisely related to the ratio of C_{gs}/C_{gd}. Thus, a MOSFET with higher C_{gs}/C_{gd} ratio should be chosen to avoid such a turn-on.

Thus, **the simulations and experimental results** from Section 4.2 show that the **parasitic components of power MOSFETs limit their fast dynamic performances**; i.e., these parasitics slow down SiC devices, stress them with higher current and voltage overshoots, and higher losses.

4.3 Comparison of SiC MOSFET and Si IGBT

This section has two parts. The first part compares the state-of-the-art SiC MOSFET module and modern Si non-punch-through (NPT) IGBT module under a series of different conditions, such as similar dv/dt per chip area, similar di/dt per chip area, and similar voltage and current overshoots. The second part compares further sets of DUTs, six-pack SiC MOSFET module and six-pack Si soft-punch-through (SPT) IGBT module under different loading conditions and junction temperatures. All the chosen modules are commercially available in standard plastic packages and each set has the same voltage and current ratings.

4.3.1 SiC MOSFET vs. Si non-punch-through IGBT modules

The key characterizing parameters, such as chip size, chip thickness, on-state resistance of MOSFET / IGBT ($R_{DS,on}/R_{CE,on}$), on-state resistance of diode (R_d), on-state knee voltage of IGBT (V_{CEO}) and diode (V_{FO}), C_{iss}, C_{oss}, C_{rss}, Q_c and reverse-recovery charge (Q_{rr}) of anti-parallel diodes in SiC MOSFET and Si IGBT respectively, total gate charge (Q_g) and internal gate resistance ($R_{g,int}$) are listed in Table 4.6 [127, 130]. The total die size in Si IGBT is larger by a factor of three compared to that in SiC MOSFET. In addition, Si has a slightly higher dielectric constant than SiC. Both of these factors lead to a larger capacitance in the Si IGBT compared to the SiC MOSFET module. (A dielectric constant in Si is 11.9, while it is 10 in 4H-SiC.) An electrical breakdown field ten times higher in SiC compared to Si allows for a thinner and shorter drift layer. However, the thickness of chip and area is a trade-off between the $R_{DS,on}$ and the capacitance of the power MOSFET structure.

4.3.1.1 Experimental results

The same hardware setup as shown in Fig. 4.1 is used for examining the set of SiC MOSFET and Si IGBT modules presented in Table 4.6. All the turn-on and turn-off switching transients are evaluated for a DC-link voltage of 600 V and a drain-source current of 300 A in each of the modules at 25 °C. Both the chosen modules are evaluated with varying $R_{g,ext}$.

Table 4.6: Key electrical parameters of SiC MOSFET versus Si NPT IGBT modules.

Parameters / Module	CAS300M12BM2 Wolfspeed (MOSFET)	SKM400GB125D Semikron (IGBT)
No. of chips	6	4
Chip size (mm × mm)	4.04 × 6.44	11.08 × 11.08
Thickness (μm)	200	180
$R_{DS,on}/R_{CE,on}$ (mΩ) @25°C	5	6.3
$R_{DS,on}$ (mΩ) @125°C	7.8	7.6
V_{CEO} (V) @25°C	Absent	1.4
V_{CEO} (V) @125°C	Absent	1.7
R_d (mΩ) @25°C	2.25	2.7
R_d (mΩ) @125°C	4.35	3
V_{FO} (V) @25°C	0.925	1.4
V_{FO} (V) @125°C	0.83	1.1
C_{iss} (nF) @ 600 V	11.7	22
C_{oss} (nF) @ 600 V	2.55	3.30
C_{rss} (nF) @ 600 V	0.07	1.2
Q_{rr}/Q_c (μC)	3.2	45
Q_g (nC)	1025	2650
$R_{g,int}$ (Ω)	3	1.25

The variables used in Table 4.6 are: on-state resistance of MOSFET / IGBT, $R_{DS,on}/R_{CE,on}$; on-state resistance of diode, R_d; on-state knee voltage of IGBT, V_{CEO}; on-state knee voltage of diode, V_{FO}; input capacitance, C_{iss}; output capacitance, C_{oss}; reverse transfer capacitance, C_{rss}; capacitive charge of SiC diode, Q_c; reverse-recovery charge of Si diode, Q_{rr}; total gate charge, Q_g; and internal gate resistance of semiconductor module, $R_{g,int}$.

Summary of measurements with varying gate resistances: A summary of the measurements taken during the experiments is provided in Table 4.7 for SiC MOSFET and Table 4.8 for Si IGBT. dv/dt and dv/dt^* are the voltage slew rate per module and the voltage slew rate per chip area during the turn-off events, while di/dt and di/dt^* are the current slew rate per module and current slew rate per chip area during the turn-on events.

Table 4.7: Summary of laboratory measurements for CAS300M12BM2 (Wolfspeed, MOSFET).

$R_{g,ext}$ (Ω)	dv/dt (V/ns)	di/dt (A/ns)	V_{os} (V)	I_{os} (A)	E_{on} (mJ)	E_{off} (mJ)	dv/dt^* (V/(ns · cm^2))	di/dt^* (A/(ns · cm^2))
0	19.56	10.93	301	198	1.63	3.74	12.5	6.9
1	15.12	9.14	260	166	3.87	5.04	9.6	5.8
2.2	13.22	7.1	207	140	5.02	5.76	8.4	4.5
3.4	10.38	6.56	188	125	7.09	7.7	6.6	4.2
5	8.55	5.35	136	111	8.56	8.64	5.4	3.4
6.8	7.12	4.46	133	105	11.84	10.78	4.5	2.8
10	5.4	3.5	102	86	16.61	15.16	3.4	2.2
12	4.9	2.97	85	65	19.62	17.74	3.1	1.9

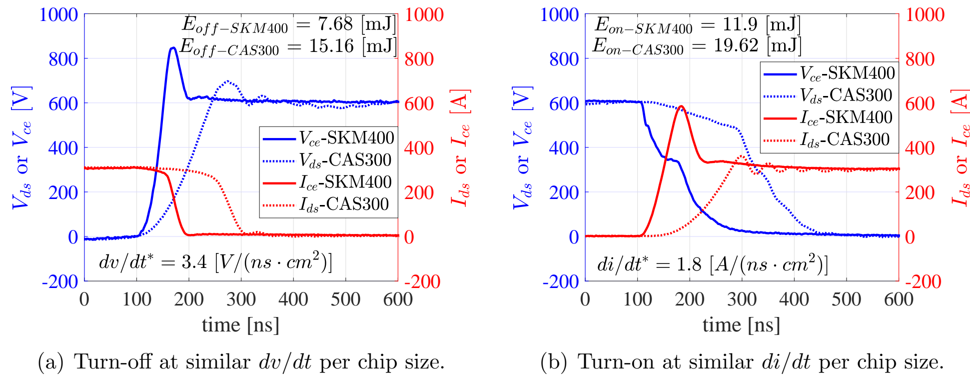
The variables in Table 4.7 are: external gate resistance, $R_{g,ext}$; voltage and current overshoot, V_{os} and I_{os}; turn-on and turn-off energy loss, E_{on} and E_{off}; dv/dt and di/dt per chip size, dv/dt^* and di/dt^*.

Table 4.8: Summary of laboratory measurements for SKM400GB125D (Semikron, IGBT).

$R_{g,ext}$ (Ω)	dv/dt (V/ns)	di/dt (A/ns)	V_{os} (V)	I_{os} (A)	E_{on} (mJ)	E_{off} (mJ)	dv/dt^* (V/(ns $\cdot$ cm^2))	di/dt^* (A/(ns $\cdot$ cm^2))
0	16.64	12.2	233	393	3.94	7.68	3.3	2.4
1	13.23	9.07	270	279	11.9	8.87	2.7	1.8
2.35	9.8	5.7	296	168	24.9	10	2.0	1.1
3.9	7.32	3.58	276	118	36.2	12.15	1.5	0.7
4.7	6.57	3.05	270	108	40	13.62	1.3	0.6
6	5.21	2.41	236	89	49.5	16.4	1.0	0.5

The variables in Table 4.8 are: external gate resistance, $R_{g,ext}$; voltage and current overshoot, V_{os} and I_{os}; turn-on and turn-off energy loss, E_{on} and E_{off}; dv/dt and di/dt per chip size, dv/dt^* and di/dt^*.

Comparison of switching at similar dv/dt and di/dt per chip area: Fig 4.10 (a) and (b) compare switching transients of SiC MOSFET versus Si IGBT at similar dv/dt^* and di/dt^*. Apparently, SiC MOSFET incurs higher losses compared to Si IGBT for the equal chip sizes. As a consequence, the former module will have a higher junction temperature; i.e., **the power loss density in SiC is considerably higher**. Moreover, for the same chip sizes, the SiC device provides a higher current rating than that of a Si device. Hence, a SiC device is anticipated to have a larger thermal ripple, and thus the probability of failure due to bond wire lift-off and solder fatigue will be higher. This also demands a more stringent requirement for the package materials compared to Si.



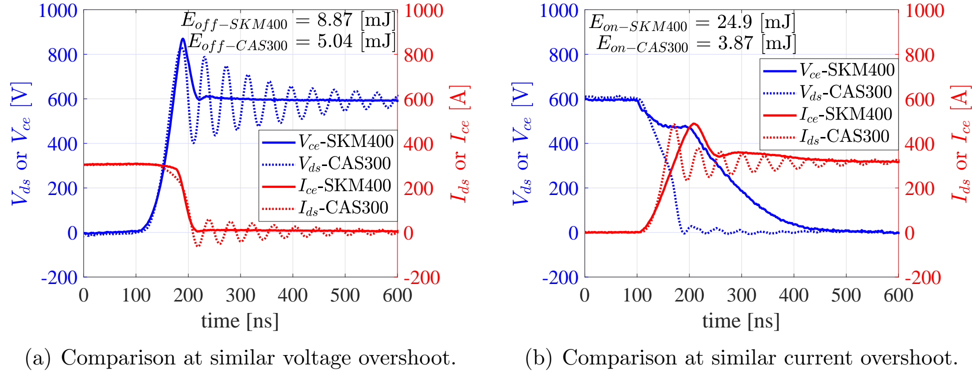
(a) Turn-off at similar dv/dt per chip size.

(b) Turn-on at similar di/dt per chip size.

Figure 4.10: Measurement of switching transients of SiC MOSFET module versus Si IGBT module at similar dv/dt per chip area during turn-off and similar di/dt per chip area during turn-on. Provided the same chip area, SiC MOSFET incurs higher losses compared to Si IGBT, indicating the possible higher junction temperature in the chip of the former module.

Comparison of switching at similar voltage and current overshoots: Fig 4.11 (a) and (b) exemplify the measured switching events at similar V_{os} during turn-off and similar I_{os} during turn-on. The turn-off energy loss is higher by a factor of 1.75 in the Si IGBT compared to the SiC MOSFET while keeping similar V_{os}. A comparison at

similar I_{os} for these modules shows that the Si IGBT entails higher turn-on energy loss, a factor of 6.4 higher in Si IGBT compared to SiC MOSFET. **The tail current in IGBT functions partly as a turn-off snubber, resulting in lower or no ringing.** However, the MOSFET is a unipolar device and has no tail current, thus the amount of parasitic ringing is markedly higher.



(a) Comparison at similar voltage overshoot.   (b) Comparison at similar current overshoot.

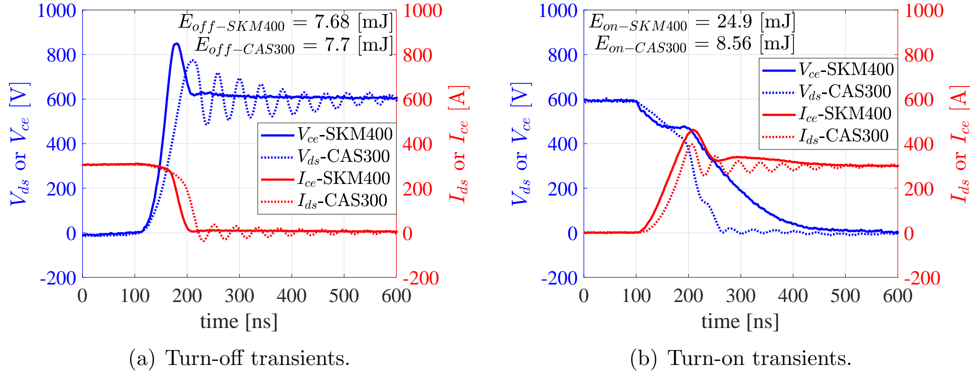
Figure 4.11: Measurement of switching transients of SiC MOSFET versus Si IGBT modules at similar voltage overshoot during turn-off and similar current overshoot during turn-on. Given the similar overshoot, SiC MOSFET shows better performance than Si IGBT from an efficiency viewpoint, but the amount of parasitic ringing is noticeably higher in SiC MOSFET. Note that turn-on losses are higher in Si IGBT which is primarily because of the higher recovery charge of Si pn diode associated with it.

Comparison of switching loss in SiC MOSFET versus Si IGBT: From Table 4.8, it is evident that V_{os} of the Si IGBT increases with gate resistance during turn-off ($R_{g,off}$), reaches a peak value and then decreases again. Therefore, $R_{g,off}$ of 0 Ω is chosen as an optimized value, which also gives the lowest loss. As a trade-off between I_{os} and turn-on losses, $R_{g,on}$ of 2.35 Ω is chosen. Considering ringing, switching losses and overshoots, $R_{g,on}$ of 5 Ω and $R_{g,off}$ of 3.4 Ω are chosen for the SiC MOSFET. Table 4.9 shows the specific switching energy loss for the selected gate resistances. The turn-off loss turns out to be equal for both modules, whereas the turn-on loss in the SiC MOSFET is 1/3 times that of the Si IGBT. The specific reverse-recovery loss of SiC diode ($E_{rr-spec}$) is 1/8.76 times that of Si diode. Fig. 4.12 displays the switching transients for an optimal case.

Table 4.9: Specific loss of SiC MOSFET versus Si IGBT for the selected $R_{g,on}$ and $R_{g,off}$.

Half-bridge parts	$R_{g,on}$ (Ω)	$R_{g,off}$ (Ω)	$E_{on-spec}$ (μJ/A)	$E_{off-spec}$ (μJ/A)	$E_{rr-spec}$ (μJ/A)
SiC MOSFET	5	3.4	28.5	25.6	1.3
Si IGBT	2.35	0	83	25.6	11.4

The variables used in Table 4.9 are: turn-on and turn-off gate resistance, $R_{g,on}$ and $R_{g,off}$; specific switching energy loss of transistor during turn-on and turn-off, $E_{on-spec}$ and $E_{off-spec}$; and specific reverse-recovery energy loss of diode, $E_{rr-spec}$.



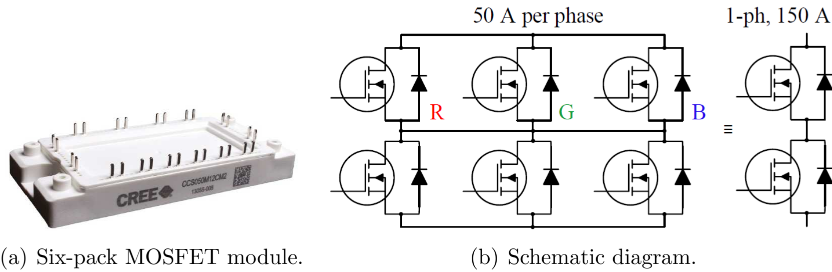
(a) Turn-off transients. (b) Turn-on transients.

Figure 4.12: Comparison of switching events for the chosen optimal case.

4.3.2 SiC MOSFET versus Si soft-punch-through IGBT

4.3.2.1 Device under test and hardware setup

A photograph of a six-pack module is provided in Fig. 4.13 (a). For achieving higher output power, three bridge-legs of the modules are paralleled forming a single half-bridge configuration, a schematic diagram of which is shown in Fig. 4.13 (b). In order to have a comparable stray inductance as in a real application circuit, a three-phase inverter power circuit board, acting as a stripline connection between the module and the DC-link capacitors, is built, and a six-pack module is mounted such that the three bridge-legs are paralleled outside the module.



(a) Six-pack MOSFET module. (b) Schematic diagram.

Figure 4.13: (a) Photograph of a six-pack SiC MOSFET module from Wolfspeed. (b) Schematic diagram showing the parallel connection of three phases in a six-pack SiC MOSFET module forming an equivalent single phase (1-ph), 150 A, half-bridge configuration.

Table 4.10 shows the key electrical parameters of the SiC MOSFET versus the Si IGBT taken from the manufacturer's data sheet [131, 132]. Both the modules have same packaging and voltage rating (1.2 kV). A complete laboratory setup showing the DPT measurement is depicted in Fig. 4.14. The Si IGBT is driven by the same gate driver as that of the SiC MOSFET, except for a small modification for obtaining ±15 V required for driving an IGBT.

Table 4.10: Key electrical parameters of SiC MOSFET versus Si SPT IGBT modules.

Parameters / Module	CCS050M12CM2 Wolfspeed (MOSFET)	FS75R12KT4_B15 Infineon (IGBT)
$R_{DS,on}$ / $R_{CE,on}$ (mΩ) @25°C	25	11.1
$R_{DS,on}$ (mΩ) @125°C	39.4	15.51
V_{CEO} (V) @25°C	Absent	1
V_{CEO} (V) @125°C	Absent	0.84
R_d (mΩ) @25°C	10	9.46
R_d (mΩ) @125°C	19.77	10.62
V_{FO} (V) @25°C	0.85	1.05
V_{FO} (V) @125°C	0.77	0.93
C_{iss} (nF) @ 600 V	2.81	4.3
C_{oss} (nF) @ 600 V	2.55	3.30
C_{rss} (nF) @ 600 V	0.014	0.16
Q_{rr}/Q_c (μC)	0.28	16
Q_g (nC)	180	570
$R_{g,int}$ (Ω)	1.5	10
$V_{gs,th}$ / $V_{ge,th}$ (V)	2.3	5.8
V_{gs} / V_{ge} (V)	+20/-5	±15
L_{module} (nH)	30	19

The variables used in Table 4.10 are: on-state resistance of MOSFET / IGBT, $R_{DS,on}/R_{CE,on}$; on-state resistance of diode, R_d; on-state knee voltage of IGBT, V_{CEO}; on-state knee voltage of diode, V_{FO}; input capacitance, C_{iss}; output capacitance, C_{oss}; reverse transfer capacitance, C_{rss}; capacitive charge of SiC diode, Q_c; reverse-recovery charge of Si diode, Q_{rr}; total gate charge, Q_g; internal gate resistance of semiconductor module, $R_{g,int}$; gate-source or gate-emitter threshold voltage, $V_{gs,th}$ / $V_{ge,th}$; gate-source or gate-emitter, V_{gs} / V_{ge}; and internal stray inductance of module, L_{module}.

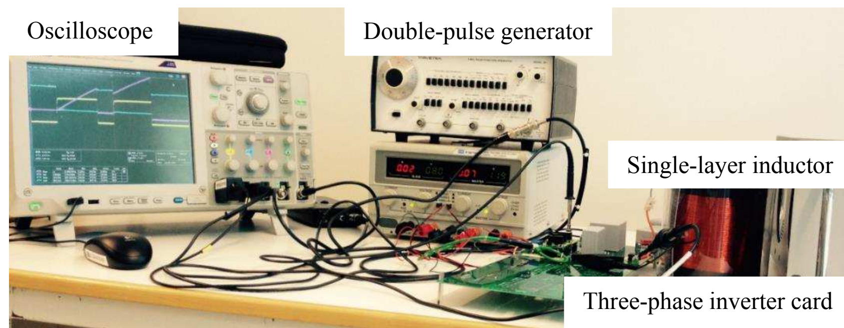
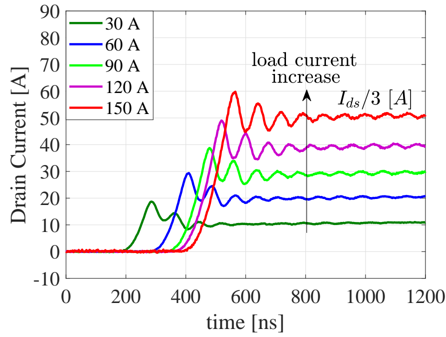


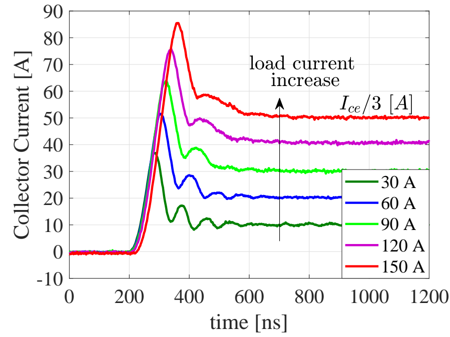
Figure 4.14: Hardware setup showing the double pulse test arrangement. Switching energy loss is measured using a three-phase inverter power circuit board in order to emulate a stray inductance of a real application circuit.

4.3.2.2 Measurement results

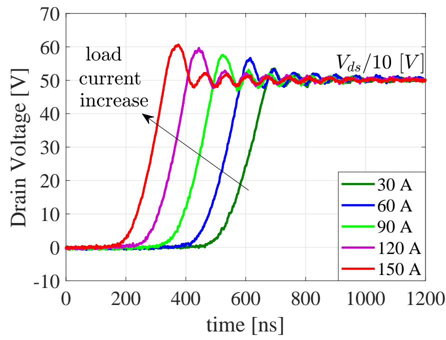
Switching transients with varying load current: In this section, the DC-link voltage is set to 500 V while the load current is increased from 30 A to 150 A. It can be observed from Fig. 4.15 that the di/dt of the current in the SiC MOSFET and the diode



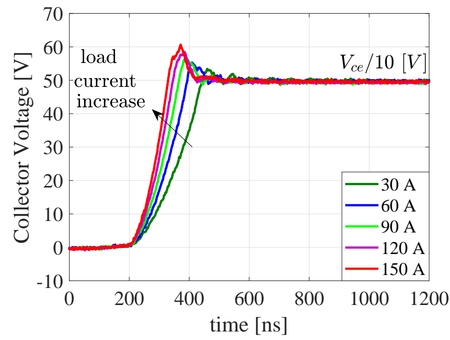
(a) Turn-on transient of the MOSFET.



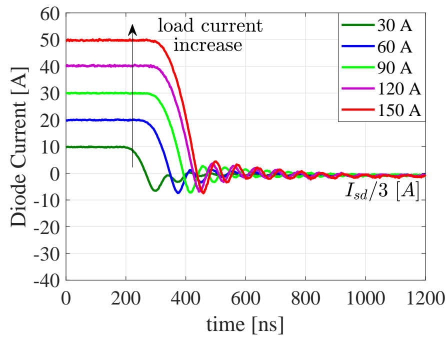
(b) Turn-on transient of the IGBT.



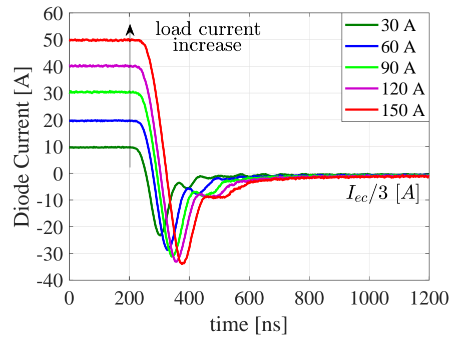
(c) Turn-off transient of the MOSFET.



(d) Turn-off transient of the IGBT.



(e) Turn-off transient of the SiC JBS.

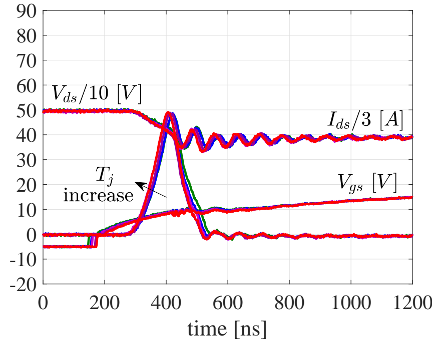


(f) Turn-off transient of the Si diode.

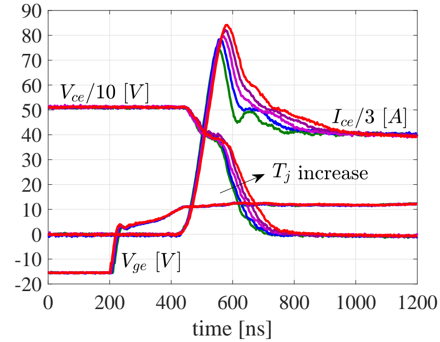
Figure 4.15: Drain-source/collector-emitter current, drain-source/collector-emitter voltage and diode current with varying load current for the SiC MOSFET versus the Si IGBT.

increases slightly, while the dv/dt of the MOSFET voltage increases noticeably. This aspect of the part of behavior in the SiC MOSFET also corresponds to that of the Si IGBT. However, **the peak reverse current of the SiC anti-parallel diode remains almost constant at all the load currents**, which is depicted in Fig. 4.15 (e). Conversely, **the peak reverse-recovery current of the Si anti-parallel diode increases with the increase of the load current**, which is apparent from Fig. 4.15 (f). This exemplifies a clear benefit of using a SiC JBS diode instead of a Si pn diode as the switching behavior of the former remains intact irrespective of the output power.

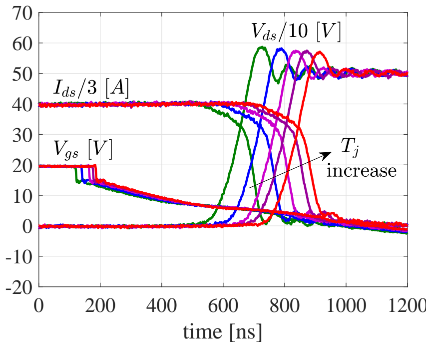
Switching transients with varying junction temperature: In this section, the DC-link voltage is set to 500 V and the load current to 120 A while the junction temperature is increased from 25 °C to 125 °C. With the increased temperature, the turn-on of SiC MOSFET becomes slightly faster, as depicted in Fig. 4.16. This is because of the negative temperature coefficient of gate threshold voltage, and therefore leads to a decrease in the turn-on switching energy loss. The SiC MOSFET module is co-packed with the SiC Junction barrier Schottky (JBS) diode as an anti-parallel diode. The reverse-recovery charge in the SiC SBD is extremely low compared to the Si diode [133]. This charge is not due to conductivity modulation as in Si diode and is independent of temperature, forward current and di/dt as inferred from these characterization and also conforms with [134].



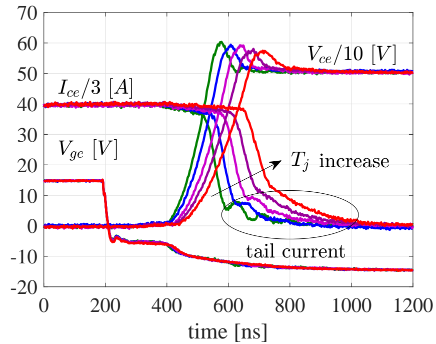
(a) Turn-on transient of the MOSFET.



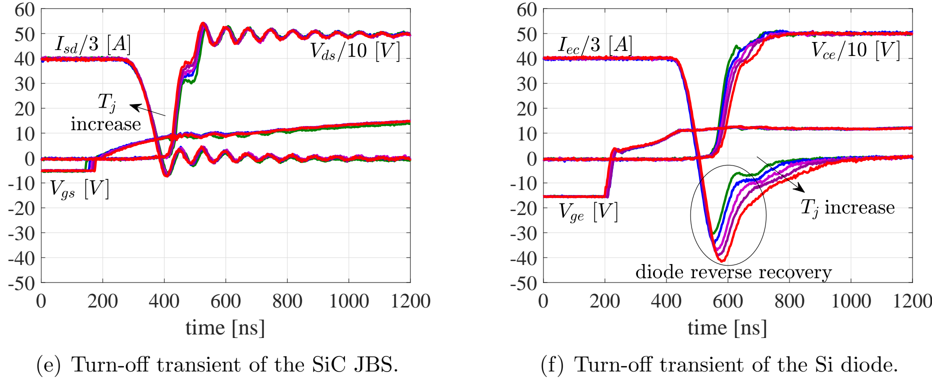
(b) Turn-on transient of the IGBT.



(c) Turn-off transient of the MOSFET.



(d) Turn-off transient of the IGBT.



(e) Turn-off transient of the SiC JBS.

(f) Turn-off transient of the Si diode.

Figure 4.16: Drain-source/collector-emitter current, drain-source/collector-emitter voltage and diode current with varying junction temperature for the SiC MOSFET versus the Si IGBT modules. Measured results illustrate that the reverse-recovery current of Si-pn diode and tail current of IGBT show strong temperature dependency while the characteristics of the SiC MOSFET and SiC diode remain less affected.

In the Si IGBT module, the Si diode is present as a freewheeling diode. It is evident from Fig. 4.16 (b) and (f) that the reverse-recovery current present at turn-off of the diode directly affects the current peak during the turn-on of the Si IGBT. This peak worsens with increased operating temperature. During the turn-off, the voltage overshoot decreases a little as the turn-off voltage rise slows down with increased temperature, as seen in Fig. 4.16 (d).

Table 4.11 shows a sample of key switching energy loss measurements for the SiC MOSFET versus the Si IGBT with a DC-link voltage of 500 V and a load current of 120 A at two different junction temperatures: 25 °C and 125 °C and two different gate

Table 4.11: Key measurements of SiC MOSFET vs Si IGBT module. V_{ds} = 500 V, I_{ds} = 120 A, two different junction temperatures: T_j = 25 °C and T_j = 125 °C, and two different gate resistances for each modules.

Device Under Test (DUT)	T_j (°C)	$R_{g,ext}$ (Ω)	dv/dt (V/ns)	di/dt (A/ns)	E_{off} (mJ)	E_{on} (mJ)	E_{rr} (mJ)
CCS050M12CM2 (Wolfspeed)	25	20	8.49	2.63	1.28	3.26	0.22
	25	36.5	**4.25**	1.33	**3.86**	6.95	0.11
	125	20	8	2.89	1.54	2.57	0.35
	125	36.5	4.08	1.5	4.08	6.28	0.12
FS75R12KT4_B15 (Infineon)	25	12.2	**4.37**	2.28	**6**	8.43	2.46
	25	20	4.42	1.43	6.36	14.13	2.34
	125	12.2	2.7	2.41	10.67	12.9	9.37
	125	20	2.4	1.5	10.36	18.36	7.7

The variables used in Table 4.11 are: device junction temperature, T_j; external gate resistance, $R_{g,ext}$; switching energy loss of transistor during turn-on and turn-off, E_{on} and E_{off}; and reverse-recovery energy loss of diode, E_{rr}.

resistances for each modules. dv/dt is the voltage slew rate during turn-off and di/dt is the current slew rate during turn-on of the DUT. The E_{off} in the Si IGBT is relatively high and is almost similar at both high (20 Ω) and low (12.2 Ω) $R_{g,ext}$. This is primarily governed by the intrinsic phenomenon within the IGBT structure. In particular, this is a result of the recombination process and the charge carrier lifetime being independent of $R_{g,ext}$.

On the other hand, the E_{off} of the SiC MOSFET decreases remarkably with decrease in $R_{g,ext}$, which is principally because of the unipolar nature of the device. The E_{on} of both devices depends strongly on $R_{g,ext}$. The E_{rr} in both the Si and SiC diodes decreases slightly with increasing $R_{g,ext}$. With the increase in temperature, E_{rr} increases substantially in the Si diode, whereas it is slightly increased or almost unaffected by the temperature in the SiC JBS. Further, at similar dv/dt of roughly 4.3 V/ns, E_{off} of Si IGBT is 1.5 times higher compared to that of SiC MOSFET, which is primarily because of the longer tail current that SPT IGBT exhibits.

4.4 Summary

The chapter has focused on the characterization of the state-of-the-art SiC MOSFET and Si IGBT modules, the summary of which are listed as follows:

1. The highest achievable dv/dt and di/dt with SiC MOSFET modules are roughly 35 V/ns and 10 A/ns for 120 A ratings and about 20 V/ns and 11 A/ns for 300 A ratings. Similarly, with the Si IGBT module the maximum dv/dt and di/dt measured at 300 A are about 17 V/ns and di/dt is 12 A/ns. This information was missing in the data sheet of the modules.

2. Both the simulation and laboratory results illustrate that higher stray parameters hinder utilization of the fast switching potential of SiC power modules; i.e., these parasitics slow down SiC devices and stress them with higher current and voltage overshoots, and higher losses.

3. A closer look into gate waveforms while varying gate-source capacitance show that higher values reduce ringing and maintain the gate loop stability. Conversely, higher gate-drain capacitance together with fast dv/dt can cause unwanted turn-on of the device owing to the fact that dv/dt related noise exceeds the threshold voltage limit of the SiC MOSFET. Overall, it is apparent that not only gate-drain capacitance but also the ratio of gate-source to gate-drain capacitance are responsible for the malfunction of the device, and this ratio should be kept high to avoid it.

4. The switching phenomenon of the SiC MOSFET is almost independent of the operating temperature, while there is a strong temperature dependence in the Si IGBT. In particular, the reverse-recovery current of the Si diode and the tail current of the IGBT worsens with increase in temperature.

5. A clear benefit of using SiC JBS diode instead of Si pn diode is exemplified as the switching behavior of the former remains intact irrespective of the loading conditions, such as higher output power and higher junction temperatures while the performance of the latter worsens with the same conditions.

Chapter 5

Characterization of body-diodes in state-of-the-art SiC MOSFETs

The information presented in this chapter is based on publication C6, the primary objective of which is to answer the following research question.

Q 1. Are the body-diodes in SiC MOSFETs good enough as freewheeling diodes?

5.1 Introduction

In power electronics applications, such as motor drives, synchronous rectifiers, phase shift PWM DC-DC power converters, an anti-parallel or a freewheeling diode is required across a semiconductor switching device to handle the current in the reverse direction. A MOSFET structure exhibits an intrinsic body-diode which has a structure of a PiN diode. In a SiC MOSFET, this PiN diode has a very high forward voltage drop (V_F = 4.8 V at V_{gs} = -5 V, I_F = 20 A, 25 °C [135]) because SiC has a wider bandgap energy (≈ 3 eV) compared to Si (≈ 1.2 eV). However, V_F in a SiC Schottky diode is significantly lower (1.8 V, I_F = 20 A, 25 °C) [136] as it is determined by the metal semiconductor barrier height instead of a p^+n junction barrier in the PiN diode [45].

There are different perspectives presented in the available literature in different time-frames. For example, in [137] the use of the body-diode is not recommended; instead, an external Schottky diode is suggested because of its high V_F. In other words, the PiN-structure of the parasitic-diode in the SiC MOSFET was not optimized for lower losses. Then the data sheet of the manufacturer would contain very limited information about the body-diode and that limited information would be presented at low di/dt (for instance 0.1 A/ns) [138]. There has been continuous improvement in the performance of the body-diode and the data sheets have been also updated accordingly. In the synchronous rectifier operation, the MOSFET channel is turned on in the reverse conducting mode so that the major part of the current flows through this channel and only a part through the body-diode. Alternatively stated, the MOSFET shunts the conduction phase current away from the body-diode reducing the conduction losses caused by the high V_F. Results with similar operations as that of Si MOSFET were also presented for SiC MOSFET in [139]. Thereafter, Wolfspeed have updated their data sheet for the second generation MOSFETs with higher di/dt of 2.4 A/ns [135] along with the third-quadrant characteristics as an addendum compared to its first generation MOSFET [138]. Looking further in various publications, eliminating the anti-parallel diode and using only the

improved body-diode (i.e., turning on the channel) for increasing current capacity in the SiC MOSFET module is presented in [140]. Reference [141] compared body-diodes of Si and SiC MOSFETs focusing on the forward and gate characteristics. In [142, 143], the switching energy loss of the SiC junction barrier Schottky (JBS) diode is compared with that of the body-diode in SiC MOSFET. Moreover, the switching and robustness of body-diodes are studied in [144].

Since **the quality of the body-diode in the SiC MOSFET is continuously improved as per data sheet, it is crucial to examine the switching quality of the body-diode of a new-generation MOSFET by laboratory measurement.** Understanding the behavior of the body-diode and Schottky diode helps us decide whether there is the need for an external diode or not. Besides, according to the author's knowledge, to date, the reverse-recovery of the body-diodes in the overall FET family has not yet been evaluated together. **In particular, when the devices are from different manufacturers, the recovery performances are not available under similar conditions, such as similar voltage, similar current, and similar di/dt. In addition, di/dt during the second-half of the reverse-recovery is barely included in the data sheet, and has been discussed in the literature to only a limited extent** Therefore, in this work the switching performances of the body-diodes in a new generation of SiC FETs: MOSFET (planar and trench types), JFET (cascode trench), are compared with the SiC Schottky diodes (planar). The dv/dt and di/dt associated with each device are discussed thoroughly. All the devices under test (DUTs) are presented in Section 5.2. Following this is the methodology in Section 5.3. Section 5.4 demonstrates the hardware setup and measurement considerations. Experimental results with a series of key electrical parameters, namely, peak reverse-recovery current (I_{rrm}), recovery time (t_{rr}), dv/dt, and di/dt during first- and second-half of the reverse-recovery are presented and discussed in Section 5.5. Finally, Section 5.6 presents the most important conclusions.

5.2 Device under test

Table 5.1 shows a comparison of the most significant parameters, such as breakdown voltage (V_{DS}), forward voltage drop (V_F or V_{SD}), forward current (I_F or I_{sd}), chip area, and device technology of the body-diodes in planar [82, 135, 145] and trench [146] SiC MOSFETs, and planar [136, 147] SiC Schottky diodes used in the measurements. The

Table 5.1: Key parameters of the investigated device under test.

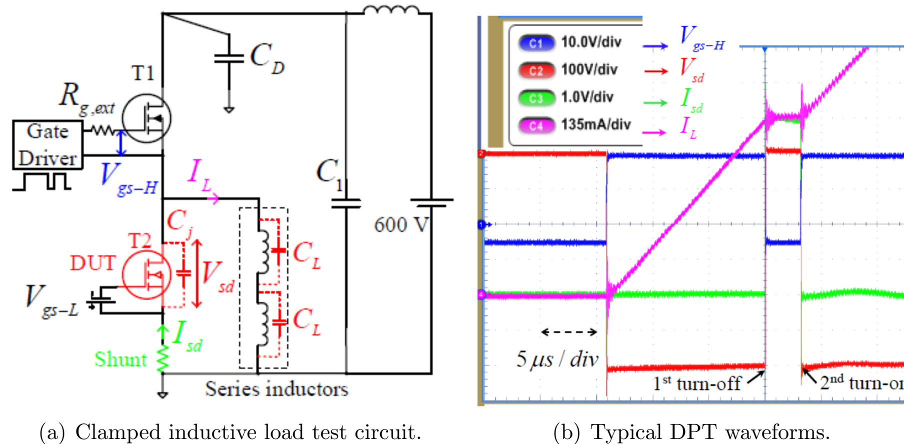
DUT	V_{DS} (kV)	V_F or V_{SD} (V) @ 25/150 °C	I_F or I_{sd} (A) @ 25°C	Die size (mm^2)	Technology
C2M0080120D	1.2	4.8/4.3	36 @ V_{gs} = -5 V	10.41	MOSFET-P
C3M0065090D	0.9	5.8/5.4	23.5 @ V_{gs} = -4 V	3.53	MOSFET-P
SCT3040KL	1.2	3.2/3.5	55 @ V_{gs} = 0 V	13.64	MOSFET-T
UJC1206K	1.2	1.45/2.1	38 @ V_{gs} = 0 V	14.67	JFET-T
C4D30120D	1.2	1.8/2.3	44	14.58	JBS diode-P
SCS310AP	0.65	1.7/2.05	10	3.06	JBS diode-P

The variables used in Table 5.1 are: breakdown voltage, V_{DS}; forward voltage drop, V_F or V_{SD}; forward current, I_F or I_{sd}; and gate-source voltage, V_{gs}. Also note that V_F is taken at I_{sd} = 20 A. Moreover, the planar and trench technologies are indicated by P and T, respectively.

body-diode in the trench SiC JFET with cascode configuration [148, 149] is also listed in Table 5.1 to give a complete overview of the diodes in FET technology. Fig. 2.3 in Chapter 2 shows the structures of SiC MOSFET with planar versus trench technology. Put simply, trench structures improve the static performances of the devices [46].

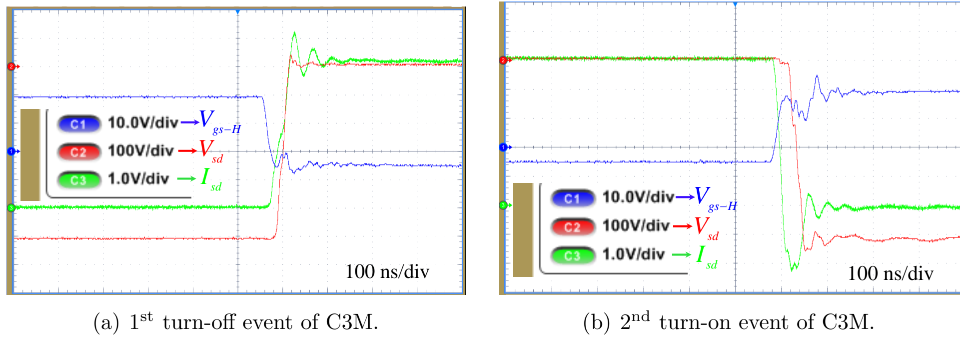
5.3 Methodology

The double-pulse test (DPT) methodology is used for accessing the dynamic performance of a body-diode in a SiC MOSFET. Two pulses are sent to a control device (transistor T1) in a clamped inductive load circuit, as shown in Fig. 5.1 (a), while the gate and source of the DUT are either shorted or supplied with -5 V in order to ensure that the DUT is turned-off all the time, and hence, only the body-diode is active in the circuit. Fig. 5.1 (b) displays the typical test waveforms, where the first turn-off (at the end of the first pulse) and the second turn-on (at the beginning of the second pulse) are indicated. Channel 1 is the gate voltage of the transistor T1 (V_{gs-H}), Channel 2 is the anode-to-cathode voltage of diode (V_{sd}), Channel 3 is the source-to-drain current (I_{sd}), and channel 4 is the current through load inductor (I_L). By regulating the width of the first pulse and the DC-bus voltage, the desired load current is achieved. Each time only two pulses are applied and the DUT is switched only twice. As a consequence, the device junction temperature rises due to the switching loss becomes negligibly small. Thus, the junction temperature can be controlled externally by the hot plate. A gate voltage of 20 V is applied during turn-on and -5 V during turn-off for the upper MOSFET. In order to use the passive probe and coaxial shunt for voltage and current measurements; respectively, with the same reference (grounding) as that of the oscilloscope, the body-diode of low side transistor T1 is hard-switched. By varying the external gate resistance ($R_{g,ext}$), the slew rates of the current and voltage across the DUTs are controlled. It should be noted that the internal resistance of T1 is 7 Ω. Detailed view of first turn-off and the second turn-on events are displayed in Fig. 5.2.



(a) Clamped inductive load test circuit. (b) Typical DPT waveforms.

Figure 5.1: Illustration of a clamped inductive load circuit for hard switching test of body-diode in SiC MOSFET (a), and an example of a typical DPT waveform in (b).

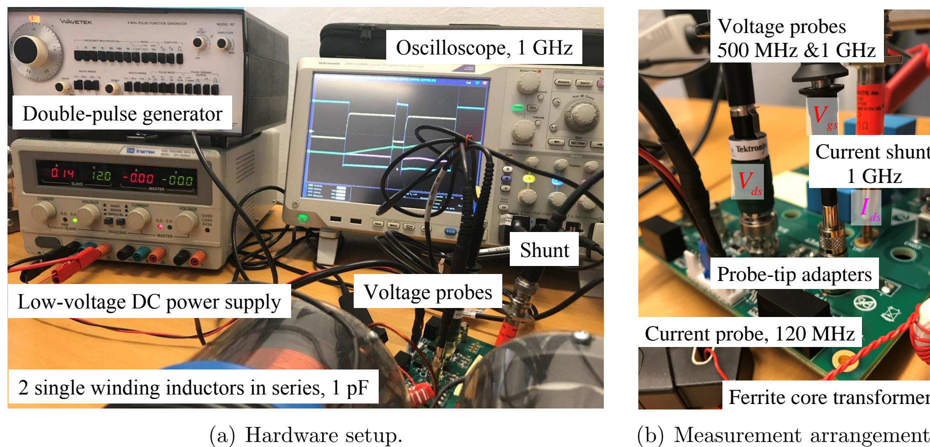


(a) 1st turn-off event of C3M. (b) 2nd turn-on event of C3M.

Figure 5.2: Illustration of the detailed view of the first turn-off and the second turn-on events, as indicated in Fig. 5.1 (b) for C3M MOSFET at 600 V and 20 A. For analyzing the reverse-recovery performance of the DUT, the second turn-on instant, where the transistor is turned-on and the diode is turned-off, is the key point of interest, which will be the focus in the upcoming sections of this chapter for different chosen DUTs. Note that the lower transistor is chosen as a DUT in order to facilitate the current and voltage measurements by shunt and passive probe with the same reference as that of the oscilloscope.

5.4 Hardware setup and measurement considerations

The complete laboratory setup with measurement is illustrated in Fig. 5.3. Double-pulses are generated using a function generator. Two single-layer winding air core inductors are connected in series as an inductive load. A printed circuit board (PCB) probe-tip adapter is employed in order to reduce the ground-lead inductance, as shown in Fig. 5.3 (b).



(a) Hardware setup. (b) Measurement arrangements.

Figure 5.3: Laboratory setup showing the arrangement for current and voltage measurements of the body-diode. The current is measured using a high-bandwidth, low-inductive-current shunt. The voltage is measured using a high-bandwidth single-ended probe, mounted to the PCB using a probe-tip adaptor for a reduction of the ground-lead inductance.

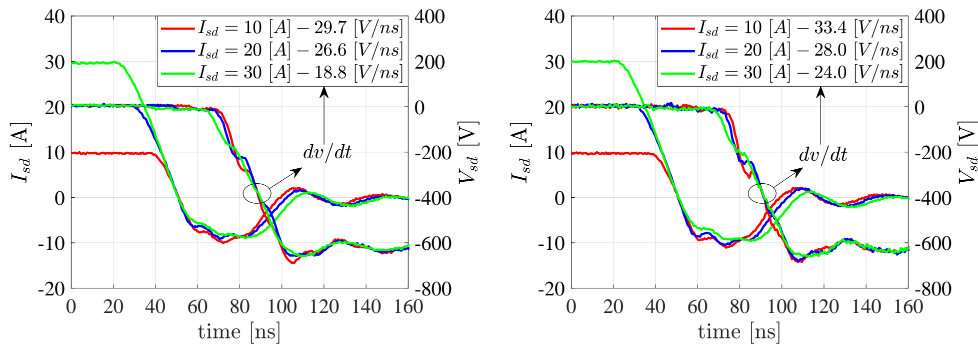
5.5 Experimental results

In this section, the reverse-recovery characteristics of the various chosen DUTs are evaluated at different operating conditions including the forward current, turn-off voltage, and current commutating slope (di/dt). Moreover, this section is divided into four subsections. Subsection 5.5.1 compares planar versus trench SiC MOSFETs. This is followed by Subsection 5.5.2, which evaluates SiC Schottky diodes with different chip areas. Then, in Subsection 5.5.3, the switching performance of cascode SiC JFET is included. Finally, Subsection 5.5.4 compares the turn-off characteristics of all DUTs at two voltages: 400 and 600 V.

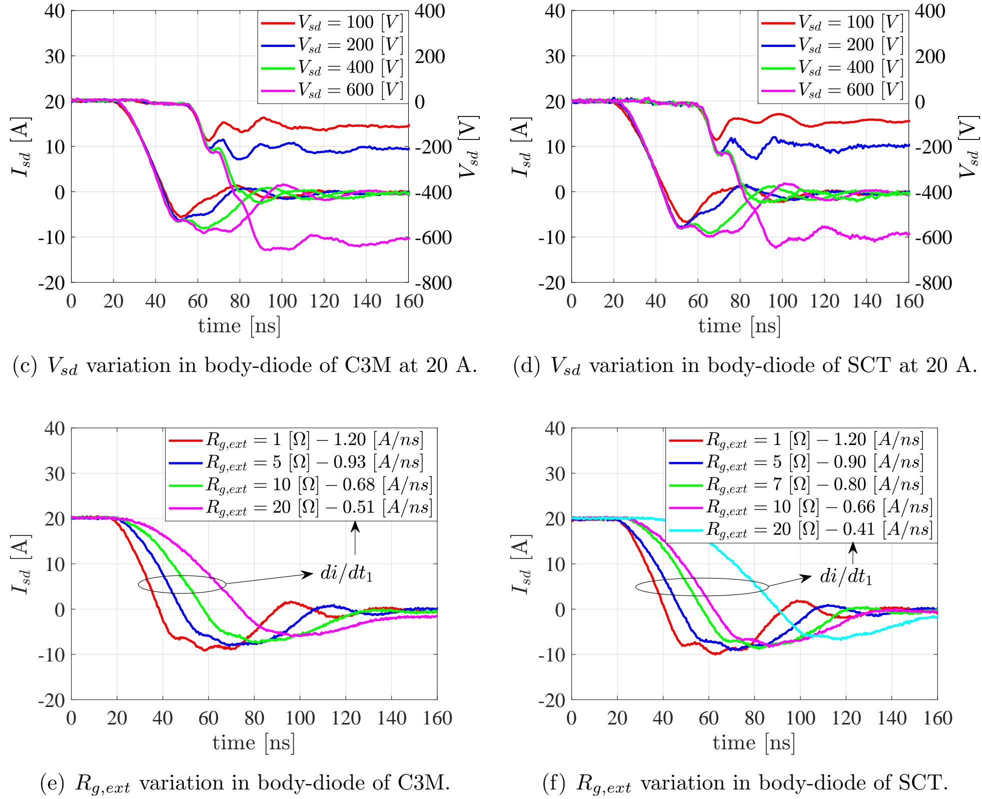
5.5.1 Planar versus double-trench MOSFETs

In this subsection, two technologies in SiC MOSFET: planar (C3M) versus double-trench (SCT) are compared. Fig. 5.4 shows the switching waveforms of body-diodes in C3M versus SCT MOSFETs. Apparently, **when I_{sd} through a body-diode increases, I_{rrm} and t_{rr} are negligibly affected provided the same V_{sd}**, as can be seen in Fig. 5.4 (a) and (b), unlike that of Si PiN diodes where these parameters significantly increase with increase in I_{sd} [90] **indicating that there is a little or no charge storage mechanism in body-diodes of these SiC MOSFETs. Indeed, there are two fundamental reasons for smaller stored charges in SiC MOSFETs: first, the lower lifetime of the minority carrier, and second, the smaller physical area of the die, and hence, smaller area for stored charges in SiC compared to that in Si.**

Furthermore, it is also elucidated from Fig. 5.4 that lower the I_{sd}, the greater the dv/dt. Note that dv/dt mainly concerns insulation strain. Examining the experimental results in Fig. 5.4 (c) and (d) at I_{sd} of 20 A, it is evident that **both I_{rrm} and t_{rr} increase with supply voltage.** Actually, **higher energy ($1/2 \cdot C_{oss} \cdot V_{sd}^2$) is stored at higher voltage, and thus leads to higher charge, which is the reason for an additional area at higher voltage compared to lower voltage.** As can be seen in Fig. 5.4 (e) and (f), the smaller gate resistance increases peak of I_{rrm} and di/dt during the first-half of recovery (di/dt_1). On closer observation, the body-diode in SCT shows noticeable decrease in di/dt_1 with increase in $R_{g,ext}$ than that in C3M.



(a) I_{sd} variation in body-diode of C3M at 600 V. (b) I_{sd} variation in body-diode of SCT at 600 V.



(c) V_{sd} variation in body-diode of C3M at 20 A.

(d) V_{sd} variation in body-diode of SCT at 20 A.

(e) $R_{g,ext}$ variation in body-diode of C3M.

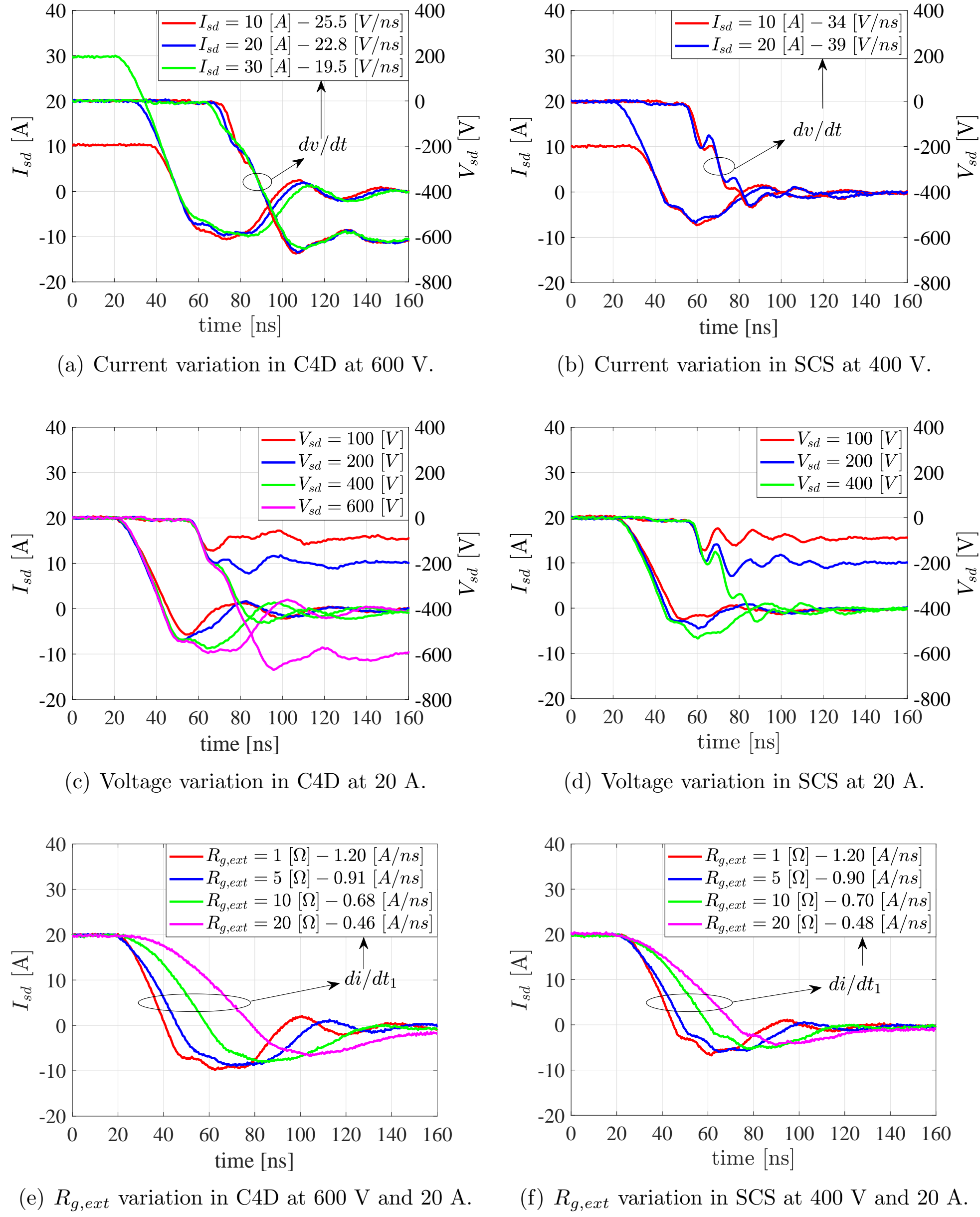
(f) $R_{g,ext}$ variation in body-diode of SCT.

Figure 5.4: Current and voltage variation in the body-diode of planar (C3M) versus double-trench (SCT) SiC MOSFETs illustrates that the recovery performances are similar in these devices, whereas gate resistance variation shows a noticeable decrease in di/dt_1 in the body-diode of SCT compared to those in C3M.

5.5.2 Planar Schottky diodes with different chip areas

In this subsection, planar Schottky diodes with different chip sizes are compared. Fig. 5.5 reveals that **SCS offers better reverse-recovery performance than C4D which, in fact, is due to the smaller chip size of SCS**, as documented in Table 5.1. Measurements with SCS are shown up to 400 V because it has a smaller voltage rating compared to C4D. It is observed that with the same $R_{g,ext}$ of MOSFET, when the I_{sd} increases, dv/dt decreases in C4D whereas for the same conditions, the reverse is true in SCS.

Table 5.2 shows the quantification of the key electrical parameters for SCS versus C4D from the laboratory measurements at $R_{g,ext}$ of 1 Ω and two different V_{sd}: 100 and 400 V. As shown, at 400 V, all the parameters including dv/dt, di/dt_2 (current slew rate during the second half of recovery), I_{rrm}, and t_{rr} are higher than those at 100 V. For the same V_{sd}, C_j in SCS is about 1.5 times smaller compared to that in C4D, and thereby the stored energy in the junction capacitance is about 1.5 times higher in C4D than in SCS. It is also observed that the dv/dt varies in the range of 20 V/ns to 39 V/ns at 400 V.



(a) Current variation in C4D at 600 V.

(b) Current variation in SCS at 400 V.

(c) Voltage variation in C4D at 20 A.

(d) Voltage variation in SCS at 20 A.

(e) $R_{g,ext}$ variation in C4D at 600 V and 20 A.

(f) $R_{g,ext}$ variation in SCS at 400 V and 20 A.

Figure 5.5: Impact of current, voltage, and gate resistance variation in the Schottky diodes, C4D versus SCS, reveal that the reverse-recovery performances are better in SCS.

Table 5.2: dv/dt, di/dt_2, I_{rrm}, and t_{rr} of C4D and SCS at 20 A and two different voltages: 100 and 400 V.

(a) dv/dt, di/dt_2, I_{rrm}, and t_{rr} at 100 V.

DUT	V_{sd} = 100 V				
	C_j (pF)	dv/dt (V/ns)	di/dt_2 (A/ns)	I_{rrm} (A)	t_{rr} (ns)
SCS310AP	90	19.7	0.29	2.46	24
C4D30120D	138	17.9	0.51	5.68	23

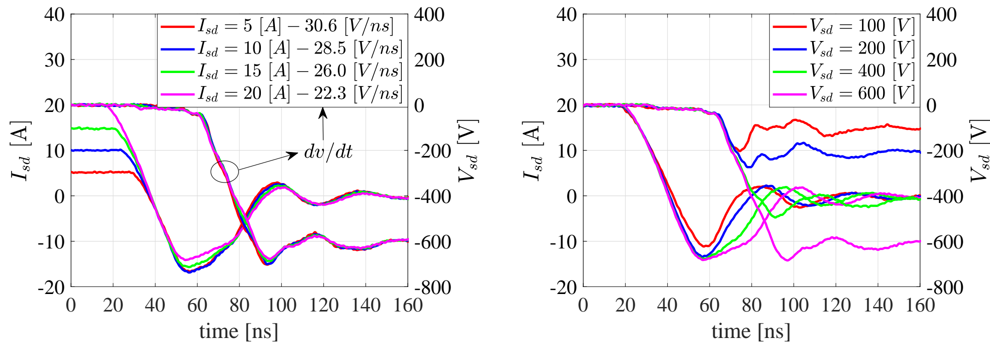
(b) dv/dt, di/dt_2, I_{rrm}, and t_{rr} at 400 V.

DUT	V_{sd} = 400 V				
	C_j (pF)	dv/dt (V/ns)	di/dt_2 (A/ns)	I_{rrm} (A)	t_{rr} (ns)
SCS310AP	48	39.0	0.36	6.66	43
C4D30120D	70	19.8	0.55	8.93	46

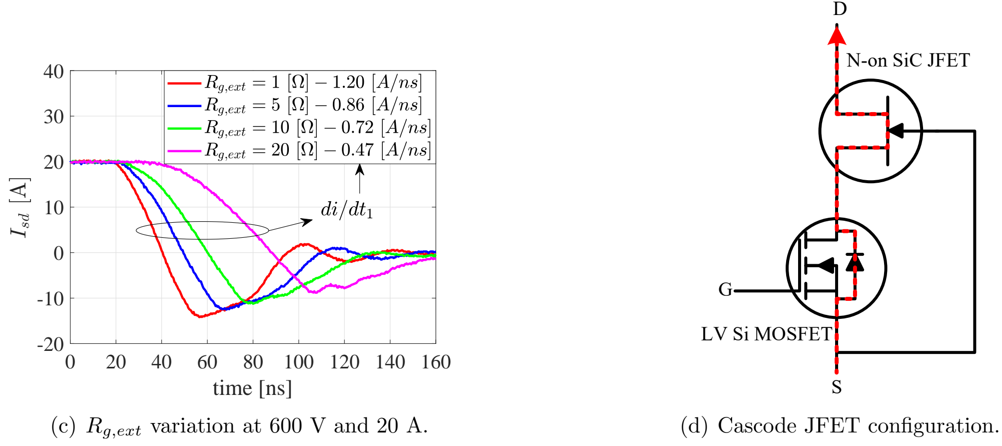
The variables used in Table 5.2 are: junction capacitance of Schottky diode, C_j; anode-to-cathode voltage of diode, V_{sd}; voltage slew rate of V_{sd}, dv/dt; current slew rate during second-half of reverse-recovery, di/dt_2; peak reverse-recovery current, I_{rrm}; and reverse-recovery time, t_{rr}.

5.5.3 Trench cascode JFET

In this subsection, the body-diode in trench cascode JFET is discussed. Fig. 5.6 (a)–(c) depicts the turn-off switching performance of JFET. Clearly, it can be observed that **the I_{rrm} in the body-diode of SiC JFET decreases as I_{sd} increases and the opposite is true as V_{sd} or di/dt increases.** It is worth mentioning that the trench SiC JFET does not contain a built-in body-diode or any parasitic NPN transistor as seen with SiC MOSFET. However, during the reverse conducting mode, the body-diode of low-voltage (LV) Si MOSFET and the JFET channel provide a current path, as routed by a red dashed line in Fig. 5.6 (d), providing the same functionality like an anti-parallel diode.



(a) I_{sd} variation in body-diodes of UJC at 600 V. (b) V_{sd} variation in body-diodes of UJC at 20 A.

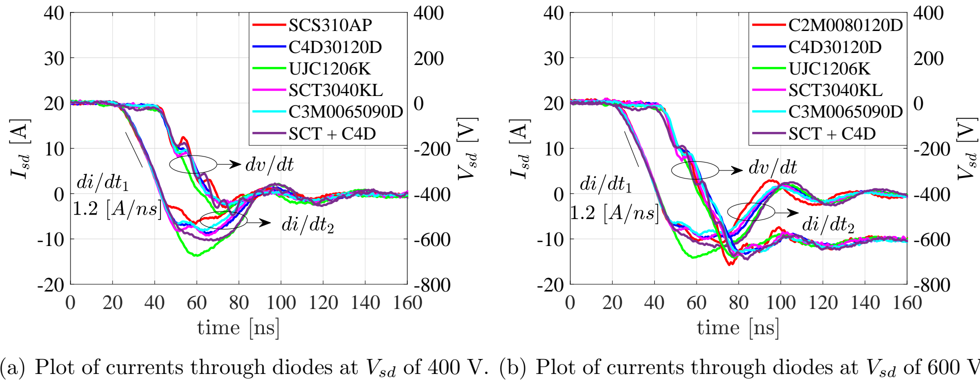


(c) $R_{g,ext}$ variation at 600 V and 20 A.   (d) Cascode JFET configuration.

Figure 5.6: Current, voltage and di/dt variations in the body-diode of trench SiC cascode JFET illustrate that as I_{sd} increases, I_{rrm} decreases; and as V_{sd} or di/dt increases, the I_{rrm} and the recovery area increases.

5.5.4 Comparison of DUTs at 400 and 600V

This section compares the turn-off voltage and current transients of all the DUTs. Fig. 5.7 shows the summary plots of all the DUTs switched at 25°C, $R_{g,ext}$ of 1 Ω, and I_{sd} of 20 A for two different V_{sd}, namely, 400 and 600 V. **At the beginning or first-half of the reverse-recovery di/dt_1 (governed by the upper transistor) is 1.2 A/ns, however, at the final part or the second-half of it, di/dt_2 (mainly impressed by the diode technology) softens down for all the devices under consideration**, as shown in Table 5.3.



(a) Plot of currents through diodes at V_{sd} of 400 V. (b) Plot of currents through diodes at V_{sd} of 600 V.

Figure 5.7: Comparison of the voltage and the reverse-recovery current of different diode technologies at 400 V (a) and 600 V (b). With $R_{g,ext}$ of 1 Ω, di/dt_1 imposed by the circuit is 1.2 A/ns at both voltage levels, while di/dt_2 depends on the technology of the diode and circuit. The key electrical parameters, such as dv/dt, di/dt_2, I_{rrm}, and t_{rr} are quantified and listed in Table 5.3 (a) and (b) for each of the DUTs.

It is clear from Fig. 5.7 that **the recovery performance of the body-diode in SiC MOSFET is comparable to that of the SiC JBS diode.** This is primarily a result of the very small minority carrier lifetime and thinner drift layer of SiC MOSFET, and thus, this leads to a considerably smaller amount of stored charges in the device drift region.

In circuits where diodes conduct for longer periods, for instance, generator-side rectifier, an external anti-parallel SiC JBS is used to bypass the conduction losses contributed by the intrinsic diode of SiC MOSFET. Therefore, a case with a SiC MOSFET and an anti-parallel SiC diode (SCT + C4D, as indicated in Fig. 5.7) is also presented, which gives an impression that their combined impact increases the recovery loss compared to that of a case with a body-diode only (marked by a legend SCT3040KL).

The t_{rr} and I_{rrm} depend on I_{sd}, V_{sd}, $R_{g,ext}$ and junction temperature (not discussed in this chapter), and are not provided for the same conditions in the data sheet, particularly when the devices are from different manufacturers. Moreover, dv/dt, di/dt_2, which are central parameters, are barely included in the data sheet. However, in this work these parameters are compared at the same conditions, for instance, the same I_{sd}, V_{sd}, $R_{g,ext}$, and temperature (room temperature) for all the DUTs, and are presented in Table 5.3. As shown, dv/dt varies in the range of 21 V/ns to 37 V/ns at 600 V.

Table 5.3: dv/dt, di/dt_2, I_{rrm}, and t_{rr} of the investigated DUTs at 400 V and 600 V while keeping a constant di/dt_1 of 1.2 A/ns. Compared to 400 V, dv/dt, I_{rrm}, and t_{rr} are measured to be higher at 600 V.

(a) dv/dt, di/dt_2, I_{rrm}, and t_{rr} at 400 V.

DUT	$V_{sd} = 400$ V				
	C_j/C_{oss} (pF)	dv/dt (V/ns)	di/dt_2 (A/ns)	I_{rrm} (A)	t_{rr} (ns)
C2M0080120D	100	28	0.53	9.80	44
C4D30120D	70	19.8	0.55	8.93	46
UJC1206K	100	21.0	0.73	13.74	46
SCT3040KL	120	28.5	0.63	9.20	52
C3M0065090D	70	25.6	0.40	8.13	45
SCT + C4D	190	34.9	0.70	10.34	47

(b) dv/dt, di/dt_2, I_{rrm}, and t_{rr} at 600 V.

DUT	$V_{sd} = 600$ V				
	C_j/C_{oss} (pF)	dv/dt (V/ns)	di/dt_2 (A/ns)	I_{rrm} (A)	t_{rr} (ns)
C2M0080120D	85	30.4	0.66	11	47
C4D30120D	56	20.9	0.64	9.8	53
UJC1206K	90	24.9	0.68	14.2	55
SCT3040KL	90	31.1	0.54	10.2	53
C3M0065090D	60	26.3	0.51	9.2	52
SCT + C4D	146	36.7	0.75	11.8	55

The variables used in Table 5.3 are: junction capacitance of Schottky diode, C_j; output capacitance of MOSFET, C_{oss}; anode-to-cathode voltage of diode, V_{sd}; voltage slew rate of V_{sd}, dv/dt; current slew rate during second-half of reverse-recovery, di/dt_2; peak reverse-recovery current of diode, I_{rrm}; and reverse-recovery time of diode, t_{rr}.

5.6 Conclusion

Aside from the fact that a body-diode in SiC MOSFET is of bipolar type, the switching characteristics are only affected to a very insignificant level by the forward currents and commutation rates like in a unipolar SiC Schottky diode. Compared to the body-diodes in SiC MOSFETs and unipolar Schottky diodes, the body-diode in the cascode JFET showed higher peak reverse-recovery current because the body-diode in cascode structure is essentially the combination of the body-diode in low-voltage Si MOSFET and the channel of JFET. However, none of these diodes showed snappy behavior and higher voltage overshoots as in Si PiN and fast recovery diodes. Thus, looking into the recovery losses of the body-diodes in FET, SiC MOSFETs are better over cascode SiC JFETs while the converse is true in terms of the conduction losses. In particular, the body-diode in a SiC JFET exhibits around the same conduction losses as the majority carrier Schottky diodes and 3-4 times lower compared to those of SiC MOSFETs. In addition, the comparison between the Schottky diodes reveals that diodes with smaller chip area (SCS) have a better reverse-recovery performance compared to those with a larger chip area (C4D).

In the initial generations of SiC MOSFETs, when body-diodes are used for a longer conduction period, $R_{DS,on}$ of MOSFET as well as V_F of body-diode increases. This leads to an increase in leakage current and, eventually, thermal breakdown of MOSFET would occur [56, 57]. However, the new-generation SiC FETs are robust and do not have such issues, i.e., FET characteristics do not degrade by the use of body-diode [56,61–63]. Thus, the body-diodes of SiC FETs are suitable for use as freewheeling diodes from a reliability perspective. Overall, as conduction losses are significant only during the dead time and the diodes are normally shunted by the transistor during the conduction phase, the body-diodes of SiC FETs are therefore effective as freewheeling diodes. However, when an external anti-parallel diode is used together with channel conduction, the aggregate conduction losses are lower compared to those without an external anti-parallel diode. Therefore, a trade-off between the optimum performance and economics has to be considered when deciding to use or not to use an anti-parallel SiC JBS diode.

Chapter 6

Applications of SiC power devices

This chapter covers three different key applications of SiC devices: a 240 kW, back-to-back connected, two-level, three-phase, voltage source converter (VSC) for wind power, an 80 kW, single-phase, full-bridge resonant converter for inducting heating, and a 1 kW boost converter for power factor correction (PFC). Most of this chapter contains results presented on publications J1, J2 and J3.

Regarding wind power applications, this chapter quantifies the benefits of using state-of-the-art SiC MOSFET over Si IGBT in a back-to-back configured, two-level, three-phase VSC converter arrangement using a space vector pulse width modulation (SVPWM) approach. Via the combination of experimental and simulation results, the converter efficiency is quantified, which demonstrated that the solution with SiC MOSFET entails lower losses compared to that of the Si IGBT over all the switching frequency ranges; the advantages of SiC being more pronounced at higher frequencies and higher temperatures. For instance, it is shown that the back-to-back converter with SiC MOSFET is 0.86% and 5.04% more efficient at 1 kHz and 50 kHz, respectively over Si IGBT. Furthermore, it is also illustrated that for the same output power the inverter switching frequency can be increased by approximately six times in the SiC MOSFET compared to that in the Si IGBT with the similar total power loss. Thus, the reduction in loss can be utilized in a number of ways to improve the circuit design, such as an increase in efficiency, and a reduction in the cooling requirement. In particular, in a grid-connected offshore wind system, by increasing the operating frequency, the size of passive components, namely the filter and transformer, can be reduced resulting in higher power density of the system.

Regarding induction heating applications, the efficiency of an SiC DioMOS-based 80 kW inverter is quantified via a calorimetric loss measurement method. It is proven that an inverter achieves an efficiency of 99.3% when switched at roughly 200 kHz. Furthermore, the current and voltage graphs from the oscilloscope are presented, which show no oscillations demonstrating a low-inductive DC-link design. This work was the basis for making a 1.85 MW, 300 kHz welder put into operation approximately one year later [23].

Concerning PFC applications, efficiency and EMI are quantified for a 1 kW converter operating in a continuous conduction mode (CCM). A low-parasitic design approach is employed together with an input EMI filter in this rectifier, the experimental results of which proved that the efficiency satisfies 80 PLUS regulation and the EMI complies with CISPR 11 class B conducted EMI limit. Moreover, a dramatic reduction in the size of boost inductor is demonstrated when the switching frequency is changed from 66 to 250 kHz. However, the emissions are increased by roughly 10 dB throughout the conducted spectra.

6.1 Wind power applications

Space and weight are of paramount importance in wind power applications because these factors directly influence the cost and size of the mechanical design of the tower/nacelle. SiC offers several advantages compared to the currently used semiconductors, which can potentially be translated to power devices with higher voltage, lower on-state and switching losses, and higher operating temperatures, leading to the compact, efficient, and thermally stable power conversion system. Accordingly, the converter can easily be mounted in the nacelle of wind turbine. SiC is recognized as a potential technology for wind power applications in [150,151]. Reference [90] compared the performance of SiC MOSFET with Si IGBT, where the IGBT was the soft-punch-through (SPT) type, also called the field-stop type, maximized for the conduction loss. Similarly, in [18], a performance comparison between SiC MOSFET with non-punch-through (NPT) type of Si IGBT (optimized for the switching loss) was investigated. Of special note is that an IGBT is a bipolar component; hence, carrier lifetime can be enhanced as per the applications requirement, i.e., a trade-off between switching loss (dv/dt) and conduction loss can be made. However, this work [22] covers the detailed loss comparison at varying load current as an extension to the work presented in [18]. Most importantly, the loss in a back-to-back converter for offshore wind application is simulated using the experimentally measured data as a look-up table input. Moreover, it verifies the simulation results with the numerical and analytical calculations. The overall quantitative evaluation of the total converter loss and efficiency at different switching frequencies provides an insight into the potential performance gains that SiC MOSFETs can bring over Si IGBTs for such applications.

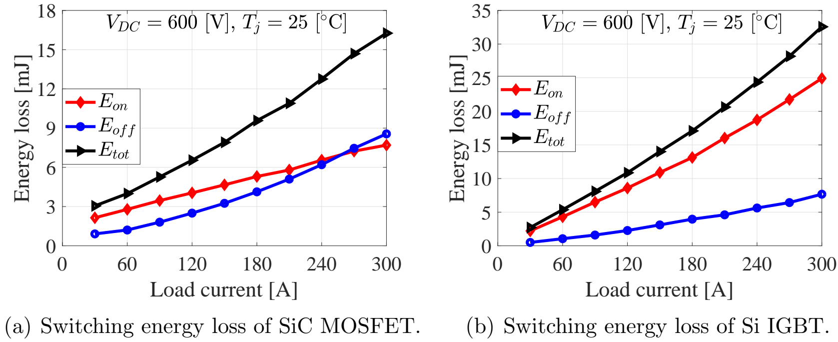
6.1.1 Methodology and measurement results

Table 6.1 shows the essential electrical parameters of the SiC MOSFET versus the Si IGBT taken at 25 °C and 125 °C from the manufacturers data sheet [127,130]. $R_{DS,on}$ / $R_{CE,on}$ is the on-state resistance of MOSFET / IGBT, V_{CEO} and V_{FO} are the on-state knee voltage of IGBT and diode, and R_d is the resistance of the freewheeling diode. Fig. 6.1 (a) and (b) show the turn-on (E_{on}), turn-off (E_{off}) and total losses (E_{tot}) with varying load current, which will be used as a look-up table input for the simulation of converter losses in Section 6.1.2.

Table 6.1: Key electrical parameters of half-bridge SiC MOSFET module versus half-bridge Si NPT IGBT module.

Parameters	SiC MOSFET Wolfspeed			Si IGBT Semikron		
	25 (°C)	125 (°C)	difference (%)	25 (°C)	125 (°C)	difference (%)
$R_{DS,on}$ / $R_{CE,on}$ (mΩ)	5.0	7.8	+ 36	6.3	7.6	+ 17
V_{CEO} (V)	Absent	Absent	Absent	1.4	1.7	+ 17
R_d (mΩ), diode	2.25	4.35	+ 48	2.7	3.0	+ 10
V_{FO} (V), diode	0.925	0.83	- 17	1.4	1.1	- 27

The column marked with "difference" in Table 6.1 refers to the percentage change in on-state resistance or knee voltage when the temperature increases from 25 °C to 125 °C.



(a) Switching energy loss of SiC MOSFET. (b) Switching energy loss of Si IGBT.

Figure 6.1: Plot of E_{on}, E_{off}, and E_{tot} of SiC MOSFET (a) and Si IGBT (b) at V_{DC} of 600 V.

6.1.2 Topology selection and simulation of losses

Primarily, there are two main popular and commercialized voltage source converter (VSC) topologies in offshore wind applications. The first is a three-phase, two-level type and the second is a three-phase, three-level neutral point diode clamped (3L-NPC) type [152,153]. The former topology is employed for the low-voltage and the latter for the high-voltage applications. These converters are mounted in a back-to-back configuration such that each shares the same DC-link as illustrated in Fig. 6.2. One converter acts as a rectifier (connected on the generator side) and another converter acts as an inverter (connected on the grid side). When IGBTs/MOSFETs along with anti-parallel diodes are used, the converter allows for a bidirectional flow of power. In this work, a three-phase, two-level topology, as shown in Fig. 6.2, is chosen where the main purpose is to study the power losses in the back-to-back converter and perform the comparison between all-Si and all-SiC devices. Using MATLAB Simulink, the switching loss obtained from the laboratory measurements and the conduction loss from the data sheet are used as a look-up table or polynomial functions based on the curve fitting for simulating the total converter loss. The loss is simulated for a space vector PWM (SVPWM) [154], DC-link voltage (V_{DC}) of 760 V, modulation index (m) of 1, and a load current ($I_{out,rms}$) of 300 A. The converter output voltage ($V_{out,rms}$) is about 460 V ($\sqrt{3}/(2 \cdot \sqrt{2}) \cdot V_{DC} \cdot$ m) and the power rating is approximately 240 kW.

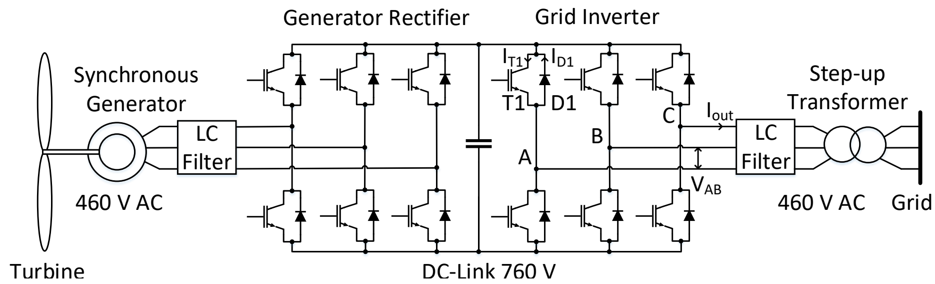


Figure 6.2: Schematic diagram of a two-level, three-phase, back-to-back converter configuration for low-voltage offshore wind applications. Current in one of the top switches and diodes of grid-side inverter are denoted by I_{T1} and I_{D1}, correspondingly.

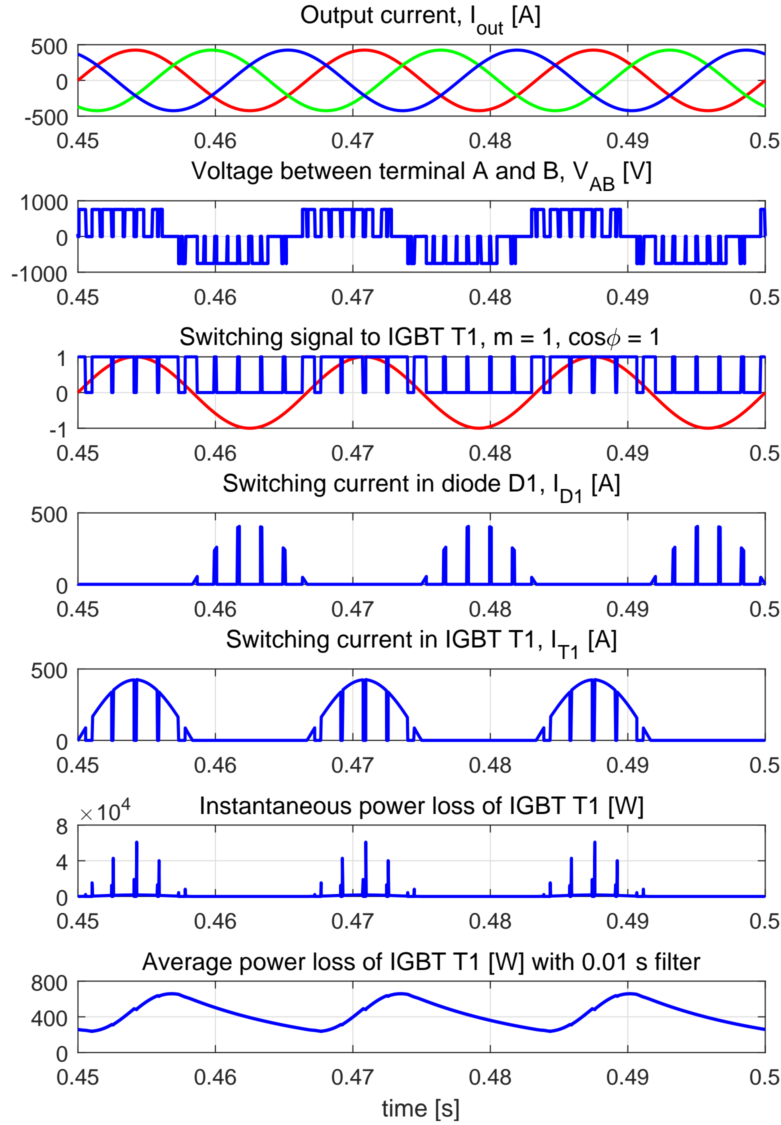


Figure 6.3: Illustration of the sample of simulated waveforms at various points in the schematic for the grid-side inverter in a standard two-level topology. With the DC-link voltage of 760 V, RMS output current of 300 A, $cos\phi$ of unity, modulation index of 1, and switching frequency of 600 Hz, the total simulated power loss of IGBT T1 is 433 W, the instantaneous and average power losses are displayed in the lower two graphs.

6.1.3 Simulation results

Fig. 6.3 illustrates the simulated waveforms of the inverter-side, such as output current (I_{out}), voltage between terminals A and B (V_{AB}), switching signal to IGBT T1, switching current in diode D1 (I_{D1}), switching current in IGBT T1 (I_{T1}), instantaneous power loss of

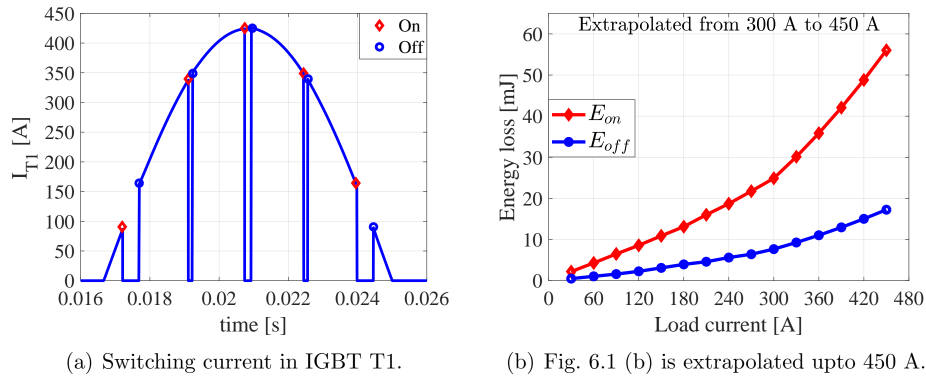
IGBT T1, and average power loss of IGBT T1 with a filter of 0.01 (1/60) s. These sample plots are exemplified with switching frequency (f_{sw}) of 600 Hz, fundamental frequency of 60 Hz and m of 1. Note that the reasons for selecting f_{sw} of 600 Hz are: lower f_{sw} means few switching events and thereby better visibility, and eases the calculation during the verification phase in the following section.

6.1.3.1 Numerical verification of the simulation results

In the numerical verification method, the turn-on, turn-off, and total switching power losses of IGBT T1; $P_{sw-on-T1}$, $P_{sw-off-T1}$, and $P_{sw-tot-T1}$, correspondingly; are computed by counting the number of switching events during the fundamental cycle of the output. Table 6.2 lists the reading of currents and the corresponding energy losses from Fig. 6.4 (a) and (b), respectively. Note that Fig. 6.4 (b) is derived from Fig. 6.1 (b) by extrapolation of data from 300 A to 450 A using the same coefficients of polynomial as obtained by curve fitting the plot from 30 A to 300 A. The total sum of E_{on} is 133.3 mJ (11.8 + 34 + 50 + 31 + 6.49 = 133.3 mJ), and as a result $P_{sw-on-T1}$ of IGBT T1 is 10.13 W (133.3/1000 × 760/600 × 60 = 10.13 W). Similarly, the total sum of E_{off} is 38.19 mJ and $P_{sw-off-T1}$ is 2.90 W, and thus, $P_{sw-tot-T1}$ is 13.03 W, as listed in Table 6.3 in the row named "Numerical". As the percentage differences between numerically calculated and simulated losses with reference to the numerical losses are below 4%, as shown in Table 6.3, indicated by row "Error", the simulation results have reasonable accuracy.

Table 6.2: Reading of currents and energy losses (refer Fig. 6.4 (a) and (b).

I_{T1} [A]	90	160	340	350	425
E_{on}[mJ]	11.8	34	50	31	6.49
E_{off} [mJ]	1.59	10	12.8	10.4	3.4



(a) Switching current in IGBT T1.

(b) Fig. 6.1 (b) is extrapolated upto 450 A.

Figure 6.4: (a) Detailed (zoomed in) view of switching current in IGBT T1. The RMS output current is 300 A, m is 1, $cos\phi$ is 1, fundamental frequency is 60 Hz, and switching frequency is 600 Hz. (b) Extrapolation of Fig. 6.1 (b) to fill in values in Table 6.2.

Table 6.3: A comparison of simulated and numerically calculated power loss of transistor T1.

Power loss [W]	$P_{sw-on-T1}$	$P_{sw-off-T1}$	$P_{sw-tot-T1}$
Simulation	9.75	2.79	12.55
Numerical	10.13	2.90	13.03
Error [%]	3.75	3.79	3.68

The variables used in Table 6.3 are: turn-on, turn-off, and total switching power losses of IGBT T1; $P_{sw-on-T1}$, $P_{sw-off-T1}$, and $P_{sw-tot-T1}$, respectively.

6.1.3.2 Analytical verification of the simulation results

The switching loss of IGBT/MOSFET ($P_{sw-trans-T1}$) can be estimated using analytical approximations as long as the energy loss during switching is linearly dependent on the collector current, as given by (6.1) [155]. Compared to the simulated results, as presented in Table 6.3, the error was found to be in the range of 5–10%. This is essentially due to the assumption of linear dependence in (6.1) during analytical calculations, whereas switching loss is taken as a quadratic function of current during simulations. Moreover, considering the sinusoidal dependency of duty cycles versus time, the on-state power loss of IGBT ($P_{cond-trans-T1}$) and diode ($P_{cond-diode-D1}$) can be calculated by using (6.2) and (6.3), respectively [156, 157].

$$P_{sw-trans-T1} = f_{sw} \cdot (E_{on} + E_{off}) \cdot \frac{\sqrt{2}}{\pi} \cdot \frac{I_{out,rms}}{I_{ref}} \cdot \frac{V_{DC}}{V_{ref}} \tag{6.1}$$

$$P_{cond-trans-T1} = V_{CEO} \cdot I_{out} \cdot \left(\frac{1}{2\cdot\pi} \pm \frac{m\cdot cos\phi}{8}\right) + R_{CE,on} \cdot I_{out}^2 \cdot \left(\frac{1}{8} \pm \frac{m\cdot cos\phi}{3\cdot\pi}\right) \tag{6.2}$$

$$P_{cond-diode-D1} = V_{FO} \cdot I_{out} \cdot \left(\frac{1}{2\cdot\pi} \mp \frac{m\cdot cos\phi}{8}\right) + R_{d} \cdot I_{out}^2 \cdot \left(\frac{1}{8} \mp \frac{m\cdot cos\phi}{3\cdot\pi}\right) \tag{6.3}$$

In these equations where $\pm$ are present, the upper sign applies for an inverter mode (motor operation) and the lower sign for a rectifier mode (generator operation). For a MOSFET, the first term in (6.2) will be zero because it does not possess knee voltage. For the greater clarity, a description of symbols used in (6.1)–(6.3) is provided in Table 6.4. Note that ϕ is a phase angle of current with respect to voltage, which is -90° $\leq$ +90° for an inverter or a motor operation, and +90° $\leq$ +270° for rectifier or generator mode. However, the worst cases: 0° for motor, and 180° for generator, are analyzed in this work. The differences in analytically calculated and simulated conduction losses with respect to those with analytically calculated alone are found to be below 3%.

Table 6.4: Definition of symbols used in (6.1) - (6.3).

Symbol	Description	Value
V_{ref}	reference voltage	600 V
I_{ref}	reference current	300 A
ϕ	phase angle between current and voltage	0° (inverter), 180° (rectifier)
I_{out}	peak output current	$\sqrt{2} \times I_{out,rms} = 424$ A
f_{sw}	switching frequency	1 kHz - 50 kHz
m	modulation index	1

6.1.4 Evaluation of inverter power loss at different switching frequencies

A detailed loss breakdown at various switching frequencies (1 to 50 kHz) is provided in Fig. 6.5. The chosen IGBT is a NPT type optimized for the fast switching over the conduction loss. Simulation results show that the conduction loss in the Si IGBT inverter is higher by a factor of 2 at 25 °C to that in the SiC MOSFET inverter. Furthermore, the results showed that the total conduction loss ($P_{cond-trans}$) is approximately equal to the total switching loss ($P_{sw-trans}$) at around 15 and 25 kHz for the all-Si and all-SiC inverters, accordingly, i.e., for the low frequency region, the conduction loss is a dominating part of the total inverter loss. It should be pointed out that the turn-off power losses of the selected devices are almost equal because the NPT IGBT switches off as fast as SiC MOSFET. The all-Si inverter has approximately 3.3 times higher $P_{sw-trans}$ than that of the all-SiC inverter, the major share being the combined loss of $P_{sw-on-trans}$ and P_{rr}. Therefore, in order to use Si IGBT at higher switching frequency, a practical solution would be the use of a SiC diode as an anti-parallel diode instead of Si diode (a Hybrid solution) as this solution leads to the reduction in P_{rr}, and subsequently its influence on $P_{sw-on-trans}$. Nonetheless, SiC MOSFET is a better solution than NPT IGBT for all the range of switching frequencies, unlike in a SPT IGBT, as discussed in the previous work, where the losses were comparable for lower frequencies ($\leq$ 3 kHz) [90].

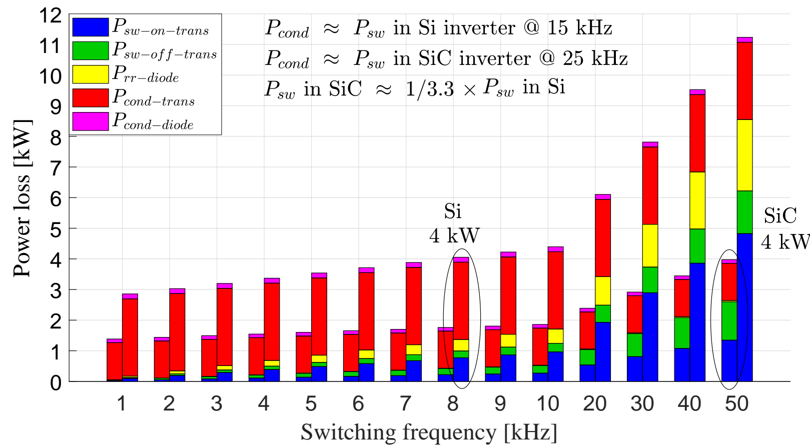


Figure 6.5: Breakdown of power loss in an inverter at different switching frequencies. The legends in the bar chart are: turn-on switching loss ($P_{sw-on-trans}$), turn-off switching loss ($P_{sw-off-trans}$), diode recovery loss (P_{rr}), conduction loss in a transistor ($P_{cond-trans}$), and conduction loss in a diode ($P_{cond-diode}$). SiC MOSFET helps to reduce the switching loss, which is a dominant part of the total loss in an IGBT inverter, particularly the $P_{sw-on-trans}$. Inverters with SiC MOSFET can switch at higher frequency compared to those with Si IGBT with almost the same total power loss: an example of which is indicated in the bar chart where the frequency is about six times higher in SiC than in Si for the same total inverter power loss of about 4 kW.

6.1.5 Evaluation of back-to-back converter efficiency at different switching frequencies

A comparison of the total converter efficiency in a back-to-back converter using the all-SiC devices with the all-Si devices is depicted in Fig. 6.6. The converter with the SiC MOSFET shows 0.86 and 5.04% higher efficiencies at 1 and 50 kHz, correspondingly over their Si IGBT counterparts, as depicted in Fig. 6.6. The simulated switching losses of the back-to-back converters are equal, but the conduction losses are not. For instance, in the case of a rectifier mode, the simulated $P_{cond-trans}$ is lower and $P_{cond-diode}$ is higher by a factor of 10 compared to those, correspondingly, in the case of an inverter mode.

Hence, the SiC MOSFET offers lower on-state and switching losses compared to Si IGBT. Moreover, the MOSFET structure possesses an intrinsic diode with a switching performance that is almost like a SiC Schottky diode, and thereby, the need for an additional anti-parallel diode can be eliminated. However, there is no such possibility in IGBT structure. The VSC with high-voltage SiC MOSFETs (when available in $\approx$ 10 kV range) will be the most attractive candidate for high-voltage direct current (HVDC) connections to offshore wind-farms as efficiency becomes more important.

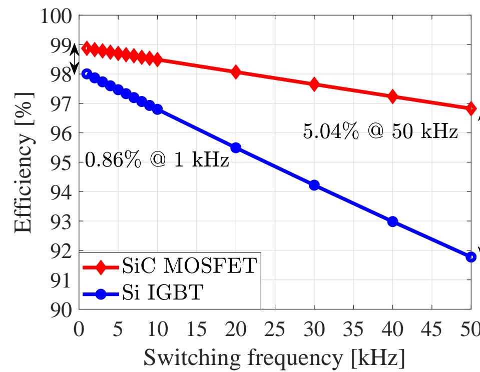


Figure 6.6: Comparison of SiC MOSFET and Si IGBT efficiencies in a three-phase back-to-back converter illustrates that at all the switching frequencies, the higher efficiency SiC MOSFETs provide a performance advantage over their Si IGBT counterparts. At switching frequencies of 1 kHz, 3 kHz (practical for today's offshore applications) and 50 kHz, converter with the SiC MOSFET shows 0.86%, 1.05% and 5.04% higher efficiencies over Si IGBT.

6.1.6 Discussion and summary

This section discusses the conduction and switching losses in two different sets of MOSFETs and IGBTs during motoring and generating modes.

6.1.6.1 Six-pack, SiC MOSFET and Si SPT IGBT

Table 6.5 lists the central parameters of six-pack SiC MOSFET versus six-pack Si IGBT modules required for computing conduction losses. Table 6.6 summarizes the conduction losses in a two-level VSC during motoring and generating modes. As mentioned in

Chapter 4, this Si IGBT is called an SPT type, where the conduction losses are optimized over switching losses. The additional variables used in Table 6.6 are: $P_{cond-tot}$ and $P_{cond-norm-SiC}$, which correspond to total conduction loss and normalized total conduction loss with regard to the total conduction loss of SiC devices. As seen in Table 6.5, the on-state resistances show a positive temperature coefficient, while the opposite is true concerning the knee-voltages. In all-Si solutions, the aggregate conduction losses are lower during both the motoring and the generating modes compared to those in all-SiC solutions at 125 °C, as evident from Table 6.6. Moreover, these losses are higher by just a factor of 1.14 in all-Si compared to all-SiC solutions at 25 °C. In [90], these sets of devices are evaluated and it is illustrated that a converter solution with SiC MOSFET is more efficient throughout the whole switching frequency range: 1 to 100 kHz, compared to the solution with Si IGBT.

Table 6.5: Key electrical parameters of the six-pack SiC MOSFET module versus the six-pack Si SPT IGBT module.

Parameters	CCS050M12CM2 Wolfspeed			FS75R12KT4_B15 Infineon		
	25 (°C)	125 (°C)	difference (%)	25 (°C)	125 (°C)	difference (%)
$R_{DS,on}$ / $R_{CE,on}$ (mΩ)	8.33	13.13	+ 57.6	3.7	5.17	+ 39.7
V_{CEO} (V)	Absent	Absent	Absent	1	0.84	- 16
R_d (mΩ), diode	3.33	6.59	+ 97.7	3.15	3.54	+ 12.2
V_{FO} (V), diode	0.85	0.77	- 9.4	1.05	0.93	- 11.4

Table 6.6: Conduction losses of SiC MOSFET versus Si IGBT modules (six-packs) in a two-level VSC during motoring versus generating operations at two different junction temperatures.

Parameters	Motoring				Generating			
	SiC MOSFET Wolfspeed		Si IGBT Infineon		SiC MOSFET Wolfspeed		Si IGBT Infineon	
T_j (°C)	25	125	25	125	25	125	25	125
$P_{cond-trans}$ (W)	520	819	593	626	43	67	62	63
$P_{cond-diode}$ (W)	54	67	62	58	515	689	577	557
$P_{cond-tot}$ (W)	574	886	655	684	558	756	639	620
$P_{cond-norm-SiC}$	1	1	1.14	0.77	1	1	1.14	0.82

6.1.6.2 Half-bridge, SiC MOSFET and Si NPT IGBT

Table 6.7 summarizes the similar results with another sets of SiC MOSFET and Si IGBT. Here the IGBT is a PT type and is optimized for high speed switching over conduction losses. Looking back in Chapter 4, at similar dv/dt of 5 V/ns, the E_{off} losses are roughly the same in these sets of devices; however, the conduction losses, as listed in Table 6.7, are significantly higher in Si IGBT compared to those in SiC MOSFET, particularly during motoring mode.

Table 6.7: Conduction losses of SiC MOSFET versus Si IGBT modules (half-bridges) in a two-level VSC during motoring versus generating operations at two different junction temperatures.

Parameters	Motoring				Generating			
	SiC MOSFET Wolfspeed		Si IGBT Semikron		SiC MOSFET Wolfspeed		Si IGBT Semikron	
T_j (°C)	25	125	25	125	25	125	25	125
$P_{cond-trans}$ (W)	1248	1947	2585	3122	102	159	250	302
$P_{cond-diode}$ (W)	126	161	177	157	1230	1683	1687	1545
$P_{cond-tot}$ (W)	1374	2107	2762	3280	1332	1842	1937	1848
$P_{cond-norm-SiC}$	1	1	2	1.55	1	1	1.45	1.0

6.1.6.3 Low speed and high speed drives

In low speed motor drive applications, the fundamental frequency of motor is 50/60 Hz. Thus, the motor is heavy and large, as a consequence, the inductance of motor works as a filter. In such an application, dv/dt is limited between 2 V/ns to 5 V/ns to keep insulation of motor winding safe, the solution with SiC MOSFETs can be considered in two ways. The first is to switch them as slowly as Si IGBTs and thereby benefit from their low conduction losses. The second is to switch them to their fast switching potential, but keep the switching frequency low like today ($<$ 5 kHz). This way, these converters can benefit from both switching and conduction losses, and thus the size of heat sink can be substantially reduced. However, if this is the case, there will be losses in the dv/dt filter. Therefore, the question is whether the losses should be in the active devices (MOSFET/IGBT) by slowing down devices via a gate driver to satisfy dv/dt limits or if the losses should be in the dv/dt filter. Note that dv/dt filter is L-RC-L (L is inductor, R is resistor and C is capacitor) type, as there will be losses in R, cooling is required. Therefore, it would be interesting to carry out research regarding the optimal losses with these solutions, but it is not within the scope of this thesis.

In high speed motor drive applications, the fundamental frequency of motor is considerably higher. For instance, in aircraft, it is $\geq$ 400 Hz. Higher frequency enables more power for the same motor volume and mass. Moreover, space and weight are predominant in such applications, and thus transformer and motor sizes can be reduced with high-frequency switching. As a consequence, the fuel consumption is reduced. SiC offers low switching losses, its characteristics remain almost unaffected by high temperatures, and heat can be readily extracted from the device, resulting in smaller cooling requirements and hence smaller and lighter converter.

6.2 Induction heating applications

High-frequency is the main driving force for induction heating applications, especially for the surface heating of relatively small parts or tubes with small diameters, where only a thin layer of the surface should be hardened or welded. In the 1.2–1.7 kV voltage class, Si-based power devices, particularly Si IGBTs, have been the primary choice for power electronic devices for the last several decades. In fact, Si MOSFETs exhibit high on-state losses in this voltage class, impeding them from being commercially available. Typically, the highest operating frequency of the state-of-the-art Si IGBTs for soft switched appli-

cations is 100 kHz [158]. However, when switched above a certain frequency, the on-state loss of a Si IGBT increases with an increase in frequency because the time required for it to return to deep saturation is not sufficient; therefore, dynamic conduction loss occurs [159]. For instance, in [160], it is shown that such a phenomenon already starts at frequencies above 30 kHz.

On the other hand, employing SiC, unipolar devices, such as power MOSFETs, is feasible in the same or higher voltage classes compared to those for Si. Indeed, SiC has a ten times higher breakdown electric field compared to Si, enabling devices with lower on-state losses, potentially lower by a factor of 1/500 to 1/1000, than those for Si at the same voltage ratings [161]. In addition, SiC unipolar devices do not exhibit a tail current. Nonetheless, the on-state losses are only dependent on the junction temperature and not on the switching frequency for these majority carrier devices [160], which are the obvious reasons for their preference in high-frequency soft-switched operations, such as high power LLC resonant type and SMPS applications.

Considering the facts about unipolar and bipolar devices discussed in the aforementioned paragraphs, this work investigates the switching performance of a 1.2 kV half-bridge SiC MOSFET module, which is different from the standard SiC MOSFET module, described in Section 6.2.1. There are several publications on loss measurements with the hard-switching of devices [16,90]; conversely, only a few publications exist regarding those with soft-switching [159,162,163]. This work examines the chosen device under both hard- and soft-switching conditions. Such a comprehensive investigation of the SiC MOSFET module has not, to the best of the author's knowledge, previously been presented. Illustrating the importance of switching slightly above the resonance, this task quantifies the soft-switching loss in a 78 kW full-bridge resonant inverter switched at approximately 200 kHz via the calorimetric method discussed in Section 6.2.2. Thereafter, a summary of the measurement results is presented along with a discussion in Section 6.2.4. Partly, this section compares the soft-switching energy loss measured by two methods: electrical method as presented in Chapter 3 and calorimetric method presented in this chapter.

6.2.1 Device under study

A 1.2 kV SiC MOSFET module, FCA150XB120, from Sanrex is the device under test (DUT) in this study. Both the MOSFET and the diode chips are fabricated on a single chip in this module, so this MOSFET is also called DioMOS, the concept of which was proposed in 2011 [164]. On the other hand, in a standard SiC MOSFET module, a MOSFET and anti-parallel diode chips are fabricated separately. Table 6.8 shows the major differences between the selected SiC MOSFET module and the standard SiC MOSFET module

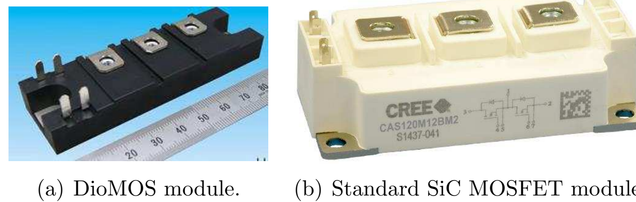
Table 6.8: Major differences between a SiC DioMOS and a standard SiC MOSFET modules.

Parameters / Module	SiC DioMOS FCA150XB120, Sanrex	Standard SiC MOSFET CAS120M12BM2, Wolfspeed
$V_{gs,th}$ (V)	4.5	2.6
$R_{DS,on}$ (mΩ)	5.3 @ I_{ds} = 150 A	13 @ I_{ds} = 120 A
$R_{th,jc}$ (°C/W)	0.120	0.125
Bonding	Solder	Wire
Module package size	30 × 93 × 14	62 × 106 × 30

(CAS120M12BM2) as specified in the respective data sheets [99, 123]. Note that each of these modules has a similar voltage and current ratings. Compared to Si MOSFETs, SiC devices have a relatively lower gate-to-source threshold voltage ($V_{gs,th}$). Although the input and output capacitances are lower in SiC, dv/dt is higher. Accordingly, sufficient charge can be coupled to the gate loop through the Miller capacitance during turn-off. If a negative gate voltage and a closed couple driver layout are not in place, this coupled charge can easily exceed the $V_{gs,th}$ boundary and cause a malfunction of the device. However, the data sheet of the DioMOS indicates relatively higher $V_{gs,th}$ compared to the standard SiC module, which is particularly attractive from an application standpoint. Author believe that once these devices are mass produced, the prices become moderate and all applications will consider using them. Currently, these devices are used in high-end applications, such as induction heating equipment, which is presented in this work.

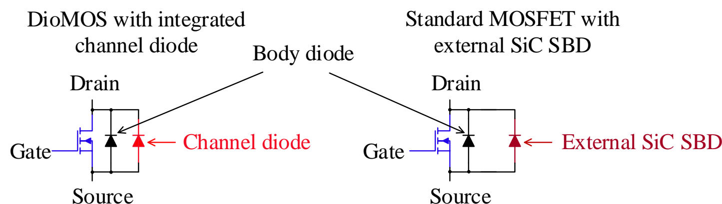
Also listed in Table 6.8 are $R_{DS,on}$, the on-state resistance, and $R_{th,jc}$, the junction-to-case thermal resistance of the MOSFET. In addition, the package size of the former module is smaller than that of the latter module because the external anti-parallel diode chip paired with the MOSFET chip is not necessary [164]. Moreover, the solder bonding technique is employed for the former module, whereas the technique for the latter is the wire bonding type. Fig. 6.7 shows photographs of the DioMOS and standard SiC MOSFET modules.

Fig. 6.8 (a) shows the circuit symbols for the DioMOS versus standard SiC MOSFET, and Fig. 6.8 (b) illustrates a cross-sectional view of the SiC DioMOS [165]. Compared to the standard vertical power MOSFET, the device structure is mostly similar in the DioMOS, except that the latter consists of an ultra-thin, highly doped n - type epitaxial layer and a highly doped p^+ - body region [164]. Different possible current paths are shown in Fig. 6.8 (b), where the arrows in solid blue, dashed red and dash-dot-dot black legends correspond to the MOSFET, channel-diode and body-diode current paths, respectively.

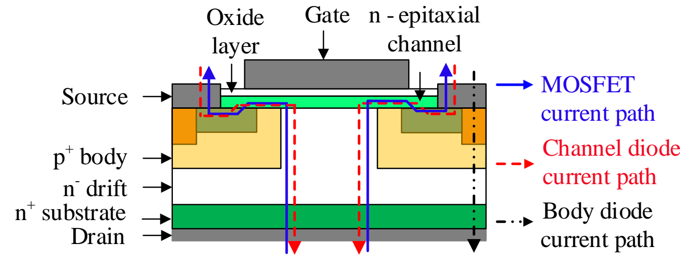


(a) DioMOS module. (b) Standard SiC MOSFET module.

Figure 6.7: Photographs of DioMOS and standard SiC MOSFET modules.



(a) DioMOS with an integrated channel-diode and standard MOSFET with an external SiC JBS. The channel-diode of the SiC DioMOS functions almost the same as the external SiC JBS.



(b) A cross-sectional view of the SiC DioMOS with the thin channel layer. It has a higher doping concentration of the channel layer and the body region compared to the standard SiC MOSFET.

Figure 6.8: (a) Circuit symbols of the DioMOS versus standard SiC MOSFET. (b) A SiC DioMOS structure showing the current paths through the MOSFET, channel- and body-diodes.

The current paths in the DioMOS, namely, the MOSFET and body-diode current paths, are exactly identical to those in the standard power MOSFET. Nonetheless, there exists an additional current path through the channel-diode in the DioMOS [164].

6.2.2 Calorimetric loss measurement in a full-bridge resonant inverter

In the following section, a typical system configuration of a voltage-fed series-resonant generator for induction heating application, as depicted in Fig. 6.9, is evaluated. Section 6.2.2.1 introduces the application along with its operating principle. Moreover, the importance of switching above the resonance is illustrated through current commutation sequences using MATLAB simulation in Section 6.2.2.2. Finally, in Section 6.2.2.3, the

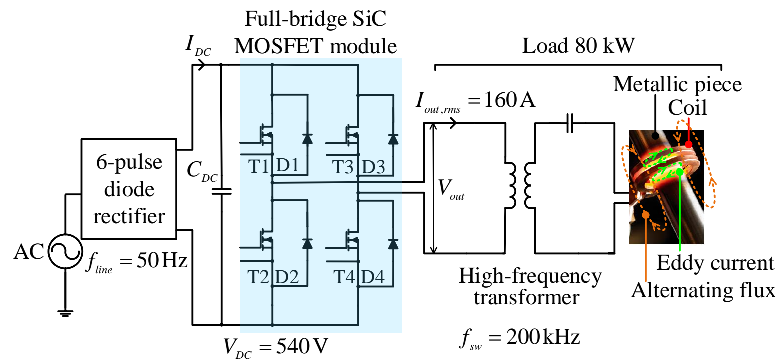


Figure 6.9: A complete schematic diagram of the experimental setup for an induction heating application. A compensation capacitor is in series with the load inductor (together they act as a current source) and is fed by the voltage source inverter. A metallic piece is placed inside the coil, encompassing the magnetic field without touching the coil as a contactless heating process. The input power of the inverter is measured in the DC-link (V_{DC} is measured by a precision voltmeter and I_{DC} by an LEM current sensor), and the loss is measured using the calorimetric method.

calorimetric loss measurement of the inverter part is presented to find the merits of using SiC MOSFETs for such an application.

6.2.2.1 System configuration and working principle

Before delving into the working principle of induction heating welders, it is important to discuss the system configuration considered in this study. As seen in Fig. 6.9, the voltage source inverter consists of two half-bridge SiC MOSFET modules with anti-parallel diodes, the DC power for which is fed through a six-pulse diode rectifier connected to a 400 V, 50 Hz power supply. The abbreviations used in the schematic are as follows. I_{DC}: DC-link current, V_{DC}: DC-link voltage, V_{out}: output voltage and I_{out}: output current. The load is composed of a compensating capacitor, a heating coil, and a metallic piece to be welded. Essentially, when the coil is subjected to a high-frequency sinusoidal current generated from the inverter, a time-varying magnetic field is induced in it. Consequently, the metal piece is heated by two physical phenomenons, eddy currents and magnetic hysteresis. Eddy currents oppose the magnetic field the work piece is subjected to and produces heating via the Joule effect, and this is the primary heat source. Furthermore, the magnetic field causes dipoles of the ferromagnetic material to oscillate when the poles change their polar orientation every cycle, thus creating additional heat due to friction, referred to as hysteresis loss. Depending on the application, the AC frequency is controlled to regulate the penetration depth into the work piece. SiC MOSFETs have potential to switch extremely fast and are very promising components for next-generation high-frequency induction heating generators. By utilizing the benefits of the skin effect, these generators can be used for surface heating of relatively small parts or tubes with small diameters, where only a thin layer of the surface should be hardened or welded.

6.2.2.2 Inductive ($f_{sw} > f_{res}$) versus capacitive ($f_{sw} < f_{res}$) mode switching - Consequence in terms of loss

When an inverter is switched at resonant frequency (f_{res}), the maximum power can be transferred. Nevertheless, the real-world system has a very low chance to operating at perfect resonance because the focal point can shift due to small changes in the load or subtle inaccuracies in the control parameters. As a consequence, in normal operation, the inverter works slightly above or below the resonance. Therefore, this section aims to study the sequence of the commutation process during the inductive (above resonance) versus capacitive (below resonance) switching modes. Thus, the full-bridge inverter configura-

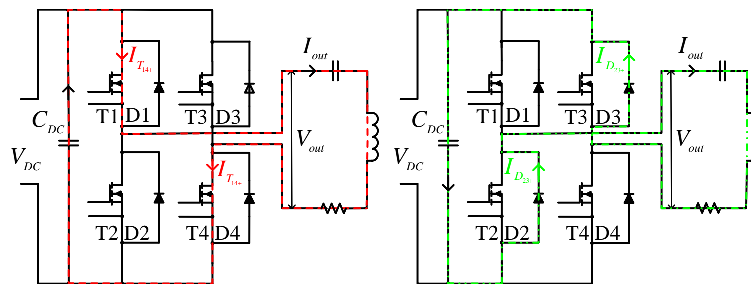
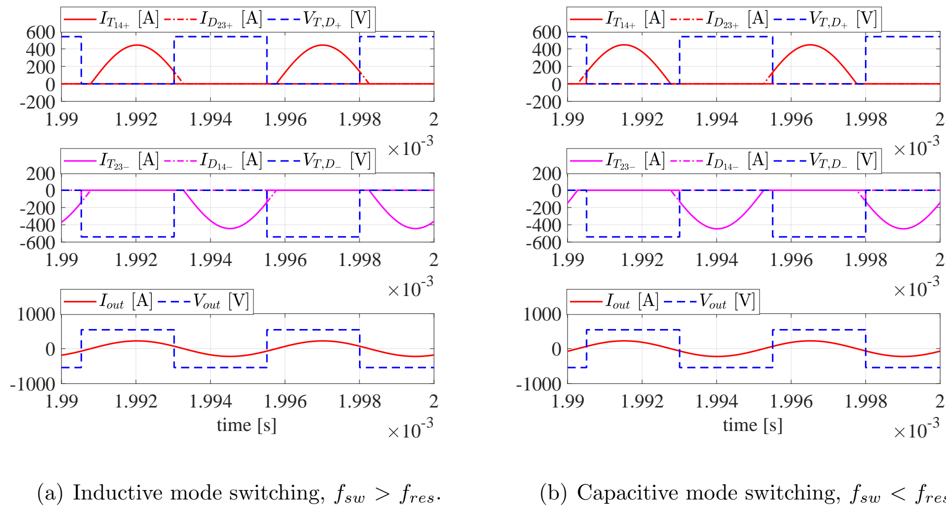


Figure 6.10: Exemplification of the current flow during the positive polarity of the load current.

tion, shown in Fig. 6.9, is simulated in MATLAB. The inputs for simulation are as follows: $V_{DC} = 540$ V, the resistance of the metallic piece is chosen such that $I_{out,rms} = 160$ A, and the inductance of the coil and compensating capacitance are tuned to acquire the desired f_{res}. Fig. 6.10 shows the current flow during the positive polarity of the load current, where the current through transistors T1 and T4 is labelled as $I_{T_{14+}}$ and that through D2 and D3 is depicted as $I_{D_{23+}}$. In a similar manner, $I_{T_{23-}}$ and $I_{D_{14-}}$ are the currents in the respective transistors and diodes during the negative polarity of the load current, as symbolized in the simulated waveforms presented in Fig. 6.11.

The plots show that while operating above the resonance, Fig. 6.11 (a), diode turn-on and switch turn-off feature hard-switching, while diode turn-off and switch turn-on exhibit soft-switching. While operating under the resonance, Fig. 6.11 (b), on the other hand, the converse of the former sequences holds true. The forward-recovery of the diode is significantly smaller compared to the reverse-recovery, so switching slightly above the resonance is preferable (to avoid turn-off losses associated with the diodes), and this approach is adopted in this work.



(a) Inductive mode switching, $f_{sw} > f_{res}$.

(b) Capacitive mode switching, $f_{sw} < f_{res}$

Figure 6.11: Illustration of inductive and capacitive switching modes in a series-resonant inverter. In the former mode, the turn-on of diodes and turn-off of switches are hard, but the turn-off of diodes and turn-on of switches are soft. However, the converse is true in the latter mode, leading to a higher switching loss, particularly that from the reverse-recovery of diodes. This is why the former mode is adopted in this work over the latter.

6.2.2.3 Laboratory measurements

First, it is essential to highlight that a low-inductive switching loop is the key factor for utilizing the fast switching potential of a SiC MOSFET and maintaining the safety, particularly during failure. Hence, a DC-link busbar is constructed with a stripline-terminated capacitor, as depicted in Fig. 6.12. The switching frequency is 187 kHz (for this case), and the inverter losses are measured calorimetrically at approximately 78 kW of input power. Fig. 6.13 displays the oscilloscope waveforms with the output voltage

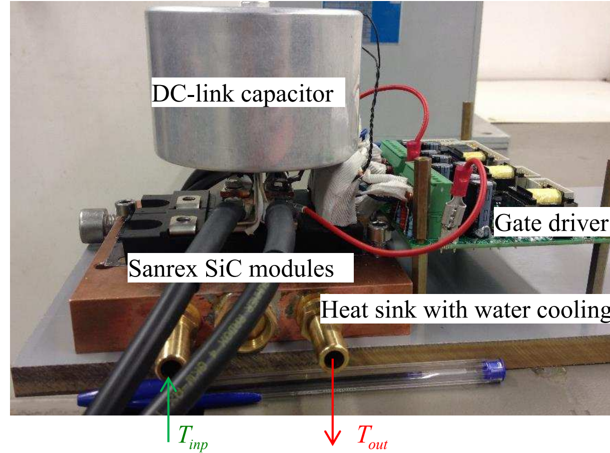


Figure 6.12: Part of the experimental setup showing a low-inductive busbar connection for a full-bridge inverter with a water-cooled heat sink for calorimetric loss measurement.

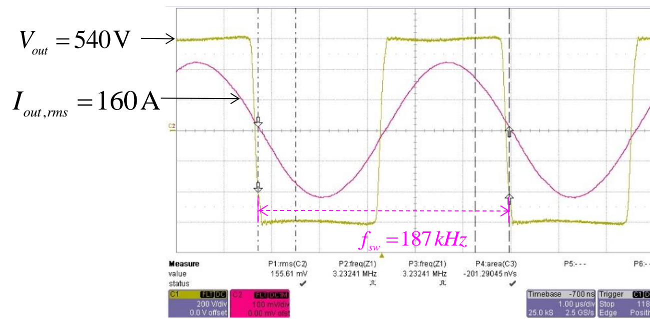


Figure 6.13: Illustration of a sample of inverter output voltage and current with a full PWM control scheme. The gate voltage is + 20 V / - 5 V, and the gate resistance is 2.85 Ω.

and current. In the calorimetric method, the inverter is placed over the water-cooled heat sink, assuming that all the heat dissipated by the inverter is removed through the cooling system. When switched just above the resonance, the turn-on loss is absent (details explained in Section 6.2.2.2), thus the total loss comprises the turn-off switching loss and conduction loss. Thereafter, by subtracting the conduction loss from the total loss, the turn-off loss is computed. Various electrical parameters, namely, I_{DC}, V_{DC}, and $I_{out,rms}$, thermal parameters, namely, the inlet and outlet water temperatures (T_{inp} and T_{out}, respectively), and the water mass (m) are monitored and listed in Table 6.9.

Table 6.9: Summary of the measured parameters at 78 kW input power.

Measured parameters	I_{DC} (A) (A)	V_{DC} (V)	$I_{out,rms}$ (A)	T_{inp} (°C)	T_{out} (°C)	m (g/min)
Values	142.8	545	160.3	15	17.5	2.990

Table 6.10 presents a summary of the calculated parameters. Using (7.4)–(7.10), the corresponding parameters in each row are computed. The abbreviations used in the equations are as follows: P_{inp}: input power of the inverter, Q: total power loss of the inverter, s: specific heat capacity of water (4.186 $J/g/$°C), η: efficiency of the inverter, P_{cond}: conduction power loss per switch, P_{sw}: switching power loss per switch, $E_{off-spec-calori}$: specific turn-off energy loss per switch, and ΔT: temperature rise from the junction to the case. The measured efficiency of the inverter is approximately 99.33%, the conduction loss per switch is 89.93 W with $R_{DS,on}$ being 7 mΩ (at the operating temperature), and the temperature rise is 15.64 °C (at the given $R_{th,jc}$ of 0.120 °C/W). It is worth mentioning that $E_{off-spec-calori}$ is computed for a drain-source current of 60 A, which is the turn-off switching current in a full-bridge.

Table 6.10: Summary of the calculated parameters for approximately 78 kW of input power.

Calculated parameters	Values	Equations	Eq. no.
P_{inp} (kW)	77.82	$P_{inp} = V_{DC} \cdot I_{DC}$	(7.4)
Q (W or J/s)	521.5	$Q = m \cdot s \cdot (T_{out} - T_{inp})$	(7.5)
η (%)	99.33	$\eta = \frac{P_{inp} - Q}{P_{inp}}$	(7.6)
P_{cond} (W)	89.93	$P_{cond} = \left(\frac{I_{out}}{\sqrt{2}}\right)^2 \cdot R_{DS,on}$	(7.7)
P_{sw} (W)	40.44	$P_{sw} = \frac{Q}{4} - P_{cond}$	(7.8)
$E_{off-spec-calori}$ (μJ/A)	3.60	$E_{off-spec-calori} = \frac{P_{sw}}{f_{sw} \cdot I_{ds}}$	(7.9)
ΔT (°C)	15.64	$\Delta T = R_{th,jc} \cdot \frac{Q}{4}$	(7.10)

6.2.3 Accuracy analysis of calorimetric efficiency measurement

As ΔT and m in (7.5) can be the sources of inaccuracies in the calorimetric loss measurement method, the inlet and outlet temperatures are measured using an analog thermometer with ± 0.05 °C accuracy. For the water flow measurement, first, the outlet water is run into a bucket over a specified time (2 minutes), second, the water in the bucket is measured via a postal weight with 0.01 kg resolution. Thus, the volumetric flow is calculated by dividing the weight of water and measurement time. Note that the water flow is controlled by connecting the inlet of heat sink directly to the water faucet (the temperature of water is less than room temperature, RT). The air temperature close to the heat sink is measured by pt100 with a resolution of < 0.01 °C and is found to be $\leq$ RT all the time.

For the highly efficient converters, it is challenging to achieve an accurate ΔT measurements with standard flow rates with those used in industrial applications. Therefore, to maintain an adequate measurement accuracy, ΔT should be kept high, thus it is essential

to maintain a low water flow rate without sacrificing a good heat transfer coefficient from water to heat sink. This is achieved via smaller cross-sectional area of cooling channel in heat sink, which will basically aid increasing the speed of water. Of special note is that the measured data is an average of 10 consecutive recordings for avoiding possible errors.

6.2.4 Discussion and summary

Table 6.11 summarizes the specific turn-off energy loss per switch measured by two different methods: calorimetric versus electrical. Note that the listed values of specific energy loss are measured at the switching current of 60 A, and the gate driving waveforms are maintained at similar levels in each case for a balanced comparison. The specific energy loss is lower by a factor of 0.9 in case (a) compared to that in case (b), the reasoning of which is explained below.

Table 6.11: Summary of the specific turn-off loss measurements in three different topologies and normalization with regard to electrically measured loss in a half-bridge resonant inverter.

Case	Method	Specific energy loss (μJ/A)	Factor with respect to (b)
(a)	Calorimetric	$E_{off-spec-calori} = 3.60$	0.9
(b)	Electrical	$E_{off-spec-elec} = 3.99$	1.0

As can be seen from Table 6.11, the specific energy loss measured via the electrical method is higher by 9.7% compared to that measured via the calorimetric method. For the sake of explaining this difference, the turn-off process and the measurement method should first be clarified. In Fig. 3.6, Chapter 3, the current routing during the turn-off process is shown. In the electrical loss measurement method, the drain current and the drain voltage are measured using high bandwidth probes and an oscilloscope. After compensating for possible probe delays, these collected switching waveforms are multiplied and integrated over the defined time limits to obtain the switching energy loss in MATLAB. Looking closely into the turn-off process, the drain current used for the loss calculation is the sum of the following two currents: (a) the current passing through the MOSFET channel, and (b) the current diverted for charging the output capacitance (C_{gd} + C_{ds}). However, the real power loss in the MOSFET is caused by the channel current only because the current that charges the device output capacitor does not generate any Joule heating and should not be accounted for as a part of the turn-off switching loss. The MOSFET channel current cannot be measured separately in the lab, so the electrical approach to loss measurement overestimates the switching energy loss, explaining the reason for the loss differences in question. This is also illustrated through simulation using a physically based device modelling approach in [166,167]. In such a simulation, there is the possibility to measure the current shared by the MOSFET channel and the output capacitor independently.

The major conclusions derived from this work are summarized below.

1. A resonant full-bridge inverter with SiC MOSFETs yielded an efficiency of approximately 99.3% at a switching frequency of roughly 200 kHz using a calorimetric loss

measurement method. For induction heating application, SiC MOSFETs not only fulfil the application demand but also save energy, thus enabling two benefits.

2. A simplified measurement setup comprising a half-bridge SiC MOSFET, split DC-link capacitors and an LC load is used for measuring the turn-off loss via an electrical method in Chapter 3, which is found to be 9.77% higher compared to that obtained using a calorimetric method. Two possible reasons for these differences are as follows: First, the drain current through the MOSFET during the electrical measurement is smaller than the measured value because a part of the measured current is charging the MOSFET output capacitor. Second, factors causing losses, for example, forward-recovery of freewheeling diodes, layouts, and wires, are neglected. However, this comparison can also be taken as a verification between the electrical and calorimetric method of loss measurements as the difference is $< 10\%$.

6.3 Power factor correction applications

Rectifiers for AC-DC conversion are widely used in many applications, such as switched-mode power supplies (SMPSs), pulse width modulated (PWM) motor drives, and uninterrupted power supplies (UPSs), which result in non-sinusoidal input currents with large harmonic components leading to a poor power factor [1, 168, 169]. This eventually entails myriad problems, for instance, interference with the communication circuits and other equipment; losses and heating of the capacitors, motors, and transformers; and an accelerated ageing of their insulation [170–172]. To improve the power quality, line harmonic regulations, namely, EN 61000-3-2 [173] and IEEE Std. 519-2014 [174], are established. As an example, for the bus voltage of ≤ 1 kV at the point of common coupling (PCC), the IEEE Std. 519-2014 recommends that the individual and total harmonic distortion be $\leq 5\%$ and $\leq 8\%$, respectively [174]. To comply with these standards, an active power factor correction (PFC) circuit must be used [1, 169]. However, this solution leads to an increased pollution within the 20 kHz to 1 GHz range because it involves a power electronic converter [175]. Therefore, this active PFC must also satisfy the standard for a high-frequency range; i.e., conducted (150 kHz to 30 MHz) and radiated (30 MHz to 1 GHz) noises must meet the IEC CISPR 16-1-2 regulation [176]

Aside from meeting the mandatory line harmonic requirements, as mentioned above, AC-DC power converters also require satisfying efficiency-related needs, which are enforced owing to economic and environmental concerns by various programs and organizations, such as the 80 PLUS incentive program [177], the U.S. Environmental Protection Agency's (EPA) Energy Star [178], and the Climate Saver Computing Initiative (CSCI) [179]. As an example, the 80 PLUS certification requires an efficiency of $\geq$80% at 20%, 50%, and 100% of the rated load [177].

Comprehensive research into an electromagnetic interference (EMI) analysis has been carried out [180–186]. In [180], two separate heat sinks are proposed to achieve a better EMC performance of SiC JFET-based motor drives. Oswald *et al.* [181] compared the spectra of SiC MOSFET/SiC, SiC MOSFET/Si, and Si IGBT/Si diodes based on switching waveforms obtained from a double-pulse tester, which revealed that SiC MOSFETs generate higher EMI noise than Si IGBTs within a frequency range of 2–50 MHz. Furthermore, the reverse-recovery effect of SiC versus Si diodes was studied in [182], in which it was concluded that parasitic oscillation during switching transients magnifies the EMI

noise within the corresponding ringing frequency range in the spectra. In addition, the CM choke sizing for 20 kHz versus 200 kHz drives [183], the suppression of EMI using random modulation techniques [184], and optimal EMI filter designs [185, 186] have been reported.

To minimize the conduction loss of the diode bridge, various PFC topologies, such as a boost bridgeless PFC, totem-pole bridgeless PFC, and numerous control strategies have been proposed and analyzed [187–193]. Since the commercialization of an SiC Schottky barrier diode (SBD) in 2001, many authors have compared the efficiency gain brought about by SiC SBD over a Si ultra-fast boost diode, primarily focusing on minimizing the reverse-recovery loss associated with it [194–200]. A Si super junction MOSFET and SiC SBD were long considered ideal solid-state devices [201–205] until the commercialization of an SiC MOSFET in 2010. For this application, many publications have reported the use of an SiC SBD and SiC MOSFET [206–212]. As the best example, a 1 kW SiC-based PFC was reported, which resulted in an efficiency of 97% when switched at 100 kHz [208].

However, in this study, a 1 kW SiC-based PFC converter is designed, developed, and evaluated using the best available low-loss SiC MOSFET and SiC diode. With the goal of fully exploiting a high switching speed and low-loss capability of SiC devices, a low-inductive and capacitive printed circuit board (PCB), along with an external gate drive resistance of 0 Ω, is employed. Initially, through low-inductive measurement connections, a clean, fast switching of the chosen state-of-the-art SiC devices is accomplished. An efficiency of 97.2% is demonstrated when switched at 250 kHz. Moreover, EMC compliance was investigated for two different switching frequencies, namely, 66 and 250 kHz, the results of which revealed that the same filter size satisfies the CISPR Class B conducted EMI regulations with excellent margins. Overall, to minimize the EMI at the source, a clean switching approach of an SiC is required; to obtain the highest efficiency, a clean, fast switching of an SiC is indispensable; and to evaluate the converter EMI, a fast and high-frequency switching of SiC is the most interesting condition (the EMI is significantly aggravated using fast- and high-frequency switching). In the present study, a PFC rectifier was evaluated under such conditions, thus extending the research in this regard.

The remainder of the chapter is organized as follows. A description of the converter and its specifications are presented in Section 6.3.1. Following this, the PFC converter loss evaluation via circuit simulation can be found in Section 6.3.2. Section 6.3.3 focuses on the circuit design considerations for the clean switching of SiC devices through the design and measurement of a conventional PFC converter prototype. The experimental results are presented in Section 6.3.4. Finally, Section 6.3.5 highlights the major conclusions of the present study.

6.3.1 Converter description and specification

A conventional or classical PFC circuit consists of an input EMI filter, diode bridge, and boost converter, as shown in Fig. 6.14. The primary objective of this circuit is the active shaping of the input current (i_s), allowing it to be in phase with the input AC voltage (v_s), thus minimizing the harmonic distortion. The current paths when the PFC operates in a continuous conduction mode (CCM) are also illustrated in Fig. 6.14, which shows that the reverse current resulting from parasitic capacitance within the diode contributes to the turn-on switching loss in the MOSFET apart from the switching loss in itself.

Table 6.12 shows the specifications of the converter. The input voltage (v_s) has a

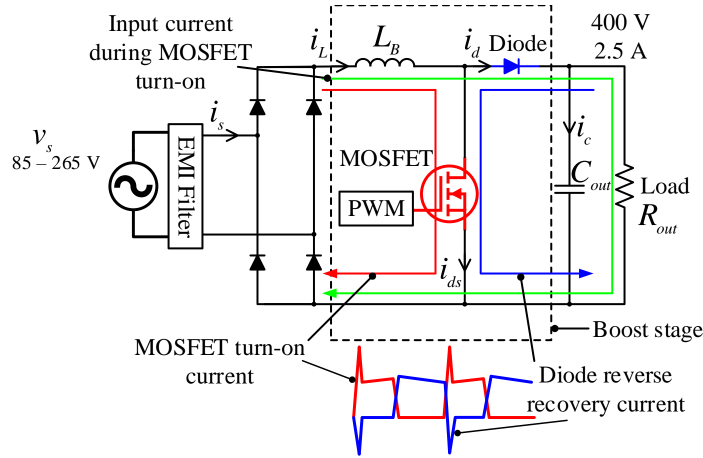


Figure 6.14: Schematic diagram of an active PFC boost converter, illustrating the current paths for the MOSFET and diode in a CCM operation. During the boost diode turn-off and boost MOSFET turn-on, the reverse-recovery current in the diode not only contributes to the switching loss in itself but also to the turn-on switching loss in the MOSFET, which demands larger die devices to meet the efficiency and thermal specifications when using a diode with a large recovery charge.

range ($v_{s,min}$–$v_{s,max}$) of 85–265 V. The line frequency (f_{line}) is 50/60 Hz, the output voltage (v_{out}) is 400 V, and the output power (P_{out}) is 1 kW. The boost inductor (L_B) is specified such that the ripple current (Δi_L) is 30% at a low-line voltage (85 V) through a circuit simulation in MATLAB. Alternatively, the simulated value of L_B is assured through an analytical expression given in (C.1) [see Appendix C]. The output capacitor (C_{out}) was designed to handle the double-line frequency peak-to-peak (pp) ripple voltage ($\Delta v_{out} = 10\ V_{pp}$) and meet the hold-up time requirement ($t_{hold} = 16.6$ ms at the minimum

Table 6.12: Specifications of PFC boost converter.

Parameters	Specifications
Input voltage ($v_{s,min}$)–($v_{s,max}$)	85–265 V
Line frequency (f_{line})	50/60 Hz
Output voltage (v_{out})	400 V
Output power (P_{out})	1 kW
Switching frequency (f_{sw})	250 kHz
Boost inductor current (Δi_L)	30% @85 V, 1 kW, 250 kHz
Output voltage ripple (Δv_{out})	10 V_{pp}
Hold-up time (t_{hold})	16.6 ms @ $v_{out,min}$ = 350 V
EMI standards	CISPR 11 Class B
Efficiency regulations	80 PLUS

Table 6.13: Chosen components with their part numbers and specifications. The on-state parameters associated with the diode, V_{FO} and R_d, and MOSFET, $R_{DS,on}$, are taken at 125 °C [82,86].

Components	Part number	Specification
Bridge diode	GSIB2580	V_{FO} = 0.98 V, R_d = 22 mΩ
L_B	CS330060	sendust, DCR = 80 mΩ
MOSFET	C3M0065090D	$R_{DS,on}$ = 82 mΩ
Boost diode	SCS220AE2	V_{FO} = 0.8 V, R_d = 34 mΩ
C_{out}	B43508A5567M062	ESR = 220 mΩ @100 Hz

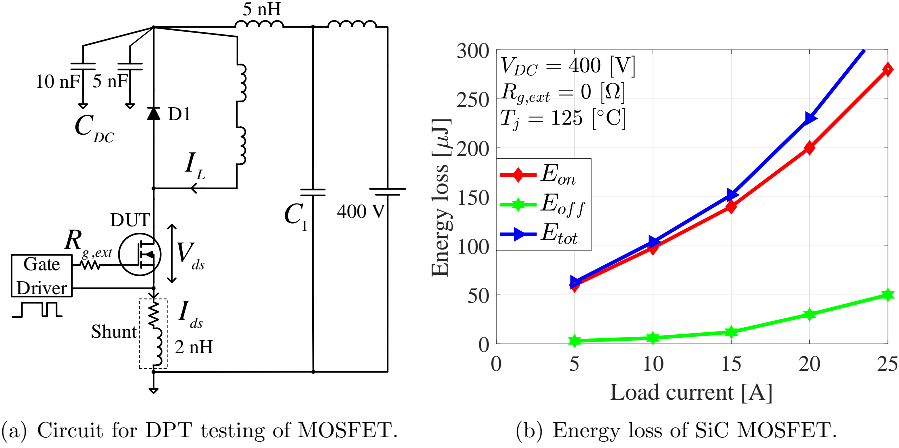
output voltage, $v_{out,min}$ = 350 V). Both the simulation and analytical approaches are used to guarantee the designed size. See the analytical expression used for C_{out} in (C.2) [See Appendix C]. Furthermore, the switching frequency was detected by the maximum possible value that a commercially available analog controller IC could offer. The controller IC, UCC28180, could operate in CCM mode with user programmable switching frequency up to 250 kHz.

Table 6.13 shows the part number and specifications of the components, particularly chosen with the goal of maximizing the efficiency in a prototype PFC converter. The bridge diodes are based on Si technology, with the lowest V_F of the commercially available devices. Using an off-the-shelf single sendust core [213] with 85 turns of the copper wire, a boost inductor is produced that provides an inductance of approximately 424 μH at zero bias and a DC resistance (DCR) of 80 mΩ. A single-layer winding approach with multiple parallel wires is used for reducing the AC losses. The boost MOSFET and diode are based on SiC and chosen based on state-of-the-art low-loss devices. An effective series resistance (ESR) of C_{out} is 220 mΩ. The on-state parameters associated with the diode, namely, the forward voltage drop (V_{FO}) and on-state resistance (R_d), and with the MOSFET, namely, on-state resistance ($R_{DS,on}$), are taken at 125 °C, whereas those related to the inductor and capacitor are provided for 25 °C in Table 6.13, which are the inputs for the loss calculation of the converter.

6.3.2 PFC converter loss evaluation via circuit simulation

The same hardware setup as presented in Chapter 5, Fig. 5.3 is used for DPT measurements of the chosen devices, a simplified schematic diagram of which is shown in Fig. 6.15 (a). The switching energy loss for the chosen MOSFET at V_{DC} of 400 V and a junction temperature (T_j) of 125 °C is shown in Fig. 6.15 (b), which is also a look-up table input for a circuit simulation of a PFC converter.

Using MATLAB Simulink, the total converter loss is simulated, the inputs for which are the switching losses obtained from the laboratory measurement and the conduction losses from the data sheet. These data are used as look-up tables or polynomial functions based on a curve fitting. To compute the losses associated with the rectifier bridge, the Si diodes on-state losses, the output capacitor ESR, and the boost inductor copper loss are used as input into the simulation model. As a cross-check, conduction losses are calculated using the simple analytical expressions provided in the Appendix in (C.3), and



(a) Circuit for DPT testing of MOSFET.

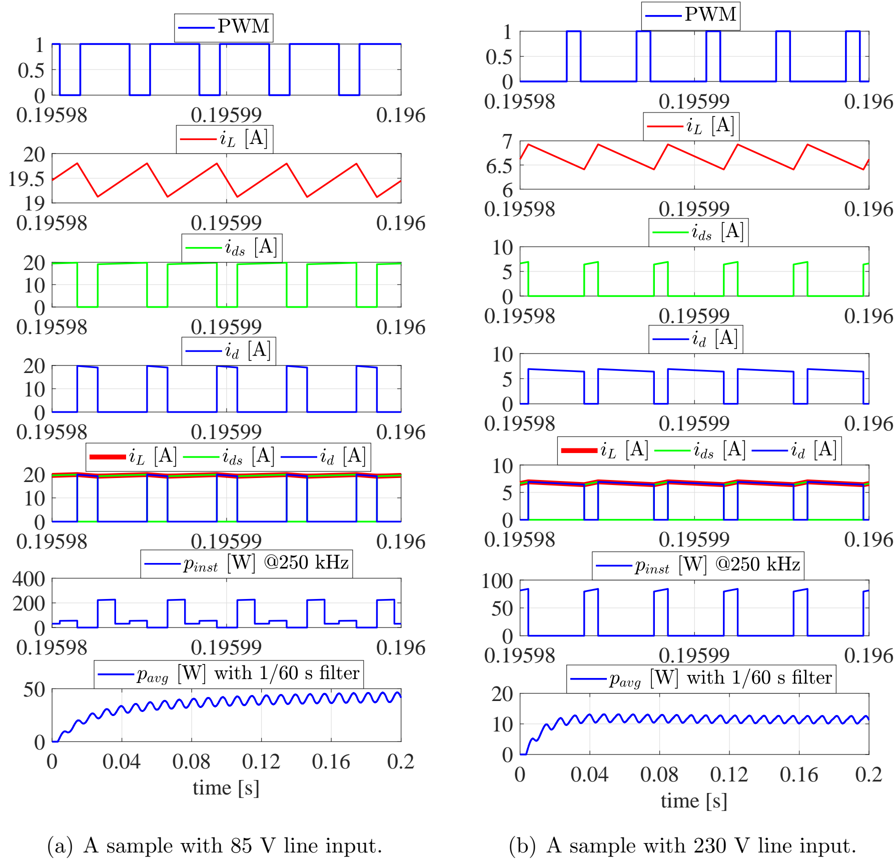
(b) Energy loss of SiC MOSFET.

Figure 6.15: (a) An inductive load circuit for a hard-switching test of the SiC MOSFET. An external gate resistor ($R_{g,ext}$) is used to regulate the dv/dt and di/dt of the DUT. (b) Switching energy loss versus load current of the chosen SiC MOSFET at a V_{DC} of 400 V and a T_j of 125 °C, which is a look-up table input for a circuit simulation of a PFC converter.

are found to be in accordance with the simulations. Regarding the switching loss, the look-up table method implemented in this study is the same as that used in Section 6.1, which calculates the switching power loss by counting the number of switching events during the fundamental cycle of the input.

Fig. 6.16 (a), (b) illustrates the simulated waveforms of the PFC converter, such as the PWM input into the MOSFET, the current through the boost inductor (i_L), the switching current in the boost MOSFET (i_{ds}), the switching current in the boost diode (i_d), the instantaneous power loss of the MOSFET (p_{inst}), and the average power loss of the MOSFET (p_{avg}) with a filter of 0.01 s (1/60, with 60 Hz being the fundamental frequency). The sample plots are given for a switching frequency of 250 kHz. Apparently, when the MOSFET is in an on-state, i_L increases, and when the MOSFET is in an off-state (namely, when the diode conducts), i_L decreases. At a low input voltage (85 V), the diode has a shorter duty cycle than the MOSFET, whereas the opposite holds true at a high input voltage, which is why the diode with a low V_F is desired for achieving a low loss, particularly at a low line voltage. The last signal in the sub-plot is the average power loss over the SiC MOSFET, which includes the conduction and switching loss. Note that this particular sub-plot has a different time range (0–0.2 s) than the other sub-plots, which has deliberately been chosen to observe the average power loss characteristics of the SiC MOSFET over a longer time frame.

The detailed conduction loss breakdown for different line inputs, namely, 85, 115, and 230 V, is shown in Fig. 6.17 (a), and the switching losses of the boost diode and MOSFET at these line inputs are shown in Fig. 6.17 (b). For the same output power (1 kW), higher losses are incurred at a low line voltage compared to a high voltage, the primary reason for which is the higher current at the low line compared to that at the high line. The capacitive charge is low for the SiC diode and almost independent of di/dt, the forward current, and the temperature. Hence, the switching loss of the SiC Schottky diode is

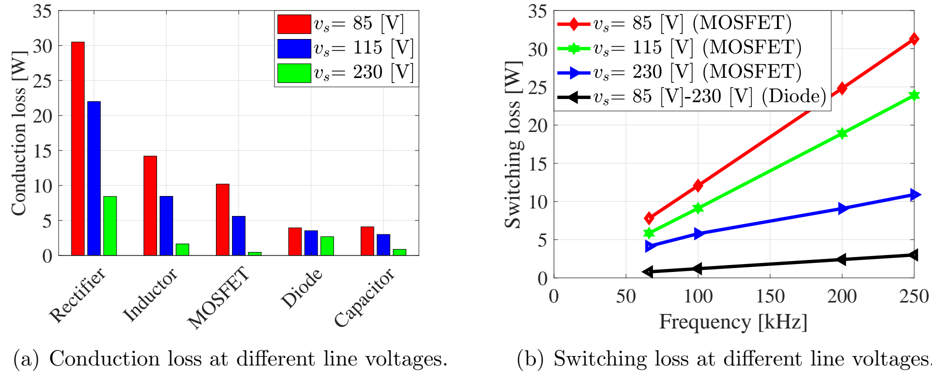


(a) A sample with 85 V line input.

(b) A sample with 230 V line input.

Figure 6.16: Sample plots at different locations in the circuit (Fig. 6.14) at two different values of v_s, namely, 85 and 230 V, when switched at a f_{sw} of 250 kHz. At a low input voltage (85 V), the diode has a shorter duty cycle than the MOSFET compared to that at a high input voltage, and thus a diode with a low V_F is desired for achieving a low loss, particularly at 85 V. In a 1 kW PFC boost converter, the total MOSFET loss reaches approximately 40 W at 85 V and 9 W at 230 V when switched at 250 kHz. It should be noted that the time scale of the last sub-plot differs (0–0.2 s) compared to those of the other sub-plots, and thus the pattern of p_{avg} can be seen over the full simulation time.

taken as a constant for a given output voltage of 400 V. Fig. 6.18 illustrates the total conduction, total switching, and their summation, P_{cond}, P_{sw}, and P_{tot}, respectively, over the entire load range at 250 kHz for two different line voltages. As shown, P_{cond} is lower over the entire load range for a v_s of 230 V, whereas the opposite is true for a v_s of 85 V.



(a) Conduction loss at different line voltages.

(b) Switching loss at different line voltages.

Figure 6.17: Illustration of conduction and switching loss breakdown at different input voltages, namely, 85, 115, and 230 V, at a 100% output power. (a) The bridge rectifier has the largest part of the conduction losses compared to the other components in the circuit. Simultaneously, the conduction losses are more pronounced at lower line voltages compared to those at higher line voltages. (b) The switching losses imposed by the SiC MOSFET are larger compared to those imposed by the SiC diode. Of special note is that the switching losses of the SiC diode are independent of the load current, hence giving the same results at different line voltages, but the losses increase with the increase in voltage in the SiC MOSFET under similar circumstances.

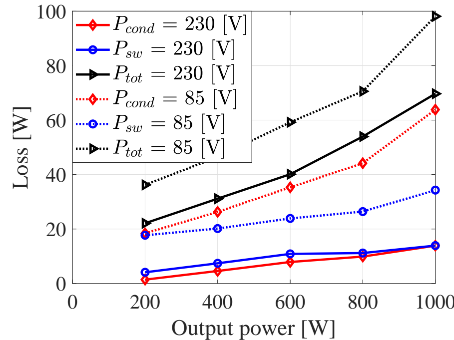


Figure 6.18: Plots illustrating the conduction loss (P_{cond}), switching loss (P_{sw}), and total loss (P_{tot}) at 250 kHz. Clearly, P_{cond} is lower throughout the entire load for a v_s of 230 V, whereas the opposite is true for a v_s of 85 V.

6.3.3 Circuit design and layout considerations of PFC rectifier

This section describes the circuit design and layout considerations in a PFC rectifier prototype for achieving the clean switching of an SiC MOSFET and SiC diode. In addition,

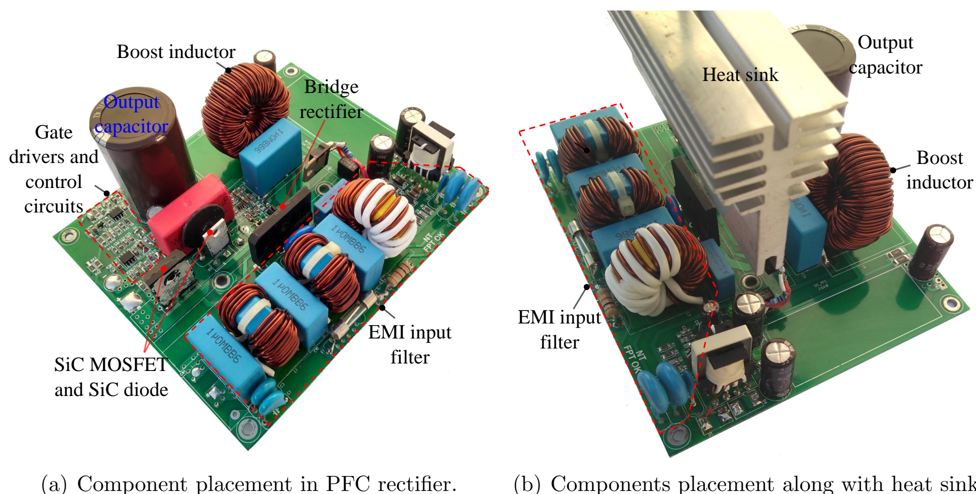
brief descriptions of the input EMI filter, boost inductor, gate driver, and PFC controller are included. A full schematic diagram of the prototype is shown in Fig. C.1 and a complete component layout along with PCB routing is shown in Fig. C.2 in Appendix C.

6.3.3.1 Circuit layout considerations

With the objective of reducing the oscillations in the switching transients, the electric and magnetic field generations are minimized for controlling the generation of the EMI at the source. High-voltage switching traces are kept as small as possible to minimize the electric fields. The heat sink is connected to the return such that it does not act as a voltage-driven antenna. The gate drive track inductance is minimized. The switching current conductors are balanced and run opposite to each other to minimize stray inductance. Guard rings are used for the current sense signals. A ground plane was used for the control circuits, the PCB routing of which is labelled in Fig. C.2 [see Appendix C]. In addition, decoupling capacitors are used as closely as possible to the switching nodes.

6.3.3.2 Hardware setup of a prototype PFC rectifier

An image of the implemented hardware prototype with two different side views delineating the placement of different components is provided in Fig. 6.19. A PFC controller UCC28180D from Texas Instruments is used with the switching frequency set to 250 kHz. Given the high switching speed capabilities of SiC devices, a higher switching frequency was possible without compromising the efficiency and achieving a dramatic size and cost reduction of the PFC boost inductor. A photograph showing the size difference in an inductor when switched at 66 kHz versus 250 kHz is provided in Fig. 6.20. The SiC MOSFET was driven by a +2.5/-5 A driver that can generate an approximately +18/-5 V drive voltage.



(a) Component placement in PFC rectifier. (b) Components placement along with heat sink.

Figure 6.19: Photographs of the prototype PFC converter with two different side views showing the placement of different components.

(a) 66 kHz. (b) 250 kHz.

Figure 6.20: Switching at 66 kHz requires 2 × stacked sendust core, CS358060, with 70-turns giving 565 μH, while at 250 kHz, only 1 × stacked sendust core, CS330060, is sufficient leading to dramatic reduction in size of inductor.

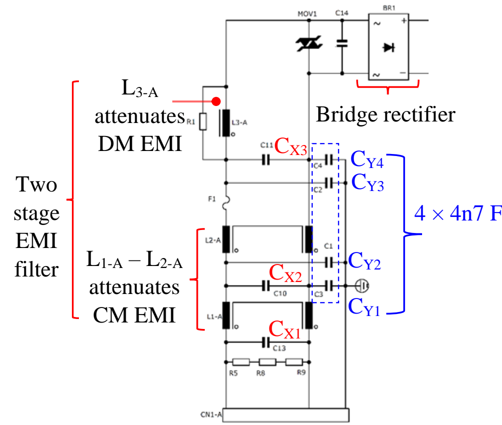


Figure 6.21: Schematic diagram showing the two-stage EMI filter, the first stage consisting of inductors, L_{1-A} and L_{2-A}, attenuating the CM EMI, and the second stage with L_{3-A} attenuating DM EMI. Capacitances C_{Y1}–C_{Y4} (nF range) primarily serve as a CM filter; and C_{X1}–C_{X3} (μF range), as a DM filter.

A two-stage EMI filter, as shown in Fig. 6.21, was designed and implemented. The first stage consisting of the inductance, L_{1-A}, L_{2-A}, and the capacitances, C_{Y1}–C_{Y4}, attenuates a common-mode (CM) EMI. The second stage incorporating the inductance, L_{3-A}, and capacitances, C_{X1}–C_{X3}, attenuates a differential-mode (DM) EMI. The procedure followed in the design of the CM and DM filter is enumerated below.

1. Because the switching transients are the sources of the EMI, the measured DPT waveforms (time domain) are taken as an input to plot the corresponding frequency domain equivalent to a Fourier transform in MATLAB. This measured original noise is compared with the CISPR limits. Selecting the filter topology, as shown in Fig. 6.21, the corner frequency is calculated such that the attenuation satisfies the limit with an extra 6 dB safety margin.

2. First, the CM capacitances, C_{Y1}–C_{Y4}, are limited based on regulations indicating that the current-to-ground must not exceed 3 mA at 50/60 Hz. Accordingly, CM inductances are calculated using the resonance principle at the computed corner frequency.

Then, the CM filter is tested in the MATLAB Simulink model of the PFC converter to check the defined 3 mA leakage current limit.

3. Because the leakage inductance of the CM choke, as well as the boost inductance of the PFC stage, help minimize the DM noise, a fairly low DM inductance is selected, namely, 1–4% of the CM inductance. Again, using the resonance equation, the CM capacitance is computed.

4. The designed filter was simulated in LTSpice employing realistic spice models of the circuit components, including SiC MOSFET, SiC diode, and EMI filters to check the EMC compliance before building the EMI filter in a laboratory.

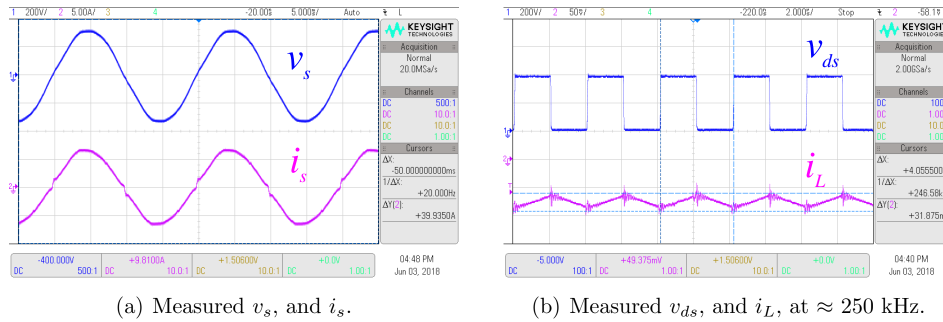
Table 6.14 shows the designed EMI filter components for the prototype.

Table 6.14: EMI filter specifications.

C_{Y1}–C_{Y4}, CM capacitances, Ceramic, Class X1/Y2 4 × 4n7F, P10 mm
L_{1-A}, L_{2-A}, CM chokes, EPCOS-TDK, R25 Ring core T38 material, 19 turns per coil, wire diameter 1.219 mm 2 × 3.6 mH ± 25% @ 1 kHz
L_{3-A}, DM chokes, Micrometal, T106-26 core, 36 turns wire diameter 1.422 mm, 1 × 120 μH ± 10% @ 1 kHz
C_{X1}–C_{X3}, DM capacitances, MKR, EPCOS, × 2 Class 3 × 1μF, 305 V, P22.5 mm

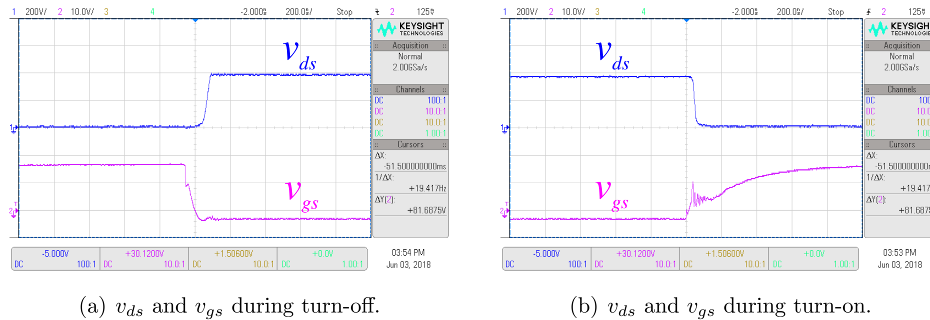
6.3.4 Experimental results

In this section, the efficiency and EMI evaluation of the prototype PFC converter are presented. The higher the ripple current in the boost inductance, the higher the AC losses in it. As a consequence, higher is the EMI because of the potential higher radiations of magnetic field. In this work, the SiC devices are switched with 0 Ω gate resistance together with the low parasitic design approach (the highest possible dv/dt and di/dt) with the aim of maximizing the efficiency and measuring the worst case EMI. However, slowing the SiC MOSFETs would potentially minimize EMI noises with the penalty of higher switching losses. Fig. 6.22 (a) shows the measured ac mains voltage and current. Clearly, i_s shapes v_s as expected. Fig. 6.22 (b) shows the MOSFET drain-source voltage and inductor current when switched at approximately 250 kHz. The discontinuity at zero-crossing of i_s is clearly seen because the dead-time comprises a major part with f_{sw} of 250 kHz compared with f_{sw} of 66 kHz. Fig. 6.23 (a) and (b) show the drain- and gate-source voltages during the turn-off and turn-on transients, respectively, illustrating the clean switching of an SiC MOSFET.



(a) Measured v_s, and i_s. (b) Measured v_{ds}, and i_L, at ≈ 250 kHz.

Figure 6.22: Oscilloscope graphs at a switching frequency of roughly 250 kHz. (a) Illustration of ac mains current, i_s, shaping ac mains voltage, v_s. (b) With f_{sw} of 250 kHz, boost inductor current, Δi_L, is 0.7 A, while it was 1.5 A with f_{sw} of 66 kHz. Influence of dead-time is seen as the discontinuity at zero-crossing of i_s.



(a) v_{ds} and v_{gs} during turn-off. (b) v_{ds} and v_{gs} during turn-on.

Figure 6.23: Measured drain-source voltage, v_{ds}, and gate-source voltage, v_{gs}, illustrating the clean switching of an SiC MOSFET. The gate oscillations are within the region where the device is beginning to partly turn on and transiting through the Miller plateau. This initial ringing is due to the input gate capacitance and the circuit parasitic inductance. Thereafter, the change in drain current is minor, resulting in insignificant ringing in v_{ds} during a turn on.

6.3.4.1 Efficiency evaluation

The simulated efficiency of the rectifier as a function of the output power for $v_s = 230$ V is shown in Fig. 6.24, together with the measurement results taken using a Yokogawa WT3000 power analyzer. As can be seen, the simulated results of the converter follow a similar pattern as the measured efficiency over a wide range of output power, and the discrepancy between the two is primarily due to two reasons. First, the simulated case does not consider the core losses in the boost inductor or the input EMI filter losses, whereas the measured case includes the overall losses in the PFC rectifier. Second, to measure such a high efficiency, an error introduced when using a power analyzer is also critical. Nonetheless, the converter achieves an efficiency of above 97% for $> 60\%$ of the rated load with a peak efficiency of 97.2%, and is well above the 80 PLUS efficiency required over the entire load range.

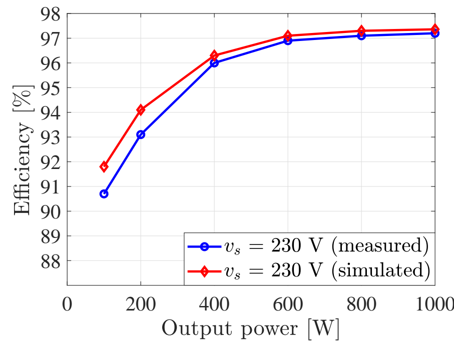
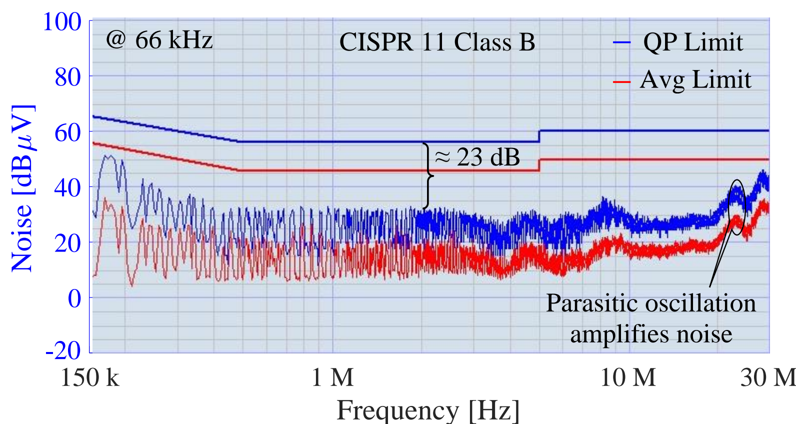


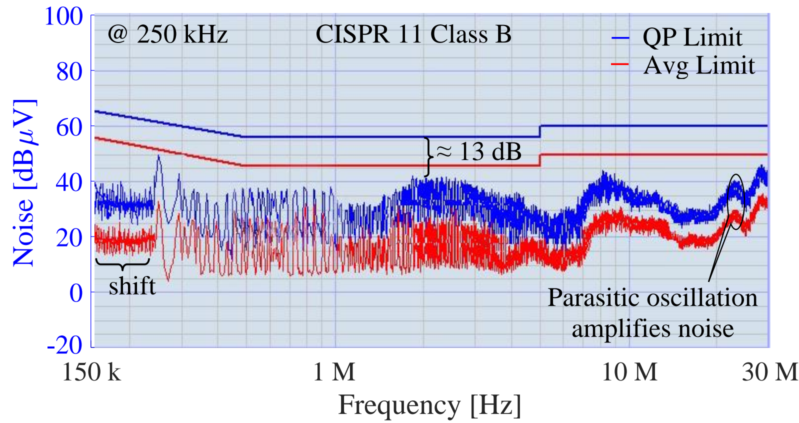
Figure 6.24: Illustration of the simulated and measured efficiency of the PFC rectifier as a function of the output power, indicating that the converter achieves an efficiency of above 97% for a rated load of >60% with a peak efficiency of 97.2%. The measurements were taken using a prototype converter with a Yokogawa WT3000 power analyzer.

6.3.4.2 EMI evaluation

A standard line impedance stabilizing network (LISN) and an EMC analyzer (Agilent E7401A) were used for measuring the EMI. Fig. 6.25 shows the measured conducted EMI emission (within the frequency range of 150 kHz–30 MHz) of the prototype PFC rectifier at an input voltage of 230 V and an output power of 1 kW at two different switching frequencies, 66 and 250 kHz. Compared to 66 kHz switching, at 250 kHz, the EMI noise shifts toward the right slightly, and then increases by approximately 10 dB (23-13 = 10 dB) over the entire spectra applied, given the same EMI filter size. Alternatively, it can be stated that, as the switching frequency increases, the filter size increases if the same noise level needs to be maintained. For the chosen MOSFET, the DPT-measured parasitic oscillations were within the range of 25 MHz. Interestingly, the EMI noises in the corresponding frequency range are augmented, which is clearly shown in Fig. 6.25. This was also corroborated through a simulation conducted in LTSpice by varying the switching loop inductance and observing the noise within the frequency domain plot.



(a) Conducted EMI at a switching frequency of 66 kHz.



(b) Conducted EMI at a switching frequency of 250 kHz.

Figure 6.25: Conducted maximum peak and average EMI noise emissions of the prototype PFC rectifier at an input voltage of 230 V and an output power of 1 kW at two different switching frequencies, namely, 66 and 250 kHz. All measurements are below the quasi peak (QP) and average (Avg) limits, and thus meet the CISPR 11 regulation for Class B equipment. Compared to 66 kHz, a 250 kHz switching incurs a higher noise provided an identical EMI filter.

6.3.5 Summary and conclusion

The main conclusions from this work are summarized below.

1. Employing low-loss SiC power devices in the boost stage, the efficiency was evaluated in a classic boost PFC topology, the results of which revealed that the major converter loss is comprised of a diode rectifier part, which is particularly pronounced at a low-line as compared to a high-line voltage.

2. A comparison between the efficiencies evaluated using a simple look-up table input from a double-pulse test follows the pattern measured using a power analyzer meeting the 80 PLUS efficiency regulation over the entire load range with an excellent margin.

3. The conducted EMI in the prototype converter was found to comply with the CISPR 11 standard. It was also concluded that, owing to the increase in switching frequency from 66 to 250 kHz, the emissions are increased by roughly 10 dB throughout the entire frequency range (150 kHz to 30 MHz). Moreover, it was revealed that EMI noise is augmented at the corresponding ringing frequency given by the parasitic in the commutation loop.

4. Increasing the switching frequency drastically minimizes the boost inductor size; however, the increase in the input EMI filter size might offset the high-power density target, and thus an optimal switching frequency should be chosen.

5. Clean switching of the state-of-the-art SiC devices was illustrated to substantiate the design of a low-parasitic layout.

Chapter 7

Low-inductive converter design considerations

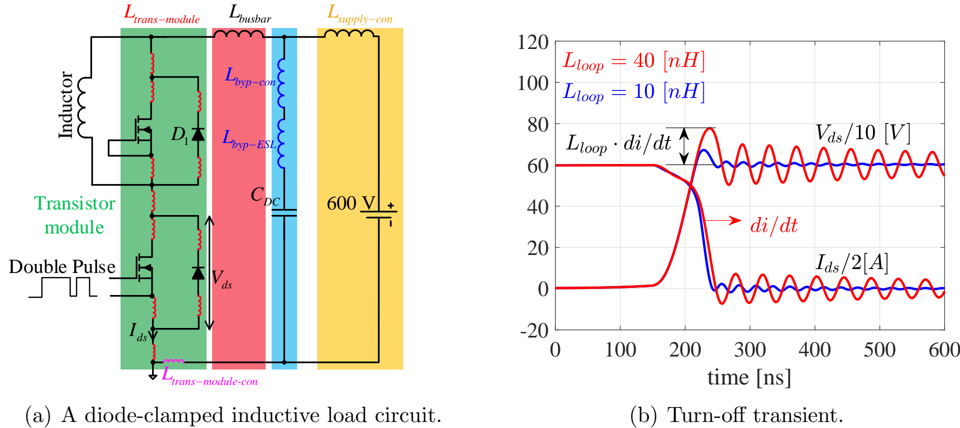
The information presented in this chapter is based on publications C4 and C5, the main purpose of which is to address the following research challenge.

SiC transistors have the potential to switch extremely fast. Often turn-off di/dt is reduced to limit the turn-off over voltages due to the stray inductances in the commutation loops. Thus, the potential low switching losses are not met. One of the benefits of designs with SiC devices is the possibility of low switching losses and therefore high switching frequencies. This opens up for a paradigm shift in power electronics. For utilizing the fast switching potential, a low-inductive circuit layout of the commutation loop consisting of the transistor, diode, connections and the DC-link capacitor is indispensable. Extensive research on low-inductive transistor case and busbars has, to date, been conducted by several research groups [25–28]. Employing low stray inductance DC-link capacitors is a must for realizing the low stray inductance designs. The method used to connect the DC-link capacitors to the system, such as the busbar, is equally important. The work analyzes the geometry and orientation of the DC-clamping capacitor for minimizing the SiC transistor turn-off over voltages. In addition, by reviewing the commercially available low inductance DC-link capacitors with different physical sizes and terminations, this thesis presents the design of a DC-link for a 100 kW full-bridge AC-DC-AC converter. Two approaches; first, measuring the parasitics of the components themselves, such as capacitor and transistor module by impedance analyzer; and, second, computing the parasitics of the bussing structure and connections via finite element analysis tool; are adopted throughout this work. Based on this, the breakdown of the total switching loop stray inductance contributed by each parts is illustrated. A few design examples for further minimizing the switching loop stray inductance when used SiC modules and discrete SiC packages are also provided.

7.1 Introduction

In a diode-clamped inductive load buck converter, as shown in Fig. 7.1 (a), the transistor current basically stays constant until its voltage has reached the supply voltage. Then the current will commutate via the freewheeling diode (D_1) to a DC protection capacitor (C_{DC}). The parasitic inductances of the commutation loop are: internal in the components themselves; for instance, in the semiconductor devices (denoted by red coils), and in the C_{DC} ($L_{byp-ESL}$); and in the busbar (L_{busbar}) [1]. Additionally, the method to connect

these components to the busbar also shares a considerable portion of stray inductances, which are indicated by $L_{trans-module-con}$ and $L_{byp-con}$. During the turn-on process, these parasitic inductances are charged, and, during the turn-off process, they are discharged. The transistor turn-off over voltage can be expressed as: $L_{loop} \cdot di/dt$, where di/dt is dictated by the transistor properties and its gate drive. A typical turn-off transient with two different loop inductances (L_{loop}) is shown in Fig. 7.1 (b), which illustrates that the higher the L_{loop}, the higher the over voltage, the lower the current slew rate [17]. It is noteworthy that voltage overshoot is increased although di/dt is reduced, the reason being a significantly higher increase in L_{loop} than the decrease in di/dt. Furthermore, for the same L_{loop}, this over voltage is more noticeably amplified for the SiC transistor compared to the Si transistor because the former switches extremely fast. For example, di/dt per chip area is measured to be 5.1 A/ns/cm^2 in SiC MOSFET and 2.2 A/ns/cm^2 in Si IGBT, i.e., di/dt is higher by a factor of 2.3 in SiC MOSFET compared to Si IGBT [18]. Often, SiC is slowed down to the level of Si to operate it safely with a penalty of higher switching losses. Thus, it is crucial to design a low-inductive layout to fully utilize the fast switching potential of SiC transistor.



(a) A diode-clamped inductive load circuit.

(b) Turn-off transient.

Figure 7.1: (a) Buck converter with various possible stray inductances in the loop, (b) turn-off transient illustrating the importance of having lower L_{loop}.

In low power electronics area, there exist several application notes and publications concerning low inductance capacitors [214,215]. However, there is limited literature available concerning those in the high power electronics area. In [216], internal inductance of DC-link power capacitors are addressed, but the method to connect them is not covered. First, this work presents some of the dielectric materials available in market in Section 7.2. Then the impact of physical dimensions of structure on the stray inductances and capacitances is discussed in Section 7.3. Thereafter, Section 7.4 reviews the current available low inductance DC-link capacitors with different physical dimensions and terminations, and measures the $L_{byp-ESL}$ associated with them using impedance analyzer, E4990. For a fair comparison, the normalization is performed with two different parameters; first, with respect to the highest capacitance value, and second, with respect to the largest ripple current possessed by the selected capacitors. Following this, the 3D finite element method (FEM) models are built for axial and circular terminated capacitors in Section 7.5. Ansys Q3D tool is used for extracting the parasitics of the required bussing structures and

plotting the current density distribution. Additionally, by highlighting the two different orienting methods for capacitors, this work provides guidelines for designing and orienting them such that $L_{byp-ESL}$ and $L_{byp-con}$, as labelled in Fig. 7.1 (a), are minimum, where the main contribution of this work lies.

Moreover, a 100 kW AC-DC-AC converter is simulated in MATLAB for finding the current stress in the DC-link capacitor in Section 7.6. Dimensioning of the DC-link capacitance for satisfying the defined voltage ripple is also included in this section. Employing each of the low-inductive types of capacitor under study, five DC-link busbars are built and simulated in Q3D. Subsequently, the parasitic inductances encompassed by various parts, such as $L_{trans-module-con}$, $L_{byp-con}$, and power supply connection ($L_{supply-con}$) are accessed. For providing a comprehensive overview of the proportion of stray inductances incorporated by different parts, inductances internal to the components themselves, for example, capacitor and transistor module are measured by impedance analyzer. An example of a complete busbar employing an optimal capacitor solution, in terms of cost and loop inductance factors, is also demonstrated. Looking into the current density distribution plot in the busbar, two different phenomenons can be distinguished: (a) the parts that are bypassed, and (b) the most stressed parts construing the major current flow. In the quest of further minimizing stray inductance, Section 7.7 and Section 7.8 exemplify low-inductive busbar designs using SiC modules and discrete SiC devices. Finally, Section 7.9 presents the most important conclusions.

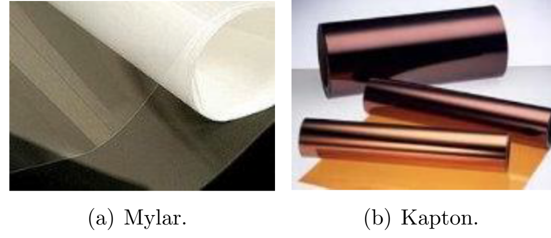
7.2 Theoretical background for the selection of dielectric material

Different dielectric materials are available in market. Some of them are listed in Table 7.1. **The thinner the dielectric, the stronger the magnetic coupling between the positive and the negative plates.** Kapton and Mylar are the thinnest ones in the list. Considering the breakdown strength, dielectric constant, operating temperature and thickness, either **Mylar or Kapton are preferred as dielectric material.** Fig. 7.2 provides the photograph of the dielectric materials; Mylar and Kapton.

Table 7.1: List of insulating materials with breakdown voltage, dielectric constant and continuous temperature.

Insulating Material Types	Breakdown voltage (kV/mil *)	Dielectric Constant (Unitless)	Continuous temperature (°C)
Kapton	5	3.7	400
Mylar (PET)	7.5	3.3	105
Teonex (PEN)	5	3.4	140
Epoxy glass (FR4)	1.25	4.3	140
Nomex	0.43-0.84	1.6	220
Tedlar (PVF)	3.5	11	105
Epoxy powder coating	0.8	4	130

* 1 mil = 0.0254 mm.



(a) Mylar. (b) Kapton.

Figure 7.2: Photograph showing the dielectric material; Mylar and Kapton.

7.3 Impact of geometry on stray inductance and capacitance

In this section, the stray inductance (L_{stray}) and distributed capacitance (C_{dis}) of coplanar, planar and coaxial structures are studied through basic physics-based expressions, as given by (7.1)–(7.5) [217–219]. The dimensions used are: width (w), length (l), distance between the positive and the negative plates (h), diameter of the inner conductor (d), and diameter of the outer conductor (D). The remaining variables used in the equations are: ϵ_r; relative permittivity of the dielectric, and ϵ_0; permittivity of the free space. Likewise, μ_r is the relative permeability of the medium and μ_0 is permeability of the free space. For greater clarity, the dimensions used in these equations are labelled in Fig. 7.3.

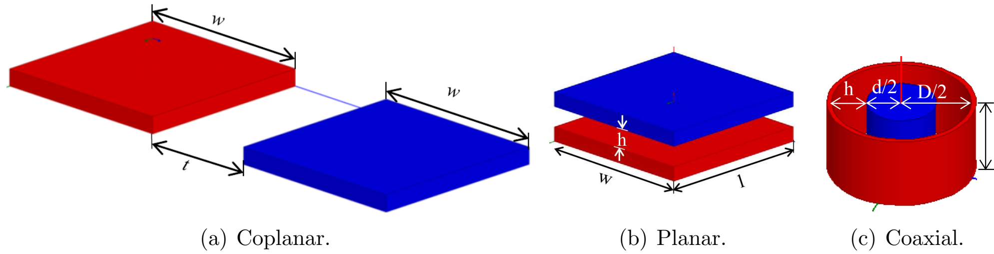
$$L_{stray,\ coplanar} = \frac{\mu_0 \cdot \mu_r}{\pi} \cdot \cosh^{-1} \frac{w+t}{w} \cdot l, \quad t \gg w, \tag{7.1}$$

$$L_{stray,\ planar} = \mu_0 \cdot \mu_r \cdot \frac{h \cdot l}{w}, \quad w \gg h \tag{7.2}$$

$$L_{stray,\ coaxial} = \frac{\mu_0 \cdot \mu_r}{2\pi} \cdot ln \frac{D}{d} \cdot l \tag{7.3}$$

$$C_{dis,\ planar} = \epsilon_0 \cdot \epsilon_r \cdot \frac{w \cdot l}{h} \tag{7.4}$$

$$C_{dis,\ coaxial} = \frac{2\pi \cdot \epsilon_0 \cdot \epsilon_r}{ln \frac{D}{d}} \cdot l \tag{7.5}$$

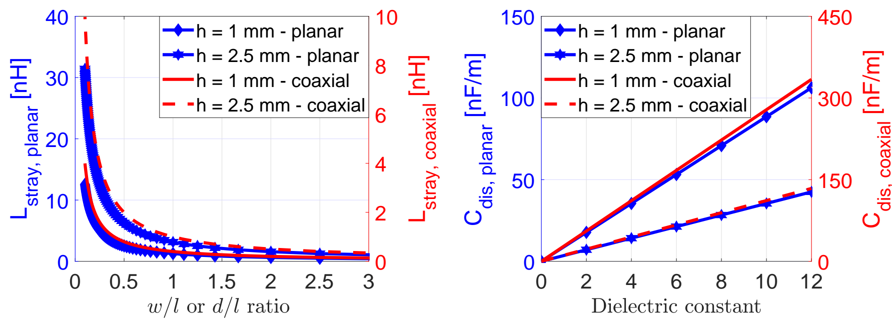


(a) Coplanar. (b) Planar. (c) Coaxial.

Figure 7.3: Example of coplanar (a), planar (b) and coaxial structures with dimensions. The coaxial structure cancels the magnetic field more effectively than the coplanar and planar ones.

Fig. 7.4 (a) shows the plot of (L_{stray}) versus w/l (or d/l) ratio for planar and coaxial structures. Apparently, there is the highest reduction in L_{stray} for w/l (or d/l) ratio up to

1, which suggests that this ratio should be ≥1. In addition, the closer the opposite plates, the lower the inductance. Nonetheless, for the same separation between the opposite plates, the coaxial structure gives four times lower L_{stray} than the planar structure. In contrast, for the same conditions, the coaxial structure entails three times higher C_{dis} than the planar structure, as conveyed in Fig. 7.4 (b). Of special note is that C_{dis} acts as a filter for instance, for reducing EMI, and it is preferred to be in the higher range, and thus the dielectric with minimum thickness and high relative permittivity is desirable. In conclusion, **the coaxial structure cancels the magnetic field more effectively than the planar and coplanar approaches, however, it not easy to realize a complete planar or coaxial design in all the places like terminations and clearances.**

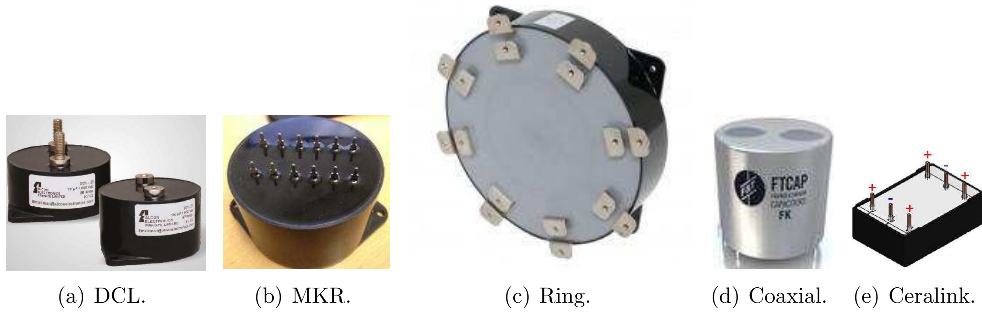


(a) L_{stray} plot with varying w/l or d/l ratio. (b) C_{dis} plot with varying dielectric constant.

Figure 7.4: L_{stray} plot of planar versus coaxial structures illustrates the highest reduction in L_{stray} for w/l (or d/l) ratio upto 1. Clearly, the smaller the h, the lower the L_{stray}. For the same h, L_{stray} is lower by a factor of 4 for the coaxial structure compared to the planar structure. μ_r is taken as 1 while plotting L_{stray}. C_{dis} plot of planar versus coaxial structures conveys that for the same h, C_{dis} is higher by a factor of 3 for the coaxial structure compared to the planar structure. As C_{dis} is a filter, it is preferred to be in the higher range, and thus the dielectric with minimum thickness and high relative permittivity is desirable.

7.4 Selection of low inductance DC-link capacitors

In this section, a brief description of the selected low inductance DC-link capacitors is presented. Fig. 7.5 provides a photograph of these capacitors, namely, DCL capacitor, MKR capacitor, Ring capacitor, Coaxial capacitor and Ceralink capacitor. The first four are film type and the last one is a Ceramic type with different dielectric material than in a classic ceramic capacitor. In reference [216], it is mentioned that the capacitance increases with increasing voltage in the dielectric used for Ceralink type, while the opposite is true in the class 2 ceramic materials used for multilayer ceramic capacitors. Primarily, the mechanical interface of capacitors are decided by their voltage and current ratings. For a fair comparison, capacitors with equal voltage ratings (900 V) have been chosen. The electrical specification of the selected capacitors is shown in Table 7.2. The capacitance and ripple current rating (I_{ripple}) are from data sheet, where the latter is taken for 85 °C [220–223]. The effective series inductance ($L_{byp-ESL}$) is measured using an impedance analyzer, E4990.



(a) DCL. (b) MKR. (c) Ring. (d) Coaxial. (e) Ceralink.

Figure 7.5: Photograph of five different commercially available low inductance capacitors, where (a) is a DCL capacitor (45 mm separation between the opposite screws), (b) is an MKR capacitor (24 mm separation between the opposite pins), (c) is a Ring capacitor, (d) is a Coaxial capacitor, and (e) is a Ceralink capacitor (7.62 mm separation between the opposite pins).

Table 7.2: Electrical specification of low inductance DC-link capacitors.

Capacitor type & parameters	Capacitance (μF)	I_{ripple} (A) @85°C	$L_{byp-ESL}$ (nH)	Cost (e)
DCL	150	50	14.85	18
MKR	95	45	4.85	25
Ring	215	175	10.2	170
Coaxial	20	20	6.7	10
Ceralink	5	25	3.5	52

Table 7.3: Parameters normalized to capacitance of Ring capacitor.

Capacitor type & parameters	No. of capacitors	I_{ripple} (A)	$L_{byp-ESL}$ (nH)	Total cost (e)
DCL	2	100	7.42	36
MKR	3	135	1.61	75
Ring	1	175	10.2	170
Coaxial	11	220	0.61	110
Ceralink	43	1075	0.08	2236

Table 7.4: Parameters normalized to ripple current of Ring capacitor.

Capacitor type & parameters	No. of capacitors	Capacitance (μF)	$L_{byp-ESL}$ (nH)	Total cost (e)
DCL	4	600	3.71	72
MKR	4	380	1.21	100
Ring	1	215	10.20	170
Coaxial	9	180	0.74	90
Ceralink	7	35	0.50	364

Considering $L_{byp-ESL}$ of a single capacitor, Ceralink has the lowest value followed by MKR, Coaxial, Ring, and DCL. Prominently, Ceralink has the largest ripple current per

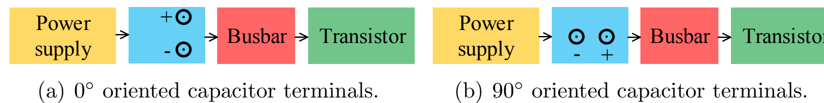
capacitance amongst all. It should be underlined that the cost is evaluated based on distributor's 1000 quantity. In order to guarantee a fairer comparison, the capacitance of each capacitor is normalized with respect to that of the Ring capacitor, and the results are given in Table 7.3. Note that the number of capacitors has been rounded up to the next whole number. The remaining parameters in Table 7.3, i.e., I_{ripple}, $L_{byp-ESL}$, and total cost are calculated based on the rounded value of capacitor. As can be observed, a new order of capacitors ascending with regard to $L_{byp-ESL}$ is Ceralink followed by Coaxial, MKR, DCL and Ring. As Ceralink has the lowest capacitance amongst all, 43 of them have to be connected in parallel to meet the same capacitance requirement as that given by the Ring. Consequently, this solution becomes the most expensive of all those considered at present (this scenario might change in future as Ceralink is an emerging technology and the price is likely to drop).

Furthermore, in the quest for a more balanced comparison, the ripple current of each capacitor is normalized with respect to that of the Ring capacitor, and the outcome is catalogued in Table 7.4. It should be asserted again that the number of capacitors is rounded up and the remaining parameters are calculated accordingly. When normalized with the ripple current, the number of parallel capacitors and the total cost comprised by each type of capacitor are closer compared to those when normalized with capacitance. Interestingly, the new order of capacitors as per the $L_{byp-ESL}$ remained unaltered in either of the normalization approaches.

7.5 Impact of capacitor orientation on inductance

7.5.1 Axial terminated capacitors

Section 7.4 focused on the selection of low inductance DC-link capacitors and the measurement of the inductance imposed by their geometries, while this section primarily focuses on the simulation of the inductance associated with the bussing connections made with each capacitor type. In particular, the orientation of capacitors while mounting them on the busbar is investigated to study their impact on the $L_{byp-con}$. Fig. 7.6 shows two directions, defined as 0° and 90°, for mounting capacitors. In the 0° case, the opposite terminals are located at equal distance to the transistor while they are not in the 90° case.



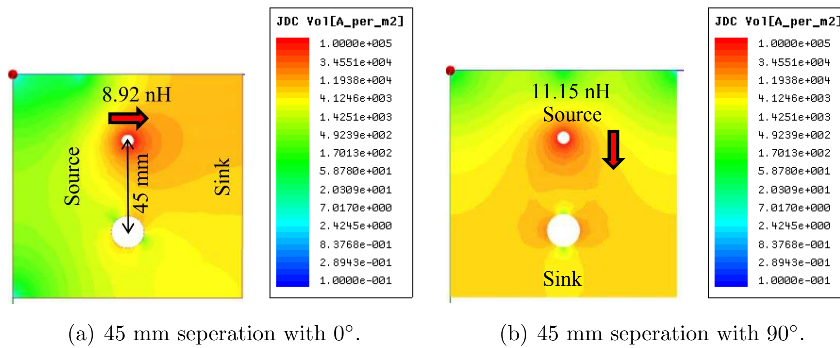
(a) 0° oriented capacitor terminals. (b) 90° oriented capacitor terminals.

Figure 7.6: Definition of orientation of capacitor. In the 0° case, opposite terminals are located at equal distance to the transistor while they are not in the 90° case.

Additionally, by specifying 3D geometry, material properties (such as copper for busbar and Mylar for dielectric), and the desired output, Q3D extractor generates the necessary impedance matrices which can be represented by the lumped element circuit model [See Appendix Fig. B.2]. Details on the basics of modelling of busbar with this tool are provided in Appendix B.

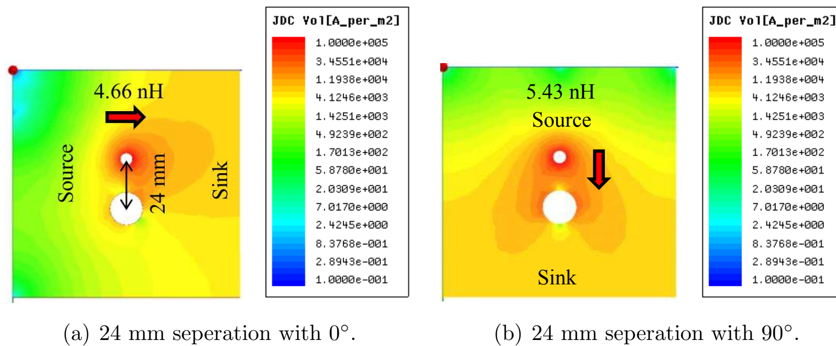
7.5.1.1 DCL capacitor

Fig. 7.7 depicts the simulated busbar for DCL capacitor with 45 mm separation between the opposite screws, where (a) is with 0° orientation and (b) is with 90° orientation along with the corresponding $L_{byp-con}$ labelled in the respective current density plots. The current flows from the capacitor (source) to the load (sink) and is indicated by an arrow head. Self-inductances (L_{11} and L_{22}) of the opposite plates are almost equal in the former case, while there is a large difference between those in the latter case, and the results are summarized in Table 7.5. It is worth emphasizing that the 0° case showed around 20% lower $L_{byp-con}$ compared to the 90° case. This is a result of **there being a stronger flux linkage between the opposite plates in the former orientation compared to the latter.**



(a) 45 mm seperation with 0°. (b) 45 mm seperation with 90°.

Figure 7.7: Simulated busbar for DCL capacitor with 45 mm separation between the opposite screws. Orientation in (a) has lower loop inductance than in (b).



(a) 24 mm seperation with 0°. (b) 24 mm seperation with 90°.

Figure 7.8: Simulated busbar for DCL capacitor with 24 mm separation between the opposite screws. Orientation in (a) has lower loop inductance than in (b).

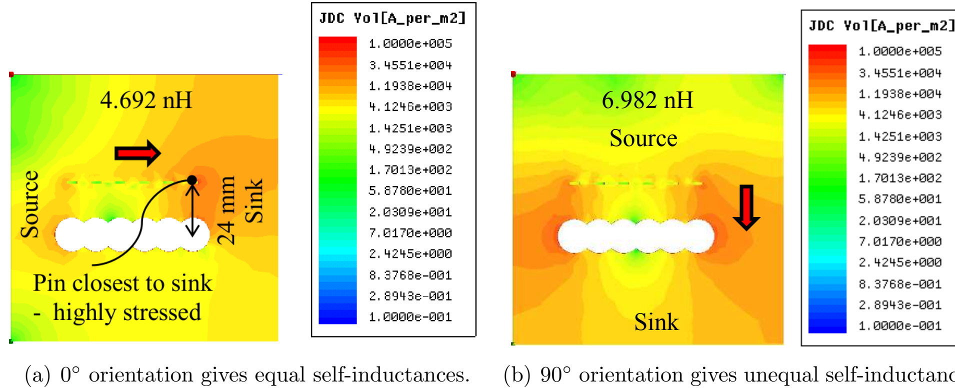
DCL capacitors are also available with 24 mm separation distance and the current density plot is shown in Fig. 7.8 (a) with 0° orientation and (b) with 90° orientation. **Simulation showed that the smaller the distance between the opposite screw holes, the lower the $L_{byp-con}$.** Capacitors with 24 mm separation showed around 47%

(0°) and 51% (90°) lower $L_{byp-con}$ compared to those with 45 mm separation. The closer the opposite screws, the better the magnetic field cancellation, which is the reason behind this result. Thus, **mounting of capacitors is critical especially when the distance between the opposite screws is larger**, as inferred from the analysis in this section.

Table 7.5: Summary of inductances for axial terminated capacitors.

Capacitor type	L_{11} (nH)	L_{22} (nH)	L_{12}, L_{21} (nH)	$L_{byp-con}$ (nH)	Reduction (%)
DCL 45 mm, 0°	13.576	13.585	9.117	8.925	19.991
90°	6.187	20.743	7.887	11.155	
DCL 25 mm, 0°	12.967	12.968	10.635	4.665	13.818
90°	9.047	16.903	10.268	5.413	
MKR 24 mm, 0°	11.529	11.123	8.979	4.692	32.798
90°	8.352	17.403	9.386	6.982	
Ceralink 7.62 mm, 0°	11.469	10.437	10.375	1.156	3.906
90°	12.298	10.977	11.036	1.203	

The variables used in Table 7.5 are: self-inductances, L_{11} and L_{22}; mutual inductances, L_{12} and L_{21}; and stray inductance associated with the connection of capacitor to busbar, $L_{byp-con}$. Note: Safety clearance of 5 mm and dielectric thickness of 0.4 mm are considered throughout the simulation.



(a) 0° orientation gives equal self-inductances. (b) 90° orientation gives unequal self-inductances.

Figure 7.9: Simulated busbar for MKR capacitor with 24 mm separation between the opposite pins. Fig. (a) has a lower loop inductance compared to Fig. (b). Q3D simulation shows that the pin closest to the sink is highly stressed in the capacitor orientated in 0°, while in the one with 90° orientation, the pins which are towards the extreme left and right sides of the sink, are the most stressed ones.

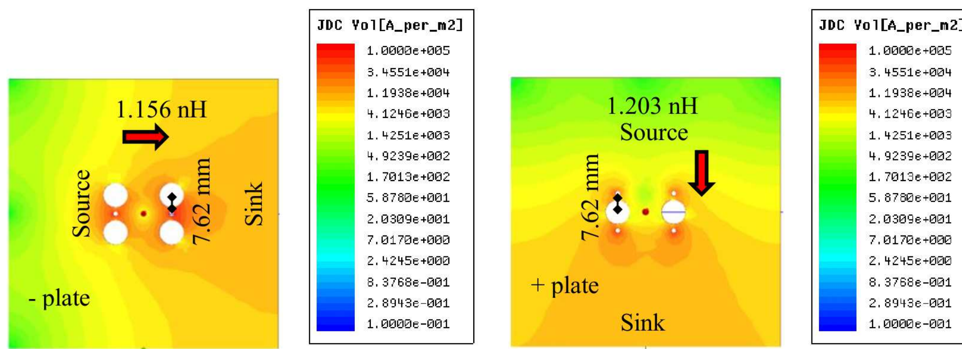
7.5.1.2 MKR capacitor

Fig. 7.9 (a) and (b) shows the current density distribution in the busbar with MKR capacitor which are placed at 0° and 90°, respectively. In the busbar with 0° orientation of the capacitor, the pin which is closest to the sink is highly stressed, while in the one with 90° orientation, the pins which are towards the extreme left and right sides of the

sink are the most stressed ones. In fact, in the former orientation, **the capacitor which is closest to the load provides the lowest impedance path for the current or it is utilized the most, compared to the ones placed further apart.** In the latter orientation, on the other hand, the clearances for the opposite pins block the direct current path, and thereby a detour is taken. It should be noted that the loop inductance is lower by around 33% in the case with 0° compared to the one located at 90°, detailed results are included in the summary in Table 7.5.

7.5.1.3 Ceralink capacitor

Fig. 7.10 (a) and (b) display the current density distribution for the Ceralink capacitors, which are located at 0° and 90°, respectively. SP900 series [222] of Ceralink capacitors are made by series connection of two capacitors, the negative plate is shown in (a) and the positive plate in (b). The end results regarding the orientation in Ceralink showed a similar pattern as in DCL and MKR capacitors, that is, 0° mounting resulted in around 4% lower $L_{byp-con}$ compared to that with 90°, the $L_{byp-con}$ of which are marked in the respective plots. These capacitors showed the lowest $L_{byp-con}$, as the opposite pins are closest of all (only 7.62 mm).



(a) 0° orientation gives equal self-inductances. (b) 90° orientation gives unequal self-inductances.

Figure 7.10: Simulated busbar for Ceralink capacitor with 7.62 mm separation between the opposite pins. Orientation in (a) has lower loop inductance than in (b). As Ceralink capacitor with 900 V rating is made by series connection of two capacitors, the negative plate is shown in (a) while the positive in (b).

7.5.2 Circular terminated capacitors

Section 7.5.1 primarily concentrated on simulating loop inductance associated with the bussing structure for axial terminated capacitors, while this section focuses on that for circular terminated capacitors. The impact of their placement in $L_{byp-con}$ is simulated for these capacitors as well, and **it is found that the orientation in either direction provides an equal outcome.**

7.5.2.1 Ring capacitor

In the chosen Ring capacitor [223], eight terminal pairs are evenly spaced around the circumference. It is large in terms of both volume and weight. The ratio of diameter (225 mm) to height (50 mm) is 4.5 (≫1), resulting in low $L_{byp-con}$ for the given capacitance and ripple current rating. Fig. 7.11 illustrates the current density distribution and the associated $L_{byp-con}$ for it. Because of the larger separation distance between the opposite screws and larger clearances needed for screw holes, the ring type has a larger loop inductance, as shown in Table. 7.6.

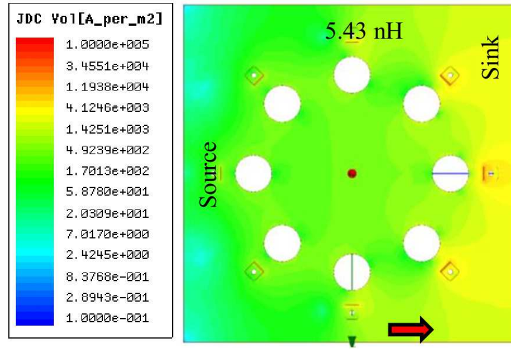


Figure 7.11: Simulated busbar for Ring capacitor (SBE) resulted in equal $L_{byp-con}$ in both orientations. This capacitor is large in terms of both size and weight. The bussing structure and the clearance holes are also larger compared to the rest of the capacitors under consideration.

7.5.2.2 Coaxial capacitor

In the Coaxial capacitor [221], three pin pairs are evenly spaced around the circumference. It is a PCB mounted type and has a relatively smaller physical size, termination pins and capacitance compared to the Ring capacitor. The manufacturer has chosen the diameter and height to be almost equal in order to realize low $L_{byp-ESL}$. The simulated busbar is illustrated in Fig. 7.12, and the details about inductance matrices are provided in Table. 7.6.

Table 7.6: Summary of inductances for circular terminated capacitors.

Capacitor type	L_{11} (nH)	L_{22} (nH)	L_{12}, L_{21} (nH)	$L_{byp-con}$ (nH)
Ring	24.770	12.202	15.933	5.430
Coaxial	9.994	9.094	8.668	1.752

The variables used in Table 7.6 are: self-inductances, L_{11} and L_{22}; mutual inductances, L_{12} and L_{21}; and stray inductance associated with connection of capacitor to busbar, $L_{byp-con}$. Note: Safety clearance of 5 mm and dielectric thickness of 0.4 mm are considered throughout the simulation.

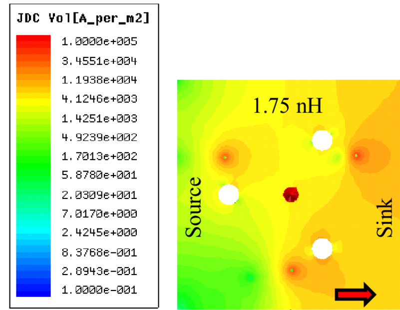


Figure 7.12: Simulated busbar for Coaxial capacitor (FTCAP). Orientation in either direction provides an equal outcome. $L_{byp-con}$ is smaller compared to that of the Ring capacitor because the opposite pin pairs are closer and smaller.

7.6 Design of DC-link for AC-DC-AC converter

In this section, there are three main objectives. The first objective concerns sizing of the DC-link capacitor in an AC-DC-AC converter, which is covered in Section 7.6.1. The second objective relates to comparing the stray inductance constituted by various components and their connections, which is presented in Section 7.6.2. The third goal entails exemplifying a DC-link busbar design employing Coaxial capacitor, and is included in Section 7.6.3.

7.6.1 Sizing the DC-link capacitor

A series-resonant converter topology for an induction heating application is shown in Fig. 7.13. The DC-link capacitor (C_{DC}) is stressed from two sides: rectifier and inverter. First, in order to find the ripple current share from the 6-pulse bridge rectifier side, a simulation is performed in MATLAB for a 100 kW converter with a DC-link voltage of 640 V. At 360 Hz (6 $\times$ 60 Hz, 60 Hz being the AC line frequency), the ripple current is simulated to be 7.2 A. Second, to find the ripple current which comprises the inverter part, the full-bridge series-resonant inverter is switched at 300 kHz for an output current (I_{out}) of 180 A, which resulted in the ripple current of 80.5 A in the C_{DC}. Adding the contribution from the rectifier part and the inverter part, the aggregate ripple current (I_c) capacity of capacitor becomes 87.7 A. Simultaneously, the DC-link capacitor should be sized such that the defined ripple voltage requirement (<10%) in a converter is ensured. The simulation was performed with the capacitance of 180 μF which gave the ripple voltage of 45 V; 7% of the DC-link voltage. When using 35 μF of Ceralink capacitors, as obtained from the normalization in Section 7.4, the ripple voltage will cross the defined ripple limit, the solution would be to connect an additional 29 Ceralink capacitors. However, this solution would be the most expensive of all. On the other hand, all the remaining capacitors give a ripple voltage well below the defined margin.

7.6.2 Comparison of stray inductance shared by various parts

In this section, FEM simulation is used to extract the stray inductance created by the connection of power supply, capacitor, and transistor module, however, the ones associated

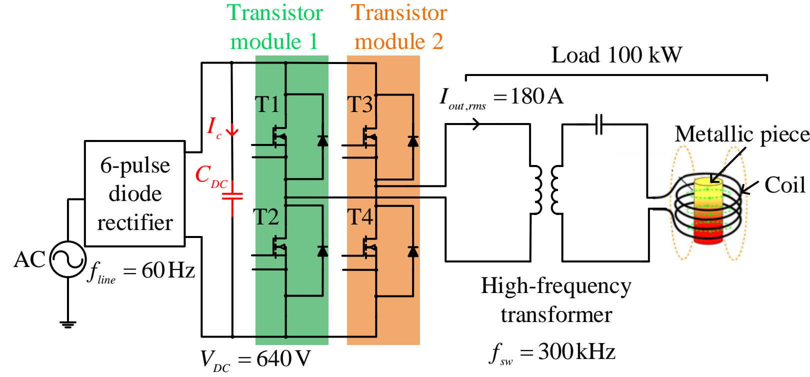


Figure 7.13: Schematic diagram of AC-DC-AC converter for an induction heating application. Capacitor (C_{DC}) is stressed partly from the front end 6-pulse diode rectifier but primarily from the 300 kHz switched series-resonant inverter. For instance, for the given 100 kW converter, the front end current stress by 360 Hz component is simulated to be 7.2 A and the current stress from the inverter part is 80.5 A, so the total capacitor current (I_c) is 87.7 A. With capacitance of 180 μF, the ripple voltage resulted in being 7% of DC-link voltage.

internal to the capacitor and the transistor module are measured using an impedance analyzer. Five different 3D models of the DC-links are built employing each type of the selected capacitors. The number of capacitors is according to the normalization with respect to the ripple current capacity, as shown in Table 7.4. It should be highlighted that $L_{byp-con}$ for the axial terminated capacitors is simulated with 0° orientation, as explained in Section 7.5.1. Furthermore, for the DCL capacitor, the case with 24 mm separation is chosen.

Table 7.7 depicts the total switching loop stray inductance (L_{loop}) which is the composite of the stray inductance contributed by all the components and connections in the switching loop. For instance, adding the inductance comprised by the capacitor part ($L_{byp-ESL} + L_{byp-con} = 0.74 + 0.55 = 1.29$ nH) and the transistor module part ($L_{trans-module} + L_{trans-module-con} = 15 + 5.96 = 20.9$ nH), L_{loop} is reckoned to be 22.25 nH for the busbar with Coaxial capacitor. Note that FEM simulation was performed with and without the supply part, but the simulated results remained unchanged. This is obvious because the supply part of the busbar is bypassed. Since $L_{supply-con}$ is bypassed, it is not accounted while computing L_{loop}.

Table 7.7: Summary of switching loop inductance.

Capacitor type & parameters	$L_{byp-ESL}$ (nH)	$L_{byp-con}$ (nH)	L_{loop} (nH)	Improvement (%)
DCL	3.71	1.61	26.67	31.28
MKR	1.21	1.94	24.52	36.82
Ring	10.20	5.43	38.81	0
Coaxial	0.74	0.55	22.25	42.66
Ceralink	0.50	0.26	21.89	43.59

Note: $L_{loop} = (L_{byp-ESL} + L_{byp-con} + L_{trans-module} + L_{trans-module-con}) \,/\!/\, L_{supply-con}$.

As can be observed from the table, the solution with Ring capacitor resulted in being the most inductive followed by DCL, MKR, Coaxial, and Ceralink. In the last column labelled as "Improvement" the percentage reduction in the total switching loop stray inductance compared to that when using the Ring capacitor is shown. In addition, the share of module part and the capacitor part can be visualized by the bar chart in Fig. 7.14. Employing DCL and MKR capacitors, the total loop inductance is improved by around 31% and 37%, correspondingly, taking L_{loop} imposed by Ring capacitor as a reference. Similarly, using the solution with Coaxial and Ceralink capacitors, the loop inductance is improved the most; by approximately 43% and 44%, respectively, compared to the loop inductance impressed by the Ring capacitor solution.

Likewise, from the bar chart, it is also clear that **the majority of switching loop stray inductance is shared by the transistor module part.** Apparently, the internal inductance of the transistor module is equivalent to that composed by the Ring capacitor in total. In fact, SiC MOSFETs are packaged in the same standard plastic package as used for Si IGBT modules, which is the reason for such a high inductance in the transistor module.

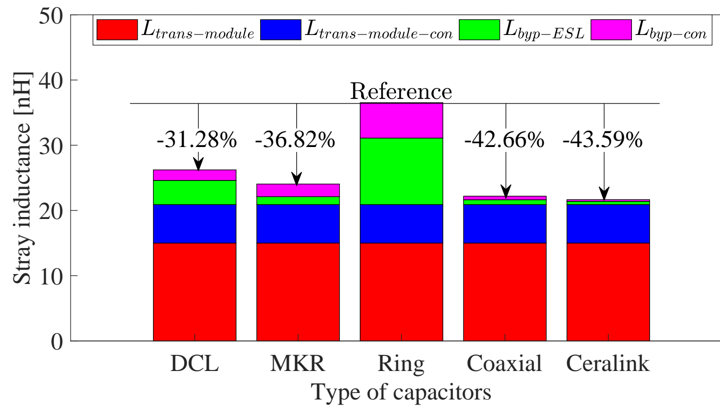


Figure 7.14: Breakdown of switching loop stray inductance in a 100 kW AC-DC-AC converter. The legends in bar chart are: internal parasitic inductance of the transistor module ($L_{trans-module}$), stray inductance from the transistor module connection ($L_{trans-module-con}$), inductance associated internally in the capacitor ($L_{byp-ESL}$), and stray inductance from the bypass capacitor connection ($L_{byp-con}$). The stray inductance shared by $L_{trans-module}$ and $L_{trans-module-con}$ are the most critical ones and have to be further reduced.

7.6.3 Exemplifying a DC-link busbar design with coaxial capacitor

An example of the simulated DC-link busbar employing nine coaxial capacitors in parallel is provided in Fig. 7.15. This combination possesses the total ripple current capacity of 175 A. With a capacitance of 180 μF, the ripple voltage in the DC-link is 45 V as per the MATLAB simulation, which is 7% of the total DC-link voltage (640 V). It is worth mentioning that for maintaining the ripple voltage within 10%, the capacitance was chosen to be 180 μF, which, in turn, ended up with double the ripple current capacity than that

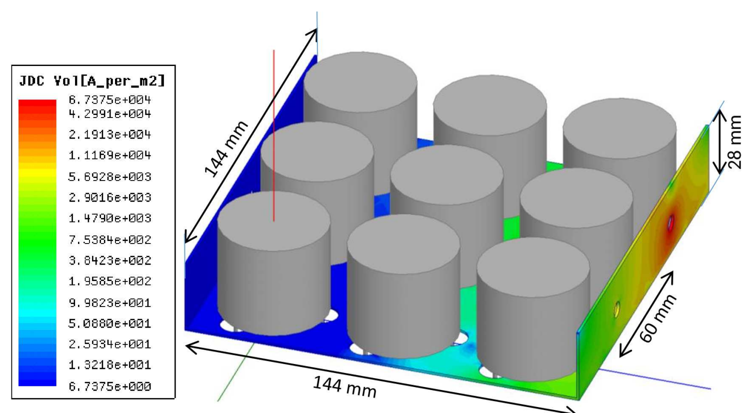


Figure 7.15: Simulated DC-link busbar with nine coaxial capacitors resulting in the total bussing stray inductance of 6.5 nH. Note that this DC-link has a total capacitance of 180 μF and ripple current capacity of 175 A. Clearly noticeable is the higher current density towards the transistor module connection side (right side), compared to the supply side (left side) indicating that the capacitors away from the transistor module are bypassed, that is, capacitor closer to the switching device provides a low inductance path for switching transients.

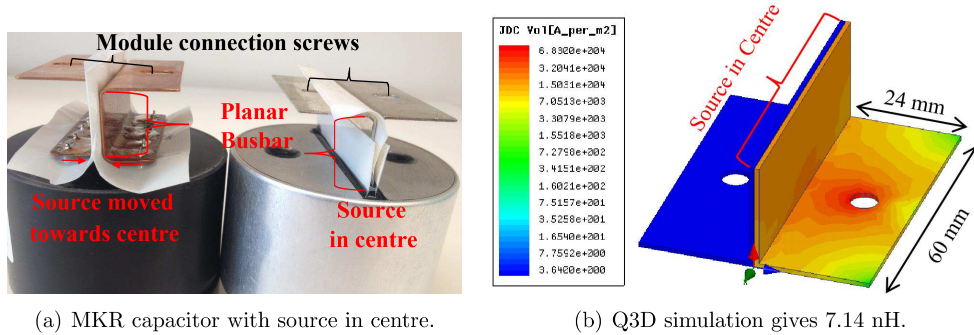
of the simulated value. Furthermore, it is noticeable from Fig. 7.15 that **current density is higher towards the transistor module side (right side), indicated by the red color, compared to the supply side, indicated by the blue color.** Observing this pattern in the current density plot, it can be inferred that the components away from the transistor module are bypassed. To rephrase it, **the capacitor closer to the switching device provides a low inductance path for switching transients.**

7.7 Example of a low-inductive busbar design for SiC MOSFET modules

The major parts of the earlier sections dealt with minimizing the stray inductance comprised by the DC-link capacitors. However, this section primarily focusses on reducing those contributed by the module connection, $L_{trans-module-con}$ apart from $L_{byp-con}$. Examples of busbars for single versus multiple screw holes modules with single and double DC-link sources are demonstrated via FEM simulations in order to address this part.

7.7.1 Busbar for single screw hole module

Fig. 7.16 (a) shows a photograph of an MKR capacitor, the opposite pins of which are moved towards the centre via a copper busbar with two main goals, the first is minimizing the stray inductance by reducing the effective distance and the second is to fit its terminal exactly to the SiC MOSFET module. The current density distribution of this bussing structure is depicted in Fig. 7.16 (b), the stray inductance of which is simulated to be 7.14 nH.



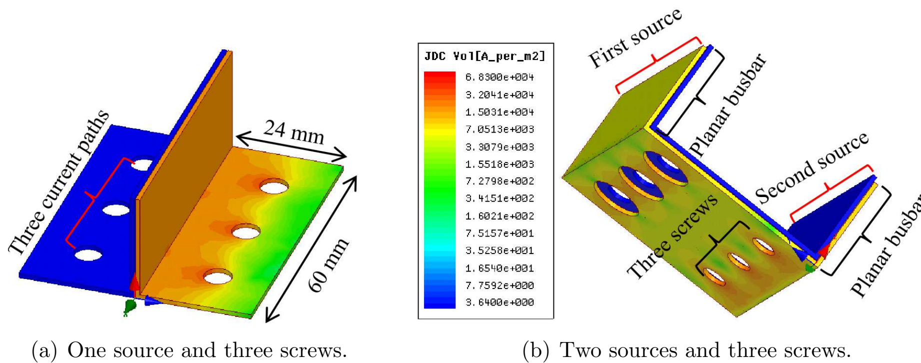
(a) MKR capacitor with source in centre.

(b) Q3D simulation gives 7.14 nH.

Figure 7.16: (a) Photograph of an MKR capacitor, busbar and termination. Pins of the standard MKR capacitor are moved towards the center via a copper busbar to minimize inductance and also to fit the termination to the SiC MOSFET module. (b) Plot showing the distribution of current density. Stray inductance of the bussing structure is simulated to be 7.14 nH.

7.7.2 Busbar for multiple screw holes module

When the SiC modules with multiple screws are commercially available, such as those traditionally used for Si modules, [224], the parallel screw holes in the busbar need to be added accordingly to facilitate the module connection. These **multiple screws are for providing parallel current paths, which results in low inductance.** With 1, 2 and 3 screws used, the DC-bus inductances are 7.14 nH, 5.92 nH and 5.66 nH respectively. Fig. 7.17 (a) shows the FEM simulation with single source and three screws busbar design, while Fig. 7.17 (b) shows that with the supply fed from two sides with three screw holes in the module. With 1, 2, and 3 screws, the DC-bus inductances ($L_{stray,ext}$, excludes internal



(a) One source and three screws.

(b) Two sources and three screws.

Figure 7.17: (a) Multiple screws provide multiple current paths and decrease the effective loop inductance. Compared to the busbar presented in Appendix B.1 (Fig. B.3), the stray inductance is reduced by 60%. (b) Multiple screws and two sources further decrease the effective loop inductance. Compared to the busbar presented in Appendix B.1 (Fig. B.3), the stray inductance is reduced by 82%. Both (a) and (b) are plotted with same scale, the deeper red color in (a) indicates that the stray inductance is higher in it compared to that in (b).

stray inductance of transistor module and capacitor) are 3.8 nH, 2.62 nH and 2.52 nH, respectively. Current density plot of the busbar design in Fig. 7.16 (b), Fig. 7.17 (a) and (b) have the same scale. The deep red color shading in the former busbar compared to that in the latter denotes that the former has higher stray inductance compared to the latter.

Table 7.8 shows the summary of simulated stray inductances for different designs. Taking the originally designed busbar (presented in Appendix B.1, Fig. B.3) as a reference, the percentage reduction in stray inductance is also included.

Table 7.8: Summary of $L_{stray,ext}$ in different designs from Q3D simulation.

Case	No. of screws	$L_{stray,ext}$ (nH)	Reduction (%)
Coplanar	1	7.14	49.0
	2	5.92	57.7
	3	5.66	59.5
Planar single source	1	6.43	54.0
	2	5.02	64.1
	3	4.69	66.5
Planar double source	1	3.80	72.8
	2	2.62	81.2
	3	2.52	82.0

Note that $L_{stray,ext}$ excludes the internal inductance of transistor module and capacitor from L_{loop}.

7.8 Example of a low-inductive busbar design using discrete SiC MOSFETs

To date, most SiC devices come in the same standard plastic housing as that designed for Si IGBTs, the internal inductance of which is in the range of 15 to 30 nH for modules [123,124,130,131] and 2 to 10 nH for discrete devices [82,146,148]. They have to either be operated at reduced DC-link voltage or their fast switching speeds have to be scarified for ensuring the safe operation. Section 7.7 highlighted few designs for minimizing the stray inductance shared by the transistor module and bypass capacitor connections. This section, on the other hand, sheds some light on **distributing the discrete SiC MOSFETs with TO-263-7 package and ceralink capacitors such that a low-inductive symmetrical busbar design is realized giving the reported minimum total switching loop inductance of 5 nH.** The techniques for achieving this result are provided in brief below.

Fig. 7.18 shows a complete 3D FEM model of the components layout in such an inverter, where the DC-clamping capacitors are evenly distributed immediately adjacent to the 4 paralleled discrete SiC MOSFETs. Several factors which involve low loop inductance are considered in this design. For instance, Ceralink capacitors are chosen as they have small height, low stray inductances and high current capacity; SiC MOSFETs with TO-263-7 packages have low height, separate power and source returns, where five pins are accounted as power return and one as source returns; and copper plates are assembled in a transmission line like layout such that width to length ratio of the current path is

kept greater than 1. Fig. 7.19 illustrates the FEM simulation of a half-symmetry of the full model, as shown in Fig. 7.18, the Q3D extracted loop inductance of which is 3 nH. Highly stressed parts are indicated by deep red color shading in the top and back view of the model.

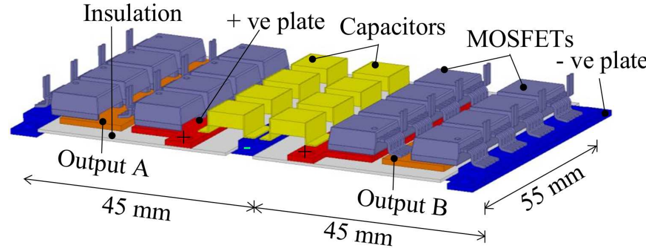


Figure 7.18: A complete components layout in a single-phase, full-bridge inverter, including DC-clamping capacitors, TO-263-7 packaged SiC MOSFETs, copper plates and insulation layer. Width to length ratio of the current path is maintained greater than unity in each of the half-bridge in order to acquire minimum loop inductance. Note that the thickness of copper plate is 1 mm.

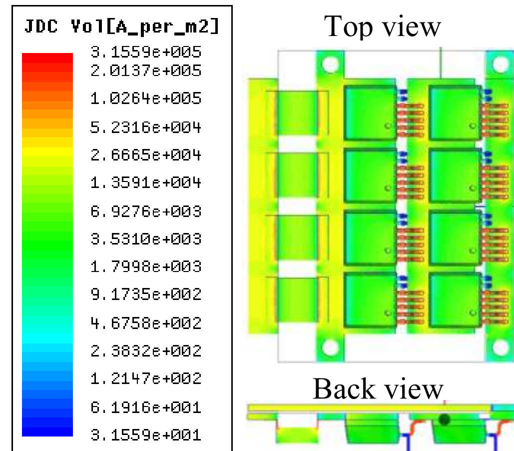


Figure 7.19: Illustration of FEM simulation of a half-symmetry model employing Ansys Q3D. Deep red color shading in the current density plot indicates the highly stressed parts in the top and back view of the model and the loop inductance shared by busing structure and component connections is computed to be 3 nH.

7.9 Conclusion

To conclude, for practical low-inductive converter design considerations, the following guidelines are recommended.

1. As the geometrical structure impacts stray inductance, while making busbar connections or DC-link capacitors, it is essential to keep the width to length ratio (w/l) or the diameter to length ratio (d/l) $\geq$1.

2. The opposite current carrying plates should run on top of each other like a transmission line like structure while the separation between them should be as small as possible for the better cancellation of magnetic field. For example, a DCL capacitor with smaller distance between the screws showed lower connection inductance than that with larger distance.

3. The axial terminated capacitors should be oriented in the direction where the opposite plates have equal self-inductances, and thereby better cancellation of magnetic field, however the circular terminated ones can be oriented in either direction in this regard.

4. As the terminations of the DC-link capacitors and the modules form coplanar structures and share the highest portion of the loop inductance, apart from choosing the capacitors with low internal inductance, their terminations should be made stripline whenever possible.

5. SiC MOSFET modules with multiple pins or screws and multiple DC-sources should be employed for further minimizing stray inductance.

6. Q3D simulation showed higher current density towards the transistor module connection side compared to the supply side when used multiple capacitors in parallel, indicating that the components away from the transistor module are bypassed, that is, capacitor closer to the switching device provides a low inductance path for switching transients, thus it is recommended to orient capacitors in a circular fashion towards the module side.

Chapter 8

Conclusions and Future work

This chapter presents the main conclusions drawn from the findings and contributions of the PhD project, which have been presented in the preceding chapters of the thesis. In addition, some ideas for future work are also discussed.

8.1 Summary and conclusions

This section is divided into seven different points. Each point summarizes and discusses the outcomes from the respective chapter. Chapter 1 primarily states research motivation, Chapter 2 summarizes the state-of-the-art SiC devices, and the advantages and challenges associated with them. The central contributions of this thesis are presented in Chapters 3–7 addressing the defined research objectives.

Chapter 1. clarifies that power electronics benefit society by saving energy and minimizing the carbon footprint. The emerging SiC power devices enable applications, such as transportation electrification, data centers, variable-speed motor drives, and renewable energy integration to be potentially more efficient, more reliable, more thermally stable, and more compact compared to the currently well-established Si technology. Moreover, the high-voltage applications employing series connection of Si IGBTs and multi-level converter topologies become simpler in addition to the aforementioned features by the use of high-voltage (10–20 kV) SiC devices when they become available. Most importantly, the ability of SiC to operate efficiently at high temperatures potentially enables high power density devices not achievable with Si electronics [11, 12, 98, 225]. Therefore, it is essential to evaluate these devices, quantify the performance gain over their Si contenders, address the potential challenges they may entail, and develop the design guidelines to unleash the full-potential they offer, which is the main motivation for carrying out this research.

Chapter 2. compares the material properties of 4H-SiC with Si, GaAs, and GaN. On this basis, it explains how the superior physical properties of SiC can be translated to develop better semiconductor devices with higher voltage, lower conduction and switching losses, higher operating temperature and faster heat extraction out of the device. In addition, this chapter provides an overview of the commercially available SiC devices, for example, SiC Schottky diodes, SiC MOSFETs, SiC JFETs and SiC SJTs. These devices have voltage ratings $\leq$ 1.7 kV. In addition, the devices in research, such as higher voltage SiC MOSFETs (10–15 kV), SiC JFETs (up to

6.5 kV), SiC BJTs (up to 15 kV), SiC IGBTs (upto 20 kV) are also discussed along with the challenges associated with each type. An overview of different commercially available packages used for SiC devices and the stray inductance encompassed by each of them is briefly provided. Moreover, the challenges in releasing the benefits of SiC devices are addressed.

Chapter 3. **recommends using realistic circuit configuration for an accurate assessment of switching loss for two reasons: first, parasitics dictate the switching signals and switching losses. Second, only the real converter configuration generates the realistic output/load current** (for example, in resonant inverter, the output current has a sinusoidal shape, while in a hard-switched inverter, it has a square shape), **and thereby a realistic switching loss, which is proven in this chapter.** Besides, **the significance of using the resonant inverter over hard-switched inverter both for minimizing the switching loss and oscillations is emphasized and substantiated via measurement results.** The major issues impacting the high-speed measurements are explained. Measures for accurately capturing the fast switching transients, such as current and voltage probes with adequate high-bandwidth and rangeability, probe-tip adapter for curtailing the connection inductances, adjustments of probe delays, are implemented.

Chapter 4. Chapter 2 provides an insight into the potential benefits of SiC devices. However, it is imperative to quantify what exactly can be achieved given these devices are packaged in standard plastic housing as today, particularly, in terms of switching speed. Thus, Chapter 4 characterizes state-of-the-art SiC MOSFET modules to resolve this research question. **Via laboratory measurements, it is found that the highest attainable dv/dt and di/dt with 1200 V, 120 A SiC MOSFET modules are 35 V/ns and 10 A/ns, respectively, given the package is 62 mm type.** Another frequently asked question is how much performance gain the SiC MOSFET module offers compared to the class-leading Si IGBT module, provided the same packages. This question was answered via measurements adopting the same experimental setup for SiC MOSFET and Si IGBT module. First, **the highest achievable dv/dt and di/dt for 1200 V, 300 A, Si IGBT module are roughly 17 V/ns and 12 A/ns, respectively, and for the same rating SiC MOSFET module those are 20 V/ns and 11 A/ns, respectively.** In order to further investigate this question, modules were compared under similar dv/dt and di/dt conditions. In the former case ($dv/dt \approx 13$ V/ns), turn-off switching energy loss in Si IGBT was measured to be higher by a factor of 1.5, while in the latter case ($di/dt \approx 9$ A/ns), the turn-on switching energy loss was higher by a factor of 3 in Si IGBT compared to SiC MOSFET. These figures show that **there is obviously certain performance gain in using SiC MOSFET, but it is not as revolutionary as SiC potentially can offer.** In fact, **this is the result of poor packaging.** Manufacturers use high internal gate resistor (for instance, 18 Ω before each parallel chip in the CAS300 module from Wolfspeed) to avoid oscillations during turn-off. Moreover, these modules were compared at similar dv/dt and di/dt per chip area, which showed SiC MOSFET incurs higher switching loss and potentially higher junction temperature. Hence, an SiC device is anticipated to have a larger thermal ripple, demanding a more stringent requirement for package

material compared to Si device. The next most commonly raised question is where and by what quantity SiC can benefit the most today. To address this question, a set of class-leading Si-IGBT versus SiC MOSFET was tested at high junction temperature, which revealed that switching loss of SiC is almost unaffected by the operating temperature. However, the losses in Si IGBT are greatly affected by the junction temperature. Notably, the reverse-recovery current of Si diode and the tail current of the IGBT worsen with the increase in temperature. Another point worth noting is that switching behavior of SiC JBS remains intact irrespective of the loading conditions (temperature, and current), while those of Si diode worsens with the same conditions, indicating a clear benefit of the former compared to the latter. **In conclusion, high temperature ($\leq$ 175 °C) applications benefit the most from SiC MOSFETs today (even with the existing package).** Better packaging enables further high temperature ($\geq$ 175 °C) and high frequency applications. Therefore, considerable research is ongoing in the high power, low inductance, and high temperature module packaging to unlock the true potential of SiC.

Chapter 5. As a MOSFET structure exhibits intrinsic-diode (also called parasitic- or body-diode), it is of great interest to know whether this diode is useable. In order to verify this, a couple of new-generation SiC MOSFETs were chosen and the switching quality of body-diodes was investigated at similar di/dt (dictated by the control transistor at the first-half of the reverse-recovery), particularly to watch the di/dt during the second-half of the recovery (governed by the diode technology) and the current peak itself. **Measured results revealed that these body-diodes exhibit almost the same switching characteristics as that of the SiC JBS.** As the conduction losses are only significant during the dead-time and the diodes are normally shunted by the transistor during the conduction phase, it was concluded that body-diodes of SiC FETs are good enough as freewheeling diodes. Operating the converter as diode-less (that is, no external anti-parallel diode as it is popularly used today in converters to provide current path in the reverse direction) helps to curtail cost of extra components, resulting in a compact, and low-inductive module. It is worth noting that other reported efforts have shown that the body-diodes in new generation SiC MOSFETs are robust and do not degrade SiC MOSFETs' performance like those in the initial generation SiC MOSFETs. It is also worth noting that there are chips available with integrated SiC Schottky diode in SiC MOSFET chip, for instance Panasonic/Sanrex DioMOS chip.

Chapter 6. presents three potential applications of SiC MOSFETs: motor drive, induction heating and power factor correction. In the first application, a 240 kW, back-to-back connected, two-level, three-phase, voltage source converter was evaluated. This effort responded to one of the research questions by quantifying the potential performance gain that the commercially available SiC MOSFET can bring over the state-of-the-art Si IGBT, from an efficiency perspective. **Through the combination of experimental and simulation results, it is revealed that the solution with SiC MOSFET is more efficient at high frequency and high temperature compared to that with Si IGBT.** Specifically, it is illustrated that **for the same output power the inverter switching frequency can be increased by roughly six times in the SiC MOSFET compared to that**

in the Si IGBT keeping the total power loss similar. In the second application, an approximately 80 kW, SiC DioMOS-based, single-phase, full-bridge resonant inverter is evaluated via a calorimetric loss measurement method. **It is verified that the inverter achieves an efficiency of 99.3% when switched at roughly 200 kHz. It is important to remark that the current and voltage graphs from oscilloscope showed no oscillations substantiating a low-inductive DC-link design.** This work was the basis for making a 1.85 MW, 300 kHz welder put into operation approximately one year later. To the best of the author's knowledge, this is the biggest SiC welder still in operation. In the third application, efficiency and EMI are quantified for a 1 kW continuous conduction mode PFC rectifier. A low-parasitic design approach is employed together with an input EMI filter in this rectifier. **It is corroborated that the efficiency satisfies the 80 PLUS regulation and the EMI complies with CISPR 11 Class B conducted EMI limit.** Furthermore, **when the switching frequency is changed from 66 to 250 kHz, it is demonstrated that the size of the boost inductor was remarkably miniaturized. However, the electromagnetic emissions were increased by roughly 10 dB throughout the entire conducted spectra.**

Chapter 7. To fully realize the fast switching potential promised by the SiC technology, ancillary components, such as packages and passive components, should be able to live in the same environment as SiC. Thus, a number of research teams have been investigating the potential direction of low-inductive, high temperature transistor cases and busbars [25–28]. Nonetheless, employing low stray inductance DC-link capacitors is essential for realizing the low stray inductance designs. Reviewing the commercially available low inductance DC-link capacitors with different physical sizes and terminations and analyzing the geometry and orientation of the DC-clamping capacitor for minimizing the SiC transistor turn-off over voltages, the design of a DC-link for a 100 kW full-bridge AC-DC-AC converter is presented in this thesis. Via an FEA tool, the parasitics of the bussing structure are computed. **It is shown that the majority of switching loop stray inductance is shared by the transistor and capacitor module terminations apart from the module housing itself. To overcome this challenge, a planar busbar with multiple DC-source and multiple screw hole modules is proposed, which resulted in bussing inductance of 2.4 nH (82% reduction compared to the classical design).** Further, to minimize the total switching loop stray inductance, a 20 kW inverter layout is designed adopting four TO-263-7 SiC MOSFET packages in parallel. FEM results disclosed that a record low inductance of 5 nH is acquired, the central reasons for which are: the use of Ceralink capacitors as they have small heights, seven-pin package of SiC MOSFET itself, and transmission line like assembly of busbar such that the width to length ratio is greater than 1. Thus, Chapter 7 provides guidelines for low-inductive designs in this respect.

8.2 Suggested future work

This thesis, aside from addressing the research objectives, has raised additional research questions. Some potential directions for future work are provided below.

1. Chapter 5 investigated the switching performance of body-diode in SiC MOSFETs at room temperature. Further examination of these devices at high temperatures is a potential topic for future work.

2. Chapter 7 presented a record low inductance (5 nH) layout design for a 20 kW inverter via FEA simulations. A possible next step would be an experimental validation of the design.

3. A discrete SiC MOSFET offers extremely low conduction and switching loss, enabling MHz of switching frequency in an inverter. As frequency is the main driver for induction heating applications, to realize a MHz switched inverter, a simulation model was developed in MATLAB Simulink for a 20 kW inverter switched at 2 MHz. Using the ideal switch model (no output C_{oss}), the switching current was observed, which revealed that there was no negative current during turn-on. Next, using the real switch model, i.e., the SiC MOSFET switch with output C_{oss} and internal inductance, an LTSpice model of the same inverter with similar switching conditions was investigated. Simulation results showed that a negative current existed during the switch turn-on. The author believes that this current is the C_{oss} discharging current in the upper switch. Moreover, if the power area in the negative side is maintained equal to that in the positive direction while turning off the lower switch, then close-to-lossless switching can be achieved. As SiC MOSFET switches in the order of 100 V/ns, this outcome is feasible, that is, the current can be switched off instantly like an ideal switch. A simulation model and the outcomes are provided in Appendix D. Thus, another proposal for future work would be to verify this concept experimentally via a calorimetric loss measurement method.

Appendix A

LTSpice Simulation for analyzing the impact of parasitics in the switching

A.1 Impact of stray inductance

A simulation study is performed in a hard switching configuration as shown in Fig. A.1 for the Rohm MOSFET module. The focus of the simulation is to study the impact of L_{stray} and stray inductance in gate side (L_g, as indicated in Fig. A.1) in the switching transients with the aim of shedding light on the experimental results in Chapter 4.

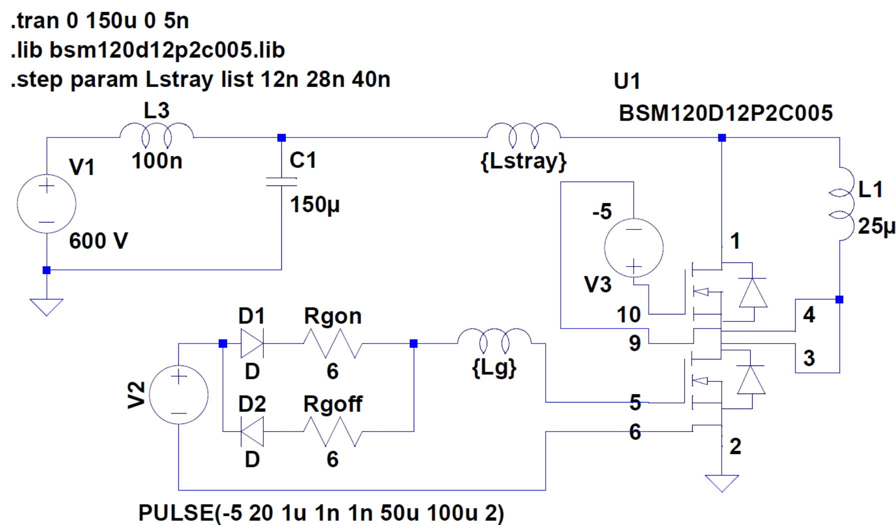
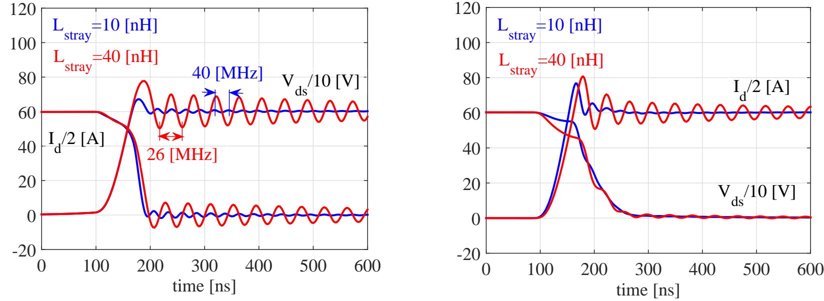


Figure A.1: Simulation model in LTSpice for the study of impact of stray inductances.

A.1.1 Impact of switching-loop inductance

The simulated turn-off and turn-on switching transients for two different values of L_{stray} are shown in Fig. A.2. With an L_{stray} of 10 nH, the frequency of oscillation is 40 MHz, while it is 26 MHz with an L_{stray} of 40 nH. V_{os} and I_{os} are higher and oscillations are larger and longer with higher L_{stray}. There are noticeable decrements in current slew rates



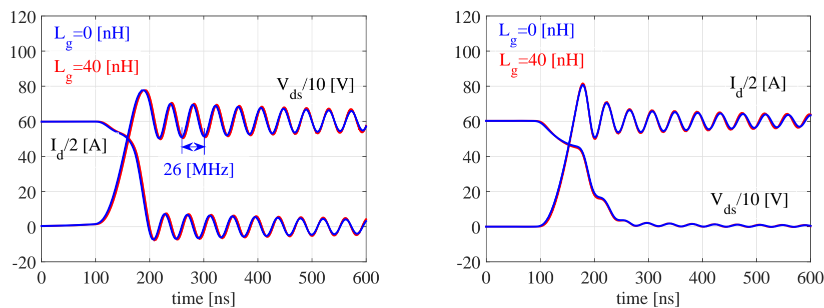
(a) Turn-off of BSM120D12P2C005 (Rohm). (b) Turn-on of BSM120D12P2C005 (Rohm).

Figure A.2: LTSpice simulation of turn-off and turn-on switching transients with two different values of L_{stray}, provided $R_{g,ext} = 6\ \Omega$. Note that an LTSpice model of a half-bridge SiC MOSFET module, BSM120D12P2C005, is considered to investigate the impact of parasitic inductance. Clearly, the higher the L_{stray}, the higher the overshoot and larger and longer the oscillations.

both during turn-on and turn-off transients with larger L_{stray}, thereby slowing the SiC transistors. Note that in Fig. A.2 (a), when di/dt is reduced, voltage overshoot or voltage drop is still increased because loop inductance is increased by more than the amount di/dt is reduced.

A.1.2 Impact of gate-loop inductance

Fig. A.3 illustrates the switching transients with an L_{stray} of 40 nH for two different values of L_g. The impact of L_g on the oscillations and slew rates is not as significant as that of L_{stray}. Nonetheless, it slows down the device a little.



(a) Turn-off of BSM120D12P2C005 (Rohm). (b) Turn-on of BSM120D12P2C005 (Rohm).

Figure A.3: LTSpice simulation with two L_g values; 0 nH and 40 nH, keeping $L_{stray} = 40$ nH and $R_{g,ext} = 6\ \Omega$.

A.2 Impact of stray capacitance

A simulation model in LTSpice is used for studying the impact of C_{gs}, C_{ds}, and C_{gd}. An example with C_{gd} connected in the model is shown in Fig. A.4. For the other cases: C_{gs} and C_{ds} variations, the capacitors are connected between the respective terminals of the MOSFET. The values are chosen as per the data sheet of the chosen modules, as listed in Table 4.5, and are considered for the case with V_{ds} of 600 V. Although, these capacitors show non-linear variations with V_{ds}, a constant value is taken into account because it is sufficient for relative performance evaluation. LTSpice model of SiC MOSFET is from Wolfspeed. This section is divided in three subsections. The simulated turn-off and turn-on transients of the currents and voltages in both the gate and drain sides with different C_{gs}, C_{ds}, and C_{gd} are elaborated in Subsection A.2.1, Subsection A.2.2 and Subsection A.2.3, respectively.

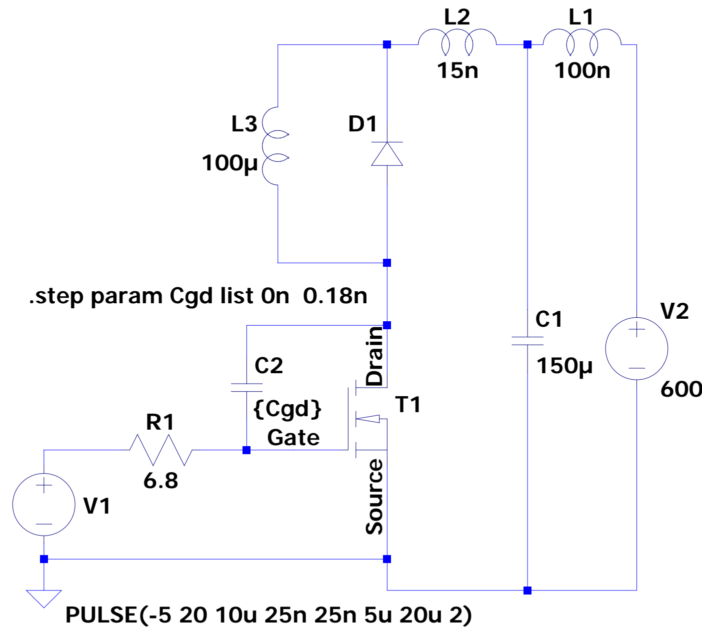
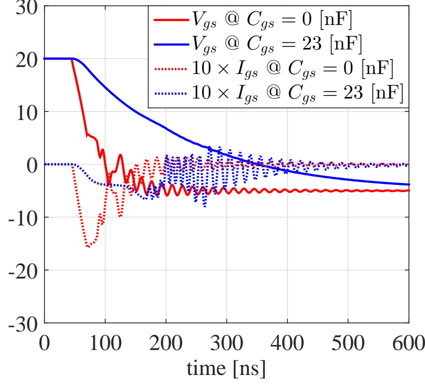


Figure A.4: Simulation model in LTSpice for the study of impact of stray capacitances. For a case with C_{gd} variation, a capacitor is connected between the gate and drain terminals of MOSFET as depicted in the model. For the other cases: C_{gs} and C_{ds} variations, the capacitors are connected between the respective terminals of the MOSFET. The values are chosen as per the data sheet of the modules, as catalogued in Chapter 4, Table 4.5, and are taken for the case with V_{ds} of 600 V. Spice model of SiC MOSFET is from Wolfspeed.

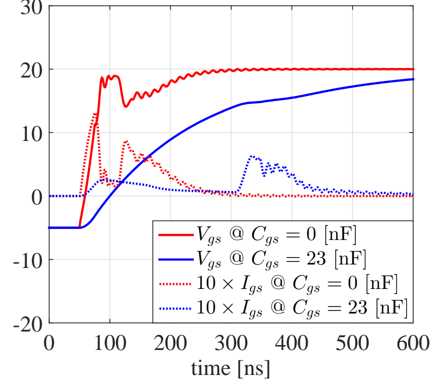
A.2.1 Impact of gate-source capacitance

The simulated switching waveforms with varied C_{gs} are illustrated in Fig. A.5. With higher values of C_{gs}, the slew rates in gate voltages are reduced significantly, the oscillations are mitigated and the delay times are prolonged, which are evident from Fig. A.5

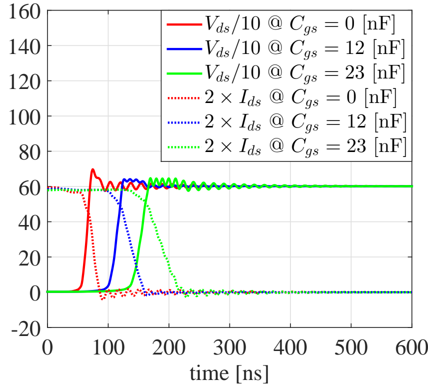
(a) and Fig. A.5 (b). As a consequence, there is a decrease of slew rates in drain currents (I_{ds}) as depicted in Fig. A.5 (c) and Fig. A.5 (d). Thus, the decreased slew rates and lengthened switching time durations will subsequently increase the switching losses.



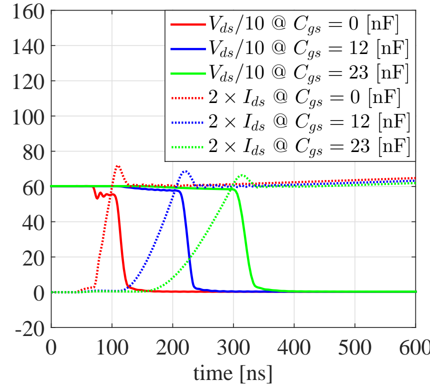
(a) Turn-off gate waveforms with different C_{gs}.



(b) Turn-on gate waveforms with different C_{gs}.



(c) Turn-off drain waveforms with different C_{gs}.



(d) Turn-on drain waveforms with different C_{gs}.

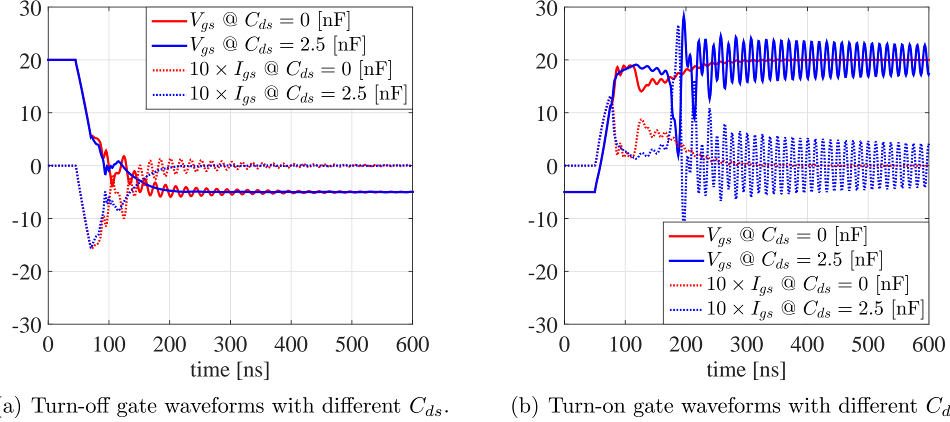
All simulations are performed at drain-source voltage of 600 V and drain-source current of 30 A. V_{ds} are plotted with ten times lower scale and I_{ds} with two times higher scale. Gate current waveforms (I_{gs}) are plotted with ten times higher scale for better clarity. Chosen values of C_{gs} in the simulation are as per the data sheet of the selected modules, as listed in Table 4.5. The gate resistor is kept constant as in Fig. A.4 (6.8 Ω).

Figure A.5: Impact of different gate-source capacitances on gate and drain waveforms illustrating that these primarily determine the time constant of gate circuit and the slew rates of drain currents.

A.2.2 Impact of drain-source capacitance

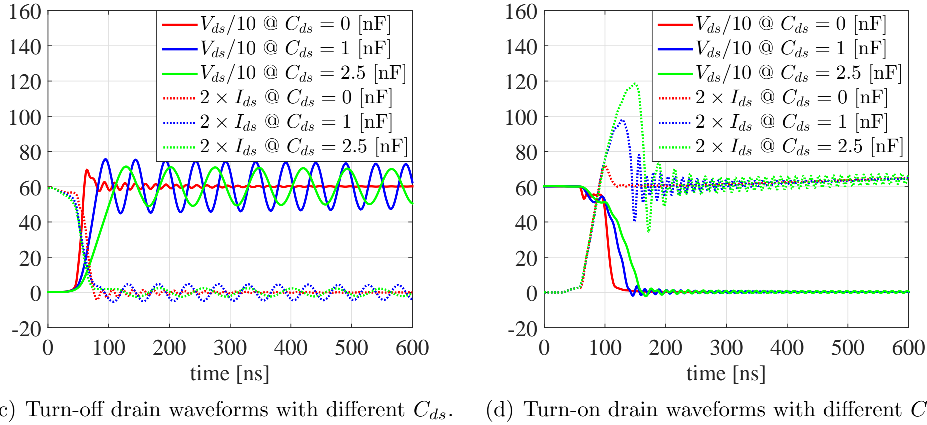
Fig. A.6 presents the simulated switching waveforms with varied C_{ds}. The larger the value of C_{ds}, the larger the noise in I_{gs} and V_{gs} waveforms during turn-on, as shown in Fig. A.6 (b). Furthermore, it is evident from Fig. A.6 (c) and Fig. A.6 (d) that the

voltage slew rates become slower and the frequency of oscillations become smaller with higher values of C_{ds}. In addition, the current slew rates become slightly faster leading to higher current overshoots, as illustrated in Fig. A.6 (d).



(a) Turn-off gate waveforms with different C_{ds}.

(b) Turn-on gate waveforms with different C_{ds}.



(c) Turn-off drain waveforms with different C_{ds}.

(d) Turn-on drain waveforms with different C_{ds}.

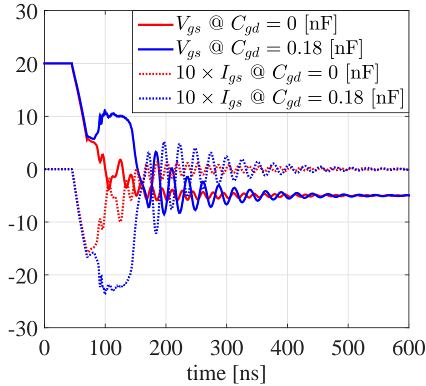
All simulations are performed at drain-source voltage of 600 V and drain-source current of 30 A. V_{ds} are plotted with ten times lower scale and I_{ds} with two times higher scale. Gate current waveforms (I_{gs}) are plotted with ten times higher scale for better clarity. Chosen values of C_{ds} in the simulation are as per the data sheet of the selected modules, as listed in Chapter 4, Table 4.5. The gate resistor is kept constant as in Fig. A.4 (6.8 Ω).

Figure A.6: Impact of different drain-source capacitances on gate and drain waveforms illustrating that these primarily determine the parasitic ringings and slew rates of drain voltages.

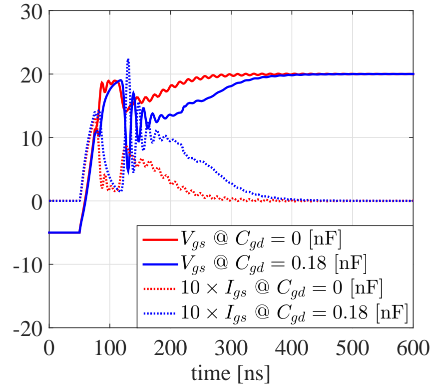
A.2.3 Impact of gate-drain capacitance

Fig. A.7 exemplifies the simulated switching waveforms with varied C_{gd}. It is apparent that both the gate current and voltage waveforms oscillate when C_{gd} increases, which is essentially because of dv/dt related noise coupled to gate side through miller capacitor (C_{gd}). This noise can exceed the threshold voltage limit of SiC MOSFET and cause

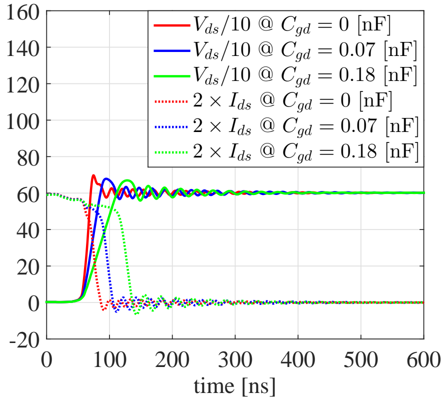
unwanted turn-on of the device. In addition, it should be noted that the increase in C_{gd} hardly affects the time constant of V_{gs}. Besides, there is visible decrease in slew rates of V_{ds} waveforms, which is clearly shown in Fig. A.7 (c) and Fig. A.7 (d). However, the slew rates of I_{ds} are not affected at all, except that during turn-off I_{ds} are slightly delayed. Thus, the decreased voltage slew rates and delayed current slew rates result in increased switching losses.



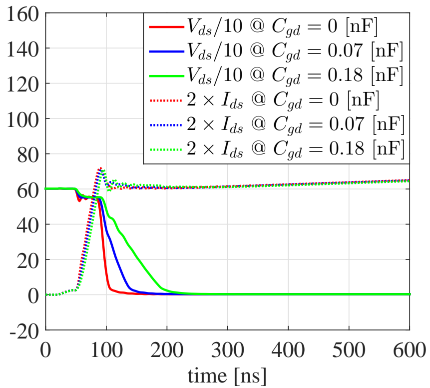
(a) Turn-off gate waveforms with different C_{gd}.



(b) Turn-on gate waveforms with different C_{gd}.



(c) Turn-off drain waveform with different C_{gd}.



(d) Turn-on drain waveforms with different C_{gd}.

All simulations are performed at drain-source voltage of 600 V and drain-source current of 30 A. V_{ds} are plotted with ten times lower scale and I_{ds} with two times higher scale. Gate current waveforms (I_{gs}) are plotted with ten times higher scale for better clarity. Chosen values of C_{gd} in the simulation are as per the data sheet of the selected modules, as presented in Chapter 4, Table 4.5. The gate resistor is kept constant (6.8 Ω as in Fig. A.4) throughout the simulation.

Figure A.7: Impact of different miller capacitances on gate and drain waveforms illustrating that these primarily determine the slew rates of drain voltages.

Appendix B

3D FEM simulation for low inductive circuit designs

B.1 Modelling of busbar in Ansys Q3D extractor

In this section, the fundamentals of modelling of busbar in Ansys Q3D extractor are described. A busbar for single-phase, half-bridge converter is presented as an example to illustrate the modelling procedure in the software. In order to model the busbar which functions as two conductors carrying the current in opposite directions, overall, three steps have to be followed.

First, a 3D geometric structure of the busbar should be built, i.e., dimensions of the busbar are taken as input parameters. Additionally, the material characteristics for each object should be specified. Second, as the stray inductance and resistance depend on the current conduction loop, the current direction, both source and sink, for each conduction path must be specified. This step is further explained in the following sub steps. Initially, the start face in the first conductor is assigned as source 1 and the end face as sink 1. Thereafter, the start face is assigned as sink 2 and the end face as source 2 in the second conductor. Fig. B.1 further clarifies which terminals are excited as sources and which as sinks. Third, the two busbars should be connected in series so that the loop inductance can be calculated. For that, the sink 1 and the source 2 are assigned as in series connections. These steps model the two plates as a transmission line where the positive and negative plates are just on top of each other. The software generates the necessary impedance matrices which can be represented by the lumped element circuit model as in Fig. B.2, where L_{11} and L_{22}, C_{11} and C_{22}, and R_{11} and R_{22} are the self-inductances, capacitances and resistances respectively. Likewise, L_{12} and L_{21}, C_{12} and C_{21} are the mutual-inductances and capacitances. As the two busbars are modelled as current carrying conductors in opposite directions, the loop inductance is also generated which follows (B.1). It should be noted that ESL of capacitor is not considered in the calculation.

$$L_{loop} = L_{11} + L_{22} - 2L_{12} \tag{B.1}$$

A method to achieve lower inductance is the paralleling of many connections, that is why capacitors with several pins are chosen. The opposite pins of the bypass capacitor are separated by 24 mm, and the height is 4 mm. These terminations effectively make

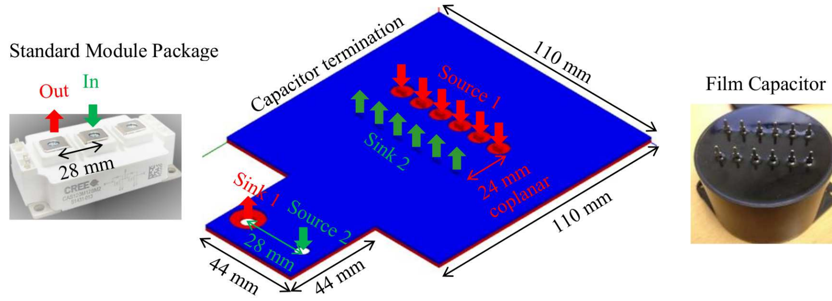
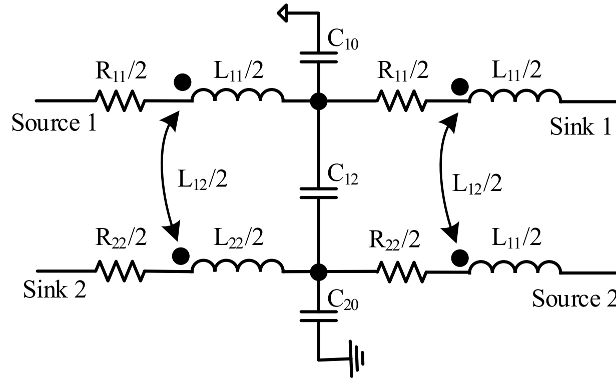


Figure B.1: Picture illustrating a standard module package with screw holes at 28 mm separation (left), a film capacitor with six pins where the opposite pins are at a distance of 24 mm (right) and a busbar connecting these two components (middle). w/l ratio of the busbar in both the capacitor and module sides are kept at 1 to achieve low inductance.



Note: The variables used in Fig. B.2 are: R_{11} and R_{22}, resistances; L_{11} and L_{22}, self-inductances; L_{12} and L_{21}, mutual-inductances; C_{11} and C_{22}, self-capacitances of each conductors (not shown in the model); C_{12} and C_{21}, mutual-capacitances, C_{10} and C_{20}, capacitances between the conductor and ground.

Figure B.2: Lumped element circuit model of busbar.

the corresponding part of the busbar coplanar. The screw terminations of the modules are 28 mm apart, however, the DC-link busbar is made such that there is some overlap (12 mm) in the termination part. This makes the effective distance between the terminations smaller. The self- and mutual-inductance, as in Fig. B.2, are L_{11} = 30.7 nH, L_{22} = 19.31 nH, and $L_{12} = L_{21}$ = 18 nH respectively, and the loop inductance L_{loop} is 14 nH. The difference in self-inductance between the two opposite plates is also the indication that the capacitor termination is coplanar.

Furthermore, the distribution of current density in the busbar from Ansys Q3D is exemplified in Fig. B.3, where the red color shading indicates the higher current density. The major parts of the current are concentrated around the holes, sharp corners and edges, therefore, it is essential to minimize the number of holes and make the edges round, which results in an increase of surface area. These considerations will eventually minimize the stray inductance. In addition, **the part of the busbar which has not contributed in**

the current flow can be eliminated. Consequently, a more compact and a lightweight converter is possible. The excluded parts and the round edges are depicted in Fig. B.3 (b).

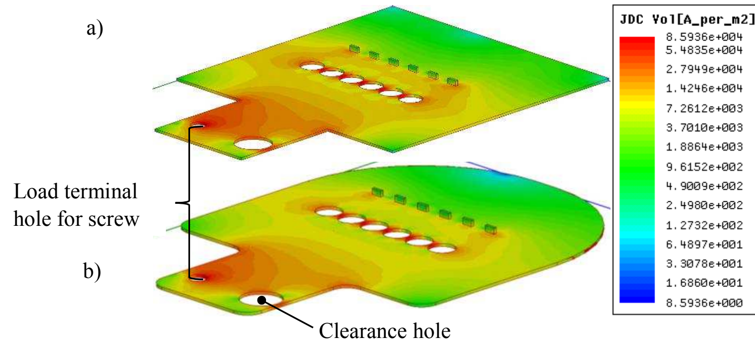
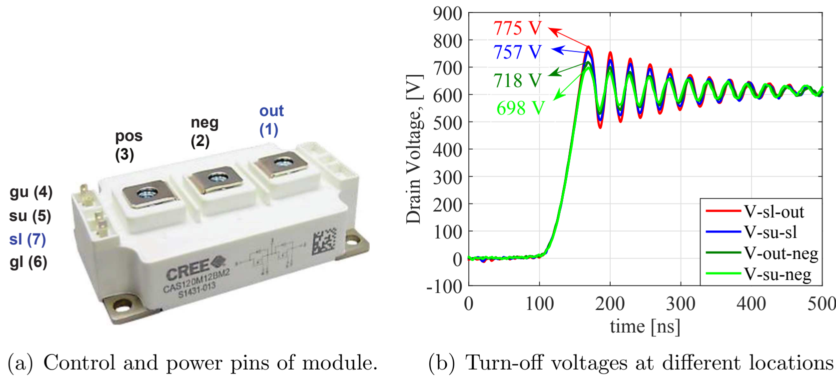


Figure B.3: Distribution of current density in the busbar from Ansys Q3D, red color shading indicates higher current density. Most of the current is concentrated towards the capacitor pins and the load terminals as they are identified to be coplanar structures. The part of the busbar that has not contributed in the current flow can be eliminated and the sharp edges can be made round, as shown in Fig. (b).

B.2 Estimation of stray inductance via measurement and analytical expression

The physical placement of the voltage probe is very important, and needs to be closer to the chips in order to measure the most accurate voltage stress on the device. Fig. B.4 (a) shows the control and power terminals of a SiC MOSFET module, and Fig. B.4 (b) shows the drain voltage measured across various different terminals. As the energy stored across the stray inductances during the turn-on will be discharged during the turn-off increasing the voltage overshoot, to select the pins closest to the chip, the measurement that gives the highest overshoot is chosen, which is between pins sl and out for this module.



(a) Control and power pins of module. (b) Turn-off voltages at different locations.

Note: The abbreviations used in Fig. B.4 are: gu (4) and su (5), upper transistor gate and source pins; sl (7) and gl (6), lower transistor source and gate pins; pos (3), neg (2) and out (1), positive, negative and output terminals of transistor module, respectively.

Figure B.4: Illustration of drain voltage measurement with physical placement of probe at different locations. The most appropriate position being closer to the chips, that is, across the source of the lower transistor and output terminal.

Using (B.2), L_{loop} can be estimated to be 175/5.5 = 31.8 nH. The stray inductance inside the module is 15 nH [127], subtracting it from the total stray inductance, the contribution from the busbar, the bypass capacitor and the current shunt is 16.8 nH.

$$V_{os} = L_{loop} \cdot \frac{di}{dt} \tag{B.2}$$

Alternatively, considering that the circuit has zero resistive loss, the oscillation in the voltage waveform can be approximated by the resonance (B.3). Using the value of f_{osc}, measured via a voltage probe and oscilloscope and C_{stray} measured via an impedance analyzer, L_{loop} can be computed. L_{loop} estimated by (B.3) is more reliable over that computed by (B.2), because the latter does not give the chip level voltage stress.

$$f_{osc} = \frac{1}{2\pi\sqrt{L_{loop} \cdot C_{stray}}} \tag{B.3}$$

Appendix C

Fundamental information for Chapter 6

C.1 Equations for passive component sizing

$$L_B = \frac{1}{\Delta i_L} \cdot \frac{v_{s,min}^2}{P_{out}} \cdot \left(1 - \frac{\sqrt{2} \cdot v_{s,min}}{v_{out}}\right) \cdot \frac{1}{f_{sw}} \tag{C.1}$$

$$C_{out} = \frac{2 \cdot P_{out} \cdot t_{hold}}{v_{s,min}^2 - v_{out,min}^2}, = \frac{P_{out}}{2 \cdot \pi \cdot f_{line} \cdot \Delta v_{out} \cdot v_{out}} \tag{C.2}$$

The higher value of C_{out} is considered to be the output capacitor size for the design.

Note: The variables used in (C.1) and (C.2) are: L_B, inductance of boost inductor; Δi_L, boost inductor ripple current; $v_{s,min}$, minimum input voltage; P_{out}, output power; v_{out}, output voltage; f_{sw}, switching frequency; $v_{out,min}$, minimum output voltage; t_{hold}, hold-up-time; Δv_{out}, output voltage ripple; and f_{line}, lines/mains frequency.

C.2 Equations for conduction loss calculation

$$\begin{aligned} P_{cond}(rectifier) &= 2 \times (I_{L,rms}^2 \times R_d + I_{L,avg} \times V_{FO}) \\ P_{cond}(inductor) &= I_{L,rms}^2 \times DCR \\ P_{cond}(capacitor) &= I_{c,rms}^2 \times ESR \\ P_{cond}(MOSFET) &= I_{ds,rms}^2 \times R_{DS,on} \\ P_{cond}(diode) &= I_{d,rms}^2 \times R_d + I_{d,avg} \times V_{FO} \end{aligned} \tag{C.3}$$

Note: The variables used in (C.3) are: P_{cond}, conduction loss; $I_{L,rms}$ and $I_{L,avg}$, rms and average current of diode rectifier; $I_{d,rms}$ and $I_{d,avg}$, rms and average current of boost diode; $I_{ds,rms}$, rms current of MOSFET; and $I_{c,rms}$, rms current of output capacitor.

C.3 A complete schematic diagram and component layout of PFC rectifier (two-layer board)

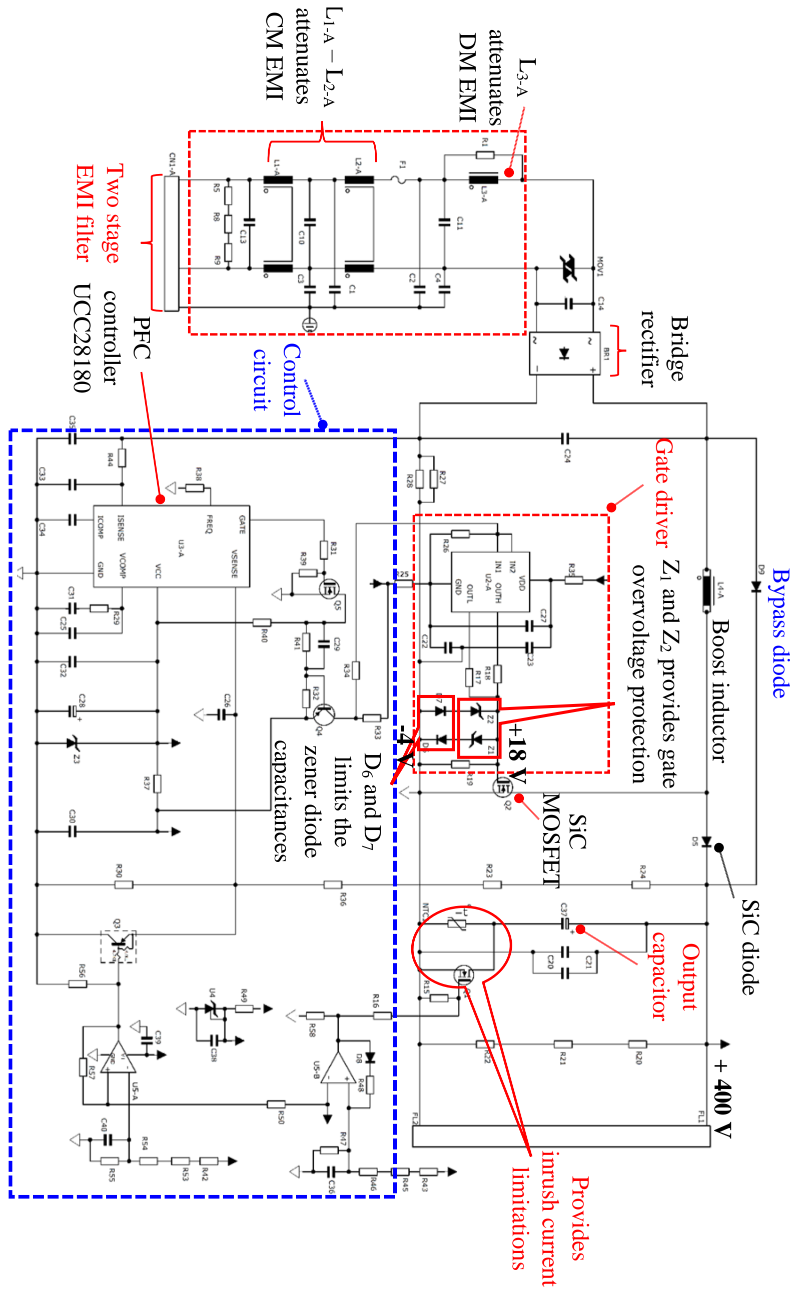


Figure C.1: A complete schematic diagram of the PFC rectifier prototype board.

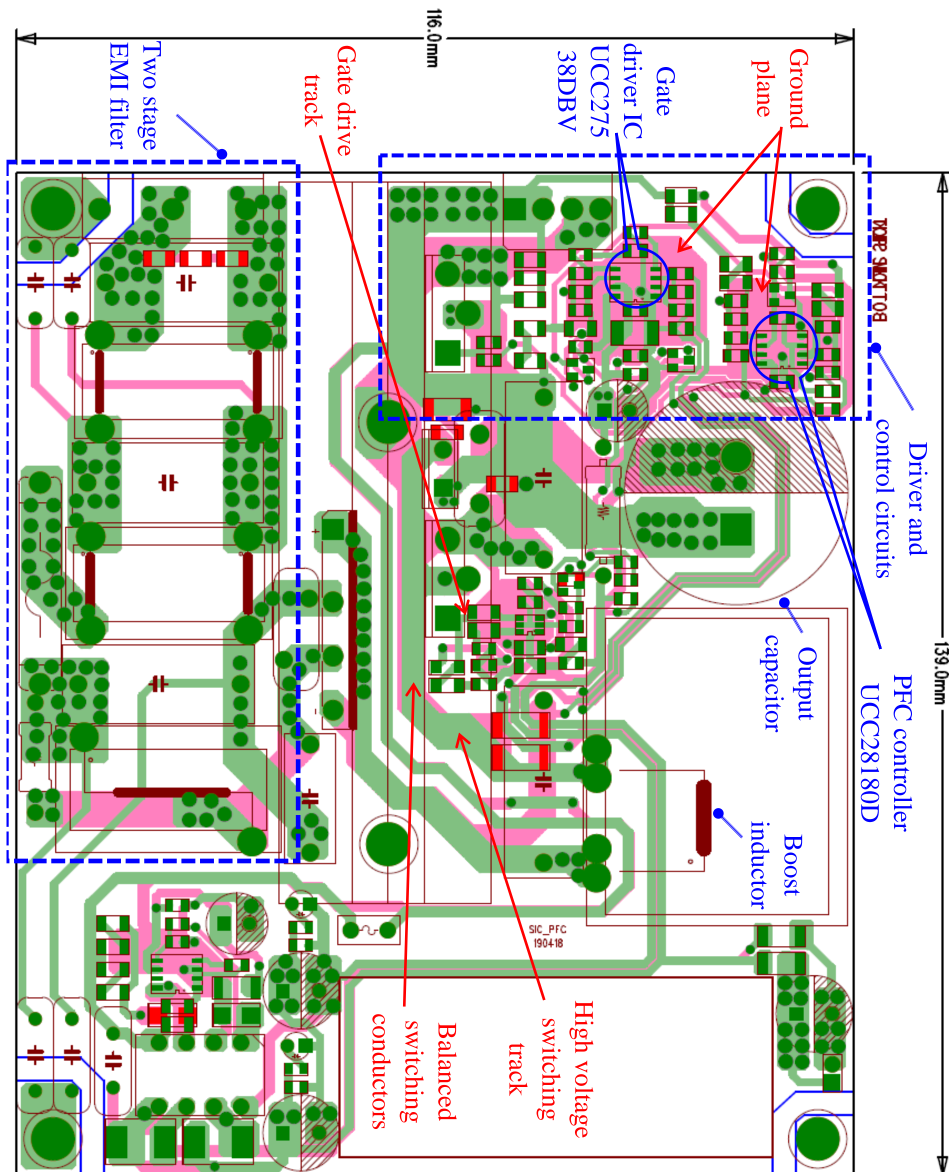


Figure C.2: A complete component layout and routing of the PFC rectifier prototype board (two-layer board).

Appendix D

An insight into close-to-lossless switching enabled by SiC MOSFET

SiC offers lower input and output capacitances compared to their Si counterparts, thereby posing an inherent potential to reduce the dynamic power loss, provided the low inductive switching loop is ensured. Therefore, for fully unleashing the fast switching benefits of SiC MOSFET, a symmetrical and a low inductive design of switching loop for a single-phase, full-bridge inverter is addressed in this chapter. Employing a 3D FEM model, the insight into the physical behavior of the current flow in a switching loop is identified. Essentially focusing on the proper orientation and distribution of the DC-clamping capacitors and SiC MOSFETs, this work demonstrates that the parasitic inductance of 3 nH including the bussing structure and connections can be achieved. A 20 kW series-resonant inverter switched at 2 MHz is simulated via an LTSpice. The model includes the device parasitics of the DC-clamping capacitors and the third generation SiC MOSFET from Wolfspeed, C3M0065090J, and circuit parasitics of 3 nH extracted from FEM simulation. At a peak load current, the inverter yielded a voltage overshoot of less than 11% of the DC-link voltage. This is the reported lowest value of loop inductance employing discrete SiC MOSFET with TO-263-7 package. In addition, explaining the detailed switching process, this work provides insight into how a close-to-lossless switching can be achieved. The concept is verified via simulation results in a 20 kW SiC-based resonant inverter.

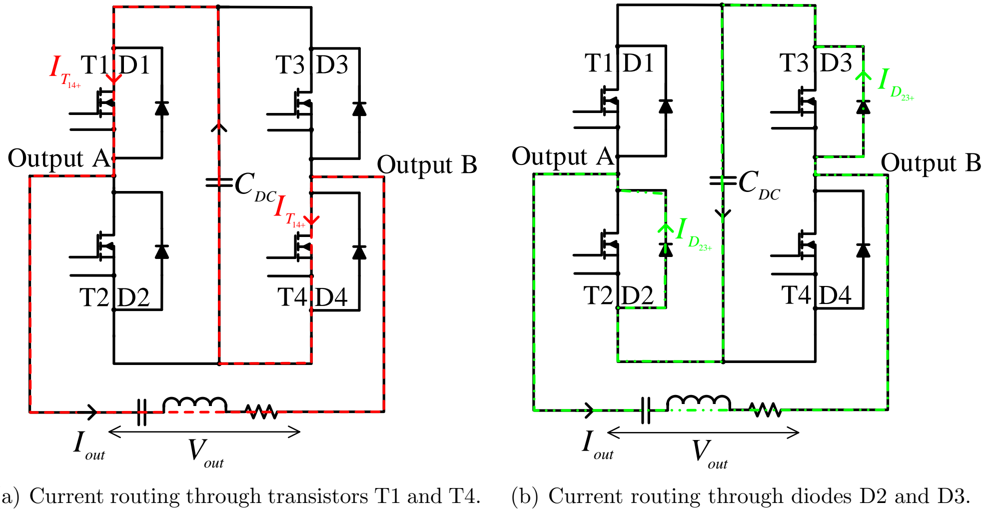
D.1 Introduction

In a sine wave current switched inverter, such as LLC resonant for induction heating applications, there are predominantly two reasons for designing the low inductive current commutation loop. First, to ensure safety, particularly during failure; i.e., in such an inverter, often, a short circuit is incurred by the shorting of coil and the work piece (which is supposed to be contactless), and the inverter needs to be turned off. With low inductive switching loop, hard turn-off will be even safer, as it does not create too high over voltage at chip level, and there will be no need for soft turn-off and thereby a simpler driver can be used. Second, dynamic loss can be reduced because stray inductance is one of the parameters hindering the device from switching fast to its highest potential.

Therefore, at first, a low inductive circuit layout is designed via Ansys Q3D, the bussing structure and connections of components resulted in a loop inductance of 3 nH. This is principally achieved by the proper selection, orientation and distribution of the DC-

clamping capacitors and SiC MOSFET, and is discussed in Section D.2. Thereafter, the simulated parasitic inductance value from Q3D, and device parasitics of the DC-clamping capacitors are used as inputs in LTSpice tool for simulating the complete inverter setup as in an experimental arrangements in Section D.3, the primary goal of which is to evaluate the voltage overshoot when switching at peak of sinusoidal load current. Note that the Spice model of third generation SiC MOSFET from Wolfspeed, C3M0065090J, includes the parasitics in it. Furthermore, an optimal operating condition is investigated such that SiC MOSFETs operate close to zero switching loss.

D.2 Design of low inductive layout via 3D FEM simulation in Ansys Q3D



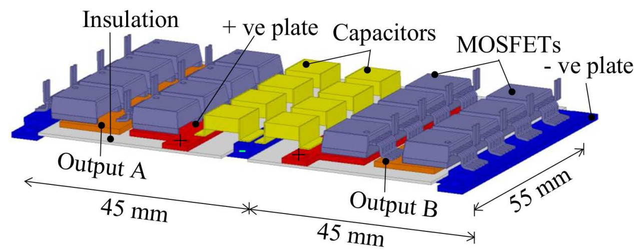
(a) Current routing through transistors T1 and T4. (b) Current routing through diodes D2 and D3.

Figure D.1: (a) and (b) Exemplification of the current flow during the positive polarity of load current. During the negative polarity of the load current, the opposite transistors T2 and T3 and the diodes D1 and D4 function.

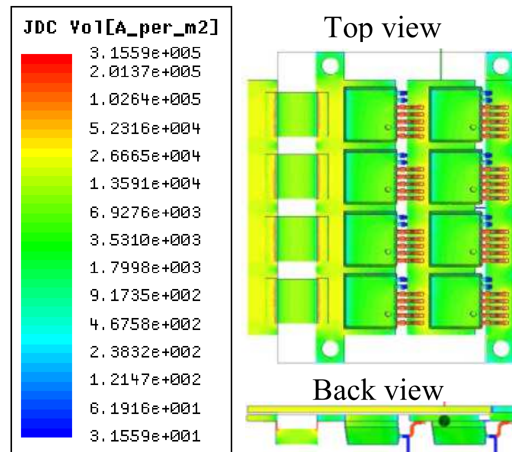
Before delving into the design of symmetrical low inductive layout, it is important to discuss the current commutation loops in a single-phase, full-bridge resonant inverter. Fig. D.1 shows the current flow during the positive polarity of load current. During the negative polarity of the load current, the complementary transistors T2 and T3 and the diodes D1 and D4 operate, which is not shown here. For equal output current and voltage, each current commutation loop should have equal stray inductances, that is, it should be symmetrical. Therefore, the DC-clamping capacitors are mounted in the middle part in Fig. D.1.

By specifying the input parameters, such as 3D geometry, material properties (such as copper for busbar and Kapton for dielectric), and the desired output, an Ansys Q3D extractor generates the necessary impedance matrices which can be represented by the lumped element circuit model. Fig. D.2 (a) shows a complete 3D FEM model of the

components layout in such an inverter, where the DC-clamping capacitors are evenly distributed immediately adjacent to the four paralleled discrete SiC MOSFETs. Several factors which involve low loop inductance are considered in this design. For instance, Ceralink capacitors are chosen as they have small height, low stray inductances and high current capacity; SiC MOSFETs with TO-263-7 packages have low height, separate power and source returns, where five pins are accounted as power return and one as source returns; and copper plates are assembled in a transmission line like layout such that width to length ratio of the current path is kept greater than 1. Fig. D.2 (b) illustrates the FEM simulation of a half-symmetry of the full model as shown in Fig. D.2 (a), the Q3D extracted loop inductance of which is 3 nH. Highly stressed parts are indicated by deep red color shading in the top and back view of the model.



(a) Total geometrical model of a single-phase, full-bridge inverter.



(b) Ansys Q3D simulation of a half-symmetry model.

Figure D.2: (a) A complete components layout in a single-phase, full-bridge inverter, including DC-clamping capacitors, TO-263-7 packaged SiC MOSFETs, copper plates and insulation layer. Width to length ratio of the current path is maintained greater than unity in each of the half-bridges in order to acquire minimum loop inductance. Note that the thickness of copper plate is 1 mm. (b) Illustration of FEM simulation of a half-symmetry model employing Ansys Q3D. Deep red color shading in the current density plot indicates the highly stressed parts in the top and back view of the model and the loop inductance shared by bussing structure and component connections is computed to be 3 nH.

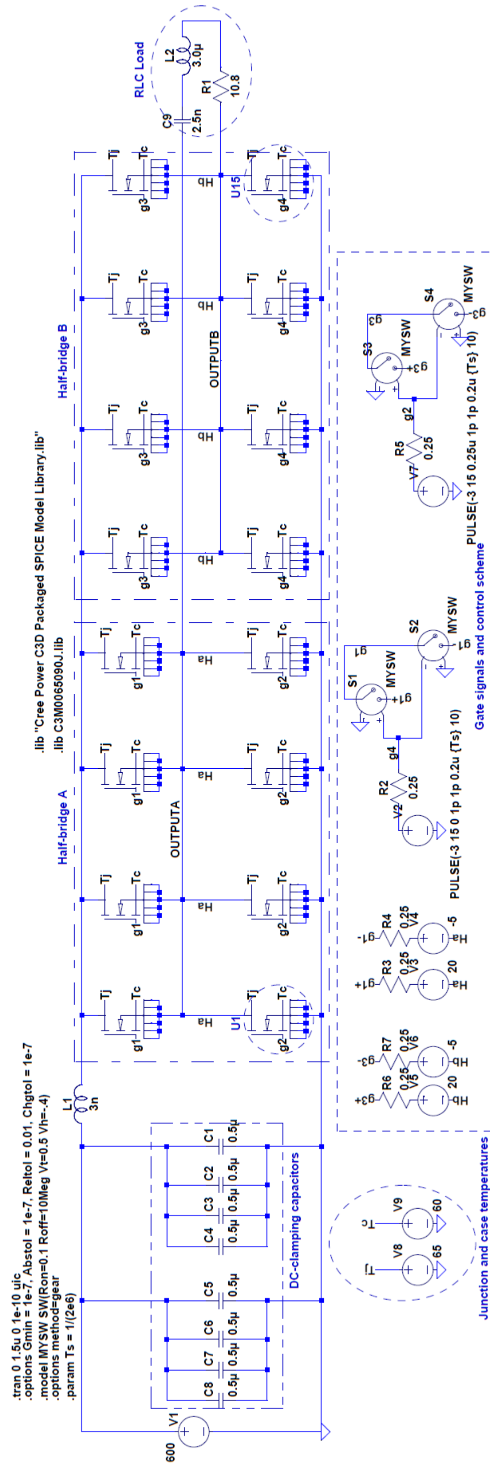


Figure D.3: Illustration of a complete simulation model of a 20 kW series-resonant inverter, switched at a frequency of 2 MHz. Note that these spice models also include package inductance.

D.3 Evaluation of inverter via LTSpice simulations

Fig. D.3 shows the simulated single-phase, full-bridge series-resonant inverter, in which the parasitics of the DC-clamping capacitors, and the device model of the chosen SiC MOSFET and its parasitics are included in order to emulate the realistic switching behaviour. It is worth mentioning that the models used in the LTSpice simulation are: SiC MOSFET (C3M0065090J) from Wolfspeed, and Ceralink capacitor (B58031L7504M062) from TDK [82, 216] which are provided in the respective websites from the companies. Note that these device models also include their internal parasitics. The stray inductance of 3 nH as extracted from the Q3D simulation is used as an input in LTSpice simulation model.

By switching the SiC MOSFET just before the zero crossing of the current (inductive mode) during turn-off and at perfect zero voltage during turn-on, this inverter results in a square wave output voltage and a sine wave output current as shown in Fig. D.4. Specifically, at a switching frequency (f_{sw}) of 2 MHz, which is slightly above the resonant frequency (f_{res}), the turn-off of switches and turn-on of diodes are hard while the turn-on of switches and turn-off of diodes are soft, as exemplified in Fig. D.5. Thus, there are losses associated with the turn-off of the active switch and the forward-recovery of the diode. As the latter part is negligible, the only significant loss is in the device that turns off. With the specified RLC load: 10.8 Ω, 2.5 nF, 3.0 μF, and the DC-link voltage of 600 V, the steady state load current of 60 A peak is obtained, thus the power rating of the inverter is approximately 20 kW ($600 \times 0.9 \times \cos 27.6° \times 60 / \sqrt{2} = 20.30$ kW).

A meticulous tuning of the switching frequency reduces the negative current to zero when used ideal switch, i.e., no parasitic capacitance. However, in employing the non-ideal switch, a negative part in the current waveform will always exist. In order to explain the reason behind this, the switching process has to be clarified at first. During the turn-on process, the output capacitance (C_{gd} + C_{ds}) is discharged, while it is charged during the turn-off process. Thus, this negative current is the capacitor discharge current, which is also mentioned in [226].

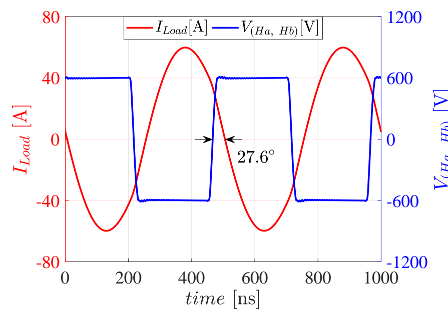
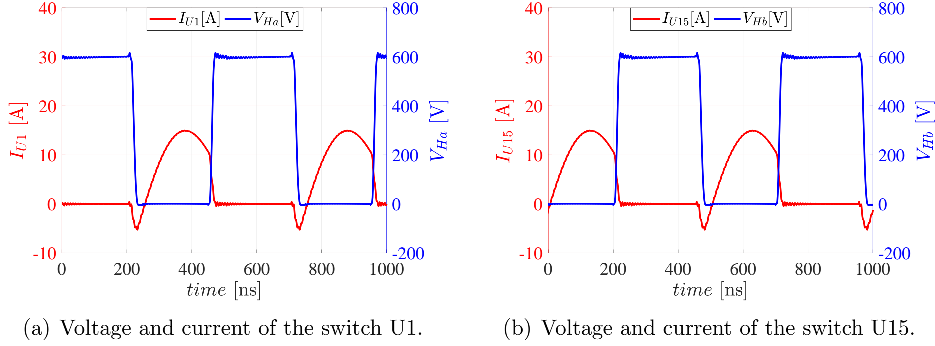


Figure D.4: Simulated output voltage ($V_{(Ha,Hb)}$) and load current (I_{Load}) with square and sinusoidal shapes, respectively, illustrating an inductive mode of switching, where the voltage is leading current by 27.6°. Displacement power factor ($\cos\theta = \cos 27.6° = \Delta T/T \times 360°$, where ΔT is the time by which voltage leads the current) in such an inverter is roughly 0.886.



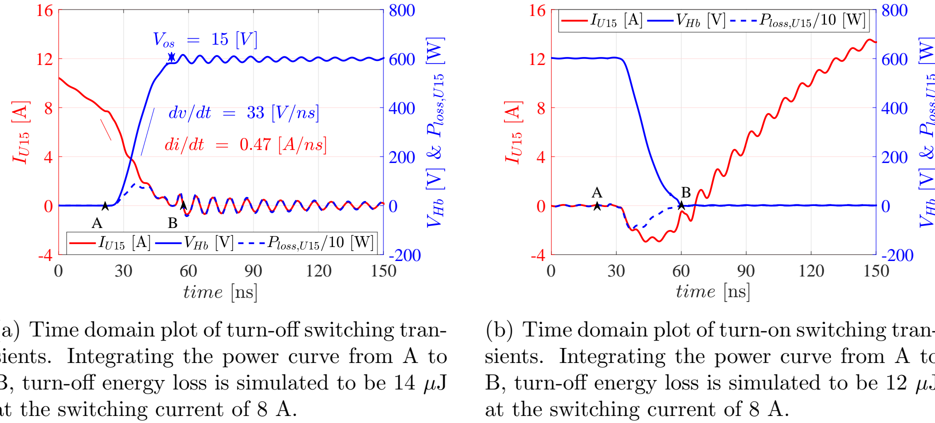
(a) Voltage and current of the switch U1.

(b) Voltage and current of the switch U15.

Figure D.5: (a) and (b) Switching voltages and currents of the complementary transistors (for instance, U1 and U15), illustrating an inductive mode of switching in a series-resonant inverter, where the switching frequency is slightly above the resonant frequency (given by RLC load).

D.3.1 Analysis of voltage overshoot when switched at 8 A

Fig. D.6 (a) and (b) show the turn-off and turn-on transients, respectively, at the switching current of 8 A and the DC-link voltage of 600 V. Apparently, the voltage overshoot is < 3% of the DC-link voltage. In a classical electrical loss measurement method, the turn-on loss is underestimated and the turn-off loss is overestimated by the amount of energy stored or discharged in the C_{oss}. Provided the upper and lower switches are identical, the losses associated with the charging and discharging of the C_{oss} are equal, the summation of the losses calculated by the classical approach will give the total actual power loss in the switching device.

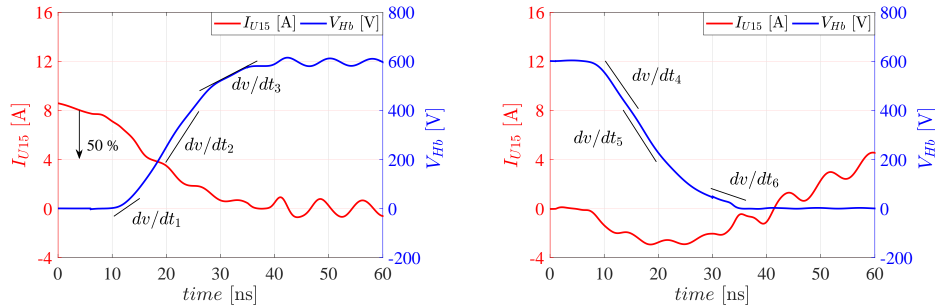


(a) Time domain plot of turn-off switching transients. Integrating the power curve from A to B, turn-off energy loss is simulated to be 14 μJ at the switching current of 8 A.

(b) Time domain plot of turn-on switching transients. Integrating the power curve from A to B, turn-off energy loss is simulated to be 12 μJ at the switching current of 8 A.

Figure D.6: (a) Turn-off switching transient when switched at 8 A, the voltage overshoot is < 3% of DC-link voltage. (b) Turn-on switching transients showing the negative current which is associated with the discharging of the MOSFET output capacitance.

In the zero voltage switching technique, switches have soft turn-on and diodes have soft turn-off, that is, there is no recovery current. The negative part of the current is, as mentioned earlier, thus the capacitor discharge current. Multiplying the voltage across the switch and the current through it, power loss in the switch is found. Integrating the power over a defined interval of time, as shown in Fig. D.6 (a) and (b), the energy loss is computed. Provided the loss during the turn-on is close to the loss during the turn-off, the inverter works close-to-lossless switching. For instance, in the simulation, turn-on energy loss was found to be 12 μJ and the turn-off energy loss to be 14 μJ. A zoomed-in view of Fig. D.6 (a) and (b) are shown in Fig. D.7 (a) and (b), respectively. Obviously, during the turn-off, C_{oss} is charged and during the turn-on, it is discharged. Examining closely, a drop of 50% in the initial switching current (8 A) entails close to zero turn-off loss.



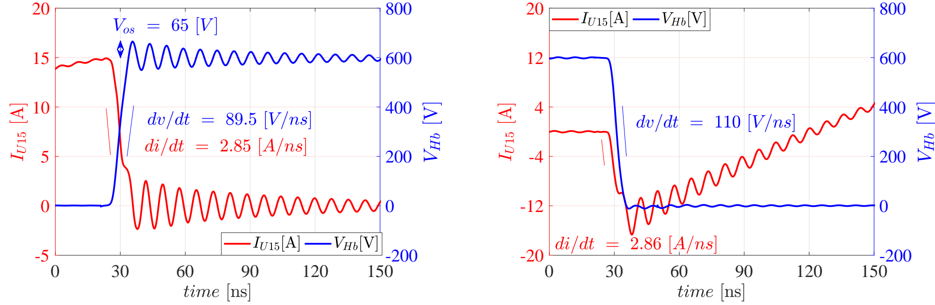
(a) Turn-off transients. Initial 50% drop in current after turn-off starts (from 8 A to 4 A) is fast, the di/dt of which is 0.47 A/ns, which is more visible with 30 ns/div of time scale in Fig. D.6 (a).

(b) Turn-on transients.

Figure D.7: (a) Turn-off transients showing different dv/dt at various points. Initially, C_{oss} is large at low voltage, so dv/dt_1 is low, then, dv/dt_2 is high, and finally, dv/dt_3 is low. (b) Turn-on transients also show similar characteristics as in (a). During the turn-off, C_{oss} is charged and during the turn-on, it is discharged.

D.3.2 Analysis of voltage overshoot when switched at 15 A

Fig. D.8 (a) and (b) show the turn-off and turn-on transients, respectively, at the switching current of 15 A (peak of sinusoidal load current) and the DC-link voltage of 600 V. Apparently, the voltage overshoot is $<$ 11% of the DC-link voltage. Note that di/dt is 2.85 A/ns and dv/dt is 89.5 V/ns, and the frequency of oscillations is 128 MHz. Of special note is that **as current increases, dv/dt and di/dt increase and as a consequence the oscillations are pronounced even though the loop inductance is 5 nH.** Following a similar approach as seen in Subsection D.3.1, turn-on and turn-off energy losses are computed and found to be 11 μJ and 14.6 μJ, respectively, leading to the actual switching loss of 3.6 μJ (14.6 - 11 = 3.6 μJ). It should be pointed out that this case is also close to zero switching loss as the specific energy loss is 0.24 μJ/A (= 3.6 μJ/15 A).



(a) Time domain plot of turn-off switching transients. Turn-off energy loss is simulated to be 14.6 μJ at the switching current of 15 A and the DC-link voltage of 600 V.

(b) Time domain plot of turn-on switching transients. Turn-on energy loss is simulated to be 11 μJ at the switching current of 15 A and the DC-link voltage of 600 V.

Figure D.8: (a) and (b) Turn-off and turn-on switching transients when switched at peak of sinusoidal load current (15 A), the voltage overshoot is $< 11\%$ of DC-link voltage. The total switching loss is 3.6 μJ (14.6 - 11 = 3.6 μJ) because the turn-off loss is positive and turn-on loss is negative.

D.3.3 Conclusion

As SiC MOSFETs can be switched with very high dv/dt; i.e., the current can be switched off instantly (close to ideal switch). In the simulation with ideal switch, the current does not appear in the negative direction during turn-on, but with real switch (with C_{oss}), it appears in the negative direction as well, which is the C_{oss} discharging current in the upper switch. If this power area in the negative side is maintained equal while turning off the lower transistor (meaning the area in the positive direction is just the energy that charges the capacitor), then close-to-lossless switching can be achieved.

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