



# RF430CL330H Dynamic NFC Interface Transponder

## 1 Device Overview

### 1.1 Features

- NFC Tag Type 4
- ISO14443B-Compliant 13.56-MHz RF Interface  
Supports up to 848 kbps
- SPI or I<sup>2</sup>C Interface to Write and Read NDEF Messages to Internal SRAM
- 3KB of SRAM for NDEF Messages
- Automatic Checking of NDEF Structure
- Interrupt Register and Output Pin to Indicate NDEF Read or Write Completion

### 1.2 Applications

- *Bluetooth*® Pairing
- Wi-Fi® Configuration
- Diagnostic Interface
- Sensor Interface

### 1.3 Description

The Texas Instruments Dynamic NFC Interface Transponder RF430CL330H is an NFC Tag Type 4 device that combines a wireless NFC interface and a wired SPI or I<sup>2</sup>C interface to connect the device to a host. The NDEF message in the SRAM can be written and read from the integrated SPI or I<sup>2</sup>C serial communication interface and can also be accessed and updated wirelessly through the integrated ISO14443B-compliant RF interface that supports up to 848 kbps.

This operation allows NFC connection handover for an alternative carrier like *Bluetooth*, *Bluetooth* Low Energy (BLE), and Wi-Fi as an easy and intuitive pairing process or authentication process with only a tap. As a general NFC interface, the RF430CL330H enables end equipments to communicate with the fast-growing infrastructure of NFC-enabled smart phones, tablets, and notebooks.

**Table 1-1. Device Information<sup>(1)</sup>**

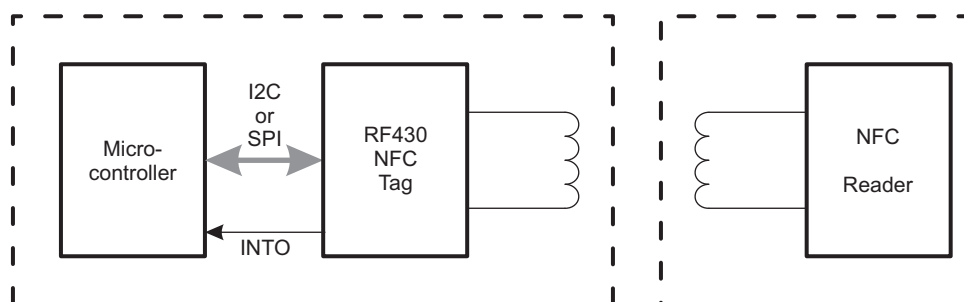
PART NUMBER	PACKAGE	BODY SIZE <sup>(2)</sup>
RF430CL330HPW	TSSOP (14)	5 mm x 4.4 mm
RF430CL330HRGT	VQFN (16)	3 mm x 3 mm

(1) For the most current part, package, and ordering information for all available devices, see the *Package Option Addendum* in [Section 7](#), or see the TI web site at [www.ti.com](http://www.ti.com).

(2) The sizes shown here are approximations. For the package dimensions with tolerances, see the *Mechanical Data* in [Section 7](#).

### 1.4 Typical Application Diagram

[Figure 1-1](#) shows a typical application diagram for the RF430CL330H device.



**Figure 1-1. Typical Application**



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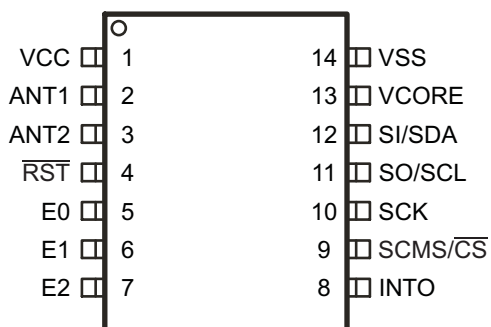
## 2 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (June 2014) to Revision C	Page
• Added RGT package to Device Information table	<a href="#">1</a>
• Added RGT package pinout	<a href="#">3</a>
• Added RGT package to <a href="#">Table 3-1</a>	<a href="#">4</a>
• Added <a href="#">Section 4.8</a>	<a href="#">8</a>

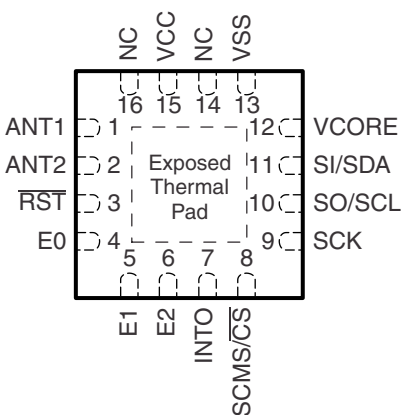
### 3 Terminal Configuration and Functions

Figure 3-1 shows the pin assignments for the PW package.



**Figure 3-1. 14-Pin PW Package (Top View)**

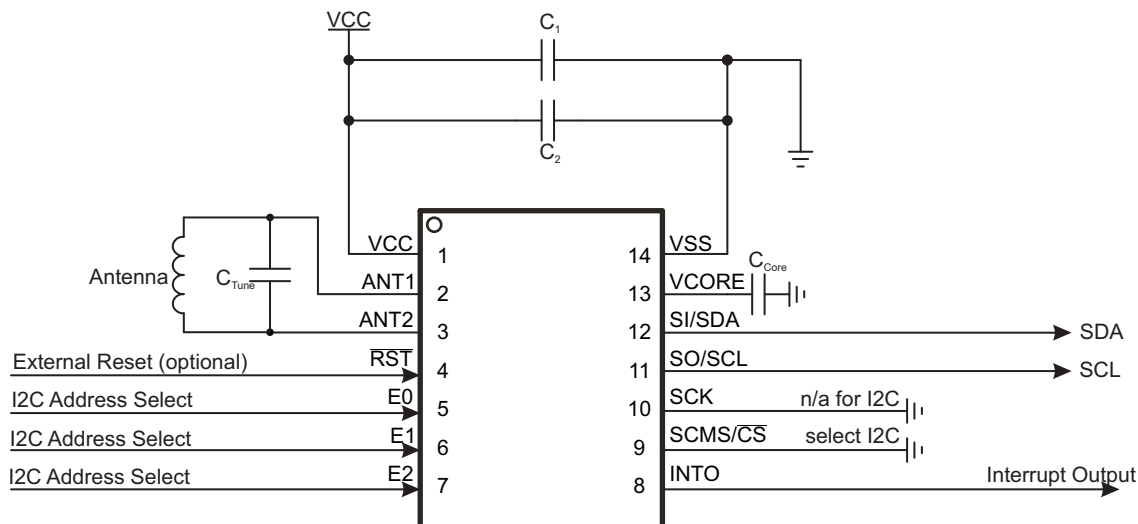
Figure 3-2 shows the pin assignments for the RGT package.



**Figure 3-2. 16-Pin RGT Package (Top View)**

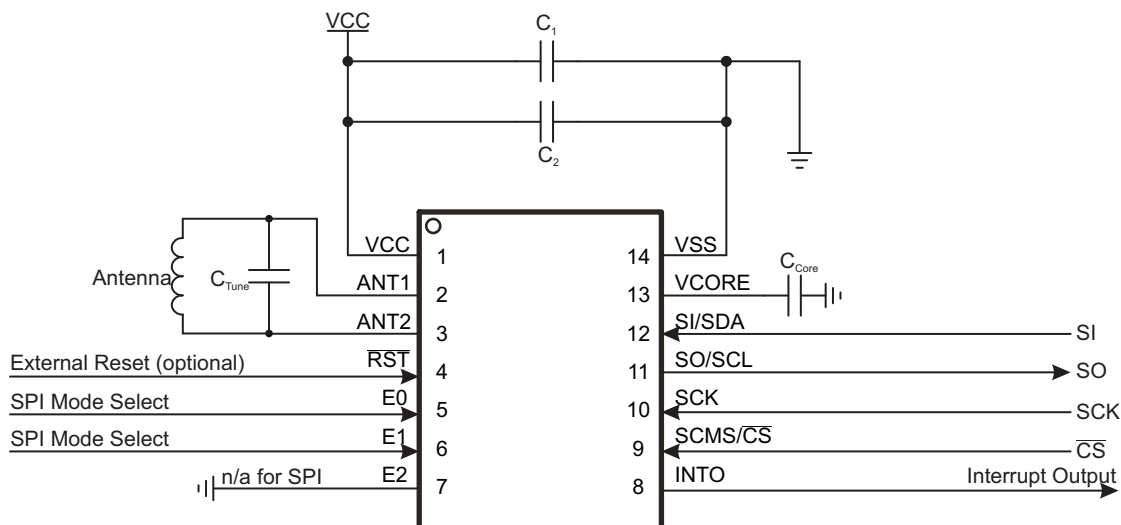
**Table 3-1. Terminal Functions**

TERMINAL			I/O	DESCRIPTION
NAME	NO.			
	PW	RGT		
VCC	1	15	PWR	3.3-V power supply
ANT1	2	1	RF	Antenna input 1
ANT2	3	2	RF	Antenna input 2
$\overline{\text{RST}}$	4	3	I	Reset input (active low)
E0 (TMS)	5	4	I	I <sup>2</sup> C address select 0 SPI mode select 0 (JTAG test mode select)
E1 (TDO)	6	5	I (O)	I <sup>2</sup> C address select 1 SPI mode select 1 (JTAG test data output)
E2 (TDI)	7	6	I	I <sup>2</sup> C address select 2 (JTAG test data in)
INTO (TCK)	8	7	O	Interrupt output (JTAG test clock)
SCMS/ $\overline{\text{CS}}$	9	8	I	Serial Communication Mode Select (during device initialization) Chip select (in SPI mode)
SCK	10	9	I	SPI clock input (SPI mode)
SO/SCL	11	10	I/O	SPI slave out (SPI mode) I <sup>2</sup> C clock (I <sup>2</sup> C mode)
SI/SDA	12	11	I/O	SPI slave in (SPI mode) I <sup>2</sup> C data (I <sup>2</sup> C mode)
VCORE	13	12	PWR	Regulated core supply voltage
VSS	14	13	PWR	Ground supply
NC	-	14, 16		Leave open, No connection



NOTE: For recommended capacitance values, see [Recommended Operating Conditions](#).

**Figure 3-3. Example Application Diagram (I²C Operation) (PW Package Shown)**



NOTE: For recommended capacitance values, see [Recommended Operating Conditions](#).

**Figure 3-4. Example Application Diagram (SPI Operation) (PW Package Shown)**

## 4 Specifications

### 4.1 Absolute Maximum Ratings<sup>(1) (2)</sup>

	MIN	MAX	UNIT
Voltage applied at V <sub>CC</sub> referenced to V <sub>SS</sub> (V <sub>AMR</sub> )	-0.3	4.1	V
Voltage applied at V <sub>ANT</sub> referenced to V <sub>SS</sub> (V <sub>AMR</sub> )	-0.3	4.1	V
Voltage applied to any pin (references to V <sub>SS</sub> )	-0.3	V <sub>CC</sub> + 0.3	V
Diode current at any device pin		±2	mA

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under [Recommended Operating Conditions](#) is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are referenced to V<sub>SS</sub>.

### 4.2 Handling Ratings

	MIN	MAX	UNIT
T <sub>stg</sub> Storage temperature range <sup>(1)</sup>	-40	125	°C

- (1) For soldering during board manufacturing, it is required to follow the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

### 4.3 Recommended Operating Conditions

Typical values are specified at V<sub>CC</sub> = 3.3 V and T<sub>A</sub> = 25°C (unless otherwise noted)

	MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply voltage during program execution no RF field present			V
	Supply voltage during program execution with RF field present			V
V <sub>SS</sub>	Supply voltage (GND reference)			V
T <sub>A</sub>	Operating free-air temperature			°C
C <sub>1</sub>	Decoupling capacitor on V <sub>CC</sub> <sup>(1)</sup>			μF
C <sub>2</sub>	Decoupling capacitor on V <sub>CC</sub> <sup>(1)</sup>			μF
C <sub>VCORE</sub>	Capacitor on V <sub>CORE</sub> <sup>(1)</sup>			μF

- (1) Low equivalent series resistance (ESR) capacitor

### 4.4 Recommended Operating Conditions, Resonant Circuit

	MIN	NOM	MAX	UNIT
f <sub>c</sub> Carrier frequency		13.56		MHz
V <sub>ANT_peak</sub> Antenna input voltage			3.6	V
Z Impedance of LC circuit	6.5		15.5	kΩ
L <sub>RES</sub> Coil inductance <sup>(1)</sup>		2.66		μH
C <sub>RES</sub> Total resonance capacitance <sup>(1)</sup> C <sub>RES</sub> = C <sub>IN</sub> + C <sub>Tune</sub>		51.8		pF
C <sub>Tune</sub> External resonance capacitance		$\frac{C_{RES}}{C_{IN(2)}}$		pF
QT Tank quality factor		30		

- (1) The coil inductance of the antenna L<sub>RES</sub> together with the external capacitance C<sub>Tune</sub> plus the device internal capacitance C<sub>IN</sub> is a resonant circuit. The resonant frequency of this LC circuit must be close to the carrier frequency f<sub>c</sub>:
- $$f_{RES} = 1 / [2\pi(L_{RES}C_{RES})^{1/2}] = 1 / [2\pi(L_{RES}(C_{IN} + C_{Tune}))^{1/2}] \approx f_c$$
- (2) For C<sub>IN</sub> refer to [Section 4.12](#).

## 4.5 Supply Currents

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP	MAX	UNIT
I <sub>CC</sub> (SPI)	SPI, f <sub>SCK,MAX</sub> , SO = Open, Writing into NDEF memory	3.3 V		250		μA
I <sub>CC</sub> (I2C)	I <sup>2</sup> C, 400 kHz, Writing into NDEF memory	3.3 V		250		μA
I <sub>CC</sub> (RF enabled)	RF enabled, no RF field present	3.3 V		40		μA
I <sub>CC</sub> (Inactive)	Standby enable = 0, RF disabled, no serial communication	3.3 V		15		μA
I <sub>CC</sub> (Standby)	Standby enable = 1, RF disabled, no serial communication	3.3 V		10	45	μA
ΔI <sub>CC</sub> (StrongRF)	Additional current consumption with strong RF field present	3.0 V to 3.6 V			160	μA
I <sub>CC</sub> (RF,lowVCC)	Current drawn from VCC < 3.0 V with RF field present (passive operation)	2.0 V to 3.0 V			0	μA

## 4.6 Digital Inputs

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP	MAX	UNIT
V <sub>IL</sub> Low-level input voltage					0.3× V <sub>CC</sub>	V
V <sub>IH</sub> High-level input voltage			0.7× V <sub>CC</sub>			V
V <sub>HYS</sub> Input hysteresis			0.1× V <sub>CC</sub>			V
I <sub>L</sub> High-impedance leakage current		3.3 V	-50		50	nA
R <sub>PU</sub> (RST) Integrated $\overline{\text{RST}}$ pullup resistor			20	35	50	kΩ
R <sub>PU</sub> (CS) Integrated SCMS/ $\overline{\text{CS}}$ pullup resistor (only active during initialization)			20	35	50	kΩ

## 4.7 Digital Outputs

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP	MAX	UNIT
V <sub>OL</sub> Output low voltage	I <sub>OL</sub> = 3 mA	3 V			0.4	V
		3.3 V			0.4	
		3.6 V			0.4	
V <sub>OH</sub> Output high voltage	I <sub>OH</sub> = -3 mA	3 V	2.6			V
		3.3 V	2.9			
		3.6 V	3.2			

## 4.8 Thermal Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		VALUE	UNIT
$\theta_{JA}$	Junction-to-ambient thermal resistance, still air <sup>(1)</sup>	TSSOP-14 (PW)	116.0
$\theta_{JC(TOP)}$	Junction-to-case (top) thermal resistance <sup>(2)</sup>		45.1
$\theta_{JB}$	Junction-to-board thermal resistance <sup>(3)</sup>		57.6
$\Psi_{JB}$	Junction-to-board thermal characterization parameter		57.0
$\Psi_{JT}$	Junction-to-top thermal characterization parameter		4.6
$\theta_{JA}$	Junction-to-ambient thermal resistance, still air <sup>(1)</sup>	VQFN-16 (RGT)	48.8
$\theta_{JC(TOP)}$	Junction-to-case (top) thermal resistance <sup>(2)</sup>		60.8
$\theta_{JB}$	Junction-to-board thermal resistance <sup>(3)</sup>		21.9
$\Psi_{JB}$	Junction-to-board thermal characterization parameter		21.9
$\Psi_{JT}$	Junction-to-top thermal characterization parameter		1.5
$\theta_{JC(BOT)}$	Junction-to-case (bottom) thermal resistance <sup>(4)</sup>		7.1

- (1) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, High-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- (2) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
- (3) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
- (4) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.



## 4.9 Serial Communication Protocol Timings

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
$t_{SP\text{Ivsl}2C}$	Time after power-up or reset until SCMS/ $\overline{CS}$ is sampled for SPI or I <sup>2</sup> C decision <sup>(1)</sup>	1		10	ms
$t_{\text{Ready}}$	Time after power-up or reset until device is ready to communicate using SPI or I <sup>2</sup> C <sup>(2)</sup>			20	ms

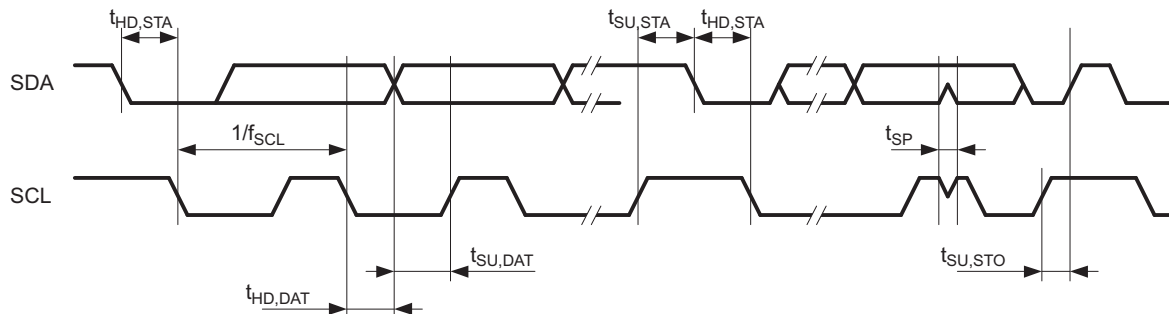
(1) The SCMS/ $\overline{CS}$  pin is sampled after  $t_{SP\text{Ivsl}2C}(\text{MIN})$  at the earliest and after  $t_{SP\text{Ivsl}2C}(\text{MAX})$  at the latest.

(2) The device is ready to communicate after  $t_{\text{Ready}}(\text{MAX})$  at the latest.

## 4.10 I<sup>2</sup>C Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 4-1](#))

PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP	MAX	UNIT
$f_{\text{SCL}}$	SCL clock frequency (with Master supporting clock stretching according to I <sup>2</sup> C standard, or when the device is not being addressed)		3.3 V	0		400	kHz
	SCL clock frequency (device being addressed by Master not supporting clock stretching)	write	3.3 V	0		120	kHz
		read	3.3 V	0		100	kHz
$t_{\text{HD,STA}}$	Hold time (repeated) START	$f_{\text{SCL}} \leq 100 \text{ kHz}$	3.3 V	4			$\mu\text{s}$
		$f_{\text{SCL}} > 100 \text{ kHz}$		0.6			
$t_{\text{SU,STA}}$	Setup time for a repeated START	$f_{\text{SCL}} \leq 100 \text{ kHz}$	3.3 V	4.7			$\mu\text{s}$
		$f_{\text{SCL}} > 100 \text{ kHz}$		0.6			
$t_{\text{HD,DAT}}$	Data hold time		3.3 V	0			ns
$t_{\text{SU,DAT}}$	Data setup time		3.3 V	250			ns
$t_{\text{SU,STO}}$	Setup time for STOP		3.3 V	4			$\mu\text{s}$
$t_{\text{SP}}$	Pulse duration of spikes suppressed by input filter		3.3 V	6.25		75	ns



**Figure 4-1. I<sup>2</sup>C Mode Timing**

## 4.11 SPI Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP	MAX	UNIT
f <sub>SCK</sub> SCK clock frequency	write	3.3 V	0		100	kHz
	read	3.3 V	0		110	kHz
t <sub>HIGH,CS</sub> $\overline{\text{CS}}$ high time		3.3 V	50			μs
t <sub>SU,CS</sub> $\overline{\text{CS}}$ setup time		3.3 V	25			μs
t <sub>HD,CS</sub> $\overline{\text{CS}}$ hold time		3.3 V	100			ns
t <sub>HIGH</sub> SCK high time		3.3 V	100			ns
t <sub>LOW</sub> SCK low time		3.3 V	100			ns
t <sub>SU,SI</sub> Data In (SI) setup time		3.3 V	50			ns
t <sub>HD,SI</sub> Data In (SI) hold time		3.3 V	50			ns
t <sub>VALID,SO</sub> Output (SO) valid		3.3 V	0		50	ns
t <sub>HOLD,SO</sub> Output (SO) hold time		3.3 V	0			ns

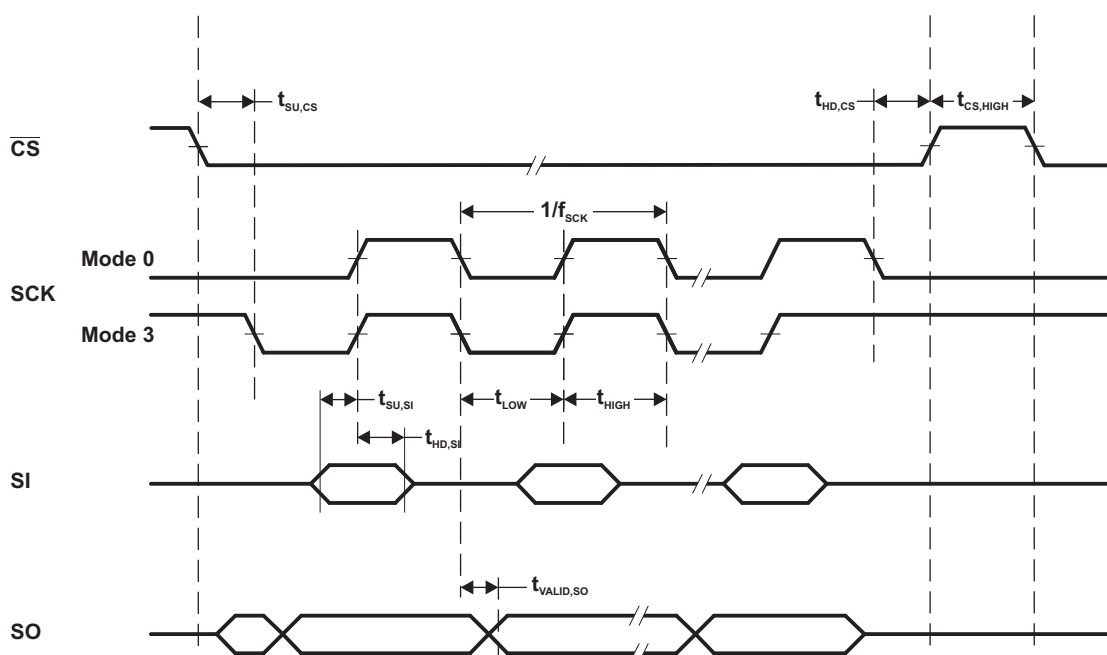


Figure 4-2. SPI Mode Timing

## 4.12 RF143B, Recommended Operating Conditions

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>DDH</sub>	Antenna rectified voltage	Peak voltage limited by antenna limiter	3.0	3.3	3.6	V
I <sub>DDH</sub>	Antenna load current	RMS, without limiter current			100	μA
C <sub>IN</sub>	Input capacitance	ANT1 to ANT2, 2 V RMS	31.5	35	38.5	pF

## 4.13 RF143B, ISO14443B ASK Demodulator

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
DR <sub>10</sub>	Input signal data rate 10% downlink modulation, 7% to 30% ASK, ISO1443B		106	848	kbps
m <sub>10</sub>	Modulation depth 10%, tested as defined in ISO10373	7		30	%

## 4.14 RF143B, ISO14443B-Compliant Load Modulator

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
f <sub>PICC</sub>	Uplink subcarrier modulation frequency	0.2		1	MHz
V <sub>A_MOD</sub>	Modulated antenna voltage, V <sub>A_unmod</sub> = 2.3 V	0.5			V
V <sub>SUB14</sub>	Uplink modulation subcarrier level, ISO14443B: H = 1.5 to 7.5 A/m	22/H <sup>0.5</sup>			mV

## 4.15 RF143B, Power Supply

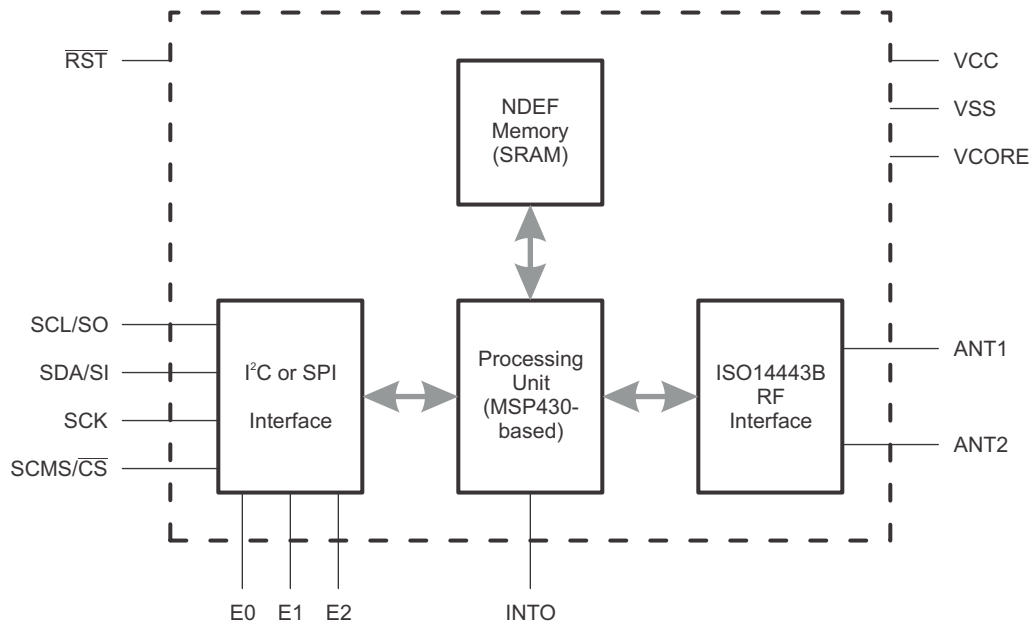
over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>LIM</sub>	Limiter clamping voltage	I <sub>LIM</sub> ≤ 70 mA RMS, f = 13.56 MHz	3.0		3.6	V <sub>pk</sub>
I <sub>LIM,MAX</sub>	Maximum limiter current				70	mA

## 5 Detailed Description

### 5.1 Functional Block Diagram

Figure 5-1 shows the functional block diagram.



**Figure 5-1. Functional Block Diagram**

### 5.2 Serial Communication Interface

A "dual-mode" serial communication interface supports either SPI or I<sup>2</sup>C communication. The serial interface allows writing and reading the internal NDEF memory as well as configuring the device operation.

### 5.3 SPI or I<sup>2</sup>C Mode Selection

The selection between I<sup>2</sup>C or SPI mode takes place during the power-up and initialization phase of the device based on the input level at pin SCMS/ $\overline{\text{CS}}$  (see Table 5-1).

**Table 5-1. SPI or I<sup>2</sup>C Mode Selection**

Input Level at SCMS/ $\overline{\text{CS}}$ During Initialization	Selected Serial Interface
0	I <sup>2</sup> C
1	SPI

During initialization, an integrated pullup resistor pulls SCMS/ $\overline{\text{CS}}$  high, which makes SPI the default interface. To enable I<sup>2</sup>C, this pin must be tied low externally. The pullup resistor is disabled after initialization to avoid any current through the resistor during normal operation. In SPI mode, the pin reverts to its  $\overline{\text{CS}}$  functionality after initialization.

## 5.4 Communication Protocol

The tag is programmed and controlled by writing data into and reading data from the address map shown in [Table 5-2](#) via the serial interface (SPI or I<sup>2</sup>C).

**Table 5-2. User Address Map**

Range	Address	Size	Description
Registers	0xFFFFE	2B	Control Register
	0xFFFFC	2B	Status Register
	0xFFFFA	2B	Interrupt Enable
	0xFFFF8	2B	Interrupt Flags
	0xFFFF6	2B	CRC Result (16-bit CCITT)
	0xFFFF4	2B	CRC Length
	0xFFFF2	2B	CRC Start Address
	0xFFFF0	2B	Communication Watchdog Control Register
	0xFFEE	2B	Version
	0xFFEC	2B	Reserved
	0xFFEA	2B	Reserved
	0xFFE8	2B	Reserved
	0xFFE6	2B	Reserved
	0xFFE4	2B	Reserved
	0xFFE2	2B	Reserved
	0xFFE0	2B	Reserved
Reserved	0x4000 to 0xFFDF		Reserved
	0x0C00 to 0x3FFF	13KB	Reserved (for example, future extension of NDEF Memory size)
NDEF	0x0000 to 0x0BFF	3KB	NDEF Memory

### NOTE

#### Crossing Range Boundaries

Crossing range boundaries causes writes to be ignored and reads to return undefined data.

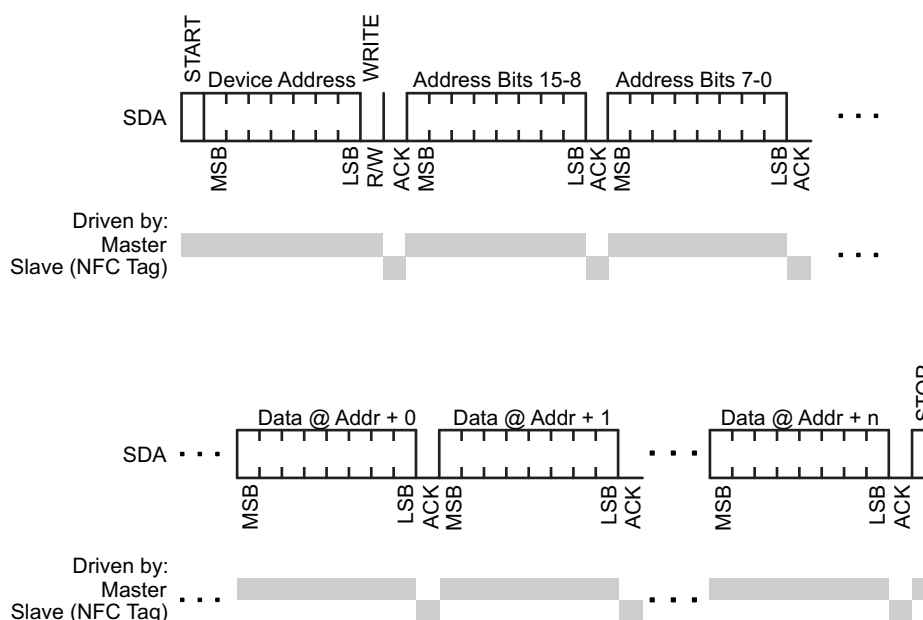
## 5.5 I<sup>2</sup>C Protocol

A command is always initiated by the master by addressing the device using the specified I<sup>2</sup>C device address. The device address is a 7-bit I<sup>2</sup>C address. The upper 4 bits are hard-coded, and the lower 3 bits are programmable by the input pins E0 through E2.

**Table 5-3. I<sup>2</sup>C Device Address**

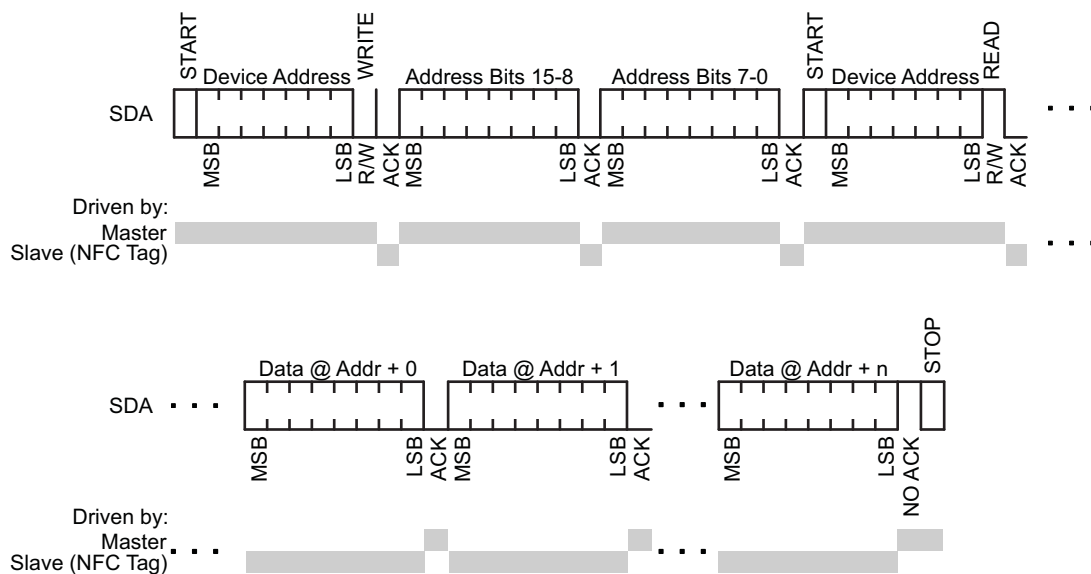
Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	0	1	E2	E1	E0
MSB						LSB

To write data, the device is addressed using the specified I<sup>2</sup>C device address with  $R/\overline{W} = 0$ , followed by the upper 8 bits of the first address to be written and the lower 8 bits of that address. Next (without a repeated start), the data to be written starting at the specified address is received. With each data byte received, the address is automatically incremented by 1. The write access is terminated by the STOP condition on the I<sup>2</sup>C bus.



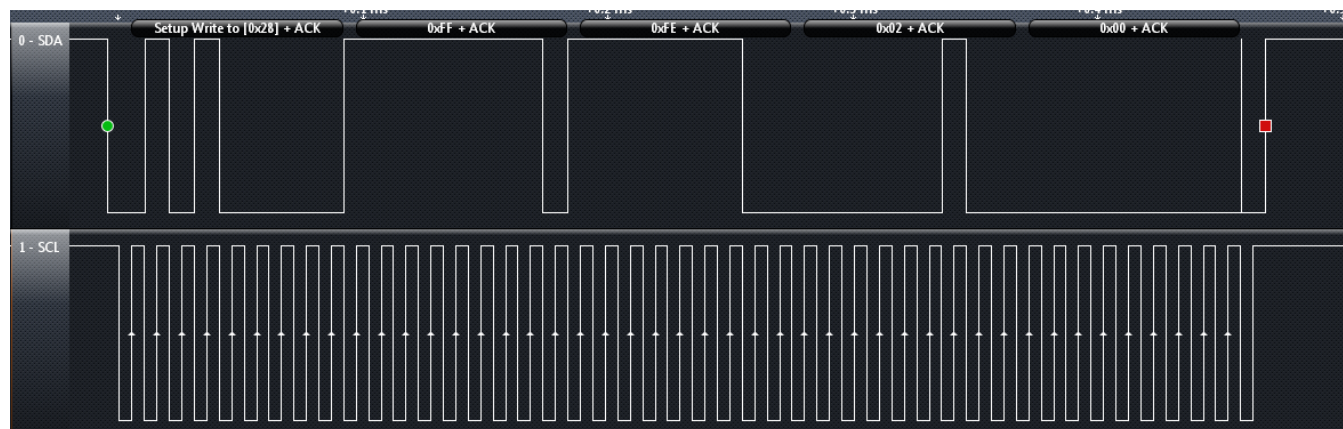
**Figure 5-2. I<sup>2</sup>C Write Access**

To read data, the device is addressed using the specified I<sup>2</sup>C device address with  $R/\overline{W} = 0$ , followed by the upper 8 bits of the first address to be read and then the lower 8 bits of that address. Next, a repeated start condition is expected with the I<sup>2</sup>C device address and  $R/\overline{W} = 1$ . The device then transmit data starting at the specified address until a non-acknowledgment and a STOP condition is received.

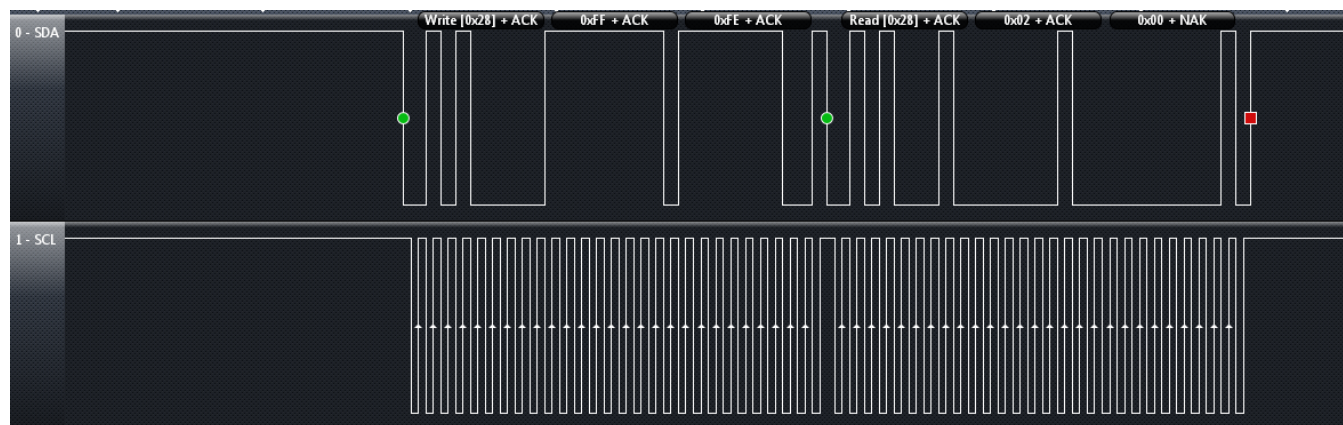


**Figure 5-3. I²C Read Access**

The following figures show examples of I²C accesses to the Control register at address 0xFFFE.



**Figure 5-4. I²C Access Example: Write of the Control Register at Address 0xFFFE With 0x00, 0x02 (RF Enable = 1)**



**Figure 5-5. I²C Access Example: Read of the Control Register at Address 0xFFFE, Responds With 0x00, 0x02 (RF Enable = 1)**

### 5.5.1 BIP-8 Communication Mode With I<sup>2</sup>C

The BIP-8 communication mode is enabled by setting the BIP-8 bit in the General Control register. All communication after setting this bit uses the following conventions with exactly 2 address bytes (16-bit address) and 2 data bytes (16-bit data).

**Table 5-4. Write Access**

<b>Master</b>	Address Bits 15 to 8	Address Bits 7 to 0	Data at Addr + 0	Data at Addr + 1	BIP-8
<b>Slave</b>	n/a	n/a	n/a	n/a	n/a

The Bit-Interleaved Parity (BIP-8) is calculated using 16-bit address and 16-bit data. If the received BIP-8 does not match with received data no write will be performed. (The BIP-8 calculation does not include the I<sup>2</sup>C device address).

**Table 5-5. Read Access**

<b>Master</b>	Address Bits 15 to 8	Address Bits 7 to 0	n/a	n/a	n/a
<b>Slave</b>	n/a	n/a	Data at Addr + 0	Data at Addr + 1	BIP-8

For read access, the Bit-Interleaved Parity (BIP-8) is calculated using the received 16-bit address and the 2 transmitted data bytes, and it is transmitted back to the master. The BIP-8 does not include the device address.



## 5.6 SPI Protocol

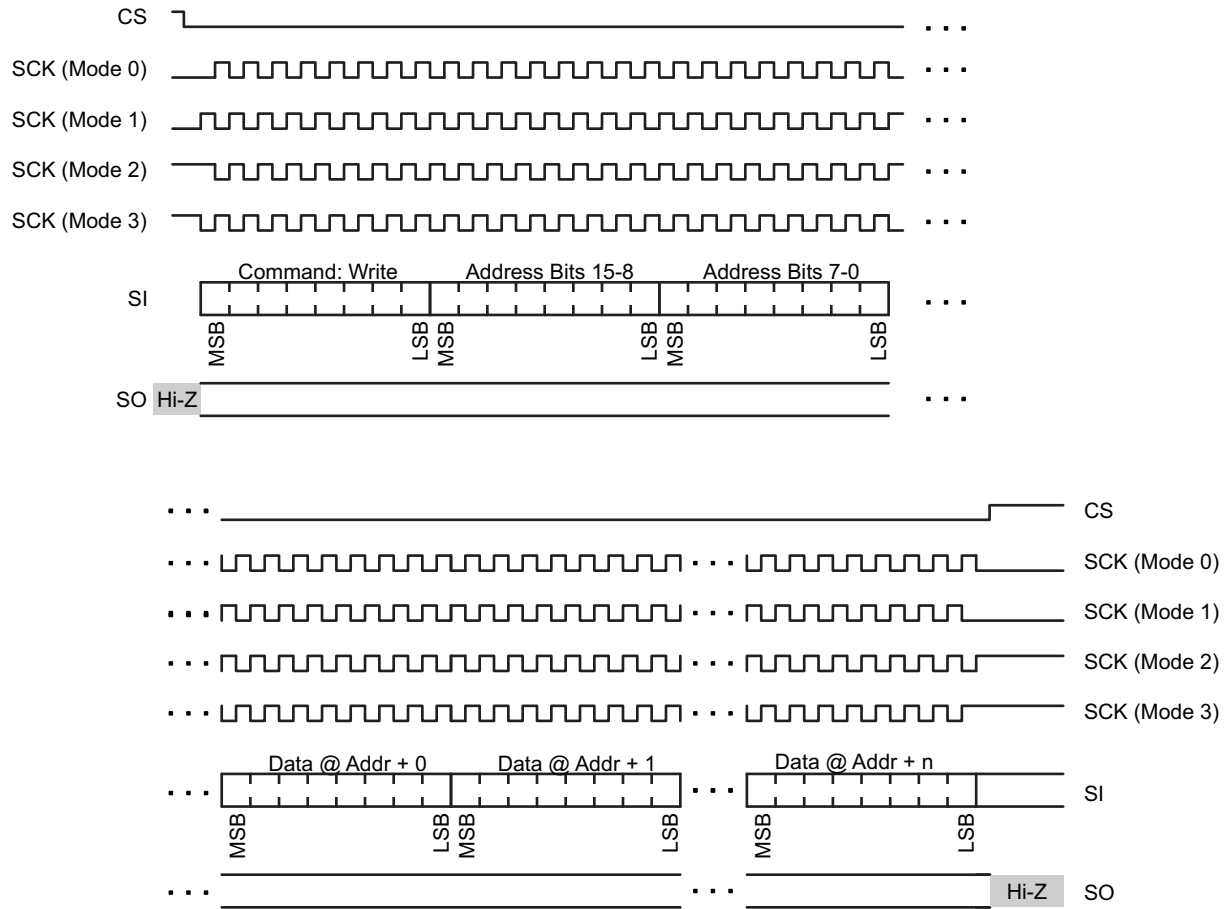
The SPI communication mode (SCK idle state and clock phase) is selected by tying E0 and E1 to VSS or VCC according to [Table 5-6](#).

**Table 5-6. SPI Mode Selection**

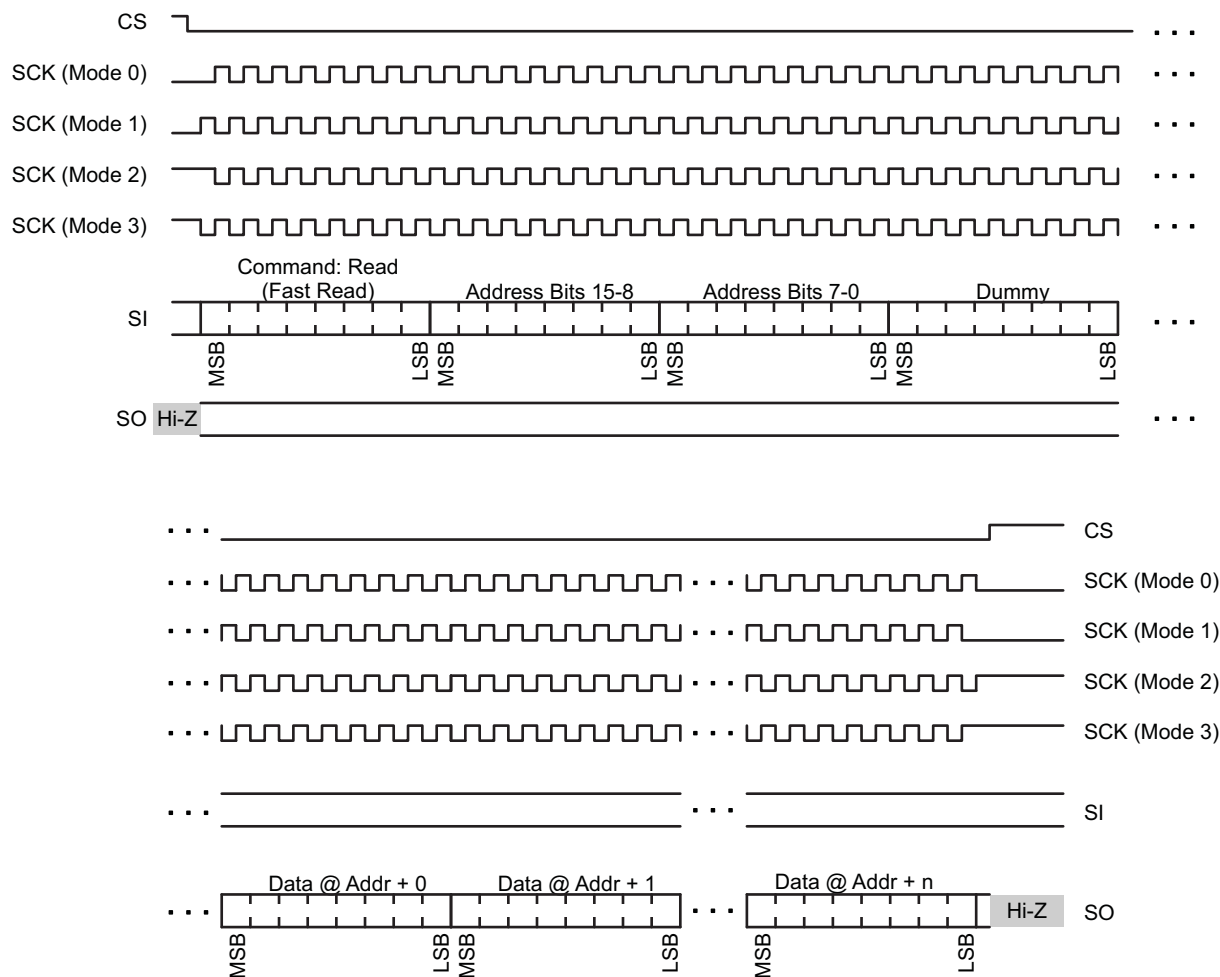
E1	E0	SPI Mode
0	0	<b>SPI Mode 0</b> with CPOL = 0 and CPHA = 0 SCK idle state: 0 SI capture starts on the first edge: SI data is captured on the rising edge, and SO data is propagated on the falling edge.
0	1	<b>SPI Mode 1</b> with CPOL = 0 and CPHA = 1 SCK idle state: 0 SI capture starts on the second edge: SI data is captured on the falling edge, and SO data is propagated on the rising edge.
1	0	<b>SPI Mode 2</b> with CPOL = 1 and CPHA = 0 SCK idle state: 1 SI capture starts on the first edge: SI data is captured on the falling edge, and SO data is propagated on the rising edge.
1	1	<b>SPI Mode 3</b> with CPOL = 1 and CPHA = 1 SCK idle state: 1 SI capture starts on the second edge: SI data is captured on the rising edge, and SO data is propagated on the falling edge.

An SPI communication is always initiated by the master by pulling the  $\overline{CS}$  pin low.

To write data into the device, this is followed by the master sending a write command (0x02) followed by the upper 8 bits of the first address to be written and then the lower 8 bits of that address. Next, the data to be written starting at the specified address is received. With each data byte received, the address is automatically incremented by 1. The write access is terminated by pulling the  $\overline{CS}$  pin high.

**Figure 5-6. SPI Write Access**

To read data from the device, pulling the  $\overline{CS}$  pin low is followed by the master sending a read command (0x03 or 0x0B) followed by the upper 8 bits of the first address to be read, the lower 8 bits of that address, and a dummy byte. The device responds with the data that is read starting at the specified address until the  $\overline{CS}$  pin is pulled high.



**Figure 5-7. SPI Read Access (Command: 0x03 or 0x0B)**

Commands other than write (0x02) and read (0x03 or 0x0B) are ignored. There is no difference in using the read command 0x03 or 0x0B.

Figure 5-8 and Figure 5-9 show examples of SPI accesses to the Control register at address 0xFFFE.



**Figure 5-8. SPI Access Example: Write of the Control Register at Address 0xFFFE With 0x00, 0x02 (RF Enable = 1)**



**Figure 5-9. SPI Access Example: Read of the Control Register at Address 0xFFFFE, Responds With 0x00, 0x02 (RF Enable = 1)**

### 5.6.1 BIP-8 Communication Mode With SPI

The BIP-8 communication mode is enabled by setting the BIP-8 bit in the General Control register. All communication after setting this bit uses the following conventions with exactly 2 address bytes (16-bit address) and 2 data bytes (16-bit data).

**Table 5-7. Write Access**

SI	Command: Write	Address Bits 15 to 8	Address Bits 7 to 0	Data at Addr + 0	Data at Addr + 1	BIP-8
SO	n/a	n/a	n/a	n/a	n/a	n/a

The Bit-Interleaved Parity (BIP-8) is calculated using 16-bit address and 16-bit data. If the received BIP-8 does not match with received data no write will be performed. (The BIP-8 calculation does not include the write-command byte.)

**Table 5-8. Read Access**

SI	Command: Read	Address Bits 15 to 8	Address Bits 7 to 0	Dummy Byte	n/a	n/a	n/a
SO	n/a	n/a	n/a	n/a	Data at Addr + 0	Data at Addr + 1	BIP-8

For read access the Bit-Interleaved Parity (BIP-8) is calculated using the received 16-bit address, the received dummy byte and the 2 transmitted data bytes and transmitted back to the master. It does not include the read-command byte.

## 5.7 Registers

### NOTE

#### Endianness

All 16-bit registers are little-endian: the least significant byte with bits 7-0 is at the lowest address (and this address is always even). The most significant byte with bits 15-8 is at the highest address (always odd).

### 5.7.1 General Control Register

**Table 5-9. General Control Register**

Addr:	15	14	13	12	11	10	9	8
0xFFFF	Reserved							
Addr:	7	6	5	4	3	2	1	0
0xFFFE	Reserved	Standby Enable	BIP-8	INTO Drive	INTO High	Enable INT	Enable RF	SW-Reset

**Table 5-10. General Control Register Description**

Bit	Field	Type	Reset	Description
0	SW-Reset	W	0	0b = Always reads 0. 1b = Resets the device to default settings and clears memory. The serial communication is restored after $t_{Ready}$ , and the register settings and NDEF memory must be restored afterward.
1	Enable RF	R/W	0	Global enable of RF interface. The RF interface should be disabled when writing to the NDEF memory. Enabling the RF interface triggers a basic check of the NDEF structure. If this check fails, the RF interface remains disabled and the NDEF Error interrupt flag is set. When the RF interface is enabled, writes using the serial interface (except to disable the RF interface) are discouraged to avoid any interference with RF communication. 0b = RF interface disabled 1b = RF interface enabled
2	Enable INT	R/W	0	Global Interrupt Output Enable 0b = Interrupt output disabled. The INTO pin is Hi-Z. 1b = Interrupt output enabled. The INTO pin signals any enabled interrupt according to the INTO High and INTO Drive bits.
3	INTO High	R/W	0	Interrupt Output pin INTO Configuration 0b = Interrupts are signaled with an active low 1b = Interrupts are signaled with an active high
4	INTO Drive	R/W	0	Interrupt Output pin INTO Configuration 0b = Pin is Hi-Z if there is no pending interrupt. Application provides an external pullup resistor if bit 3 (INTO Active High) = 0. Application provides an external pulldown resistor if bit 3 (INTO Active High) = 1. 1b = Pin is actively driven high or low if there is no pending interrupt. It is driven high if bit 3 (INTO Active High) = 0. It is driven low if bit 3 (INTO Active High) = 1.

**Table 5-10. General Control Register Description (continued)**

Bit	Field	Type	Reset	Description
5	BIP-8	R/W	0	<p>Enables BIP-8 communication mode (bit interleaved parity).</p> <p>If BIP-8 is enabled, a separate running tally is kept of the parity (that is, the number of ones that occur) for every bit position in the bytes included in the BIP-8 calculation. The corresponding bit position of the BIP-8 byte is set to 1 if the parity is currently odd and is set to 0 if the parity is even – resulting in an overall even parity for each bit position including the BIP-8 byte.</p> <p>All communication when this bit is set must follow the conventions defined in the BIP-8 communication mode sections for <a href="#">I2C</a> and <a href="#">SPI</a>.</p> <p>0b = BIP-8 communication mode disabled 1b = BIP-8 communication mode enabled</p>
6	Standby Enable	R/W	0	<p>Enables a low-power standby mode. The standby mode is entered if the RF interface is disabled, the communication watchdog is disabled, and no serial communication is ongoing.</p> <p>0b = Standby mode disabled 1b = Standby mode enabled</p>
7	Reserved	R/W	0	
8-15	Reserved	R	0	

**5.7.2 Status Register****Table 5-11. Status Register**

Addr:	15	14	13	12	11	10	9	8
0xFFFF	Reserved							
Addr:	7	6	5	4	3	2	1	0
0xFFFC	Reserved					RF Busy	CRC Active	NDEF Ready

**Table 5-12. Status Register Description**

Bit	Field	Type	Reset	Description
0	Ready	R	0	<p>0b = Device not ready to receive updates to the NDEF memory from the serial interface.</p> <p>1b = Device ready. NDEF memory can be written by the serial interface.</p>
1	CRC Active	R	0	<p>0b = No CRC calculation ongoing 1b = CRC calculation ongoing</p>
2	RF Busy	R	0	<p>0b = No RF communication ongoing 1b = RF communication ongoing</p>
3-15	Reserved	R	0	



### 5.7.3 Interrupt Registers

The interrupt enable register (see [Table 5-13](#) and [Table 5-14](#)) determines which interrupt events are signaled on the external output pin INTO. Setting any bit high in this register allows the corresponding event to trigger the interrupt signal. See [Table 5-17](#) for a description of each interrupt.

All enabled interrupt signals are ORed together, and the result is signaled on the output pin INTO.

**Table 5-13. Interrupt Enable Register**

<b>Addr:</b>	15	14	13	12	11	10	9	8
<b>0xFFFB</b>	Reserved							
<b>Addr:</b>	7	6	5	4	3	2	1	0
<b>0xFFFA</b>	Generic Error	Reserved	NDEF Error	BIP-8 Error Detected	CRC Calculation Completed	End of Write	End of Read	Reserved

**Table 5-14. Interrupt Enable Register Description**

Bit	Field	Type	Reset	Description
0-15	Interrupt Enables	R/W	0	Enable for the corresponding IRQ. All enabled interrupt signals are ORed together, and the result is signaled on the output pin INTO.  0b = IRQ disabled 1b = IRQ enabled

The interrupt flag register (see [Table 5-15](#) and [Table 5-16](#)) is used to report the status of any interrupts that are pending. Setting any bit high in this register acknowledges and clears the interrupt associated with the respective bit. See [Table 5-17](#) for a description of each interrupt.

**Table 5-15. Interrupt Flag Register**

<b>Addr:</b>	15	14	13	12	11	10	9	8
<b>0xFFF9</b>	Reserved							
<b>Addr:</b>	7	6	5	4	3	2	1	0
<b>0xFFF8</b>	Generic Error	Reserved	NDEF Error	BIP-8 Error Detected	CRC Calculation Completed	End of Write	End of Read	Reserved

**Table 5-16. Interrupt Flag Register Description**

Bit	Field	Type	Reset	Description
0-15	Interrupt Flags	R/W	0	Flag pending IRQ.  Read Access: 0b = No pending IRQ. 1b = Pending IRQ.  Write Access: 0b = No change. 1b = Clear pending IRQ flag.

**Table 5-17. Interrupts**

Bit	Field	Description
0	Reserved	
1	End of Read	This IRQ occurs when the RF field is turned off by the reader after the reader has performed a read of the NDEF message.
2	End of Write	This IRQ occurs when the RF field is turned off by the reader after the reader has performed a write into the NDEF message.
3	CRC Calculation Completed	This IRQ occurs when a CRC calculation that is triggered by writing into the CRC registers is completed and the result can be read from the CRC result register (see <a href="#">Section 5.7.4</a> ).
4	BIP-8 Error Detected	This IRQ occurs when a BIP-8 error is detected (only if the BIP-8 communication mode is enabled).
5	NDEF Error	This IRQ occurs if an error is detected in the NDEF structure after an attempt to enable the RF interface.
6	Reserved	
7	Generic Error	This IRQ occurs for any error that makes the device unreliable or non-operational.
8-15	Reserved	

### 5.7.4 CRC Registers

Writing the CRC address and the CRC length registers initiates a 16-bit CRC calculation of the specified address range. The length is always assumed to be even (16-bit aligned). Writing the length register starts the CRC calculation.

During the CRC calculation, the CRC active bit is set (=1). When the calculation is complete, the "CRC completion" interrupt flag is set and the result of the CRC calculation can be read from the CRC result register. It is recommended to perform a CRC calculation only when the RF interface is disabled (RF Enable = 0).

**Table 5-18. CRC Result Register**

<b>Addr:</b>	15	14	13	12	11	10	9	8
<b>0xFFF7</b>	CRC CCITT Result (high byte)							
<b>Addr:</b>	7	6	5	4	3	2	1	0
<b>0xFFF6</b>	CRC CCITT Result (low byte)							

**Table 5-19. CRC Result Register Description**

Bit	Field	Type	Reset	Description
0-15	CRC-CCITT Result	R	0	CRC-CCITT Result

**Table 5-20. CRC Length Register**

<b>Addr:</b>	15	14	13	12	11	10	9	8
<b>0xFFF5</b>	CRC Length (high byte)							
<b>Addr:</b>	7	6	5	4	3	2	1	0
<b>0xFFF4</b>	CRC Length (low byte)							

**Table 5-21. CRC Length Register Description**

Bit	Field	Type	Reset	Description
0-15	CRC Length	RW	0	CRC Length - always assumed to be even (Bit 0 = 0). Writing into high byte starts CRC calculation.

**Table 5-22. CRC Start Address Register**

<b>Addr:</b>	15	14	13	12	11	10	9	8
<b>0xFFF3</b>	CRC Start Address (high byte)							
<b>Addr:</b>	7	6	5	4	3	2	1	0
<b>0xFFF2</b>	CRC Start Address (low byte)							

**Table 5-23. CRC Start Address Register Description**

Bit	Field	Type	Reset	Description
0-15	CRC Start Address	RW	0	CRC Start Address. Defines start address within NDEF memory. This address is always assumed to be even (bit 0 = 0).

The CRC is calculated based on the CCITT polynomial initialized with 0xFFFF.

CCITT polynomial:  $x^{16} + x^{12} + x^5 + 1$

### 5.7.5 Communication Watchdog Register

When the communication watchdog is enabled, it expects a write or read access within a specified period; otherwise, the watchdog resets the device. If the BIP-8 communication mode is enabled, the transfer must be valid to be accepted as a watchdog reset.

**Table 5-24. Communication Watchdog Register**

<b>Addr:</b>	15	14	13	12	11	10	9	8
<b>0xFFFF1</b>	Reserved							
<b>Addr:</b>	7	6	5	4	3	2	1	0
<b>0xFFFF0</b>	Reserved				Timeout Period Selection			Enable

**Table 5-25. Communication Watchdog Register Description**

Bit	Field	Type	Reset	Description
0	Enable	R/W	0	0b = Communication Watchdog disabled 1b = Communication Watchdog enabled
1	Timeout Period Selection	R/W	0	000b = 2 s $\pm$ 30% <sup>(1)</sup> 001b = 32 s $\pm$ 30% <sup>(1)</sup> 010b = 8.5 min $\pm$ 30% <sup>(1)</sup> 011b to 111b = Reserved
4-15	Reserved	R	0	

(1) This value is based on use of the integrated low-frequency oscillator with a frequency of 256 kHz  $\pm$  30%.

### 5.7.6 Version Registers

Provides version information about the implemented ROM code.

**Table 5-26. Version Register**

<b>Addr:</b>	15	14	13	12	11	10	9	8
<b>0xFFEF</b>	Software Version							
<b>Addr:</b>	7	6	5	4	3	2	1	0
<b>0xFFEE</b>	Software Identification							

**Table 5-27. Version Register Description**

Bit	Field	Type	Reset	Description
0-7	Software Identification	R		0x01: RF430CL330H Firmware
8-15	Software Version	R		Software version

## 5.8 NFC Type-4 Tag Functionality

This device is an ISO14443B-compliant transponder that operates according to the NFC Forum Tag Type-4 specification and supports the NFC Forum NDEF (NFC Data Exchange Format) requirements. Through the RF interface, the user can read and update the contents in the NDEF memory. The contents in the NDEF memory (stored in SRAM) are stored as long as power is maintained.

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### NOTE

This device does not have nonvolatile memory; therefore, the information stored in the NDEF memory is lost when power is removed.

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This device does not support the peer-to-peer or reader/writer modes in the ISO18092/NFC Forum specification. All RF communication between an NFC forum device and this device is in the passive tag mode. The device responds by load modulation and is not considered an intentional radiator.

This device is intended to be used in applications where the primary reader/writer is for example an NFC-enabled cell phone. The device enables data transfer to and from an NFC phone by RF to the host application that is enabled with the dual interface device. In this case, the host application can be considered the destination device, and the cell phone or other type of mobile device is treated as the end-point device.

This device supports ISO14443-3, ISO14443-4, and NFC Forum commands as described in the following sections. A high-level overview of the ISO14443B and NFC commands and responses are shown in [Figure 5-10](#).

106-kbps, 212-kbps, 424-kbps, and 848-kbps data rates are supported.

The device always answers ATTRIB commands from the PCD that request higher data rates. Note, this is not NFC-compliant, because for NFC-B the maximum data rate specified is 106 kbps. It is assumed that an NFC-compliant PCD would not request higher data rates thus no interoperability issues are expected.

Even though all data rates up to 848 kbps are supported, the device by default reports only the capability to support 106 kbps to the PCD. To change this behavior, use the sequence described in [Section 5.8.3](#).

The ISO14443B command and response structure is detailed in ISO14443-3, ISO14443-4, and NFC Forum-TS-Digital Protocol. The applicable ISO7816-4 commands are detailed in NFC Forum-TS-Type-4-Tag\_2.0.

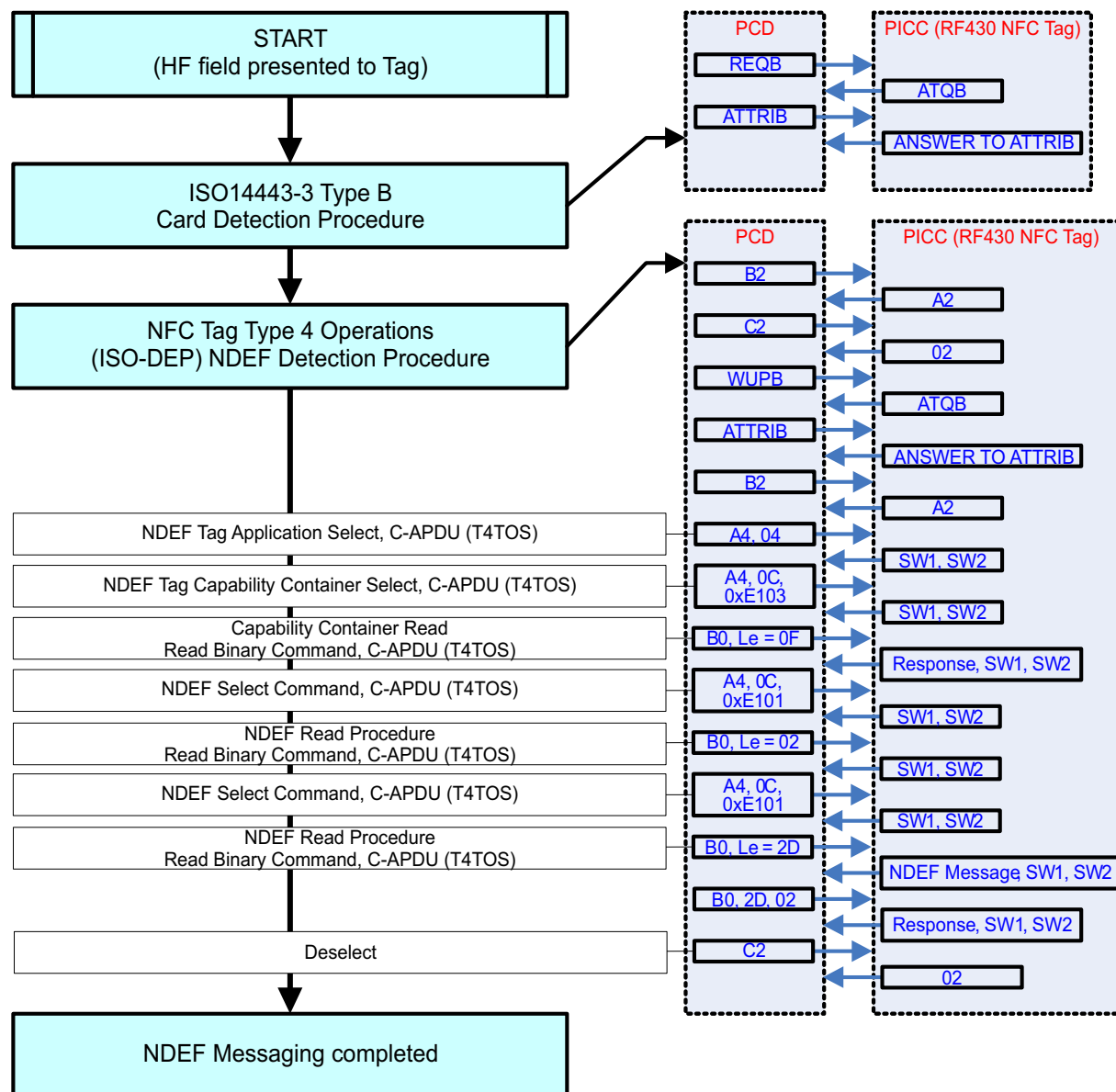


Figure 5-10. Command and Response Exchange Flow

### **5.8.1 ISO14443-3 Commands**

These commands use the character, frame format, and timing that are described in ISO14443-3, clause 7.1. The following commands are used to manage communication:

#### **REQB and WUPB**

The REQB and WUPB Commands sent by the PCD are used to probe the field for PICCs of Type B. In addition, WUPB is used to wake up PICCs that are in the HALT state. The number of slots N is included in the command as a parameter to optimize the anticollision algorithm for a given application.

#### **Slot-MARKER**

After a REQB or WUPB Command, the PCD may send up to (N-1) Slot-MARKER Commands to define the start of each timeslot. Slot-MARKER Commands can be sent after the end of an ATQB message received by the PCD to mark the start of the next slot or earlier if no ATQB is received (no need to wait until the end of a slot, if this slot is known to be empty).

#### **ATTRIB**

The ATTRIB Command sent by the PCD includes information required to select a single PICC. A PICC receiving an ATTRIB Command with its identifier becomes selected and assigned to a dedicated channel. After being selected, this PICC only responds to commands defined in ISO/IEC 14443-4 that include its unique CID.

#### **HLTB**

The HLTB Command is used to set a PICC in HALT state and stop responding to a REQB. After answering to this command, the PICC ignores any commands except the WUPB.

### **5.8.2 NFC Tag Type 4 Commands**

#### **Select**

Selection of applications or files

#### **ReadBinary**

Read data from file

#### **UpdateBinary**

Update (erase and write) data to file

### 5.8.3 Data Rate Settings

106-kbps, 212-kbps, 424-kbps, and 848-kbps data rates are supported by the device.

The device always answers ATTRIB commands from the PCD that request higher data rates. Note, this is not NFC-compliant, because for NFC-B the maximum data rate specified is 106 kbps. It is assumed that an NFC-compliant PCD would not request higher data rates thus no interoperability issues are expected.

Even though all data rates up to 848 kbps are supported, the device by default reports only the capability to support 106 kbps to the PCD.

To change this behavior, follow these steps using the selected serial interface (I<sup>2</sup>C or SPI):

1. Read the version register.
2. Use the version register content to select one of the following sequences:
  - If "Software Identification" = 01h and "Software Version" = 01h, follow the sequence in [Table 5-28](#).
  - If "Software Identification" = 01h and "Software Version" = 02h, follow the sequence in [Table 5-29](#).
3. If you do not want to support all data rates up to 847 kbps, then change the Data Rate Capability byte (Data 0 of Step 3. Write Access) according to [Table 5-30](#).
4. Perform the steps in the following tables.

**Table 5-28. Data Rate Setting Sequence (Version = 0101h)**

Access Type	Addr Bits 15 to 8	Addr Bits 7 to 0	Data 0	Data 1
1. Write Access	0xFF	0xE0	0x4E	0x00
2. Write Access	0xFF	0xFE	0x80	0x00
3. Write Access	0x2A	0xA4	0xC4 <sup>(1)</sup>	0x00
4. Write Access	0x28	0x14	0x00	0x00
5. Write Access	0xFF	0xE0	0x00	0x00

(1) Data Rate Capability according to [Table 5-30](#). 0xC4: all data rates up to 847 kbps are supported.

**Table 5-29. Data Rate Setting Sequence (Version = 0201h)**

Access Type	Addr Bits 15 to 8	Addr Bits 7 to 0	Data 0	Data 1
1. Write Access	0xFF	0xE0	0x4E	0x00
2. Write Access	0xFF	0xFE	0x80	0x00
3. Write Access	0x2A	0x7C	0xC4 <sup>(1)</sup>	0x00
4. Write Access	0x28	0x14	0x00	0x00
5. Write Access	0xFF	0xE0	0x00	0x00

(1) Data Rate Capability according to [Table 5-30](#). 0xC4: all data rates up to 847 kbps are supported.

**Table 5-30. Data Rate Capability**

Data Rate Capability Byte								Description
b7	b6	b5	b4	b3	b2	b1	b0	
0	0	0	0	0	0	0	0	PICC supports only 106-kbps in both directions (default).
1	x	x	x	0	x	x	x	Same data rate from PCD to PICC and from PICC to PCD compulsory
x	x	x	1	0	x	x	x	PICC to PCD, data rate supported is 212 kbps
x	x	1	x	0	x	x	x	PICC to PCD, data rate supported is 424 kbps
x	1	x	x	0	x	x	x	PICC to PCD, data rate supported is 847 kbps
x	x	x	x	0	x	x	1	PCD to PICC, data rate supported is 212 kbps
x	x	x	x	0	x	1	x	PCD to PICC, data rate supported is 424 kbps
x	x	x	x	0	1	x	x	PCD to PICC, data rate supported is 847 kbps



## 5.9 NDEF Memory

This device implements 3KB of SRAM memory that must be written with the NDEF Application data.

[Table 5-31](#) shows the mandatory structure. The data can be accessed through the RF interface only after the NDEF memory is correctly initialized through the serial interface (I<sup>2</sup>C or SPI).

While writing into the NDEF memory, the RF interface must be disabled by clearing the Enable RF bit in the General Control register. After the NDEF memory is properly initialized, the RF interface can be enabled by setting the Enable RF bit in the General Control register to 1. When the RF interface is enabled, the basic NDEF structure is checked for correctness. If an error in the structure is detected, the NDEF Error IRQ is triggered, and the RF interface remains disabled (the Enable RF bit in the General Control register is cleared to 0).

If the NDEF application data must be modified through the serial interface after the RF interface is enabled, it is recommended to read the RF Busy bit in the Status register. If the RF interface is busy, defer disabling the RF interface until the RF transaction is completed (indicated by RF Busy bit = 0).

[Figure 5-11](#) shows the recommended flow how to control the access to the NDEF memory.

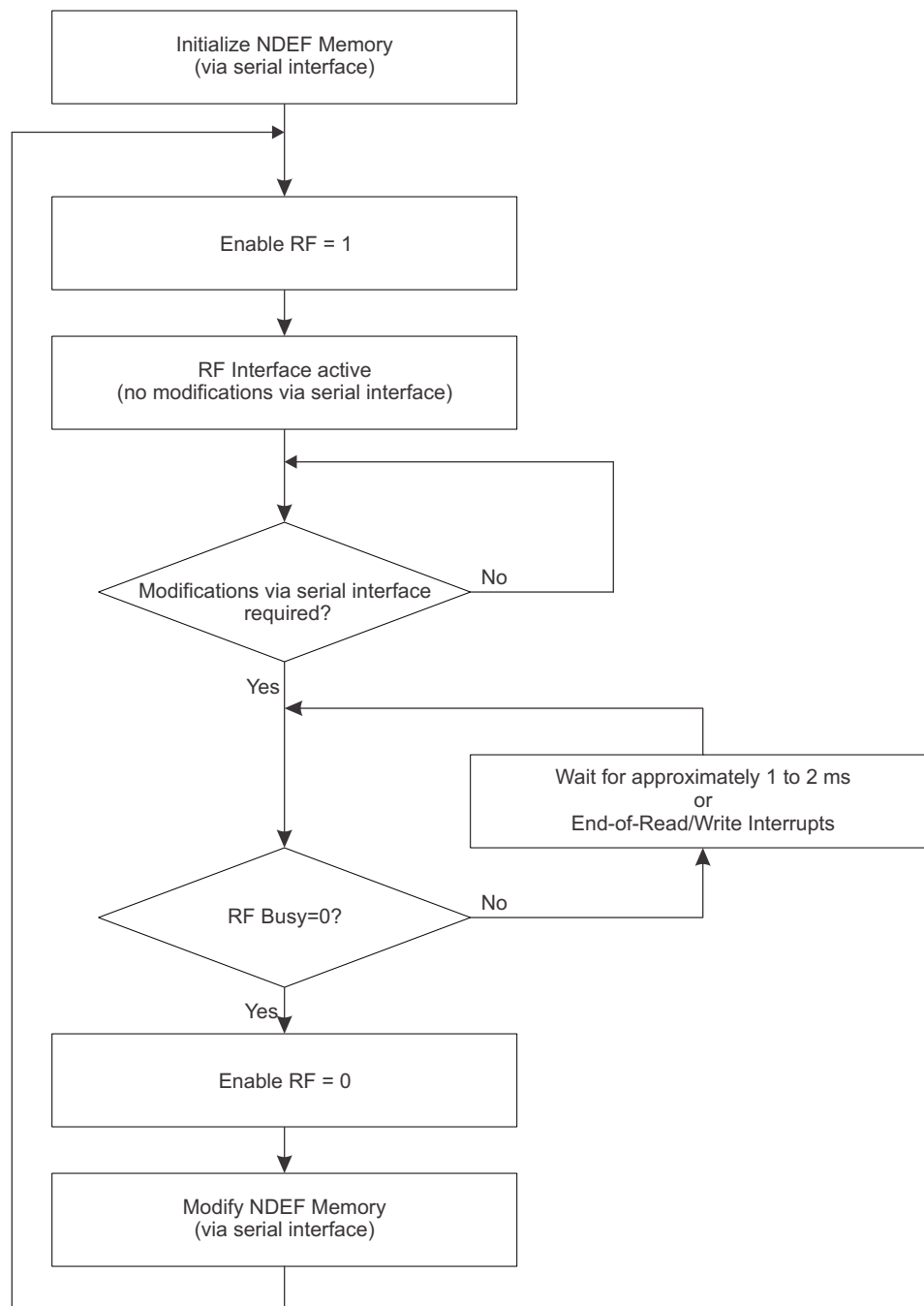
The address range for the NDEF memory is 0x0000 to 0x0BFF.

**Table 5-31. NDEF Application Data (Mandatory)**

NDEF Application  Selectable by Name = D2_7600_0085_0101h	Capability Container  Selectable by File ID = E103h	2B - CCLen			
		1B - Mapping version			
		2B - MLe = 000F9h			
		2B - MLc = 000F6h			
		NDEF File Ctrl TLV	1B - Tag = 04h		The NDEF file control TLV is mandatory
			1B - Len = 06h		
	6B - Val		2B - File Identifier		
			2B - Max file size		
		1B - Read access			
		1B - Write access			
NDEF File  Selectable by File ID = xxyyh	2B - Len			Mandatory NDEF file	
	xB - Binary NDEF file content				
	yB - Unused if Len < Max file size in File Ctrl TLV				

**Table 5-32. NDEF Application Data (Includes Proprietary Sections)**

NDEF Application  Selectable by Name = D2_7600_0085_0101h	Capability Container  Selectable by File ID = E103h	2B - CCLen			
		1B - Mapping version			
		2B - MLe = 000F9h			
		2B - MLc = 000F6h			
		NDEF File Ctrl TLV	1B - Tag = 04h		The NDEF file control TLV is mandatory
			1B - Len = 06h		
			6B - Val	2B - File Identifier	
				2B - Max file size	
				1B - Read access	
		1B - Write access			
		Proprietary File Ctrl TLV (1)	1B - Tag = 05h		Zero or more proprietary file control TLVs
			1B - Len = 06h		
			6B - Val	2B - File Identifier	
				2B - Max file size	
	1B - Read access				
	1B - Write access				
	⋮				
	Proprietary File Ctrl TLV (N)	1B - Tag = 05h			
		1B - Len = 06h			
		6B - Val	2B - File Identifier		
			2B - Max file size		
			1B - Read access		
	1B - Write access				
NDEF File  Selectable by File ID = xxyyh	2B - Len		Mandatory NDEF file		
	xB - Binary NDEF file content				
	yB - Unused if Len < Max file size in File Ctrl TLV				
Proprietary File (1)  Selectable by File ID = xxyyh	2B - Len		Optional proprietary file		
	xB - Binary proprietary file content				
	yB - Unused if Len < Max file size in File Ctrl TLV				
⋮					
Proprietary File (N)  Selectable by File ID = xxyyh	2B - Len		Optional proprietary file		
	xB - Binary proprietary file content				
	yB - Unused if Len < Max file size in File Ctrl TLV				



**Figure 5-11. Recommended NDEF Memory Flow**

### 5.9.1 NDEF Error Check

With the RF interface is enabled, the basic NDEF structure is automatically checked for correctness. If any of the following conditions are true, the error check fails, an NDEF error IRQ is triggered, and the RF interface remains disabled.

- CLEN less than 0x000F or greater than 0xFFFFE.
- MLe value is less than 0xF. Note, for best performance the MLe value should be programmed to 0x00F9.
- MLc is equal to zero. Note, for best performance the MLc value should be programmed to 0x00F6.
- TLV tag does not equal 0x4.
- TLV length does not equal 0x6.
- File ID equals 0, or 0xE102, or 0xE103, or 0x3F00, or 0x3FFF, or 0xFFFF.
- Max NDEF size is less than 0x5 or greater than 0xFFFFE.
- Read access is greater than 0 and less than 0x80.
- Write Access is greater than 0 and less than 0x80.

Also the proprietary TLVs are checked. The check fails if any of the following conditions are true.

- TLV tag does not equal 0x05.
- TLV length does not equal 0x6.
- File ID equals 0, or 0xE102, or 0xE103, or 0x3F00, or 0x3FFF, or 0xFFFF.
- Max NDEF size is less than 0x5 or greater than 0xFFFFE.
- Read access is greater than 0 and less than 0x80.
- Write Access is greater than 0 and less than 0x80.

### 5.10 Typical Usage Scenario

A typical usage scenario is as follows:

1. Write capability container and messages into the NDEF memory (starting from address 0) using the serial interface.
2. Enable interrupts (especially End of Read and End of Write).
3. Configure the interrupt pin INTO as needed and enable the RF interface.
4. Wait for interrupt signaled by INTO.
5. Disable RF interface (but keep INTO settings unchanged).
6. Read interrupt flag register to determine interrupt sources.
7. Clear interrupt flags. INTO returns to inactive state.
8. Read and modify NDEF memory as needed.
9. Enable RF interface again (keeping INTO settings unchanged) and continue with .

### 5.11 References

ISO/IEC 14443-2: 2001, Part 2: Radio frequency interface power and signal interface

ISO/IEC 14443-3: 2001, Part 3: Initialization and anticollision

ISO/IEC 14443-4: 2001, Part 4: Transmission protocols

ISO/IEC 18092, NFC Communication Interface and Protocol-1 (NFCIP-1)

ISO/IEC 21481, NFC Communication Interface Protocol-2 (NFCIP-2)

NDEF NFC Forum Spec, NFC Data Exchange Format Specification

## 6 Device and Documentation Support

### 6.1 Device Support

#### 6.1.1 Development Support

##### 6.1.1.1 Getting Started and Next Steps

For more information on the RF430 family of devices and the tools and software that are available to help with your development, visit the [Tools & Software for NFC / RFID](#) page.

The Dynamic Near Field Communication (NFC) Type 4B Tag design ([TIDM-DYNAMICNFC TAG](#)) outlines the required components, layout considerations, and provides firmware examples to implement NFC into applications such as *Bluetooth*/Wi-Fi pairing, equipment configuration and diagnostics, or as a general purpose NFC data interface. The documentation, hardware, and example code provided allows the designer to quickly implement NFC functionality with an MSP430™ MCU or other MCU of choice.

#### 6.1.2 Device and Development Tool Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all RF430 MCU devices and support tools. Each commercial family member has one of three prefixes: RF, P, or X (for example, RF430CL330H). Texas Instruments recommends two of three possible prefix designators for its support tools: RF and X. These prefixes represent evolutionary stages of product development from engineering prototypes (with X for devices and tools) through fully qualified production devices and tools (with RF for devices tools).

Device development evolutionary flow:

**X** – Experimental device that is not necessarily representative of the final device's electrical specifications

**P** – Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification

**RF** – Fully qualified production device

Support tool development evolutionary flow:

**X** – Development-support product that has not yet completed Texas Instruments internal qualification testing.

**RF** – Fully-qualified development-support product

X and P devices and X development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

RF devices and RF development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X and P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, RGE) and temperature range (for example, T). [Figure 6-1](#) provides a legend for reading the complete device name for any family member.

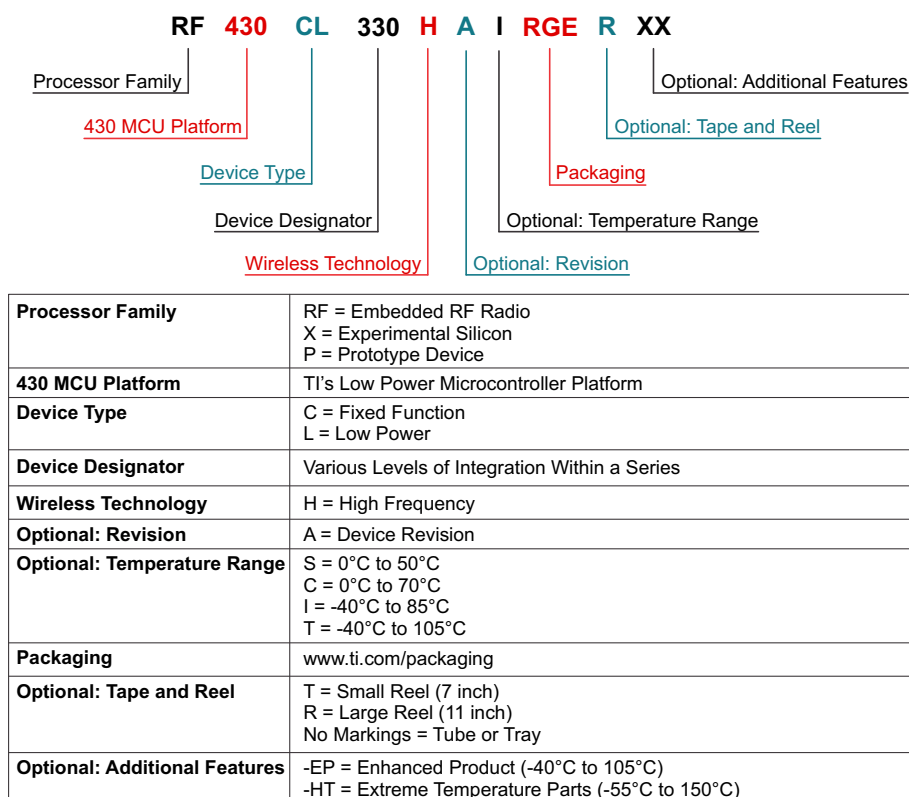


Figure 6-1. Device Nomenclature

## 6.2 Documentation Support

The following documents describe the RF430CL330H device. Copies of these documents are available on the Internet at [www.ti.com](http://www.ti.com).

[SLAZ540](#) **RF430CL330H Device Erratasheet.** Describes the known exceptions to the functional specifications for the RF430CL330H device.

[SLOA187](#) **Automating Bluetooth(R) Pairing With Near-Field Communications (NFC).** This collaborative document is a follow up to a previously released specification by the NFC Forum titled *NFC Forum Connection Handover Specification*, which began to define the structure and sequence of interactions that enable two NFC-enabled devices to establish a connection using other wireless communication technologies. This application report explains how to implement the NFC Forum/Bluetooth SIG specification in an embedded application using the RF430CL330H dynamic NFC transponder.

## 6.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### [TI E2E™ Community](#)

**TI's Engineer-to-Engineer (E2E) Community.** Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

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## 6.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 6.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 7 Mechanical Packaging and Orderable Information

## 7.1 Packaging Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
RF430CL330HCPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CL330H	<a href="#">Samples</a>
RF430CL330HIRGTR	ACTIVE	VQFN	RGT	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CL330H	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
RF430CL330HCPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
RF430CL330HIRGTR	VQFN	RGT	16	2000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
RF430CL330HCPWR	TSSOP	PW	14	2000	338.1	338.1	20.6
RF430CL330HIRGTR	VQFN	RGT	16	2000	336.6	336.6	28.6

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

**RGT 16**

**GENERIC PACKAGE VIEW**

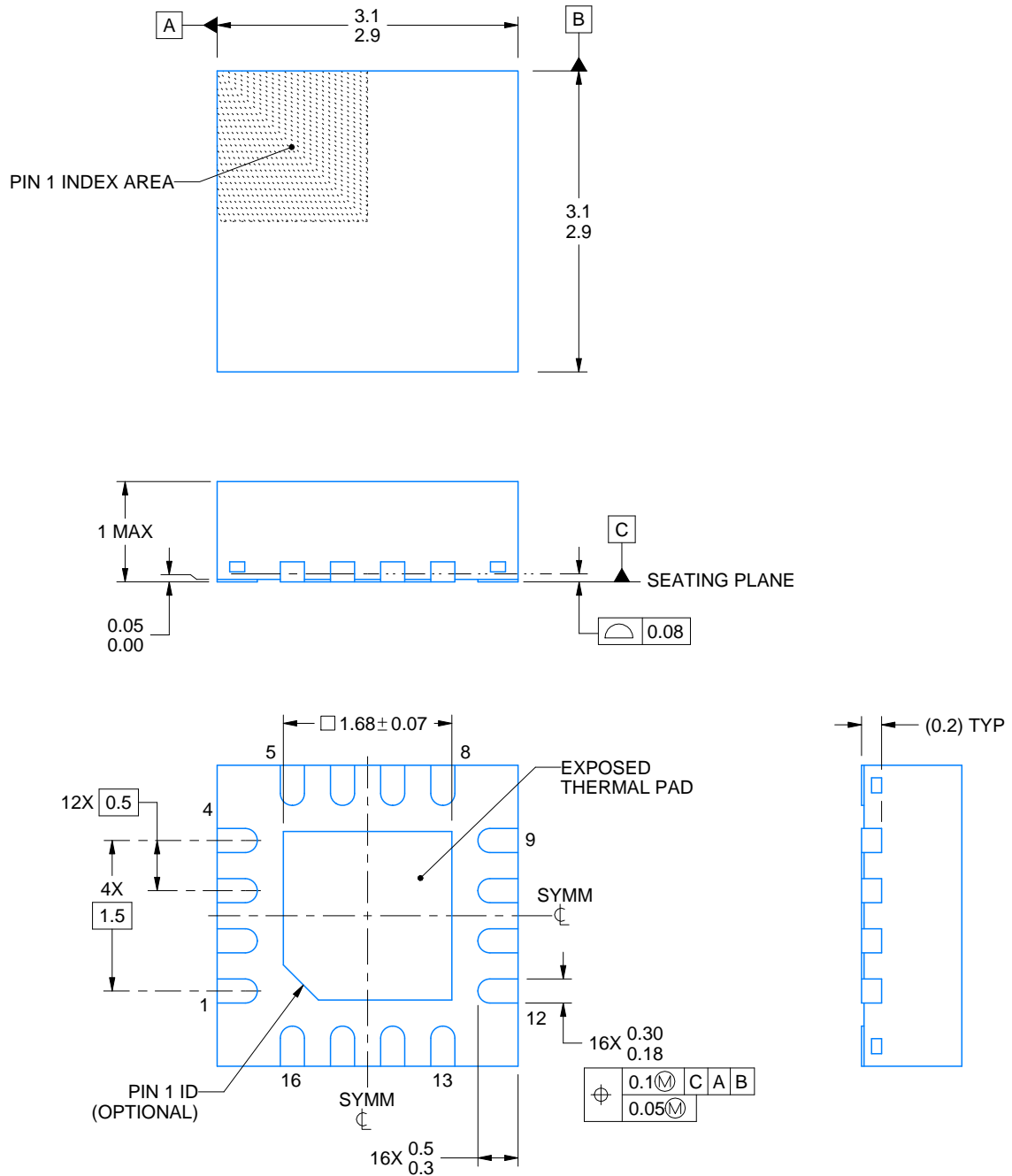
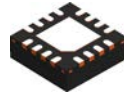
**VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4203495/1



4222419/B 11/2016

## NOTES:

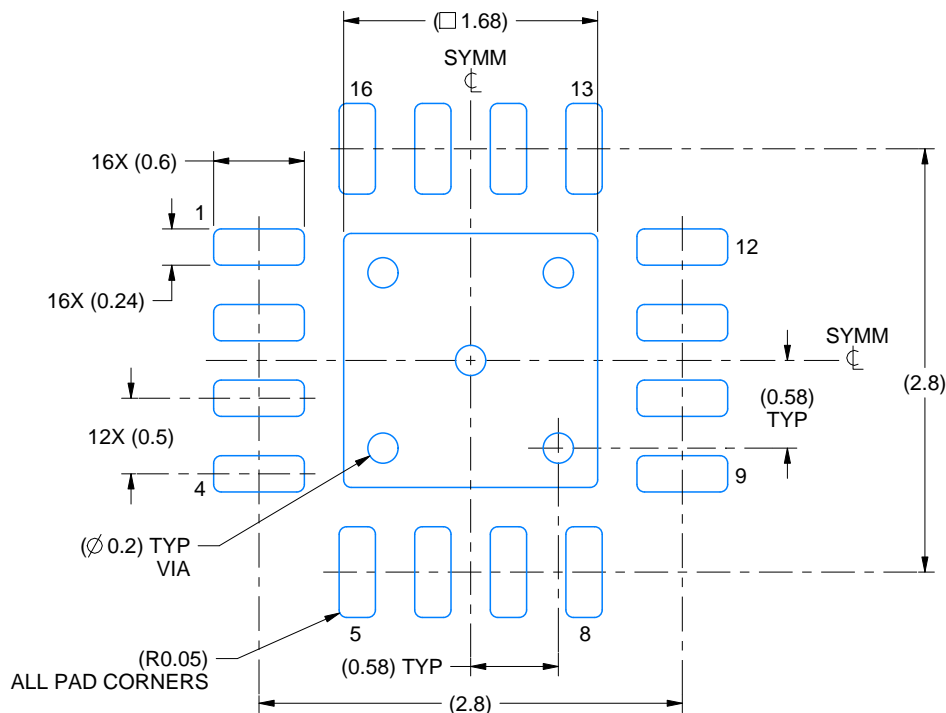
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

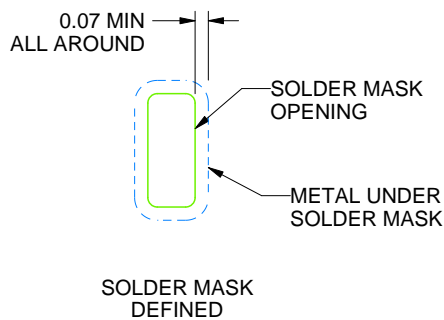
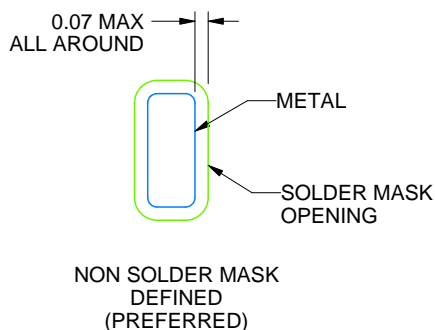
RGT0016C

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
SCALE:20X



SOLDER MASK DETAILS

4222419/B 11/2016

NOTES: (continued)

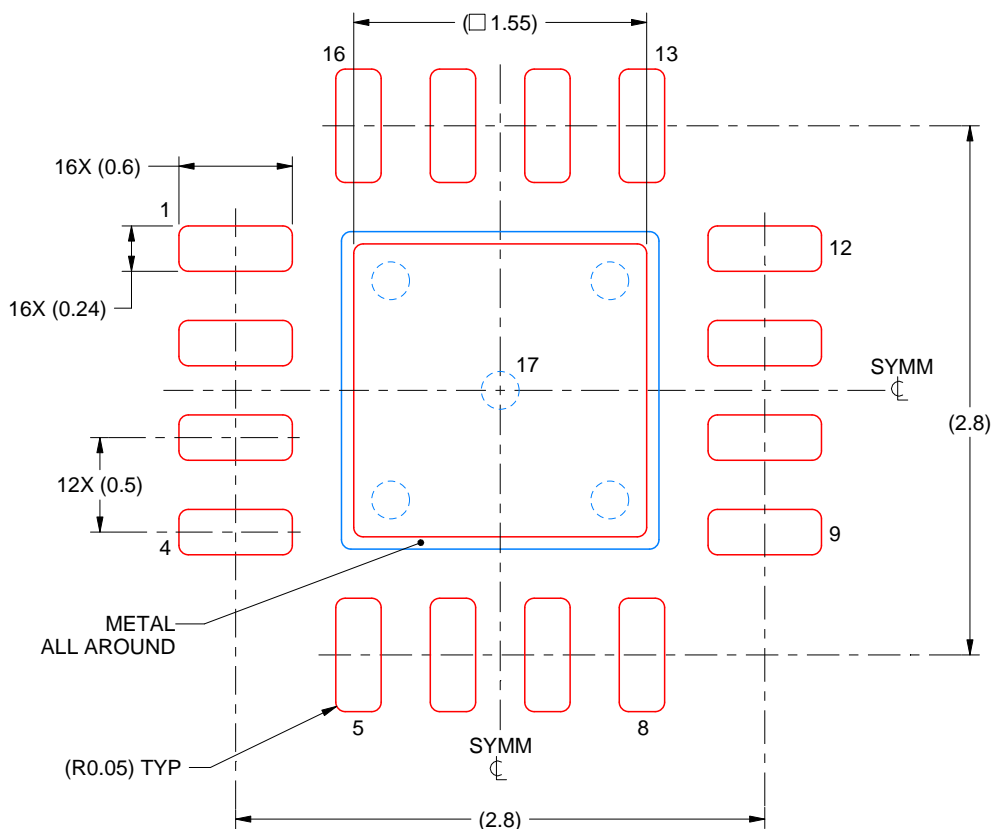
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slue271](http://www.ti.com/lit/slue271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



**RGT0016C**

### VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



## SOLDER PASTE EXAMPLE BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:  
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:25X

4222419/B 11/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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