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Analysis and Simulations of Hybrid Circuit Breaker Technologies in Multi-Terminal HVDC Networks

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Problem Description

The future HVDC network is considered to be meshed with multi-terminals, in order to obtain sufficient flexibility and reliability. A vital part to achieve this is HVDC circuit breaker technology. This report will focus on the circuit breaker and how to interrupt a DC side fault in a selective way. The interruption methods, different circuit breaker technologies, and the requirements for multi-terminal operation will be further investigated. The desired circuit breaker topology will be investigated and simulated in depth. The circuit breaker is to be implemented in a multi-terminal network, and extensively tested for operation under steady-state and during fault conditions, using the numerical simulation tool PSCAD.

Abstract

It is established that voltage source converters (VSC) are required for multi-terminal operation of a HVDC network. This converter technology is vulnerable to DC side faults, and it is crucial for a fast interruption to avoid its freewheeling diodes to have a breakdown. Several circuit breakers have been investigated to find the best one for multi-terminal operation. It is found that the fastest circuit breaker, with a reasonable on-state loss, is the hybrid circuit breaker. Two circuit breaker models are tested, active hybrid circuit breaker with 1 % on-state losses, and passive hybrid circuit breaker with 0.001 % on-state losses. They are compared to check how the interruption time will affect the system, and the requirements of the circuit breaker.

For a multi-terminal operation, it is important with a proper detection algorithm. The algorithm allows for a proper detection of the fault and where it has occurred. This is important for a seamless operation of the multi-terminal network. It is found that the derivative of the current is a good detection algorithm, as it is quite simple and works properly. A fault that occurs close to the converter in a symmetrical system is difficult to handle for the circuit breakers detection algorithm. This is due to the similar magnitude of the derivative that may occur on the circuit breakers in the adjacent cables.

When the faulty cable is isolated, the power flow will change direction through the adjacent cable. This gives a seamless operation of the multi-terminal network. It is found that the faulty cable can be isolated within 3 ms, using the active hybrid circuit breaker.

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Acronyms

AC Alternating Current

A-HCB Active Hybrid Circuit Breaker

BJT Bipolar Junction Transistor

CB Circuit Breaker

CLR Current Limiting Reactor

CSC Current Source Converter

DC Direct Current

FCL Fault Current Limiter

JFET Junction gate Field-Effect Transistor

GTO Gate Turn-Off Thyristor

HVAC High Voltage Alternating Current

HVDC High Voltage Direct Current

IGBT Insulated Gate Bipolar Transistor

LCS Load Commutation Switch

MMC Modular Multilevel Converter

MOA Metal Oxide Arrester

MOV Metal Oxide Varistor

MOSFET Metal Oxide Semiconductor Field-Effect Transistor

MTDC Multi Terminal Direct Current

OHL Overhead Line

P-HCB Passive Hybrid Circuit Breaker

UFD Ultra-Fast Disconnecter

VSC Voltage Source Converter

XLPE Cross-linked Polyethylene

ZnO Zinc Oxide

Chapter 1

Introduction

1.1 Background

The green energy shift is a political desire by EU, and states that 20 % of the energy consumption should be from renewable sources. This decision was made in 2005, when the final consumption of energy from renewable sources was 8.7 %.[1]

In the aftermath of the Fukushima accident, there has been a pressing desire in Europe to move away from atomic energy production. To meet the same consumption requirements, a mass development of renewable sources is necessary. The renewable energy sources not yet exploited and with the highest potential is offshore wind power and solar power.

Wind and solar power production will vary from day to day, and gives an uncertainty to the daily output power. It is proposed to use the existing hydro power plants as green batteries by changing them to pumped-storage hydro power plants. This will allow for better handling on the shifting power generation from solar and wind power.

The remote location of the renewable power production and large transferring of power, will produce high losses if transferred by HVAC. HVDC have superior transferring capability over HVAC for long distances. However there are some challenges related with the HVDC transmission. The largest obstacle is considered to be the interruption of DC current. The HVDC CBs is complex, and have stricter requirements than the HVAC CBs.

A HVDC CB will make it possible for an Multi Terminal Direct Current (MTDC) network. A MTDC network allows for a higher redundancy in the net-

work, and higher power flow.

1.2 Scope of This Thesis

The scope of this thesis is to investigate the different HVDC CB topologies and their operational principle. The interruption time and losses of the best performing Circuit Breaker (CB) are to be evaluated. The superior CB will be thoroughly tested before implemented in a multi-terminal network.

1.3 Limitations

The HVDC CB and the MTDC network is a large topic, and the time does not allow for a detailed study of all components. For implementation of the CB in an MTDC network there are some limitations in the simulation program used, PSCAD. The educational version of PSCAD has a limitation of 250 electrical nodes, and some reduction and simplifications are necessary before simulations of the MTDC network.

1.4 Methodology

Based on the theoretical background, a simulation model of the hybrid CBs will be thoroughly tested to check their viability in a multi-terminal network. Three different test systems are created to determine the viability of the hybrid CBs.

All simulations are conducted in the electromagnetic transient simulation software PSCAD.

1.5 Main Contributions

This report is looking into details of the hybrid CB, its components and operation. The hybrid CB is tested in MTDC operation, preparing for implementation of the hybrid CB in a larger network, and its operation.

1.6 Structure of the Thesis

Chapter 2: Background on the present HVDC network and future MTDC network.

Chapter 3: Theoretical background information about the fault current interruption methods and the proposed CB topologies.

Chapter 4: More detailed description of the hybrid CB topologies considered, and the components in the CB. Theory and background regarding the electric arc.

Chapter 5: Introduction to the simulation models used in this report, and previous work done in the same field of study. The results of the hybrid CB testing, and the MTDC grid implementation.

Chapter 6: Conclusion of the theoretical background and simulations results obtained

Chapter 7: Discussion of future work to be done in this field

Chapter 2

HVDC Background

This chapter will introduce the potentials of High Voltage Direct Current (HVDC) transmission, and the MTDC network. It will also introduce the converter technology available for MTDC operation.

2.1 Why HVDC Transmission?

The classical transmission system is Alternating Current (AC) Overhead Line (OHL). The AC system is very reliable and easy to operate, at least in the terms of short circuit faults . It has several advantages over Direct Current (DC) transmission systems, but the AC system has some disadvantages for long transmissions. This is due to the frequency dependent quantities that will increase with the length. Long transmissions with AC are undesired, unless largely compensated.

Considering the same system with the same arrangement of the conductors, voltage level of the insulation, same resistance and amount of transferred power. For this system, the power losses of the DC system will be half of the losses in the AC system. Due to the larger amount of power that can be transferred, no skin and proximity effect, and simpler line construction, the environmental impact will be less for a DC system. Figure 2.1 gives an illustration of the effect of DC OHL compared to AC. It shows how the transmission right of way may be drastically reduced for the same voltage level and transferred power. [2, 3]

The frequency dependent parameters consumes a lot of reactive power, thus long lines consumes a lot of reactive power. For long transmission lines, reactive power compensation is needed. DC on the other hand, has only resistive losses in the transmission line. Given this information, Figure 2.2 illustrates the break-even cost for AC and DC transmission for both OHL and cable transmission. The

break-even distance for OHL is about 800 km, and for cables approximately 50 km. These values takes into account reactive compensation of the AC system. [2, 4]

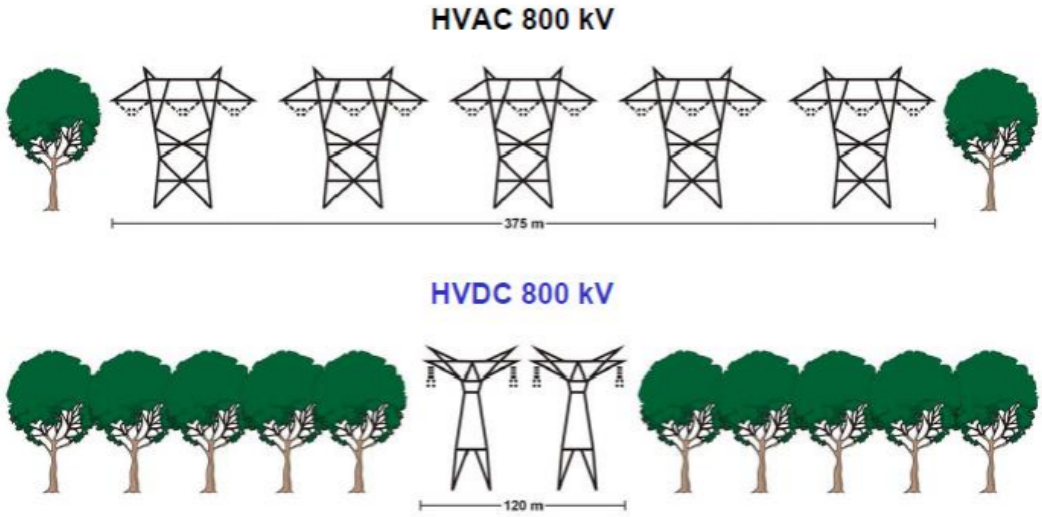


Figure 2.1: Environmental impact of AC and DC OHL [2]

2.2 The HVDC Network

The present HVDC network is mainly for long distance cables, but some bulk OHL installations exist. Today's HVDC network is mostly point-to-point connected, with a few exceptions.

Point-to-point connection gives little to none redundancy, and is unreliable if a fault occurs. To make the HVDC network more reliable, a MTDC network has been proposed. MTDC network gives a higher redundancy and power transferring capability, but at a higher cost, similar to the present AC network.

If a MTDC grid without DC CB is used, the network will have many converter stations, illustrated with the white squares in the left part of figure 2.3. If the same network uses DC CBs, the number of converters can be reduced, illustrated by the black squares in the right part of Figure 2.3.

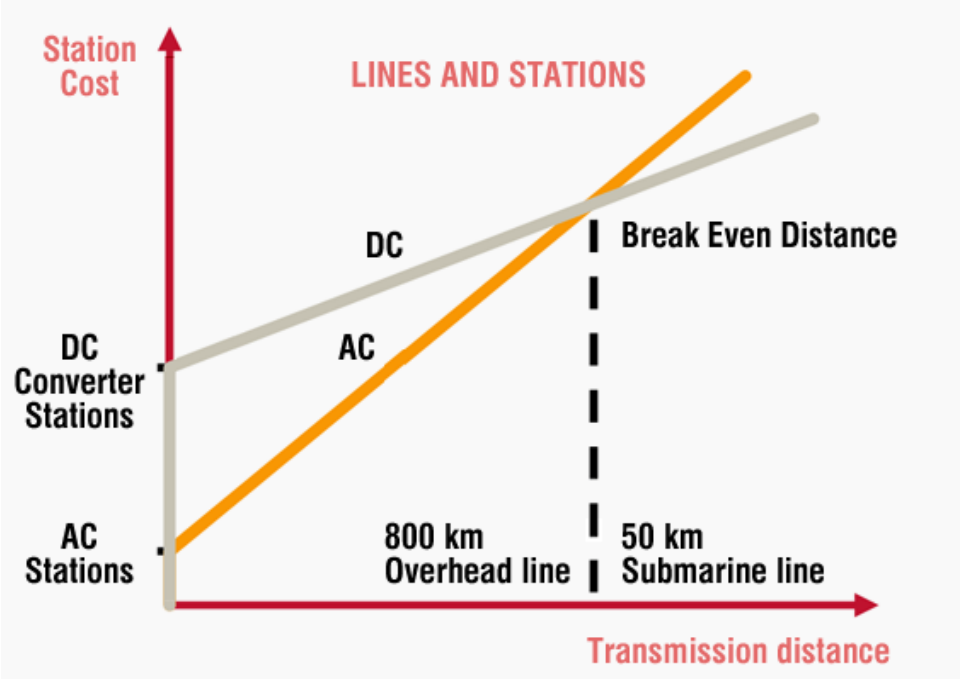


Figure 2.2: Cost comparison of AC and DC [4]

The green shift in Europe will change the power generation from fossil fuel, to a more decentralized renewable power generation. The remote location of renewable generation, gives a need for HVDC transmission. The renewable power generation is often unreliable, and only produces power during certain periods and conditions. Therefore it might be large variations in produced energy from day-to-day. To balance out the production variation, it is crucial to have a way of quickly storing and utilization of energy. Thus the hydroelectric dams might be used as a green battery, by pumping water from the outlet and up to the dam. The interconnection of solar power plants in the Sahara, offshore wind energy from the North Sea and hydro power in Norway and Switzerland requires a vast DC network. This network is illustrated in Figure 2.4. It is labelled as the European super grid, and will have the ability to transfer vast amounts of energy with minimum losses.

2.3 The Multi-Terminal DC Network

The idea of a MTDC network is not a new conception. In 1972 the reasons for installing a MTDC was stated in [7]:

1. The cost can be significantly reduced since fewer converters are necessary.

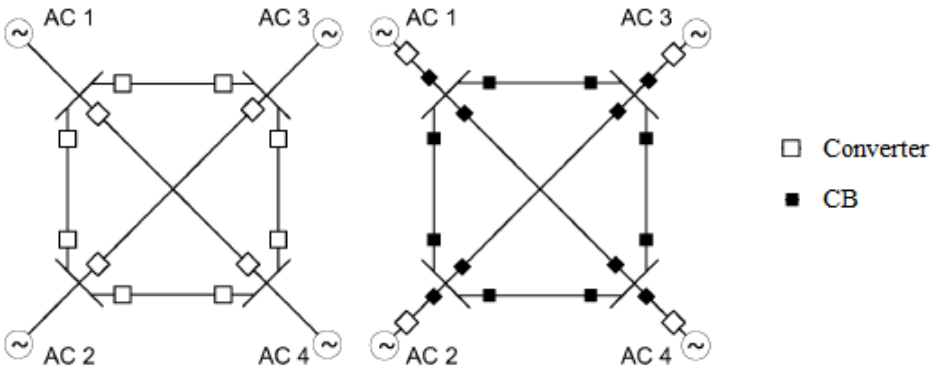


Figure 2.3: Comparison of a HVDC network with and without CBs [5]

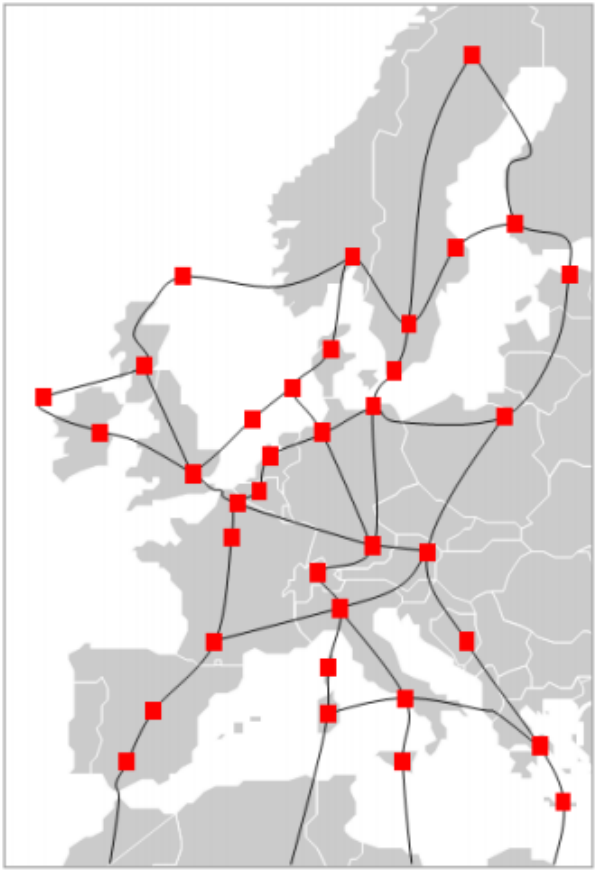


Figure 2.4: The MTDC network proposed by ABB [6]

2. Reducing the number of converters minimizes the total losses due to high converter losses.

3. MTDC operation gives a more flexible system with higher redundancy and overload capability.

These reasons sums up why MTDC network is desired over point-to-point connections. There is already a vast number of point-to-point connections around the world. The logical next step towards a MTDC network is by connecting the existing converter stations to each other. In practice this can be done by changing the CSC converter stations to VSC. To maintain the reliability it is important to introduce a protection scheme, that allows for a seamless operation if a DC fault occurs. This protection scheme was presented on the right hand side of Figure 2.3.

2.3.1 Voltage Source Converter

The Voltage Source Converter (VSC) uses Insulated Gate Bipolar Transistor (IGBT)s and diodes in an anti-parallel pair to convert the power. Unlike the CSC that uses thyristors to convert the power, the VSC system allows for a reversal of power flow by reversing the current and not by changing the voltage polarity. For VSC a cheaper cable insulation, Cross-linked Polyethylene (XLPE), may be used [8]. The VSC converter system allows for control of both active power and voltage independently at different nodes. This is essential for a proper control of a MTDC network with several nodes. Figure 2.5 illustrates the 6-pulse VSC in a classical Graetz bridge configuration. Newer VSC systems rarely use this two-level topology, but rather a three- or five-level VSC. The increased level of the VSC topology allows for a better control of the converter.

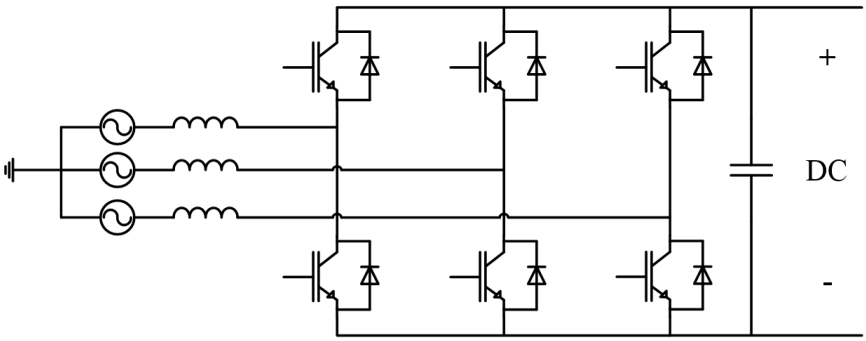


Figure 2.5: 6-pulse Voltage Source Converter in a Graetz bridge [8]

Modular Multilevel Converter

The Modular Multilevel Converter (MMC) consists of several different submodules in series at each leg of the converter, as shown in Figure 2.6 shows. The submodules are basically small single phase converters. There are three main types of submodules, the half-bridge, the full-bridge and clamp-double, as illustrated in Figure 2.7. They have different attributes, but all have an internal capacitor to smooth out the voltage and power. The internal capacitor is quite small, but there are many of them, one in each submodule. When a fault occurs in a MMC system based on half-bridge submodules, the fault will find a way through the diodes [9]. The full-bridge and clamp-double submodules have the ability to interrupt the current flow.

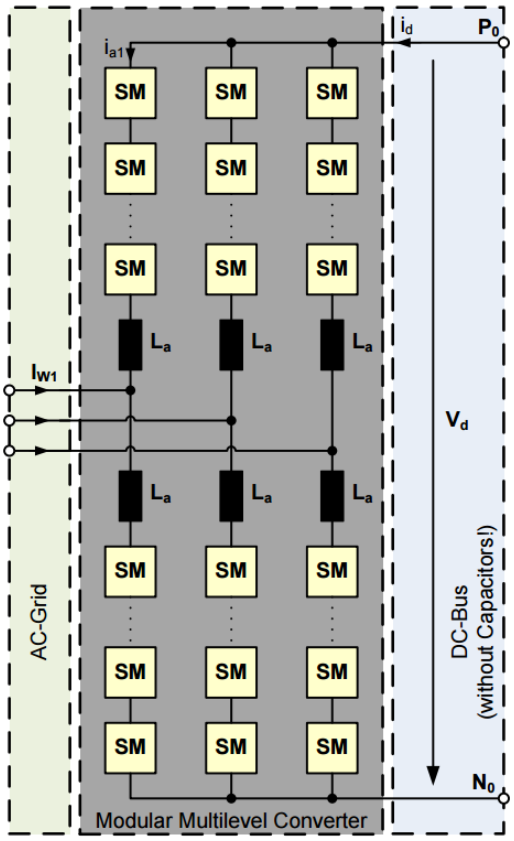
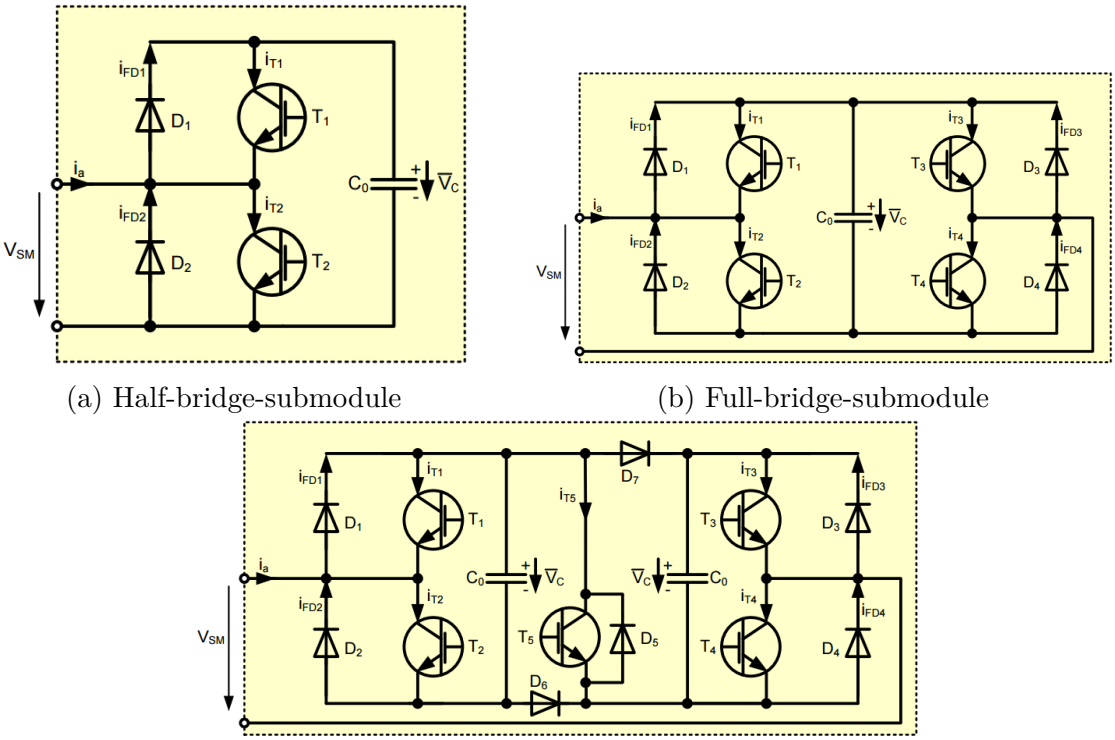


Figure 2.6: MMC topology and submodule arrangements [10]



(a) Half-bridge-submodule

(b) Full-bridge-submodule

(c) Clamp-double-submodule

Figure 2.7: Submodules for the MMC [10]

Comparison of Converter technologies

A comparison of the converter technologies available is illustrated in Table 2.1. As mentioned earlier, the lack of control of active and reactive power makes the CSC an undesirable technology for MTDC operation, but is added in this table as a reference for the newer technologies. The VSC has higher switching losses than the thyristor based CSC technology, but the switching losses may be reduced by increasing the levels of the converter. This becomes more clear with the MMC, where the switching losses are as low as 0.69 %. Since the MMC technology based on the VSC, they are very similar in most aspects, as illustrated in the table. The most significant difference is the complexity of the MMC, which gives a higher converter cost, but also allows for current interruption by the MMC. The black start capability of both VSC and MMC allows for easier start-up of offshore wind farms, and other island grids.

Table 2.1: Comparison of the converter technologies [3, 8]

	CSC	**VSC**	**MMC**
Fault handling	AC or DC side CB	DC side CB	DC side CB, full-bridge and clamp-double submodules may block the fault currents
Switching losses	0.7%	1.7% for two-level, 1 % for five-level Decreasing with higher levels	0.69% for half-bridge submodules
Energy storage	Inductive	Capacitive	Capacitive
Station area	Large	Compact 50-60% of LCC	Compact, similar as VSC
Price	Low	10-15% higher than LCC	Higher
Control of active and reactive power	No	Yes	Yes
Control	Simple	More complex. Increase with levels	Most complex
Black-start capability	No	Yes	Yes

Table 2.2: Existing MTDC networks [11–15]

Name of Connection	**Connections**	**Put in service**	**Converter**
SACOI 1	3	1986	CSC
SACOI 2	3	1992	CSC
Quebec - New Engalnd	3	1992	CSC
Nanao Island	3	2014	VSC
Zhoushan Island	5	2014	VSC (MMC)
North-East Agra	3	2016	CSC

2.3.2 MTDC Projects

In Table 2.2, the existing MTDC networks are listed. It is shown how the most MTDC networks uses CSC technology. The first MTDC network to use VSC

technology was the Nan'ao island connection. Since then there has been built one additional MTDC network, the connection to Zhoushan island and its surrounding wind power plants. This network have a revolutionary 5 nodes.

2.4 Discussion

For long distances there is clear advantages of using HVDC transmission, compared to HVAC. For distances around 800 km, the cost of the systems are equal, but the most important aspect is the environmental. Choosing HVDC transmission instead of HVAC, the transmission right of way might be drastically reduced, or the capacity increased. HVDC also gives the possibility of subsea cables, and cables in the soil. By doing this, the environmental footprint will be reduced to the converter stations.

If there are several point-to-point connections close to each other, it could be beneficial to connect them, and thereby reducing the numbers of converters. In order for a large MTDC network to operate as desired, it is important to use VSC technology. Using the VSC, the costs and losses of the system will increase, but it allows for a better control. It is also an important aspect to consider that the size of the converter station will be reduced.

Most of the MTDC networks in operation today uses CSC technology, but as can be seen in Table 2.2, they are limited to 3 nodes. VSC on the other hand is more or less unlimited.

Chapter 3

CB Background

This chapter will look into DC faults, its propagation and how to interrupt it. The HVDC CB topologies available are to be discussed and evaluated for MTDC operation.

3.1 DC Faults

There are two types of DC faults that may occur; pole-to-ground and pole-to-pole faults. In this report, the main focus is on an offshore VSC MTDC network, with submarine cables. In such a system, where there are two parallel conductors dug into the seabed, it is considered very unlikely that a pole-to-pole fault is occurring, and the main focus of this report is to investigate pole-to-ground faults. For a HVDC system with OHL the probability for a pole-to-pole fault is significantly increased.

3.1.1 Fault Propagation

VSC systems are exposed to high DC side fault currents that may harm the converter and cable. When a DC side fault occurs, the large capacitors on the VSC will immediately discharge as illustrated in Figure 3.1a. In stage 2 the diodes rectify uncontrolled, so called freewheeling, seen in Figure 3.1b. This is the most challenging phase for the converter diodes since there is an abrupt rise of the fault current, which may damage the diodes. The current is discharged from inductive elements in the AC side . The last stage is AC feeding of the fault, as illustrated in Figure 3.1c. This phase is a steady state condition for the DC side, as the generators are feeding the fault. In practice, this stage will never be reached since the DC breakers should have reacted already. Otherwise, the diodes would probably have been destroyed in the previous phase. The current waveforms during these

stages are illustrated in Figure 3.2. [16]

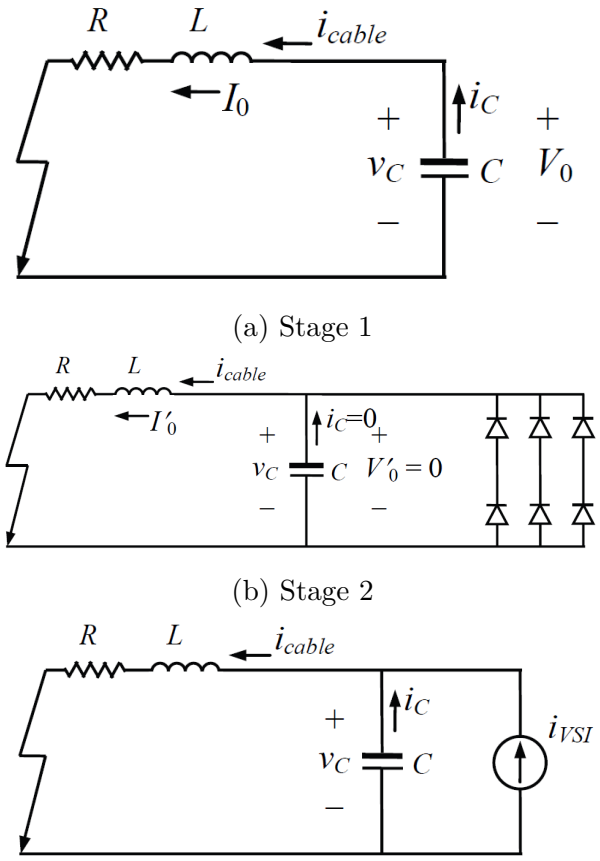


Figure 3.1: DC fault propagation in a two level VSC system [16]

3.2 DC Current Interruption

For a VSC system the only option for interrupting the fault is by a DC CB. To interrupt the DC current with a CB is difficult due to the lack of a current zero crossing. For a proper fault current interruption, a current zero crossing must be produced. This can be accomplished by one out of two following methods:

1. Current injection with opposite polarity

2. Injection of a counteracting voltage

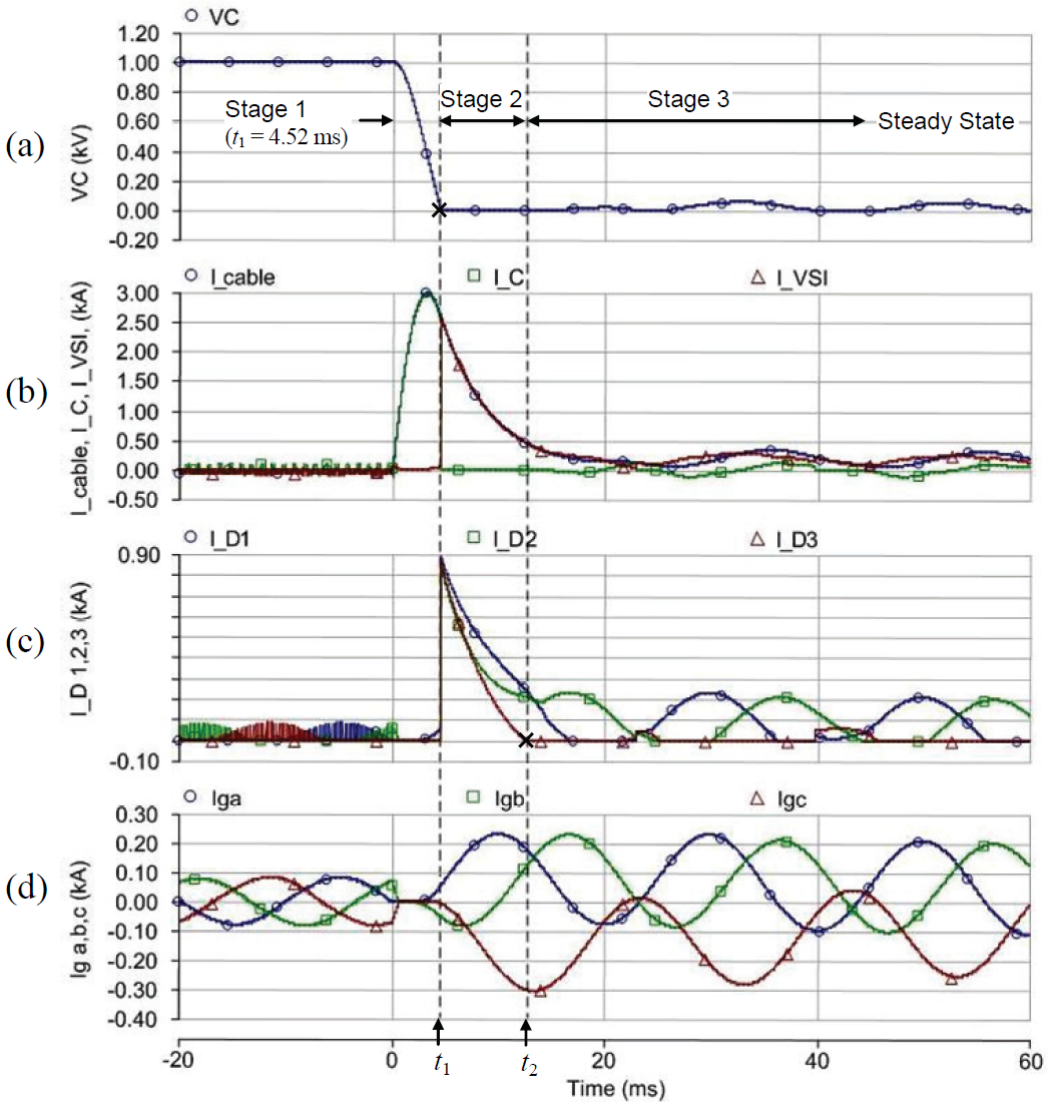


Figure 3.2: Stages for a DC side faults in a two level VSC system: (a) DC-link capacitor voltage v_c; (b) cable current i_{cable}, capacitor current i_C, VSI feeding current i_{VSI}: (c) three-phase diode current $i_{D1,2,3}$; (d) grid side three-phase current $i_{g\ a,b,c}$ [16]

3.2.1 Current Injection With Opposite Polarity

The current injection method inserts a current with opposite polarity to force the fault current to a current zero crossing. In practice this is done with a pre-charged capacitor, creating an opposing current. Since a pre-charged capacitor is used, this current interruption method allows only for a unipolar current interruption,

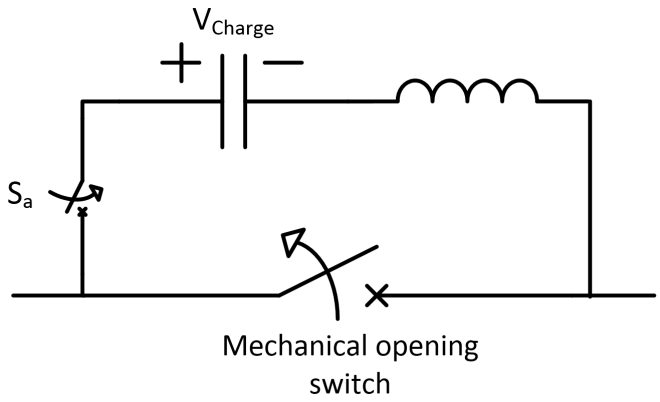


Figure 3.3: Current injection

i.e. only forward direction.

3.2.2 Insertion of a Counteracting Voltage

The insertion of a counteracting voltage forces the fault current to a zero crossing. The counteracting voltage can be created by any resistive element, but the most time efficient method is by a non-linear resistive devise like an arrester. This fault current interruption method allows for a bipolar current interruption. Figure 3.4 show the mechanical switch with the parallel arrester.

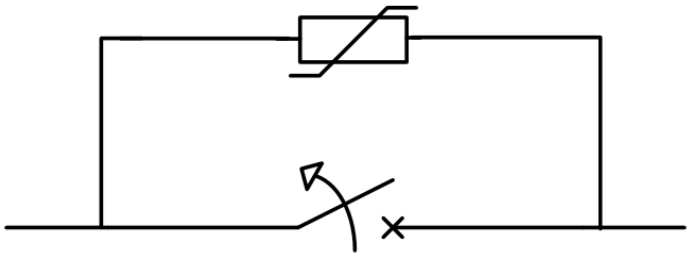


Figure 3.4: Counteracting voltage

Figure 3.5 illustrates a simplified model of the DC system. The system can then be explained by equation (3.1). To create a current zero crossing the voltage across the breaker, V_{CB}, must exceed the system voltage V_{DC}, explained by equation (3.2).[17]

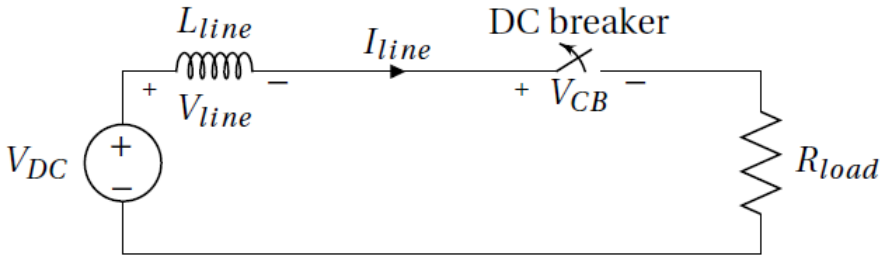


Figure 3.5: Simplified model of the DC system, with an ideal CB [17]

$$\frac{dI_{Line}}{dt} = \frac{V_{DC} - V_{CB}}{L_{Line}} \tag{3.1}$$

$$V_{CB} > V_{DC} \Rightarrow \frac{dI_{Line}}{dt} < 0 \tag{3.2}$$

Magnetic energy to be dissipated by the arrester

Considering an arrester in parallel with the DC CB presented in Figure 3.5, it must be able to absorb the remaining energy in the system. The energy stored can be deduced from the DC system. Equation (3.3) shows the energy dissipation required by the arrester. I_0 is the peak current going through the line. The entire deduction is found in [17]. The arrester are more thoroughly explained in section 4.4.4. [17]

$$W_{tot} = \frac{1}{2} L_{Line} I_0^2 (1 + \frac{V_{DC}}{(V_{CB} - V_{DC})}) \tag{3.3}$$

3.2.3 Current Interruption With MMC

A third method of fault current interruption is by using full-bridge or clamp-double submodules in the MMC. These submodules have the capability to interrupt the current. If such a system is used, the extra stress on the power electronic components in the converter should be taken into consideration, and snubber circuits might be a necessity. The drawback in this system is the lack of a seamless operation, thus disconnecting the entire DC system when a fault occurs. Since the HVDC connection may transfer power in the range hundreds to thousands MW, there might be problems when suddenly disconnecting this, leading to undesired power swings in the AC system. The fault needs to be located, and when there are no charges in the DC system, the load break switches must be disconnected before the MMCs turn on again. This operation will save a lot on the investment

cost, as the HVDC CB is estimated in the same price range as a converter station. [9]

3.3 DC CB Requirements

There are several requirements for a DC CB, they are to be presented. The requirements were discussed more detailed in [8]. The requirements for the CB can be divided into two parts; physical requirements of the mechanical switch, and detection and operational requirements.

The physical requirements for the mechanical switch are the same for both AC and DC CBs. The requirements are found, and explained in [18].

- When the CB is closed, the losses should be approximately zero, it must therefore be an almost perfect electric conductor. The CB must be able to interrupt any currents, without generating unacceptably large over-voltages.
- When the CB is open, it should be a perfect insulator. The contacts should be able to close, without welding together.

The detection and operational requirement describes the detection algorithm requirements and the operational time necessary for proper interruption of the fault current. These requirements are listed in [19, 20].

- **Selectivity** The fault must be detected, located and the faulty component should be isolated from the network.
- **Sensitivity** Every fault must be detected, and no triggering during normal operation.
- **Speed** To prevent the fault to propagate to the healthy parts of the grid, and destruction of components.
- **Reliability** In case the primary protection system fails, a back-up system is required.
- **Robustness** Faults should be detected in all mode of operation.
- **Seamless** The remaining power system should resume to normal operation after fault.

3.4 DC Fault Propagation in a MMC System

It is established that the VSC (or MMC) is a crucial component in able to accomplish a MTDC network. The VSC has exposed diodes in the rectifying path. The fault propagation for a two level VSC system has already been described in section 3.1.1. There are some differences in the fault propagation in a VSC and MMC system, due to the submodules and its internal capacitor. And the three phases of the fault propagation will look different in a MMC. If the fault is not controlled by the submodules, the freewheeling diode phase is likely to be similar, thus leaving the MMC system as vulnerable to DC fault as a VSC.

3.5 HVDC CB in General

There are three different CB technologies available that will be explained in this chapter:

- Resonance CB
- Solid state CB
- Hybrid CB

These technologies are very different in principle and operation, but can be explained by the same general model illustrated in Figure 3.6. For the solid state CB, the nominal path and the commutation path is the same. The HVDC breakers have a low impedance branch for conducting the nominal current, also known as main path. When the fault is detected, the fault will be commutated to the main current interruption branch, shown as commutation path. The absorber path will absorb the energy stored in the system after the other two paths have opened. In practice the parallel paths are not necessary, since the arc in the mechanical switch will create a counteracting voltage by itself. This is very slow, and will not interrupt the current within the desired time. Besides, there is a lot of energy left in the system that must be dissipated to avoid re-ignition of the arc. The parallel paths will help interrupting the current faster, and dissipate the energy left in the system.

The arresters function is not only to create a counteracting voltage, able to exceed the system voltage, but also to absorb the inductive energy stored in the system [21].

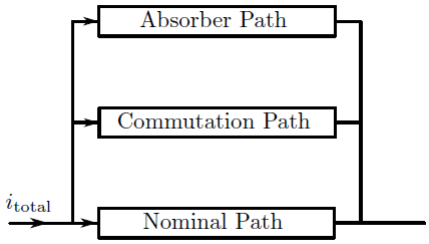


Figure 3.6: General HVDC CB model [22]

3.6 Resonant CB

The resonant CB is the oldest available topology for DC fault current interruption, it uses a mechanical switch in the main branch. This mechanical switch is traditionally a standard spring loaded AC CB, but to improve interruption time a faster disconnecter is possible to use. The commutation path consists of an inductor and a capacitor in series.

3.6.1 Passive Resonant CB

The passive resonant CB uses the principle of a counteracting voltage, and will use between 30-60 ms or more to successfully interrupt the fault current [22, 23]. The topology of the resonant CB can be seen in Figure 3.7. S_1 is a mechanical disconnecter, and must be able to withstand the arcing voltage and temperature. The interruption time is dependent on the opening time of the mechanical switch, whether it is a conventional AC disconnecter or an Ultra-Fast Disconnecter (UFD). Shortly after the fault is detected, S_1 starts to open, and an arc will form between the contact members. Simultaneously S_2 closes and is ready to oscillate the current to a zero crossing, when the arc commutates it to this path. The current will oscillate with a frequency set by the inductor, L, and capacitor, C, in the commutation path. The frequency, f, of the oscillation is given in equation (3.4), and the current amplitude, I_{max}, is shown in equation (3.5), here $V_{capacitor}$ is the voltage across the capacitor.

$$f = \frac{1}{2\pi\sqrt{L \cdot C}} \tag{3.4}$$

$$I_{max} = \sqrt{\frac{C}{L}} \cdot V_{capacitor} \tag{3.5}$$

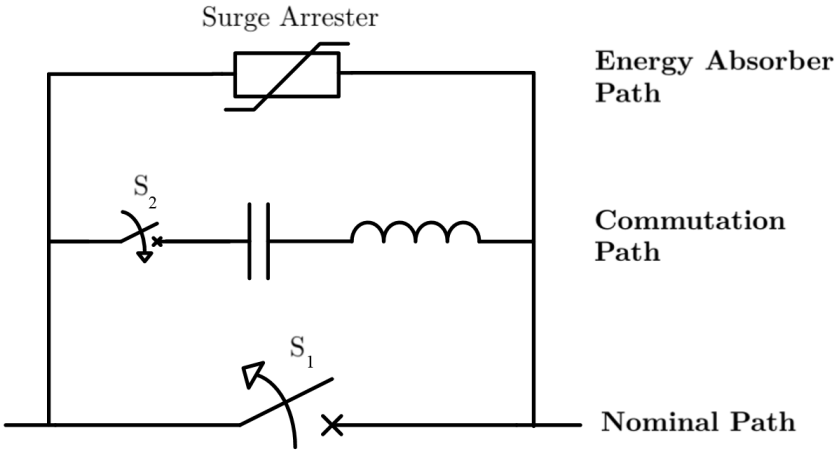


Figure 3.7: Passive Resonant CB

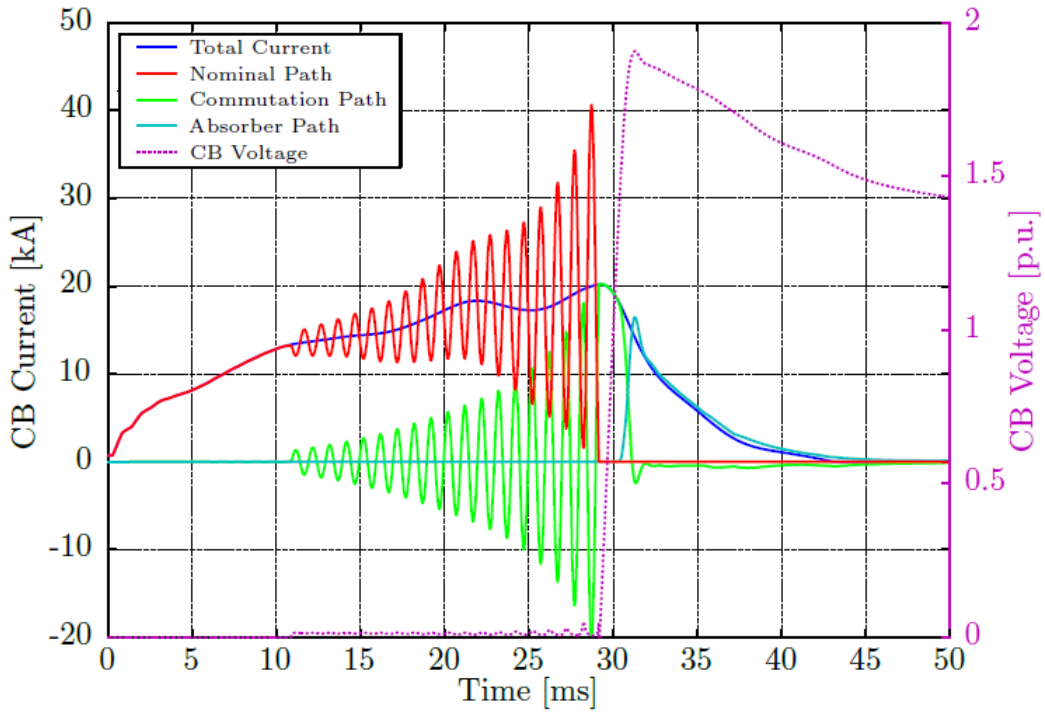


Figure 3.8: Current interruption in passive resonant CB [22]

The currents and voltage behaviour during interruption is illustrated in Figure 3.8. There it can be seen how the current oscillates between the nominal path and the commutation path until $I_{NominalPath} \geq I_{TotalCurrent}$ and the arc is extinguished. Now the entire current will go through the commutation path and the voltage

builds-up until it reaches the threshold values for the arrester. The counteracting voltage will force the total current to zero, and the fault is interrupted within 45 ms.

3.6.2 Active Resonant CB

The active resonant CB uses the principle of current injection, to force the fault current to a zero crossing, and is thus unidirectional. The scheme of the active resonant CB is illustrated in Figure 3.9. The capacitor is pre-charged through closing of S_b, and the current is injected when S_a closes. The waveforms of the fault current can be seen in Figure 3.10. The current will go trough the main path until S_a closes. The total interruption time will be in the range of 10-20 ms, depending on the system and the CB. Since the commutation path is injecting a current with opposite polarity, there will be no oscillation between the main and commutation path as it is for the passive resonant CB. Since there is no need for a oscillation to create a current zero crossing, the interruption process will be much quicker.

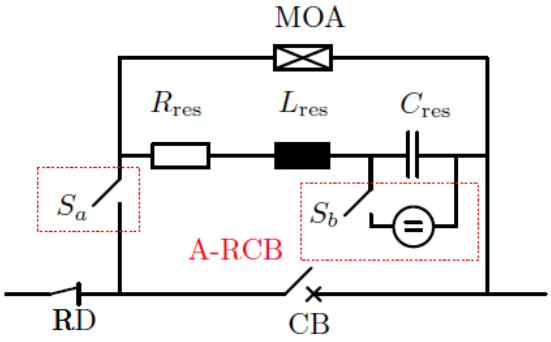


Figure 3.9: Active Resonant CB [22]

3.7 Solid State CB

The solid state CB is illustrated in figure 3.11. The nominal path consists of large strands of IGBTs in series with similar large strands of anti-parallel diodes. The number of the IGBTs and diodes in series depends on the voltage it must withstand. It uses the method of counteracting voltage to interrupt the fault current. When the fault occurs, the IGBTs rapidly turn off. The voltage immediately builds up across the breaker until it reaches the threshold values of the arrester. The arrester creates a counteracting voltage, and starts to force the current to a

zero crossing. The solid state CB allows for a very fast interruption of the fault, typically faster than 1 ms.

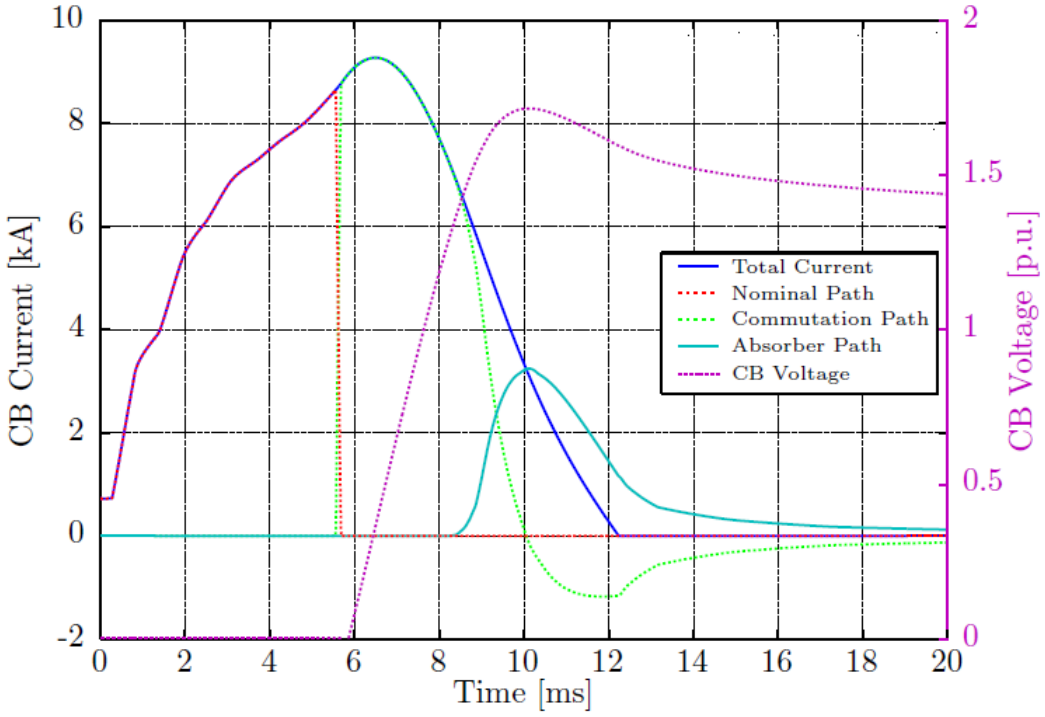


Figure 3.10: Current waveform of the fault current [22]

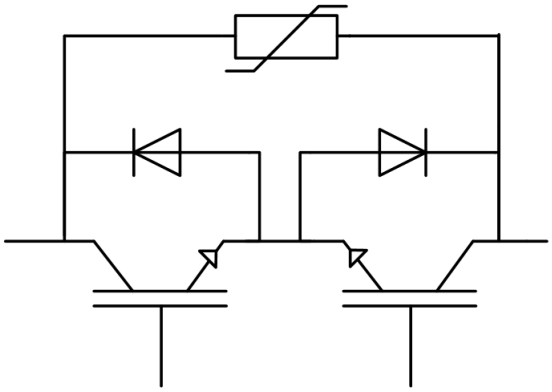


Figure 3.11: Solid state CB [8]

In Figure 3.12 the currents and voltage waveforms for a current interruption can be seen. The turn-off time for the IGBTs could be reduced to less than 1 ms, but the figure illustrates the interruption in a solid state CB quite nicely. It shows how the snubber circuit helps to build up the voltage before the IGBTs turns off. The threshold levels for the arrester is reached when the IGBTs turns off, a counteractive voltage is produced, and the current is forced to a zero crossing.

The power electronic switches in the nominal current path gives very high on-state losses. Since the number of IGBTs in series is voltage dependent, there will be high losses for use in high-voltage application.

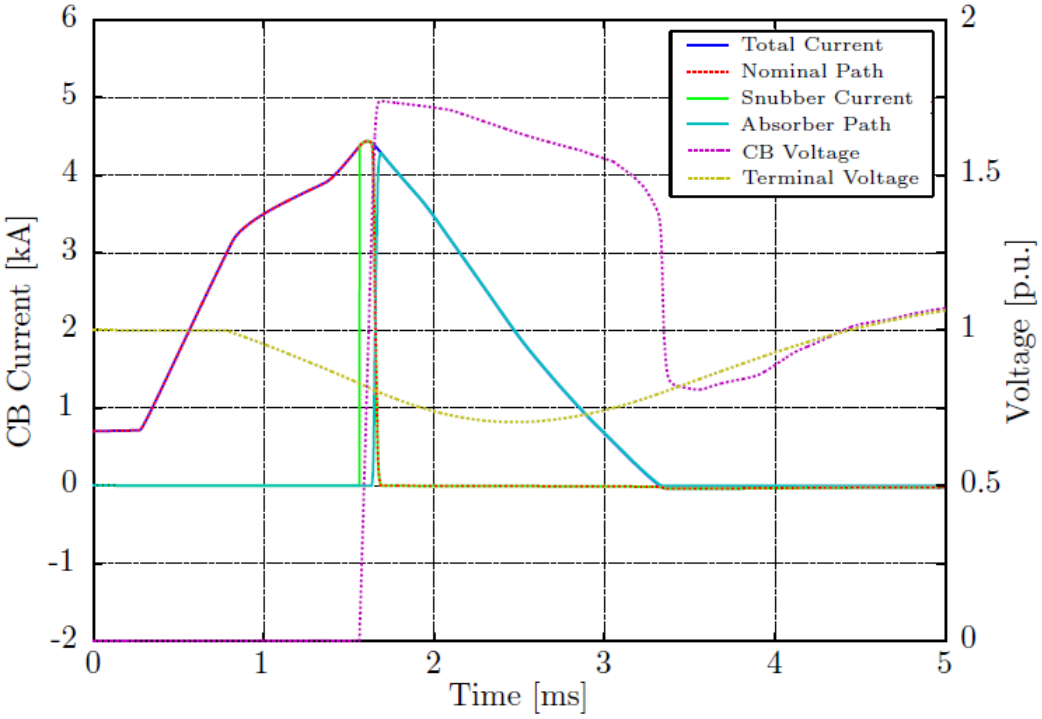


Figure 3.12: Solid state CB current waveform [22]

3.8 Hybrid CB

The hybrid CB is a relatively new invention, developed by ABB in 2011. It combines a mechanical switch and a solid state CB in parallel. There are several different topologies of this HVDC CB presented, the most common is the ones presented below, with and without a LCS in the main path. The one with the LCS in the

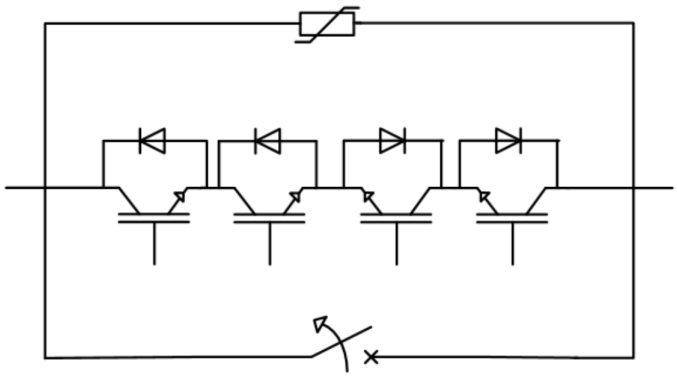


Figure 3.13: P-HCB

nominal path is called Active Hybrid Circuit Breaker (A-HCB), since it actively commutates the fault current. The Passive Hybrid Circuit Breaker (P-HCB) uses the arc that forms in the mechanical switch to commutate the current, and are thus passively commutating the fault current. These are presented with IGBTs as the power electronic switches, but it is possible to use other power electronic devices.

3.8.1 Passive Hybrid CB

The first hybrid CB considered is the P-HCB. This topology uses the arc that forms across the contact members in the mechanical disconnecter to commutate the fault current to the commutation path. With this topology, the steady state losses are negligible, but the arc uses long time to commutate the fault current. It is however possible to have several branches of IGBTs in the commutation path, thus gradually increasing the commutation path resistance (voltage drop), and thus allowing for a faster commutation of the fault current from the main path. The IGBTs in the commutation path will open when the mechanical disconnecter is fully open and full dielectric strength is achieved.

When the fault is detected, the IGBTs in the commutation path will close, and prepare to conduct the fault current. At the same time, the mechanical disconnecter starts to separate and an arc forms. The arc is what commutates the fault current. When the mechanical disconnecter is fully open, and has reached a fully open state, the commutation path IGBTs will turn off, and the voltage will start to build up. The voltage rises abruptly, until it reaches the pre-set values for which the arrester starts to conduct the fault current. When that happens, the fault current will be forced to a zero crossing.

3.8.2 Active Hybrid CB

The topology first presented by ABB in [24], is an A-HCB, and is illustrated in Figure 3.14. This topology allows for a much faster fault current commutation, to the commutation path. When the fault occurs, the commutation path IGBTs and mechanical disconnecter react at the same time, in respect to each other one closes and the other one opens. After a small delay, the LCS will react by opening, hence the commutation process is allowed to happen within 0.5 ms after the fault is detected. Further, this CB topology reacts in the same way as the P-HCB. The interruption time of the fault current, can with this topology be below 2 ms. However the losses in the LCS cannot be neglected. The losses will be around 1 % of the total power. Although far less than the solid state CB, it is much more than the other CBs. Since most of the voltage drop during interruption will be across the mechanical disconnecter, it is not necessary with a large IGBT module in that path, and hence the losses are severely reduced compared to the solid state CB. The interruption process and behaviour can be seen in Figure 3.15. The opening times of each component in this simulation is not optimized, and it is presumed that an UFD has not been used.

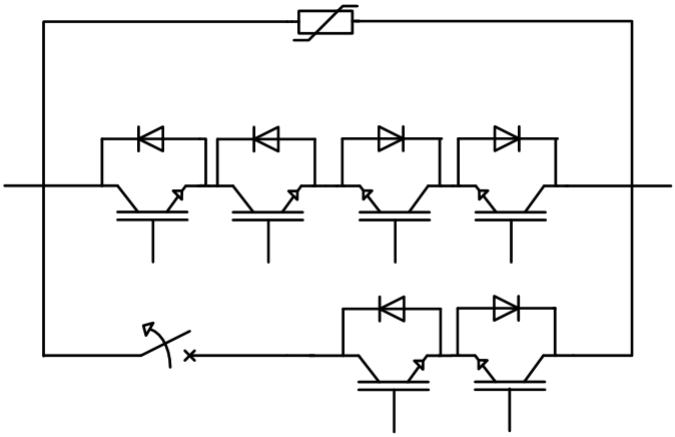


Figure 3.14: A-HCB

3.8.3 Comparison of the Hybrid CBs

It became clear from the two previous sections that there is a trade off between interruption time and power losses in the CB, and this should be more thoroughly investigated.

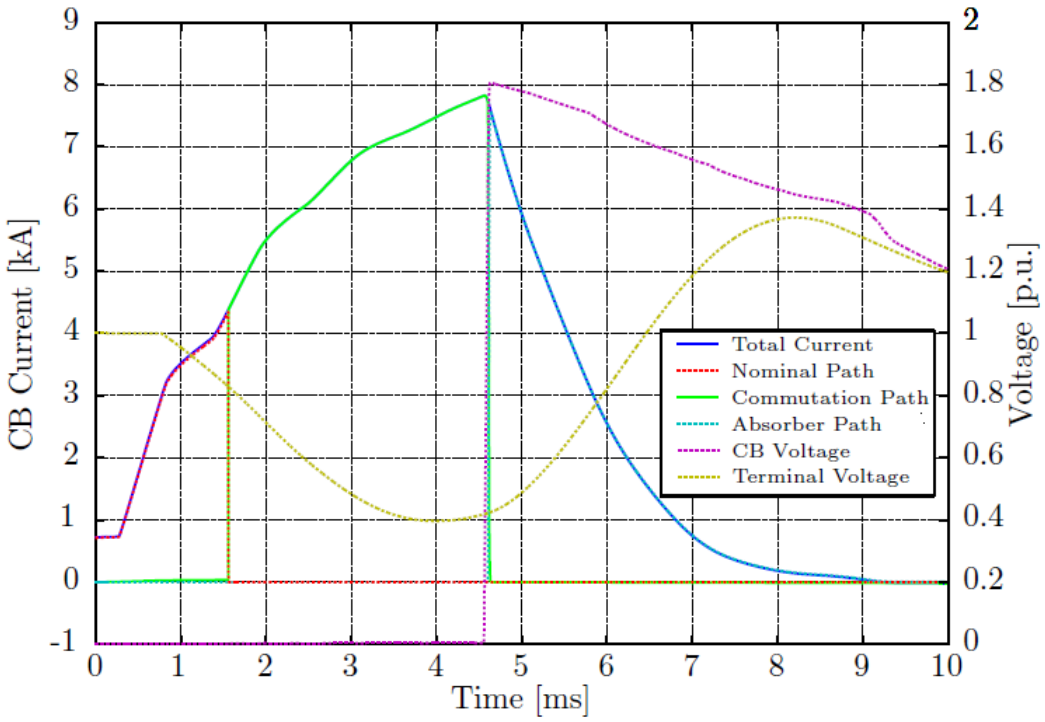


Figure 3.15: Waveform of the fault current in the A-HCB [22]

An increased fault current interruption time, will increase the maximum current breaking capability for the mechanical switch. This increased interruption time will in turn increase the energy to be absorbed by the arrester. The interruption should thus be as fast as possible. The increased energy dissipation required by the arrester, increases the total cost of the CB. On the other hand, a fast fault current interruption increases the voltage level of the arrester. The higher voltage level of the arrester, results in higher voltage requirements of the mechanical switch and the commutation path IGBTs. This also leads to a higher cost. [24]

3.9 Comparison of the CB Topology Performance

The CB topologies are compared in Table 3.1. From this table it can be seen that the solid state CB has the fastest interruption time, but the two different hybrid CBs are also quite fast. All of the CBs use insertion of a counteracting voltage to create a current zero crossing, except the active resonance CB who uses injection of current with opposite polarity. Thus all CBs, except the active resonance CB, have the ability for bidirectional current interruption. It is found that the resonant CBs

have a high voltage withstand and current carrying capability, but its interruption time makes it unsuitable for fault interruption in a VSC system. The solid state CB also has a high voltage withstand and current capability. For this CB the on-state losses are very high, with the present power electronic technology. With 30 % on-state power loss, the heat dissipation will be very high. The hybrid CB without the LCS in the main path needs an UFD to interrupt a fault at less than 5 ms. The UFD has a low withstand voltage, but a high current capability. The low voltage capability does not allow for application in the intended 320 kV HVDC grid. This leaves the hybrid CB with the LCS in the main path as the only CB option left. It has good withstand voltage and high current carrying capability. The expected interruption time of the hybrid CB with the LCS is within 2 ms. The on-state losses are higher than for the other CB using a mechanical opening switch due to the LCS. It is however expected to be less than 1 % on-state power loss. This leaves the hybrid CB with the LCS as the best possible CB for HVDC application.

3.10 Discussion

The fault propagation described in Figure 3.1 and 3.2 is only applicable for a 2-level VSC model, but can in some aspects be transferred to other VSC topologies. The stages will therefore occur in the same manner for all VSC systems, but differently for MMC systems. The reason for this are the internal capacitances in the submodules. The fault propagation for the different submodules might also be different, and has different reaction to the fault. Due to time limitations this has not been studied.

The methods for interrupting the fault current are quite different in operation and function. The current injection with opposite polarity is unidirectional, since it needs a pre-charged capacitor as a current source. The insertion of a counteracting voltage on the other hand allows for a bidirectional, and also a faster current interruption.

Current interruption by means of fault blocking in MMC is an interesting method. For a point-to-point connection this interrupting method is the simplest way. This way, no CB is necessary, and thus the costs may be reduced. In a MTDC operation, this blocking method is not desirable since it does not allow for seamless operation after a fault occurs. As previously mentioned the sudden loss of large loads or sources, may inflict problem on the AC side of the system. For a large MTDC network, it is not desirable to disconnect all the converters on the occasion of a fault.

There are several aspects to consider when choosing an HVDC CB. Firstly the converter system must be addressed, since it has big impact on the interruption time required by the CB. On one hand the CSC might be used for a point-to-point connection, and a three node MTDC. The CSC do not require a fast interruption, so the resonant CB might be used. In a VSC system however, the fault must be interrupted fast and thus the solid state and hybrid CBs are the only solution in terms of interruption time. Given the high on-state losses of the solid state CB, this topology is undesirable for high voltage applications. It is however possible to reduce the on-state losses with new power electronic technology. The same applies for the MMC converters. The hybrid CB is therefore the best possible CB topology for interrupting the fault current. The two hybrid CB models using different commutating methods, are quite different in operation and interrupting time. To commutate the current from the main path to the commutation path, the voltage drop across the main path must be higher than the commutation path voltage drop. In the A-HCB, the voltage drop is created by the LCS. The commutation path voltage drop might be in the range of a few kV, implying that the LCS must be able to withstand this drop. For the other hybrid breaker, the arc is the commutating medium. The arc is a chaotic and complex phenomenon, and will be further described in section 4.5. The arc voltage drop is small after the contact members separate, and will not significantly increase until the arc is being cooled by forced convection.

Table 3.1: Comparison of the different CBs [22, 23]

	Passive Resonant CB	**Active Resonance CB**	**Solid State CB**	**Active Hybrid CB**	**Passive Hybrid CB**
Expected interruption time	<60 ms	<30 ms	<1 ms	<2 ms	<5-30 ms
Interuption method	Counteracting voltage	Current injection	Counteracting voltage	Counteracting voltage	Counteracting voltage
Maximum voltage rating	$\leq$ 550 kV	$\leq$ 550 kV	$\leq$ 800 kV	$\leq$ 320 kV expected	$\leq$ 12 kV with UFD
Maximum interruption current	$\leq$ 4 kA	$\leq$ 8 kA	<5 kA expected	$\leq$ 16 kA expected	6-12 kA estimated
On-state losses	<0.001 %	<0.001 %	<30 %	<1 %	<0.001 %
Current interruption	Bidirectional	Unidirectional	Bidirectional	Bidirectional	Bidirectional
Expected cost	Relatively low	Relatively low	High	Very high	Very high
Prediction	Slow acting, not suitable for VSC HVDC systems	Slow acting anduniidirectional, not suitable for VSC HVDC systems	Fast acting, but the on-state losses are to high. Undesirable with present PE technology.	Fast acting, relatively low on-state losses. Expected to be very expencive.	Relatively fast acting, and low on-state losses. Untested, and low maximum voltage rating.

Chapter 4

Detailed Operation of the Hybrid CB

This chapter will go into detail on the operational principle of the two hybrid CB topologies considered in this report. It will also give a brief introduction to the hybrid CB topologies proposed by ABB and ALSTOM.

4.1 Operational Principle of the Passive Hybrid CB

To further illustrate the interruption process and times for each step of the way, a more detailed description is laid out. Before the fault is detected, and any actions are taken, the current will flow through the mechanical switch in the main path, shown in Figure 4.1. When the fault is detected, the IGBTs in the commutation path will immediately turn on, and prepare for commutation of the current. Simultaneously the mechanical switch will start to open, and create an arc burning between its electrodes. During this stage, the current will flow through both paths as illustrated by Figure 4.2. There will be a short delay from detection to reaction of less than 0.1 ms. As mentioned in section 3.8, there is a relation between the voltage drop over the main and commutation path, and the current in each path. The voltage drop across the arc will increase as the gap between the electrodes increases, almost linearly. The arc cooling is crucial for increasing the voltage drop, and the cooling time is dependent on the mechanical switch which is used. The fastest mechanical switch is the UFD, this actuator is to be more thoroughly explained in section 4.4.5. The UFD is fully opened at around 2 ms, and the cooling will have started already. Figure 4.3 shows the stage when the current is only conducted by the commutation path. When the current is fully commutated to the commutation path, there will be a short delay, allowing for the build-up of

the dielectric before the IGBTs turn off. As the commutation path IGBTs turns off, the voltage builds up across the CB until the arrester is turned on, and forces the current to a zero crossing, illustrated by Figure 4.4.

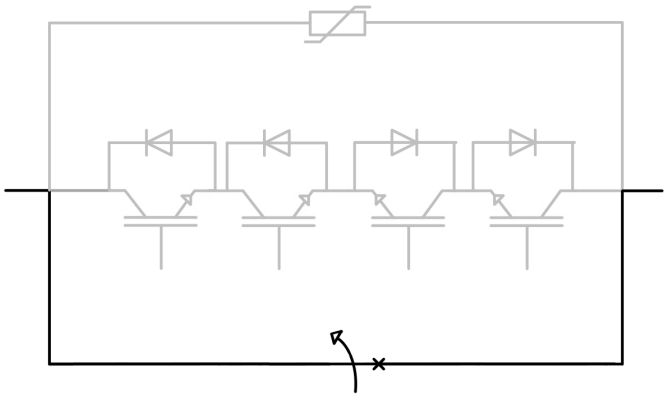


Figure 4.1: Stage 1 for hybrid CB without LCS

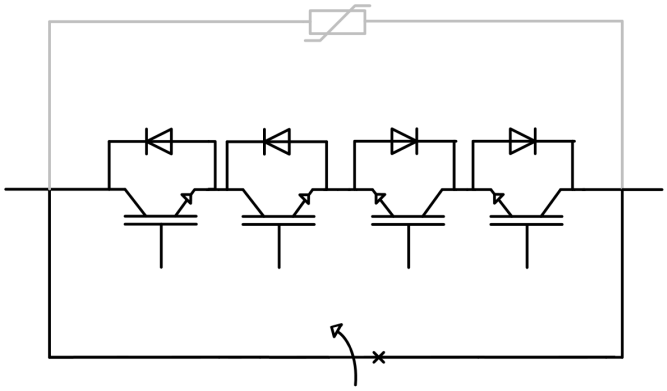


Figure 4.2: Stage 2 for hybrid CB without LCS

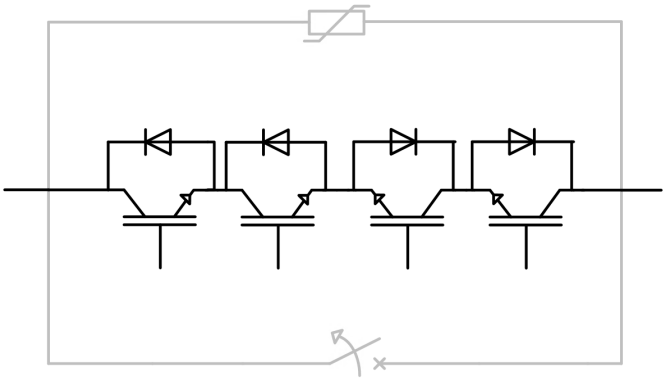


Figure 4.3: Stage 3 for hybrid CB without LCS

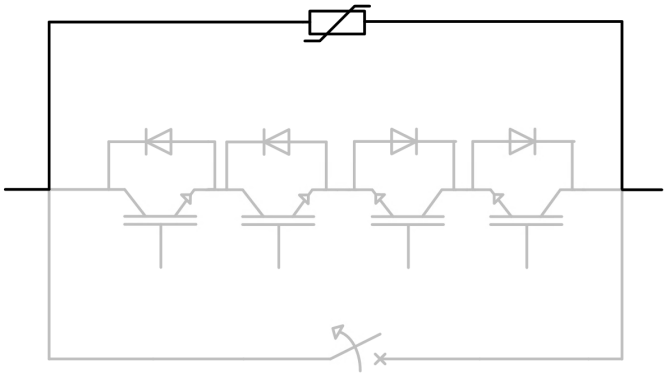


Figure 4.4: Stage 4 for hybrid CB without LCS

4.2 Operational Principle of the Active Hybrid CB

The best CB model available is A-HCB, this topology allows for a rapid interruption of the fault currents, and relatively low losses.

Before the fault occurs the current will only go through the mechanical switch and LCS, as illustrated in Figure 4.5. The conducting branch is highlighted. It takes some time before the fault is detected and the components react. The first reaction of the system is to close the parallel path IGBTs, and open the mechanical

switch. The IGBTs go from insulating stage to conducting stage in a few μs, while the mechanical switch will use in excess of 2 ms to fully open and gain a maximal dielectric strength. During the opening of the mechanical switch an arc will form across the contact members.

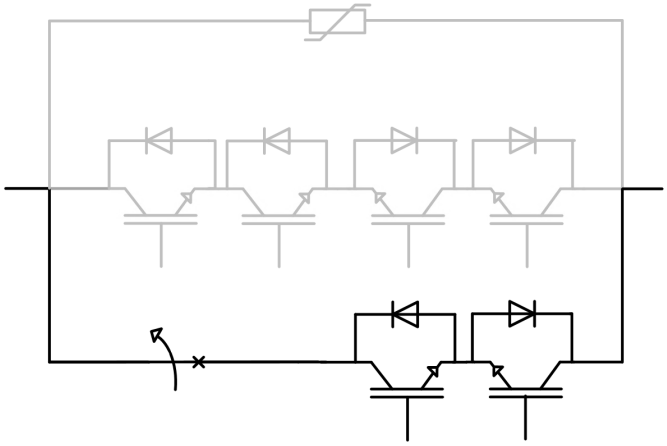


Figure 4.5: Nominal and pre-detection current path

When the mechanical switch has opened and the IGBTs in the parallel path have closed, the current will initially flow through the main path. The arc resistance across the contact members of the mechanical switch will increase, and as it does more of the current will flow through the IGBTs. This stage is illustrated in Figure 4.6. When the voltage drop across the mechanical switch is high enough, the LCS switch opens.

The full fault current is now being conducted through the commutation path IGBTs. There will be a high power loss across the main DC breaker, and cooling is required. This stage is illustrated in Figure 4.7.

When the mechanical switch is fully open and has gained maximum dielectric strength, there is a minimum chance of reignition of the arc, and the IGBTs in the main DC breaker can safely open. The voltage will immediately build up across the CB. The voltage rises until it reaches the turn on values of the arrester. The arrester will start to conduct the current and force it to a zero crossing. The last stage is illustrated in Figure 4.8.

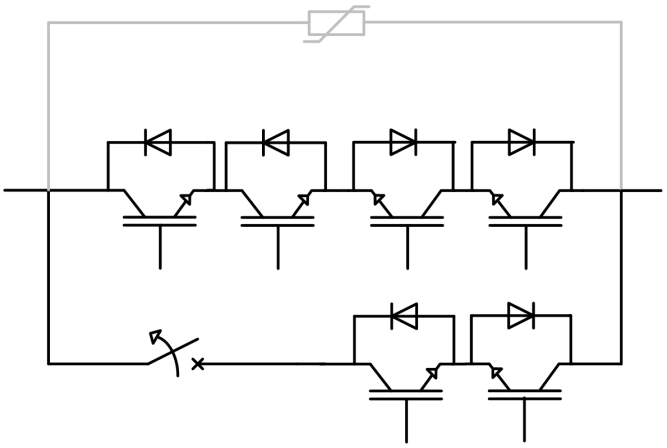


Figure 4.6: Current flow during stage 1

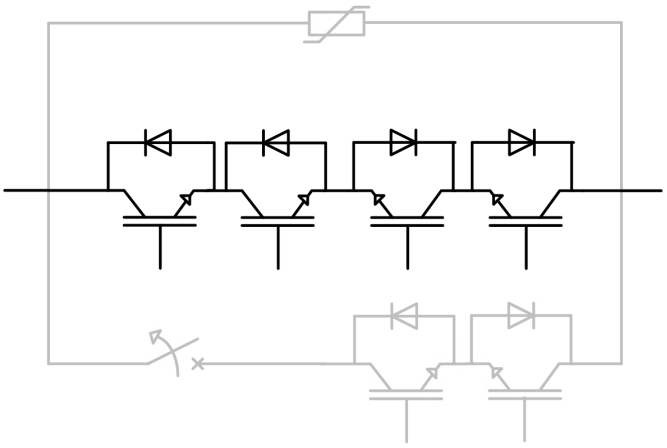


Figure 4.7: Current flow during stage 2

4.3 Manufacturers Active Hybrid CB Topologies

Until the writing moment, only two manufacturers have announced testing of a HVDC CB prototype. ABB were the first to announce it in 2011, and ALSTOM followed shortly after.

ABB's Solution

When the fault occurs, the LCS opens at the same time as the ultra-fast disconnecter does. The current is then commutated to the main breaker path. The

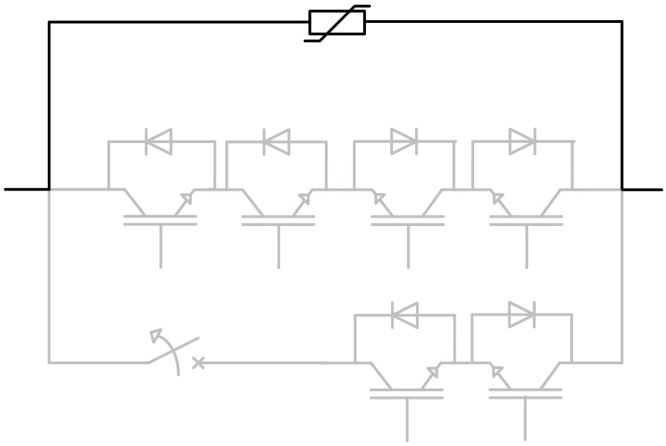


Figure 4.8: Current flow during stage 3

main path is conducting the fault current until the ultra-fast disconnecter is fully opened. The IGBTs in the main breaker will then turn off, causing the voltage across it to rise. When the voltage is within the range of the arrester it will start operating, and force the current to a zero crossing. ABB's solution of the hybrid CB can be seen in Figure 4.9. The residual current disconnecting CB is a necessary component. Its purpose is to disconnect after fault clearance and interrupt the residual currents and fully isolate the cable, and also to protect the arrestor banks for thermal overload. The main DC breaker, as the commutation path and absorber path is named by ABB, is divided into several modules with their own arrest. They have the possibility for different turn-off time and size of the arrester.

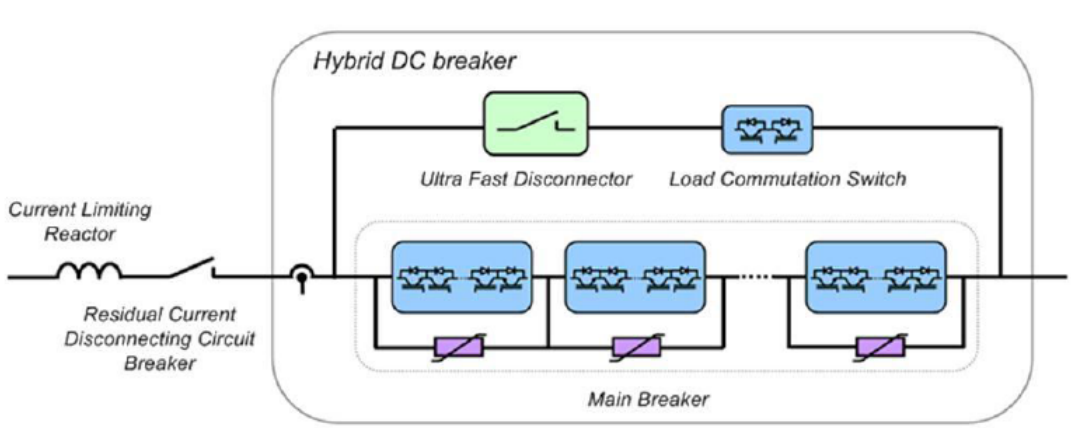


Figure 4.9: ABB A-HCB topology [25]

The maximum fault current the breaker is able to interrupt is 8.5 kA, due to the limitations on the semiconducting devices. The fault current in this test, is interrupted within 2 ms. With the next generation power electronic devices it is expected that the maximum interruptible fault current will rise to 16 kA. The maximum system voltage achieved is 320 kV, but though with a fault current of 2.6 kA.

ALSTOM's Solution

The Hybrid CB proposed by ALSTOM is quite similar to ABB's solution. They both have a small power electronic part in series with the switch, a larger power electronic part in the commutation path and an arrester, as showned in Figure 4.10a. However, there are some difference in the commutation path, as ALSTOM does not use IGBTs in antiparallel with diodes, but instead uses thyristors in series, with a large capacitor in parallel with an arrester at the end of each thyristor strands. When the capacitor is fully charged it will discharge into the arrester, and thus creating a higher voltage at the cathode than the anode, and forcing the thyristor to turn off. [26]

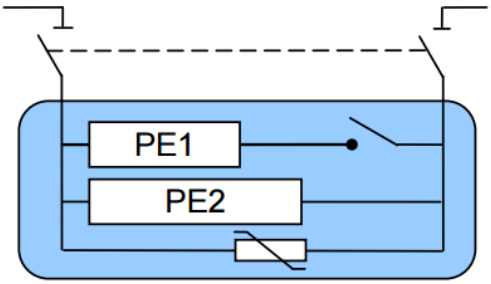
Figure 4.10b shows a more detailed description of ALSTOMs hybrid CB topology. The figure is not completely accurate since it does not contain the back-to-back thyristors, and is thus not unidirectional, the full model is illustrated in [21, 27].

When a fault occurs, the IGBTs in the nominal path turn off, and commutate the current into the auxiliary branch (commutation path). The auxiliary branch carries the fault current with a low impedance, until the ultra-fast mechanical switch is fully open. When the ultra-fast mechanical switch is fully open, the auxiliary path increases the impedance until the voltage across it is high enough for the arrester to react. As explained earlier the arrester forces the current to a zero crossing. [19, 27]

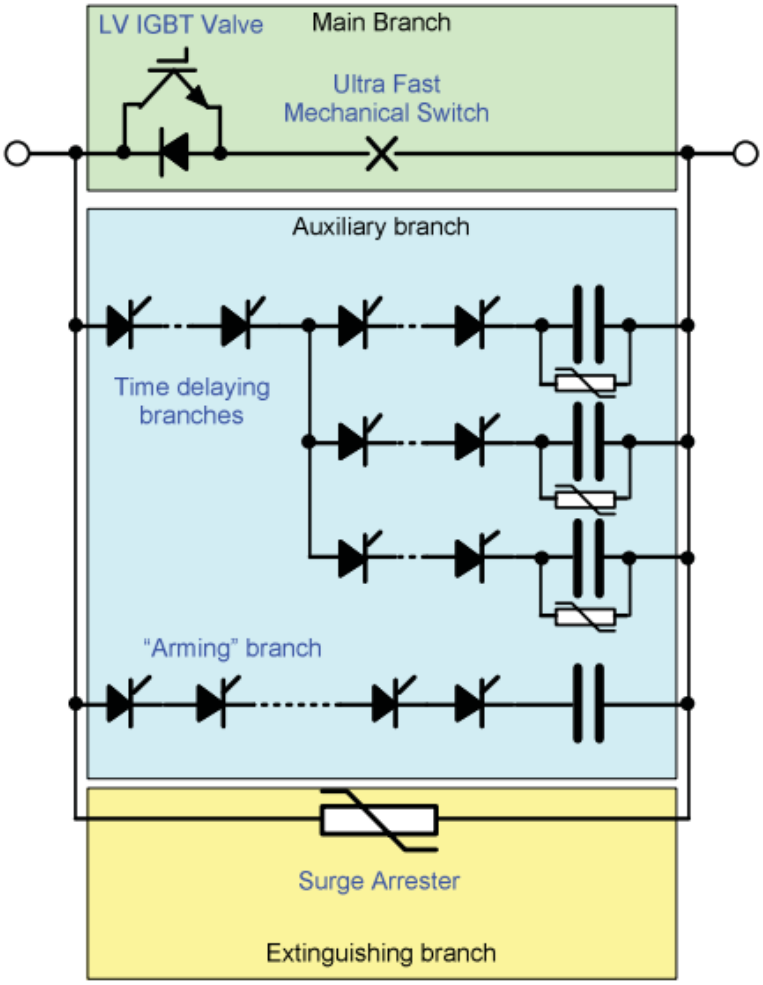
A various test of ALSTOM's hybrid CB have been conducted. Until the writing moment the highest fault current broken is 5.2 kA, it was interrupted in 5.2 ms. With a fault current of 3 kA it is possible to break the current within 2.5 ms. [21, 27, 28]

Comparison

In Table 4.1, ABB and ALSTOM's solution for the hybrid CB are compared. As can be seen, ABB has the shortest interruption time, the highest voltage and



(a) Simple schematic [27]



(b) A more detailed description [21]

Figure 4.10: ALSTOMs hybrid CB topology

current ratings. The hybrid CB is yet not commercial available, but will probably be within a few years. The cost of the hybrid CB is expected to be quite high, and be in the same range as the VSC converter. The on-state losses for the manufacturers hybrid CB topology is not mentioned in any public reports, but it is expected to be less than 1 %, as mentioned in Table 4.1.

Table 4.1: Comparison of the manufacturers Hybrid CB topologies [25, 27, 28]

	ABB's A-HCB	ALSTOM's A-HCB
Interruption time	<2 ms	5.2 ms for 5.2 kA <2.5 ms for 3 kA
Voltage rating	320 kV proven with low current	120 kV
Highest interruption current	8.5 kA Expected to rise to 16 kA	5.2 kA Expected 7.5 kA

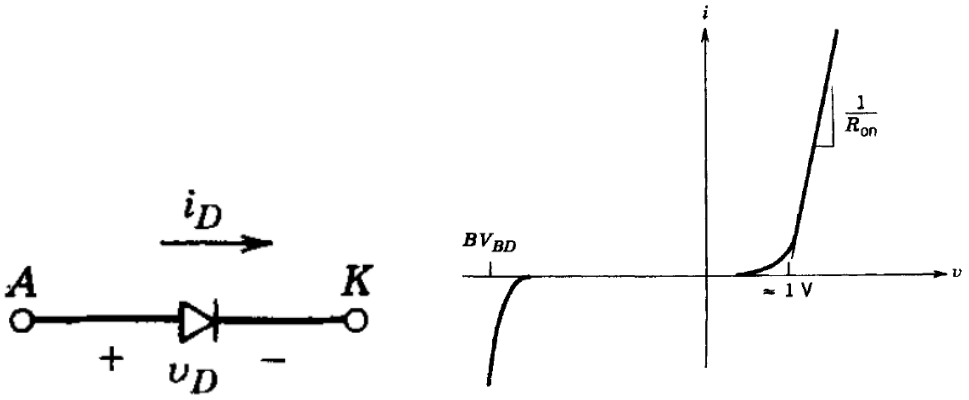
4.4 Components in the Hybrid CB

To understand the behaviour of the components in the hybrid CB, each component must be investigated.

4.4.1 Diode

The diode is a power electronic switch entirely controlled by the circuit. When the voltage across the diode V_D is positive, the diode is on and forward biased. When V_D is negative, the diode is off, and reversed biased. The diode only needs a small forward voltage across it to start conducting (around 1 V). In reverse bias, the diode will have a very small leakage current flowing through it, until the reverse breakdown voltage is reached. It is critical that the reverse breakdown voltage is not reached, for the safety of the diode. Figure 4.11a shows the symbol for the diode, and its forward direction. Figure 4.11b shows the i-v characteristic of the diode, how it turns on at 1 V, and conducts more at a higher voltage, dependent on the on-state resistance R_{on}. BV_{BD} is the reverse breakdown strength of the voltage. In reverse bias, there will be a small leakage current, but it will increase drastically when the reverse breakdown voltage is reached. [29]

The turn-on of the diode is close to an ideal switch, this is not the case for turn-off. When the diode turns off, its current reverses for a reverse-recovery time



(a) Symbol of the diode (b) I-V characteristic of the diode

Figure 4.11: Diode, and its characteristics [29]

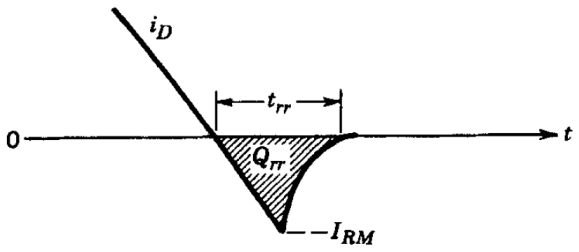


Figure 4.12: Diode turn off [29]

t_{rr}, as illustrated in Figure 4.12. In order to block the negative polarity voltage, the reverse-recovery current must sweep out the excess carriers in the diode [29].

The high power semiconductors, are more complex than the low power counterparts, even for diodes. The n^- region is often called the drift region, and is not found in the low power diodes. The drift region's function is to "absorb the depletion layer of the reverse-biased p^+n^- junction." [29]. The on-state resistance and reverse breakdown voltage of the diode is directly related to the size of the n^- layer.

The power diode has a low on-state resistance, and is therefore often desired before the thyristor and Gate Turn-Off Thyristor (GTO). The diode is only controlled by the circuit behaviour, and might be undesired if on- or off-state must be controlled.

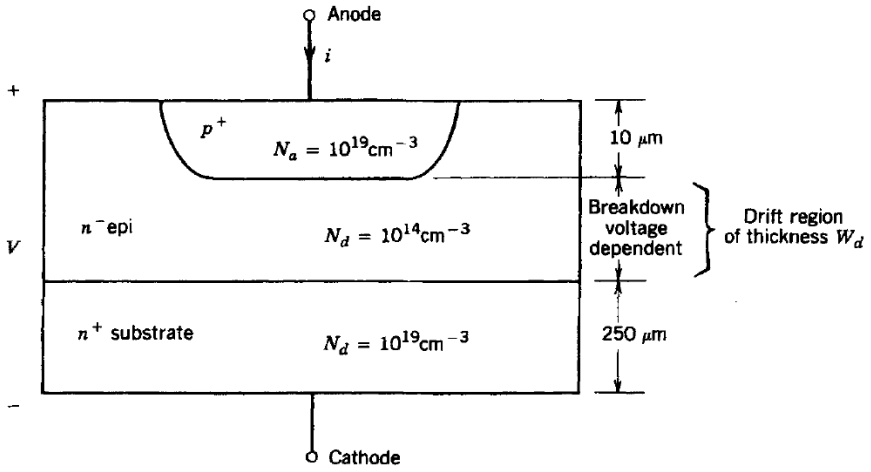


Figure 4.13: Cross-sectional view of a power diode [29]

4.4.2 The Power Electronic Switch

There are several components that can be controlled in both turn-on and turn-off operation. An analysis of the different power electronic components should be conducted in able to choose the switch with the best properties for current interruption. The power electronic switch in a hybrid CB must be controllable and fast acting. It needs to have low on-state resistance and switching losses. The switch should also be able to carry large currents, and withstand high voltages in forward and reverse bias.

There are several power electronic switches available, that have good controllability. The BJT, MOSFET, JFET, thyristor, GTO and IGBT are some of the most common power electronic switches

Starting with the BJT, it is current controlled and requires thus a high base-current to conduct the current. This gives the BJT a poor efficiency, and the BJT is not suitable for the hybrid CB. [30]

The MOSFET is easily controlled and has a very high switching speed. The MOSFET can carry large currents and withstand large voltages, but however it is a very expensive technology, and costs must be kept at a minimum. [30]

The JFET is also easily controlled, like the MOSFET. The JFET have very low current carrying capability, and for this component to be able to carry several kA, it will require hundreds of parallel branches. For hybrid CB the JFET is not

suitable. [30]

The thyristor has high current and voltage ratings, but lacks turn-off capability. The turn-off capability is an essential part of the hybrid CB, and the thyristor is not suitable for DC current interruption. [30]

The GTO is a thyristor with turn-off capability and a low on-state voltage drop. But like the BJT, the GTO uses current signals for switching and is thus more suitable for low switching frequencies application. [30]

The IGBT has high current and voltage ratings, and is relatively cheap. The downside of the IGBT is the slow switching speed. It is however considered the best power electronic switch for use in the hybrid CB. [30]

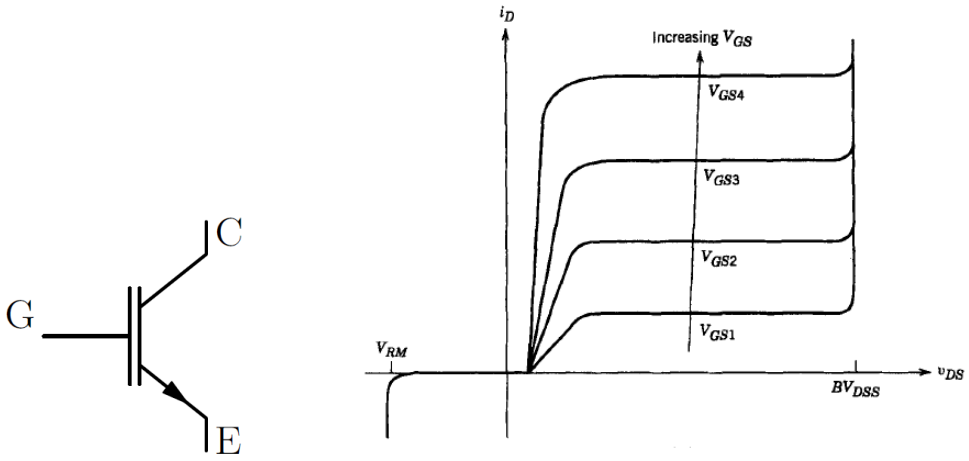
IGBT

The IGBT is a power electronic switch able to conduct large currents, and withstand high voltages. It is a bipolar switch, built up by BJT and MOSFET. The IGBT is easily controlled by voltage pulses at the gate (G) as illustrated in figure 4.14a. Due to high modulation space carriers, the switching speed of the IGBT is quite slow, but it might be increased by increasing the gate current [29, 30]. To turn on the IGBT a minimum forward voltage drop of 0.7 V is required [31]. When there is a forward voltage drop, a positive gate emitter voltage must be applied to turn on the IGBT. In figure 4.14a the collector (C) and emitter (E) is the input and output of the current.

Figure 4.14b illustrates the i-v characteristic of the IGBT. It can be seen that a minimum voltage is required for on-state conduction, and that the applied voltage from the gate to the emitter is determining the collector current in the IGBT.

In Figure 4.15 the structure of the IGBT is illustrated. In the figure, the BJT and MOSFET parts are also illustrated. Like the power diode, the n^- layer is the drift region.

In hybrid CB operation, the turn-on is not that relevant, but the turn-off is. Figure 4.16 shows the transient waveforms of the IGBT current and voltage. Since there are two parts in the IGBT structure, there will be two different parts in the turn-off waveform. First the voltage from the gate to the emitter will drop, until the collector to emitter voltage starts to increase. When the collector voltage is reached, the collector current will decrease. This is the MOSFET current. As the current decreases, so does the gate to emitter voltage. When this voltage reaches



(a) IGBT [30] (b) Output characteristics for an IGBT [29]

Figure 4.14: IGBT symbol, and i-v characteristics

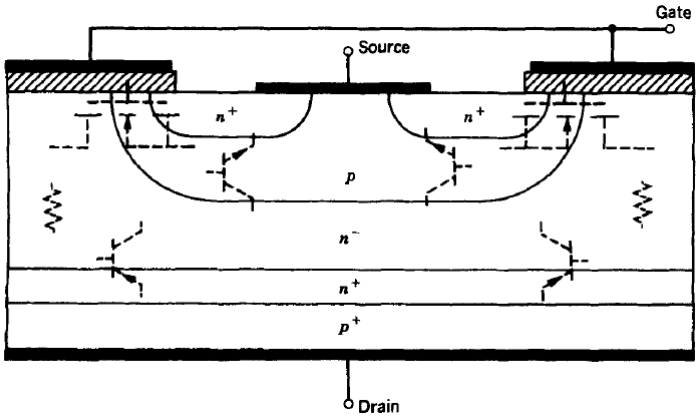


Figure 4.15: IGBT structure, with the different parts of the components [29]

the threshold voltage for conducting, set to be 0.7 V, the current will decrease slower. The slowest decreasing slope of the collector current is the BJT region. When the gate emitter voltage goes below zero, the IGBT is in off-state.

The IGBT is a rugged device, and does not require a snubber circuit for many different operations. For hybrid CB current interruption, the stray inductances may cause high transient currents that might be problematic for the IGBT. [31]

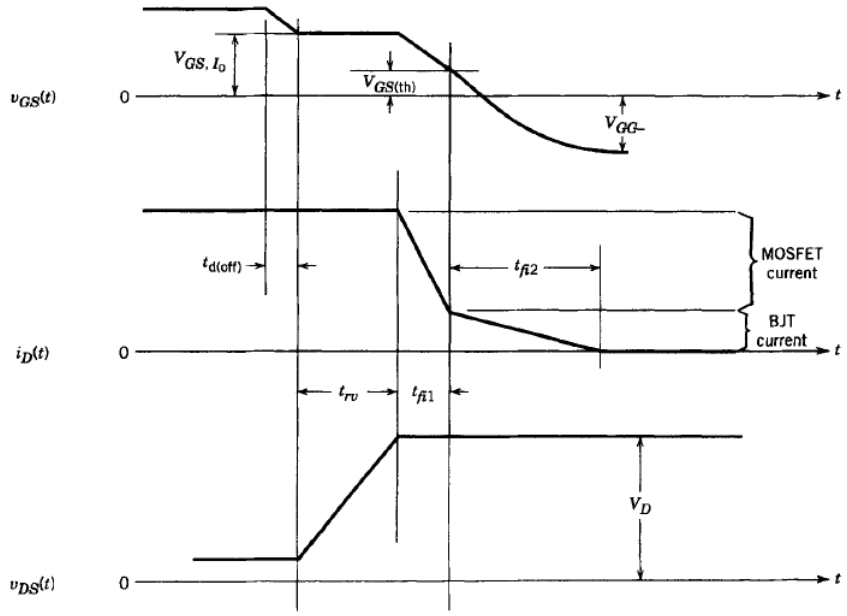


Figure 4.16: IGBT turn-off waveform [29]

4.4.3 Snubber Circuit

The snubber circuit is a parallel connected circuit to the power electronic switch, designed to relief the semiconducting device from the stresses that may occur during turn-on or -off. This is needed due to the very fast switching time of the semiconductors. In a high voltage and current system, there might be transients oscillating between the capacitive and inductive elements in the circuit. The snubber circuit reduces these transients by slowing down the switching time.

In a HVDC CB the inductive elements causing problems are the stray inductances, since only a small inductance might significantly increase the voltage across the semiconducting device. This is illustrated by equation (4.1), derived from Figure 4.17.

The stray inductance is undesired and must be reduced. It can be reduced by making the distance between the components in each branch as small as possible. However, the arrester and power electronics should be placed in a certain distance from each other, since the arrester will heat up quite much when it is conducting the current. It is undesired that the power electronics are heated-up more than necessary since it might affect their operation.

$$U_{semiconductor} = U_{MOA} + L_{stray}\frac{di_{MOV}}{dt} \tag{4.1}$$

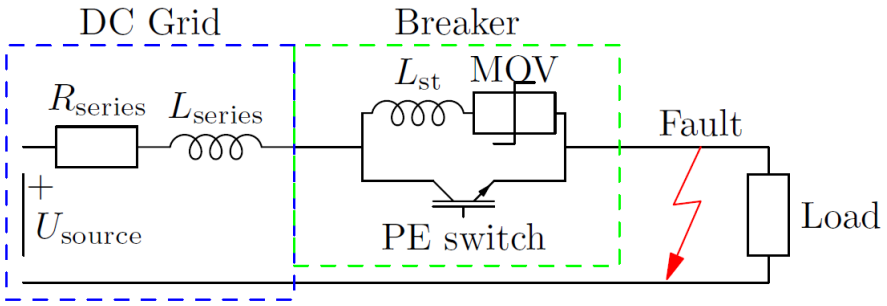


Figure 4.17: Schematic diagram of a DC fault, and interruption [30]

For a HVDC CB, it is only necessary with a turn-off snubber, since it is only in the turn-off switching event the semiconducting device truly is put to the test. A snubber circuit might help to increase the safe operating area of the power electronic, and might also reduce its switching losses. It is desirable to switch the semiconductors as fast as possible to avoid high over-voltages. Due to the parallel energy absorbing unit, the Metal Oxide Arrester (MOA) (called Metal Oxide Varistor (MOV) in Figure 4.17), there is no margin for transient over-voltages during the switching.

In a HVDC CB, the power electronic switch will only force the current into a parallel energy absorber branch. It is important to have control of the stray inductances, since each microhenry stray inductance may result in one kilovolt increased over-voltage, for high power application where several kiloampere is switched in matters of a few microseconds.[30]

Figure 4.18 shows the effect of no snubber circuits for an experimental set-up. To improve the turning of transient voltage, different snubber circuit should be compared.

Snubber Circuit Solutions

There are different kind of snubber circuits, depending on the operation of the power electronic device. The snubber circuit is added to protect the power electronic switch or reduce losses across it during switching operations. [30]

- Gate resistance

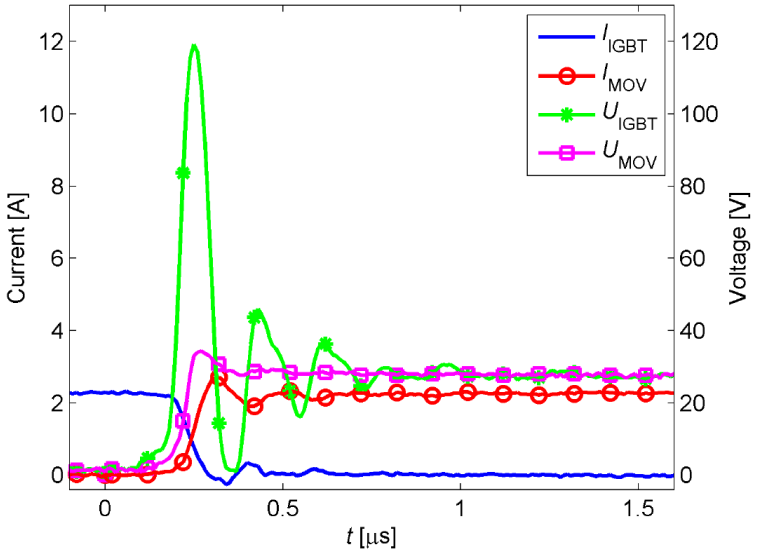


Figure 4.18: Low voltage eperimental set-up, illustrating the transient over-voltage across the IGBT due to stray inductance [30]

- C-snubber
- RCD-snubber
- MOA snubber

4.4.4 Arrester

An arrester is a non-linear resistance used for protection of vital components in the power system. It consists of metal oxide disks in a series connection. The most common metal oxide used in the arrester is Zinc Oxide (ZnO). The arrester is basically a semiconductor, and acts very fast. Each metal oxide disk consists of several million grains, as illustrated by Figure 4.19. Each grain is highly conductive by itself, but the junction between the grain is a voltage dependent semiconductor. At high voltages, it will be conductive. [17, 32]

The ZnO grains are about 10 μm in diameter and have a very low resistivity. Each grain is surrounded by a granular layer. The granular layer have a thickness of about 0.1 μm, and has a high resistivity during normal conditions. The resistivity of the granular layer is depending upon the field strength across it, and it may vary from $10^8 \Omega m$ for low electric field stress, to below $0.01 \Omega m$ for high stress. [32, 33]

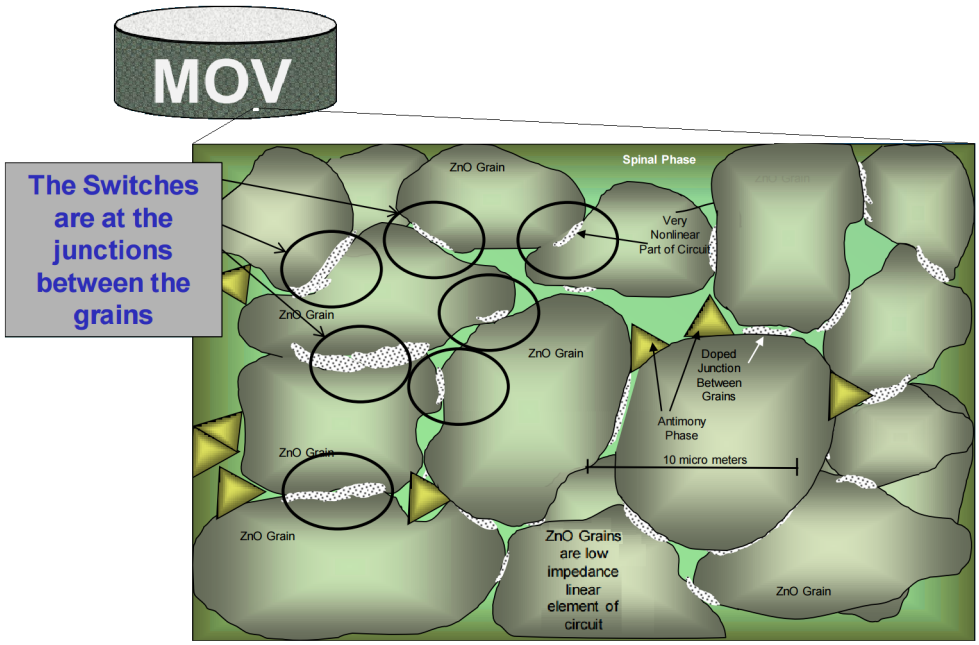


Figure 4.19: Arrester disk and the grains within it [32]

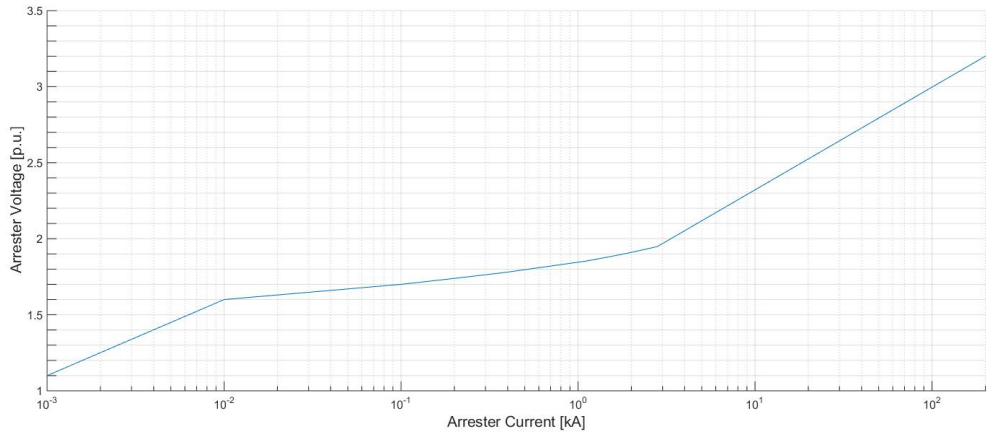


Figure 4.20: V-I characteristic of the arrester used in the simulations to come

A typical v-i characteristic of an arrester is illustrated in Figure 4.20. This characteristic of the arrester is used for the simulation models in chapter 5.

The characteristic of the resistive part of the arrester can be divided into three regions as described by [33, 34]:

1. Low Electric field region

   - The grains of the ZnO have an granular energy barrier around it. This barrier is insulating, and prevents the flow of electrons from one grain to another. If an electric field is applied across the arrester, the granular barrier allows electrons to pass over them thermally, also called Schottky emission. As the field across the arrester increases, the more electrons are allowed to pass through the barriers. The current density is approximately given by equation (4.2). J_0 is a constant depending on the granular layers geometry and material, Φ_B is the barrier potential, E is the electric field stress, e is the electron charge, ϵ is the dielectric constant, k is the Boltzmann's constant and T is the absolute temperature. Increasing the temperature allows more electrons to pass over the granular barrier, and with more energy. [33]

$$J_r = J_0\, exp\left(\frac{\sqrt{\frac{Ee^3}{4\pi\epsilon}} - \Phi_B}{kT}\right) \tag{4.2}$$

2. Medium electric field region

   - "When the electric field in the granular layer reaches about 100 kV/mm, electrons move through the barriers by the tunnel effect, represented by equation (4.3), where J_1 and A are material constants" [33].

$$J_r = J_1\, exp\left(-\frac{A\Phi_B^{3/2}}{E}\right) \tag{4.3}$$

3. High electric field region

   - "In this region, the voltage droop at the barrier due to the tunnel effect is small and the voltage drop across the resistance R_z of the ZnO grains dominates. The current then gradually approaches the linear relation with the voltage, described by equation (4.4)." [33]

$$J_r = \frac{E}{\rho} \tag{4.4}$$

4.4.5 Ultra-Fast Disconnecter

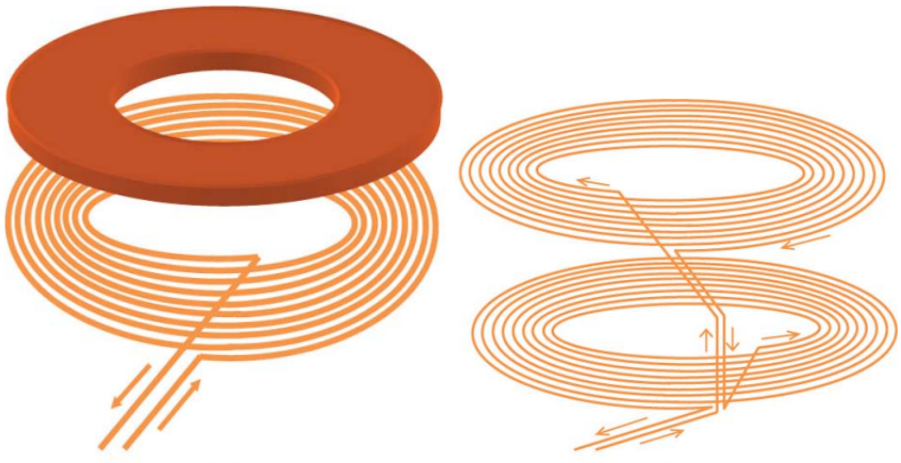
This section is taken from [8]. As mentioned in section 3.1.1 the fault current has a very short rise time, and must thus be interrupted within a few milliseconds. There is no conventional actuator fast enough, to handle the DC faults within the

time requirements. An actuator concept has been proposed, to obtain the desired disconnecting time, involving the use of a Thompson coil. The Thompson coil uses electromagnetic repulsion to separate the contacts [30]. Two ways of separation are considered; Single sided Thompson coil (Figure 4.21a), and double sided Thompson coil (Figure 4.21b).

The Thompson coil is connected to an AC charged capacitor. When the fault occurs, the capacitor discharges into the coil(s) as a current pulse. This gives a fast increase in magnetic flux.

The single sided Thompson coil produces a magnetic field, that induces mirrored eddy currents in the disk. These eddy currents, then again produce an opposing magnetic field and thus an electromagnetic repulsion. On the other hand the double sided Thompson coil works in a different manner, with two coils connected together. The currents in the coils flow in opposite directions, thus creating opposing magnetic fields and a repulsion. One of the coils is connected to the disk, forcing the disk to accelerate in the direction of the magnetic field. The two coils are connected through brushes. [30, 35, 36]

Since the coils in the double sided Thompson coil are connected through brushes, this concept requires far more maintenance than the single sided [35].



(a) Single sided Thompson coil (b) Double sided Thompson coil

Figure 4.21: Sketches of the Thompson coils [35]

The physical aspect of the Thompson coil can be explained by Lenz's law shown in equation 4.5, where ε is the induced voltage and $\partial\Phi$ is the change in magnetic flux.

$$\varepsilon = -\frac{\partial \Phi}{\partial t} \tag{4.5}$$

The change in the magnetic flux has a different sign than the induced voltage. Lenz's law states that whenever a change in a magnetic field occurs, and electric field is generated to oppose the change [37].

To create a change in a magnetic field an AC current pulse must be exerted into the coil(s). To create a high enough change in the magnetic field, a capacitor is connected to the coil with a switch. In normal operation the switch is open, and when the fault occurs, the switch closes. The switch must be a semiconductor, in able to react quickly enough. [38]

Figure 4.22 illustrates the theory of the Thompson coil. The coil produces a magnetic field, that can be decomposed into two components, a z and r component. The r component is the radial component working on the x and y plane on the disk.

The coil creates a magnetic field, the magnetic field induces eddy current in the disk. The mirrored eddy currents then creates an opposing magnetic field, thus causing the disk to accelerate away from the Thompson coil.

The coil produces a radial flux, who induces the current in the disk, as shown in Figure 4.22. The flux density B_r is shown in equation (4.6).

$$B_r = \vec{B_r} sin(\omega t) \tag{4.6}$$

The radial magnetic flux induces mirrored eddy currents in the disk. These eddy currents then again creates an opposing magnetic field to the field created in the z-direction by the Thompson coil. The force created is then showed in equation (4.7). F_z is the force created by the repulsion between the coil and the disk, in z direction.

$$F_z = i_\phi B_r \tag{4.7}$$

$F_z = F_{total}$ for the single sided Thompson coil. The total acceleration of the disk is found from equation (4.8), where F_{total} is the total force on the disk, m is the mass of the disk of which the force is exerted on. The acceleration of the disk is labelled a.

$$F_{Total} = ma \tag{4.8}$$

Figure 4.23 is one of the first fast acting breaker models. In the illustrated figure, the current flows from left to right as illustrated in the disconnecter in closed

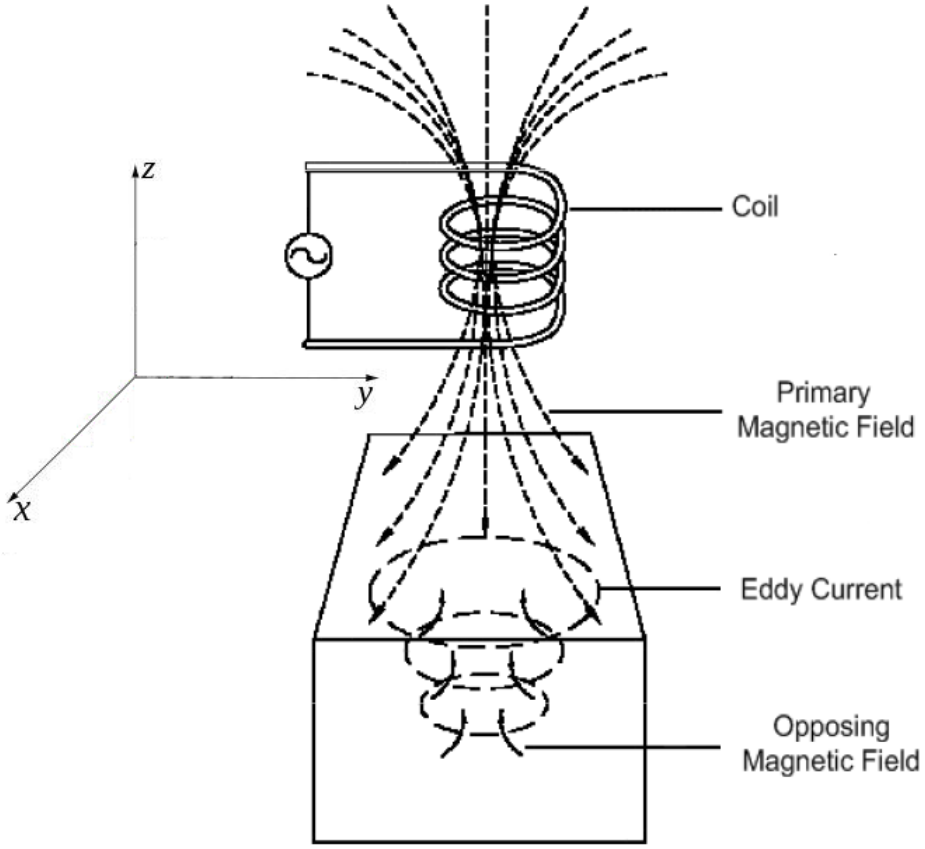
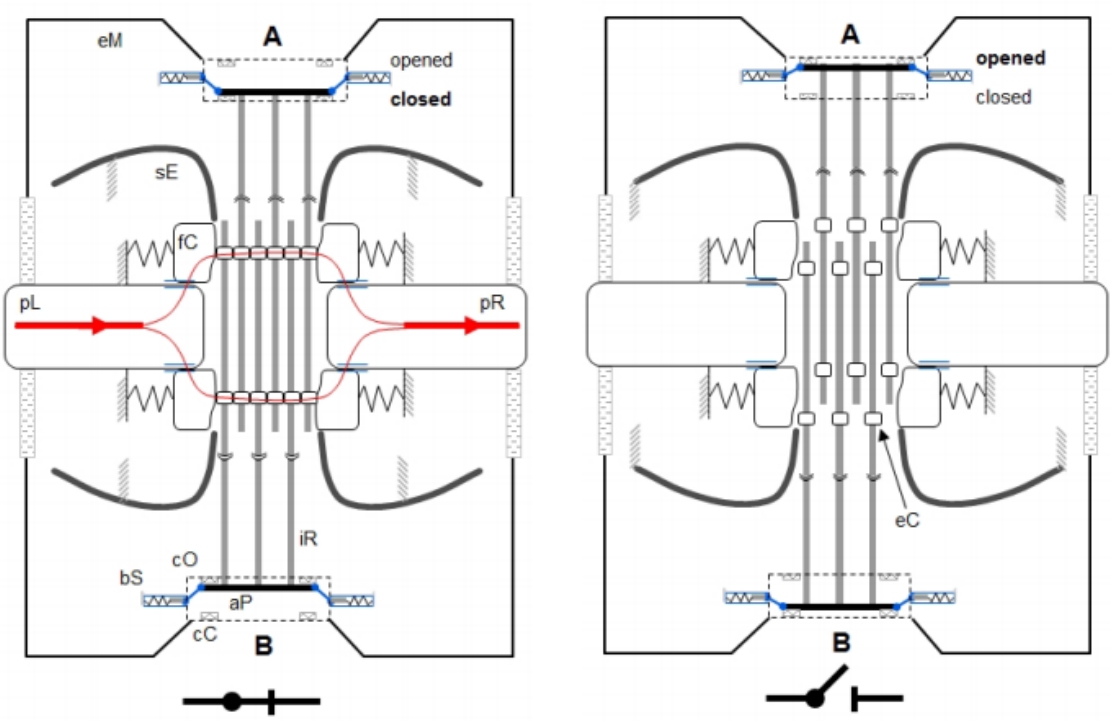


Figure 4.22: Thompson coil on a metallic disk [39]

operating mode. For detailed information about the components see [36]. When the fault occurs, the capacitor connected to the Thompson coil discharges (cO), causing the disc (aP) to move away from the Thompson coil. The moving contact members (eC) are then separated and an arc is formed between them until the current is forced to zero by the arrester.

The Ultra-fast disconnecter is an essential component in able to disconnect the faulted circuit before it rises to critical levels. CBs on the AC side, are slow acting, and use tens of milliseconds to disconnect the fault. On DC application the fault must be disconnected within a few milliseconds. In able to do so, the Thompson coil must be used.



(a) Closed (b) Open

Figure 4.23: Ultra fast disconnecting switch [36]

4.4.6 Current Limiting Reactor

The low impedance of the DC cable system, causes higher fault currents when a DC side fault occurs. The Current Limiting Reactor (CLR) is installed to limit the fast transient fault currents to occur.

It is described in [40] that CLRs are necessary in order for the hybrid CB to interrupt the fault current without damaging the components. The inductor decide the rate of current rise ($\frac{di}{dt}$), and is the only adjustable parameter when the interruption time is set. The current limiting reactor should be as small as allowed for interruption of the fault current since there are large costs affiliated with a reactor, and a high inductance might affect the stability of the system. [40]

Fault current limiter

The fault current limiter is connected with a back-to-back GTO, which conducts the nominal current. In parallel an inductor and an arrestor are connected, as illustrated in Figure 4.24. When the fault occurs the GTO turns off, and the current through the fault limiting inductor builds up slowly. In the commutation

process from the GTO to the limiting inductor, a large $L(\frac{di}{dt})$ develops across the switch, causing a high voltage spike to be absorbed by the parallel arrester [41, 42]

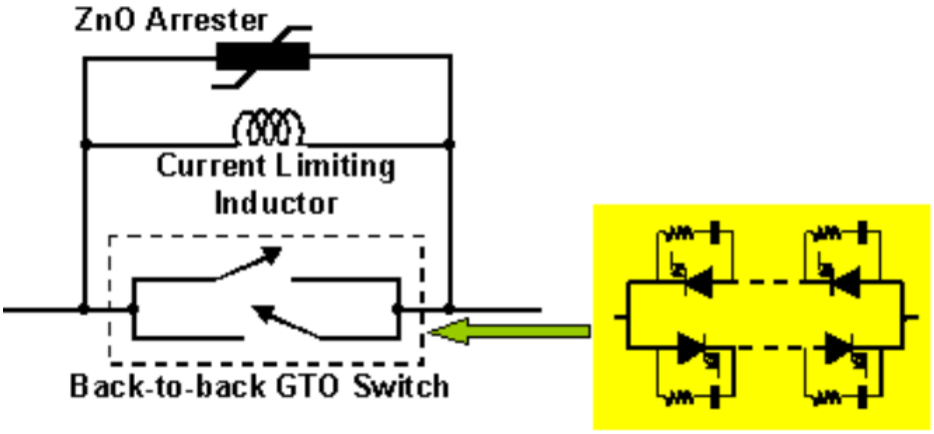


Figure 4.24: Fault current limiter [41]

4.5 The Electric Arc

In a mechanical CB without another commutating mechanism, the arc must commutate it. The arc must create a sufficient voltage drop across it, so that it will increase the on-state voltage drop across the commutating path.

When the contacts of an energized system separates, the gas between them will heat up to such high temperatures that the molecules decomposes. The mixture of free electrons, positive and negative charged ions is called a plasma, and is the key ingredient if the arc. The arc is the conducting medium between the contact members. When the arc has a high temperature, the conductance of it will be high, and only require a small voltage drop. If the temperature decreases significantly the molecules will reform and the conductance will decrease and thus the voltage drop will increase significantly. The arc conductance is temperature dependent. To successfully interrupt a fault current, the arc must be cooled. The first step of doing this is by increasing the gap between the contacts. This is not enough, and another cooling mechanism is needed. There are several ways to cool the arc, but this report only considers a forced cooling. [18, 43]

The electric arc is a discharge phenomenon with a low voltage drop, which behaves like a non-linear resistance. The arc itself has a small voltage drop, and may conduct large currents. Figure 4.25 shows an equivalent model for calculating

the arc voltage, V_{arc}. V_{DC} is the DC system voltage, R is the line resistance, and L is the line inductance. When the mechanical switch (MCB) opens, an arc forms between the contacts. The arc voltage is described by equation (4.9). [43]

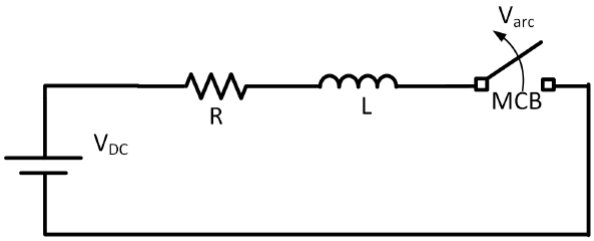


Figure 4.25: DC system equivalent and it relation to the electric arc [43]

$$V_{arc} = (V_{DC} - Ri) - L\frac{di}{dt} \tag{4.9}$$

4.5.1 Arc Characteristics

The arc characteristic is distinguished by static and dynamic arcs. The dynamic arc characteristic describes the arc for rapidly changing currents and is therefore mainly used for the AC system. The static arc is often used to describe the DC arc propagation. [18]

A general v-i characteristic of a freely burning static arc is illustrated in Figure 4.26. From the figure it can be seen that for high currents, the voltage drop across the arc is quite small. When there is a small current flow through the arc, the voltage drop will be higher. [18]

Figure 4.27 shows the three different arc regions, known as the anode, cathode and arc column region. The different regions have a different voltage drop, but within each region the voltage drop is constant. [44]

The arc current in the P-HCB changes rapidly and the dynamic arc characteristic is considered as the best description of the DC arc.

4.5.2 Arcing Model

The electric arc is a complex phenomenon, and is difficult to express mathematically. Since the arc may behave differently from each time it is formed, the models are only an approximation to the arc behaviour. But the models are sufficient for

Figure 4.26: Static arc voltage current characteristic [43]

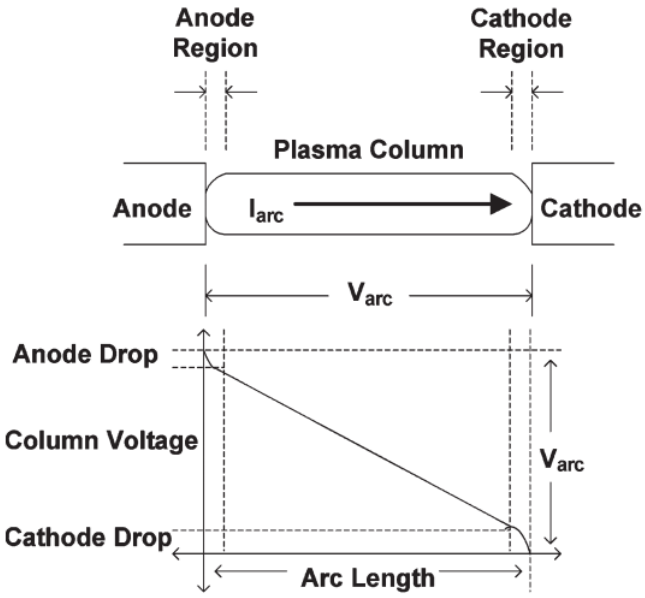


Figure 4.27: General characteristics of an electric arc [44]

determining the current flow in the HVDC CB.

In Table 4.2 some of the most important mathematical models are listed. The first model was derived by Ayrton in 1902. The oldest models describes the arc behaviour only during certain conditions, and are thus not generally applicable for other cases. Later models are often built upon the Cassie and Mayr equations.

The Cassie and Mayr equations developed in around 1940 describe the arc

Table 4.2: Most of the arcing models developed

Arc models	
Ayrton	1902
Steinmetz	1906
Nottingham	1923
Van and Warrington	1931
Cassie	1939
Mayr	1943
Miller and Hildebrand	1972
Hall, Myers and Vilicheck	1978
Stokes and Oppenlander	1991
Paukert	1993
Sölver	2006

quite good. The models are often used in combination since they describe the arc for different currents. "Cassie assumed that the arc has a fixed temperature being cooled by a forced convection. This implies that the cross-section area of the arc is proportional to the current and that the voltage over the arc is constant. Cassie arc model is suitable for arcs with high currents" [45]. "Mayr assumed that power losses are caused by thermal conduction and the arc conductance is dependent on temperature.The cross-section area of the arc is assumed constant. Mayr arc model is fit for currents near zero" [45]. Several models are based on the Cassie-Mayr equation. [46]

The equations are derived from the energy balance equation, seen in equation (4.10).[22] This equation gives the imbalance of the power loss due to heating of the arc and the cooling power on the arc. This imbalance describes the rate of change of the arcs energy.

In this thesis, a modified version of the Mayr equation is used, known as the Mayr-Schwarz equation. The energy balance equation, seen in equation (4.10)is a simplification of the Cassie and Mayr equation. Where Q is the stored energy in the arc, resulted by an imbalance between the ohmic heating P_{heat} and cooling P_{cool}. [23]

$$\frac{dQ}{dt} = P_{heat} - P_{cool} \tag{4.10}$$

From this equation a modification can be made to make it possible to implement it in PSCAD. Equation (4.11) shows this equation that can be implemented in PSCAD. Where g is the arc conductance, τ_{arc} is the arc time constant, i is the arc

current and P is the cooling power on the arc. [22].

$$g = \int_0^t \frac{1}{\tau_{arc}(g)} \left(\frac{i^2}{P(g)} - g \right) dt' \tag{4.11}$$

The arc parameters described above are calculated like it is illustrated in equation (4.12) and (4.13). Where P_0 and τ_0 is the constant cooling factor, and the constant arc time constant. a and b are variable parameters.

$$P(g) = P_0 \cdot g^a \tag{4.12}$$

$$\tau_{arc}(g) = \tau_0 \cdot g^b \tag{4.13}$$

4.6 Discussion

For the hybrid CB there might be possible with different stages of increasing the on-state voltage drop across the commutation path. This is a method used by ALSTOM in there hybrid CB solution. This is not further investigated in this report, but should be considered in more detailed studies.

The different interruption time used to describe the hybrid CBs with are more or less ideal. Meaning they are the interruption times derived from several reports as the future expected operation time. The biggest uncertainty is the UFD, as it is still in the prototype phase. How the ultra fast opening switch will handle the arc, the opening speed and the cooling mechanism is still uncertain. The cooling of the arc, and especially the time for cooling is important parameters for the hybrid CB without the LCS. This will determine the time of commutation, and thus the time of interruption. In this report, the cooling of the arc is expected to occur roughly 2.5 ms after the fault, and half a ms longer before the commutation path IGBTs turn-off. These values are chosen based upon information collected from [23] on the expected interruption time of the hybrid CB without LCS.

It should be mentioned that the fault current limiter, and residual current CB should be implemented in all HVDC CB. The current limiter is necessary for the to decrease the required interruption time of the CB, and is also important in MTDC operation. The residual current CB is important to prevent thermal overload and degradation of the arrestor banks after fault current interruption. The residual current CB is not meant to interrupt the full fault current, but only a few amperes.

The two manufacturers topologies are quite different in topology and operation. At the moment of writing, the topology presented by ABB seems to be the

most promising, due to its leading qualities in interruption time, voltage rating and current interruption capability as can be seen in table 4.1. However, since ALSTOM's solution uses thyristors in the commutation path, they should achieve a lower on-state voltage drop, and thus commutate the current faster, leading to a faster interruption. The details of the CB solutions are not public, and the detailed operation of it would just be qualified guessing. However the manufacturers are still in the prototype phase, and the ratings and interruption time might change.

The components considered are for the hybrid CB topology presented by ABB in [24], and are generalized for a simpler understanding.

It have been difficult to find a arc model suitable for the P-HCB application. The choice fell on the Mayr-Schwarz model, since it have been used in two other thesis involving DC arcs.

Chapter 5

Models and Simulations

The aim is to analyse the effectiveness of the CB model in transient simulations. The different test system are simulated in PSCAD. This program allows for a detailed analysis of a transient in a fast switching situation. The first test system is an ideal source, the second is a diode rectifier test, and the third is a MTDC network.

5.1 Hybrid CB Model

There are two hybrid CB models, as described in section 3.8. The two models are modelled with the exact same commutation path and arrester, but with different nominal paths. The A-HCB uses the LCS to commutate the fault current, while the P-HCB commutates the current with the arc, and does therefore not have a LCS in the nominal path, but arcing model. It has not been described earlier, but all models of DC CBs must have a residual disconnecter to disconnect after the current zero crossing. The residual disconnecter is a load break switch designed to interrupt the residual currents. If no residual disconnecter is used, the arrester might be thermally overloaded.

5.1.1 Active Hybrid CB

There have been done several studies on the hybrid CB and its behaviour. Since the LCS is the commutating force, it has been decided that the arc model is not relevant for this topology. The model used in this report is given by PSCAD, and based upon the ABB hybrid CB model illustrated in [24] and figure 4.9. This model uses two modules with IGBTs and diodes in anti-parallel in a bipolar configuration. Each of these modules have their own arrester, allowing for a better interruption of the fault current. There are two mechanical switches used, the ultra

fast disconnecter with a series connected LCS. The UFDs purpose is to create a significant enough voltage drop allowing the LCS to commutate the current to the commutation path. The model used is better explained in [24].

Parameter selection

The parameters should carefully be selected to replicate a realistic situation as possible. The voltage and power levels of the system are defining for the selection of the components. This report will consider both a 320 kV and a 400 kV system, with a nominal current variation from 1 kA to 9 kA. Due to time limitations, the stray inductances and cooling of the components have not been considered, although it is also a crucial part of the switching, to withstand the high currents and voltages that may increase to 30 kA and 1300 kV. From a data sheet provided by the power electronics manufacturer, Infinion, it is found that the number of IGBT modules in series should be around 300, giving a total on-resistance for the main DC breaker in the region of 30 mΩ. [47] To meet the required current values, there should be 13 parallel paths. In the simulation, the number of IGBTs in series are added up as a total resistance in the IGBTs. The parallel IGBTs are not included for simplicity of this simulation. Is is however worth mentioning that the IGBTs in series and parallel are only for one direction. For a bidirectional operation, the same number of IGBTs are required, in the opposite direction as well.

For the LCS to successfully commutate the fault current to the main DC breaker, the LCS must be able to withstand a higher voltage drop than the on-state voltage drop of the commutation path. This voltage drop will typically be around a few kilo volts, thus will the on-state voltage drop of the LCS be in the range of a few volts. Therefore the LCS does not consist of a large IGBT module, and the on-state losses might be reduced to less than 1 %. In the simulation, the on-state voltage drop must be manually typed in. Therefore a constant on-state voltage drop of 1.6 kV across the commutation path is selected. This values are a bit incorrect, but gives a good illustration of the fault behaviour in the hybrid CBs.

Previous Work

ABB developed the first hybrid CB in 2011, with ALSTOM following shortly after. Their models are quite different, but uses the same principle of operation. There have been a few thesis continuing the study of the A-HCB model proposed by ABB, amongst them are [22] and [43].

5.1.2 Passive Hybrid CB

The P-HCB is a more difficult CB to model. It uses the same arrester and commutation path as the A-HCB, but uses a different nominal path. Instead of the LCS, it has a black-box arcing model.

In a P-HCB the interrupting process is entirely dependent on the arc. The arc behaviour is very crucial for the CB. Black box models are used for simulating of the arc behaviour, the choosing of the correct parameters are important for the accuracy of the arc. The black box model used in this report is taken from [22], and based upon the the Mayr-Schwarz equation. This black box model uses two submodules, one for the arc elongation and one for the dynamic behaviour.

The arc elongation is illustrated in Figure 5.1 and arc behaviour during contact separation, until the mechanical switch is fully open.

$$r_{arc}(t) = \frac{E_{arc} \cdot l_{arc}/\Delta T_{nozzle}}{i_{arc}} \cdot t \tag{5.1}$$

Equation (5.1) is the basis for Figure 5.1. Where r_{arc} is the arc resistance, E_{arc} is the arc voltage gradient, l_{arc} is the length of the arc, ΔT_{nozzle} is the required opening time of the nozzle and i_{arc} is the current through the arc.

The governing equation for the Figure 5.2 is presented in section 4.5.

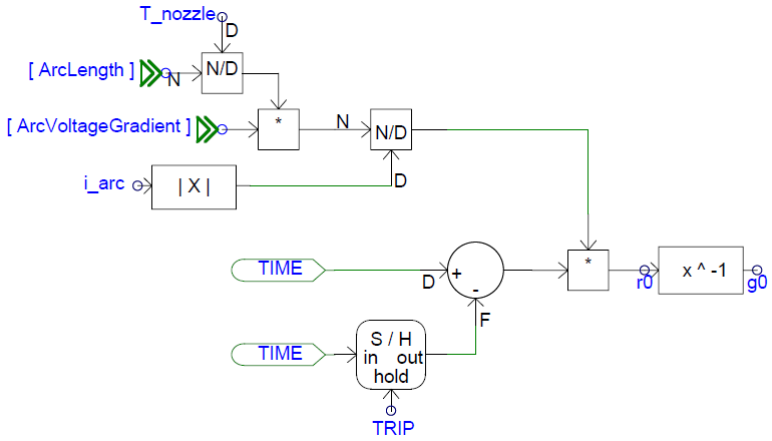


Figure 5.1: Arc elongation implementation in PSCAD [22]

Parameter selection

The parameters used for the arcing model illustrated in Figure 5.1 and 5.2 is illustrated in Table 5.1. The on-state voltage drop is considered equal for the P-HCB and the A-HCB.

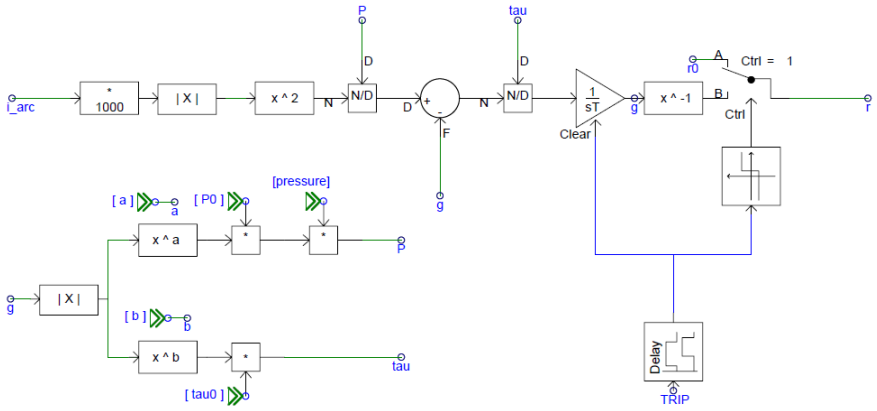


Figure 5.2: Dynamic arc implementation in PSCAD [22]

Table 5.1: Parameters used in the black box module [22]

Parameters	Value
ΔT_{nozzle}	1 ms
Arc gradient, E_{arc}	2 kV/m
Lengt of arc, L_{arc}	15 cm
Cooling power, P_0	393
Blow pressure	70 bar
a	0.25
b	0.5
τ_0	15 μs

Previous Work

There have been several reports working on the DC arc model. Most of whom have been working on the DC arc model for the resonance CB. The thesis focusing on the resonance CB are [22, 23], using the classical Cassie and Mayr equations. In [43] the emprical Paukert method is used. It has been decided to use the classical Cassie-Mayr equations for this report. The PSCAD implementation can be seen in Figure 5.1 and 5.2, and is taken from [22].

5.2 Methodology for the Circuit Breaker Testing

The main goal of this report is to evaluate the hybrid CB operation. To test the different requirements mentioned in section 3.3, three different test are to

be conducted for the hybrid CBs viability. The testing can be divided into two sections;

1. **Component level test:** Reference system 1 and 2
2. **System level test:** Reference system 3

The component level test is conducted to check if the hybrid CB behaves as expected. The system level test will have its main focus on the detection method, but it is also important to evaluate the CBs fault handling in a system with several feeders.

The different test systems are simulating the CBs reaction to a short circuit fault. The fault is modelled to be instantaneous, and therefore the gradual fault propagation behaviour that often occurs in subsea cables is not implemented.

5.3 Reference System 1: Ideal Source

Reference system 1, seen in Figure 5.3, is used to check the viability of the hybrid CB. This system is using an ideal DC voltage source. The voltage source is set to 320 kV pole-to-ground voltage. The fault is modelled as a load resistance suddenly shifting from full load to short circuit resistance. This emulates the short circuit in a good manner. The fault is occurring close to the converter. The inductance is emulating both the cable and the current limiting reactor. The parameter size is listed in Table 5.2. The advantages of using this test system is the simplicity of implementation and study of it. The drawbacks are the lack of a DC side capacitor, thus not emulating the complete transient behaviour. There is neither a cable model implemented, and the ideal source gives no current ripples.

In this test system the arrester voltage is set to be 240 kV in module 1 and 120 kV in module 2.

Table 5.2: Parameters used in reference system 1

Parameters	Value	unit
V_{DC}	320	kV
L	0.08	H
R_{Load}	200	Ω
$R_{SC,fault}$	0.01	Ω

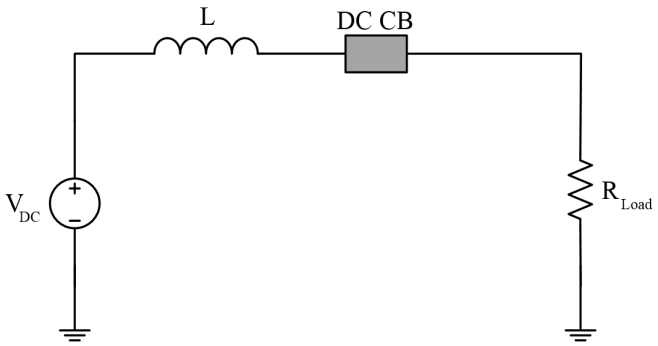


Figure 5.3: Ideal CB test

5.3.1 Simulation Results

Active Hybrid Circuit Breaker

In Figure 5.4, the current characteristics of an A-HCB are illustrated. The fault is commutated from the LCS at 0.15 ms after the fault occurs. The commutation path IGBTs conduct the current until the UFD is fully open and have regained full dielectric strength, at 1.2 ms after the fault occurs.

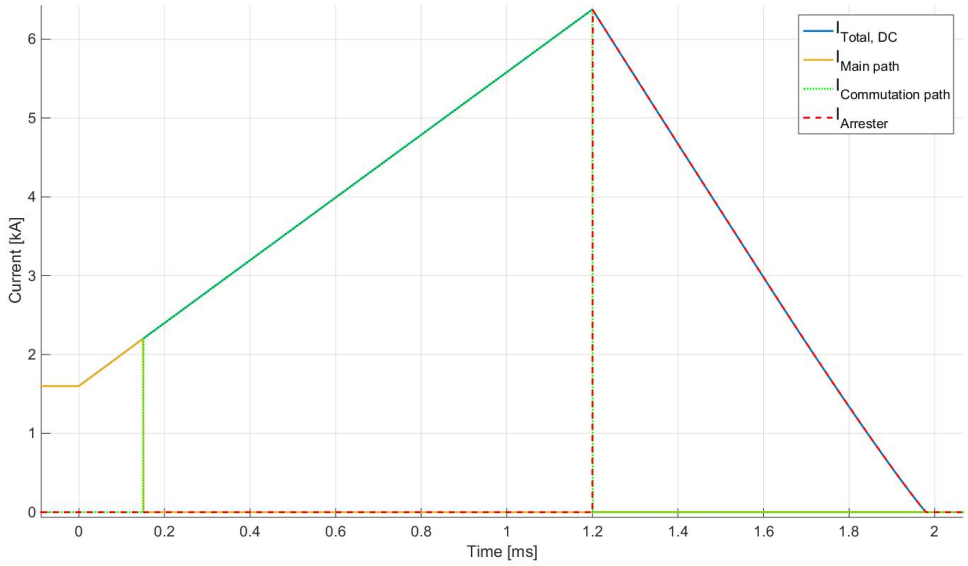


Figure 5.4: Current behaviour for in an ideal test system

When the commutation path IGBTs are turned off, the voltage will instan-

taneously build up across the breaker, a counteracting voltage. The voltage will increase until it reaches a pre-defined value for the arrester. The counteracting voltage forces the current to a zero crossing. The voltage behaviour is shown in figure 5.5, and after the fault is cleared the V_{CB} settles at the pre-fault system voltage level.

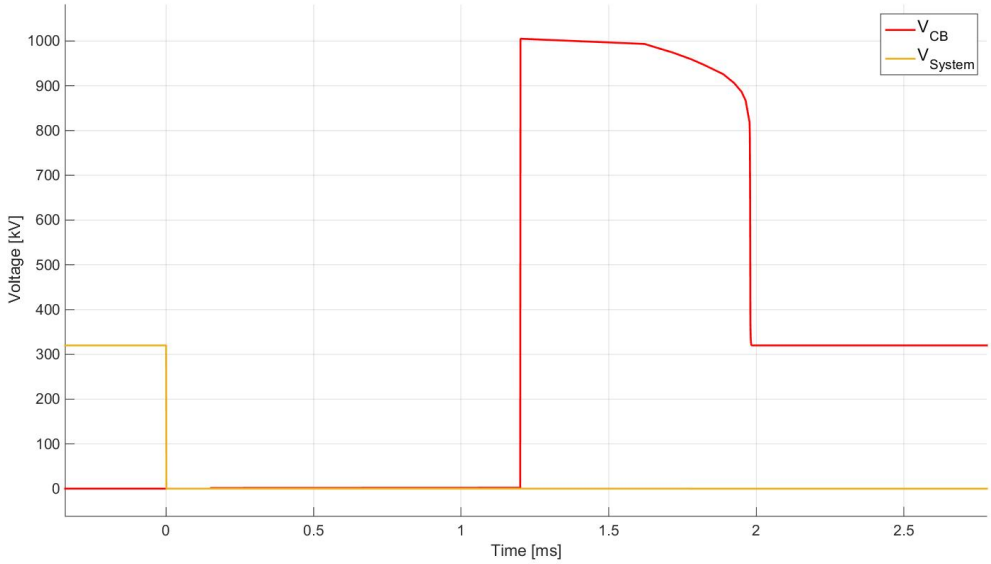


Figure 5.5: Voltage behaviour for in an ideal test system

The remaining energy in the system is dissipated in the arrester. Figure 5.6 illustrates how the arresters dissipate the remaining energy in the system at the same time as the voltage increases above the arresters settings. The energy is dissipated through the different arresters in the two modules. They have different voltage ratings, and are thus dissipating different amount of energy.

Passive Hybrid Circuit Breaker

The effect of removing the LCS as the commutating component is significant. The arc now has to create a voltage drop across it higher than the on-state voltage drop across the commutation path. Figure 5.7 shows that the commutation path IGBTs turn-on at 0.15 ms after the fault, but the current is not commutated before 1.6 ms after the fault. 0.9 ms later, the commutation path IGBTs turns off, forcing the voltage to build up across the breaker until it reaches the pre-set value

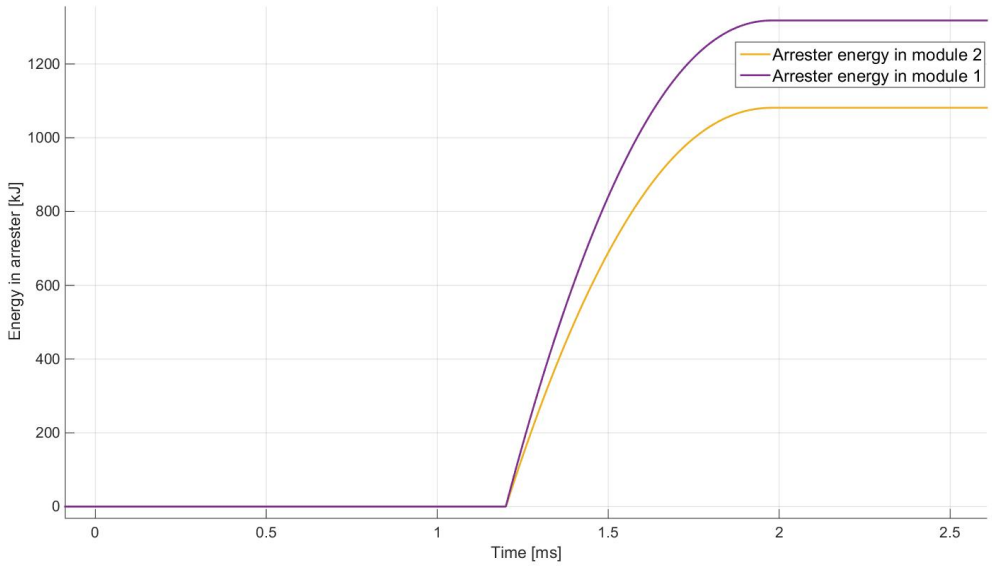


Figure 5.6: Energy absorbed by the arresters in an ideal test system

of the arrester and it start to conduct the current, as illustrated in figure 5.8. The operation time of the different components are difficult to estimate, as there have not been done any detailed studies of this topology. The results of this section is thus purely academic, and might not be transferred into a real CB.

Figure 5.9 shows the energy dissipated by the arrester. Compared to the previous simulated hybrid CB with LCS, the energy in this model has a much higher energy dissipation. This higher energy dissipation requires much more of the arrester, and will significantly increase the total system costs.

The arc resistance obtained from the simulations results is low before the cooling of the arc starts, and the current is commutated to the commutation path. This action occurs roughly 1.6 ms after the fault occurs, and the arc resistance immediately goes towards infinity.

5.4 Reference system 2: Diode Rectifier

Reference system 2 is an 2-level diode rectifier, in a Graetz-bridge configuration as illustrated in Figure 5.11. Unlike reference system 1, this is a non-idealized system and is used to compare the effect of the interruption time on the rectifying diodes, and a better understanding of the fault current behaviour. The DC voltage in this system is dependent on the load resistance and current through it, given by ohms

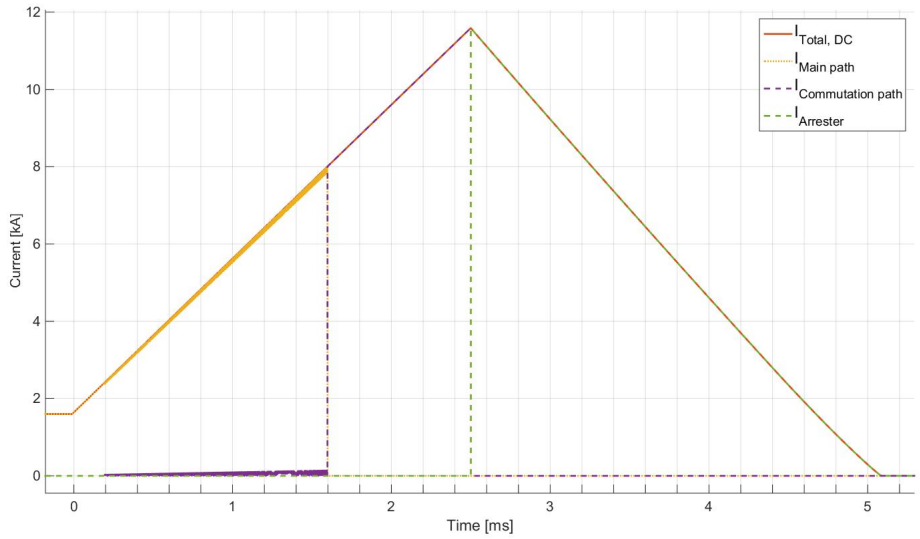


Figure 5.7: Current behaviour

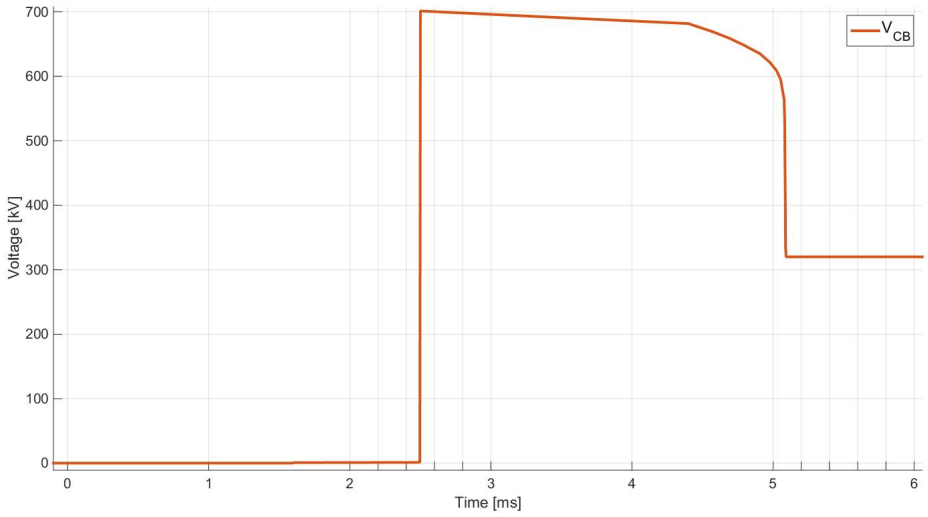


Figure 5.8: Voltage behaviour

first law. The advantages of using this test system is its simple 2-level rectifier, the DC side capacitors and possibility to investigate the diode currents. This system is also lacking a cable model, the cable model will give a better detailed description of how the cable resistivity and the delay due to the length. The large DC side capacitors are undesirable, and not realistic, but necessary in this case for correct

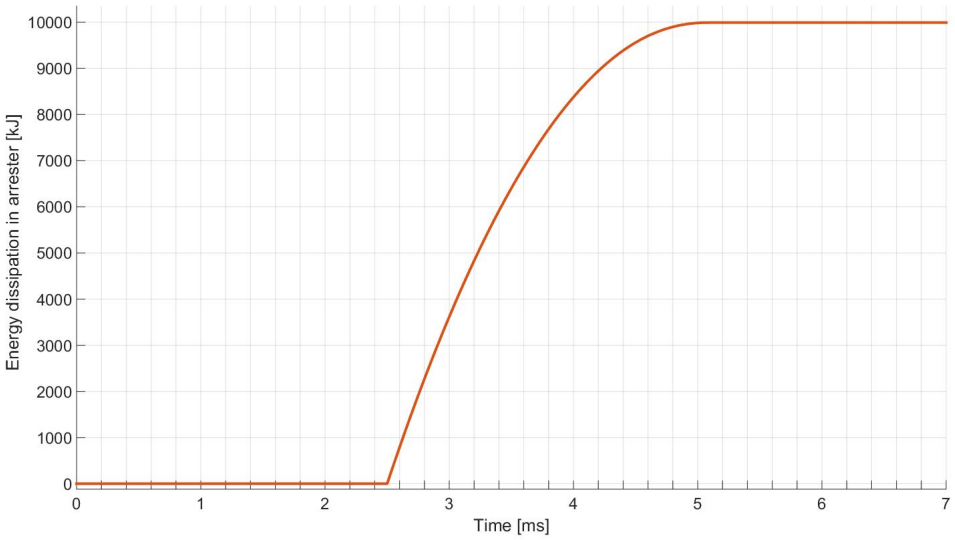


Figure 5.9: Energy through the arrester

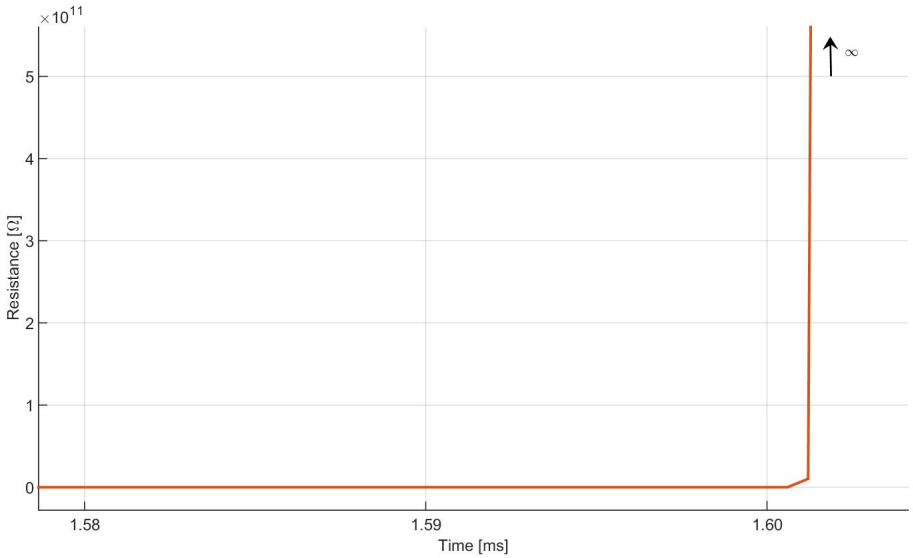


Figure 5.10: Arc resistance

fault behaviour. In Table 5.3 the parameters used for this reference system is shown.

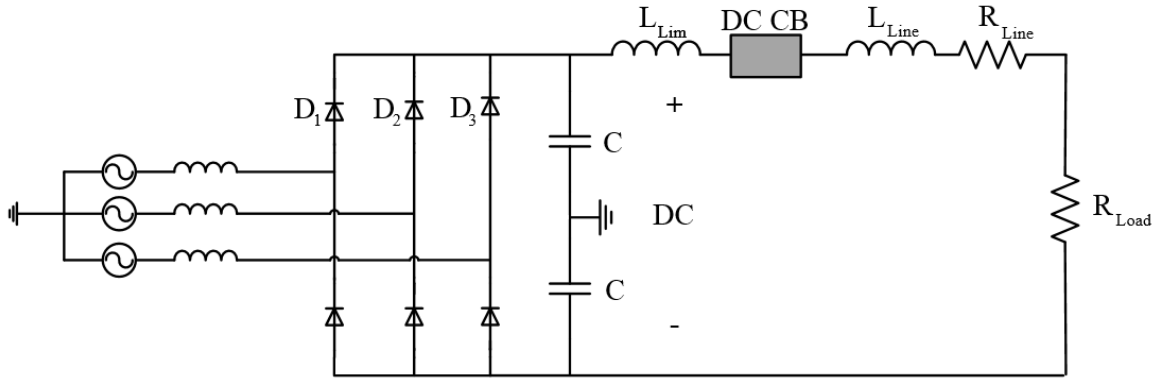


Figure 5.11: 6-pulse VSC test system for the CB

Table 5.3: Parameters used in reference system 2

Parameters	Value	Unit
V_{DC}	320	kV
L_{Line}	0.2	mH
R_{Line}	2	mΩ
L_{Lim}	8	mH
R_{Load}	170	Ω
$R_{SC,fault}$	0.01	Ω
C	2000	μF

5.4.1 Simulations of Fault Current and Temperature Behaviour

To estimate the current, Cauers electro thermal model is used, this is shown in Figure 5.12. This model will give an estimation to how the diode will react to the high fault current, and it is important to emphasise that temperature may increase differently with other cooling arrangements.

The values used for this model are found in [48], and illustrated in Table 5.4.

Table 5.4: Values used for the Cauer model [48]

i	1	2	3	4
R_i [K/kW]	0.5167	0.6997	1.5762	1.2524
C_i [kJ/K]	0.0024	0.0114	0.025	0.4227

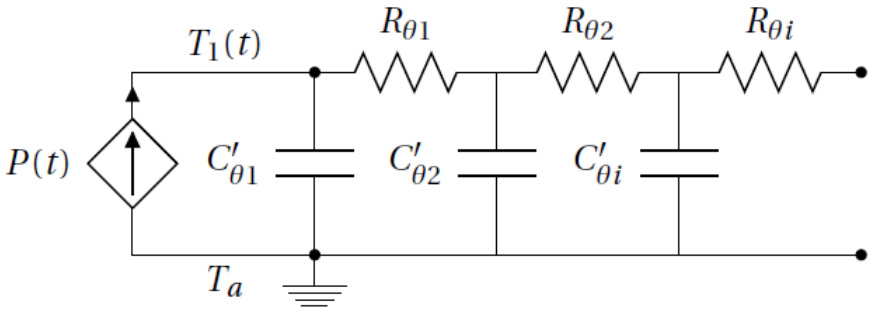


Figure 5.12: Cauers electro thermal model [17]

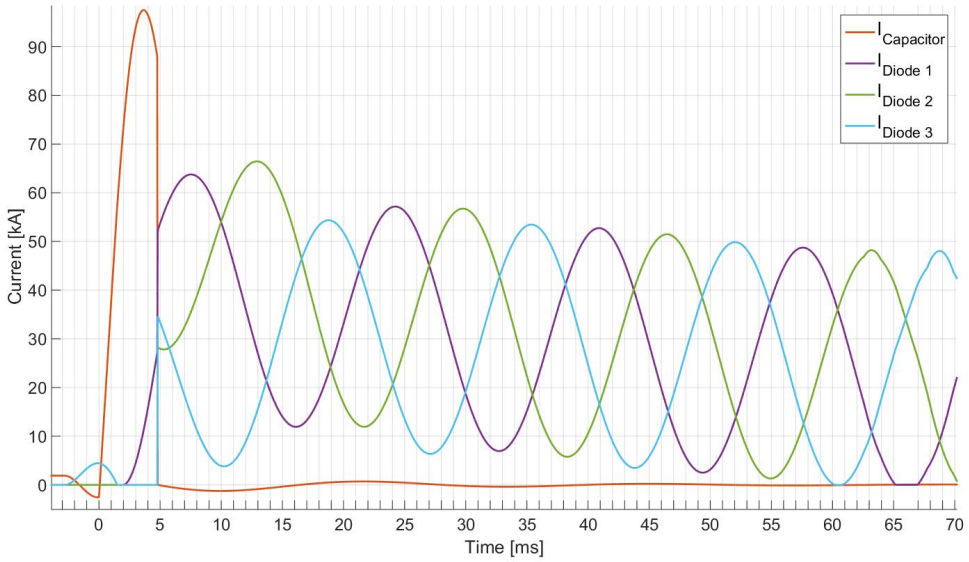
Without Fault Current Interruption

A VSC system is very vulnerable to DC side faults, as discussed in section 3.1.1. To illustrate the problem when a DC fault occurs, a fault is applied in reference system 2. The fault current behaviour is illustrated in figure 5.13a. The fault occurs at 0 ms, and an immediate discharge of the DC side capacitors occurs. When the capacitors are fully discharged, stage 2 commences, this is also the most critical stage of operation. 55 ms after the fault occurs stage 3 starts, this is clear as the diode currents reaches a steady state. It is important to mention that the current behaviour is only valid for this particular case.

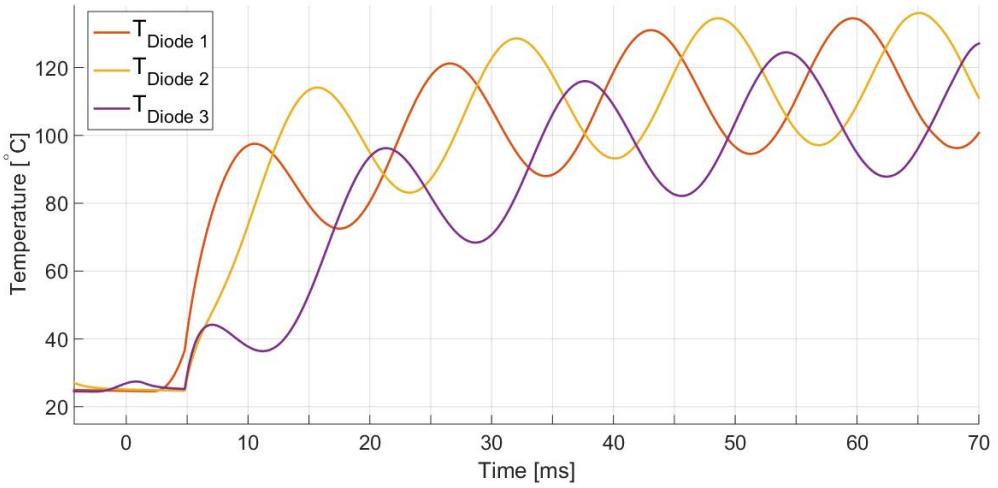
To illustrate the impact of the fault current through the freewheeling diodes, an estimation of the current has been simulated. The temperature estimation is shown in figure 5.13b. In reality there will be significant cooling systems for all the power electronic equipment in operation, this have not be considered in these simulations, as the purpose is only to illustrate the challenges for the HVDC CB. When stage 2 starts, the diode temperature immediately rises from the ambient temperatur of 25 °C, to 100 °C at 10 ms after the fault. A continuous operation of the diode at this temperature will lead to a thermal breakdown, given there is no cooling.

With Fault Current Interruption

Figure 5.14a illustrate the current behaviour in the same reference system as figure 5.13a, and with the same parameters. The fault is interrupted with the standardized behaviour of the hybrid CB with LCS. As can be seen the fault is now successfully interrupted in stage 1, as the peak value of $I_{Capacitor}$ now is reduced with 40 kA. After the fault is interrupted the capacitor is still being charged, but are considered as a swinging before a steady state is reached.



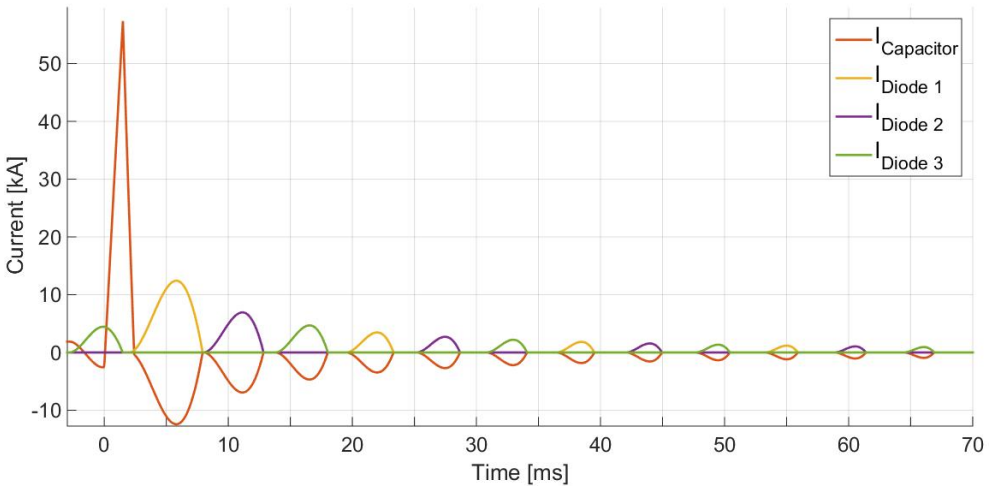
(a) Current



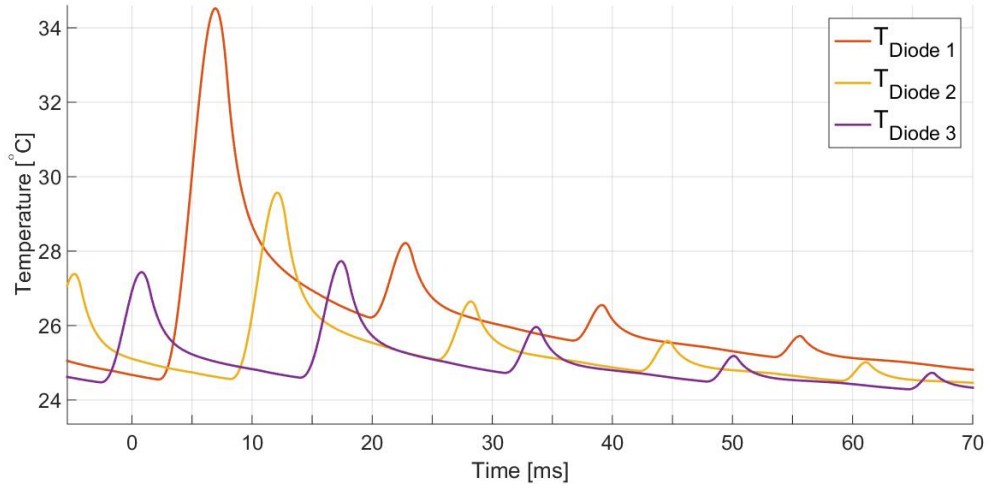
(b) Temperature

Figure 5.13: Current and temperature in the rectifying diodes when a fault is not interrupted

Figure 5.14b show a significant reduction of the temperature through the rectifying diodes compared to when there are no CB operation.



(a) Current

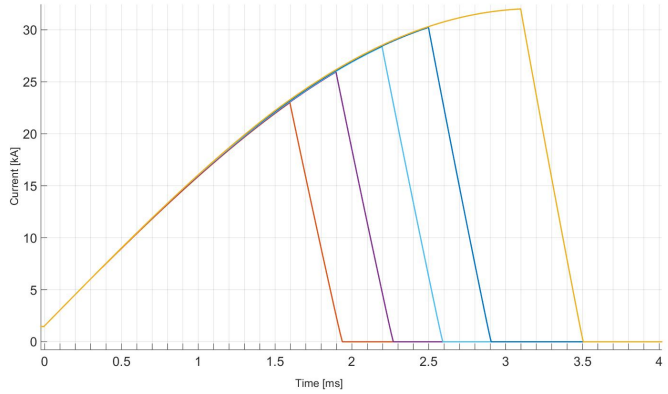


(b) Temperature

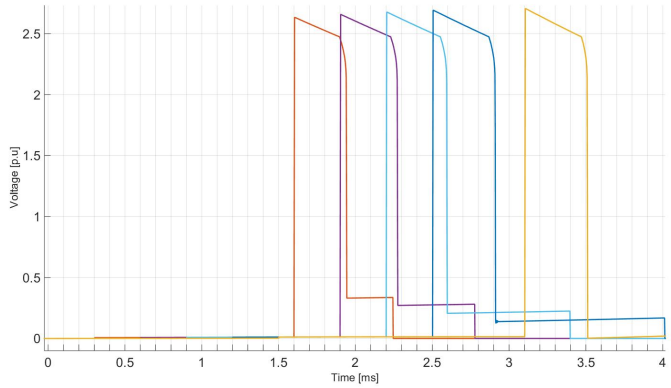
Figure 5.14: Current and temperature in the rectifying diodes when a fault is interrupted

5.4.2 Effect of Interruption Time

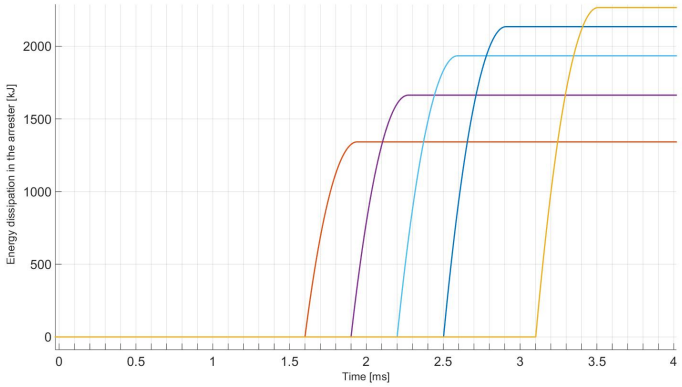
It have been mentioned in chapter xx, that it is important to interrupt the current as fast as possible. To prove this, an comparison of the current, voltage and arrester energy, is illustrated in figure 5.15. These simulations are conducted in reference system 2. As The interruption time increases, the peak current will also increase. When the turn-off time increases, the more energy must be dissipated by the



(a) Total Current



(b) Voltage across the CB



(c) Energy dissipated by the arrester in module 1

Figure 5.15: Effect of the interruption time

arrestor banks. From the minimum arrester energy of 1400 kJ, to the maximum of 2300 kJ. The increased energy to be absorbed by the arrester, gives higher requirements to the arrester on both energy absorption capability and cooling. This increases the cost of the arrester bank significantly, thus it should be as low as possible.

As mentioned in chapter xxx, the length of each cable is 200 km, and symmetrical. The system consists of one on-shore node, controlling the voltage, and 2 offshore nodes each controlling the power. Each systems should be tested thoroughly in able to determine the detection threshold of the detection algorithm, whether it is derivative, wavelet or some other method. The cable system is set up as a symmetric monopole with grounded midpoint and earthed return, illustrated in the specialization project.

The worst case scenario for protection and for the converters, is a fault applied close to them. Therefore all faults are applied close to the converters to test the worst case scenario for the CB operation. In a symmetrical system like this, the detection algorithm might have problems to distinguish between faults in different zones but close to the same converter.

5.5 Reference system 3: Multi-Terminal, with MMC

Reference system 3 is inspired by the CIGRÉ B4 test system described in [49]. Figure 5.16 show the entire system from CIGRÉ , and all the different nodes. In reference system 3, Figure 5.17, only three nodes are used, one onshore (A) and two offshore (C and E). The same nodes can also be seen in Figure 5.16, but the cable distances are changed to make a simpler system. Test system 3 only have three nodes for simplicity and due to software limitations. Some of the parameters for the listed in Table 5.5. This system will have 3 nodes, all equipped with a monopolar MMC. The system was originally using bipolar MMC configuration, but had to be reduced due to limitations in the simulation software. The advantage of this test system is that a complete fault behaviour can be seen, and all the cable parameters are very similar to the reality. The arrester values used for this reference system is 320 kV for module 1 and 280 kV for module 2.

The MTDC network simulated in this report is based upon the CIGRÉ offshore network, but limited to three nodes. Each node have a monopolar MMC converter, and each cable is 200 km long. Converter A represents a on-shore connection, controlling the voltage, while the other two nodes represent off-shore wind farms. The offshore nodes control the active power. This model will emulate how the DC breaker will react when faults is applied on different locations, this way the

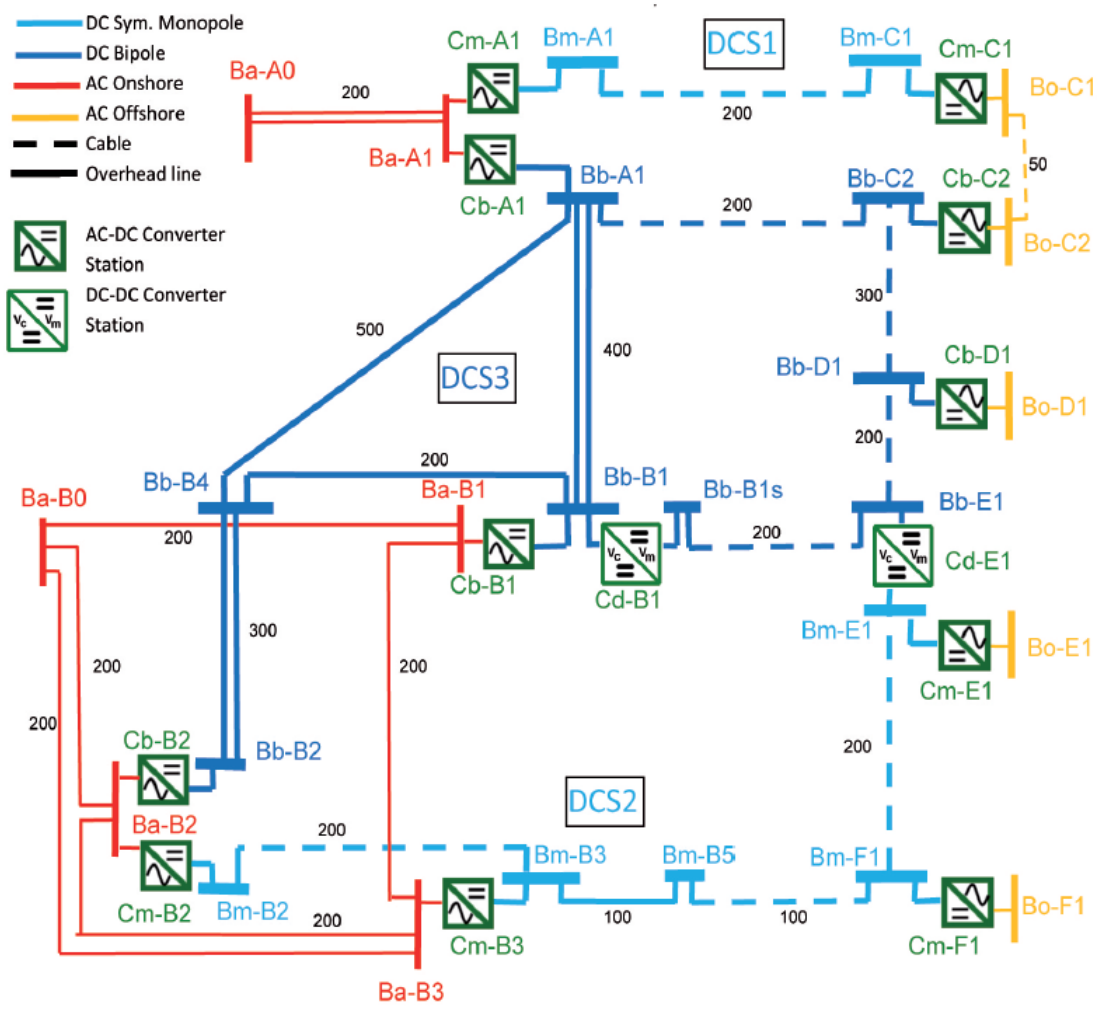


Figure 5.16: The detailed B4 DC test system [49]

Table 5.5: Parameters used in reference system 3

V_{DC}	400 kV
R_{Cable}	$1.89 \cdot 10^{-8}\Omega$m
L_{Lim}	0.08 H
$P_{A,AC}$	-1064 MW
$P_{C,AC}$	782 MW
$P_{E,AC}$	384 MW

selectivity of the CB is checked. To ensure selectivity the detection algorithm needs to be carefully selected and tuned. A big caution on the selected value of

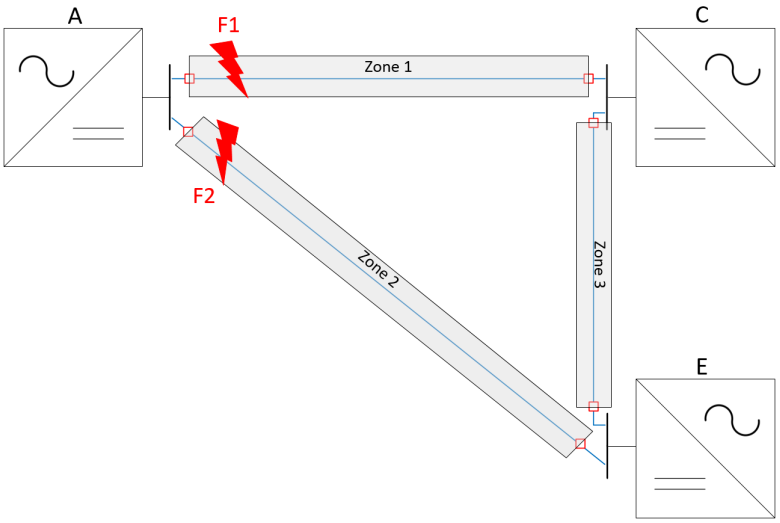


Figure 5.17: MTDC network with protection zones

the current limiting inductor is needed. It is a necessary evil as it becomes easier to interrupt the fault current, but it should not be to high as it might disturb the detection of the fault current. It is also very costly with a big current limiting reactor, and it is preferred that it remains as small as possible.

Converters

The PSCAD MTDC network used for this report, originally used a bipolar MMC configuration as illustrated in Figure 5.18. All three nodes were equipped with the similar converter and configuration. Due to limitations of electrical nodes in the educational version of PSCAD, the converters has to be reduced to a monopolar configuration. This change of the converter have a undesired affect on the fault current behaviour. During a pole-to-ground fault the voltage is expected to go to half of its rated value, since only one of the cables are missing, but this does not occur. To see the effects of the fault, a pole-to-pole fault is implemented. in the new system.

Cable modelling

There are two cable connection between each node in a symmetrical monople with grounded midpoint and earth return [42]. The cable is modelled as a frequency dependent phase model, and are based upon the travelling wave method. This is the recommended cable model over the Bergeron and frequency dependent mode

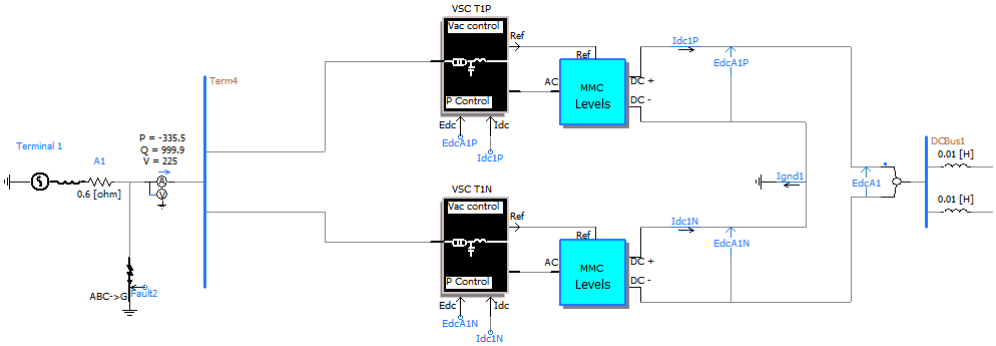


Figure 5.18: The bipolar MMC converters in the original PSCAD scheme

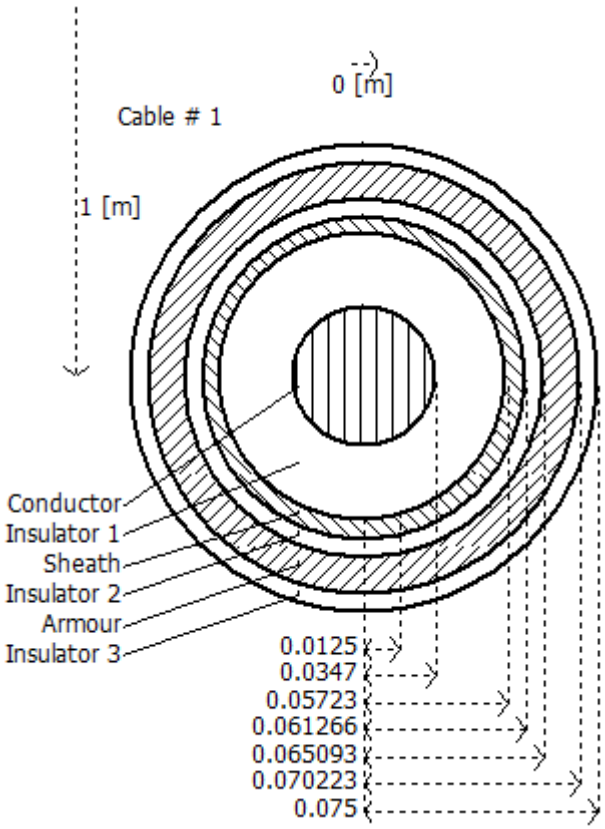


Figure 5.19: Configuration of the frequency dependent cable model

model.

5.5.1 Steady State Behaviour

In order to understand the what happens during a fault, it is useful to study the steady state behaviour, without any fault. Figure 5.20 show the current amplitude and direction for each cable. There are some disturbance in the current waveforms due to the reduction of the converter to a mono-polar one. Time limitations did not allow for a better tuning of the converters, but the disturbance is not considered important for understanding the behaviour. In Figure 5.21 the pole-to-pole DC voltage is illustrated. Like the DC currents, there is some disturbance for the DC voltage. The power production and consumption is illustrated in Figure 5.22. Figure 5.23 shows the RMS voltage at each converter.

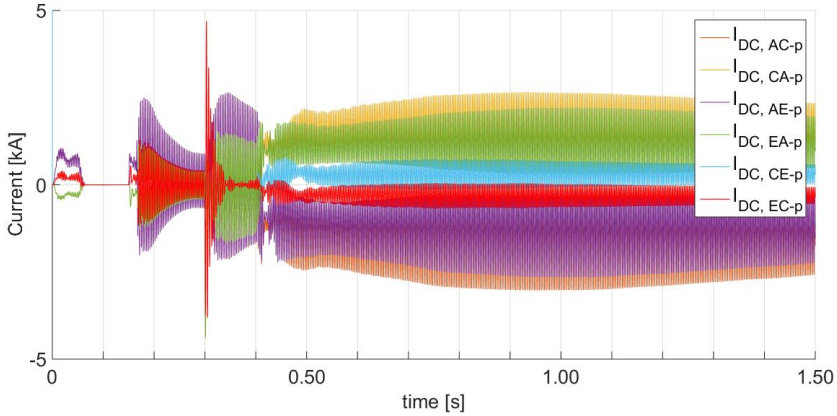


Figure 5.20: Current in the cables in steady state operation

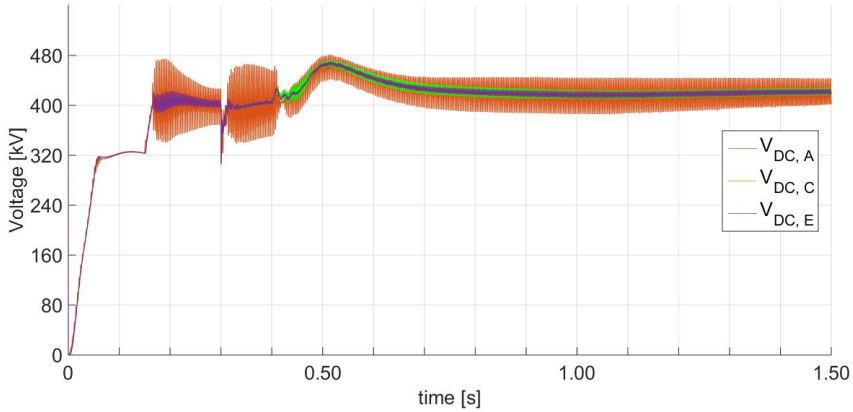


Figure 5.21: Pole-to-pole voltage on the DC side of each converter in steady state operation

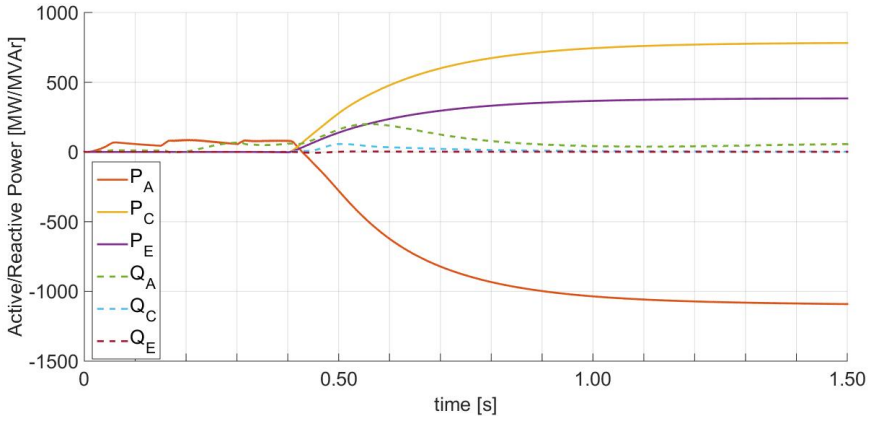


Figure 5.22: The active and reactive power on the AC side of each converter in steady state

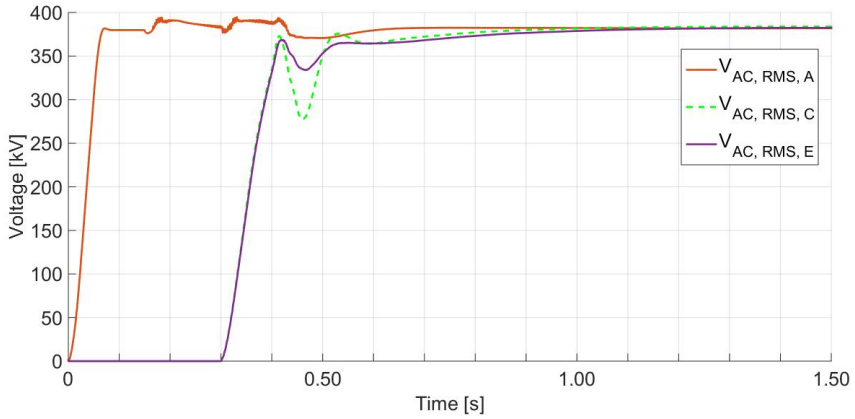


Figure 5.23: The AC RMS voltage on each node during steady state

These figures illustrate the entire simulation, but also how the initiation stages of the converters are. Converter A turns on at the start, but does not immediately start to control the voltage. At 0.05 s the AC voltage has reached it rated value, and the DC side voltage stabilizes at 320 kV. At 0.15 s the voltage controlling converter, A, turns on. The voltage is now being actively controlled. At 0.3 s, the power controlling converters turns on, as can be seen in Figure 5.23. This turn-on can also be seen in Figure 5.21 as a dip in the voltage. From Figure 5.22 it can be seen that it takes until 0.4 s for converter C and E to deliver power to the grid. The active power transfer reaches a steady state at about 1.2 s. From the same figure, shows how the converters require a lot of reactive power at turn-on. During steady state, only the voltage controlling converter requires some reactive power.

5.5.2 System Behaviour Without Fault Current Interruption

A pole to ground, SC fault is applied on the positive pole of the cable from converter A to converter C. The SC fault is applied 1 km from converter A.

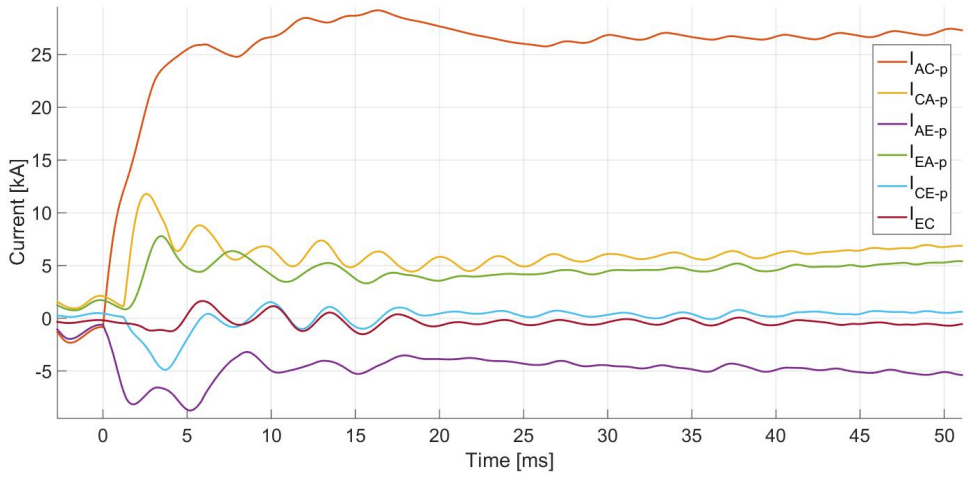


Figure 5.24: Current in the positive cable pole during a pole-to-pole fault without current interruption

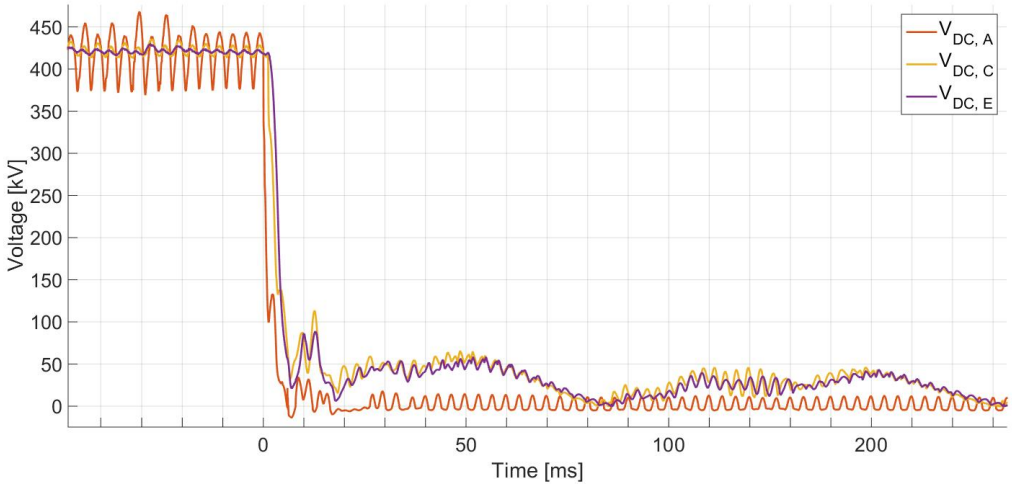


Figure 5.25: Pole-to-pole voltage at each converter during a pole-to-pole fault without current interruption

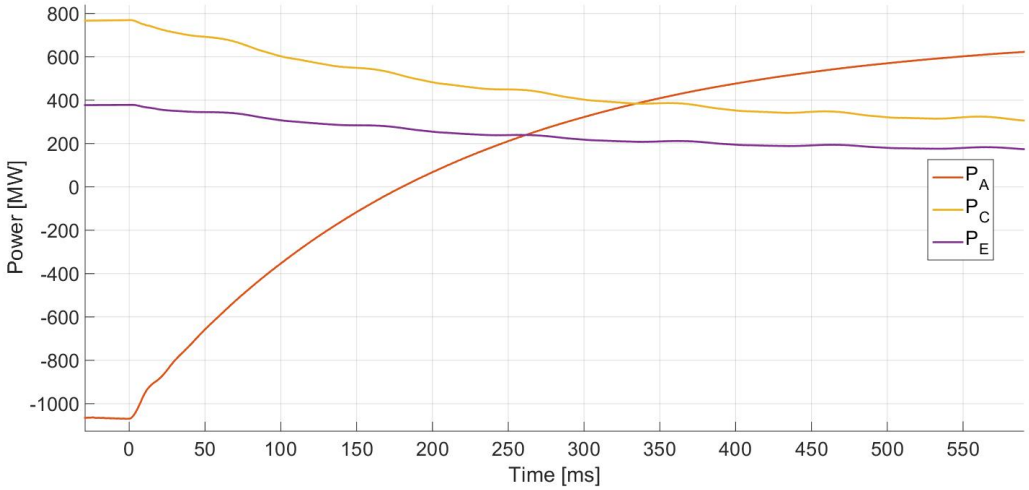


Figure 5.26: Active power behaviour during a pole-to-pole fault without current interruption

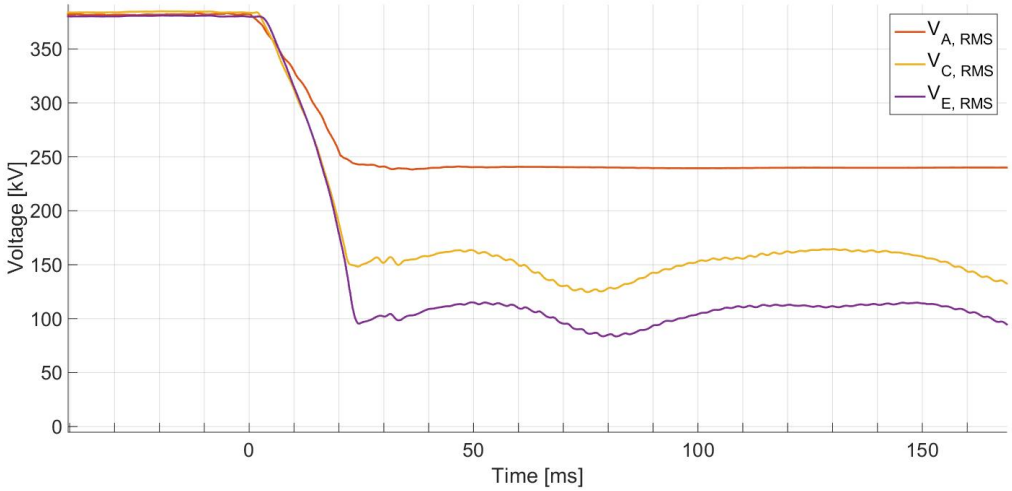


Figure 5.27: The AC grid RMS voltage during a pole-to-pole fault without current interruption

5.5.3 Detection method

In each system it is important to determine the what detection method and thresholds to choose. This is crucial to achieve a proper fault current interruption. There are several detection methods developed, in this report, the derivative protection is used. To determine if the current occurs in the CBs protection zone, the cur-

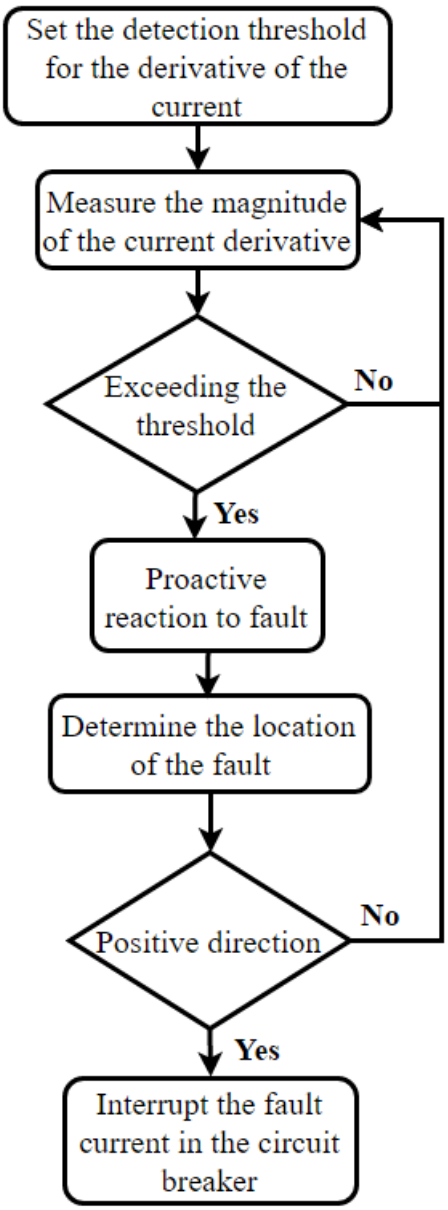


Figure 5.28: Flow chart for the detection method

rent direction is measured. In the derivative protection only the derivative of the current is measured, but it could also be possible to measure the derivative of the voltage. Other possible protection methods are differential protection, distance relays, travelling wave and wavelet protection. Since there are low inductances and capacitances the fault will travel near to the speed of light, and the fast fault

propagation, there is not possible to use communication between the CB in the same zone. It is however possible to use communication between the CBs close to the same converter, if there is a DC bus fault.

To determine the thresholds for the current derivative it is important to establish the highest and lowest value, to obtain selectivity in the system. In practice this is done by applying a fault close to a converter with two adjacent cables. In the example given in Figure 5.17 a fault, F1, is first applied in zone 1, 1 km from converter A. Then a second fault, F2, is applied on the same distance from converter A, but know in protection zone 2. The reason for doing this, is because the fault will look almost the same for CA-p and EA-p when the fault is applied at F1. The threshold for the current derivative for CB CA-p and EA-p, can after testing of these two faults be determined. By assuming that the system is symmetrical, the threshold should be similar for all the CBs given in this reference system.

The flow chart in Figure 5.28 illustrate the detection method for each CB. And describe more detailed how the practical implementation of the detection algorithm illustrated in Figure 5.29.

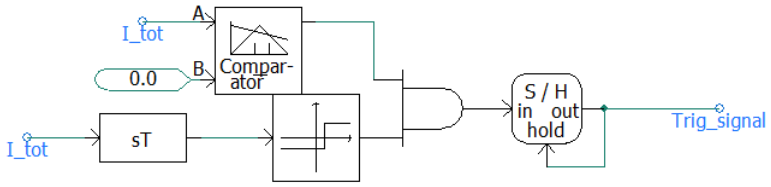


Figure 5.29: Detection algorithm

Previous work

There have been conducted several studies on this topic, latest in Raymundo Torres's IEEE report but also by a CIGRÉ Work group. They have looked into the fault detection and location methods. Raymundo uses a discrete wavelet method for the detecting and locating of the fault. This part of this report builds on his report.

Effect of the current limiting reactor inductance

The reference system 3 is symmetrical in the sense of the cable length. Therefore the current limiting reactors are set to an equal size. In such a system, when a pole-to-pole fault is applied close to converter A in protection zone 1, the derivative

of the fault will be almost the same on breaker CA and EA. The threshold value selected in the detection mechanism must therefore be able to distinguish between a fault that occurs inside and outside of its protection zone. In practice, this is done by studying the maximum derivative value for both cases. Figure 5.31 shows the threshold margin for F1 fault. The largest threshold is set by CB CA-p, and the minimum value for the threshold is set by the maximum detection value on CB EA-p. In Figure 5.30 the effect of changing the CLR can be seen. Every values are normalized based on the average threshold margin. It becomes obvious that the larger the the CLR becmomes, the larger the threshold margin will be.

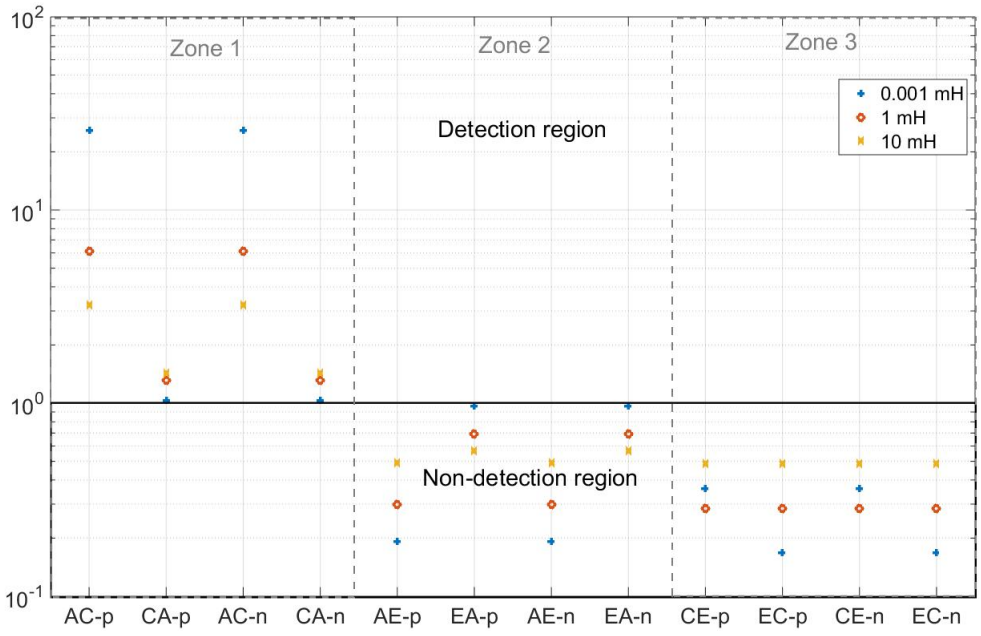


Figure 5.30: Normalized derivative threshold values for different inductor sizes

Effect of fault resistance

The resistance of the DC fault in sea cables are not widely studied. There are two main reasons for faults in a DC sea cable system; failure due to external forces i.e. an anchor, and due to internal insulation failure. The fault resistance depend on the insulation material of the cable. Since the fault resistance might vary a lot, it is imperative that the interruption of the fault also is investigated with different resistances.

The MTDC network was tested with different fault resistances, as can be seen

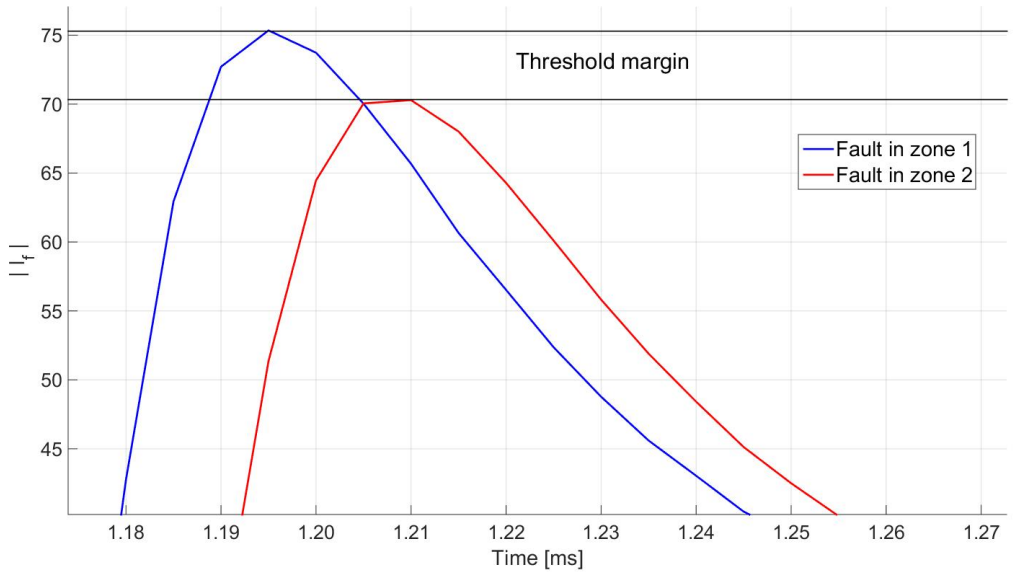


Figure 5.31: Threshold margin with a 0.001 mH reactor for CA-p

in appendix A. The reactor size is chosen to be 10 mH, and the fault is applied on line AC, 1 km from converter A. The highest possible fault resistance within the range of detection for a system with reactor value of 10 mH is 10 Ω . The detection region of the fault is illustrated in figure A.1. The detection region is defined by the threshold set in the detection algorithm. This test uses a pole to ground fault, so it is not quite accurate, but gives an illustration of the difficulties with increasing fault resistance.

5.5.4 Pole-to-pole fault, F1, With A-HCB

A pole-to-pole fault is applied close to converter A in zone 1. This fault is illustrated as F1 in Figure 5.17. All the currents and waveforms depicted in the following subsections are for the different CBs relevant for this fault. All currents measured on the cables are measured with the positive direction towards the midpoint of the cable. In the negative pole cables, the positive direction

AC-p

The current interruption on CB AC-p are shown in Figure 5.32. The operational time of the CB is equal to that described in section 5.3. The detection time is a bit slower due to the negative nominal current. This is reflected by a 1 ms slower detection and reaction to the fault. The total interruption time is now 1.4 ms after

the fault occurs.

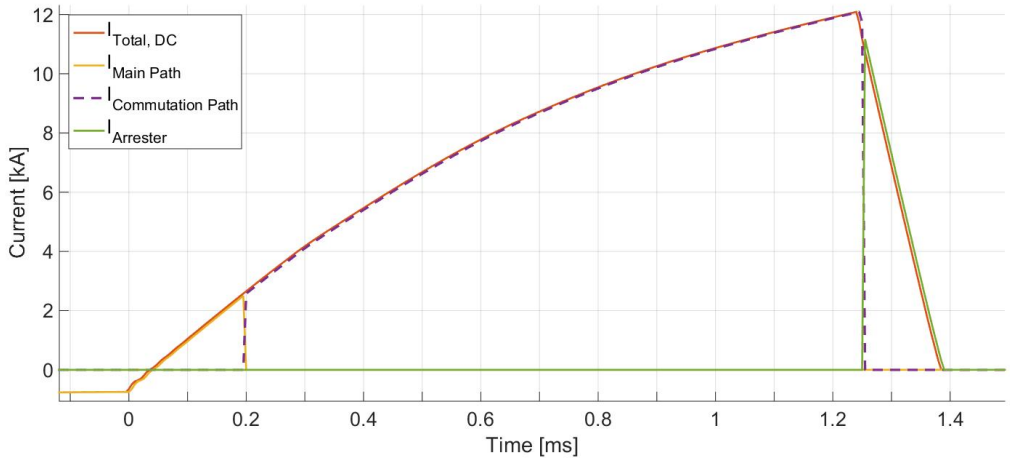


Figure 5.32: Current behaviour in AC-p

When the commutation path IGBTs turn-off, the voltage builds-up instantly as can be seen in Figure 5.33. As the arrester forces the current decreases, the voltage will decrease. When the current is interrupted and a zero crossing is achieved, the voltage across the CB goes to the system voltage. For a bipolar cable configuration, the voltage across the CB are half of the system voltage.

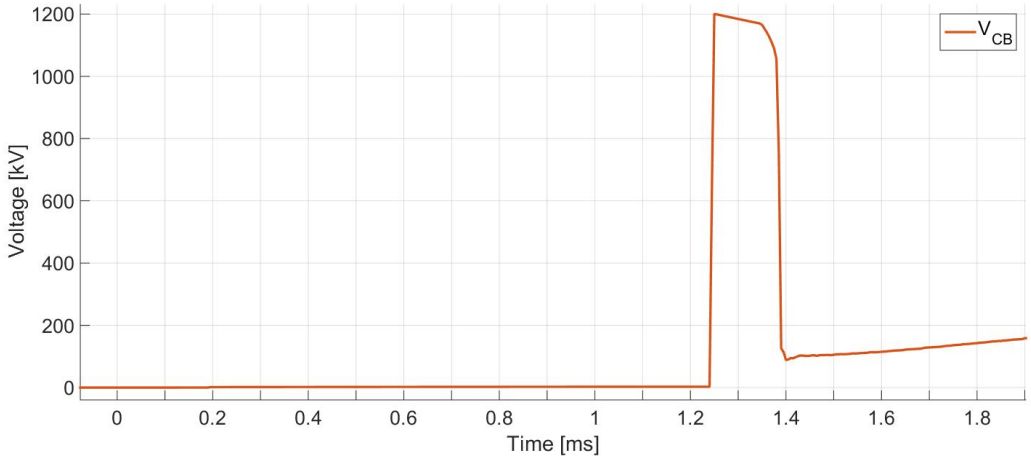


Figure 5.33: Voltage behaviour in AC-p

The energy dissipated in the arrester can be seen in Figure 5.34. Since there

are one arrester in parallel with each main breaker module, the total dissipated energy in the arresters are about 1000 kJ.

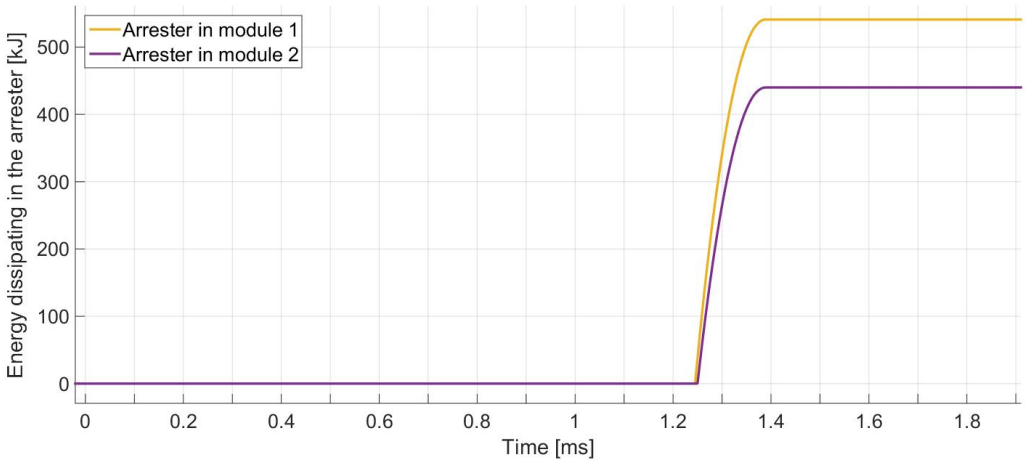


Figure 5.34: Energy behaviour in AC-p

CA-p

The fault is located 199 km from CA-p, causing a time delay of 1.2 ms before it can see the fault. The waveforms of the currents for both AC-p and CA-p is more or less equal during the interruption. Figure 5.35 show the current waveforms.

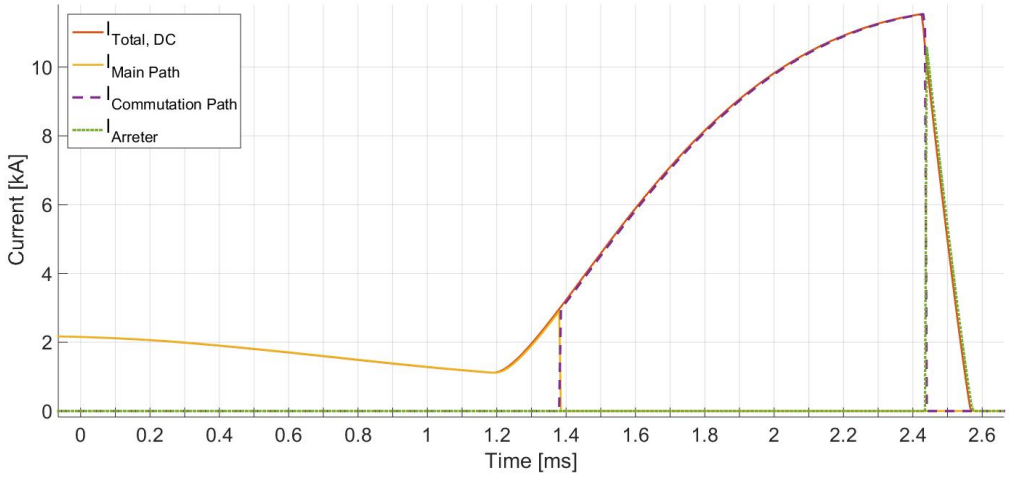


Figure 5.35: Current behaviour in CA-p

At 2.4 ms after the fault, the commutation path IGBTs turns off, and the voltage instantly builds up. This is shown in Figure 5.36, and the voltage reaches the same level as the corresponding CB AC-p does. When the current crosses zero right before 2.6 ms, the voltage goes to the system half of the system voltage.

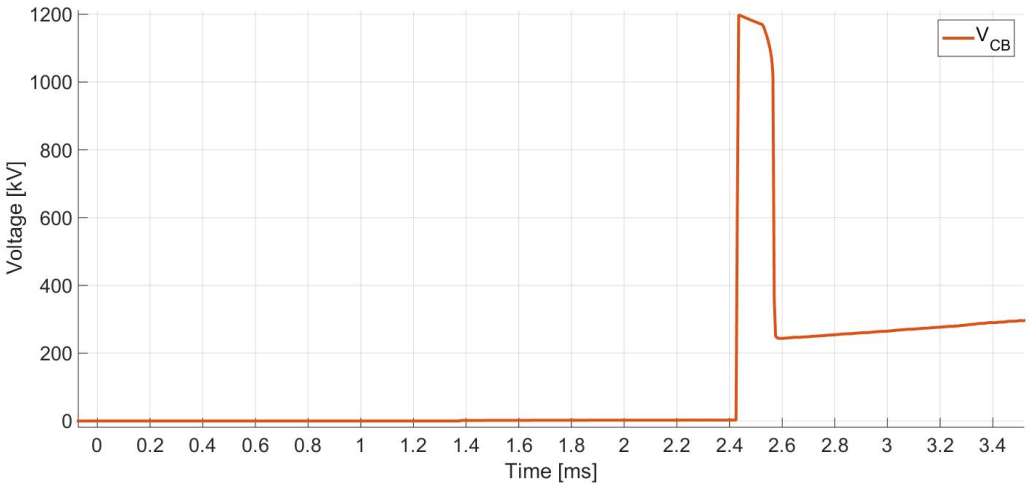


Figure 5.36: Voltage behaviour in CA-p

When the current zero is reached, the arrestor start to dissipate the remnant energy stored in the system. Figure 5.37 show how the two arresters dissipates almost 900 kJ.

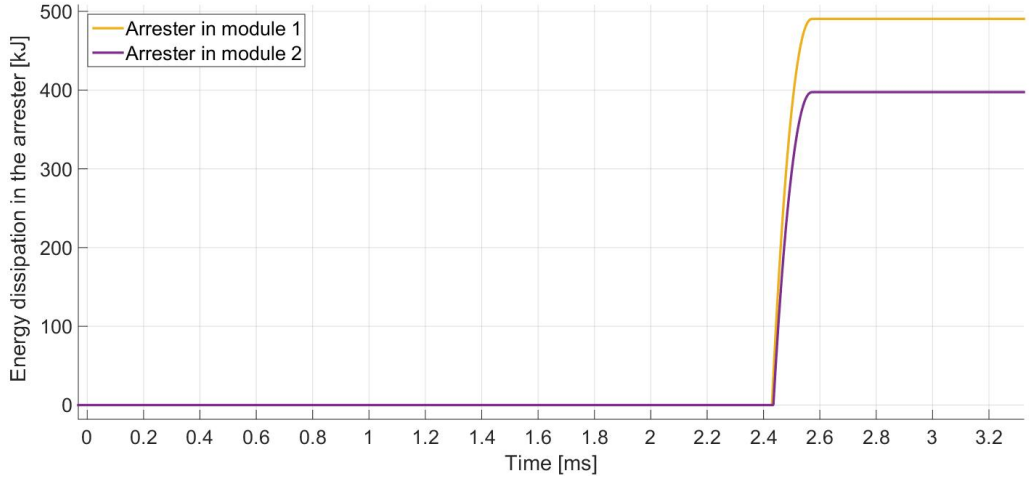


Figure 5.37: Energy behaviour in CA-p

Power flow

As can be seen in the Figure 5.20, the most of the power is flowing by cable AC and AE. When a fault occurs on cable AC or AE, and is successfully interrupted and thus isolated, the power flow should change. Figure 5.38 show how the current flow change after fault interruption, the current through cable AC goes to zero, and the power from converter C is now solely conducted through the cable CE. It is shown how the current is interrupted, and the current uses about 110 ms to settle in a new steady state. The more detailed current behaviour can be seen in Figure 5.39, a zoomed section of Figure 5.38.

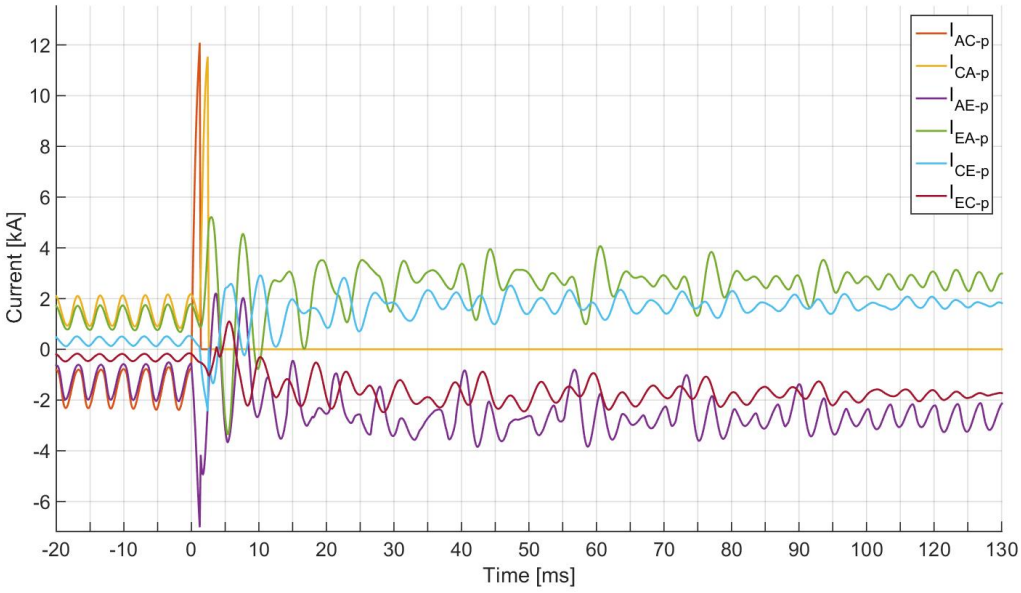


Figure 5.38: Current flow in the cables

The behaviour of the converter pole-pole voltage can be seen in Figure 5.40. The DC voltage will drop towards 0 when the fault occurs, but the fault is interrupted by AC-p at 1.4 ms, instantaneously restoring the voltage at converter A. The voltage also starts to decrease at converter C, but the fault interruption at 2.6 ms for CA-p restores the converter DC voltage.

Figure 5.41 show how the power flow on the AC side of each converter reacts to the fault. As can be seen, there is not much change in the power flow. P_C and P_E keeps at its rated values, but converter A will consume less power. In Figure 5.42 shows only the power of converter A. It show how the converter consumes 50

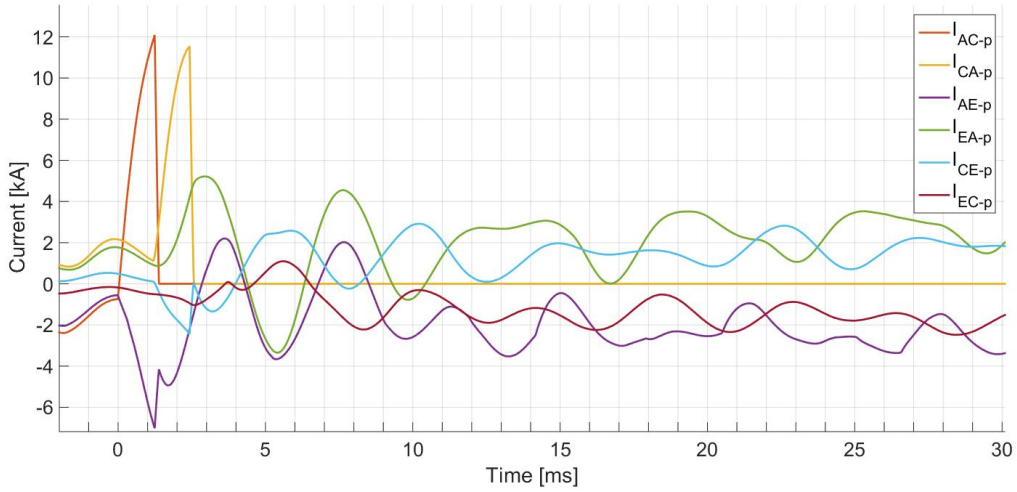


Figure 5.39: Current flow in the cables, zoomed

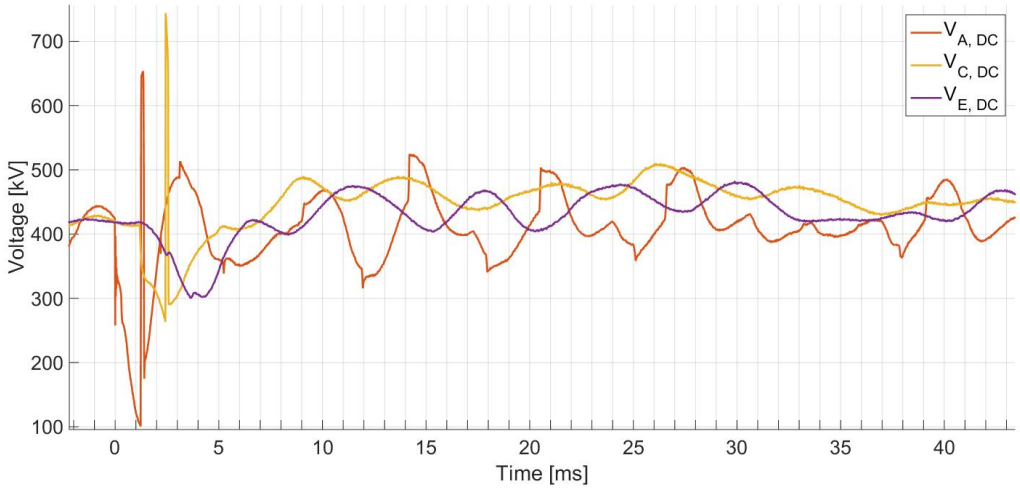


Figure 5.40: Voltages in the respective converters

MW power, and would have rise to much higher if not interrupted. The AC power production output is slowly acting, this is why it takes roughly 0.5 s from the fault until the power reaches a steady state.

The RMS voltage on each converter can be seen in Figure 5.43. It can be seen how the voltage goes towards zero, but the interruption of the fault current helps restoring the voltage.

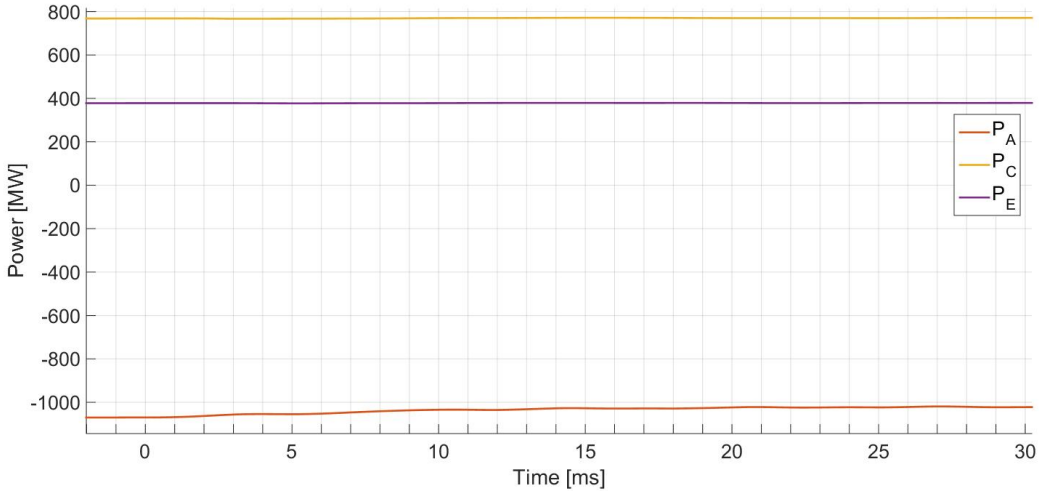


Figure 5.41: Power flow in the converters

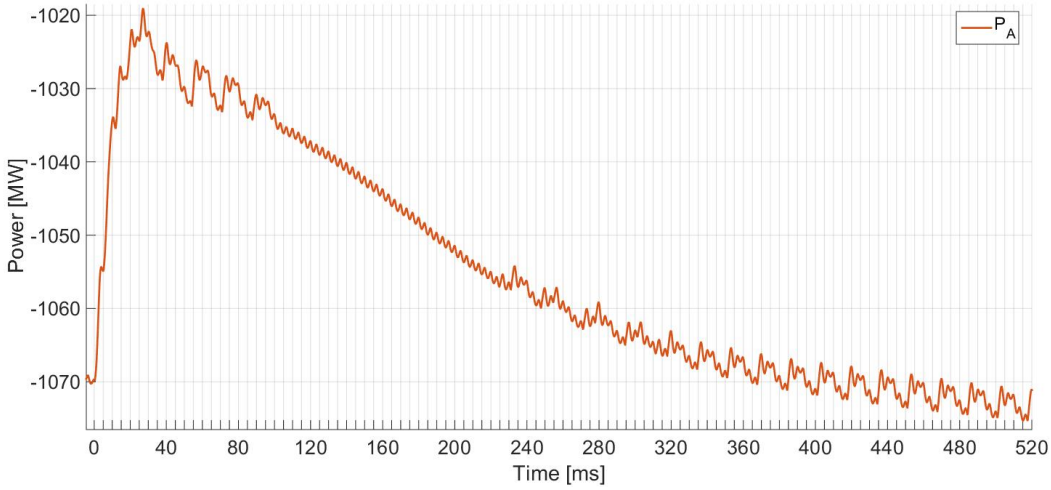


Figure 5.42: Power flow in the converters

5.5.5 Pole-to-pole fault, F1, With P-HCB

To compare the system behaviour with a longer interruption time, the P-HCB have been tested with the same fault and under the same conditions as for A-HCB in section 5.5.4. The operational times for the P-HCB is equal to those in section 5.1.2. In this section, only the CBs on the positive pole on the faulty line is illustrated since the negative pole CB will be equal to the positive pole CB except for a opposite current and voltage direction. The waveforms of the negative pole

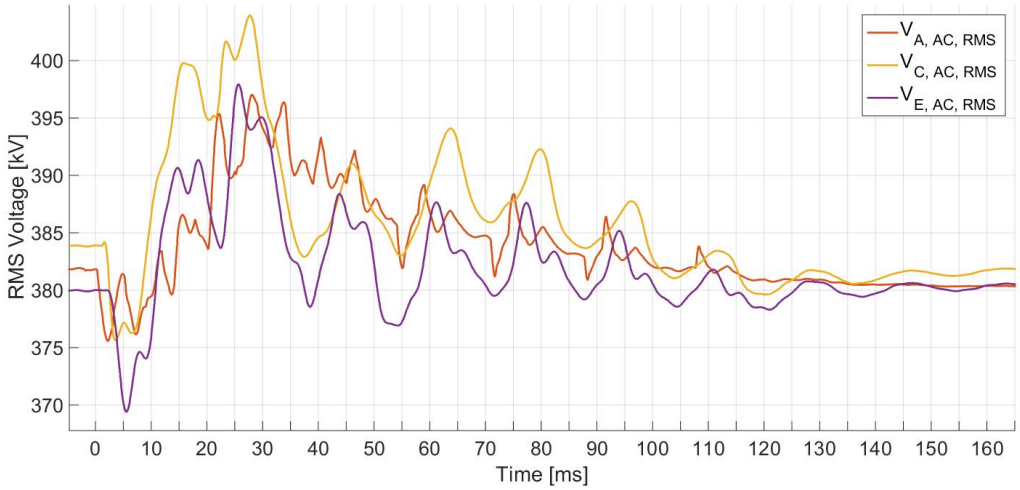


Figure 5.43: RMS voltage on the AC side of each converter

is illustrated in Appendix C.

AC-p

The current waveforms is illustrated in figure 5.44. It takes 1 ms after the contact separation for the arc to create a voltage drop that increases that across the commutation path. The arc resistance is illustrated in Figure 5.45. When this occurs, the current almost instantaneously commutates. The commutation path conducts the current until the mechanical switch is fully open, and have gained full dielectric strength.

Since the arrester have the same curve and voltage settings as for the AHCB, it will have approximately the same voltage. The voltage behaviour is illustrated in Figure 5.46.

The energy dissipated in the arrester can be seen in Figure 5.47, and is approximately 2000 kJ for the two arresters. The increase of the dissipated energy compared to the AHCB is due to increased interruption time. This phenomenon is explained in section 3.8.3.

CA-p

The 199 km distance from the fault location for CB CA-p, gives an delayed response to the fault. The waveform of current is shown in Figure 5.48. After the

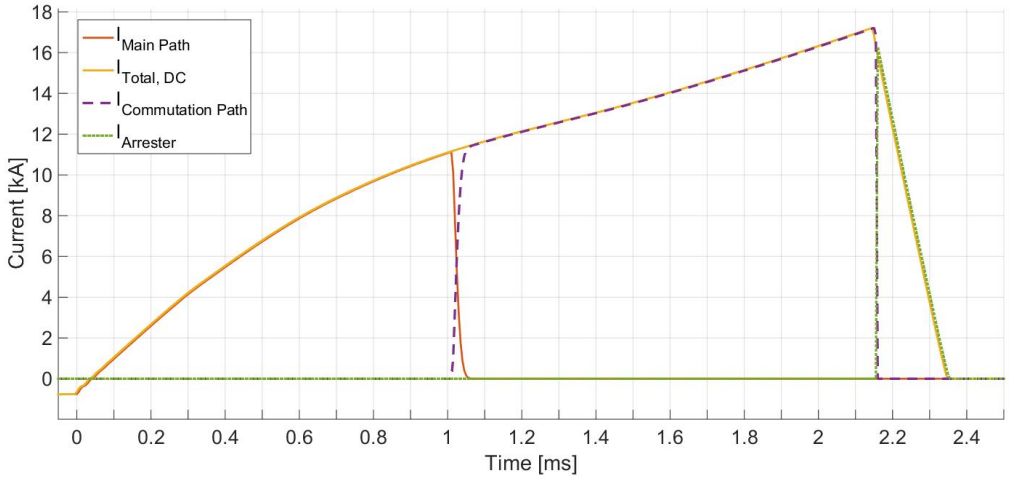


Figure 5.44: Current behaviour in AC-p

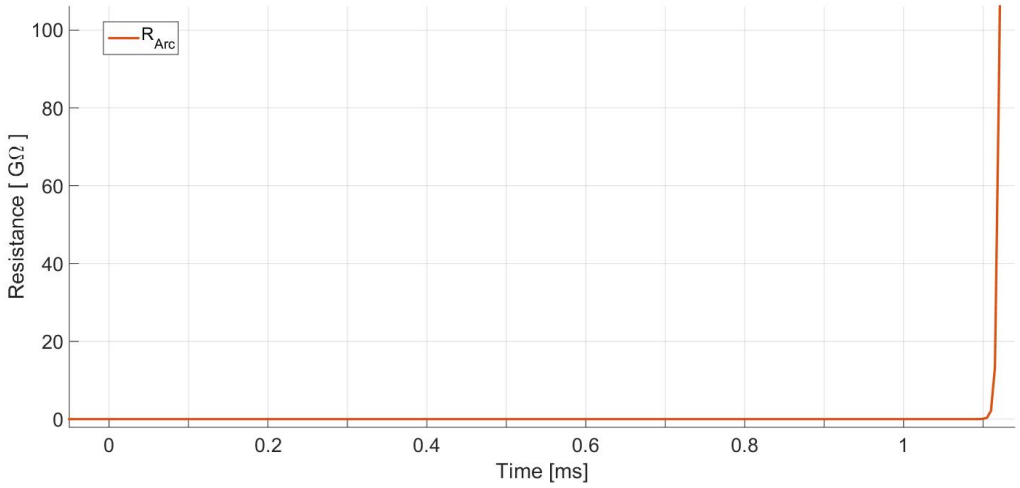


Figure 5.45: Resistance in AC-p

current commutation from by the arc, the total current magnitude $I_{Total,DC}$ is decreasing. This is due to the low current flowing in the adjacent cable. The fault current from converter A will flow in cable AE since this have half the length distance to the fault as the other way around.

The resistance of the arc is shown in figure 5.49, and show how the resistance goes towards infinity as the current is fully conducted by the commutation path.

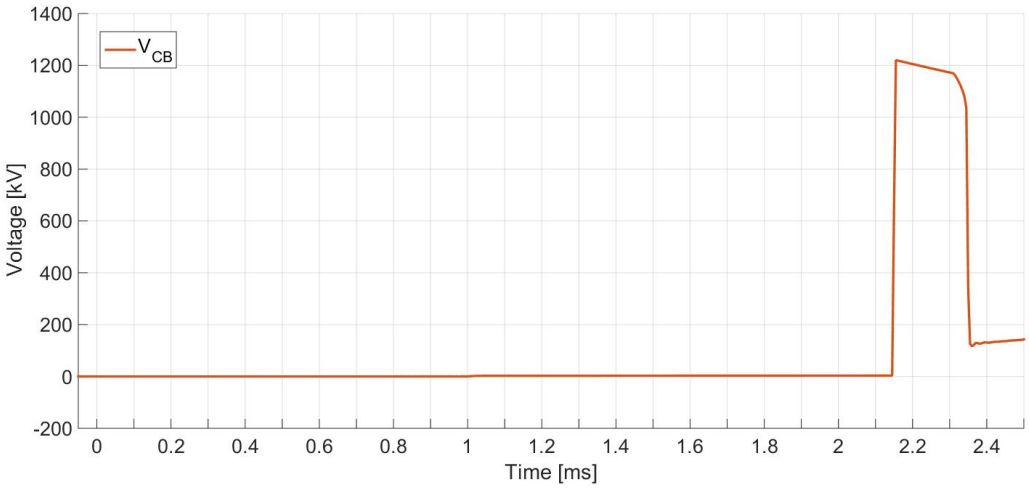


Figure 5.46: Voltage behaviour in AC-p

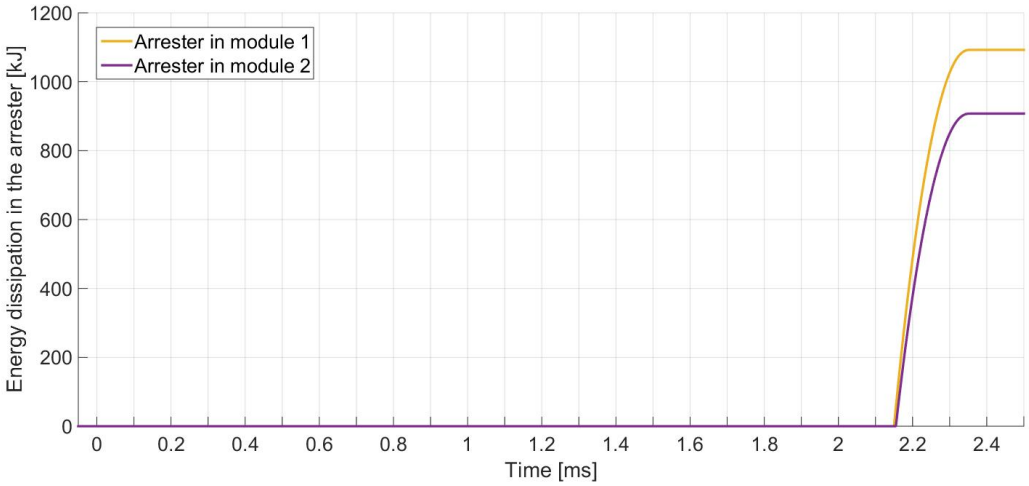


Figure 5.47: Energy behaviour in AC-p

The voltage across the CB is illustrated in Figure 5.50. The voltage across the CB will increase when the commutation math IGBTs turn-off. The voltage reaches 1200 kV, due to the settings of the arresters. When a current zero is achieved, the voltage will settle at the system voltage. The system voltage is ± 200 kV.

When the current zero is achieved, and the voltage drops to zero, the remnant energy will be dissipated by the arresters. The dissipated energy is shown in Figure 5.51.

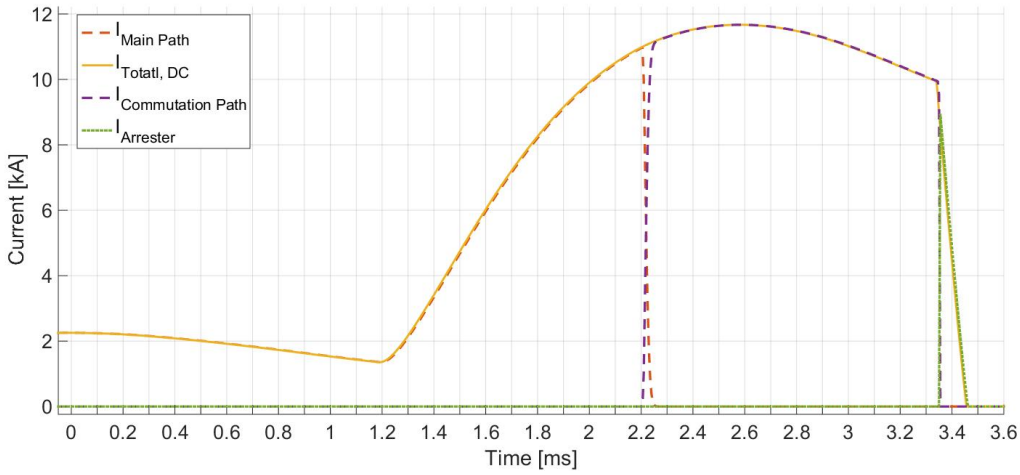


Figure 5.48: Current behaviour in CA-p

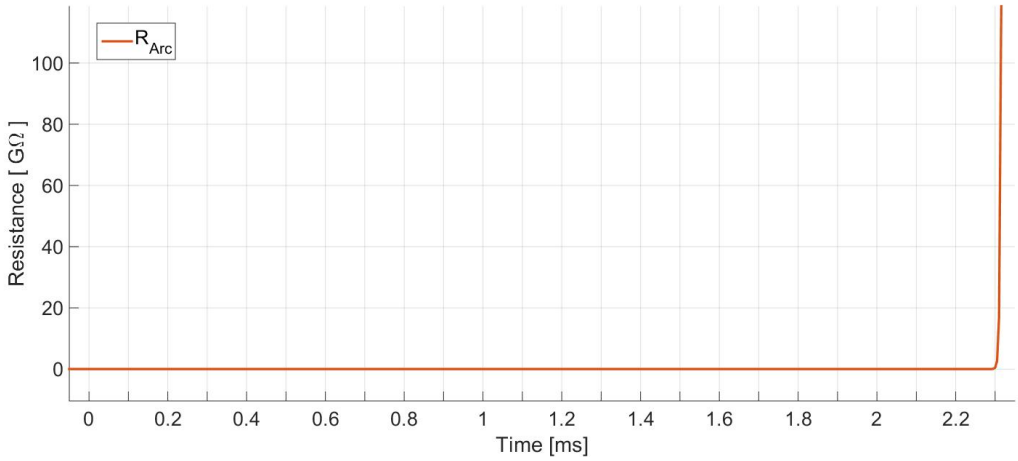


Figure 5.49: Arc resistance in CA-p

Power Flow

In Figure 5.52, the cables through all the positive cables can be seen. As expected the current flow, and thus the power flow is changed. The fault is isolated 3.5 ms after the fault occurs, and thus the current from converter C is directed to converter E, and through cable AE to converter A. This can be seen in the figure, as both AC-p an CA-p goes to zero, and the current through cable CE and AE increases. The current uses about 100 ms to reach a steady state.

The DC pole-to-pole voltage seen in Figure 5.53, behaves similar to the one in

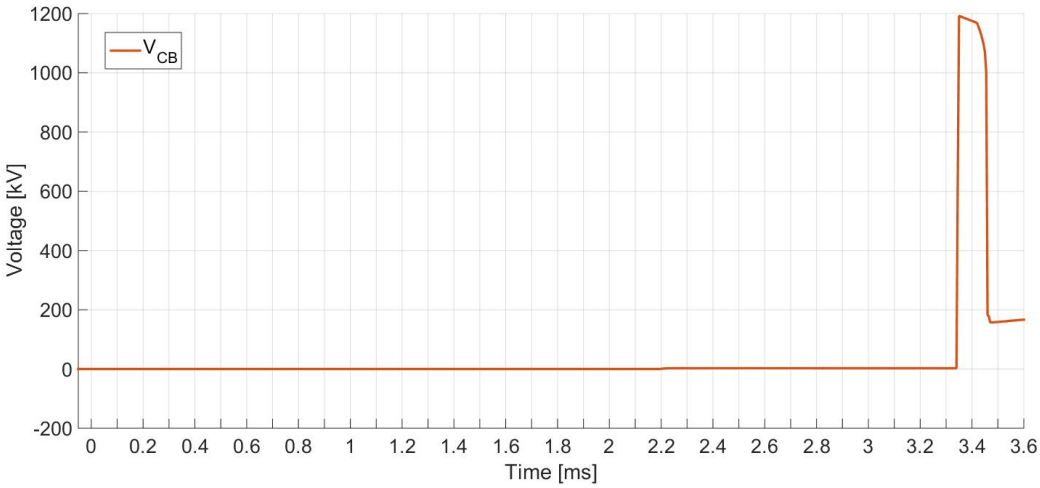


Figure 5.50: Voltage behaviour in CA-p

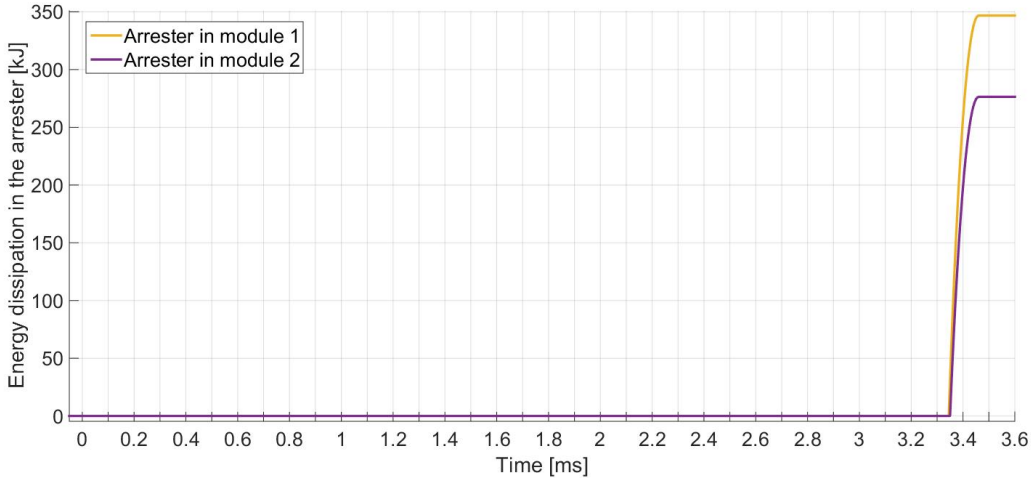


Figure 5.51: Energy behaviour in CA-p

section 5.5.4. It has stabilized at a steady state at 90-100 ms after the fault.

The power consumption at converter A, in Figure 5.54, also behaves in the same manner as for the AHCB in section5.5.4, but have a higher change in the consumption of power.

The RMS voltage is illustrated in Figure 5.55, and show how it changes after a proper fault interruption. The voltage is more or less equal is in section 5.5.4.

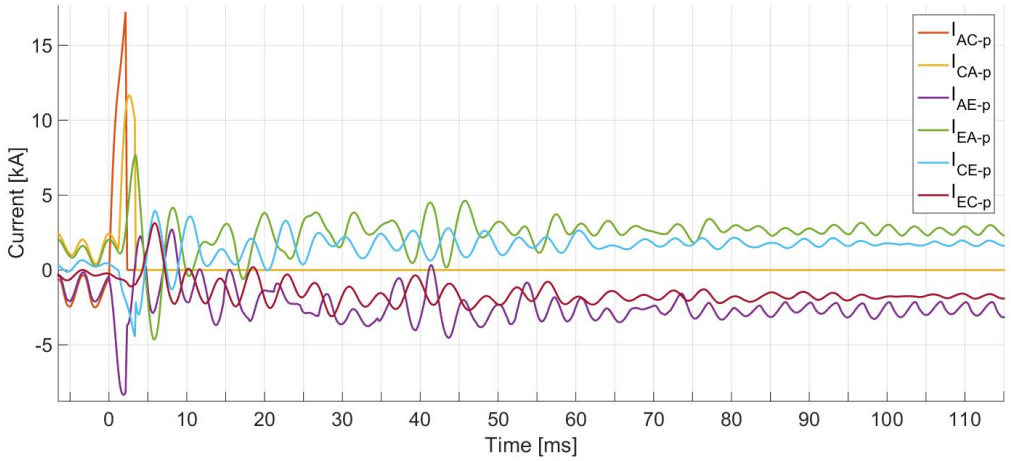


Figure 5.52: Current through the positive pole of the cables

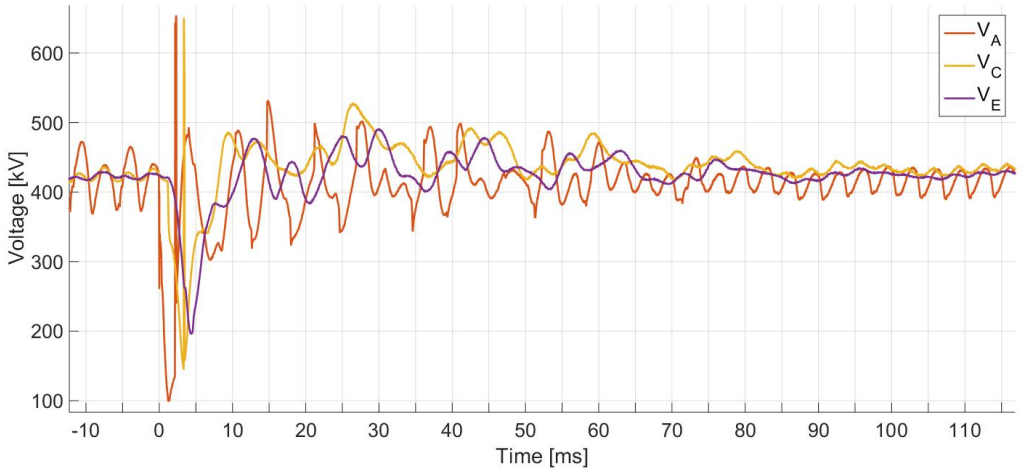


Figure 5.53: Pole to pole DC voltage at each converter

5.6 Discussion

The parameters selected for the hybrid CB are difficult to estimate. For a better idea of what values to select for the on-state voltage drop of the IGBTs, it is first calculated what voltages the IGBTs should be able to withstand. Based on this, the number of IGBTs are calculated, and it was found that a on-state voltage drop of 1.2 kV is close to the real value. This have not been added to the report, but only used as a reference basis. For the AHCB, the on-state voltage drop in the commutation path decides what off-state voltage the LCS must be able to

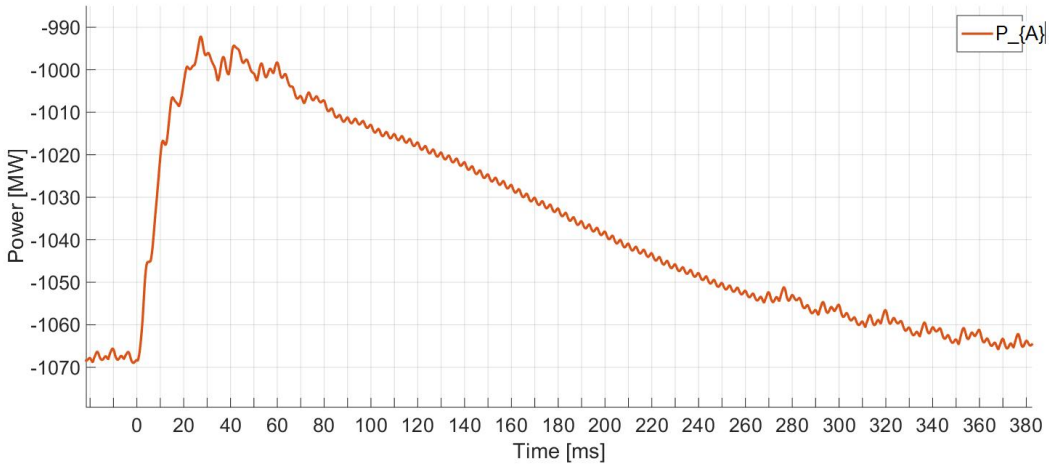


Figure 5.54: AC power production and consumption

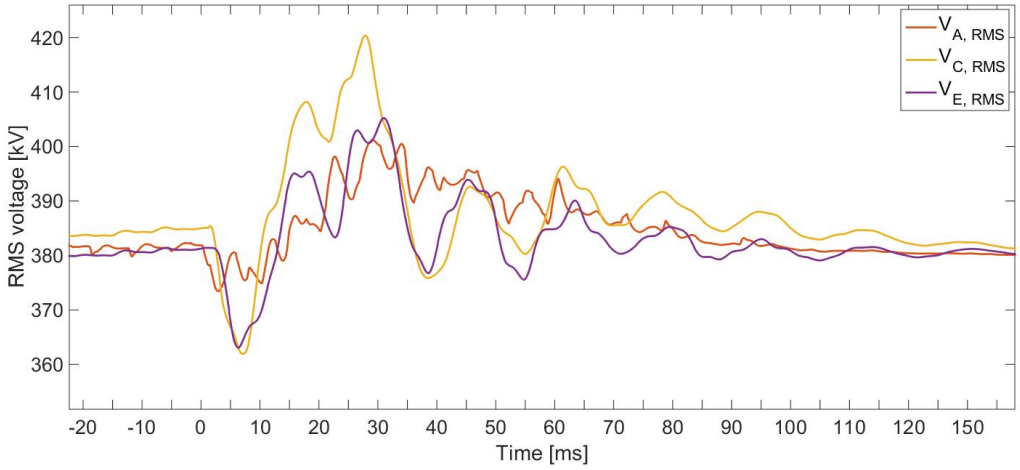


Figure 5.55: The RMS voltage at the AC side of each converter

withstand. The commutation path on-state voltage drop is also important for the time of commutation arc. It is therefore crucial to keep this voltage drop as low as possible. The hybrid CB model is provided by PSCAD, but are modified with the reaction times. It is chosen to use two modules of IGBTs and arrester. This gives the possibility for a faster and smoother interruption, but also for optimized setting of each module.

The parameters selected for the arcing model, presented in Figure 5.1 and 5.2, have been difficult to select. Therefore, the parameters used are mostly the same

as in [22]. The opening time of the nozzle have been changed, since [22] consider a slow acting disconnecter for resonant CB operation. The arc model is not implemented in the AHCB, since it is not the main commutating mechanism. However, in real operation the arc is a crucial part, since it will reduce the stresses on the LCS.

The methodology for testing the CB is divided in two parts; the component and system level. Reference system 1 gives a simple testing, but it does not have any DC side capacitor, nor any ripples in the current. The system does therefore not replicated the behaviour when a fault is applied. Using a variable resistance to replicate the short circuit fault, replicates the behaviour of the fault resistance in a good manner. The parameters used in the reference system 1 is provided by PSCAD, and are considered as similar to the real values.

Reference system 2 uses diode rectifiers, and were originally implemented to have more detailed look at the current behaviour. It proved difficult to make the current behaviour to act as expected. To obtain the expected behaviour, the capacitor values were set to unrealistic high values. In the end, the current behaviour turned out to be very similar to the current behaviour in reference system 1. The current plots were thus not included in this report. It is important to evaluate the temperature stresses that the rectifying diodes might experience. To estimate the temperature, the Cauer electro thermal model was used. This model and its parameters were not studied in detail, since the temperature estimation is only used for illustrative purposes. A more detailed study of the temperature in the diodes are required before a full scale implementation. For this case, the temperature of the diodes reaches critical levels within 20 ms after the fault occurs. The critical temperature for a diode is typically 120 $^{\circ}C$, but the time until this temperature is reached depends on the cooling of the diode and heat convection from nearby components.

To illustrate the need for a fast interruption, a comparison of interruption time have been made in Figure 5.15. This comparison is simulated in reference system 2, but the effect of increasing the interruption time is expected to be more or less equal.

Reference system 3 is a simplified part of the CIGRÉ B4 test system, and symmetrical in terms of cable length and current limiting inductor. These simplifications make it easier to understand the behaviour in the MTDC network. A fault located in either cable would look more or less similar, and the threshold for the detection mechanism is set to be equal for all CB. The detection method

is a well known method, and since it is not in the main focus of this thesis, it has thus not been thoroughly explained. Deciding the threshold in this symmetrical system is quite simple, since only two simulation is needed to find the threshold.

The simulation plots for the A-HCB and P-HCB in the MTDC network have been conducted with the same system parameters. It becomes clear that the interruption time do affect the system, both in terms of losses and remnant energy after fault interruption. As explained in section 3.8.3, the increased interruption time lowers the required voltage ratings of the arrester, and thus reducing the maximum voltage across the CB. This has not been taken into account for in this report, and the voltage ratings of the arresters are the same in each of the reference systems. The fastest interruption method is with the A-HCB, seen in section 5.5.4, and this results should be compared with those found in section 5.5.5. The interruption time for the P-HCB is almost twice as that for the A-HCB, this is illustrated by the increased fault current rushing to the fault location, and by the doubling of the energy to be dissipated. The current through the cables, power in the converters and voltages does not behave much different for the two different CBs.

Chapter 6

Conclusion

From the previous work in [8] it is concluded that the VSC and MMC technology is required in able to have fully controllable MTDC network. This is due its ability to control active and reactive power through independently.

It is proved that the hybrid CB topologies have a faster interruption time or less losses than the other topologies and are thus preferred for HVDC operation. The operational principle is thoroughly explained for both hybrid CB topologies.

The A-HCB uses a LCC in the nominal path, this allows for an active and fast fault current commutation, and a rapid interruption. The P-HCB on the other hand commutates the current by the arc, and are thus a slower commutation mechanism, but with almost none on-state losses.

The simulations of both models are based on the hybrid CB presented by ABB. This model is relative simple, and easier to understand. A real implementation of the hybrid CB should somehow have a structure like ALSTOMs mode, which allows for a gradual increase of the commutation path on-state voltage drop. This could especially prove important for the P-HCB.

The simulation of A-HCB and P-HCB shows what is expected. The A-HCB have a faster fault current commutation, and interruption of the fault current. The opening time of the LCS in both the A-HCB and P-HCB are the same, but P-HCB uses some time to complete the commutation. All simulations are based on the UFD technology, which gives the possibility for a faster disconnection of the contacts. This technology have relatively low voltage ratings (less than 12 kV), and can not by itself withstand the full voltage of the system. This is why the manufacturers consider the A-HCB as the best CB solution for HVDC application It is considered as the “weakest link” of the hybrid CB. The UFD is still under

development, and improvements are expected.

The detection method chosen in this report is the derivative of the current. This method was found to be easier to implement than some of the other methods. As it is illustrated in section 5.5.3, it becomes easier to distinguish between faults with an increased current limiting inductance. It is however important to keep the inductance as small as possible, to avoid stability issues.

The interruption and isolation of the fault is illustrated for two cases, with the same fault location and size, but with different hybrid CBs. The waveforms of the CBs are quite straight forward, and it is illustrated that they work as expected. The interesting simulations is to see how the system reacts to the fault, and redirects through adjacent cables. It does so for both the CBs, but at least 1 ms faster for the A-HCB.

Based on the result obtained in this report, and based on the fact that the UFD has low voltage ratings, the only viable operation for MTDC application is a A-HCB.

Chapter 7

Further Work

There are several studies to be conducted for the grid companies to realise the potential of an MTDC network. First there must be made a full-scale hybrid CB, that can handle the high fault currents that might occur. At writing moment, the UFD is the limiting component, since it may only interrupt a 4.5 kA current at the highest, making it a load break switch and not a CB. There have not been many studies on the affect of the electric arc on PE in the parallel path, and the ripples and harmonics this phenomenon might cause. The life cycle of the arrester should be thoroughly investigated, and the snubber circuit as well. As can be seen there are a lot of future work to be done in the field of the hybrid CB.

- Unsymmetrical MTDC network, and different inductor sizes
- Snubber circuit
- Effect of harmonics
- Full scale model and testing
- Investigate the fault handling for a MMC full-bridge
- Investigate a MTDC OHL network

Appendix A

Effect of changing the fault resistance

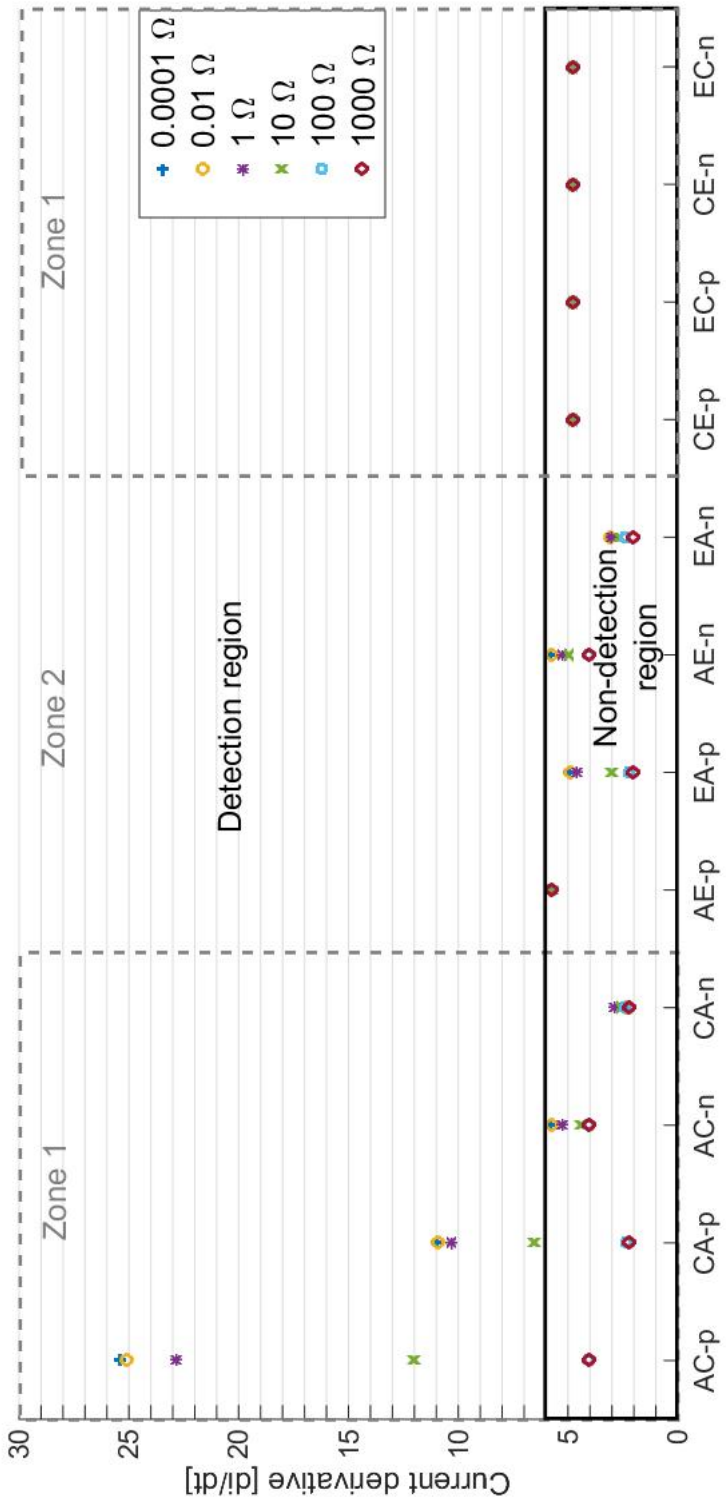


Figure A.1: Fault on cable AC, close to converter A

Appendix B

Pole-to-pole, F1, with A-HCB for the negative pole CB

AC-n

CA-n

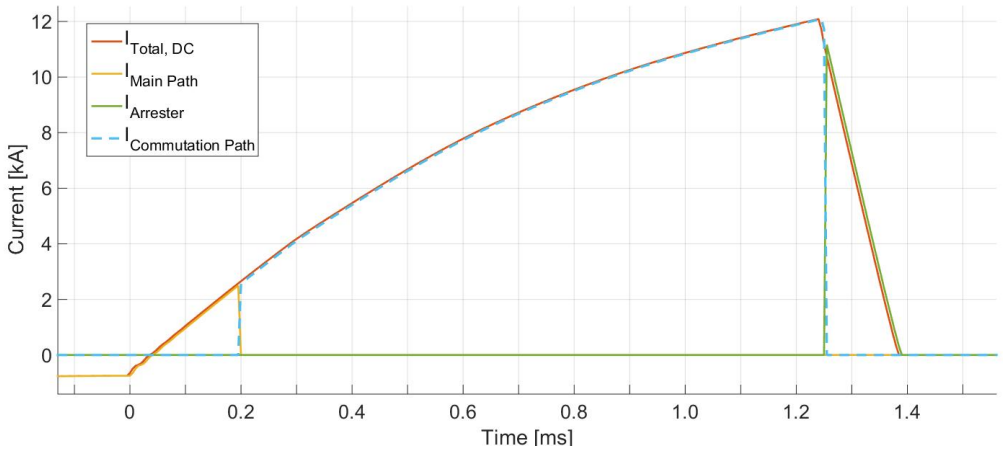


Figure B.1: Current behaviour in AC-n

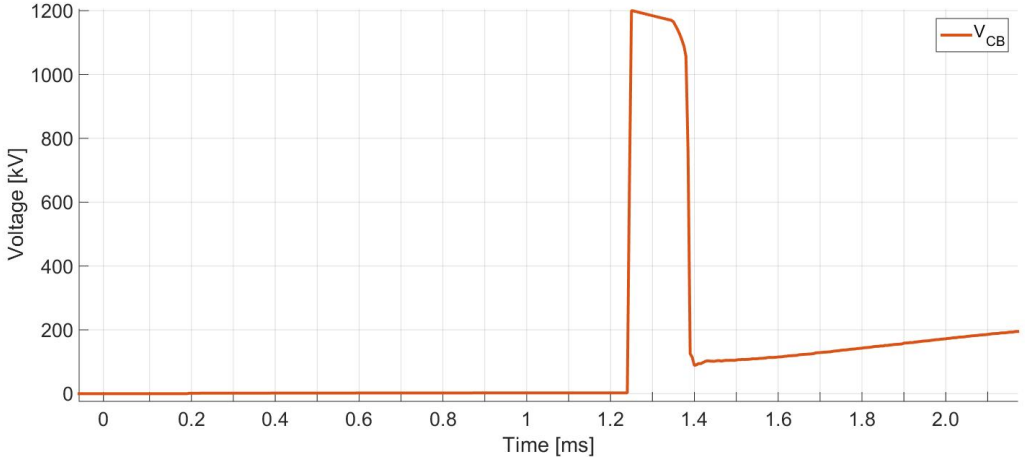


Figure B.2: Voltage behaviour in AC-n

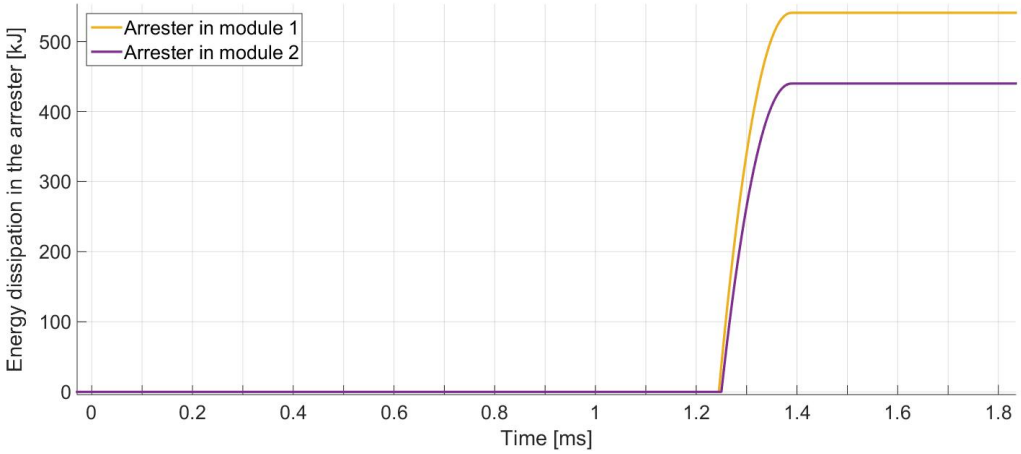


Figure B.3: Energy behaviour in AC-n

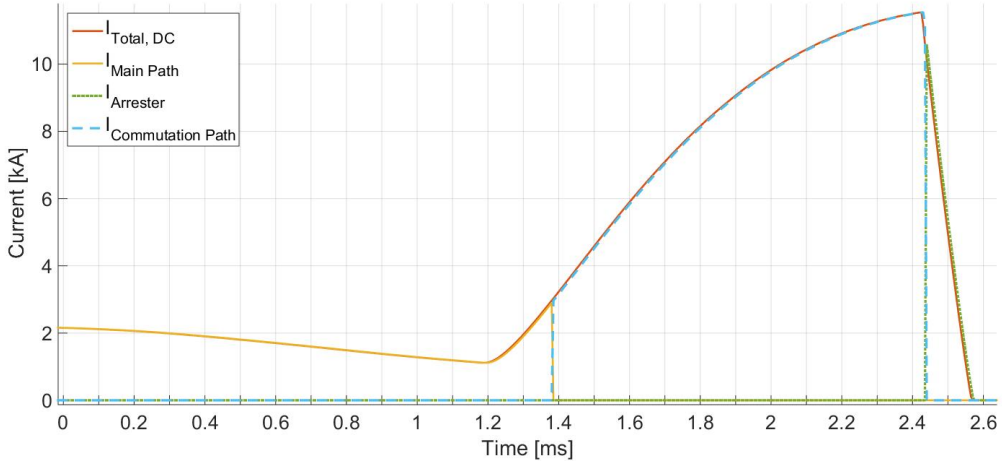


Figure B.4: Current behaviour in CA-n

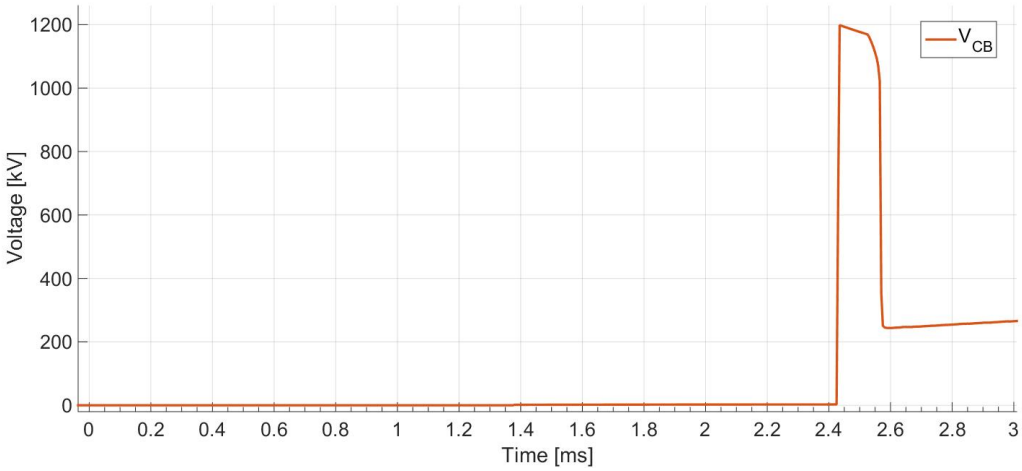


Figure B.5: Voltage behaviour in CA-n

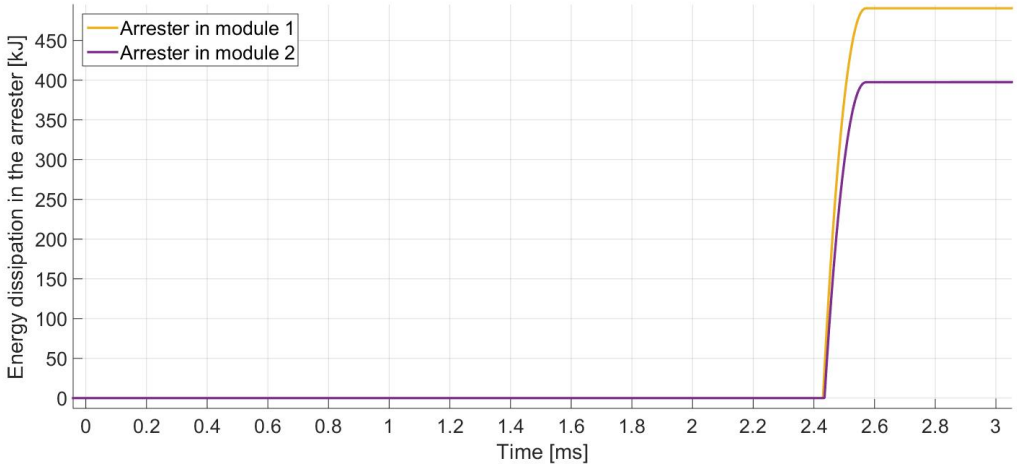


Figure B.6: Energy behaviour in CA-n

Appendix C

Pole-to-pole, F1, with P-HCB, negative pole CB

AC-n

CA-n

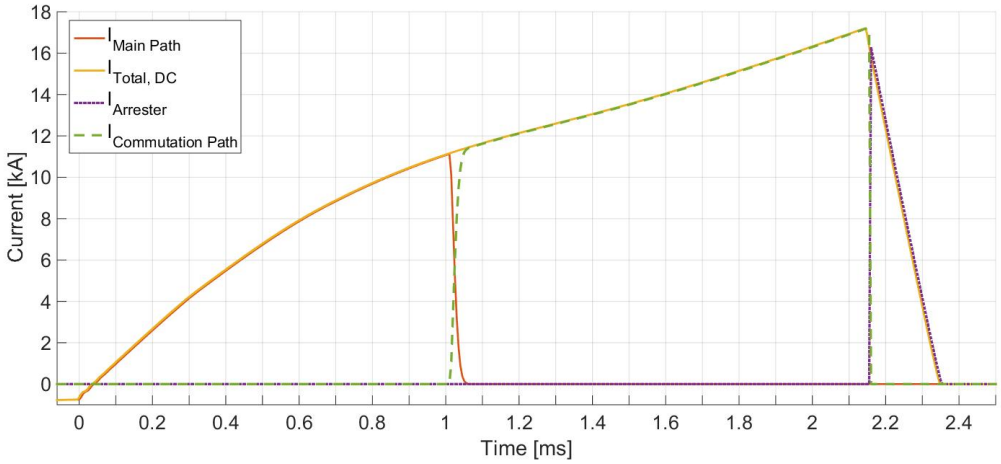


Figure C.1: Current behaviour in AC-n

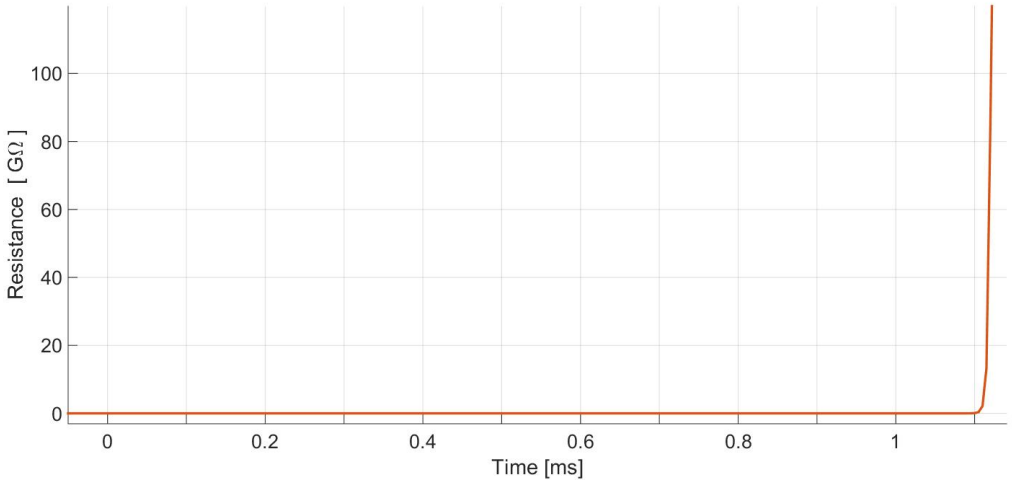


Figure C.2: Resistance in AC-n

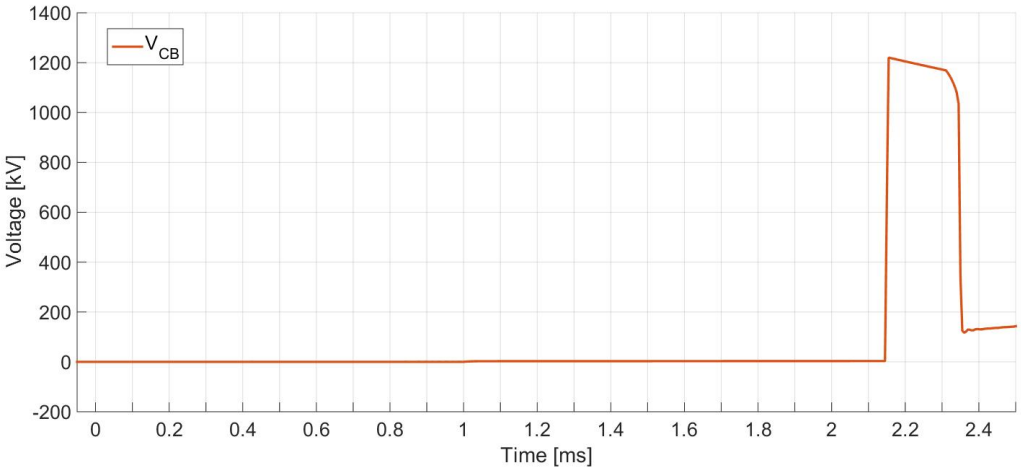


Figure C.3: Voltage behaviour in AC-n

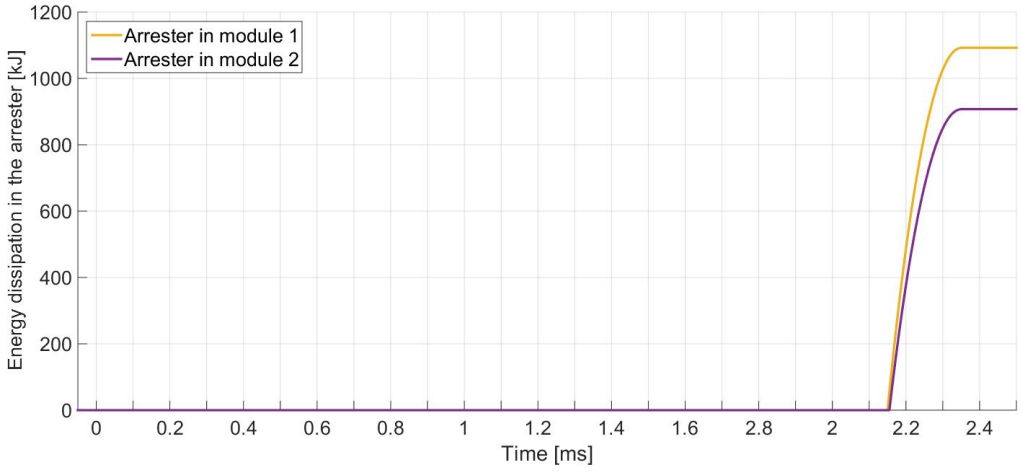


Figure C.4: Energy behaviour in AC-n

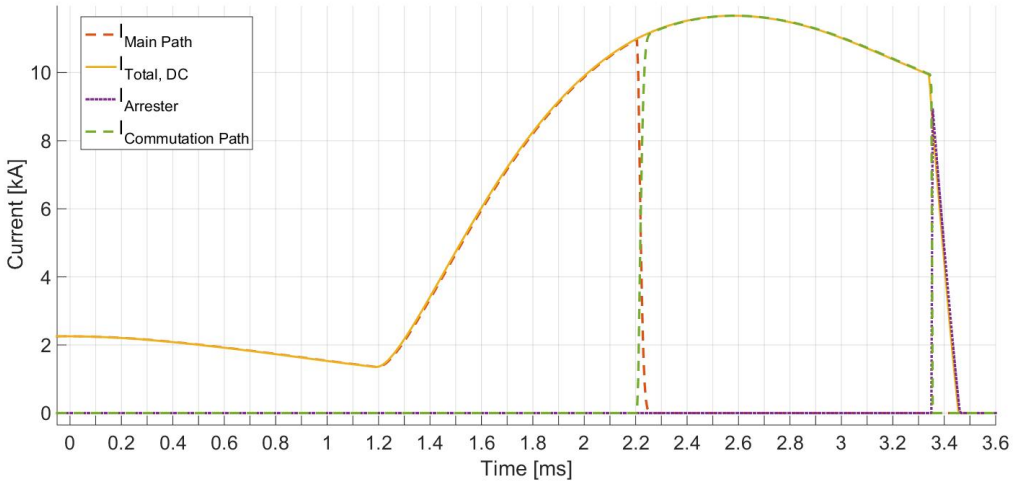


Figure C.5: Current behaviour in CA-n

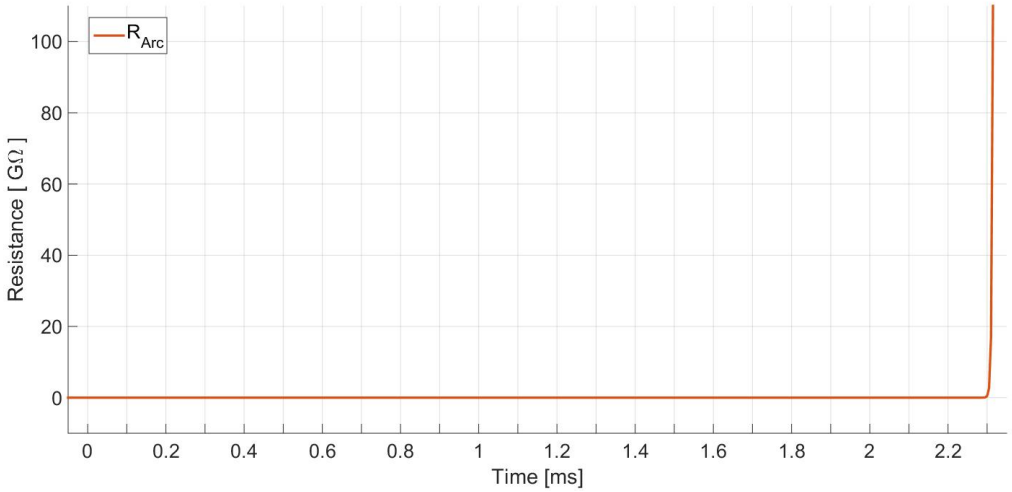


Figure C.6: Resistance in CA-n

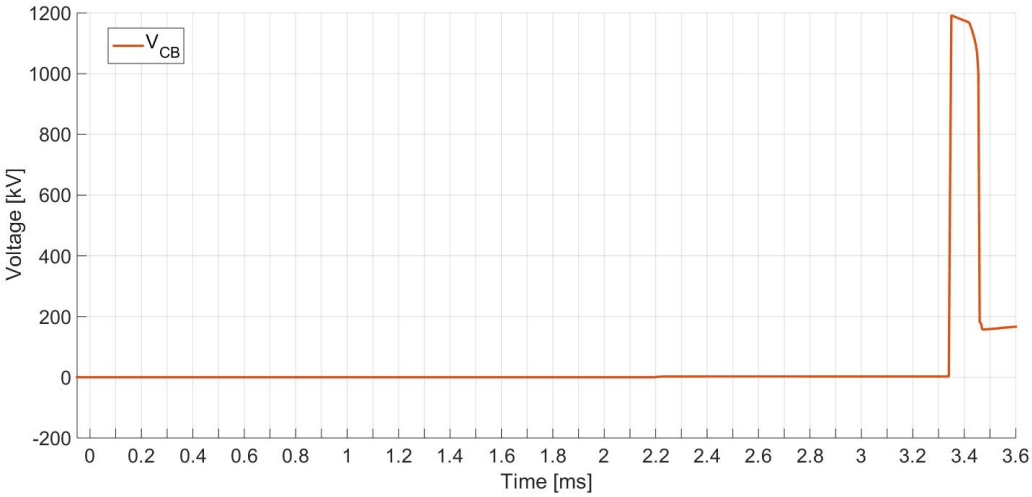


Figure C.7: Voltage behaviour in CA-n

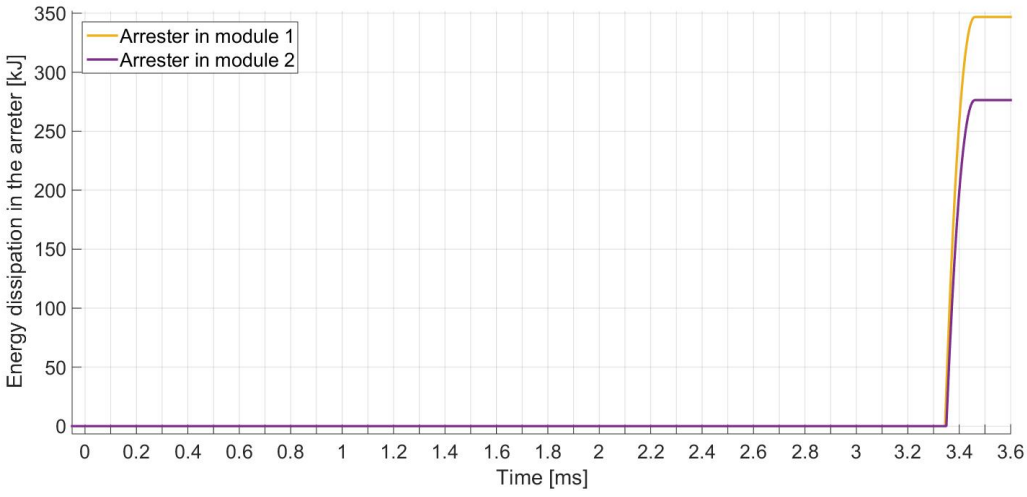


Figure C.8: Energy behaviour in CA-n

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