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Wideband, Robust Low Noise Amplifier

Magnus Nøkleby Pedersen

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Supervisor: Morten Olavsbråten, IES

Norwegian University of Science and Technology
Department of Electronic Systems

Assignment description

Assignment title: Wideband, Robust Low Noise Amplifier

KONGSBERG provides reconfigurable communication systems in challenging environments (maritime and military) in addition to multiple other business areas. One area of specific interest is autonomous vehicles and this Master Thesis looks into some of the areas related to the communication between autonomous vehicles. Autonomous vehicles may require multiband, multi-waveform communication equipment and they should be reconfigurable. Modern software defined radio systems can meet this requirement, but a limiting factor is the RF front end, which have to have both a wide RF-bandwidth and be robust. One answer to this challenge is the development of GaN MMIC.

An earlier project looked into using the Wolfspeed CGH40006S discrete GaN transistor for a low noise amplifier in the 4400 - 5000MHz band. This was discontinued as the noise figure became too high. One alternative is to use the Cree/Wolfspeed GaN MMIC G40V4-process for a LNA design. The LNA should provide more than 13dB gain over the 1.3 - 5.8GHz band to cover most LTE bands as well as Wi-Fi and the noise figure should be less than 2dB. Look into possible wide band configurations and make an evaluation of the noise figure capability of the mentioned process.

Table 1: Specifications.

Frequency	1.3 - 5.8 GHz
Gain	$>$ 13dB
Noise figure	$<$ 2dB
Linearity	Best possible

Summary

Low noise amplifiers are important parts of receiver units in radio systems that enables communication between military vehicles. The use of such an amplifier in military and maritime equipment poses challenges to the robustness of the amplifier. This report deals with the design and simulations of a low noise amplifier using the robust GaN MMIC GH25-10 process from Wolfspeed. It is specified that such an amplifier should deliver more than 13dB gain and have less than 2dB in noise figure for a 1.3 - 5.8GHz frequency band. Simulations of the amplifier in Keysight's Advanced Design System shows a maximum gain of 33.8dB at 1.3GHz while a minimum of 13.9dB is located at 5.8GHz. The noise figure demonstrates to be 1.68dB at most for 5.8GHz with a minimum of 1.08dB at 1.8GHz. The designed amplifier is also found to be unconditional stable from simulations. Intermodulation distortion is simulated in a two-tone test marking the linearity of the amplifier, while the output power is simulated in a single-tone test. To give an idea of robustness, there have been done simulations that shows at which input powers the amplifier reaches maximum ratings of the gate current, gate-source voltage and drain-source voltage. Junction temperature is simulated for different input powers with an ambient temperature of 85°C for both transistors to further prove the robustness. Finally, the work has resulted in a layout that has been tested through an electromagnetic simulation. The results of this last simulation matches the previously simulated values for noise figure, gain and stability.

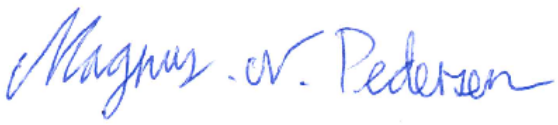
Sammendrag

Lavstøyforsterkeren er en viktig blokk i mottakerenheten i et radiosystem for kommunikasjon mellom militære kjøretøy. Ved bruk i militære og maritime miljøer blir robusthet en utfordring for en slik forsterker. Denne rapporten tar for seg design og simuleringer av en lavstøyforsterker hvor man benytter seg av den robuste GaN MMIC GH25-10-prosessen til Wolfspeed. Det er spesifisert at en slik forsterker bør levere mer enn 13dB forsterkning og ha mindre enn 2dB i støyfigur for båndet 1.3 - 5.8GHz. Ved simuleringer i Keysight's Advanced Design System blir det funnet en maksimal forsterkning på 33.8dB ved 1.3GHz og et minimum på 13.9dB ved 5.8GHz. Støyfiguren simuleres til å ha et maksimum på 1.68dB for 5.8GHz med et minimum på 1.08dB ved 1.8GHz. Lavstøyforsterkeren er designet med stabiliseringskretser slik at man oppnår ubetinget stabilitet i småsignalsimuleringer. Som et mål på forsterkerens linearitet simuleres intermodulasjonsstøy i en to-tone-test, mens utgangseffekten simuleres i en én-tone-test. For å gi en pekepinn på forsterkerens robusthet, utføres det simuleringer for å vise ved hvilke effekter forsterkeren oppnår satte maksverdier for strømmen målt ved gate, spenningen målt over gate-source og spenningen over drain-source. Ved å sveipe inngangseffekten til forsterkeren blir også junction-temperaturene for de to transistorene simulert. Arbeidet resulterer i en layout som testes gjennom en elektromagnetisk simulering, for å inkludere eventuelle induktive koblinger mellom komponenter. Resultatene fra denne simuleringen stemmer godt overens med tidligere simulerte verdier for støy, forsterkning og stabilitet.

Preface

This master thesis was carried out the spring semester of 2018 in association with the Department of Electronic Systems at the Norwegian University of Science and Technology (NTNU). Associate professor Morten Olavsbråten has provided guidance and help with the thesis. The assignment was formulated by Kongsberg Defence & Aerospace, which has submitted input on the assignment through meetings during the work. It is assumed that the reader has basic knowledge within amplifiers and electronical engineering.

24-06-2018, Trondheim



Magnus Nøkleby Pedersen

Acknowledgment

First, I would like to thank Kongsberg Defence & Aerospace for giving me the opportunity to work with this assignment and for follow up on my work via Skype during the designing phase. I would also like to thank my supervisor Morten Olavsbråten for valuable guidance with the thesis. The conversations during the semester on different approaches to the assignment and input on which steps to take forward have been very useful.
Lastly, I would like to thank all the friends I have made at NTNU and in Trondheim during my time in the city. Thanks to them, it has been a pleasure to be a student during the five years of this master's degree.

M.N.P.

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Abbreviations

2DEG	=	Two-dimensional electron gas
ADS	=	Advanced Design System
AlGaN	=	Aluminium gallium nitride
BGR	=	Bandgap Voltage Reference
dBc	=	Decibel referenced to carrier
DRC	=	Design Rule Check
EM	=	Electromagnetic
FET	=	Field-effect transistor
GaN	=	Gallium Nitrid
GaaS	=	Gallium Arsenid
HEMT	=	High-electron-mobility transistor
I-V	=	Current-voltage
IMD	=	Intermodulation distortion
IMD3	=	Third-order intermodulation distortion
IP3	=	Third-order intercept point
LNA	=	Low Noise Amplifier
MAG	=	Maximum Available Gain
MESFET	=	Metalsemiconductor field-effect transistor
MIM	=	Metal-insulator-metal
MMIC	=	Microwave Monolithic Integrated Circuit
NFmin	=	Minimum Noise Figure
UMS	=	United Monolithic Semiconductors

Chapter 1

Introduction

The development of electronic circuits for military vehicles and devices often places strict demands on robustness. In the communication between such vehicles, the RF front end may be a limiting part of the system. It is desirable that this part is both robust and wideband, which can be a challenge to obtain. It has previously been common to use Gallium Arsenid (GaAs) to create integrated RF circuits due to transistor speed, but the technology has gradually developed and Gallium Nitrid (GaN) has rised as an alternative to use for Microwave Monolithic Integrated Circuit (MMIC). High electron mobility, high breakdown voltage and operation at high temperatures has made GaN a preferred option for MMIC in systems that require robustness [2], [3].

The use of GaN gives the benefit of reduced need of additional protection circuits and thus reduces the complexity of the receiver. Another advantage of this is the reduction in noise level [4]. This is especially beneficial in the design of a low-noise amplifier (LNA) intended for integration into a radio receiver. The LNA is responsible for amplifying a weak signal that is received by the antenna. In the case of amplification it is highly desirable that the noise level is kept low. The LNA is usually one of the first blocks in a receiver and should therefore add minimal noise to keep the signal above the noise level in the following stages in the receiver.

1.1 Objectives

This thesis investigates the noise performance and robustness of the GaN MMIC G40V4-process from Wolfspeed. There will be designed a low noise amplifier using the CAD software Advanced Design System (ADS) provided by Keysight. The amplifier will be designed using two stages to achieve gain higher than 13dB while holding the noise figure below 2dB. This will apply to the bandwidth 1.3 - 5.8GHz to cover WiFi and most LTE bands. As there is not specified any gain flatness, the only focus on gain will be to exceed 13dB. The amplifier will be simulated for robustness in terms of maximum ratings and power handling. Linearity will be simulated using both single and two-tone analysis, while properties as gain and noise figure will be simulated in a small-signal analysis. In the end, there will be made a layout which will be verified in electromagnetic (EM) simulations.

1.2 Overview of Report

This section summarizes the structure for the rest of the report.

- Chapter 2 provides theory and relevant background. The technology will be presented as well as relevant theory for the design and analysis of the amplifier.
- Chapter 3 will go through the design stages which will result in a layout in the end.
- Chapter 4 presents results from simulations.
- Chapter 5 discusses the results from Chapter 4 and the design choices in Chapter 3.
- Chapter 6 concludes the report and sums up the obtained results. It will also look into possible future work with the amplifier.

Chapter 2

Theory

2.1 Technology

This subsection provides a short background on the technology that will be used for the amplifier.

2.1.1 GaN

Gallium nitride (GaN) is a semiconductor material consisting of Gallium and Nitrogen. GaN is a wide bandgap material meaning that there exists a large area with no permissible energy levels. This allows electrical properties in the bed between a typical insulator and a typical semiconductor. The wide bandgap causes GaN to have high breakdown voltages, thus it requires high voltage before the GaN device deviates from normal operation. This also gives higher operating temperatures. GaN allows operation at higher frequencies as the high carrier mobility will cause the electrons to move fast through the material [5].

2.1.2 HEMT

A High-electron-mobility tranistor (HEMT) is built up in the same way as a metalsemiconductor field-effect transistor (MESFET). It has a n-doped channel with contacts for drain and source, while the metal for the gate lies directly on the channel making a Schottky-barrier. In contrast to the MESFET, the channel is made up by using layers of different materials. The two different materials form a two-dimensional layer where the electrons can have very high

mobility [2]. The materials have different band gaps, which means that a two-dimensional electron gas (2DEG) will move vertically. A combination of GaN and Aluminium gallium nitride (AlGaN) is of growing popularity as high-power performance is desired.

2.1.3 MMIC

In a Monolithic Microwave Integrated Circuit (MMIC) all active and passive components are based on the same semiconducting substrate (monolithic). This leads to smooth transitions between components and minimal loss for this types of circuit. The frequency range is as microwave indicates in the range 300 MHz to 300 GHz. The high frequencies make the transmission lines short and result in a small chip size with low weight. The first fabrication of an MMIC chip can be costly as the entire circuit must be manufactured before the functionality can be verified. On the other hand, MMIC fits well with mass production as all components will be related to the same physical parameters, in comparison to hybrid microwave integrated circuits that will experience chip-to-chip variations [6].

2.2 Components

This subsection will give a brief overview of the models of components that are included in the Wolfspeed library.

Transistor

The chosen transistor for this project is the G40v4 HEMT based on a 0.25 μm gate. The G40V4 has been validated for the following set of data:

Table 2.1: Recommended ranges for the Wolfspeed G40v4 HEMT model [1].

Frequency	DC - 18 GHz
Drain voltage bias	6 V to 84 V
Gate-source voltage	-8 V to 2 V
Maximum Junction Temperature	225°C

The gate-source breakdown voltage is stated to be -8V, while the drain-source breakdown voltage is declared to be 84V. The maximum forward gate DC current is 1 mA/mm.

Resistor

The type of resistor that is used for the project is a Bandgap Voltage Reference (BGR) resistor. This is validated with a peak current of 0.2 mA/μm and with a minimum width of 10 μm. The typical sheet resistance is stated to be 415 Ω/square [1]. Figure 2.1 shows the model of this resistor.

Figure 2.1: BGR resistor from the Wolfspeed library.

Capacitor

Wolfspeed provides metal-insulator-metal (MIM) capacitors which are formed by two parallel plates insulated by a dielectric layer in-between. The MIM capacitors that are to be used in this design have a typical capacitance density of 180 pF/mm^2. Such a capacitor can be seen in Figure 2.2 below. The provided model is valid with a maximum DC+RF voltage of 100 V and a RF current density of 0.35 mA/μm^2 [1].

Figure 2.2: MIM capacitor from the Wolfspeed library.

Inductor

The model for the rectangular spiral inductors that are to be used in the amplifier is wired in the METAL1 material. Thus, the maximum DC current through the spiral is 15 mA/μm [1]. The minimum width of METAL1 is stated to be 6 μm. Figure 2.3 shows the provided spiral inductor.

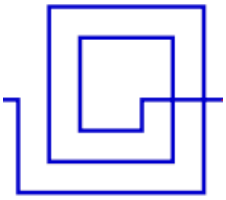


Figure 2.3: Spiral inductor from the Wolfspeed library.

Microstrip

Some parameters have to be included in ADS by using the process variable controller in order to simulate microstrip lines. The values that are included in the process variable controller are summarized in Table 2.2 below.

Table 2.2: Definition of substrate parameters.

H [μm]	Cond [$\cdot 10^7$]	TanD	Rs [Ω / $\square$]	Cpua [pF/mm^2]
100	3.7	1.0e-4	12	180

The significance of these data is illustrated in Figure 2.4, together with the length and width of a microstrip line.

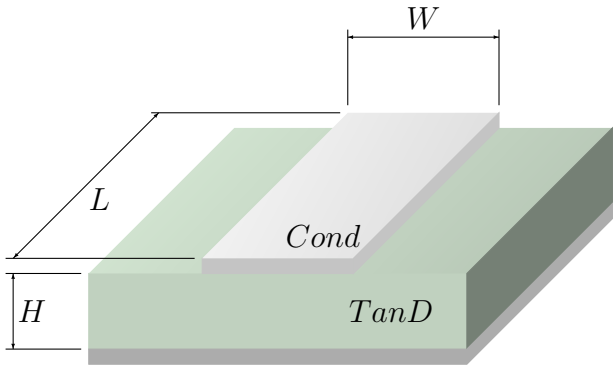


Figure 2.4: Structure of a microstrip line.

The parameter H is the thickness of the substrate. $Cond$ is the conductivity of the conductor, while $TanD$ is the dielectric loss tangent. Rs is the sheet resistivity stated in Ohm per square and $Cpua$ indicates the capacitance per unit area.

2.3 Biasing

The biasing of a transistor is determined by two things; the choice of bias point and the bias network. The bias network will be treated as a part of the matching network in Section 2.9, while the choice of quiescent point will be discussed in this section. The choice of bias point is important in an amplifier because it is of great importance to the amplifier's characteristic.

Usually one can use an IV-characteristic for choosing a quiescent point. A challenge is to maintain constant current as the transistor will explore process and temperature variations. An IV-characteristic like Figure 2.5 can be divided into two regions. The linear region is the operating region for passive components with loss. Transistors used for amplification are usually biased in the saturation region which provides gain and power.

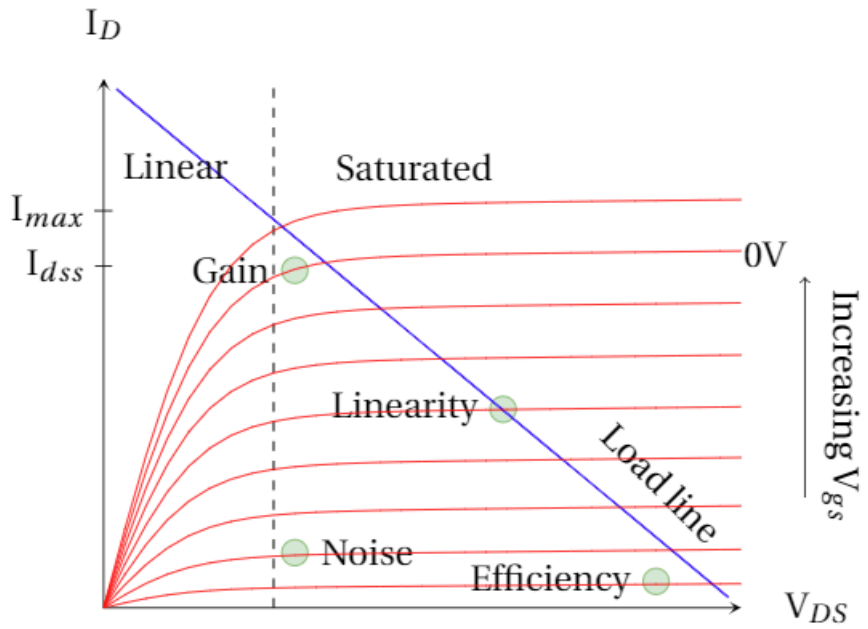


Figure 2.5: IV-curves with different bias points, amplifier properties and a load line.

The I_{max} line in Figure 2.5 represents the maximum drain current which occurs at positive gate-source voltage in the saturated region. I_{dss} is the saturated current when the gate-source voltage is zero.

The intended application of the transistor determines the selection of bias point. It is common to have a high V_{ds} and high I_{ds} for maximum power application. The drain voltage is often

reduced in cases where low noise is of more importance. Drain voltage can be chosen based on recommendations from the foundry and preferably with a value that fits well for system integration. The choice of gate-source voltage is dependent on the desired behaviour in terms of efficiency, gain, noise and linearity. The ideal bias point for the different properties are plotted in Figure 2.5. For low-noise performance, the gate-source voltage is commonly low so that the current I_{ds} is minimized.

2.4 Linearity

An amplifier is considered linear when the output power increases proportionally to the input power, or when the power gain is kept constant with increasing input power. As the input power increases, the device will reach its maximum power level depending on its size. The transfer function of the amplifier will be nonlinear and one will eventually reach a point where the output power will no longer increase with the input power. As mixing occurs, there may exist more than one carrier frequency in a non-linear amplifier. This will cause multiple sidebands to be generated as intermodulation products. The combination of amplitude modulation in one step and AM to PM conversion in another step is another source to intermodulation distortion.

2.4.1 Single-tone test

A simple method of measuring the linearity of the amplifier is to see when the output power deviates with 1dB from the input power. This is called the 1dB compression point and can be found by performing a single-tone test. The singel-tone test supplies the input of the amplifier with a single tone with frequency ω_0 and amplitude V_0, described in Equation 2.1.

$$v_{in}(t) = V_0 \cos(\omega_0 t) \tag{2.1}$$

The output can be modelled as a power series, reduced to three terms in Equation 2.2 due to complexity.

$$v_{out}(t) = a_0 + a_1 v_{in}(t) + a_2 v_{in}^2(t) + a_3 v_{in}^2(t) \tag{2.2}$$

where the coefficients are calculated using Equation 2.3.

$$a_i = \frac{\partial v_{out}}{\partial v_{in}^i}|_{v_{in}=0} \tag{2.3}$$

By the use of Equation 2.2, we obtain the voltage gain for the fundamental frequency, ω_0 [7].

$$G_v = a_1 + \frac{3}{4}a_3 V_0^2 \tag{2.4}$$

In practice, a_3 will be negative so that the gain will decrease for large values of V_0. This is referred to as gain compression.

The singel-tone test shows how the gain and output power act when there are nonlinearities in the circuit. The effect of these nonlinearities can be observed in how the curve of the output power in Figure 2.6 becomes nonlinear.

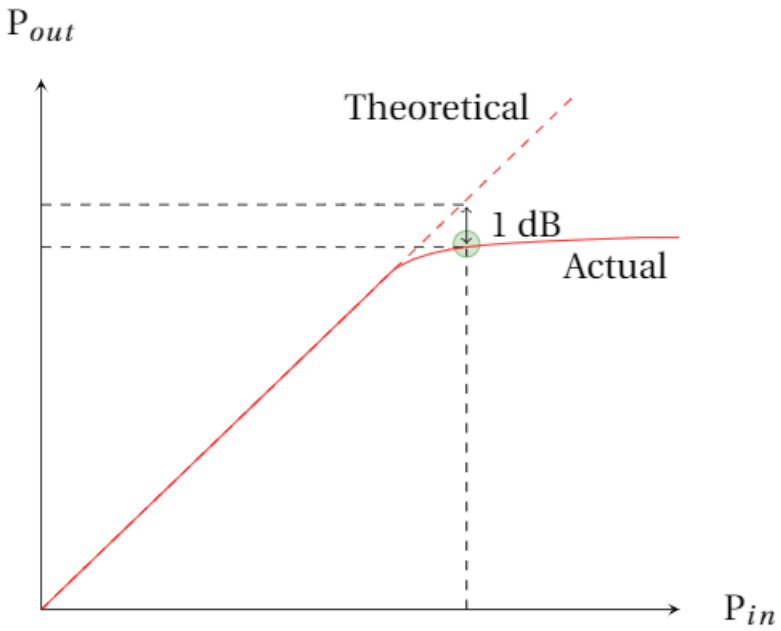


Figure 2.6: The real curve compresses as the input increases and deviates by 1dB from the linear curve in the 1dB compression point.

2.4.2 Two-tone test

Another common linearity test is the two-tone test where two tones are applied to the input of the amplifier. The equation for the input to the device under test is shown in Equation 2.5 with

the frequencies ω_1 and ω_2.

$$v_{in}(t) = V_0(\cos\omega_1 t + \cos\omega_2 t) \tag{2.5}$$

Inserting this equation into Equation 2.2 gives rise to frequency components with frequency $m\omega_1 + m\omega_2$, where $m, n = 0, \pm1, \pm2, \pm3$. This combination of input frequencies is called intermodulation with order $|m| + |n|$. The combination that gives $|m| + |n| = 3$ is thus called third-order intermodulation product. If the new components are located in the bandwidth, they can not be filtered out and we will experience distortion that affects the linearity of the amplifier. In order to measure the linearity, it is common to plot the power of the intermodulation product together with the power of the fundamental. The point where the two lines intersect is called the third-order intercept point (IP3) and applies for an amplifier with linear gain. This is plotted in Figure 2.7.

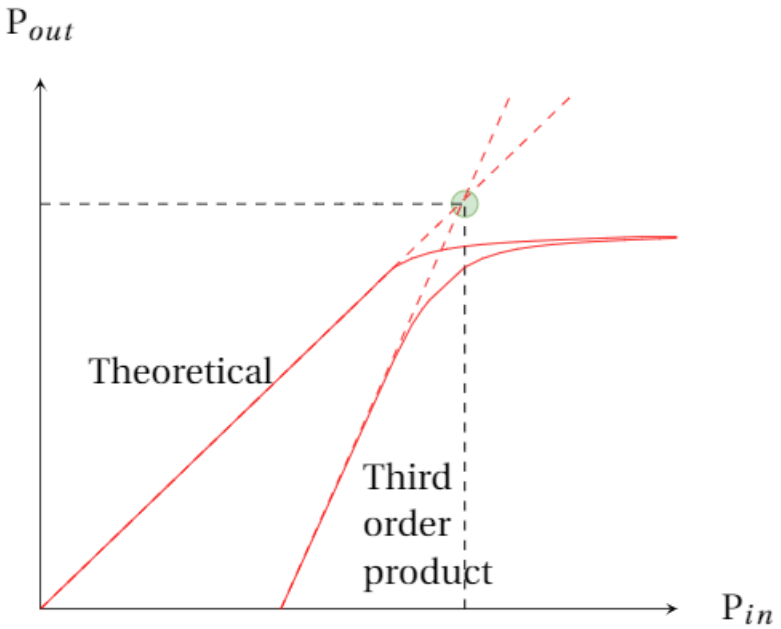


Figure 2.7: The characteristic of the fundamental frequency meets that of the third-order nonlinear products, making the third-order intercept point.

Mathematically, the intermodulation distortion (IMD) ratio is defined as

$$\text{IMD} = 10\log\frac{P_1}{P_3} \tag{2.6}$$

This is the ratio between the power of one of the two output tones, P_1, to the power of the third-

order intermodulation product, P_3. In the ideal case, the amplitudes of the two input tones are assumed to be the same. The IMD is usually measured in decibel with reference to the carrier (dBc).

2.5 S-parameters

When large signals are presented to the input of the amplifier we can experience the creation of nonlinear distortion. Most commonly one perform the singel-tone and two-tone tests presented in the previous section to explore how the amplifier responds to nonlinearities. But when the input signal to the device is small enough, we can rather use linear equations to describe the behaviour of the amplifier. Thus we can ignore the nonlinear effects so that inductors, capacitors and resistors are linearized and the operating point is kept constant.

By decomposing the voltage at the two ports of the amplifier, we can obtain incident and reflected voltage waves. This can further be used to define the S-parameters for the circuit. The S-parameters give us the opportunity to express useful properties as gain, stability and noise figure for the amplifier that is to be analyzed. Some of these properties will be explored further in the following sections.

2.6 Stability

In order to avoid oscillations in an amplifier it is necessary that the real part of the input and output impedance are not negative. Γ_{in} and Γ_{out} in Figure 2.8 are often matched to Γ_l and Γ_s to maximize the power transfer in a two-port network. This means that Γ_{in}, Γ_{out} and the stability will be determined by the matching network. The optimum matching will change with frequency, thus making the stability frequency dependent.

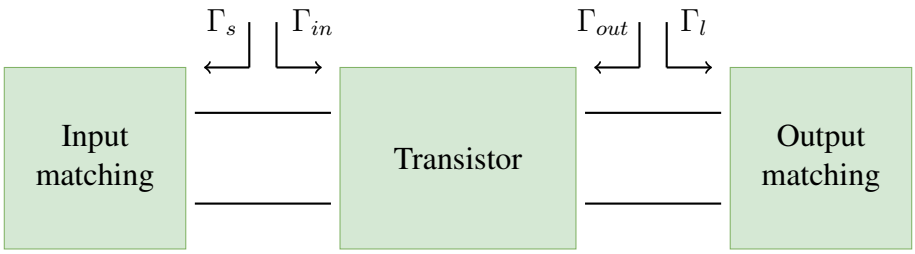


Figure 2.8: A transistor will see certain reflection coefficients at its input and output depending on the matching networks.

The stability of an amplifier can be either conditional or unconditional. In order for an amplifier to be unconditionally stable it must meet the requirements of $|\Gamma_{in}| < 1$ and $|\Gamma_{out}| < 1$ for all passive source and load impedances. In a conditionally stable amplifier the conditions $|\Gamma_{in}| < 1$ and $|\Gamma_{out}| < 1$ must be fulfilled for only certain source and load impedances. Thus, a conditional stable amplifier will be potentially unstable for other source and load impedances.

To know if an amplifier is unconditionally stable there exist two tests. The $K - \triangle$ test is determined by Rollet's condition given by Equation 2.7 [8].

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\triangle|^2}{2|S_{12}S_{21}|} > 1 \tag{2.7}$$

where $\triangle = |S_{11}S_{22} - S_{12}S_{21}| < 1$

When the amplifier meets these conditions it is unconditionally stable. A drawback with this test is that the size of K does not say anything about how stable the amplifier is. This is on the other hand offered by the μ-test and is an advantage of using this test. The μ-test is given by Equation 2.8 and has only one condition that needs to be met in order for the amplifier to be unconditionally stable [8].

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22} - \triangle S_{11}^*| + |S_{12}S_{21}|} > 1 \tag{2.8}$$

where $\triangle = |S_{11}S_{22} - S_{12}S_{21}|$.

A larger μ provides greater stability. This may be wise to keep in mind to ensure having a margin against production variations that may occur.

2.6.1 Inductive series feedback

The prevailing rule for a low noise amplifier is to match the input of the amplifier for minimal noise. By inserting an inductive series feedback as shown in Figure 2.9 it is possible to achieve simultaneous conjugate input impedance and optimal noise match impedance [9]. In other words, the input match for gain will be closer to the input match for optimum noise figure in the Smith Chart. This will make the optimum input reflection coefficient $|\Gamma_{opt}|$ a function of series inductance. The addition of such a series feedback reduces the gain, which helps the amplifier to become more stable. The increase in input impedance caused by the inductor makes the amplifier more tolerant to variations in device parameters.

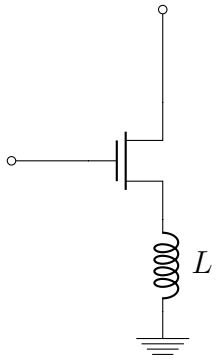


Figure 2.9: Stabilization scheme using a series feedback inductor.

2.6.2 Parallel RC-feedback

Another method for improving the stability of an amplifier is to add a resistive feedback between the drain side and gate side of the transistor. While this method makes the input and output impedances more convenient for matching, it will also increase the level of noise [6]. The resistor ensures that the amplifier becomes more stable throughout the frequency band, while the capacitor allows the different DC levels on the gate and drain side to be kept separate. Such a feedback circuit is shown in Figure 2.10. This is a technique that can almost exclusively be used in integrated circuits.

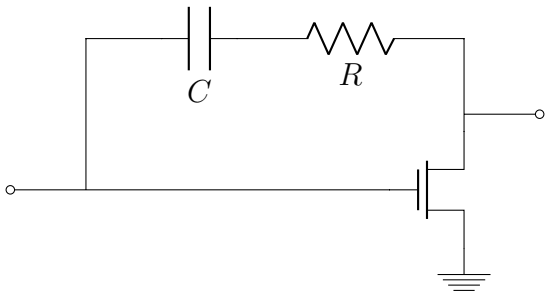


Figure 2.10: Stabilization scheme using a parallel resistor-capacitor feedback.

2.7 Noise

Even in the absence of an input signal there is possible to measure an output signal in a stable amplifier. This is caused by noise and the signal you measure is the noise power of the amplifier. The total noise measured at the output consists of amplified input noise in addition to noise generated by the amplifier itself. The noise power on the input can be modeled using a noise resistance as in Figure 2.11. The noise occurs as a result of the random movements of the electrons in the resistor. The thermal agitation makes this type of noise known as thermal or Johnson noise. The maximum available noise power, N_o, from a resistor R_n is

$$N_o = ktB \tag{2.9}$$

where B [Hz] is the bandwidth, t [K] is the temperature and $k = 1.38 \cdot 10^{-}23$ J/K is Boltzmann's constant. Thus, a smaller bandwidth will reduce the amount of noise power. One can also observe that the noise power is independent of the value of the noise resistance. Nevertheless, the amount of noise power actually delivered to the load resistor will decrease as the ratio between the source and load resistor differs from unity. The idea of making a mismatch on the input is central in the design of a low noise amplifier because it reduces the noise contribution from source.

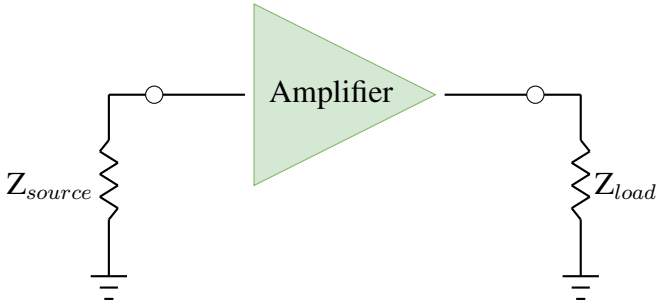


Figure 2.11: A two-port amplifier with a load resistor and a noisy source resistor.

As shown in Equation 2.9, the noise power is not given by a single specific frequency. Instead, the noise power depends on the bandwidth and gives a distribution that is referred to as white noise. However, in reality, there exists no proper white sources with infinite noise over an infinite bandwidth. For microwave frequencies, most dissipative elements can be characterized as ideal noise sources described by Equation 2.9.

Moving the focus to lower frequencies there dominates another type of noise. This low-frequency noise is often referred to as flicker noise or $1/f$. The frequency where the $1/f$ noise is as large as the ktb noise is called the $1/f$ knee frequency. Because the knee frequency of transistors often is less than 100 MHz, flicker noise is regarded less important in the design of RF and microwave amplifiers [9].

In addition to the previously mentioned types of noise there also occurs generation of shot noise in microwave transistors. This noise is generated as a result of random passage of charges in the modulating channels. From DC to 100 MHz, the shot noise is fairly constant before it increases with frequency.

The occurrence of noise in the receiver sets a limit to the S/N-ratio, defined as $SNR = \frac{desired\ signal}{undesired\ signal}$. Thus, less noise will give better reception of the signal. There are two types of noise encountered in the receiver; antenna noise and noise generated by components in the receiver. Noise factor is used in order to describe the amount of noise generated from a component or an entire system. The noise figure is the noise factor given in decibel. The noise factor is dependent on losses from components, amplification in the circuit and the bias applied to the circuit.

For a two-port network, the noise factor, F, is defined as

$$F = \frac{SNR_{input}}{SNR_{output}} = \frac{(S_i/N_i)}{(S_o/N_o)} \tag{2.10}$$

The relationship between the input and output of the network is shown in Figure 2.12.

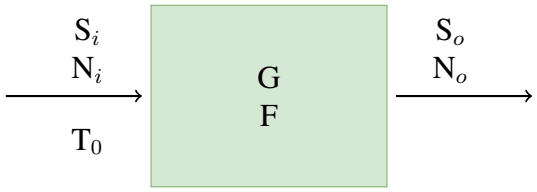


Figure 2.12: Relationship between the input and output in a two-port network.

Substituting $S_0 = GS_i$ and $N_i = kT_0B$ into Equation 2.1 gives

$$F = \frac{N_0}{GkT_0B} \tag{2.11}$$

where N_0 is the output noise, G is the gain, k is the Boltzmann constant, $T_0 = 290$ K and B is the bandwidth. Gain is defined as the power gain, which is the ratio between the power dissipated in the load and the power delivered into the two-port [8]. This ratio is defined in Equation 2.12.

$$G = \frac{P_L}{P_{in}} \tag{2.12}$$

2.8 Multistage

The amplifier's characteristic can largely be changed by dividing into several stages and connecting them together. Expanding the amplifier by several stages is particularly relevant in cases where required specifications are hardly obtainable through using only one stage. A multistage amplifier is shown in Figure 2.13.

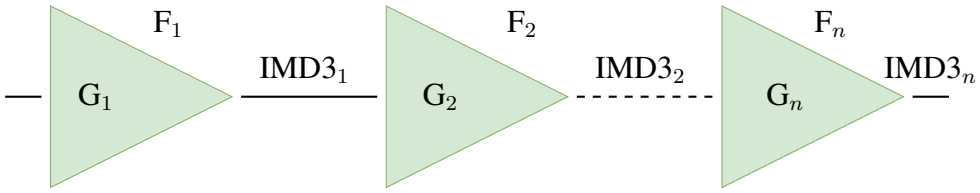


Figure 2.13: Multistage cascaded amplifier with properties of each stage.

2.8.1 Noise

When connecting multiple two-ports in cascade, the total noise factor will be determined by the noise factor and gain from each step of the cascade.

$$F = F_1 + \frac{F_2 - 1}{G_1} + .. + \frac{F_n - 1}{G_1 G_2 .. G_n} \tag{2.13}$$

From Equation 2.13 one can observe that the noise factor is dominated by the first step. Therefore, it is desirable to have low noise and high gain in the first step for the overall noise factor to be as low as possible.

2.8.2 Third-order intermodulation distortion

To find the third-order intermodulation distortion (IMD3) of the input to a multi-stage amplifier, it is possible to add the power from each stage in parallel. Equation 2.14 shows input IMD3 of an n-stage amplifier, given that the intercept points are independent and uncorrelated.

$$IMD3input = \frac{1}{\frac{1}{IMD3_1} + \frac{G_1}{IMD3_2} + \frac{G_1 G_2}{IMD3_3} + ... + \frac{G_1 G_2 ... G_{n-1}}{IMD3_n}} \tag{2.14}$$

IMD3$_n$ and G_n in Equation 2.14 are respectively IMD3$_n$ (in mW) and gain for each stage of the amplifier. By multiplying the total power gain ratio with the input IMD3 from Equation 2.14 it is possible to calculate the output IMD3. The sum of the amplifier's total gain and input IMD3 will also give the output IMD3, as shown in Equation 2.15.

$$IMD3_{output} = G_{tot} + IMD3_{input} \tag{2.15}$$

2.9 Impedance Matching

The challenge in creating a matching impedance network is to accentuate the desired properties of the amplifier in a best possible way. To minimize noise that will be generated, it is desirable to have as few components as possible. Nevertheless, one should have a large enough network to cover all the different input and output impedances of a broadband amplifier. The matching network is based on which impedances the transistor ”sees” as shown in Figure 2.14. By the use of a simple LC network one can make an impedance transformation from the transistor's desired impedances to 50 Ω. The amplifier can then be connected to external 50 Ω devices such as an antenna. It is recommended to use capacitive and inductive elements every second time in the match to reduce the risk of resonance.

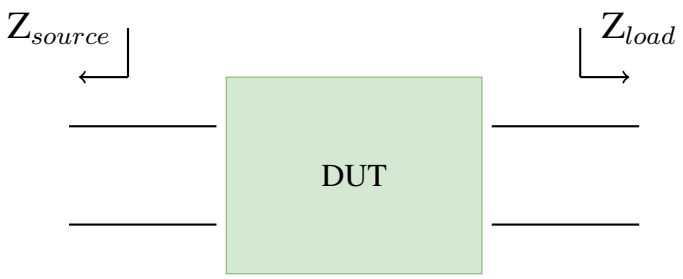


Figure 2.14: The device needs to see certain impedances at the input and output in order to minimize the noise figure.

To prevent RF from leaking into the DC supply, it is possible to add a RF choke in series with the DC supplies in the input and output matching networks. This inductor eliminates RF frequencies while DC is allowed to pass. There is also possible to add a shunt capacitor at the DC input to reject the RF energy from going to the power supply. This decoupling capacitor should be set to a value as large as possible if only having size restrictions for the layout. Thus, shunt capacitors included in input and output matching networks will preferably have fixed, large capacitance values. A decoupling capacitor combined with a RF choke will effectively reject all of the RF frequencies.

Another common block included in a matching network is a series capacitor connected right to the input and the output in the RF path of the amplifier. This element is the DC block that prevents DC from flowing through the RF input and output. The value of the capacitor is not

important as it prevents DC from flowing in any case. Both the DC block and the RF choke can be considered parts of the matching networks as they can be tuned for more accurate matching. This gives the matching networks more degrees of freedom which can be exploited when the amplifier circuit is optimized for better results.

Chapter 3

Design of Amplifier Stages

To achieve sufficient gain, the goal is to make an amplifier using two stages coupled in cascade as shown in Figure 3.1. The same transistor type (CG40v4) will be used for both stages. The amplifier will be designed using Keysight's Advanced Design System (ADS).

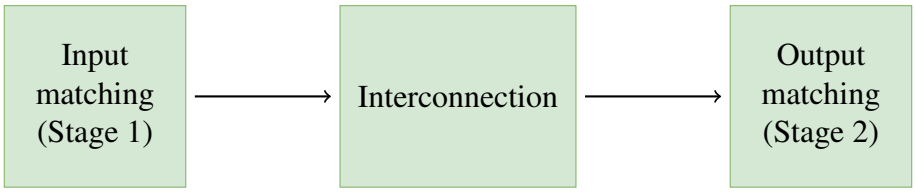
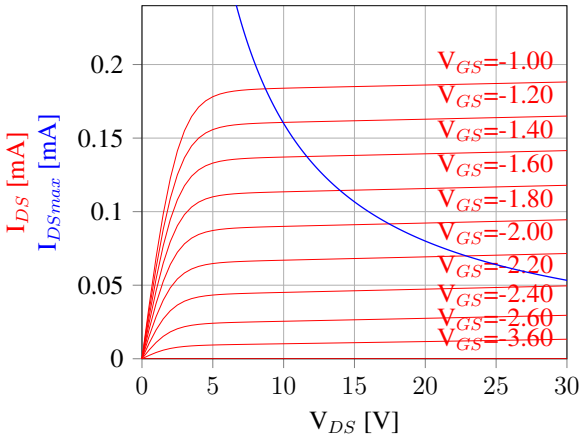


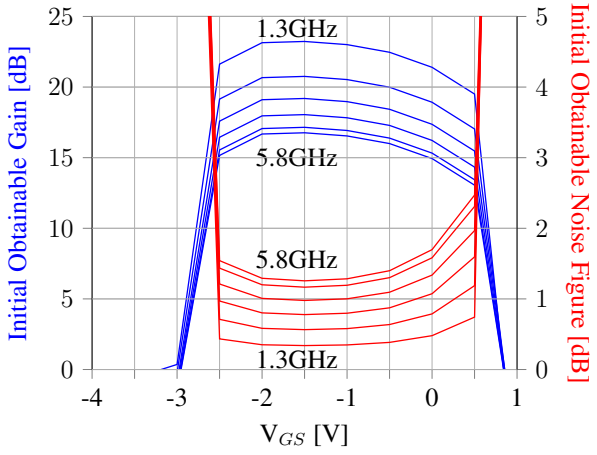
Figure 3.1: Setup for a cascaded two-stage amplifier.

3.1 Bias

As mentioned in the theory, system integration could be emphasized when selecting drain voltage and 12V may therefore be a reasonable value for both stages. By using a testbench in ADS there is possible to generate IV curves for use in the selection of bias point. Such a testbench can be found in Appendix A.1. The testbench sweeps V_{ds} from 0 to 30V, while V_{gs} will be swept from -1 to -4V for a CG40v4 transistor with $4\cdot$ 100 μm gate width. A starting point can be in the range of 50-60mA drain current giving V_{gs} = -2.0V. This can be adjusted later if another bias turns out to produce better results. IV-curves for the CG40V4 transistor can be seen in Figure 3.2a. Figure 3.2b shows how the selection of V_{gs} affects the performance of the G40V4 transistor in terms of gain and noise. The different curves indicate frequencies in the range 1.3-5.8GHz and are obtained using ideal matching.



(a) Generated bias curves for the G40V4 transistor.



(b) Initial obtainable Noise Figure and Gain.

Figure 3.2: Supporting figures in the selection of bias.

3.2 Stabilization

To stabilize the amplifier it is advisable to add an inductor to the source of the transistor for low noise applications. As this is not necessarily sufficient to achieve the desired stability, it is possible to add a RC network in addition. This combination will result in a stabilization topology as shown in Figure 3.3 below.

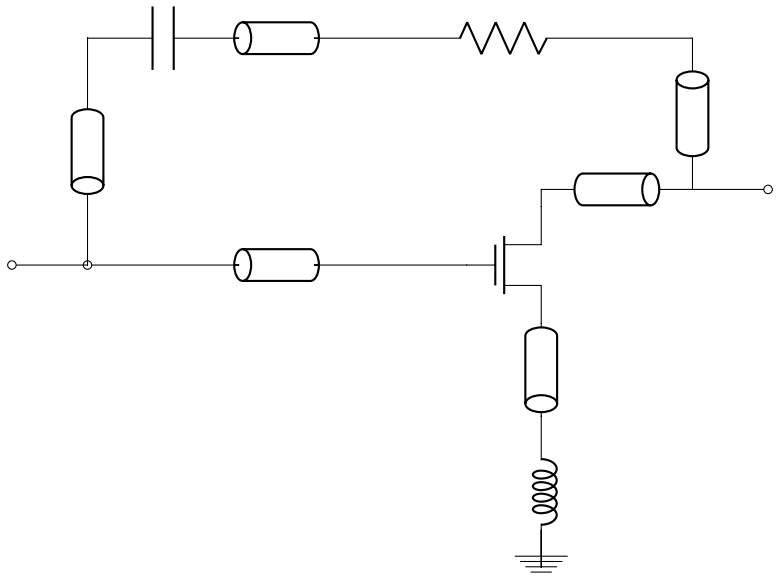


Figure 3.3: Stabilization circuit for both stages.

A small-signal analysis will be simulated in ADS showing stability indicated using μ in order to check if the obtained stability is sufficient.

3.3 Matching

By running a small-signal simulation of the transistor together with the stabilization circuit in ADS, there is possible to find the needed impedances, Z_{source} and Z_{load}, for noise matching. As the amplifier is to be wideband, the impedances should be recorded with 0.5 GHz increments in the range 1.3 - 5.8 GHz. In this design, the system impedance is set to be 50 Ω and impedance transformations have to be made from 50 Ω to Z_{source} and from Z_{load} to 50 Ω. The small-signal testbench that is to be used can be seen in Appendix A.4.

3.3.1 Input matching

The input matching for the whole two-stage amplifier will be determined by stage one. The input network in stage one will be matched for noise of reasons given in Chapter 2. The optimal reflection coefficients for minimal noise, NFmin, are found by running a small-signal analysis over the frequency range. The reflection coefficients are plotted with 0.5 GHz increments in the Smith Chart in Figure 3.4. It is then possible to use inductive and capacitive elements to match these coefficients to the 50 Ω system impedance in the center of the Smith Chart.

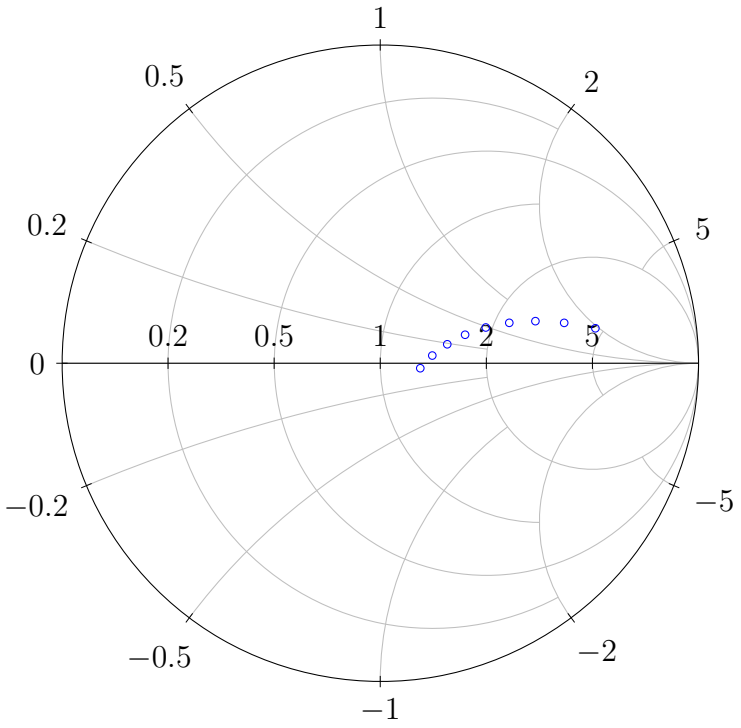


Figure 3.4: Impedances for input matching network.

A finished input network will then look like the LC network in Figure 3.5. The ADS schematic of the input network including component values can be found in Appendix B.1.

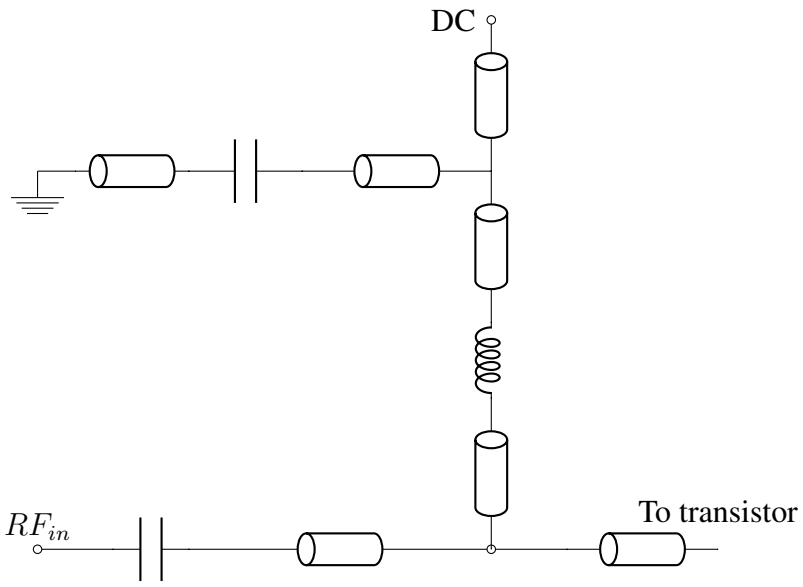


Figure 3.5: Input circuit connected to stage 1.

3.3.2 Interconnection stage

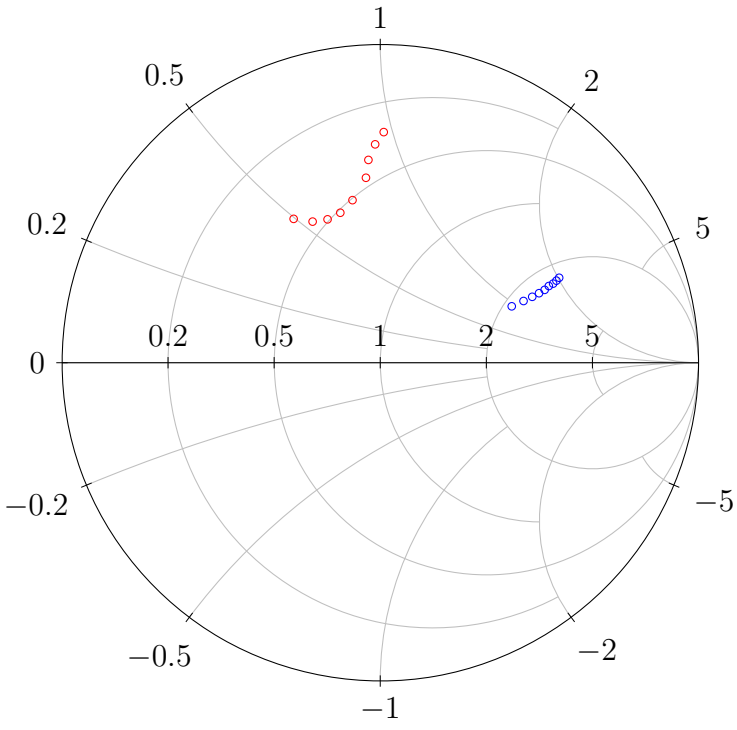


Figure 3.6: Impedances for interconnection network.

For matching the two stages in the best possible way, the reflection coefficients of the output of stage one and the input of stage two can be plotted in a Smith Chart. The reflection coefficients

from stage one will optimize the amplifier with respect to noise, while the reflection coefficients of stage two provide optimum gain. To connect the two stages it is possible to use inductors and capacitors that would join the optimal impedance points in Figure 3.6 together. One way to do this is to combine the two RF chokes that need to be included anyway and insert a DC block inbetween. The network will then be optimized in ADS against impedances that stage one and stage two want to see towards the interconnection stage. This is shown in Equation 3.1 where $\triangle S_{11}$ optimizes for matching with stage one and $\triangle S_{22}$ optimizes for matching with stage two. This causes the transistor in stage one to see the correct impedances for optimal noise on the drain side while the transistor in stage two will see impedances for optimal gain on its input.

$$\begin{aligned} \triangle S_{11} &= \big||S_{11}| - |OptimZsource|\big| \rightarrow 0 \\ \triangle S_{22} &= \big||S_{22}| - |OptimZload|\big| \rightarrow 0 \end{aligned} \tag{3.1}$$

The interconnection stage will by the use of this method end up with the topology in Figure 3.7. The ADS schematic of the interconnection network with component values can be found in Appendix B.2.

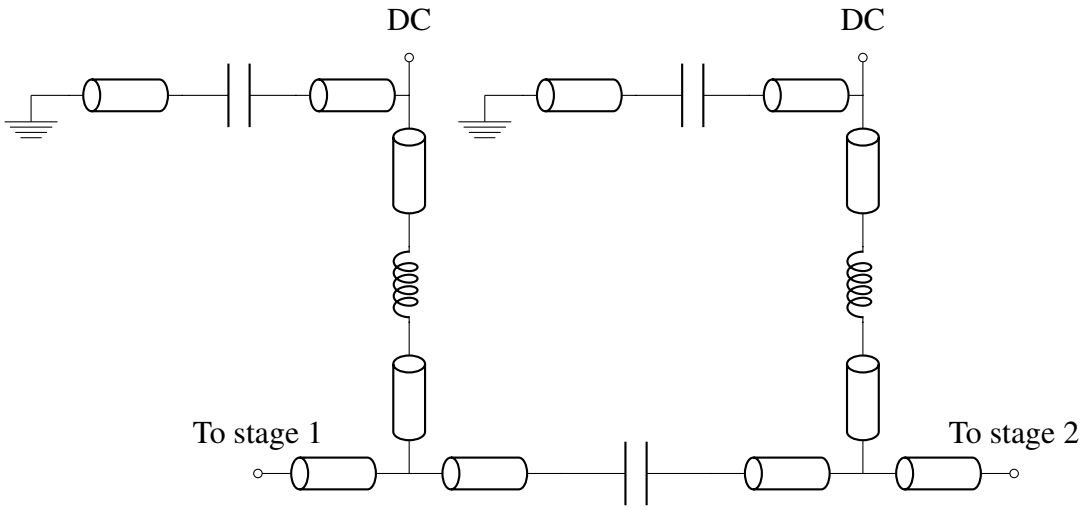


Figure 3.7: Interconnection circuit between stage 1 and stage 2.

3.3.3 Output matching

Stage two must be matched for optimal gain in order to meet the specifications. The output of the amplifier will therefore be matched against optimal load impedances for maximizing gain. The optimal load impedances for the bandwidth with 0.5GHz increments are plotted in Figure 3.8. These are found by running a small-signal analysis over the frequency band. The output will then be matched to 50Ω, which is the system impedance, using an inductive-capacitive network. To keep it simple, it may suffice to just use the RF choke and the DC block for the matching network.

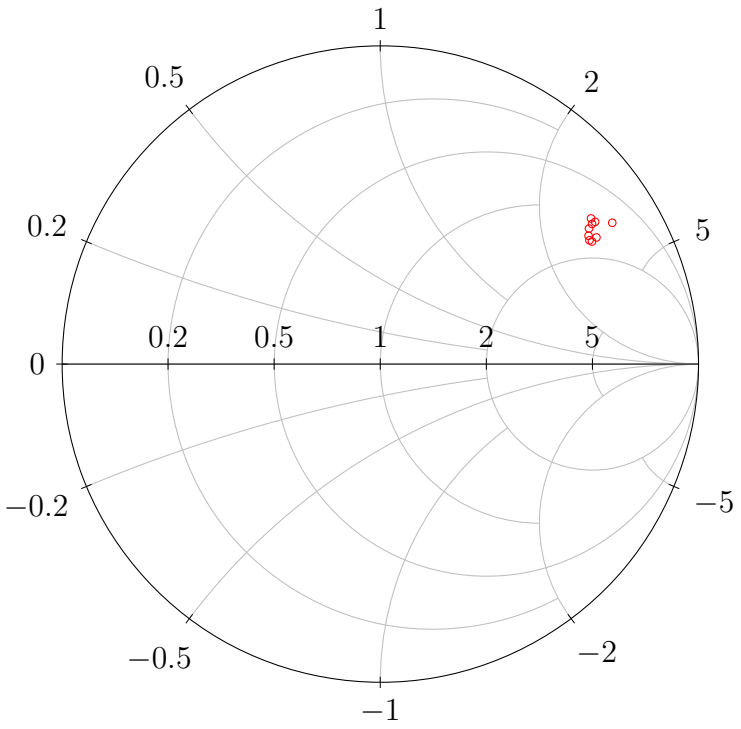


Figure 3.8: Impedances for output matching network.

The finished output network will then have a topology similar to the the one in Figure 3.9. The ADS schematic of the input network with component values can be found in Appendix B.3.

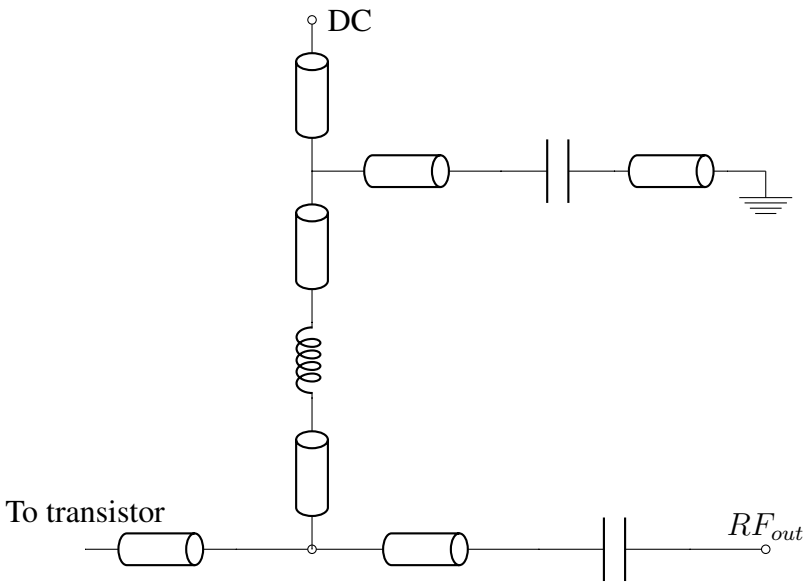


Figure 3.9: Output circuit in stage 2.

A full circuit schematic from ADS including all the stages can be found in Appendix B.4. This circuit shows the idea from Figure 3.1 adapted to a working schematic.

3.4 Layout

As can be observed in the previous section there are included transmission lines in the matching in view of a layout that is to be created in the end. The layout must be made with regard to possible production of the amplifier and to carry out electromagnetic (EM) simulations. There are no restrictions on space usage and the layout will be made compact enough without having problems with proximity between components. A proposal for a layout can be seen in Figure 3.10. The size of this layout is 1730μm x 1165μm. The layout is checked against a Design Rule Check (DRC) provided by Wolfspeed for the purpose of verification. Notice that this check only tests a set of constraints and gives no guarantee that the produced amplifier will operate correctly. However, no violation of rules will obviously give a higher probability of desired operation.

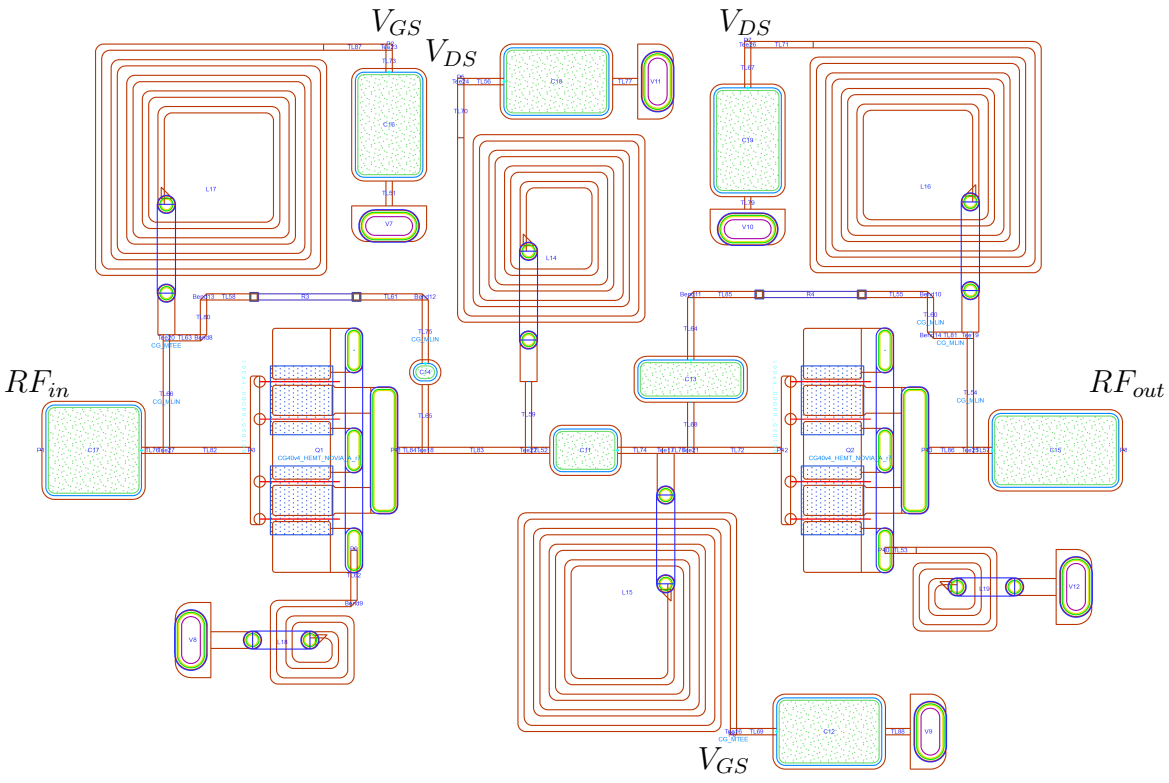


Figure 3.10: Layout for a two-stage LNA.

Chapter 4

Results

The results in this section are based on simulations done in ADS. The amplifier has not been manufactured and it will therefore not be presented any measurements. First, the results from small-signal analysis will be presented before showing results of the linearity from large-signal analysis. Then the results indicating the robustness of the amplifier will be presented. Finally, EM simulated results of the layout in Section 3.4 will be shown in the last section of this chapter.

4.1 Small-signal analysis

The results in this section origin from simulations in ADS using the testbench in Appendix A.4.

4.1.1 Stability

The results in Figure 4.1 shows the margin of stability for the two-stage amplifier. The red line is for the K-test, the blue line shows μ_{load} and the green line marks μ_{source}.

4.1.2 Gain

Figure 4.2 shows the results for the small signal gain. The red line marks the associated power gain ($Pgain_{associated}$), the blue line is the Maximum Available Gain (MAG) while the green line is the simulated small signal gain S_{21}. $Pgain_{associated}$ is the obtainable gain when the input and the output of the amplifier are perfectly matched for optimum noise. MAG is the gain that is obtainable when the whole amplifier is matched for gain. The results show that the amplifier peaks with 33.8dB at 1.3GHz while the amplification is at its lowest with 13.9dB at 5.8GHz.

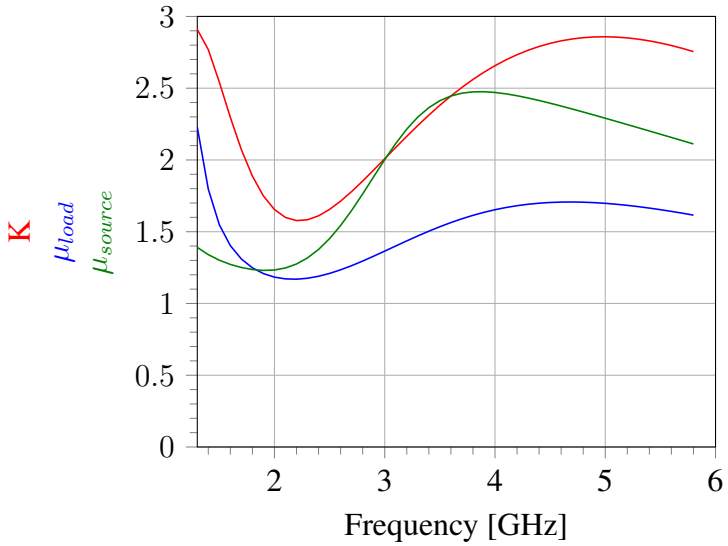


Figure 4.1: Simulated K, μ_{load} and μ_{source} showing the stability.

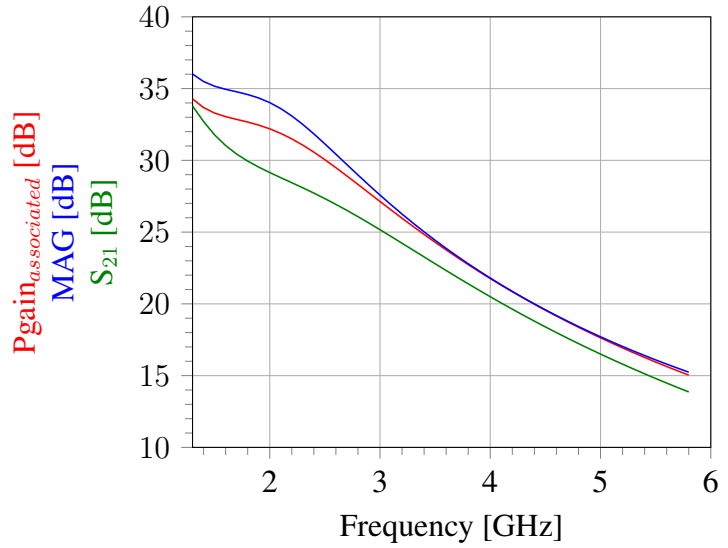


Figure 4.2: Simulated small signal gain.

4.1.3 Noise

The simulated noise performance is presented in Figure 4.3. The red line is showing the minimum noise figure ($NFmin$), while the blue line shows the resulting noise figure. $NFmin$ refers to the noise figure that can be obtained when the amplifier is perfectly matched for optimum noise performance.

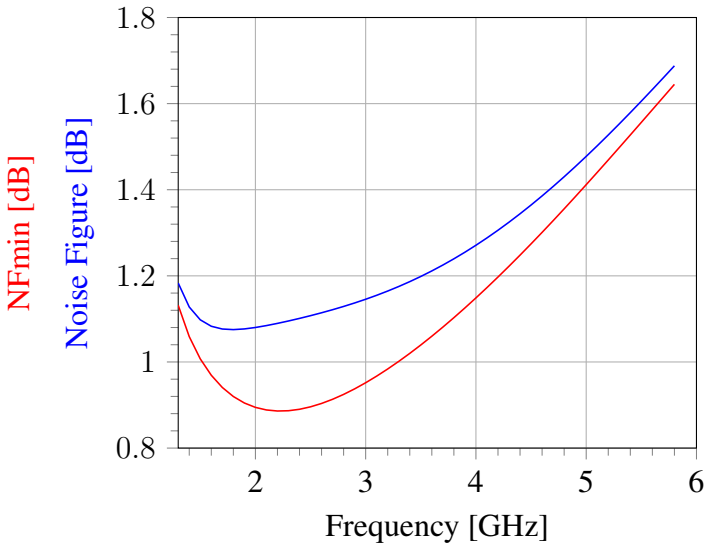


Figure 4.3: Simulated Noise Figure and Minimum Noise Figure.

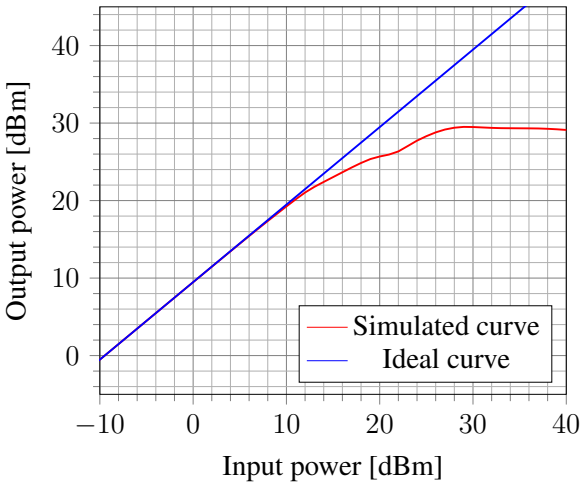
From the results it can be seen that the noise is peaking with 1.68dB at 5.8GHz, while the noise figure is at its lowest with 1.08dB at 1.8GHz.

4.2 Linearity

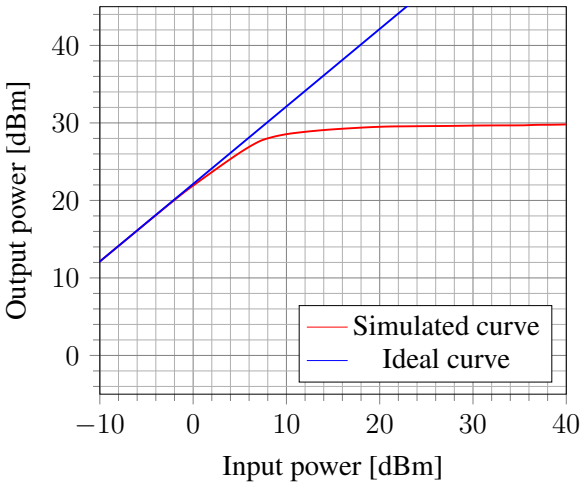
Appendix A.2 shows the single-tone testbench setup that have been used to simulate the output power of the amplifier. The intermodulation distortion has been simulated using the testbench in Appendix A.3.

4.2.1 Output power

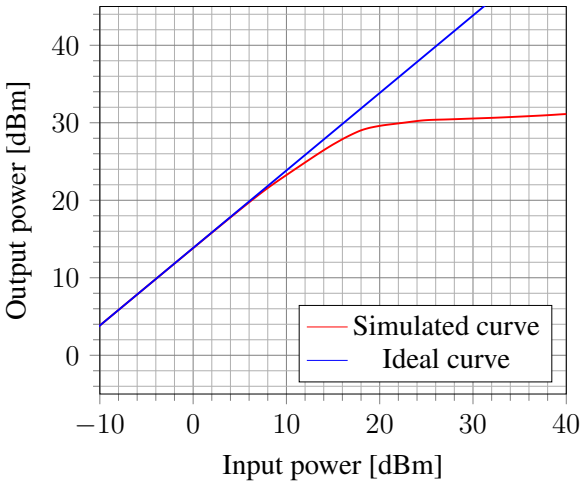
The simulation of the output power with increasing input power is performed using a single tone with frequencies of 1.3GHz, 3.5GHz and 5.8GHz. Figure 4.4 shows when the amplifier starts deviating from the linear curve and goes into saturation.



(a) $f = 1.3$ GHz



(b) $f = 3.5$ GHz



(c) $f = 5.8$ GHz

Figure 4.4: Output power plotted to the input power for a single tone with a specified frequency.

4.2.2 Intermodulation Distortion

Simulations for intermodulation distortion for different center frequencies have been performed using two tones swept with different frequency spacings. The input power was fixed to 19 dBm during simulations. The resulting output can be observed in Figure 4.5.

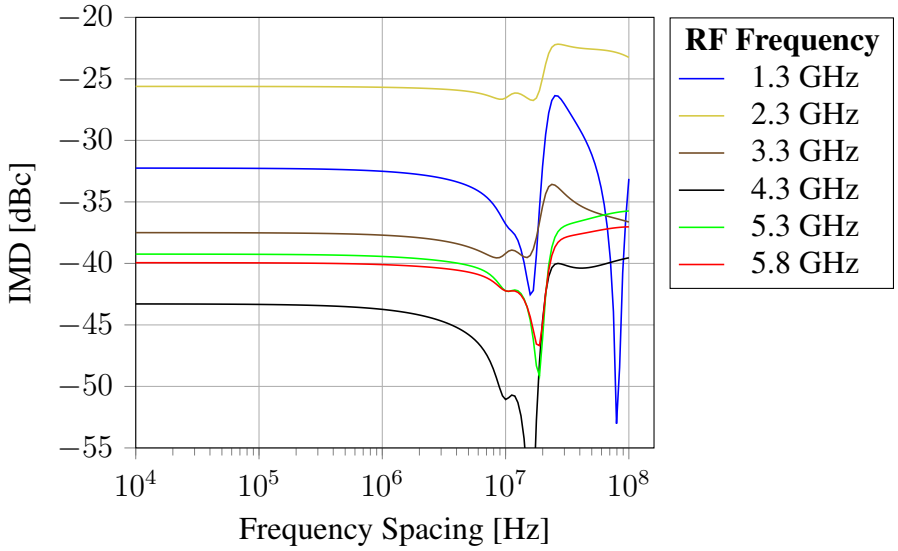


Figure 4.5: Intermodulation distortion for different center frequencies over different frequency spacings. The input power was set to a constant value of 19 dBm for simulations.

4.3 Robustness

Simulations of robustness have been done to check how the junction temperatures changes with increasing input power and for which input powers the amplifier reaches maximum ratings provided by Wolfspeed. These tests have been simulated using the testbench in Appendix A.2. There is set an ambient temperature of 85°C for these simulations to test the device under tough conditions.

4.3.1 Maximum ratings

The results in this subsection are obtained by extracting values from the nodes in Figure 4.6. The same method are used for both stage one and stage two. Input power refers to the power applied to the RF input connected to stage one of the amplifier. This applies for all figures and tables in this subsection.

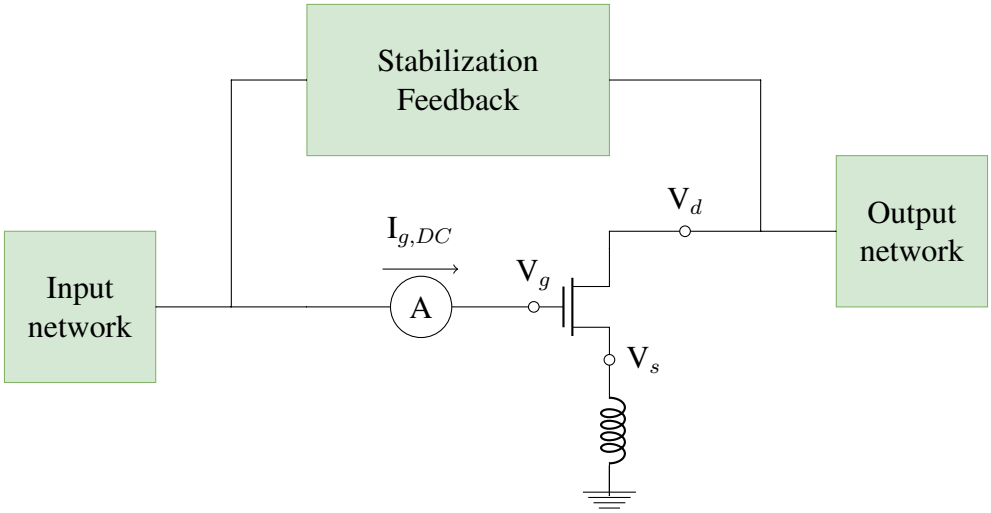


Figure 4.6: Position of nodes and ammeter used to obtain values of V_{gs}, V_{ds} and $I_{g,DC}$.

Figure 4.7 and Figure 4.8 shows which levels of input power delivered to stage one that makes the amplifier exceed V_{gs} = -8V and V_{ds} = 84V. Figure 4.7 shows the results for the transistor in stage one, while Figure 4.8 shows V_{gs} and V_{ds} for the transistor in stage two. Figure 4.9 and Figure 4.10 shows the different input powers fed respectively to the amplifier that makes $I_{g,DC}$ greater than 1 mA/mm · 400μm = 0.4 mA in stage one and stage two, respectively. The plots are simulated using the center frequency $f = 3.5$GHz and with an ambient temperature of 85°C.

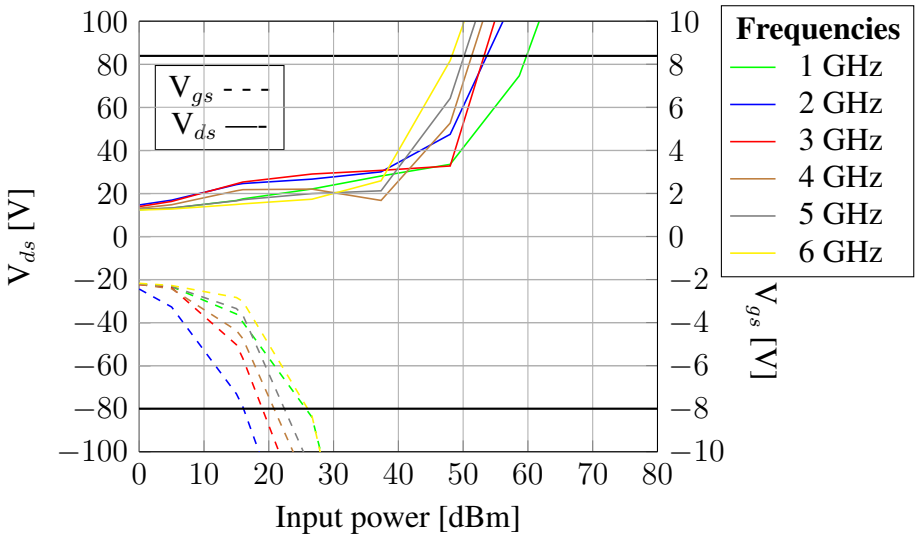


Figure 4.7: Simulated input powers to stage one exceeding maximum ratings of V_{ds} and V_{gs} for different frequencies for the transistor in stage one. The black solid lines mark V_{ds} = 84V and V_{gs} = -8V.

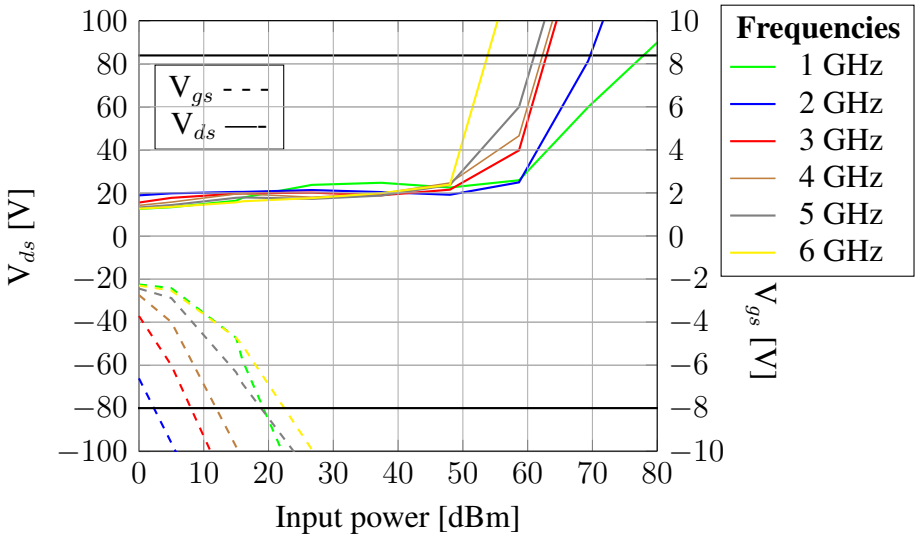


Figure 4.8: Simulated input powers to stage one exceeding maximum ratings of V_{ds} and V_{gs} for different frequencies for the transistor in stage two. The black solid lines mark V_{ds} = 84V and V_{gs} = -8V.

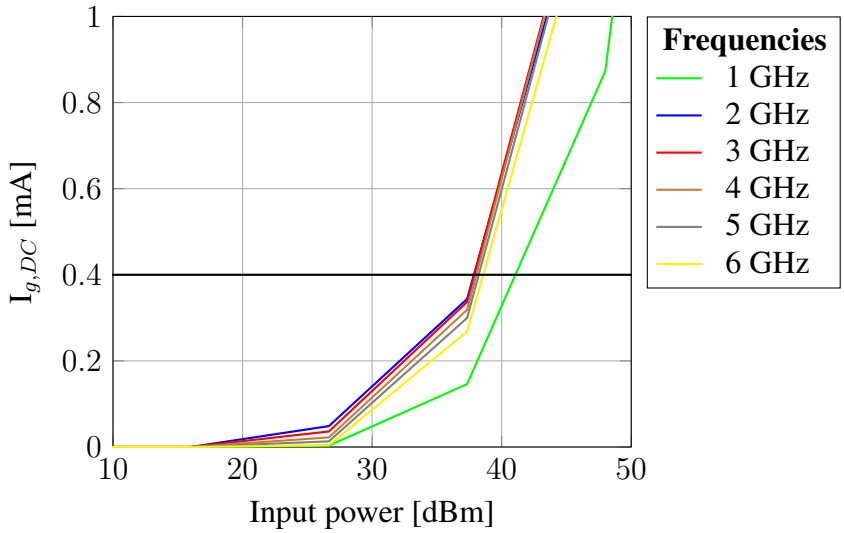


Figure 4.9: Simulated input powers to stage one exceeding maximum ratings of $I_{g,DC}$ for different frequencies for the transistor in stage one. The black solid line marks $I_{g,max}$ = 0.4mA.

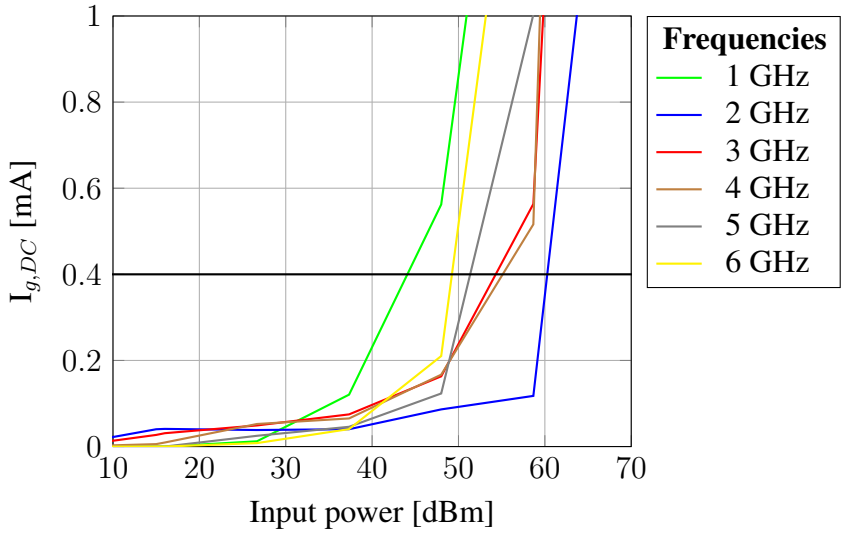


Figure 4.10: Simulated input powers to stage one exceeding maximum ratings of $I_{g,DC}$ for different frequencies for the transistor in stage two. The black solid line marks $I_{g,max}$ = 0.4mA.

Table 4.1 shows the exact input powers where $I_{g,max}$, $V_{gs,max}$ and $V_{ds,max}$ are exceeded for different frequencies. The input power is swept in the range -15 to 80 dBm. Table 4.1 contains values for the transistor in stage one.

Table 4.1: Applied input powers to stage one where $V_{g,max}$, $V_{gs,max}$ and $V_{ds,max}$ are exceeded in stage one for different frequencies.

Frequency [GHz] / Input power [dBm] at	1.0	2.0	3.0	4.0	5.0	6.0
$I_{g,max}$	43	39	39	38	39	40
$V_{gs,max}$	26	16	19	22	23	27
$V_{ds,max}$	58	54	55	52	49	48

Table 4.2 shows when $I_{g,max}$, $V_{gs,max}$ and $V_{ds,max}$ are reached for the transistor in stage two. This table summarizes the results in Figure 4.8.

Table 4.2: Applied input powers to stage one where $V_{g,max}$, $V_{gs,max}$ and $V_{ds,max}$ are exceeded in stage two for different frequencies.

Frequency [GHz] / Input power [dBm] at	1.0	2.0	3.0	4.0	5.0	6.0
$I_{g,max}$	46	64	57	57	56	52
$V_{gs,max}$	18	5	9	13	19	23
$V_{ds,max}$	78	75	64	63	60	57

4.3.2 Power handling

Figure 4.11 shows the junction temperature in unit degree Celsius for both transistors. The ambient temperature and the backside temperature of the chip is set to 85°C during the simulation. The thermal resistance is set to 34°C/W. This number is estimated out of figures provided by United Monolithic Semiconductors (UMS) for a similar MMIC GaN HEMT process [10]. The temperature is plotted together with the output power to simulate how the amplifier responds to increasing input power in tough environments. The frequency is set to $f = 3.5$GHz for this plot.

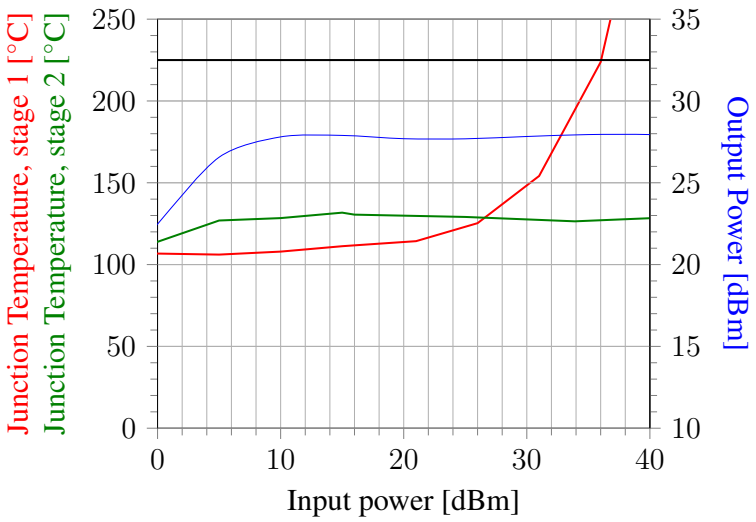


Figure 4.11: Output power and junction temperature plotted to the input power of the amplifier. The black solid line marks the absolute Maximum Junction Temperature of 225°C.

4.4 EM-simulations

The layout is verified through EM-simulations. This was done by removing the transistors and generating an electromagnetic model consisting of the passive components from the remaining circuit. By doing this you may include any inductive couplings that have occurred due to the fact that components are placed too close in the layout. The transistors are then placed back into the generated EM model and the entire circuit is verified using the small-signal testbench in Appendix A.4. Such an EM model can be found in Appendix C.1 together with the substrate model used for these simulations. The stability of the amplifier is plotted in Figure 4.12 with the same stability parameters as in Section 4.1.1. The results for the simulated small signal gain can be observed in Figure 4.13, while the noise figure is plotted in Figure 4.14.

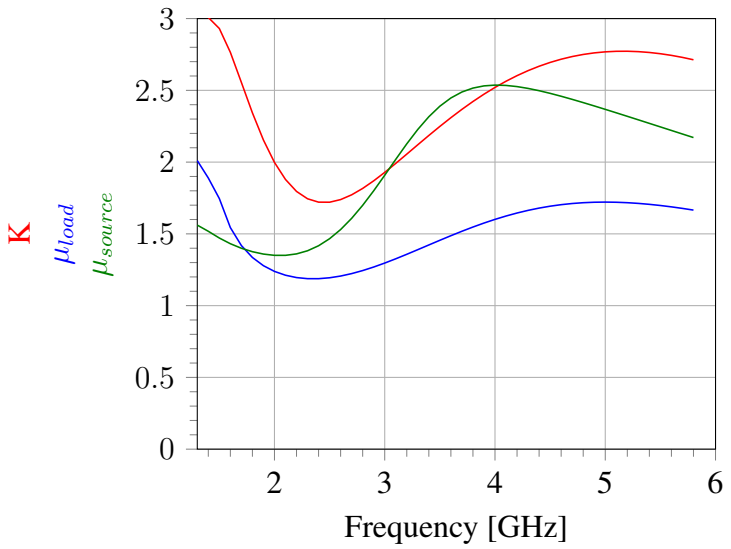


Figure 4.12: EM-simulated results for stability.

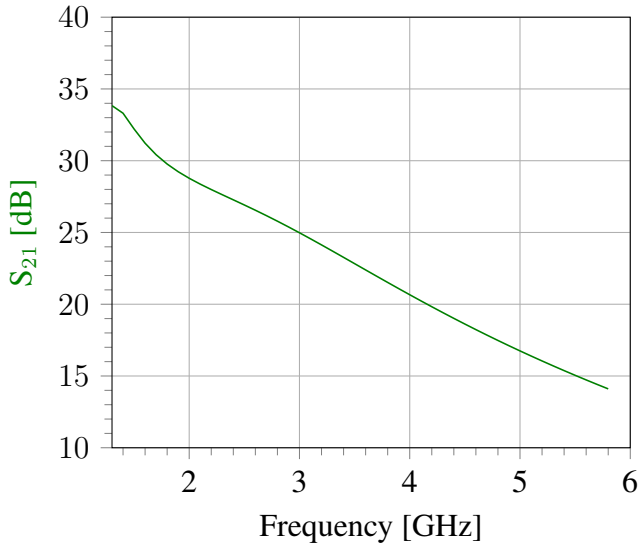


Figure 4.13: EM-simulated results for small signal gain.

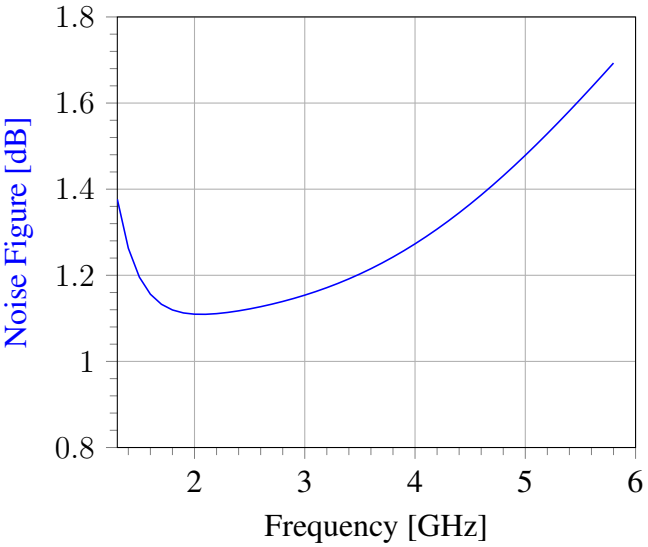


Figure 4.14: EM-simulated results for noise figure.

Chapter 5

Discussion

5.1 Simulation results

From Figure 4.1 it is observable that the amplifier is stable across the bandwidth with at least a margin of 0.17dB at 2.2GHz. This margin is conceivably large enough to ensure against production variations and to avoid oscillations. The curve designating the noise figure in Figure 4.3 follows the curve of NFmin closely and differs with only 0.16dB at most. The noise figure peaks at 5.8GHz with 1.68dB and is well below the maximum limit of 2dB from specifications. The simulated gain reaches just above the requirement of 13dB for 5.8GHz with a simulated magnitude of 13.9dB. The curve of S_{21} does not differ much from the curve of MAG, which can be considered adequate for an amplifier that is matched primarily for noise performance and not gain. Based on experience with simulations and repeated optimizations of the amplifier, there was a trend that the process delivered poorer results in the upper bandwidth. By expanding the bandwidth beyond 5.8GHz, it could be difficult to achieve sufficient gain with this design.

The maximum ratings for the process are 84V for V_{ds}, -8V for V_{gs} and 1mA/mm for I_{gmax} as stated in Section 2. Looking at the figures in Section 4.3 it is noticeable that the amplifier must be jammed very strongly before it will exceed any of these breakdown values. In order for this to happen at all, a radio jamming device must be placed very close to the RF receiving antenna. The amplifier's gate width of 400μm gives an I_{gmax} of 0.4 mA. This maximum current will first occur when the input power has driven the amplifier far into saturation. This is observed in Figure 4.11 where the output power flattens out at roughly 18dBm input power. Evidently,

the maximum rating of V_{gs} will be most critical for breakdown of both transistors as can be observed in tables in Section 4.3. The V_{gs} applied to stage one will be the maximum rating causing the amplifier to fail. Figure 4.11 shows that the junction temperature in stage two will be the hottest transistor as the output power from stage one will be fed to the gate of the second transistor. However, this junction temperature will stop increasing when the transistor is in saturation at 14dBm. The junction temperature of stage one will continue increasing with input power, but will not reach the critical Maximum Junction Temperature of 225°C before 37dBm input power. It should be noted that the amplifier is not tested for operation over time which indicates the lifetime of the amplifier. These results show that the amplifier will work well for its main application of amplifying weak input signals with low decibel values. Critical conditions will first occur when the device is exposed to jamming.

5.2 Design choices

By inspecting Figure 4.2, it is possible to observe that the gain varies with 10dB in the bandwidth and is thus not particularly flat. A flat gain can be achieved by introducing more resistance in the circuit, for example by connecting a resistor in series with the DC supply on the gate side. However, this has not been tested in this design as gain flatness was not a specified requirement and thus not been prioritized during the design phase.

Another decision made early in the project was modifying the drain voltage down from 20V to 12V. This was done due to simpler system integration. This adjustment was not found to make any notable difference on the performance of the amplifier. It resulted in some less gain but decreased the noise figure slightly. In a power amplifier it would be more ideal with a higher drain voltage, but as the main focus was set on noise figure the decrease in gain was neglected. A possible approach for future work would be to experiment with different bias for the two stages to possibly achieve improved gain at higher frequencies. The downside of doing this is that it will make system integration harder.

The EM simulations in Figure 4.12, 4.13 and 4.14 are correct with what was achieved in the small-signal analyzes in Figure 4.1, 4.2 and 4.3 of the schematic. This means that any inductive

couplings have not affected the results any noteworthy. With stricter area restrictions there would have been a need to experiment further with making the layout area even more tight. This could have been done until the occurrence of inductive couplings that would affected the EM-simulated results. The revised layout in Figure 3.10 is indeed done according to this principle, but it is possible that other than the author could find further improvements and shrink the area even more. It was explored with a one-stage amplifier at the early start of the project phase, but the required gain forced the amplifier to be two-staged. The downside of this extension is that the layout requires a larger area. However, this was a necessary decision to make as there was a requirement for gain and not for used layout area.

Chapter 6

Conclusion

This thesis has explored the design of a robust low noise amplifier in GaN MMIC using the CAD software Advanced Design System (ADS). It was required to obtain gain higher than 13dB and hold the noise figure below 2dB for 1.3 - 5.8GHz. The amplifier was designed with two stages in order to achieve desired level of gain. These stages were linked together in an interconnection network using the output matching network of the first stage and the input matching network of the second stage. The matching networks were designed using optimal impedances for noise in stage one and optimal impedances for gain in stage two. A producible layout was designed in the end for the purpose of electromagnetic (EM) simulations and the possibility of production in the future.

The results were simulated in ADS using testbenches for small-signal analysis and large-signal analysis. The small signal gain is simulated to have a minimum of 33.8dB at 1.3GHz and a maximum of 13.9dB at 5.8GHz. The noise figure peaks at 1.68dB for 5.8GHz, while a minimum is found at 1.8GHz with 1.08dB. The EM-simulation of the layout produced values that agrees with these results. Simulations of intermodulation distortion and output power have been done to show the linearity of the amplifier. Junction temperatures and V_{gs}, V_{ds} and I_g have been simulated with swept input power to demonstrate the robustness of the amplifier. These simulations found the gate-source voltage for the transistor in stage one to be the limitation for the amplifier.

6.1 Future work

In order to improve the amplifier's usability in tough environments it may be an idea to look into improvement of linearity for future work. Saini et al [11] look in their paper on a linearization technique for low noise amplifiers where a single field-effect transistor (FET) is divided into two parallel FET transistors of half the original gate width. The two parallel transistors are biased with different bias current, which causes phase cancellations and reduces the power level of third-order intermodulation products. However, the presented hybrid low noise amplifier is based on Roger's 4350 substrate material and implementation of this technique in a MMIC LNA is yet to be demonstrated.

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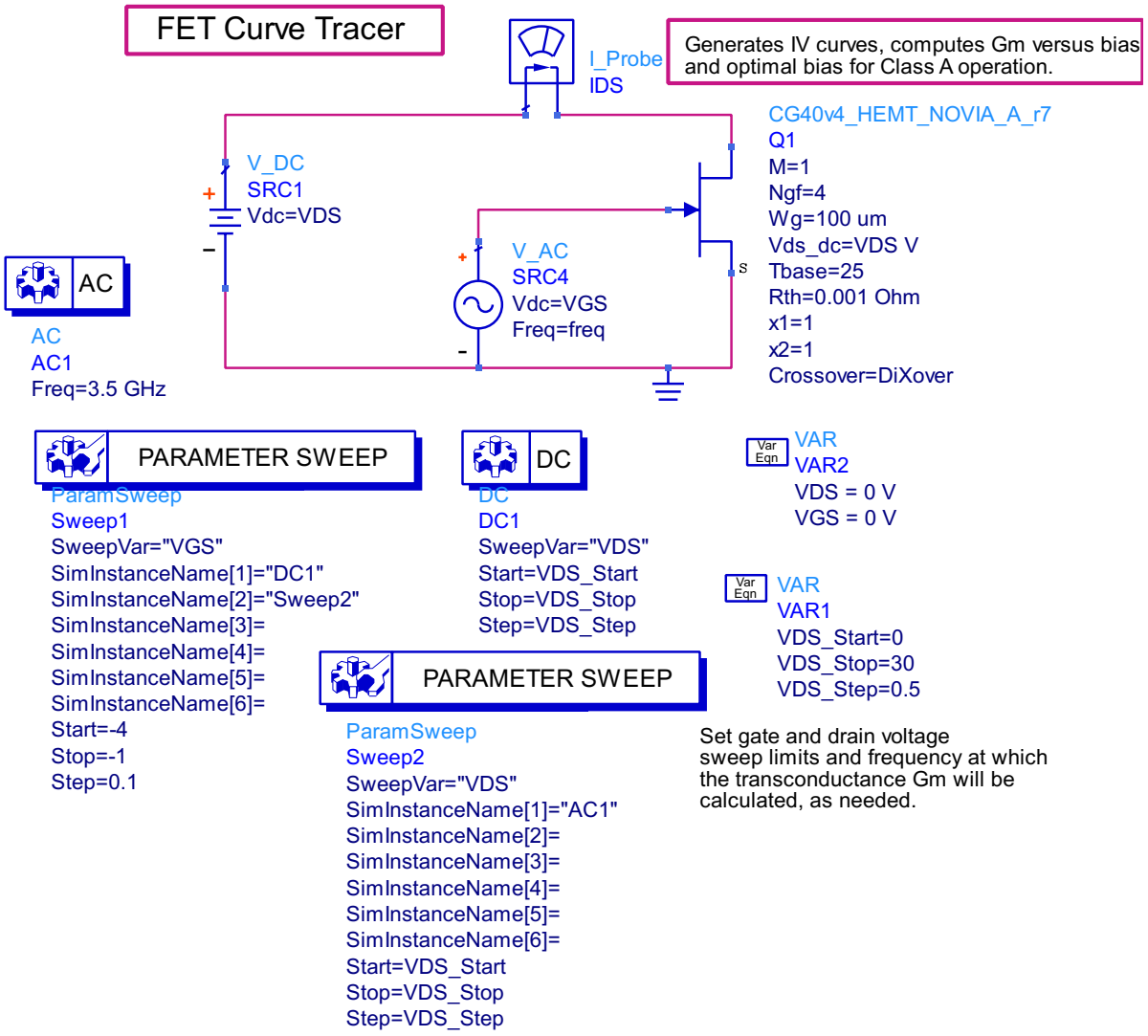
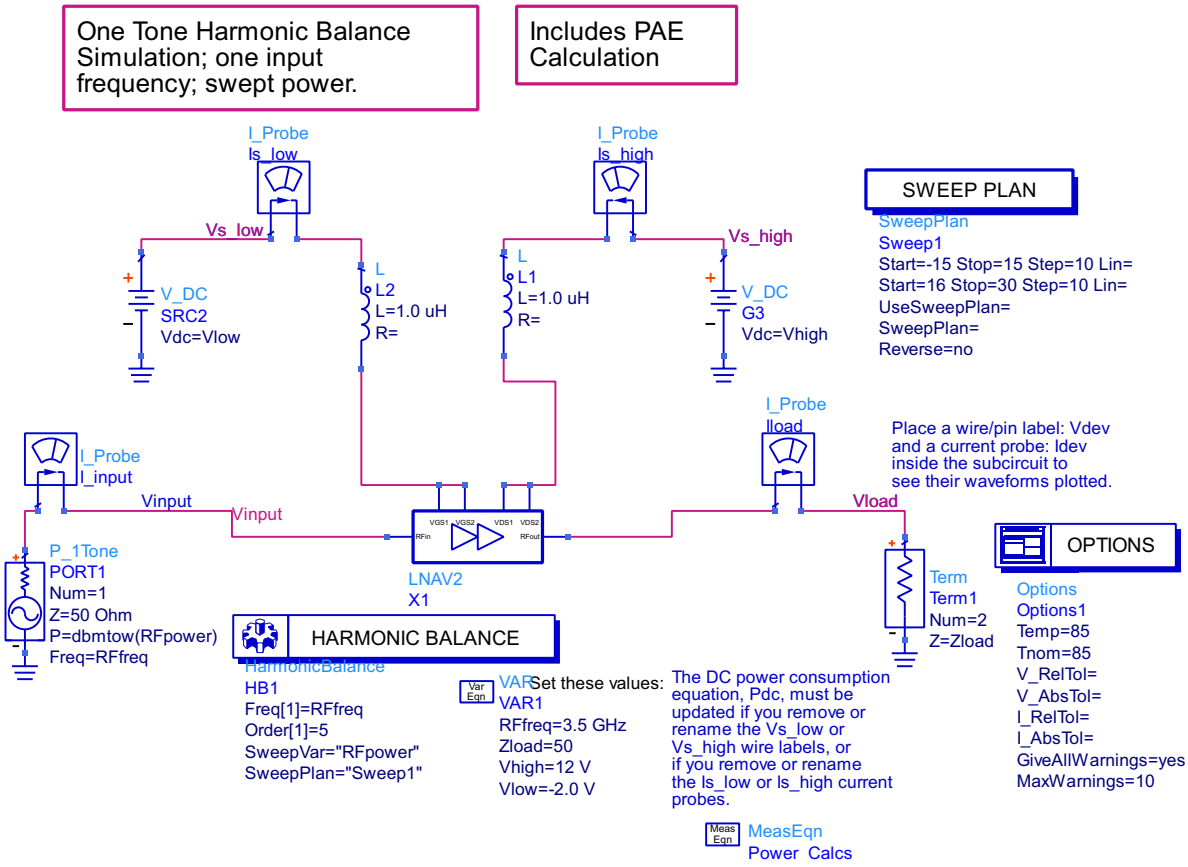
Appendix A

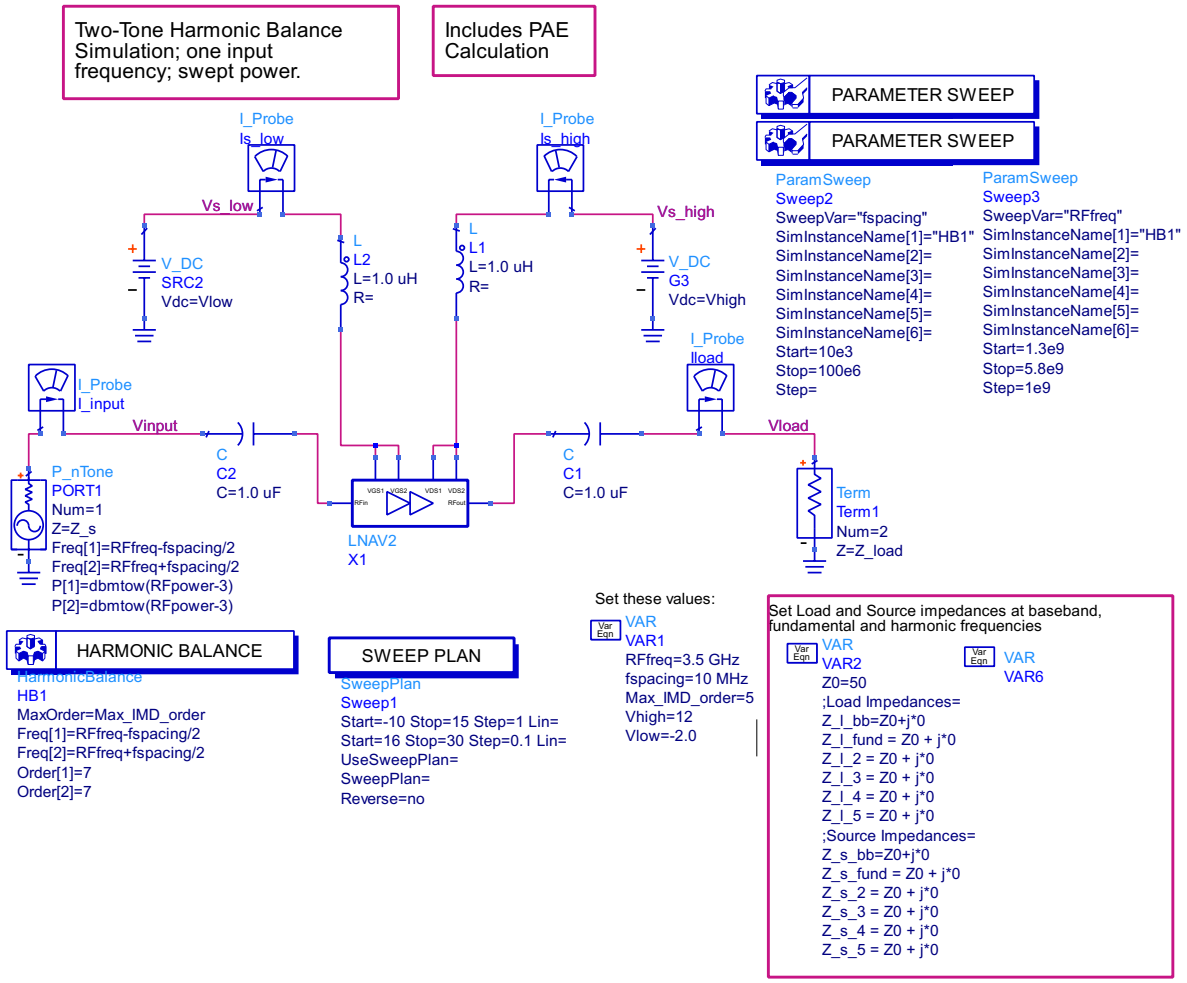
A.1 Testench for Bias



A.2 Testbench for Single-tone analysis



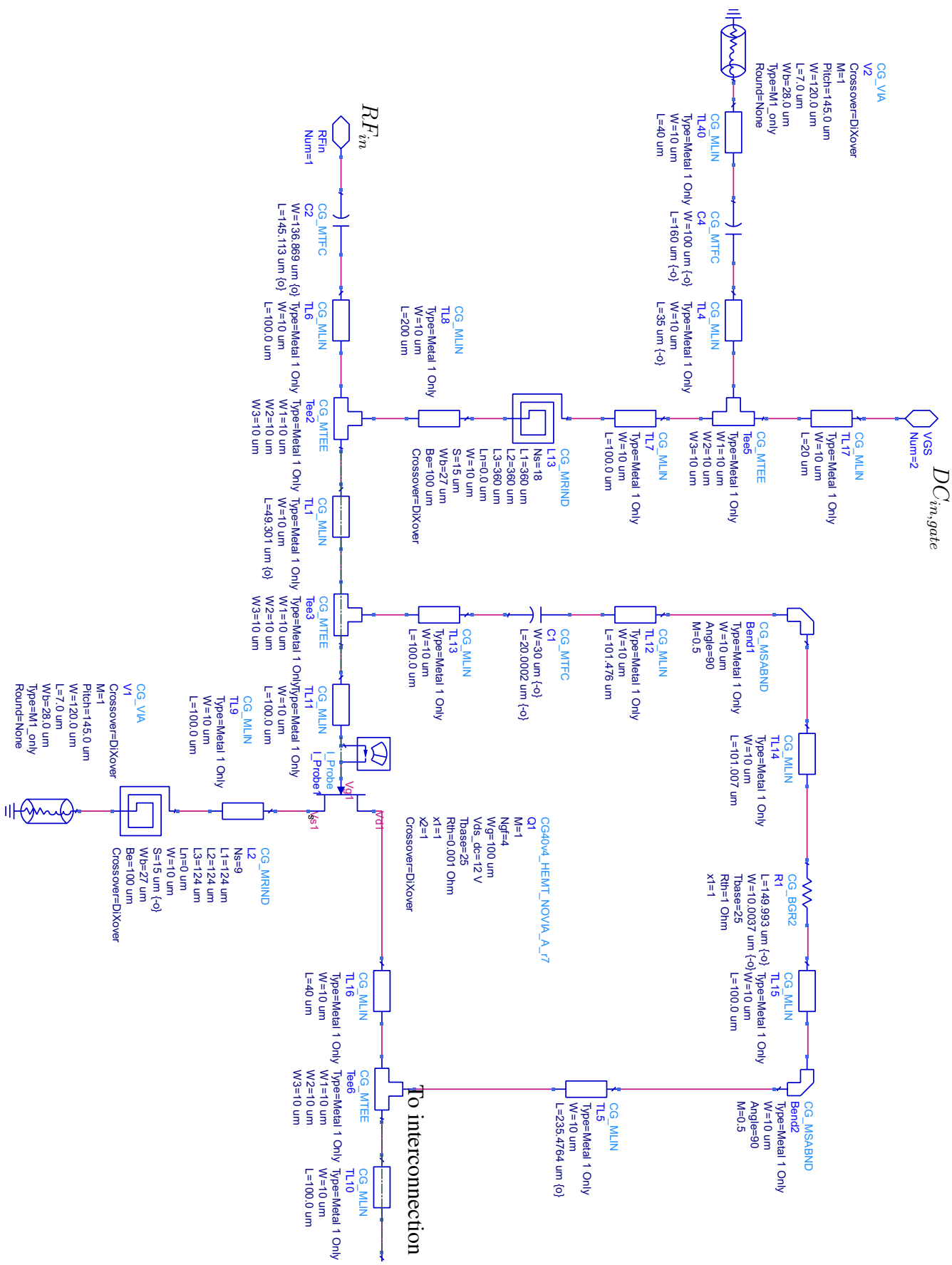
A.3 Testbench for Two-tone analysis



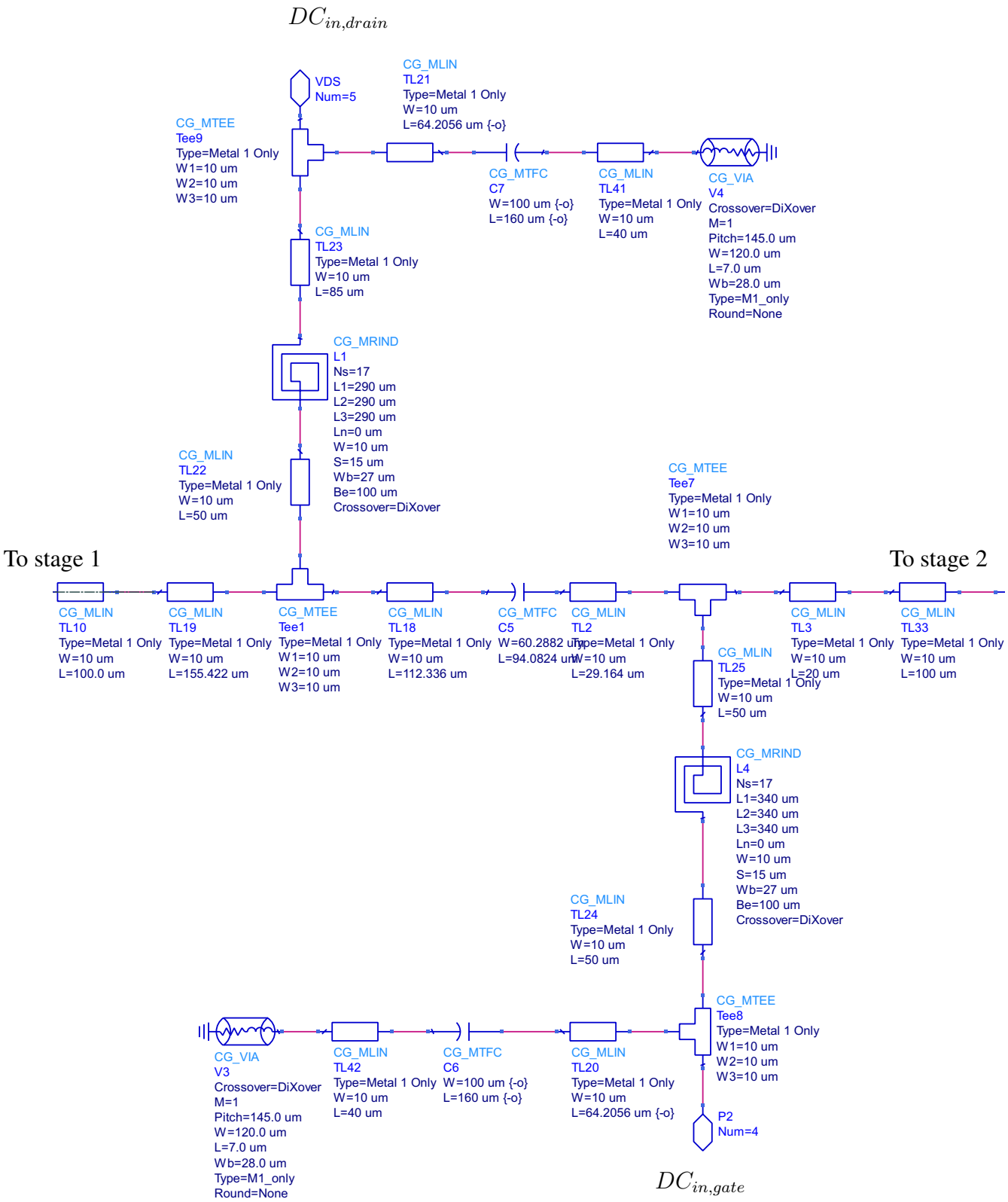
A.4 Testbench for Small-signal analysis

Appendix B

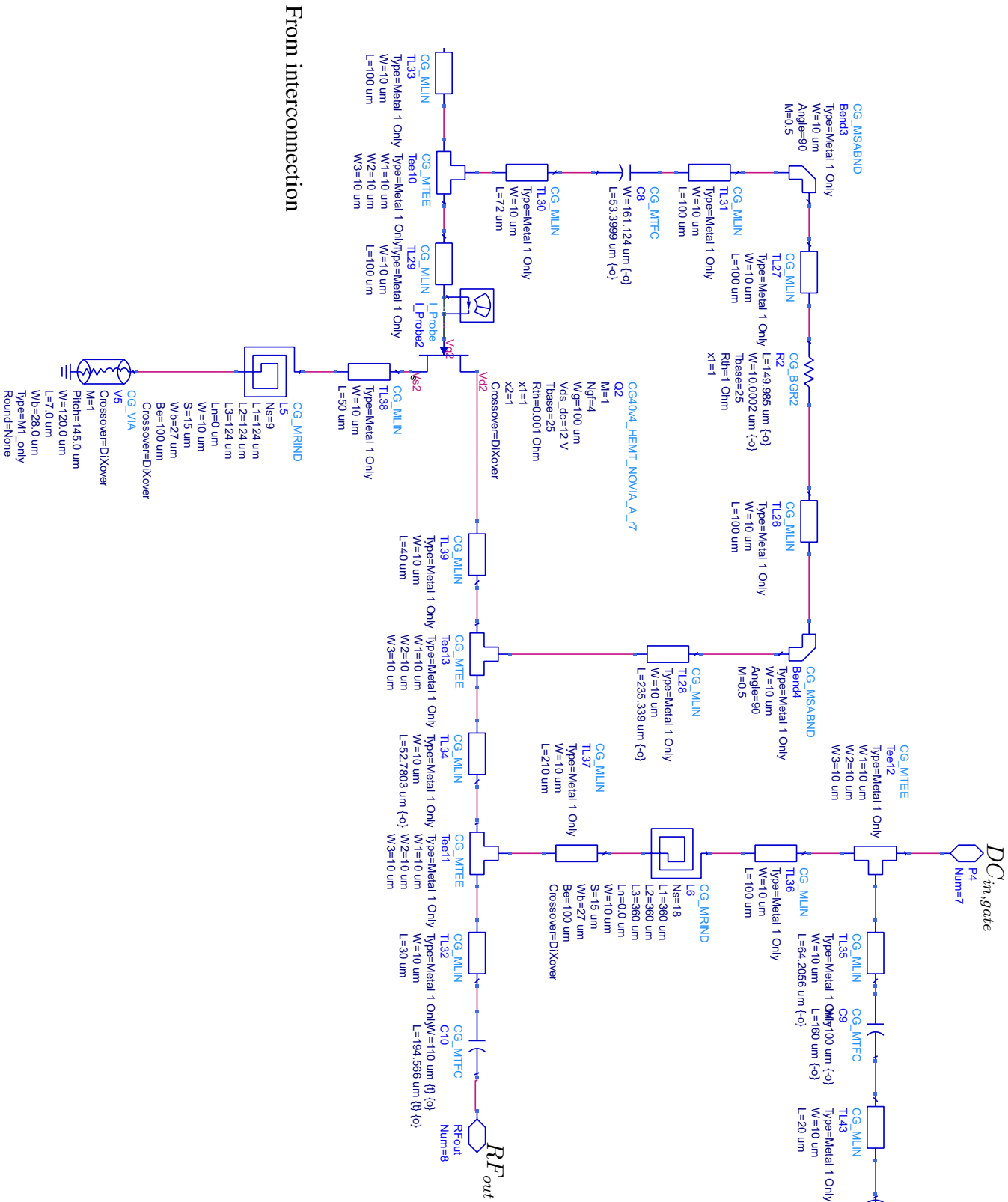
B.1 Input network



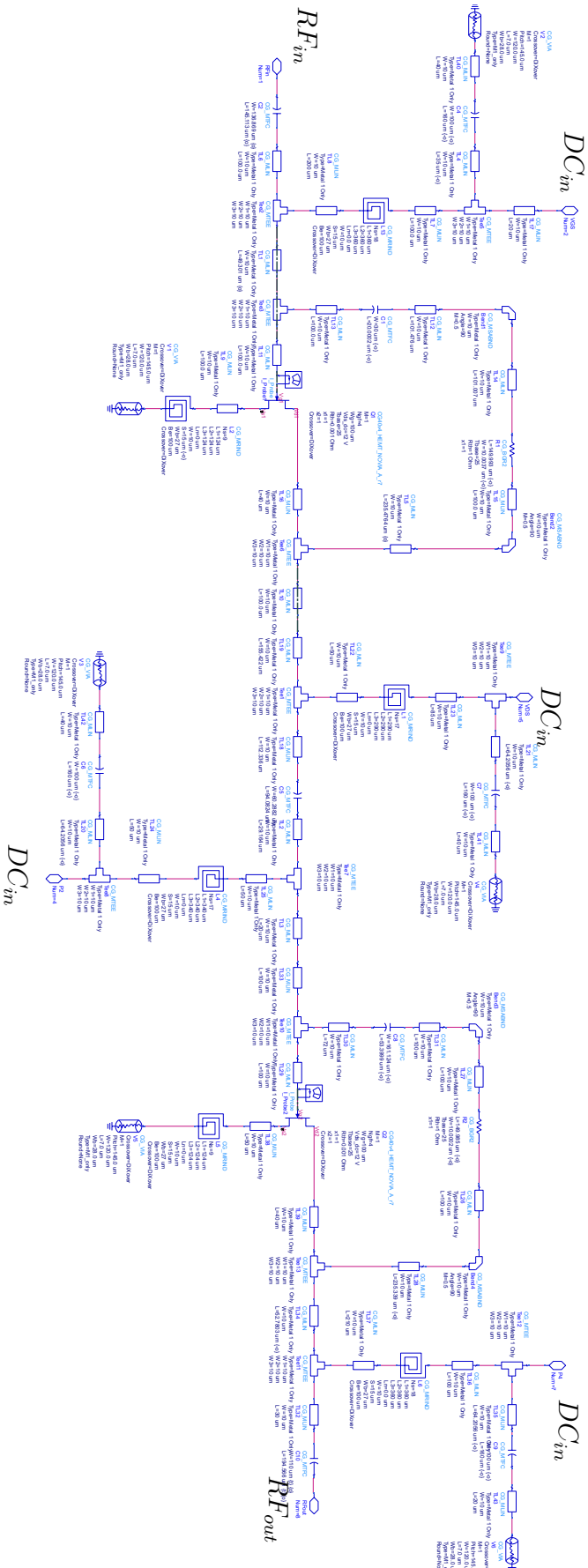
B.2 Interconnection network



B.3 Output network



B.4 Full schematic



Appendix C

C.1 Electromagnetic modelling

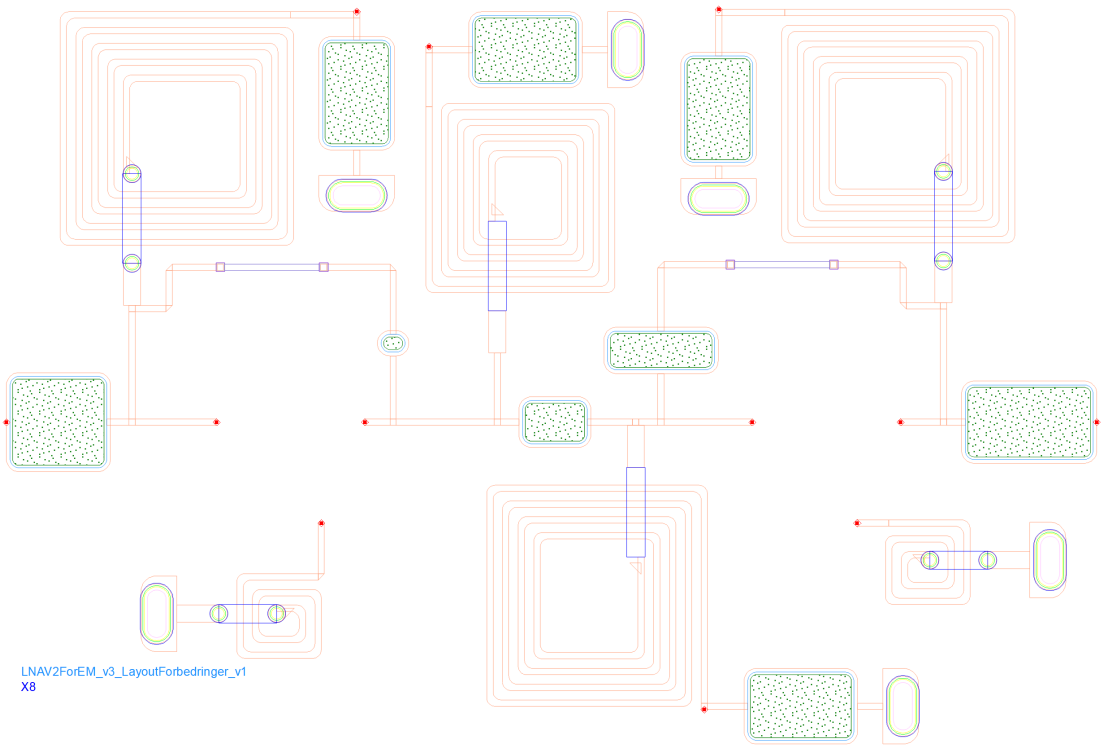


Figure 1: The generated electromagnetic model based on the layout.

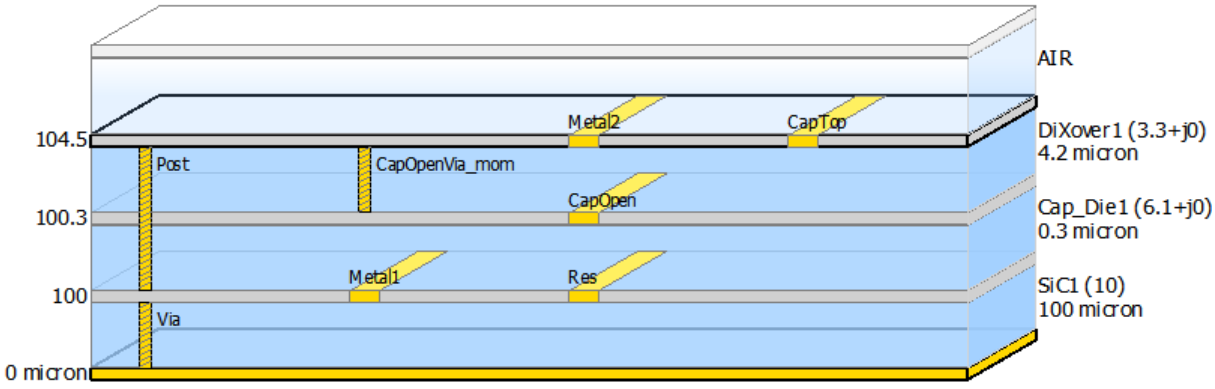


Figure 2: Substrate model used for electromagnetic simulations in ADS.