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Generic operational amplifier for MCU integration

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Master of Science in Electronics
Submission date: June 2017
Supervisor: Trond Ytterdal, IES
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Problem Description

An operational amplifier is a versatile building block for analog circuits and is used in a vast range of applications. Traditionally, operational amplifiers are made as stand alone ICs or they are completely integrated in an IC as part of a larger analog system.

The main objective in this assignment is to specify and design a generic operational amplifier system that can be integrated in an MCU as a general purpose building block. The inputs and output of the operational amplifier should be available on pins such that it is possible to connect/configure the operational amplifier for different functions by adding external passive components (gain stage, integrator, buffer, etc.). It could also be considered adding configurable internal components (i.e. resistors, capacitors) such that the operational amplifier can be set up to implement various functions without the need for external components.

Abstract

The versatility and useability of the opamp makes it widely used in hardware design. Thus having a general purpose opamp built in to the MCU can save many hardware developers both time, effort and money. As Microchip's popular Atmel AVR line of MCUs doesn't yet have this as an option.

This thesis will attempt to design a general purpose opamp in Atmel's 59k91 130nm CMOS technology based on Microchip Atmel's specifications. The main specifications are: rail-to-rail input and output ($\pm$100mV on output), a GBW of 3MHz and an open loop gain of 90dB. This thesis discusses opamp design and the specifics of the chosen design. Because of the requirement for rail-to-rail operation on both inputs and on the output some special considerations had to be made. This design is a two stage amplifier using dual input stages with constant g_m control by way of quadroupling the bias current when only one input pair is active, and a class AB output stage with floating bias. The first stage also incorporates a modified telescopic cascode to meet the requirement for open-loop gain.

The design meets all specification requirements in the nominal corner except for stability, and it falls short in some other corners. Further tweaking is thus necessary before layout and implementation. In addition, the design needs to be fitted with the switches needed for integration with the MCU power gating.

Preface

I would like to thank my supervisors Trond Ytterdal and Torgeir Fenhem for all the help they provided even though they both were for the most part far away and communication had to go via email and Skype. I would especially like to thank Torgeir, without whom I would not have been able to complete this thesis. Thank you for all your help, and for putting up with me through all the long Skype calls.

I would also like to thank my parents Ingrid and Geir, and my sister Helene. Thank you for your encouraging words and emotional support during my work on this thesis, and thank you for never doubting in me. It has meant a great deal to me during my work.

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List of Abbreviations and Acronyms

ADC	Analog to Digital Converter
CMOS	Complementary Metal Oxide Semiconductor
CMRR	Common-mode Rejection Ratio
DMA	Direct Memory Access
FET	Field Effect Transistor
FOM	Figure of Merit
GBW	Gain-Bandwidth product
MCU	Microcontroller Unit
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
Opamp	Operational Amplifier
OTA	Operational Transconductance Amplifier
PM	Phase Margin
PSRR	Power Supply Rejection Ratio
SNR	Signal-to-Noise Ratio
TBD	To Be Decided
vcm	Common Mode Input Voltage

Chapter 1

Introduction

The microcontroller is perhaps the most versatile electronics component in the World today. It powers everything from car infotainment systems to microwaves, computer keyboards and TV remotes. A big part of what makes the microcontroller so versatile is the on-board peripherals. These can range from UART and SPI communications to timers and USB and DMA controllers. Another very versatile electronics component, especially in analog electronics, is the operational amplifier. Depending on how the differential inputs and single ended output are connected its use cases include as an inverting or non-inverting amplifier, comparator, level detector, buffer, integrator or oscillator to name a few. Having a general purpose opamp as a peripheral in a microcontroller can thus provide the designer with a very versatile do-it-all package, with little need for external peripherals. This is especially true if the opamp is implemented in such a way that the designer can map the opamp inputs and outputs to pins on the MCU to use external components for feedback, and/or route the opamp output directly to other peripherals on the MCU. For instance, if the design incorporates an analog sensor, the opamp could be used as an amplifier feeding the sensor output directly to the on-board ADC in the microcontroller. While microcontrollers with on-board general purpose DACs already exist, the widely popular Atmel AVR line of microcontrollers does not yet feature any opamp-equipped MCUs.

1.1 Goal of Thesis

The goal of this thesis is to design and test an operational amplifier that fulfills the desired specifications discussed in chapter 3.1. The amplifier will be designed using Microchip's "59k91" CMOS process, a 130nm CMOS embedded flash process using the 5V transistor option. The design will ideally be ready to implement in the Atmel AVR line of microcontrollers from Microchip.

1.2 Thesis Outline

The rest of the thesis is as follows:

Chapter 2 - Background Theory: Contains important theory for the rest of the thesis.

Chapter 3 - Amplifier Design: Contains theories and approaches in amplifier design important to this thesis.

Chapter 4 - Implementation: A description of how the theories from chapter 3 were implemented into the final design.

Chapter 5 - Results: The simulation results from the completed amplifier design.

Chapter 6 - Discussion: Discusses the results found in chapter 5.

Chapter 7 - Conclusion: Concludes the thesis and outlines further work necessary before the design can be implemented in an MCU.

Chapter 2

Background Theory

The aim of this chapter is to give background theory relevant to the thesis. The chapter establishes many of the core terms and expressions used in the rest of the text to make it easier for the reader to follow, in addition to providing information on the principles behind some of the techniques used in the design.

2.1 Operational Amplifier Design

While there is a near endless range of opamp variations, most can be placed into one of a few important categories. First, we have the simple single stage opamp. It consists of a differential input pair, a current mirror and an active load to provide a bias current through the input pair. Such an amplifier is shown in fig. 2.1. It is the basis for the input stage of most opamps. The single ended output and simple design lets it go to very high frequencies, with a GBW described as

$$GBW = \frac{g_{m1}}{2 * \pi C_L} \tag{2.1}$$

Another common configuration is the telescopic OTA, shown in fig. 2.2. The cascodes increase the impedance at the output node, increasing gain. The GBW is unchanged from equation 2.1 however, and the power consumption is the same as the simple single stage. The reason for this is that the cascode only increases gain at lower frequencies.

Next we have the miller OTA, which forms the basics of the design in this paper. This configuration uses a compensation capacitance C_C to increase the stability of the opamp using the miller effect. The miller OTA shown in fig. 2.3 is the simplest variation, using the simple single stage opamp as the input stage and a single NMOS as the second stage. C_C provides feedback

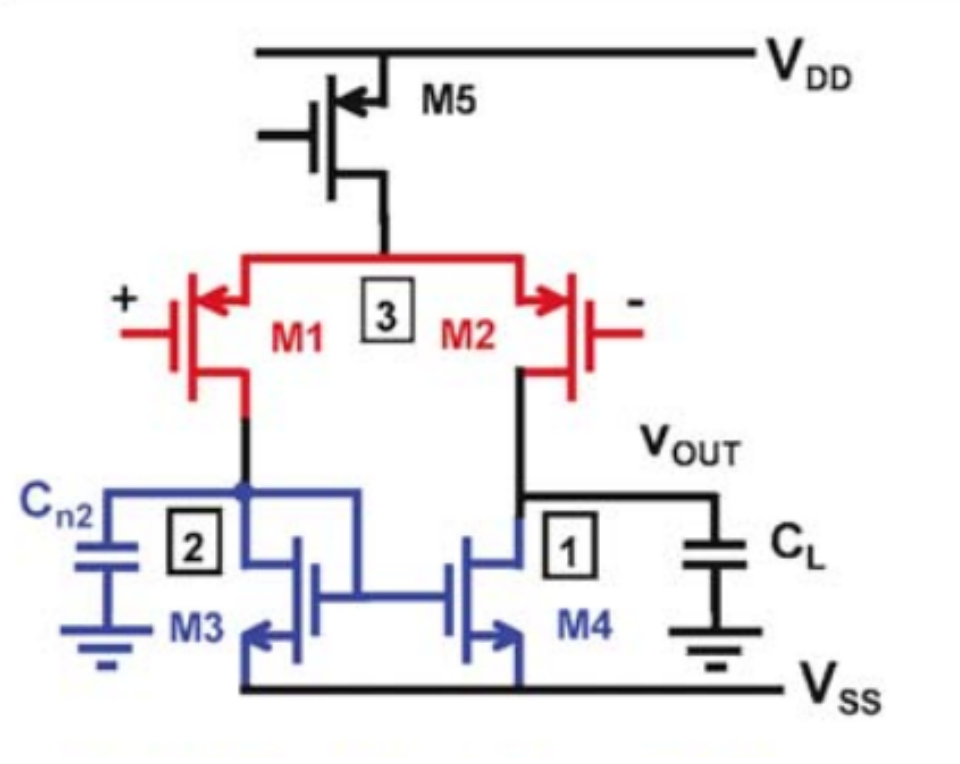

Figure 2.1: Simple single stage opamp [1]

from the output node to the input of the second stage. The GBW is still found to be the same as in equation 2.1, but since the load impedance to the first stage in this case is C_C the GBW now becomes equal to $\frac{g_{m1}}{2*\pi C_C}$. The miller compensation principle can be used in any two-stage amplifier, as discussed in chapter 3.2.

2.2 Amplifier Stability and Compensation

Stability is an important factor when designing an amplifier that can be used with negative feedback. The principle of negative feedback is that part of the output is connected to the input, in a way that detracts from the input signal. This way, if the output increases rapidly the negative feedback will decrease the input thus slowing the increase on the output. What is generally not desired is positive feedback, where the output signal adds to the input. When this happens, an increase in the output will increase the input, further increasing the output. This will force the output to one of the power rails, and can in some cases cause it to oscillate. Any amplifier will change the phase of the signal as it passes through, and if the amplifier is not designed right it will under some circumstances alter the phase so much

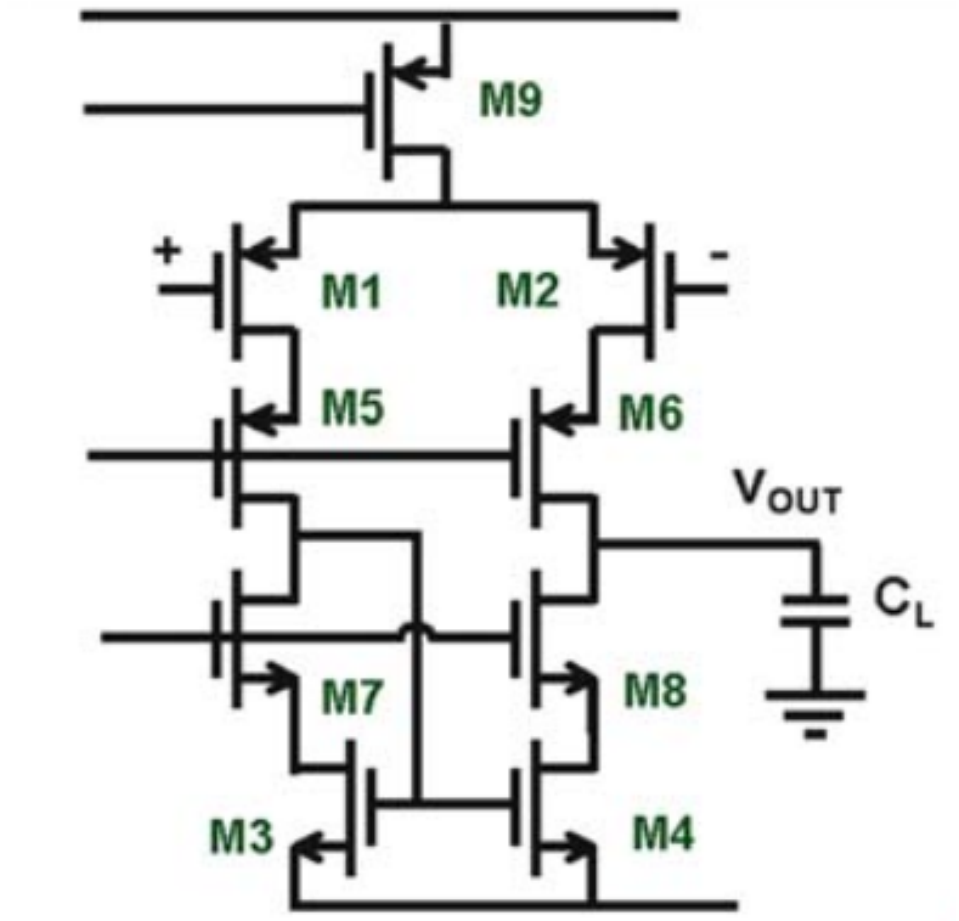

Figure 2.2: Telescopic OTA [1]

that the output signal essentially is inverted from the input. This will turn a negative feedback into a positive feedback, giving a drastically different effect than the one intended. This happens at a 180°phase change, and so the distance between this worst case scenario and the actual phase change is called phase margin. A higher margin is better, and the maximum possible margin is 180°.

2.3 Rail-to-Rail Inputs and Outputs

The positive and negative power inputs on an operational amplifier are often referred to as the power rails. In many applications, and low-voltage applications in particular, it is desired that the operational amplifier can handle input voltages in the entire range from the negative and up to the positive power rail. In addition, it is desired that the output voltage also can go all

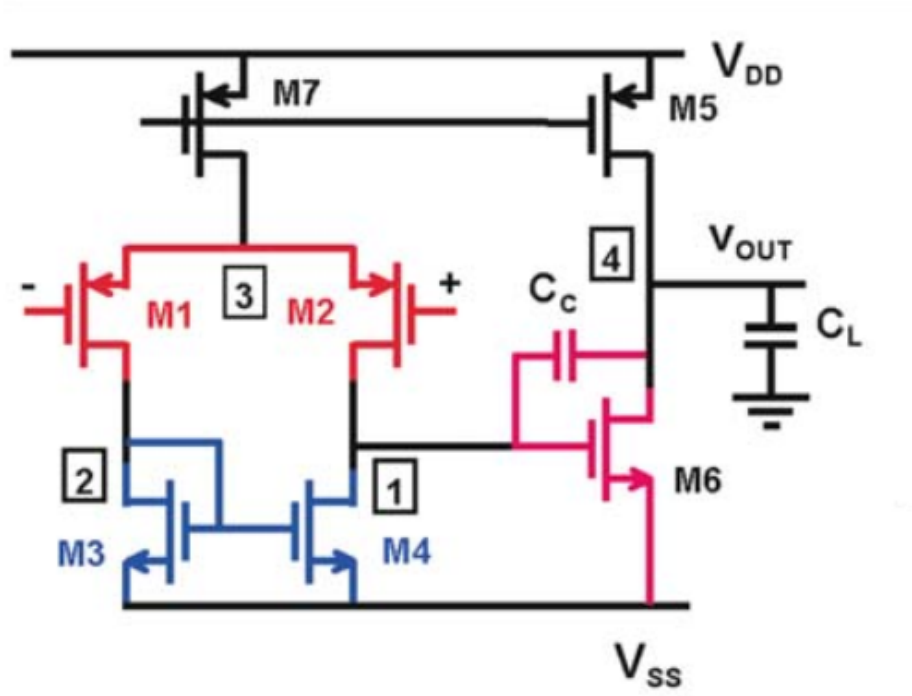

Figure 2.3: Simple miller OTA

the way from the negative rail and up to the positive rail. Hence the term rail-to-rail. This is to be able to use as large a voltage swing as possible, something that is important with low voltages since even the full rail-to-rail voltage swing isn't that large. Because the in- and output transistors need to be kept in the same region [1] at all times for the amplifier to function properly, it means that NMOS transistors require a minimum voltage before they will function as needed, and the inverse is true for PMOS. As a result, the in- and output stages need to be designed specially for rail-to-rail operation.

2.3.1 Rail-to-rail input stage

Rail-to-rail common-mode voltage swing at the input can only be obtained by using two input stages in parallel such that the common-mode (CM) voltage of one can reach the positive supply rail and that of the other the negative supply rail [2]. This is done using a NMOS input pair and a PMOS input pair in parallel. This way, at least one of the pair will always be active. However, this double input stage presents a challenge. When both transistor pairs are active, we have twice the transconductance compared to when

[1] Either weak or strong inversion, depending on the design

only a single pair is active. This is an issue because the transconductance in the first stage among other things affect the GBW of the entire amplifier, as discussed in chapter 3.2. There are several ways to compensate for this, and the method used in this design is to increase the current in the transistor pairs when the other pair is inactive [3]. An example of this is shown in fig. 2.4. Here, M_5, M_6 and M_7 provide extra current to the PMOS input pair (M_3 and M_4) when the NMOS pair (M_1 and M_2) turns off, and M_8, M_9 and M_{10} do the same for the NMOS pair. The way this works is that M_5 and M_8 work as switches that turn on when M_1/M_2 and M_3/M_4 turn off respectively. M_5 has the exact same size as M_1/M_2, and V_{b2} is set so M_5 starts conducting at the voltage where M_1/M_2 start turning off. The same goes for M_8 and M_3/M_4. This means that when the common-mode voltage is too low for the NMOS input pair to work, M_5 is conducting. The NMOS load current I_{R2} is drawn through M_5 and M_6, and is copied to M_7. Since M_6 and M_7 form a 1:3 current mirror, the current through M_7 is equal to $3 * I_{R2}$. This current is added to I_{R1}, effectively quadroupling the current through M_3/M_4. This will double the transconductance, thus returning the total g_m to the same level as it is when both input pairs are conducting. This works well in practice too, and we only see a $\approx 15\%$ increase in g_m at the points where the input pairs start turning off and the current mirror switches start conducting. This is shown in fig. 2.5.

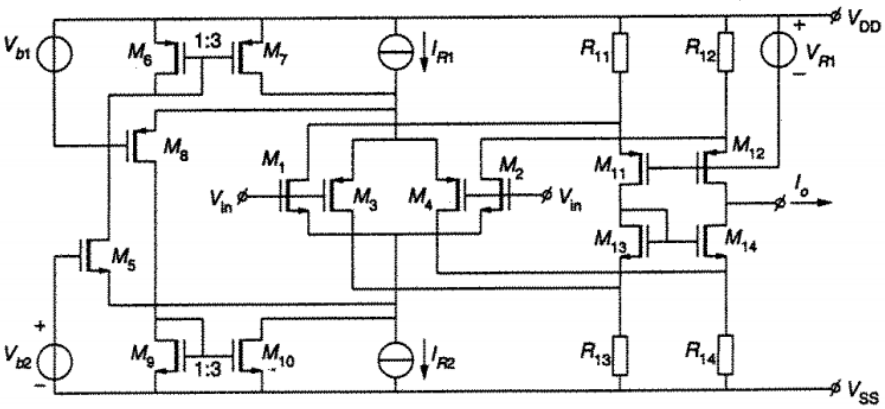

Figure 2.4: An opamp input stage with constant g_m control [3]

2.3.2 Rail-to-rail output stage

As with the input stage, a rail-to-rail output stage can only be achieved using both an NMOS and a PMOS output transistor. The most common rail-to-

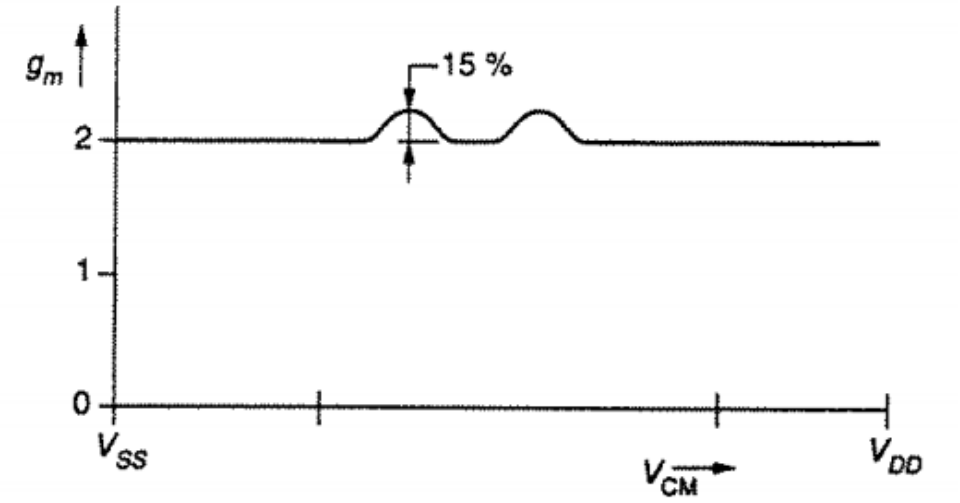

Figure 2.5: g_m as a function of common mode voltage [3]

rail configuration is the class AB amplifier, and this is also the configuration used in this thesis. The class AB is a good compromise between linearity and power consumption, and can drive more current demanding loads so a separate buffer stage becomes unnecessary.

Chapter 3

Amplifier Design

The aim of this chapter is to give a general overview of the high level design, and why the specific solutions were chosen. The design is a two-stage miller compensated amplifier. The first stage uses double input transistor pairs for rail-to-rail operation and a folded cascode for increased open-loop gain. The second stage is a single ended class AB rail-to-rail output with a floating class AB bias control built into the folded cascode of the first stage. The design is mainly based on the design described in [3], in combination with similar designs from [1] and [2].

3.1 Desired Specifications

Table 3.1 shows the desired specifications for this amplifier. These specifications were drawn up by Microchip at the beginning of this project.

Parameter	Condition	Min	Typical	Max	Unit
Operating Conditions					
Junction temperature	Within spec Functional[1]	-40 -40	25	125 145	°C
mix50vdd!		1.71/2.7[2]	3.0	5.5	V
mix50vss!			0		V
vdd_hvp!		3.0		5.5	V
DC Characteristics					
Current cosumption	i50en = '1' i50en = '0'		TBD	 50	μA nA
Input current			±100		pA
Input offset current			±100		pA
Input offset voltage			±100		mV
DC open loop gain			90		dB
Input common mode range		mix50vss		mix50vdd	mV
Output voltage swing		mix50vss +100 mV		mix50vdd -100 mV	mV
Power supply rejection ratio			70		dB
Common mode rejection ratio			70		dB
Transient Characteristics					
Startup time				10	μs
Slew rate			2		V/μs
AC Characteristics					
GBW			3		MHz
Phase margin			60		°
Notes					
Note 1: Reduced performance in temperature range 125°C - 145°C. Note 2: Reduced performance in suply range 1.71V - 2.7V					

Table 3.1: Desired amplifier specifications

3.2 System Overview

As mentioned in chapter 2.1, this amplifier is based on the miller OTA. Fig. 3.1 shows a high level overview of a generic miller-compensated two-stage opamp. It is also representative of the design used in this thesis. The design methodology used is taken from Chapter #5 of "Analog Design Essentials" by Willy M.C. Sansen [1]. The transconductances in the two stages, along with the compensation capacitance C_C will be calculated based on the desired GBW. The individual stages will then be designed for rail-to-rail operation, and the first stage will be modified to achieve the desired open-loop gain. The relationship between GBW, transconductance and the compensation capacitance is described as:

$$GBW = \frac{g_{m1}}{2\pi C_C} \tag{3.1}$$

$$f_{nd} = \frac{g_{m2}}{2\pi C_L} \tag{3.2}$$

We see that the GBW is independent from the transconductance in the second stage, g_{m2}. This is expected, since an increase in g_{m2} will decrease the bandwidth and thus not affect the GBW. By definition, a two-stage amplifier has two nodes at high impedance [1]. This translates to two poles, a dominant and a non-dominant one. Since the non-dominant pole f_{nd} determines the stability of the amplifier, it is important that f_{nd} is large enough not to cause problems. A good starting point is $f_{nd} \approx 3 * GBW$ [1]. We now have two equations (3.1 3.2) containing all our design variables. Unfortunately, we only have three known quantities (GBW, C_L and f_{nd}) which also gives us three unknowns (g_{m1}, g_{m2} and C_C). With only two equations it is not possible to solve for three unknowns, so it is necessary to choose one unknown in order to be able to calculate the other two.

Both g_{m1} and g_{m2} work on a "the larger the better" basis, but this is not the case for C_C. C_C provides a tradeoff between GBW and stability; a larger C_C increases stability but decreases GBW and vice versa. Because of this there is a certain range C_C should fall within, based on C_L and the required stability. [1] gives a good rule of thumb that gives a decent place to start: C_C should be between $\frac{1}{2}$ and $\frac{1}{3}$ the size of C_L and the non dominant pole f_{nd} should be around 3 GBW. This will result in a phase margin around 70°, and gives a rough equation that can be used as a starting point for the design:

$$\frac{g_{m2}}{g_{m1}} \approx 4\frac{C_L}{C_C} \tag{3.3}$$

From the specifications in section 3.1 we see that we desire a GBW of at least 3GHz with a C_L of 100pF. Due to the large area of the capacitors available to the process, we will be setting C_C to 10pF. We can now use equation

3.2 to calculate g_{m1}: $3 * 3MHz = \frac{g_{m1}}{2\pi 50pF \Rightarrow g_{m1} \approx 1.885 * 10^{-4}S}$. Solving equation 3.3 for g_{m2} we find: $\frac{g_{m2}}{1.885*10^{-4}S} \approx 4\frac{100pF}{10pF} \Rightarrow g_{m2} \approx 7.54 * 10^{-3}S$. Using the spreadsheet we can then use these numbers to calculate our transistor sizes.

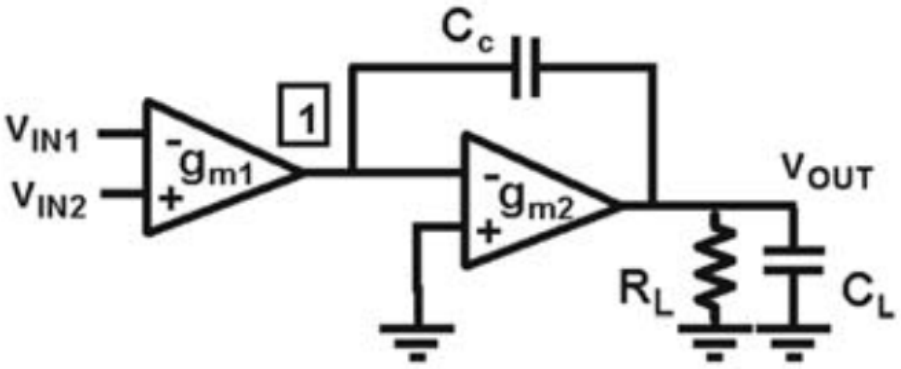

Figure 3.1: A generic two-stage opamp with Miller compensation [1]

3.3 First Stage

As discussed in chapter 2.3.1, the input stage consists of an NMOS and a PMOS input pair in parallel and a constant g_m control circuit. The design is based off a design found in [4], and similar designs are used in [3] and [1] as well.

3.4 Second Stage

The output stage in this project is based off of the output stage from [4], which is shown in fig. 3.2. Since we need to be able to drive a resistive load, the output stage needed to be a class AB design. This design was chosen because it fits our needs well and was well described both in [3] and [4]. It uses a floating current source to provide the bias required for AB-operation. One of the drawbacks of this design is that the quiescent current is dependent on variations in the power supply voltage. In addition, placing the output stage in cascade with the input stage places the class AB control in parallel with the cascodes in the input stage, reducing the gain. These drawbacks have been overcome by integrating the class AB control in the cascode output of the input stage, as shown in fig 3.3. Here, the class AB control (M19 and M20) has been placed in series with the cascoded output from the input stage. This removes the gain penalty from having these in

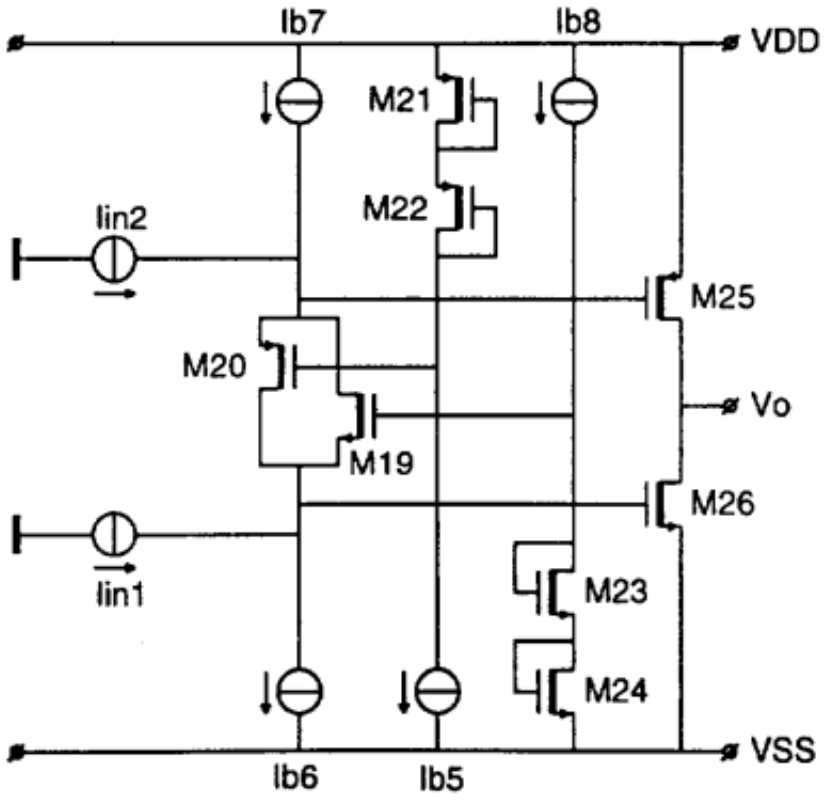

Figure 3.2: A class AB rail-to-rail output stage with translinear loop bias [4]

parallel. In addition, an identical floating current source (M27 and M28) has been added to the input branch of the cascoded current mirror. This gives both sides of the current mirror the same supply voltage dependency, effectively cancelling the effect.

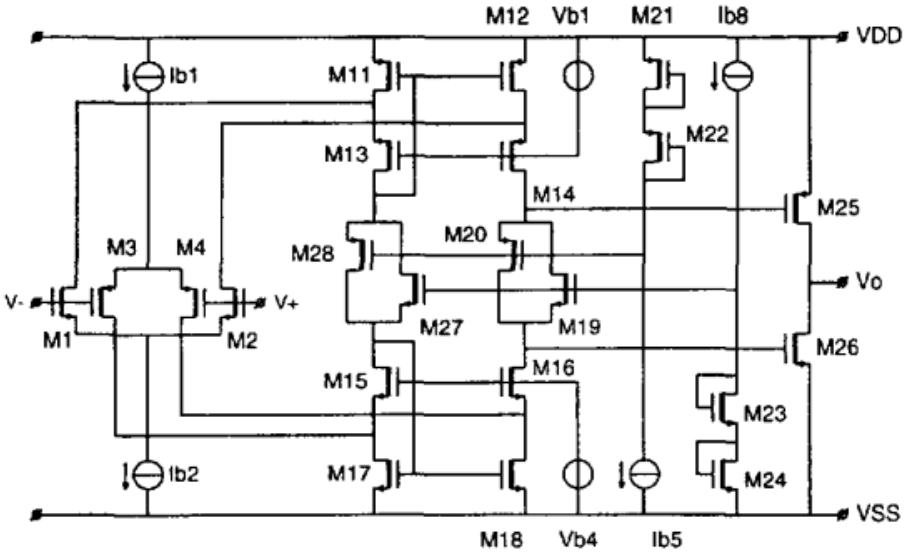

Figure 3.3: Floating AB control integrated into input stage cascode [4]

Chapter 4

Implementation

The aim of this chapter is to show how the design in chapter 3 was implemented in the 59k91 process. A process specific spread sheet made by a designer working at Microchip was used to calculate the transistor dimensions.

4.1 Bias Network

The bias network, shown in fig. 4.2 is a modified version of a bias network found in another Atmel product. It uses two $1uA$ reference currents generated by a separate bias block used in Atmel microcontrollers.This current is then copied through cascoded current mirrors and the controlling voltages are set by the current mirror branches and the MNCB and MPCB transistors set the cascode bias voltages. Similarly, the MrnB and MrpB transistors set the bias for the 3:1 current mirror switches discussed in chapter 3.3.

4.2 Input Stage

The input transistors were designed for the g_m calculated in chapter 3.2. As discussed in 2.3.1, the g_m is doubled when both input pairs are conducting. Because of this each of the four input transistors are designed to have half of g_{m1}. When only one transistor pair is operating the g_m control will double its g_m, keeping the transconductance where it needs to be. The acive load is provided by MP0/MPC0 for the PMOS pair and MN0/MNC0 for the NMOS pair. These are part of the current mirrors in the bias network and are simply scaled using m-factor to give the I_d necessary to give the transistors the correct g_m. Both the input transistors and their current were scaled up from their initial values during testing to optimize performance.

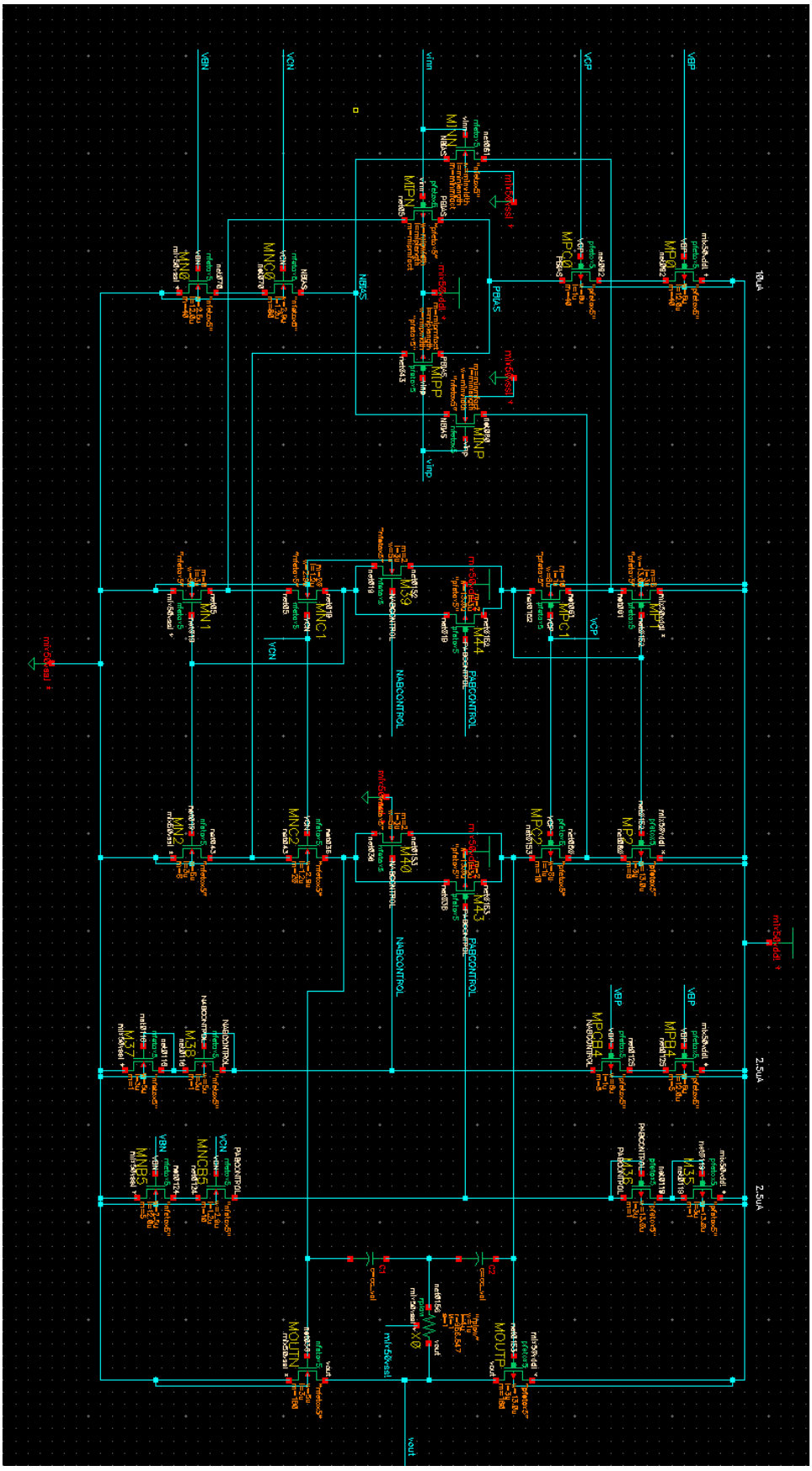

Figure 4.1: Final realization of opamp input and output stages

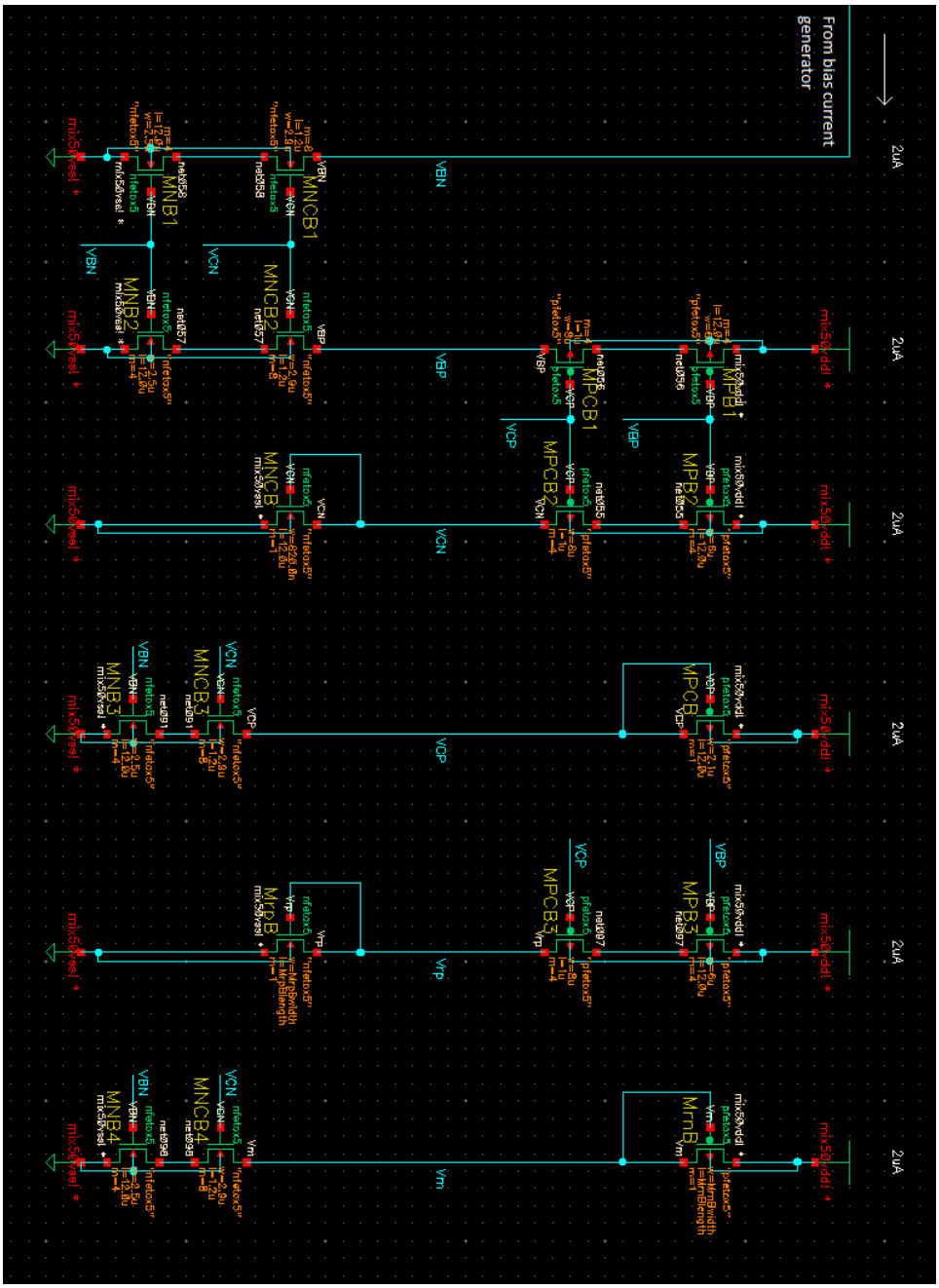

Figure 4.2: Final realization of opamp bias network

4.2.1 Constant gm Control

Figures 4.3 and 4.4 show the 1:3 current mirrors controlling the g_m of the NMOS and PMOS input pairs respectively. The V_{rn} and V_{rp} bias voltages are generated by the MrnB and MrpB transistors as seen in fig. 4.2. V_{rn} and V_{rp} were set so that Mrn and Mrp transistors will turn on and off at the same vcm as the input pairs. Because of this, Mrn and Mrp are also identical in size and m-factor to the PMOS and NMOS input transistors respectively. M25/26 and M29/30 are simple 1:3 current mirrors. This concept of constant g_m control is discussed in chapter 2.3.1.

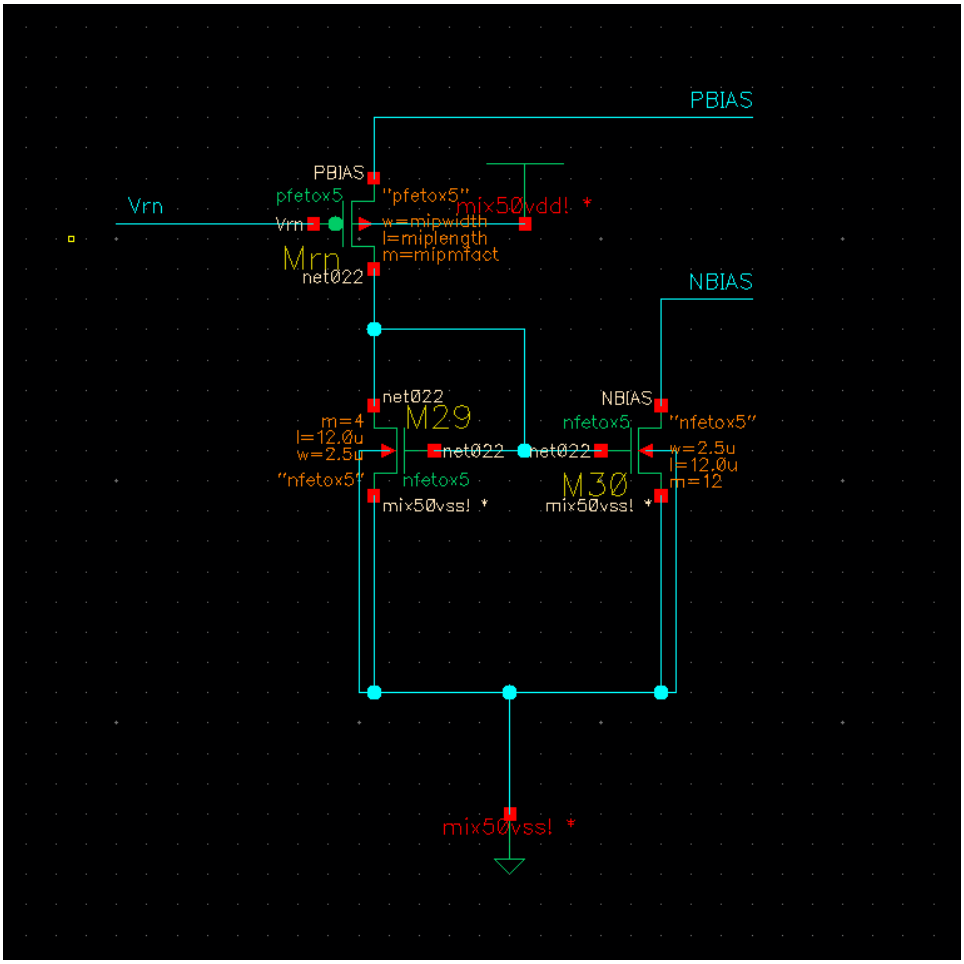

Figure 4.3: Constant g_m implementation for NMOS input pair

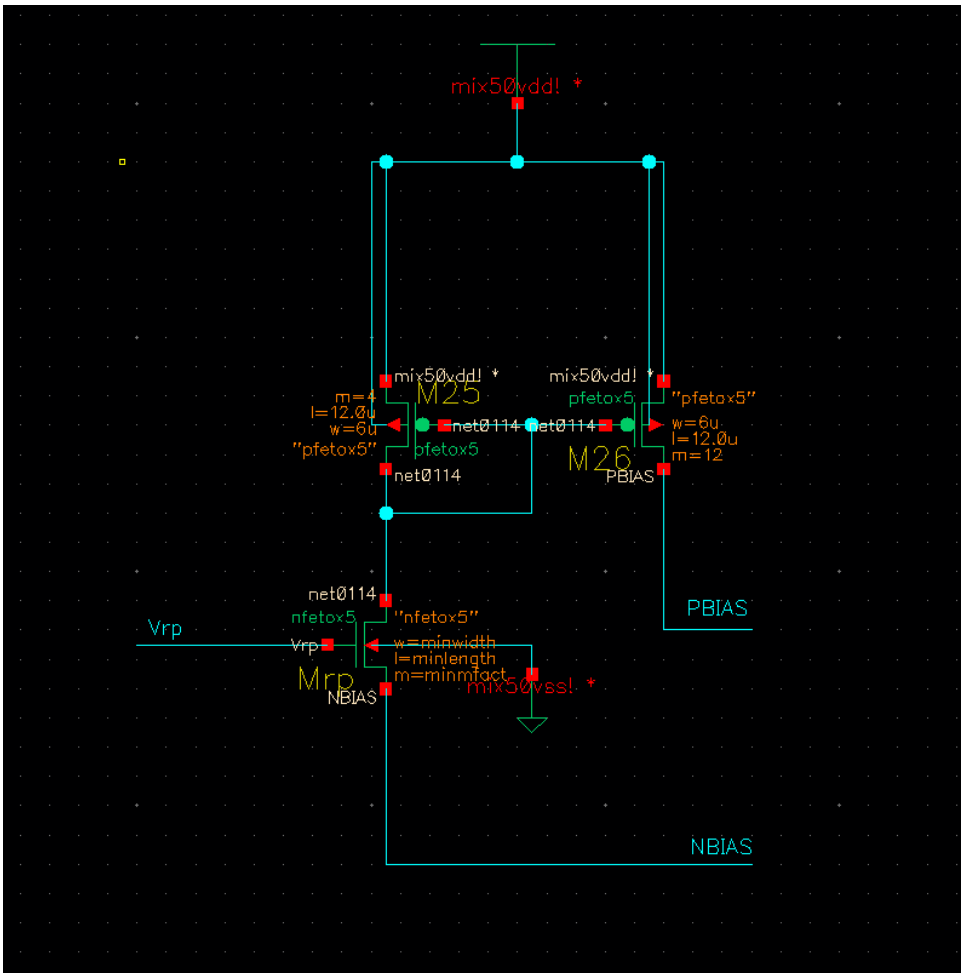

Figure 4.4: Constant g_m implementation for PMOS input pair

Chapter 5

Results

Parameter	BCL[1]	WCL[2]	Unit
DC Characteristics			
Current consumption	522.8	655.8	μA
Input current	0		pA
Input offset voltage	1.68		mV
DC open loop gain	109.2	94.39	dB
Maximum input common mode voltage	mix50vdd! + 1.6V		V
Minimum input common mode voltage	mix50vss! - 1.6V		V
Maximum output voltage	mix50vdd! - 0	mix50vdd! - 7	mV
Minimum output voltage	mix50vss! + 1.2		mV
Power supply rejection ratio	93		dB
Common mode rejection ratio	119		dB
Transient Characteristics			
Slew rate	2.49	2.39	V/μs
AC Characteristics			
GBW	4.418	3.592	MHz
Phase margin	87.03	49.98	°
Notes			
Note 1: Best Case Load: $R_L \geq 1G\Omega$, $C_L = 0pF$ Note 2: Worst Case Load: $R_L = 10k\Omega$, $C_L = 100pF$ **Nominal parameters:** mix50vdd! = 5.5V, temperature = 25°C and nominal process corner			

Table 5.1: Final simulation results, nominal

All simulations in this chapter were made using the Cadence Spectre simulator. Unless stated otherwise, all simulations were performed at mix50vdd! = 5.5V with a load of $C_L = 100$pF and $R_L = 100$k Ω, using a 100 point monte

carlo mismatch simulation using Atmel's nom_mm parameter for nominal mismatch. To improve readability, most figures can be found in appendix D. Chapter 6.6 in [5] was used as guide for the set-up of the various tests.

5.1 DC Characteristics

5.1.1 Current Consumption

Current consumption was measured using DC analysis, simulating current drawn from the voltage source driving the mix50vdd! power rail. The measured current does not include the 2μA bias current from the ptatbias block.

5.1.2 Input Current

The input current was simulated using DC analysis, measuring the current drawn from the voltage source driving the common-mode input signal to the amplifier input pairs. The measured values were in the atto- and zeptoampere ranges.

5.1.3 Input Offset Current

Given the results from the input current simulations this test was deemed redundant and thus not conducted.

5.1.4 Input Offset Voltage

Input offset voltage was simulated by connecting the output of the amplifier to the negative input and applying a voltage to the positive input. Offset is calculated as the difference between positive and negative input voltages. Figure 7.8 shows a histogram plot of the 100 points from the monte carlo simulation. The value given in table 5.1 is the mean value. As can be seen in fig. 7.9, the worst offset voltages measured are ± 3.0mV.

5.1.5 DC Open Loop Gain

Parameter	**Min**	**Max**	**Unit**
Gain	-47.23	133.7	dB
GBW	676.7	$6.75*10^6$	Hz
Phase margin	41.22	124.1	°

Table 5.2: DC open loop gain, GBW and stability across 600+ corners

Parameter	**Values**	**Unit**
Temperature	-40 25 125	°C
mix50vdd!	2.7 5.5	V
R_L	10k 100G	Ω
C_L	0 100p	F
vcm	0 0.2 mix50vdd!/2 mix50vdd!-0.2 mix50vdd!	V
model group	bcs wcs sfc fsc nom	

Table 5.3: Corners setup for gain, GBW and phase margin simulations

		Temp	**mix50vdd!**	**vcm**	R_L	C_L	**model group**
Gain	Min	-40	5.5	5.5	10k	0/100p	bcs
	Max	-40	2.7	1.35	100G	0/100p	bcs
GBW	Min	-40	2.7	2.7	100G	0/100p	wcs
	Max	-40	2.7	0.2	100G	0	bcs
PM	Min	-40	2.7	2.5	100G	100p	bcs
	Max	25	2.7	0	10k/100G	0/100p	wcs

Table 5.4: Best and worst case simulations of gain, GBW and phase margin with corresponding corners

Open loop gain, GBW and phase margin was simulated using Spectre single point AC simulations across a variety of corners. The corners used were temperature, C_L, R_L, common mode and process variations. The simulation was run twice, once at mix50vdd! = 2.7V and once at mix50vdd! at 5.5V. The complete results can be found in an excel spreadsheet in the digital attachments folder. As can be seen in table 5.2 all parameters varied wildly across the 600+ corners. Note that GBW and phase margin can only be calculated when the DC open loop gain is greater than 1 dB. The minimum values thus correspond to the worst cases that were actually calculateable.

5.1.6 Input Common Mode Voltage

Spectre Region Parameter	
0	Off
1	Triode
2	Saturation
3	Subthreshold
4	Breakdown

Table 5.5: The values of the region parameter in Spectre and corresponding CMOS operating regions

The common mode range of the input transistor pairs was measured as the range where the input transistors themselves stay in either saturation or subthreshold regions. The plots in fig. 7.11 show the input transistor regions as simulated by Spectre. The region parameter in Spectre changes value according to region, as shown in table 5.5. The green plot corresponds to the MIPN and MIPP p-mos input pair and the red plot to the MINN and MINP n-mos input pairs. All four transistors are plotted, but as they line up perfectly only the plots for MINP and MIPP are visible.

5.1.7 Output Voltage Swing

The output voltage swing was tested using a single point sweep of the common mode voltage on the amplifier inputs and measuring the output voltage. The four corners used are $C_L = 0/100\text{pF}$ and $R_L = 10\text{k}/100\text{G}\Omega$. Simulation results can be seen in figures 7.12 and 7.13. The red and yellow plots in fig. 7.12 refer to the corners where $R_L = 10\text{k}\Omega$.

5.1.8 Power Supply Rejection Ratio

vcm [mV]	**Min [dB]**	**Mean [dB]**	**3σ**
mix50vss! - 200	67.28	67.88	68.76
mix50vdd!/2	86.06	92.98	112.603
mix50vdd! - 200	75.60	76.76	78.54

Table 5.6: Simulated PSRR at various vcm voltages

PSRR was simulated using an AC source in series with the DC source feeding the mix50vdd! power rail and the amplifier connected as a buffer (output fed back to negative input and input signal fed only to positive input). Table 5.6 shows an overview of the values simulated at the different common-mode voltages. Figures 7.14, 7.15 and 7.16 show histogram plots of the 100 point monte carlo simulation results for vcm = mix50vss! + 200mV, mix50vdd!/2 and mix50vdd! - 200mV respectively.

5.1.9 Common Mode Rejection Ratio

vcm [mV]	**Min [dB]**	**Mean [dB]**	**3σ**
mix50vss! - 200	86.95	99.95	130.449
mix50vdd!/2	103.9	118.9	149.315
mix50vdd! - 200	96.54	110.4	142.307

Table 5.7: Simulated CMRR at various vcm voltages

CMRR was simulated using an AC source in series with the DC source driving the common-mode voltage to the inputs and with the amplifier connected as a buffer. Table 5.7 shows an overview of the most important simulation results. Histogram plots of the three simulations can be found in the appendix, as figures 7.17, 7.18 and 7.19.

5.2 Transient Characteristics

5.2.1 Startup Time

As no power switches or any other power gating measures were implemented in the design this test was not conducted.

5.2.2 Slew Rate

Slew rate was simulated by connecting the amplifier as a buffer and applying a step on the positive input. The step went from vcm - 0.5V to vcm + 0.5V, at vcm = mix50vdd!/2 and mix50vdd! = 5.5V. The actual slew rate was calculated by the slewrate function (10% to 90%) in ADE XL /Spectre, as seen in fig. 7.21. C4_1 (green plot) is a load of $R_L = 100\text{G}\Omega$ ($C_L = 0\text{pF}$) while C4_2 (yellow plot) is for a load of $R_L = 10\text{k}\Omega$ and $C_L = 100\text{pF}$. A plot of the input and output voltages can be found in fig. 7.20. C4_1 and C4_2 represent the same values as in fig. 7.20, while C4_0 (red) and C4_3 (cyan) represent loads of $10\text{k}\Omega/0\text{pF}$ and $100\text{G}\Omega/10\text{pF}$ respectively.

5.3 AC Characteristics

5.3.1 GBW

As mentioned in chapter 5.1.5, GBW was measured along with open loop gain and phase margin. GBW was calculated using the "unityGainFreq" in ADE XL. Complete results of GBW simulations (along with DC gain and phase) are found in the excel spreadsheet in the digital attachments folder.

5.3.2 Phase Margin

As mentioned in chapter 5.1.5, phase margin was measured along with open loop gain and phase margin. Phase margin was calculated using the "phaseMargin" calculator function in ADE XL. The complete results are found in the excel spreadsheet in the digital attachments folder.

Chapter 6

Discussion

The results chapter shows that the amplifier meets most specifications, but falters in certain corners and struggles with certain loads. The aim of this chapter is to analyze the results, and speculate as to the reason the results came out the way they did.

6.1 DC Gain, Stability and GBW

Gain, slew rate and GBW are close to spec, while stability is a definite issue with large load capacitances. As tables 5.2 and 5.4 show, the performance is worst when the common mode voltage is equal to or close to the rails. This can also be seen in fig. 7.9, where the offset changes drastically when vcm approaches either rail. According to the simulated input and output voltage ranges this shouldn't be a problem, which suggests that the issue isn't with the input or output transistors themselves. This leaves the input cascode, the output transistor bias and the input constant g_m control. The latter is unlikely to be the problem, as the constant g_m current mirrors did not affect the operation of the input transistors during the input voltage range simulations. It is more likely to be a combination of the cascode summing circuit and the floating class AB bias, as these heavily affect each other and the circuit is quite complex. Due to time constraints, this part of the amplifier has received little tuning or optimization beyond what was needed to make the amplifier work. In addition, any input signal beyond the rails cannot be amplified by the input transistors and is therefore lost. One would not expect a user to run the amplifier with a common mode input voltage equal to one of the rails, but the tests were included for transparency.

As mentioned at the beginning of this chapter, stability is the Achilles' heel of this amplifier particularly when compared to the desired specifications. As seen in table 5.1, the amplifier is very stable at low capacitive loads but drops out of spec by about ten degrees at 100pF capacitive load. This could be improved by increasing the compensation capacitance C_L, but this

will decrease the GBW as discussed in chapter 2.1. Both gain and GBW do have some headroom when compared to the desired specifications (tab. 3.1), so this is the first thing that should be attempted. If this is not sufficient, either the g_m of the input or output transistors could be increased further. The next step beyond this would again be to look at optimizing the input cascode/summing/AB control circuit. There was unfortunately not enough time to attempt these measures during this project.

6.2 Other Parameters

As table 5.1 shows, the amplifier is a slightly unbalanced one performance wise when compared to the desired specifications (table 3.1). Things like input offset voltage, input common mode voltage range, output voltage range, PSRR and CMRR are quite a lot better than needed. This is mainly down to the transistor sizes, as the input and output transistors are very large. This gives very good matching, but also increases area. Much of the reason for this is the need to increase the g_m during tuning of the amplifier. This is not the ideal solution, and there are probably ways to achieve similar performance with smaller transistors.

Chapter 7

Conclusion

In this thesis, a general purpose operational amplifier has been designed in Atmel's "59k91" 130nm CMOS embedded flash process with the 5V transistor option. According to simulations the amplifier has a nominal GBW of 3.6MHz, a gain of 94.4 dB and a phase margin of 50.0°at the maximum load of a 10kΩ resistor and a 100pF capacitor in parallel. The gain and GBW are according to the design specifications, but the stability is 10°lower than spec at this load. A 50°phase margin is still more than usable, even though it is lower than desired. All other specifications are within spec at nominal operation. As expected, the amplifier does not perform to spec when the inputs have a common mode voltage closer to either rail than a little over 100mV but beyond that it performs as expected again with the exception of the phase margin.

The amplifier is based on [3], with [1] used for the design methodology and reference. The design exists as a single schematic diagram, designed and simulated using Cadence Virtuoso and Atmel's device models for the process. Layout has not been part of this project.

7.1 Further Work

Going further, the first thing that needs to be done is to improve the phase margin. Beyond that, the inclusion of the switches required for the microprocessors' power gating is required before layout and post-layout simulation. In chapter 6 the summing/cascode/AB control circuit was found to be the part of the design that would benefit the most from further optimization. It would therefore be interesting to see if more optimization of is possible, and how that would improve overall performance. Adding positive feedback protection to the g_m control circuits could also be considered to avoid a possible scenario where both current mirrors are active (for specific common mode voltages at power voltages below 2.9V), though this did not seem to cause problems during simulation.

Appendix A: References

[1] W. M. Sansen, *Analog Design Essentials*. Springer International Publishing AG, 2006, ISBN: 978-0-387-25747-1.

[2] J. H. Huijsing and D. Linebarger, "Low-voltage operational amplifier with rail-to-rail input and output ranges," *IEEE Journal of Solid-State Circuits*, vol. SC-20, no. 6, pp. 1144–1150, 1985.

[3] E. Sanchez-Sinencio and A. G. Andreou, *Low-Voltage/Low-Power Integrated Circuits and Systems, Low-Voltage Mixed-Signal Circuits*, ser. IEEE Press Series on Microelectronic Systems. IEEE, 1999, ISBN: 0780334469.

[4] R. Hogervorst, J. P. Tero, R. G. H. Eschauzier, and J. H. Huijsing, "A compact power-efficient 3 v cmos rail-to-rail input/output operational amplifier for vlsi cell libraries," *IEEE Journal of Solid-State Circuits*, vol. SC-29, no. 12, pp. 1505–1513, 1994.

[5] P. E. Allen and D. R. Holberg, *CMOS Analog Circuit Design*, 2^{nd} Edition, ser. Oxford series in electrical and computer engineering. Oxford University Press, 2002, ISBN: 0-19-511644-5.

Appendix B: List of Transistors and Sizes

Table 7.1: Complete list of transistors and sizes.

Transistor	**Type**	**W**	**L**	**m-fact**
M25	P	6	12	4
M26	P	6	12	12
M29	N	2.5	12	4
M30	N	2.5	12	12
M35	P	13	3	1
M36	P	13	3	1
M37	N	5	3	1
M38	N	5	3	1
M39	N	5	3	2
M40	N	5	3	2
M43	P	13	3	2
M44	P	13	3	2
MINN	N	9	3	16
MINP	N	9	3	16
MIPN	P	8.2	3	16
MIPP	P	8.2	3	16
MN0	N	2.5	12	40
MN1	N	5	3	8
MN2	N	5	3	8
MNB1	N	2.5	12	4
MNB2	N	2.5	12	4
MNB3	N	2.5	12	4
MNB4	N	2.5	12	4
MNB5	N	2.5	12	5
MNC0	N	2.9	1.2	80
MNC1	N	2.9	1.2	20
MNC2	N	2.9	1.2	20

Cotinuation of table				
Transistor	**Type**	**W [μm]**	**L [μm]**	**m**
MNCB	N	0.82	12	1
MNCB1	N	2.9	1.2	8
MNCB2	N	2.9	1.2	8
MNCB3	N	2.9	1.2	8
MNCB4	N	2.9	1.2	8
MNCB5	N	2.9	1.2	10
MOUTN	N	5	3	180
MOUTP	P	13	3	180
MP0	P	6	12	40
MP1	P	13	3	8
MP2	P	13	3	8
MPB1	P	6	12	4
MPB2	P	6	12	4
MPB3	P	6	12	4
MPB4	P	6	12	5
MPC0	P	8	1	40
MPC1	P	8	1	10
MPC2	P	8	1	10
MPCB	P	2.1	12	1
MPCB1	P	8	1	4
MPCB2	P	8	1	4
MPCB3	P	8	1	4
MPCB4	P	8	1	5
Mrn	P	8.2	3	16
MrnB	P	14	12	1
Mrp	N	9	3	16
MrpB	N	4.5	12	1
End of table				

Appendix C: Layout

This appendix contains figures displaying the full schematics of the completed amplifier. While the amplifier is shown in full in the thesis itself, a full figure of the amplifier and close ups of the various parts are included here for the reader's convenience.

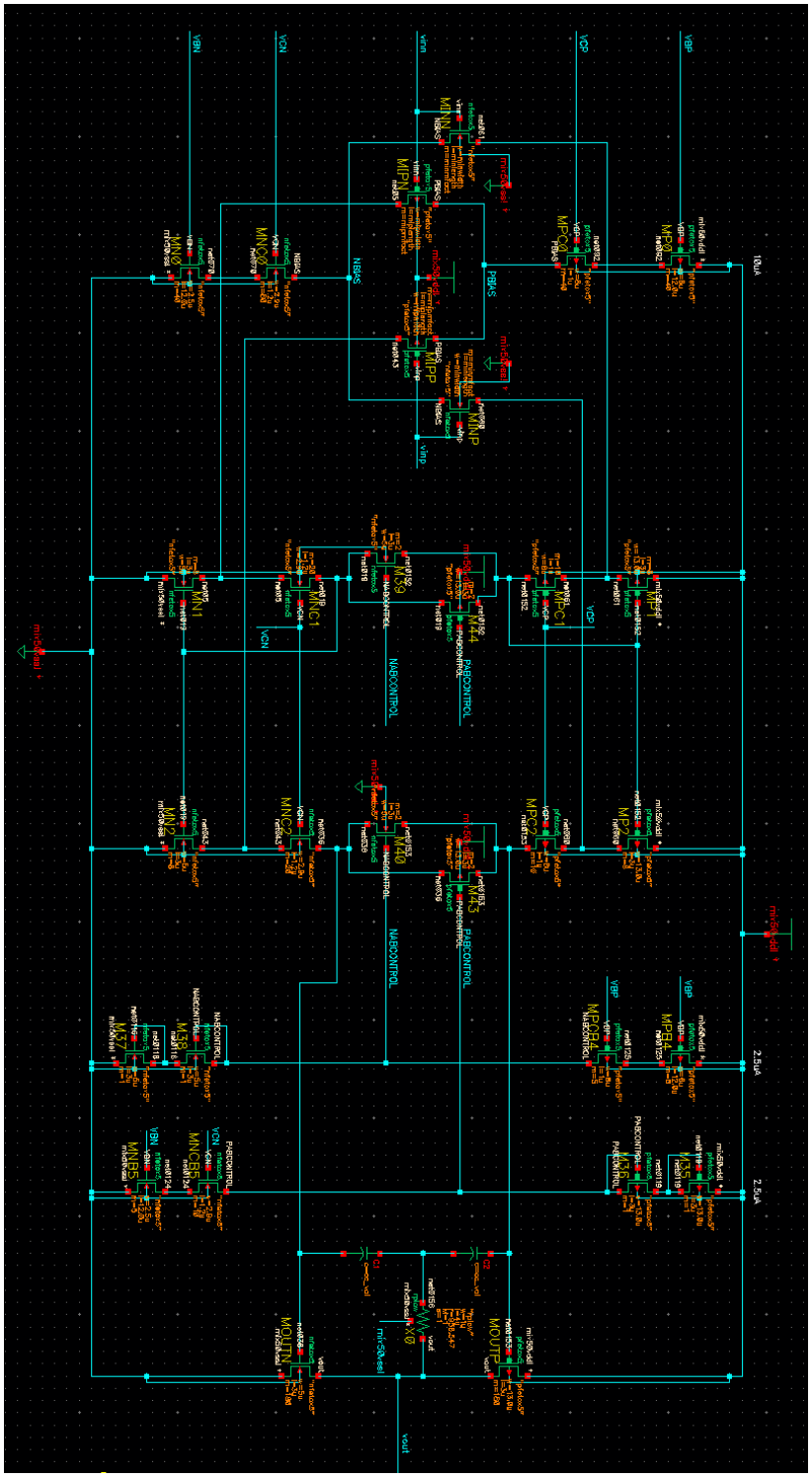

Figure 7.1: Schematics of the full amplifier, excluding the bias net and g_m control

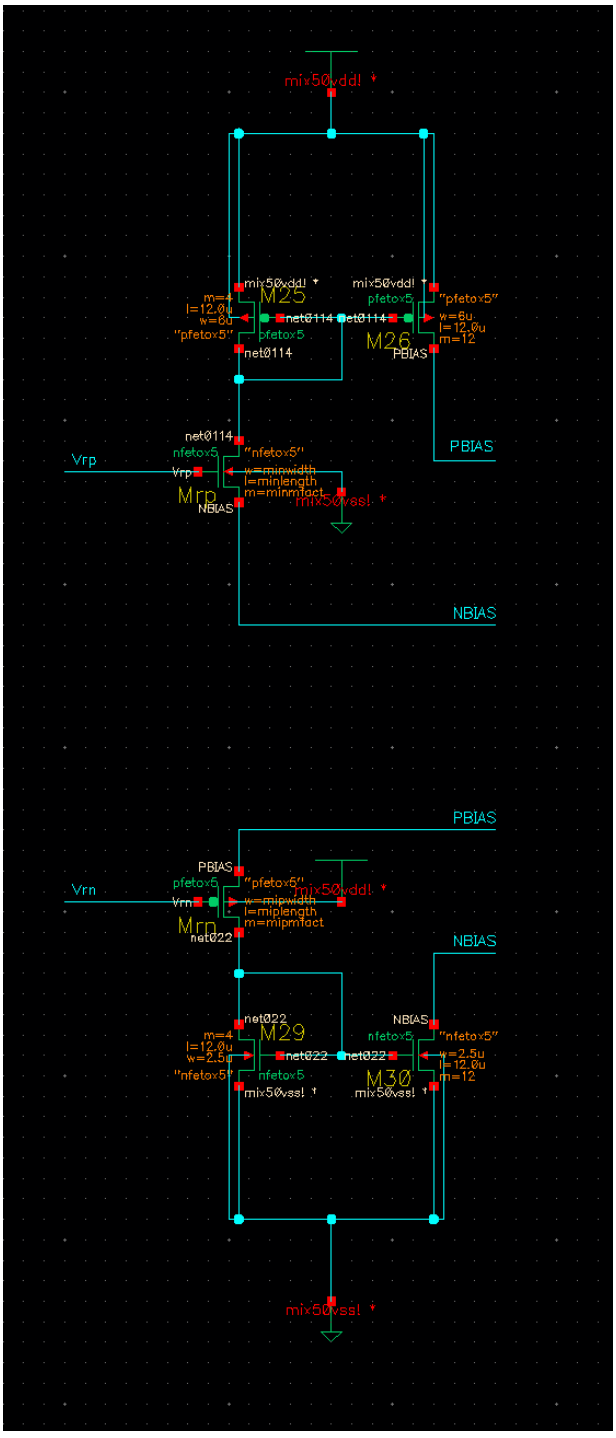

Figure 7.2: Schematics of the g_m control

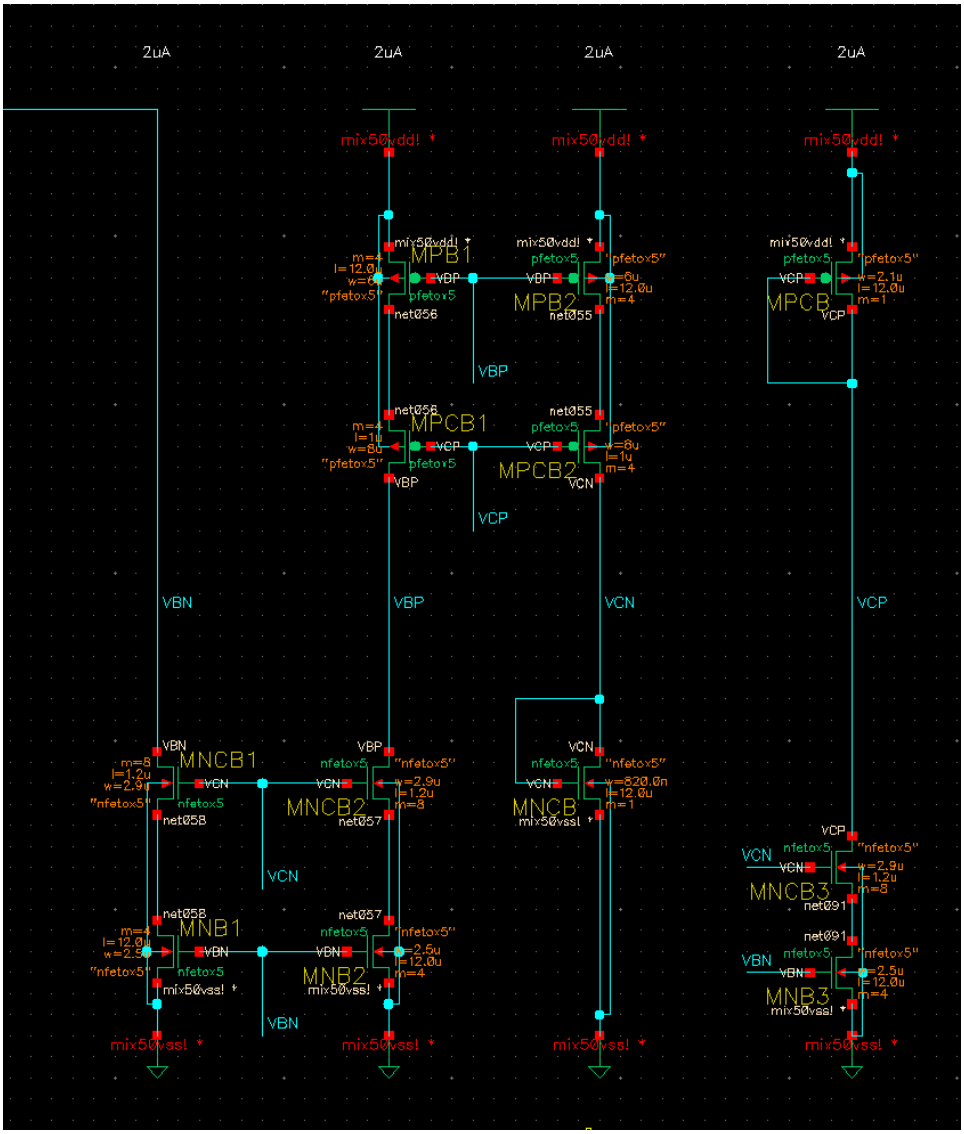

Figure 7.3: Schematics of the part of the bias net generating the VCN, VBN, VCP and VBP voltages

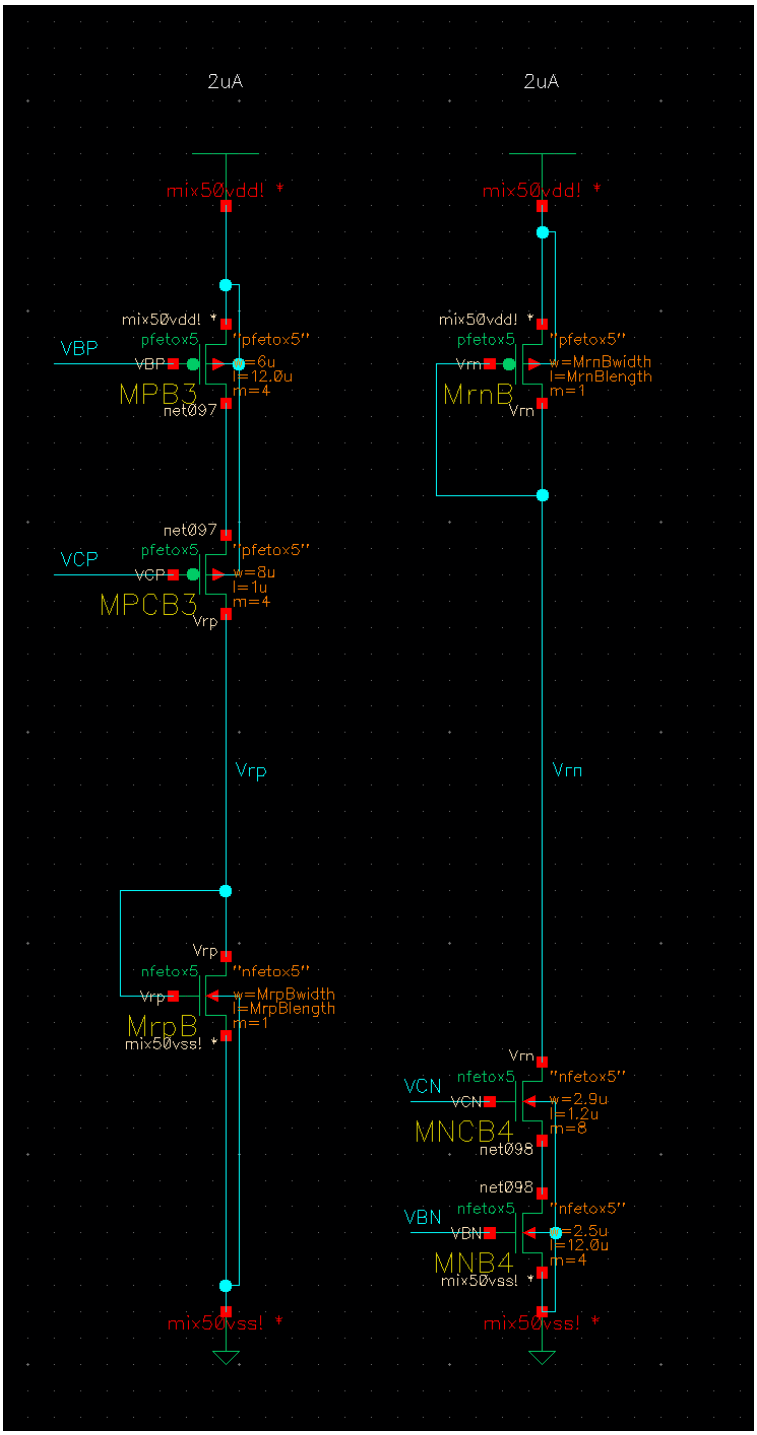

Figure 7.4: Schematics of the part of the bias net generating the Vrp and Vrn voltages

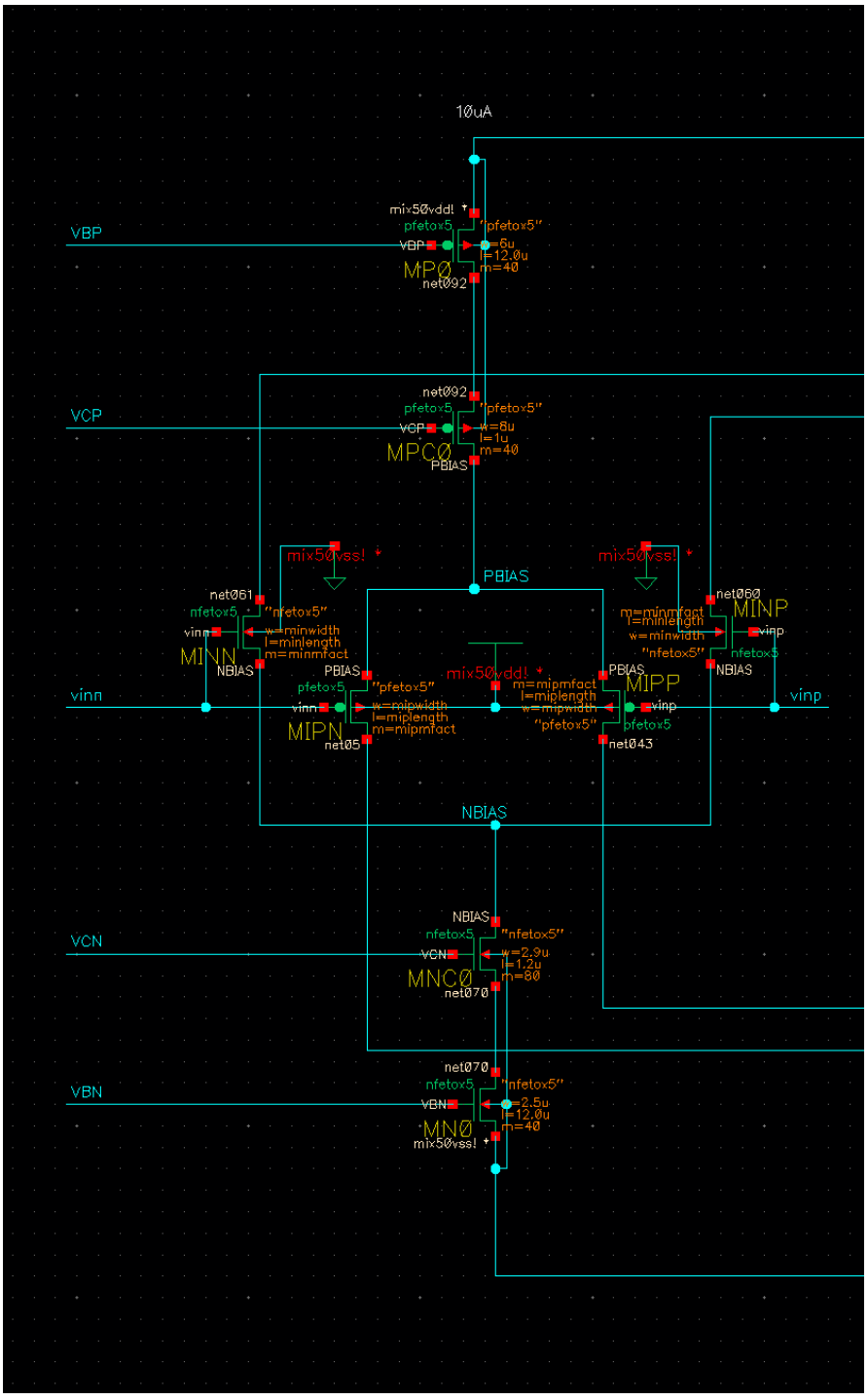

Figure 7.5: Schematics of the input pairs and their bias current generation

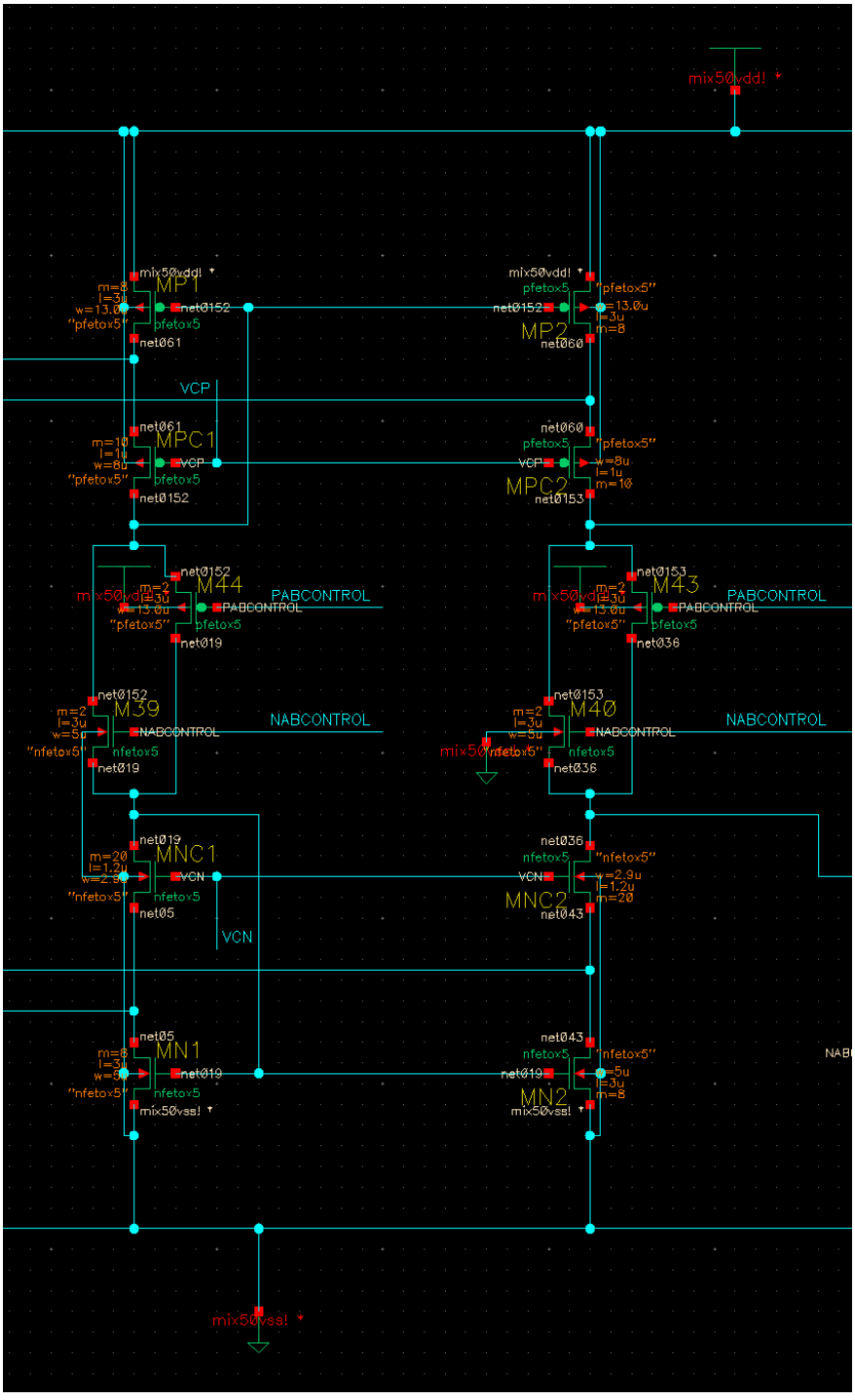

Figure 7.6: Schematics of the summing/cascode/AB control circuit

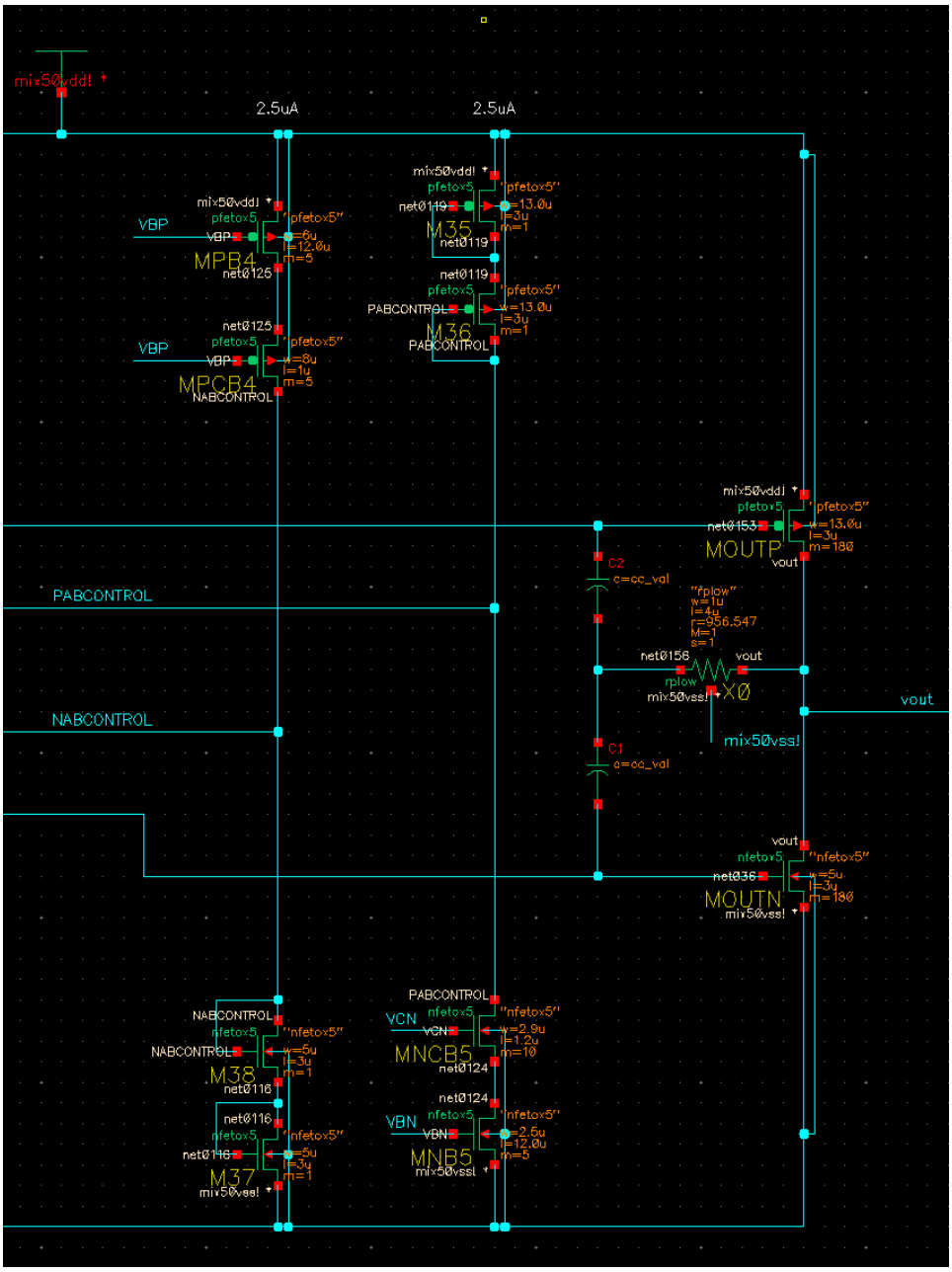

Figure 7.7: Schematics of the amplifier output

Appendix D: Simulation Results

This appendix contains large figures of the simulation results to improve the structure and readability of the thesis. To make the figures as readable as possible each figure is sized to cover a full page. Extensive simulation results from a 600+ corner AC simulation for gain, GBW and phase margin is included in the digital appendix folder in the form of an Excel spreadsheet named "gain_gbw_phasemargin_simulation_results.xlsx".

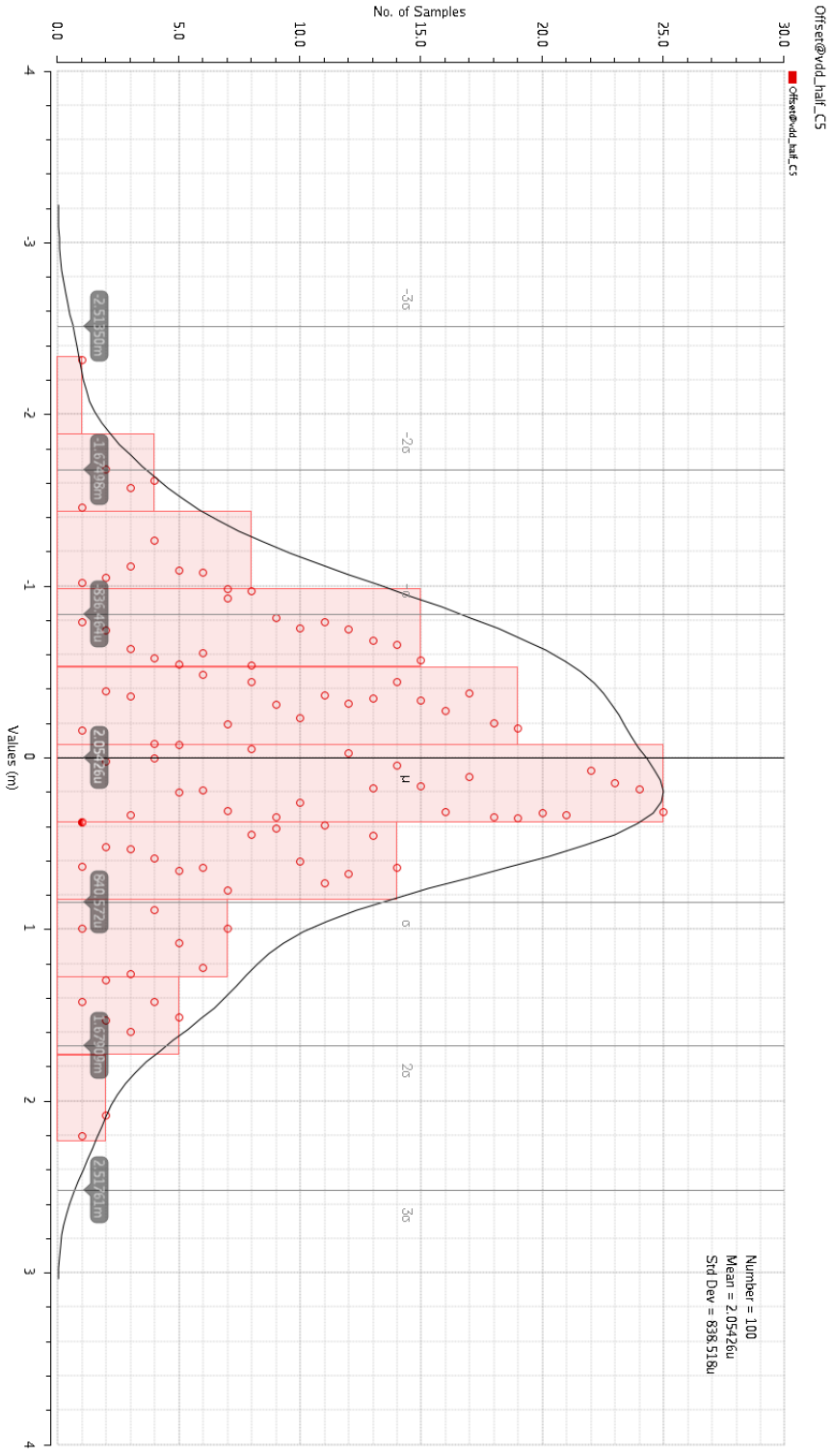

Figure 7.8: Histogram of simulated input offset

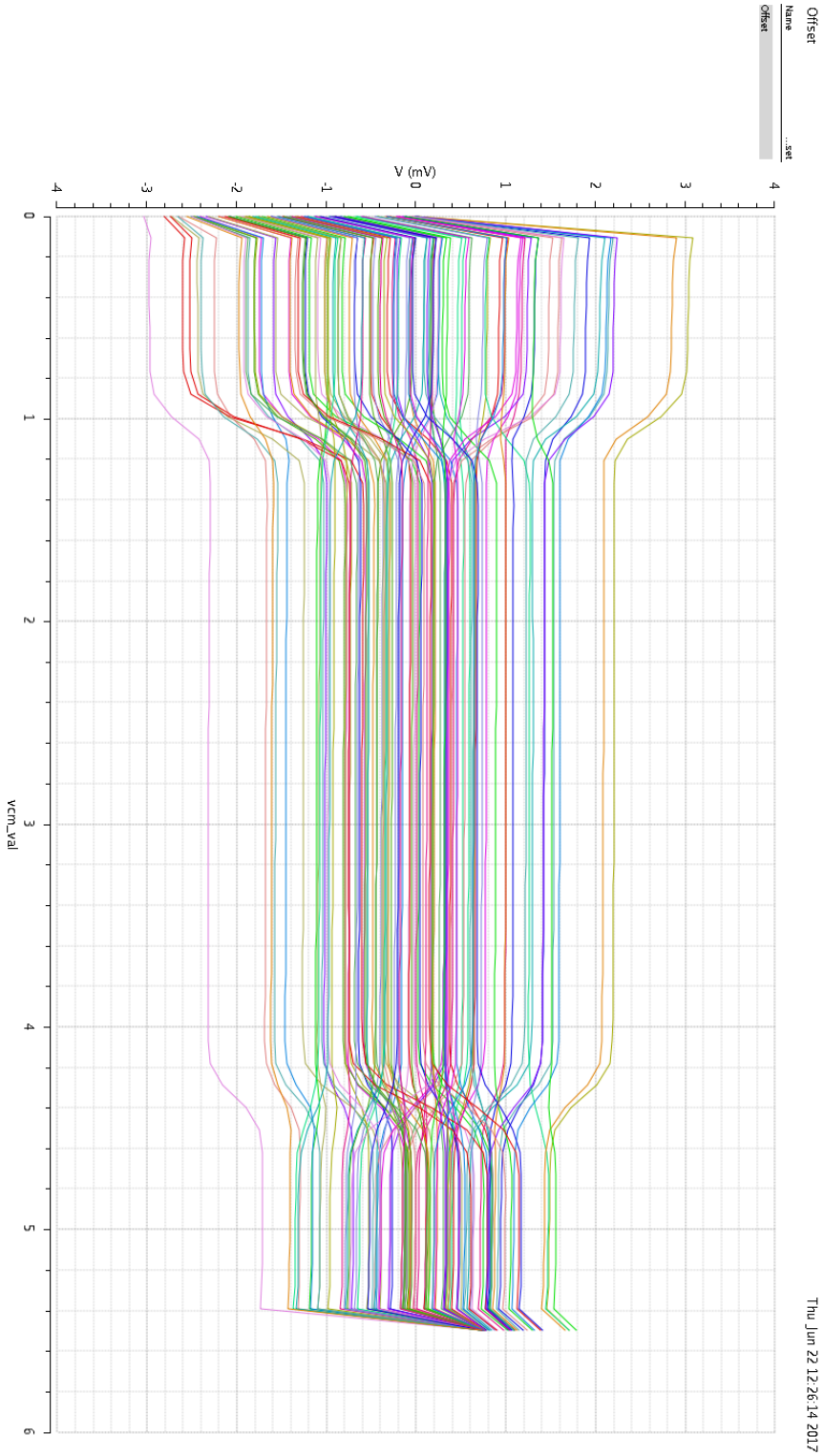

Figure 7.9: Plot showing simulated input offset

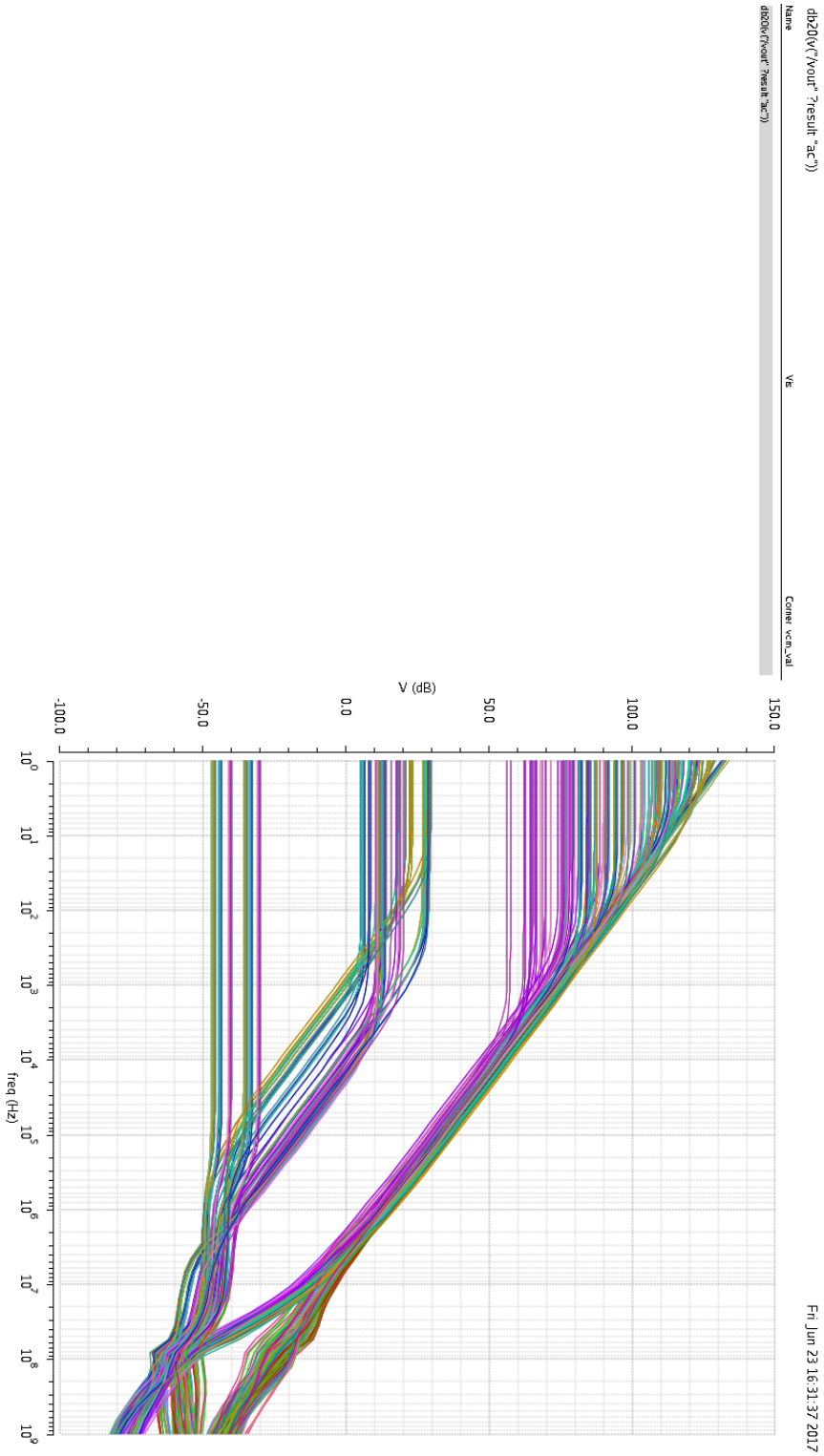

Figure 7.10: Plot of open-loop gain curves across all corners

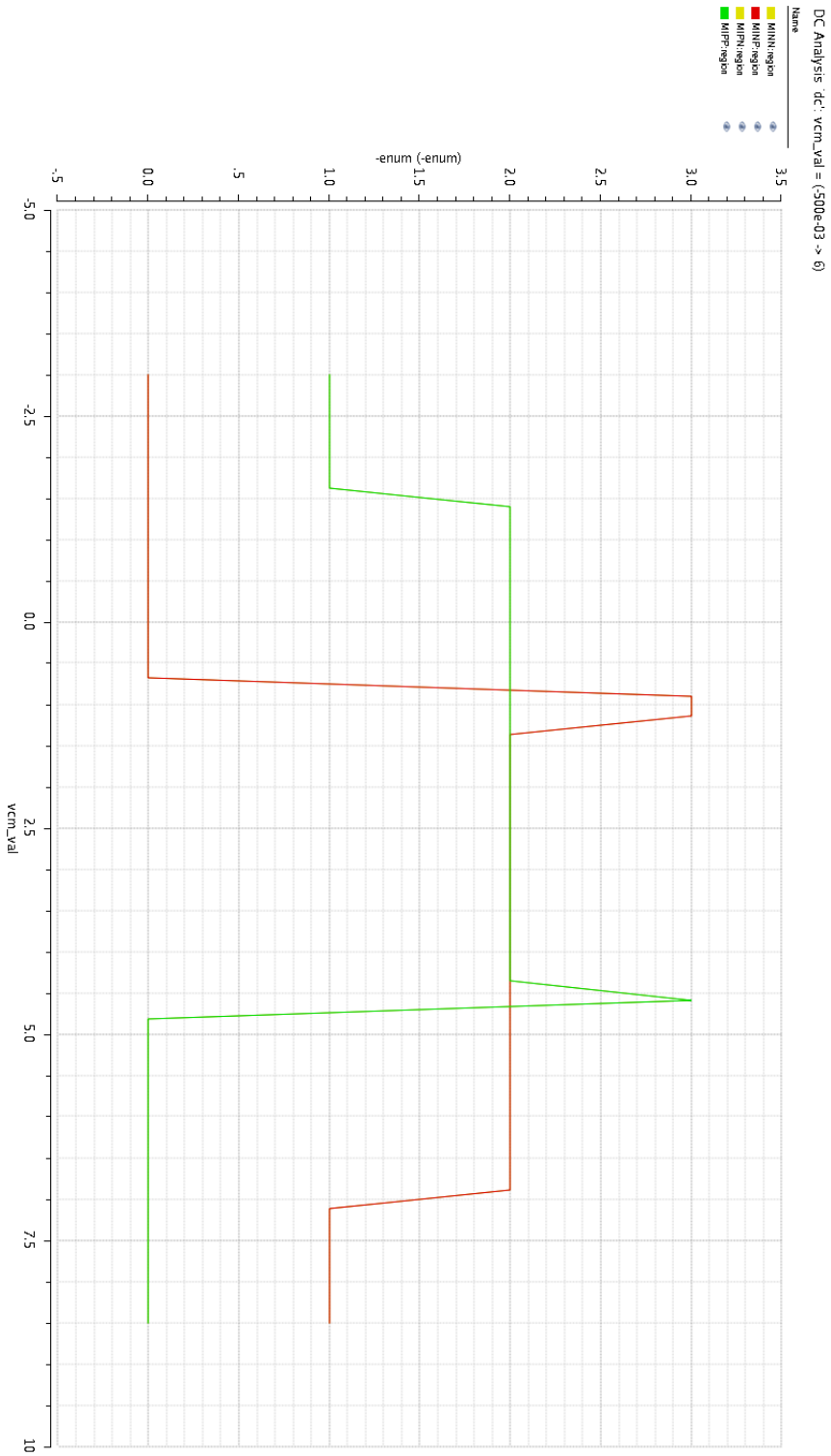

Figure 7.11: Plot showing input transistor pair operating region as a function of common-mode input voltage

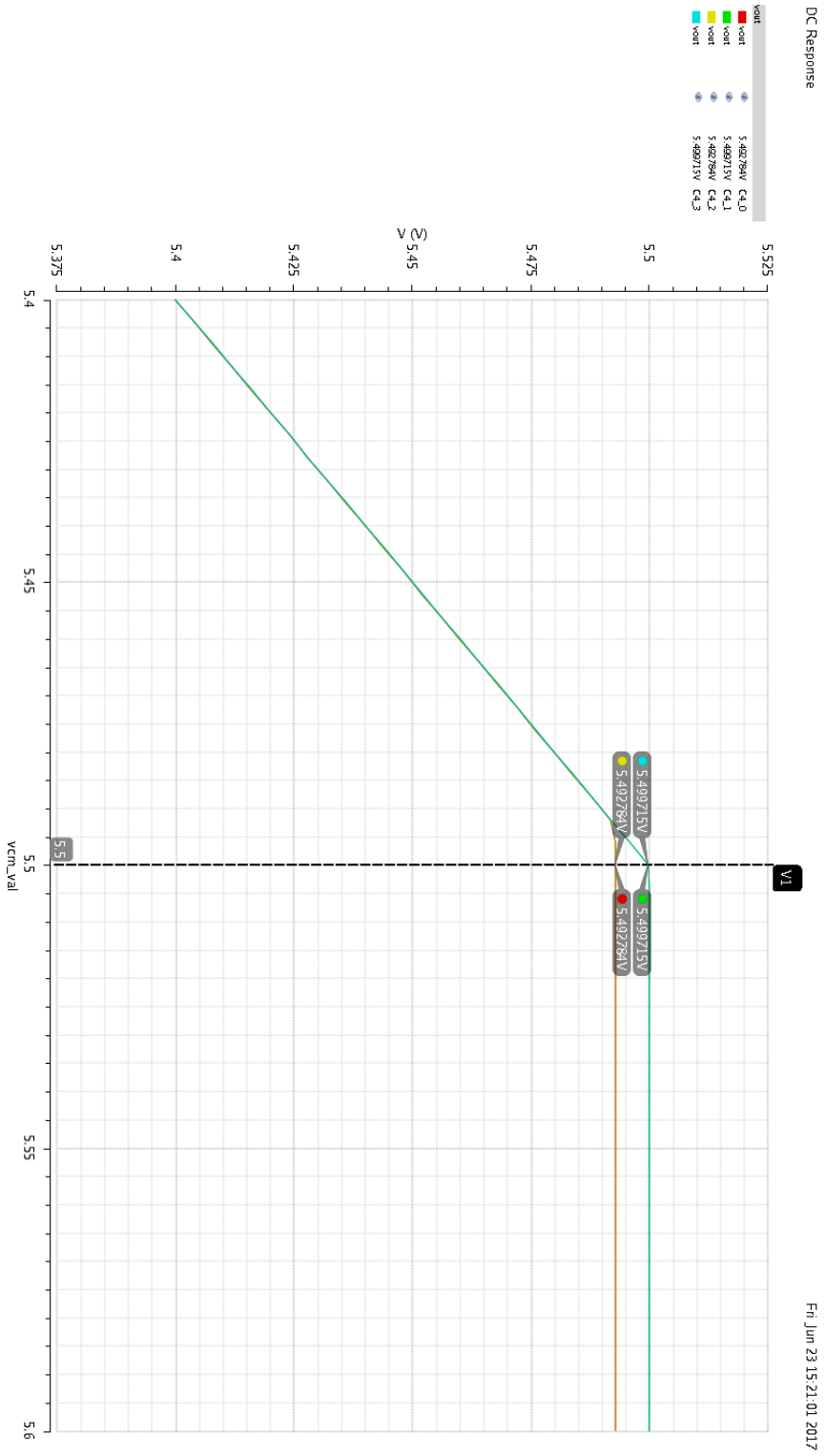

Figure 7.12: Plot of output voltage as a function of input common mode voltage near positive rail

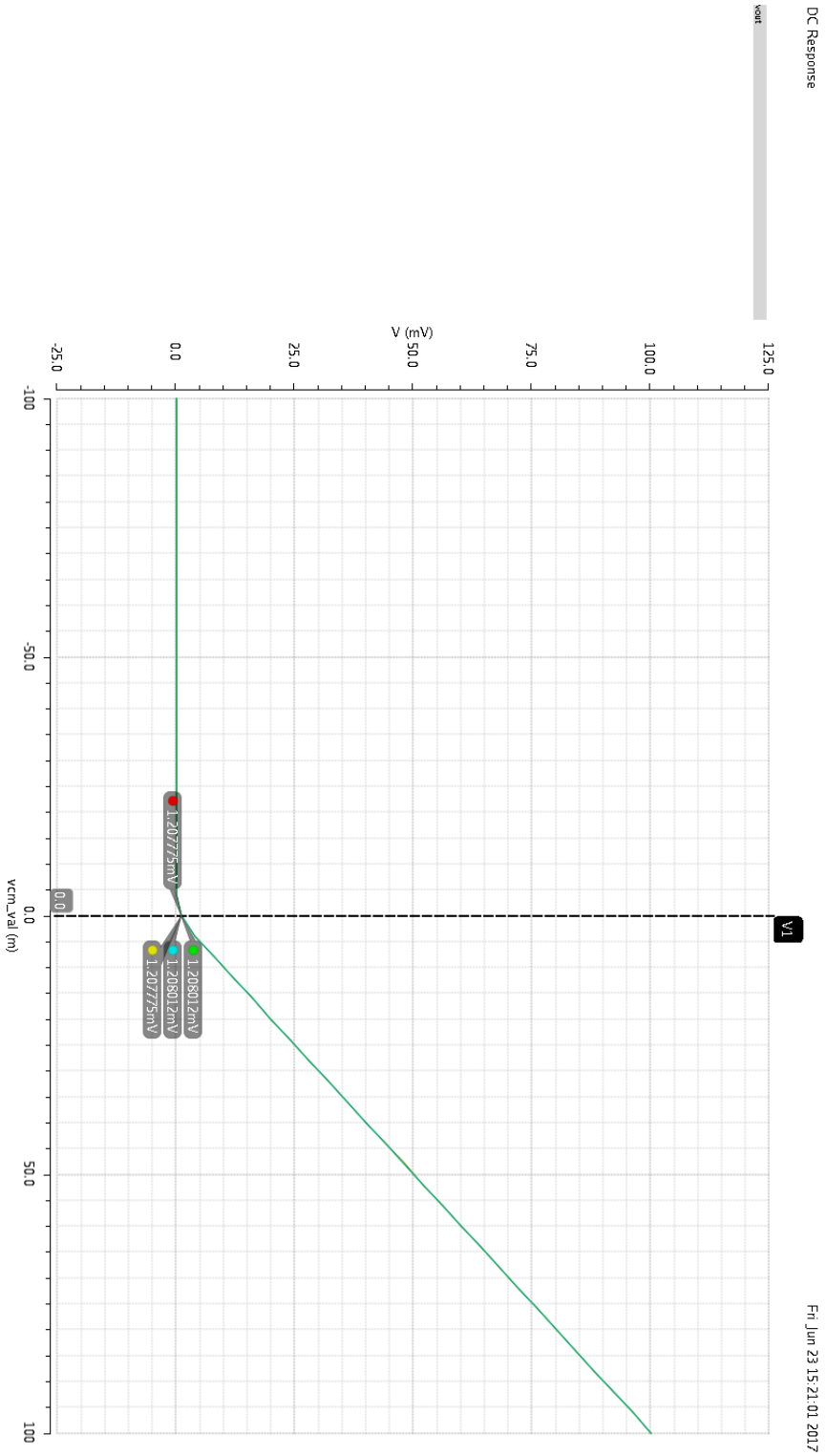

Figure 7.13: Plot of output voltage as a function of input common mode voltage near negative rail

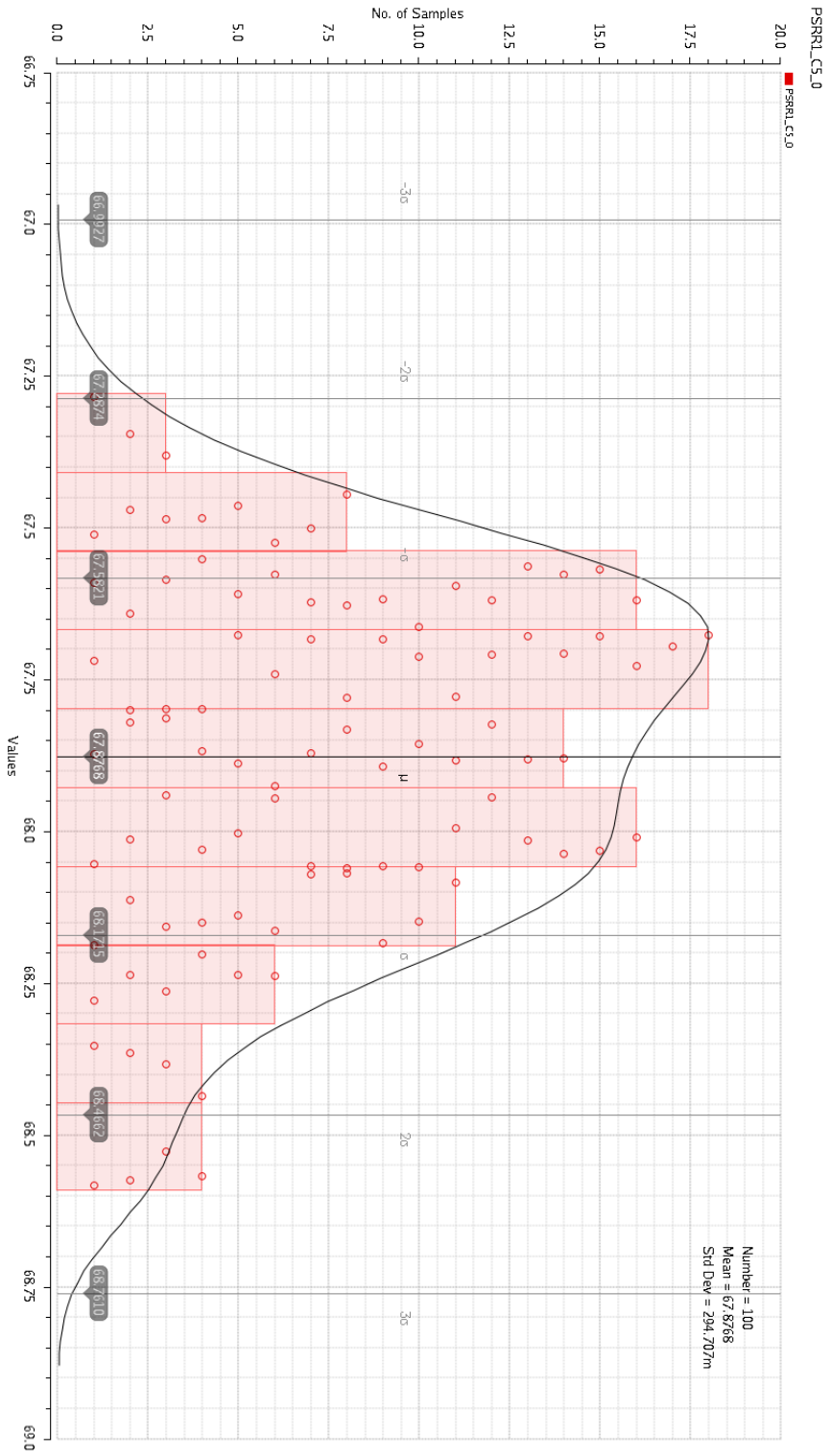

Figure 7.14: Histogram of PSRR at vcm = mix50vss! + 200mV

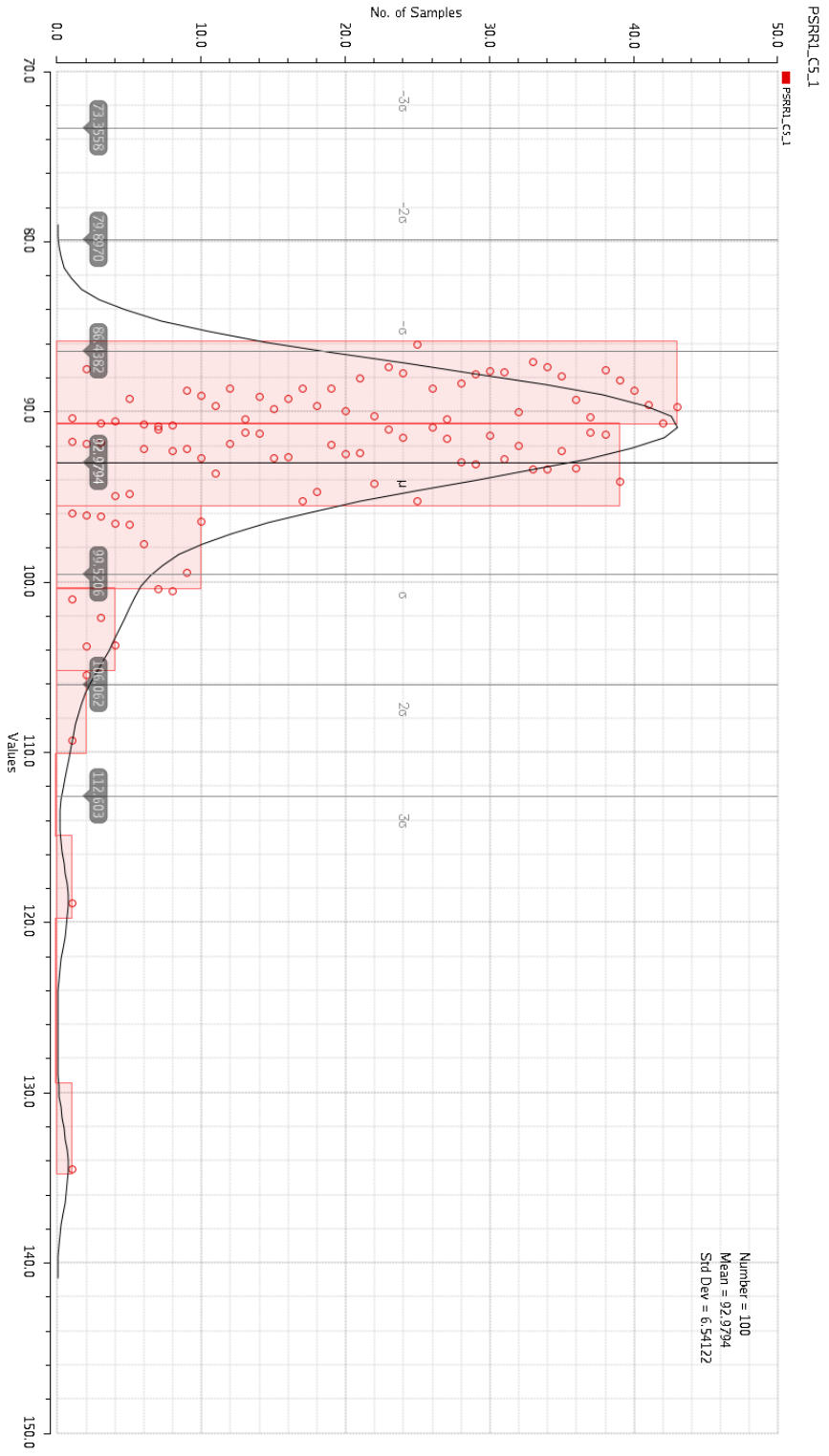

Figure 7.15: Histogram of PSRR at vcm = mix50vdd!/2

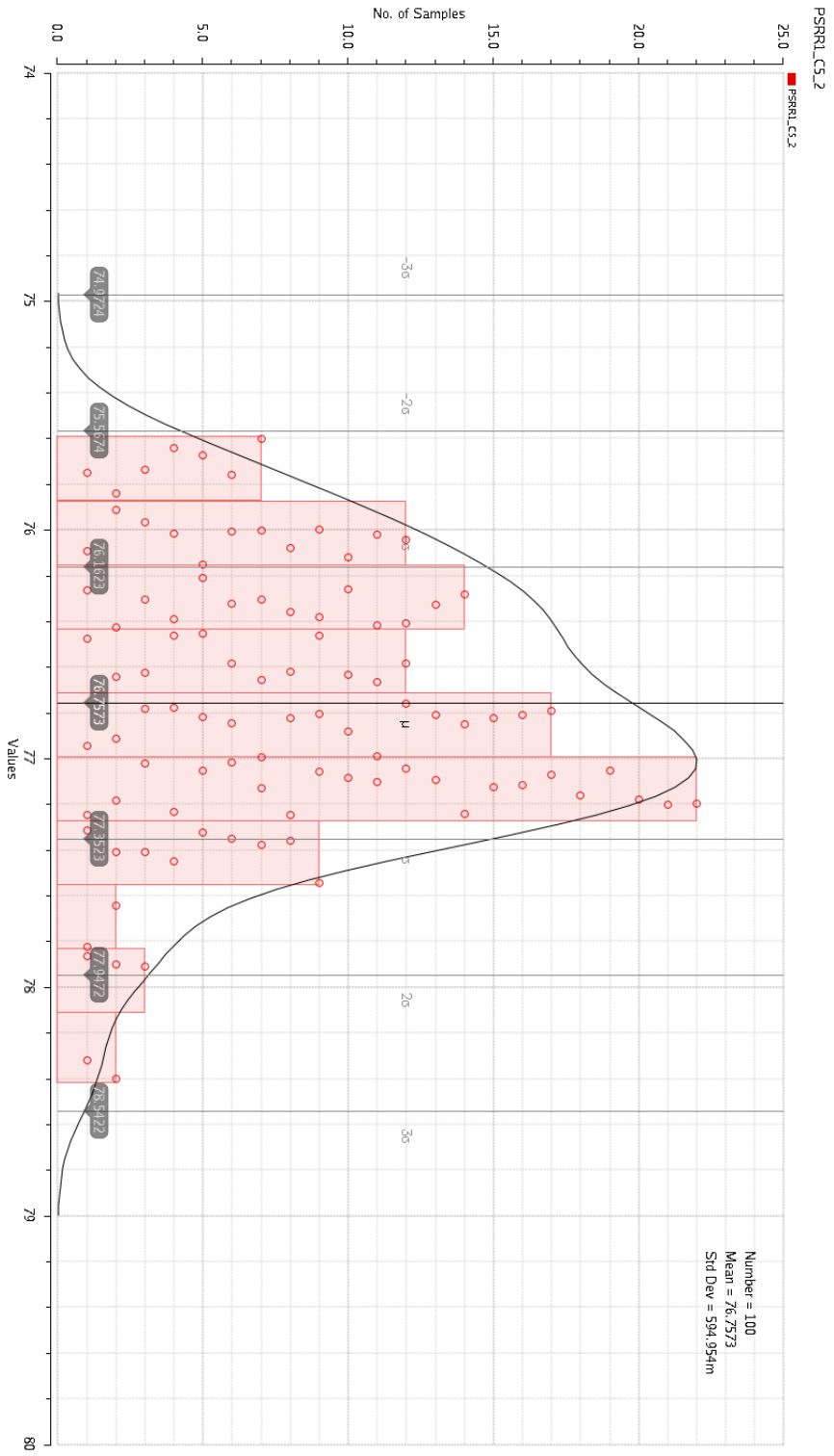

Figure 7.16: Histogram of PSRR at vcm = mix50vdd! - 200mV

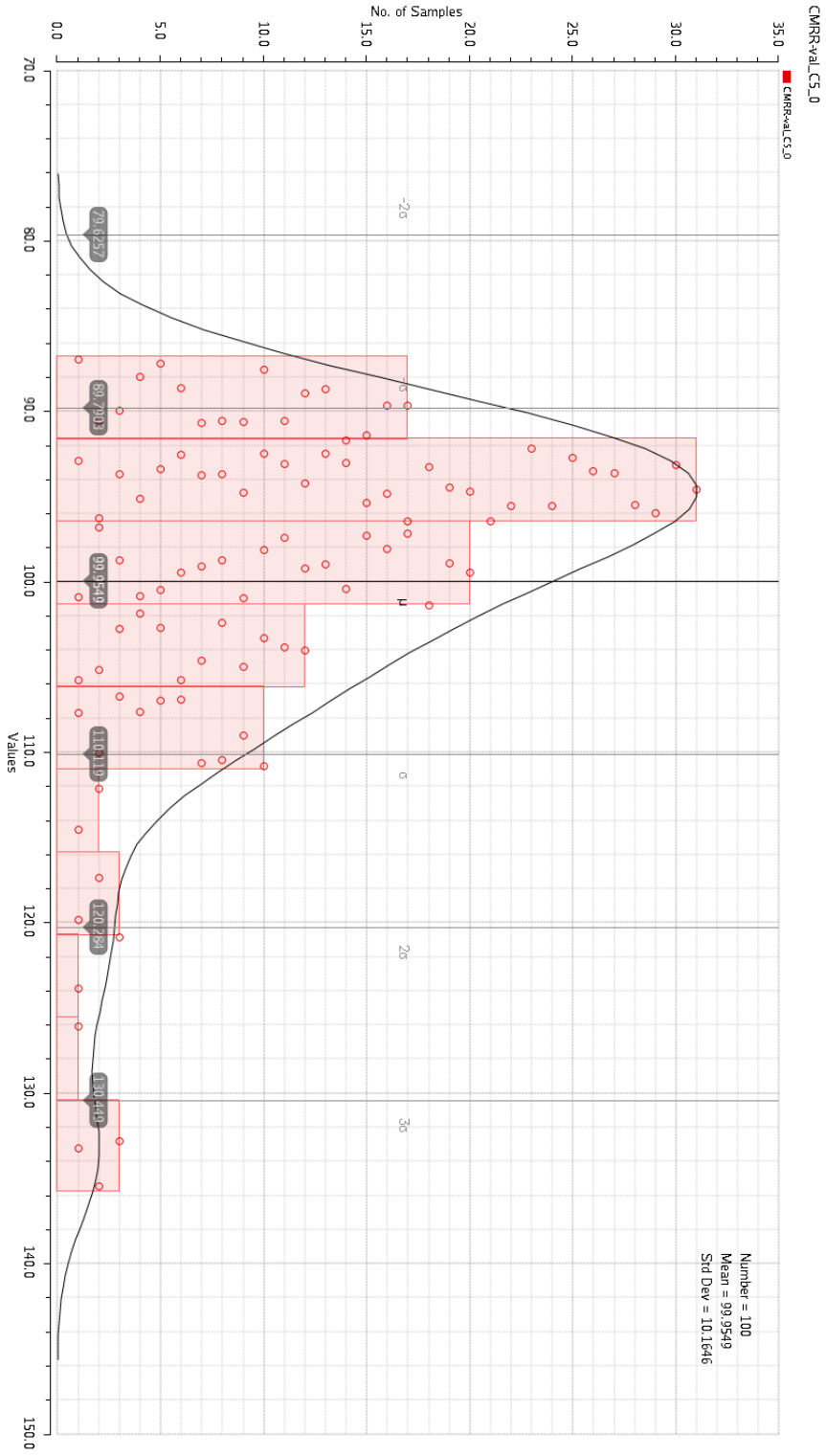

Figure 7.17: Histogram of CMRR at vcm = mix50vss! + 200mV

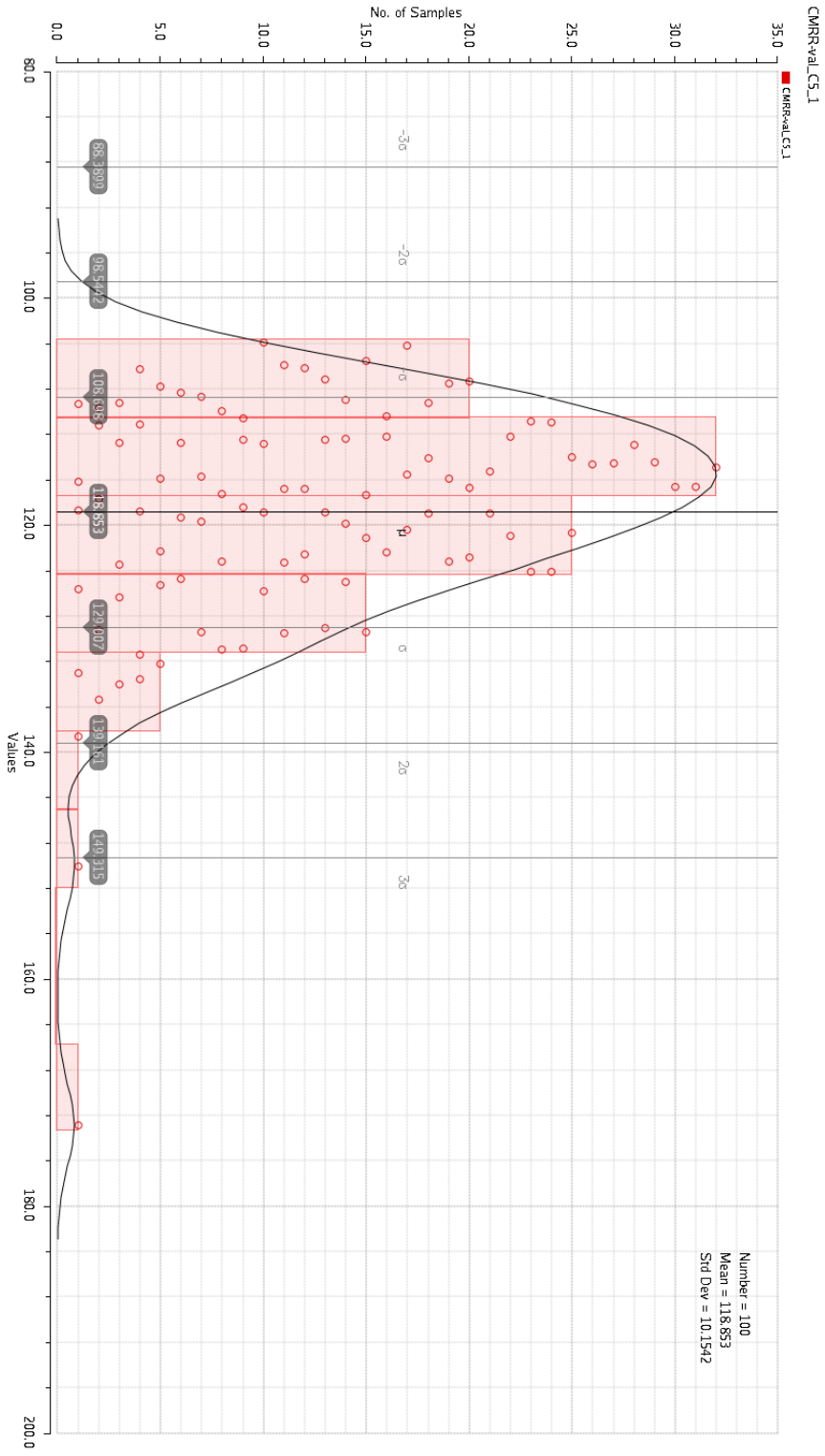

Figure 7.18: Histogram of CMRR at vcm = mix50vdd!/2

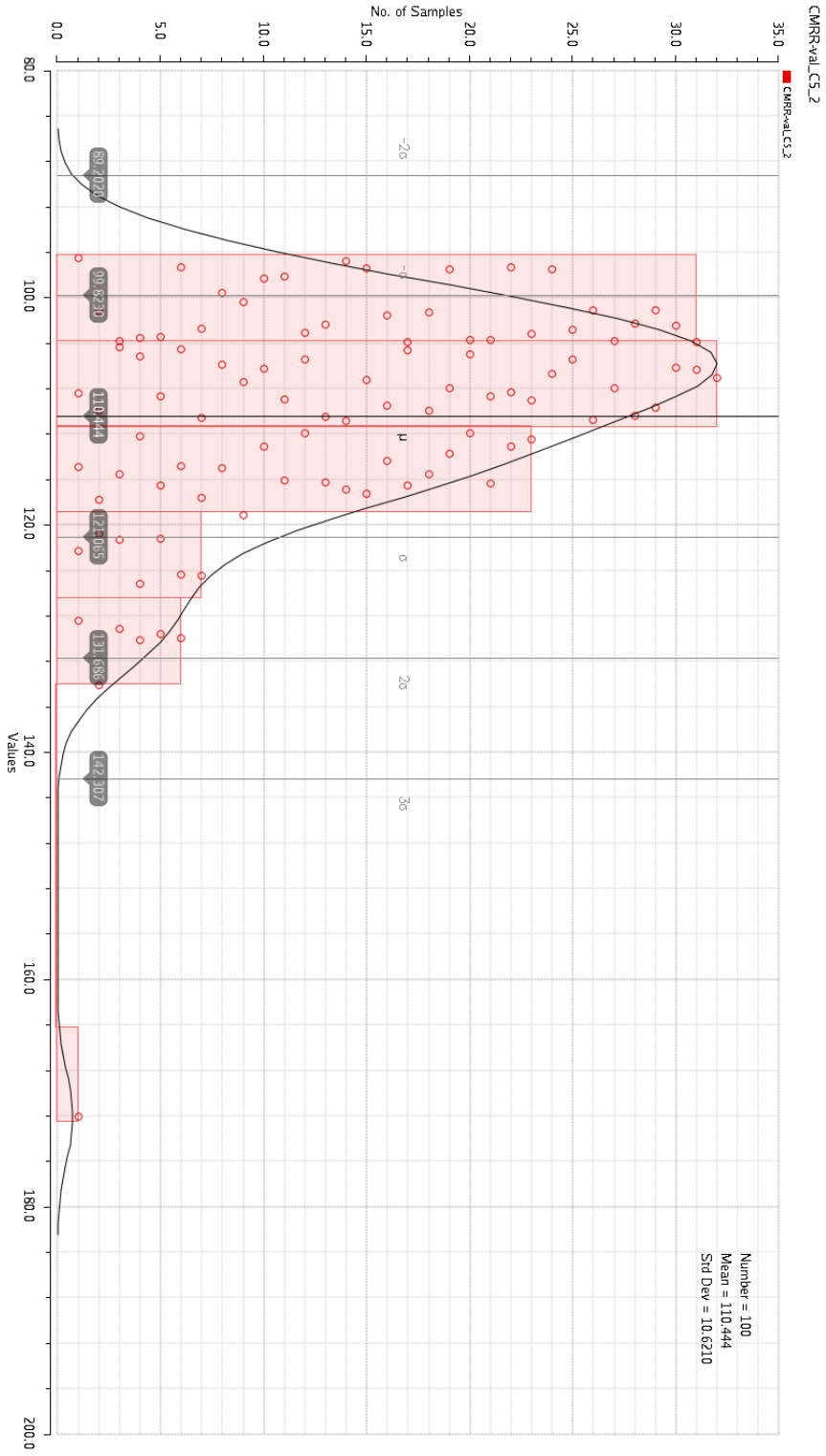

Figure 7.19: Histogram of PSRR at vcm = mix50vdd! - 200mV

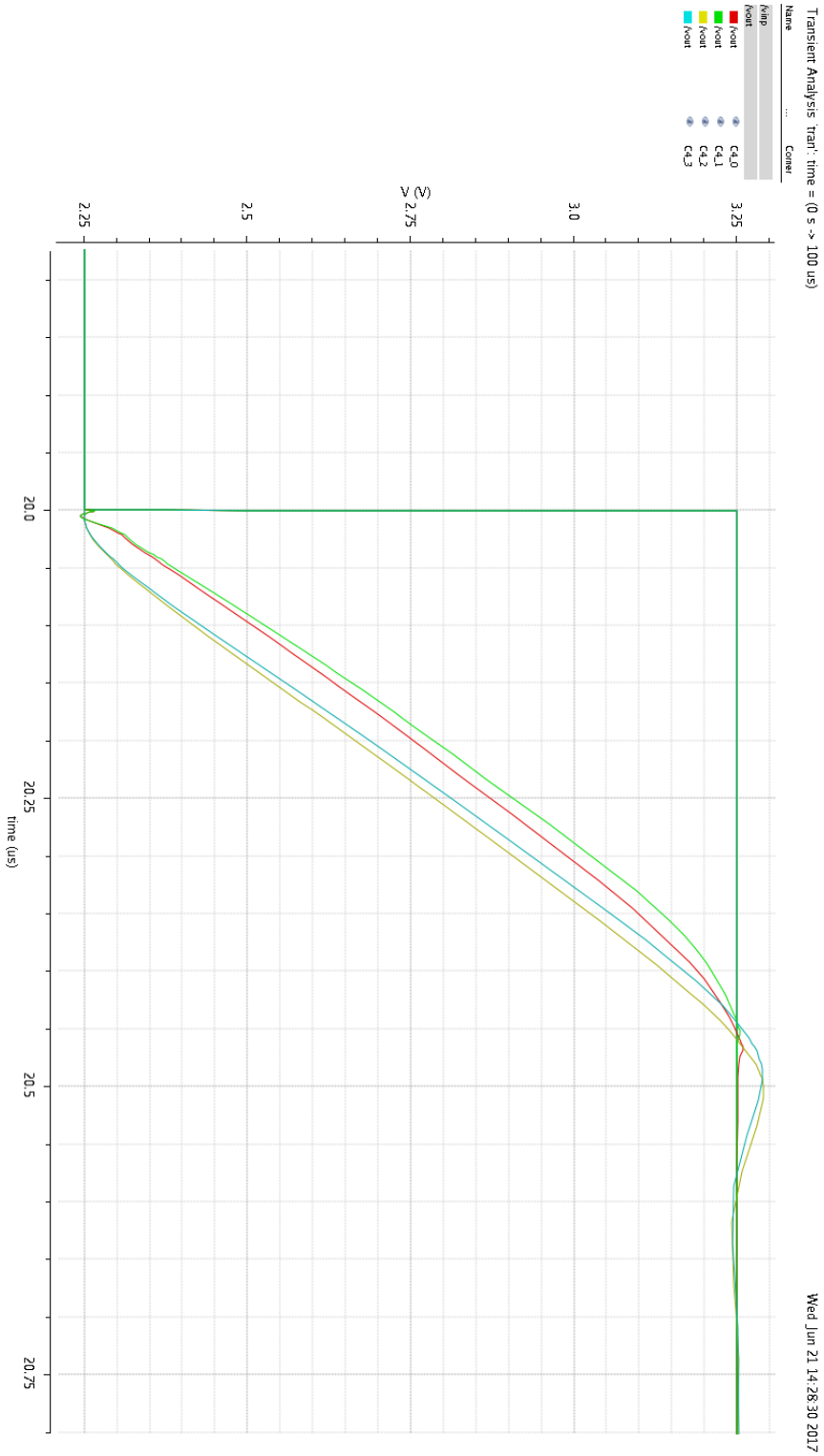

Figure 7.20: Input and output signals during slew rate simulation

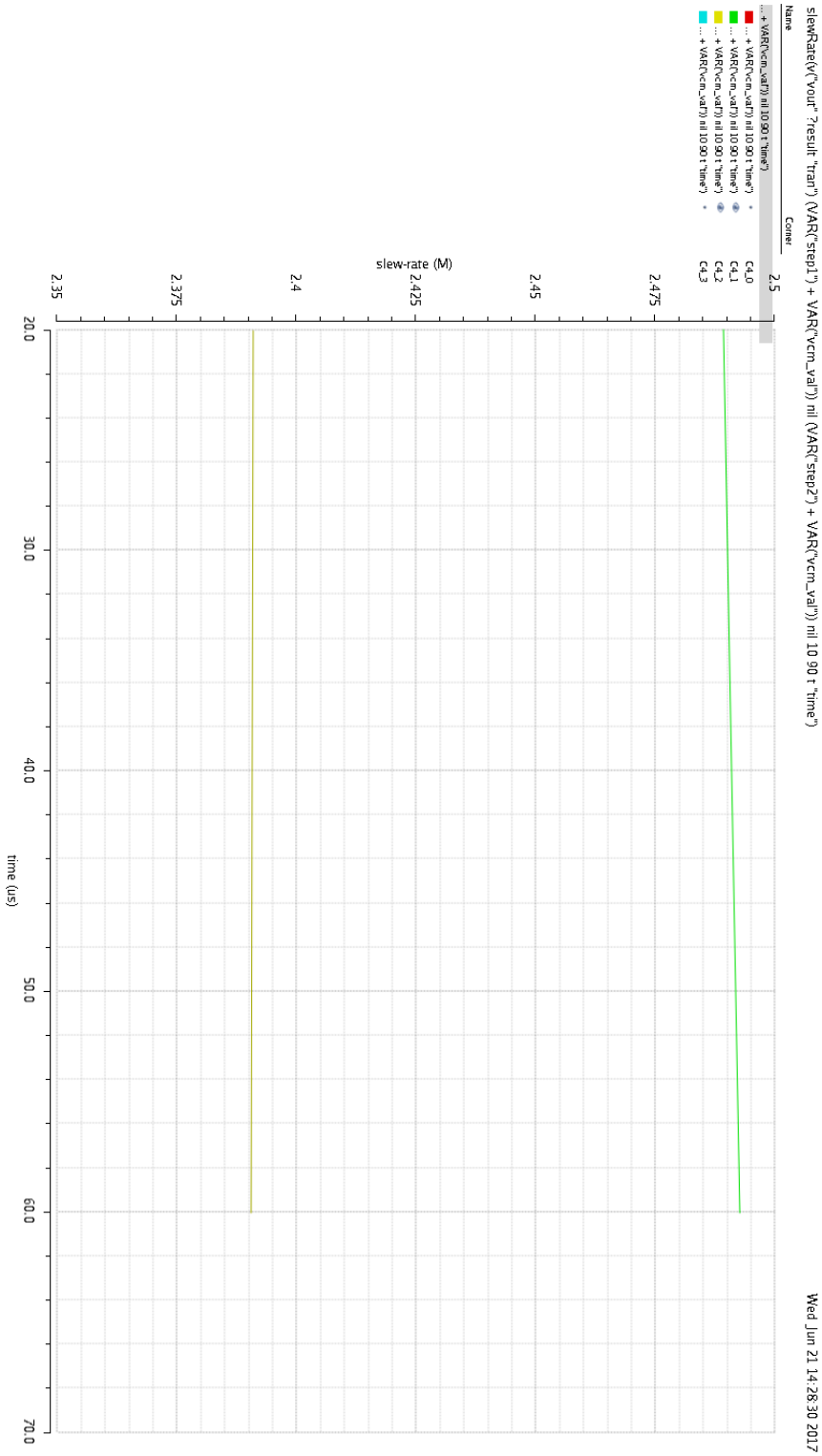

Figure 7.21: Calculated values for slew rate