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An Implantable Device for Electrical Nerve Stimulation

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Abstract

Background - Neural stimulation is currently subject to heavy research for the control of obesity using Vagus Nerve Stimulation (VNS). The available devices for such research is however developed for human use only, causing unnecessary complications when testing in smaller animals models due to the physical size of the device. A device for use in small animal models based on commercially available components would serve as a low-cost and more optimal solution to VNS research and similar disciplines.

Method - The design of an small electrical nerve stimulator was developed based on a comprehensive literature study combined with a detailed analysis of the requirements given by the end user. The system is described using a modular architecture with explicit interfaces, supporting easy verification and reproduction of the essential parts of the system.

Results - The result is a prototype design for an implantable electrical nerve stimulator with the ability to be miniaturized into 1/4 of the size of similar stimulating systems. The design meets the requirements from the end user, but must be miniaturized and encapsulated together with a connector for the electrode pin to be ready for implementation in animals.

Conclusion - This thesis describes a novel prototype design of an implantable stimulator with a primary use in VNS applications, compatible with the bipolar 304 leads from Cyberonics Inc. The stimulator is designed with commercially available components resulting in a low-cost and portable solution. A modular architecture describes the system with respect to specifications given by end user and limitations from a literature study.

Sammendrag

Bakgrunn - Nevral stimulering er under intens forskning for å avdekke om Vagus Nerve Stimulering (VNS) kan brukes til behandling av overvekt. De tilgjengelige stimulatorene som brukes i slik forskning er imidlertid utviklet for bruk på mennesker, noe som fører til unødvendige komplikasjoner for bruk i små forsøksdyr som følge av den fysiske størrelsen på stimulatoren. En stimulator som kan brukes på små forsøksdyr og som har et design basert på lett tilgjengelige komponenter vil fremstå som en rimelig og god løsning for forskning på VNS og tilsvarende disipliner.

Metode - Designet av en elektrisk nervestimulator for bruk i små forsøksdyr var utviklet basert på en omfattende litteraturstudie, kombinert med en analyse av en kravspesifikasjon gitt av sluttbruker. Systemet er beskrevet ved en modulær arkitektur med eksplisitte grensesnitt for enkel verifikasjon og reproduksjon av essensielle deler i systemet.

Resultater - Resultatet er et prototype design for en implementerbar elektrisk nervestimulator som kan utvikles til et ferdig produkt der størrelsen er redusert til 1/4 sammenlignet med tilsvarende systemer. Kretsdesignet møter kravene til sluttbruker, men forutsetter at det blir redusert i størrelse og innkapslet med tilkobling for elektrodene til å være klar for implementering i dyr.

Konklusjon - Oppgaven beskriver et enkelt prototype design for en implementerbar nervestimulator, hovedsakelig for bruk i VNS applikasjoner og er kompatibel med de bipolare 304 elektrodene fra Cyberonics Inc. Stimulatoren er designet ved bruk av kommersielt tilgjengelige komponenter for et rimelig og portabelt design. Systemet er beskrevet ved en modulær arkitektur som samsvarer med spesifikasjonene gitt av sluttbruker og begrensninger fra et litteraturstudie.

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I'm grateful for the guidance given by Luke Theogarajan for his permission to let me study the field of neuromodulation in more detail at UCSB, which has been an important contribution in understanding the fundamentals..

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A thanks to my office buddy Max Heger for sharing the same mental state during the longest day.

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Abbreviations

ADC: Analog to Digital Converter

AP: Action Potential

AIROF: Activated Iridium Oxide Film

BJT: Bipolar Junction Transistor

BLD: Battery Low Detect

BOM: Bill Of Materials

CAP: Compound Action Potential

CE: Counter Electrode

CCS: Current Controlled System

CIC: Charge Injection Capacity

CPU: Central Processing Unit

CU: Control Unit

CV: Cyclic Voltammetry

DAC: Digital to Analog Converter

DC: Direct Current or Duty Cycle depending on context

DDC: Device Duty Cycle

ECF: ExtraCellular Fluid

EDL: Electrical Double Layer

EOS: End Of Service

ETI: Electrode-Tissue Interface

GSA: Geometric Surface Area

HDI: Human Device Interface

ICF: Intracellular Fluid

IPD: Interphasic delay

m102: The model number of the Cyberonics stimulator

MCU: Micro Controller Unit

MSO: Microstimulating Output

MUX: Multiplexer

n/pMOS: n-type and p-type MOSFET transistor

op-amp: operational amplifier

PCB: Printed Circuit Board

PU: Power Unit

PWM: Pulse Width Modulation

mQFN: Mini Quad Flat No-leads

RC: Resistor-Capacitor

RE: Reference Electrode

RSA: Real Surface Area

SFE: Stimulating Front End

SFE-A: Stimulating Front End - Anodic

SFE-C: Stimulating Front End - Cathodic

SFE-TC: Stimulating Front End - Timing and Control

SIROF: Sputtered IRidium Oxide Film

SOT: Small Outline Transistor

SPDT: Singe Pole Double Throw

SPICE: Simulation Program with Integrated Circuit Emphasis

SPST: Singe Pole Single Throw

UPAP: Unidirectionally Propagating Action Potential

VCS: Voltage Controlled System

VNS: Vagus Nerve Stimulation

WE: Working Electrode

Chapter 1

Introduction

Electrical stimulation of neural tissue is termed neuromodulation by the International Neuromodulation Society (INS) and covers a broad range of medical conditions. Stimulating body parts with electricity has been reported to be practised already in the ancient Egypt with the use of electric eels. The first reported study on bioelectricity was conducted by Luigi Galvani in 1780, when he discovered that muscles of dead frogs twitched when struck by a spark.

The true science of neuromodulation emerged in the aftermath of the work by Hodgkin and Huxley in the early 50's. Their work of mapping the electric properties of the neural membrane to an electric model known has the Hodkin-Huxley model was awarded with the Nobel price in 1963. The model was the "missing link" for the development of neural prostetichs and other disciplines based on electrical excitation of neural tissue.

Today, many people benefit from neural prostetichs such as cochlear and retinal implants. A small selection of the most common applications is given below:

Brain, Spinal Cord and Peripheral Nerve Therapies: Deep Brain Stimulation (DBS) for Parkinson's suppression, Motor Cortex Stimulation for stroke rehabilitation, Pudendal Nerve Stimulation to relieve urinary incontinence, and Vagus Nerve Stimulation (VNS) to control epilepsy and depression.

Functional Electrical Stimulation: Retinal Stimulation, Cochlear Implants, and various applications to restore limb functionality, e.g drop foot neuroprosthetics for gait abnormality.

Pharmacological: Intrathecal, Intraspinal and Intracisternal Drug Delivery to modulate neurons using analgesic agents that suppress pain and spasticity.

Neuromodulation is a highly relevant and important subject to research in today's society. Research in the discipline may solve medical conditions linked to the neural system which do not have any known solution today.

1.1 Problem

VNS is currently subject to heavy research for the control of obesity. The vagus nerve is mainly conveying sensory information from the body's organs to the central nervous system, and it is hypothesised that stimulation of this nerve may suppress the sensation of hunger. The problem is that available devices for VNS research is developed for human use only. This causes unnecessary complications when testing in small animal models due to the physical size of the devices, which can result in biased data due to post-operational stress.

1.2 Motivation

The motivation for this thesis was to design a functional circuit, suitable for use in small animal models, that later can be developed into an implantable device used by researchers with ease. The circuit design was completed with commercially available components, resulting in a low cost and fast start-up solution for emerging researchers in VNS or similar disciplines.

1.3 Outline

The approach to the problem followed the principle of the V-model, shown in Figure 1.1 and gives the high-level outline for this thesis:

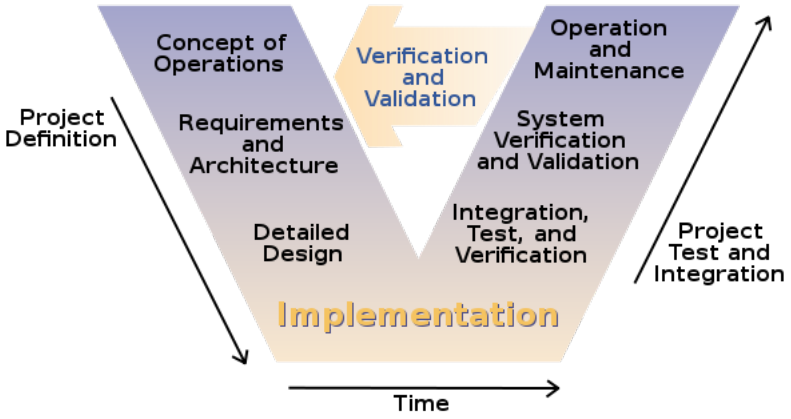

FIGURE 1.1: The v-model as the project outline, from [1].

Electrical excitation of neural tissue: Chapter 2: Theory with identification of major challenges in electrical excitation of neural tissue. Requirements for design of a neural stimulator. (Concept of Operations)

System requirements analysis: Chapter 3: Detailed requirements analysis. Modular architecture with explicit interfaces. Traceable architecture model. (Requirements and Architecture)

System design and implementation: Chapter 4: Detailed system design and implementation. HW/SW and mechanical design. (Detailed Design)

Discussion: Chapter 7: Assessment of system compliance. (Integration, Test, and Verification). The rest of the V-model is not applicable as the design was limited to a prototype.

The functional requirements for the device was given by researchers at the Department of Cancer Research and Molecular Medicine, NTNU, which currently conduct studies on the control of obesity using Vagus Nerve Stimulation using laboratory rats.

Chapter 2

Electrical excitation of neural tissue

The aim for this chapter is to identify the concepts in the transition from electrons in the conducting surface of the electrode to the biological electrolyte in the tissue. These concepts may identify the major challenges of electrical excitation of neural tissue, and serve as a theoretical basis and limitation for the requirements analysis and design in Chapter 3 and 4.

The information presented is based upon a large selection of acknowledged sources in the field, and is systematized specifically for peripheral nerve stimulation. A comprehensive review on the physical basis for electrical stimulation by Merill et al. [2] has later been found to cover most of the important aspects, and will therefore be referred to throughout the chapter.

2.1 Neural physiology

A brief introduction to neural physiology is given based on the last year's term project (Moen 2013, [3]).

2.1.1 The neuron

The basic function of the nervous system is to provide a way of fast communication between cells or body parts. The nervous system can be classified into the central nervous system (CNS) and the peripheral nervous system (PNS). The CNS consists mostly of interneural communication and is found in the brain and spinal cord, while the PNS consists mainly of signal conduction from (afferent) and to (efferent) extremities and organs.

The cell structure of neurons shares the same basal anatomy as other cells. It has a cell membrane, a nucleus with genes, organelles, protein synthesis and energy production. The neuron distinguishes from other cells by having dendrites for incoming signals, an axon for sending outgoing signals, and an axon terminal which relays the signal into the next neuron(s), depicted in Figure 2.1.

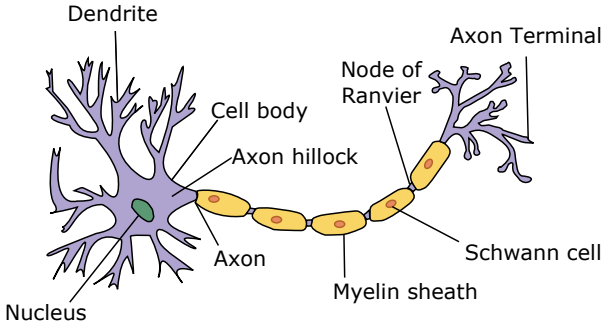

FIGURE 2.1: Basic Anatomy of the Neuron. The dendrites process incoming signals which are summed in the axon hilloc. The summation includes inhibitory and excitatory signals, where an equal amount of both would result in a neutral response. If the incoming signals meets threshold due to a majority of excitatory signals, an action potential is generated and propagated via the axon to the axon terminal. Figure taken from from [3].

When several neurons project their axons along a common path, they tend to group together to what is commonly known as a nerve. The nerve has several

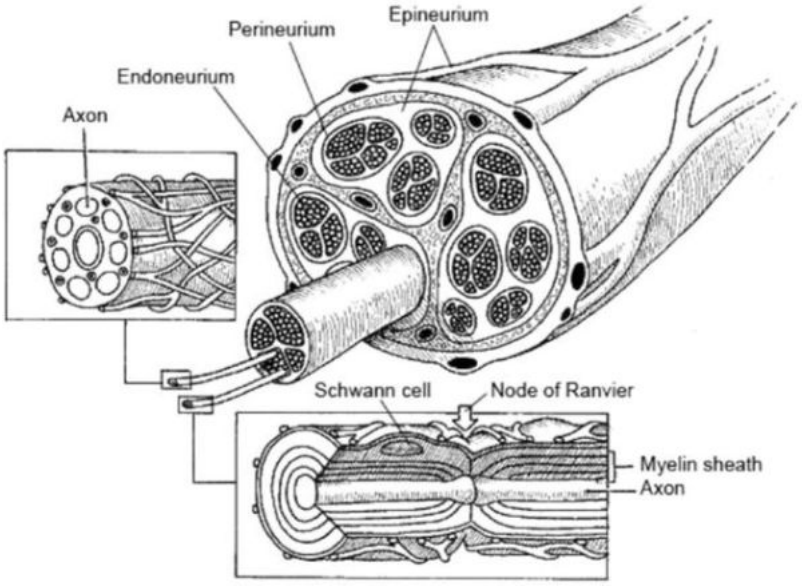

FIGURE 2.2: Basic Anatomy of the Nerve, from [3]

layers of connection tissue that insulates and provides mechanical strength to the axons, shown in Figure 2.2.

2.1.2 The action potential

The action potential is the process where the neuron generates a neural signal. The name originates from the action of changing and conducting a potential by utilizing the electrical properties of ions over a selectively permeable membrane.

The neural cell can be considered to have two states: non-excited state (at rest) and an excited state (the action potential). The mechanics behind the resting membrane is discussed first, as this gives the basis for the action potential.

The resting membrane

The neural membrane is on the outer surface in contact with extracellular fluid (ECF), where water and ions is the main constituents. This is also the case for the intracellular fluid (ICF) on the inside of the membrane. The most predominant ions in the ECF and ICF is listed in Table 2.1.

The neuron actively regulates the permeability of the membrane, resulting in a change in ion concentration at the outside and inside of the membrane. A differential potential over the membrane is generated from the nature of ions as the net rate of diffusion is proportional to the difference in concentration. Since the diffusional and electrostatic forces oppose each other, they establish an electrochemical equilibrium.

The regulation of the membrane potential is conducted by three types of specialized membrane proteins:

- **Channels:** Passively allow ions to cross the membrane
- **Pumps:** Actively move ions across the membrane (requires energy)
- **Exchangers/transporters:** Uses the concentration gradient and a ligand to carry ions across the membrane

Ion channels is classified by gating, i.e. what opens and closes the channels. Voltage-gated ion channels (vg) open or close depending on the voltage gradient across the membrane, while ligand-gated ion channels open or close depending on binding of ligands to the channel. Channels may also be non-gated (ng) such as the ng-K^+ channel.

The most notable ion pump is the Na^+/K^+, which pumps 2x Na^+ out of the membrane, and 3x K^+ in for every ATP powered cycle. Since the membrane has an active ion gradient it proves that the ion pumps are maintaining a finite leakage current.

The Nernst equation relates the concentration gradient to the electrical gradient by

$$V_m^r = \frac{RT}{zF} \ln \left(\frac{[\text{ion}]_{outside}}{[\text{ion}]_{inside}} \right) \tag{2.1}$$

where R is the ideal gas constant, T the absolute temperature, z the ion valency, and F the Faraday constant.

The potential depends on the concentration of each ion listed in table 2.1, which represents the four most significant ions contributing to the membrane potential. The potential generated by each ion is calculated with the Nernst Equation (2.1) with the resulting potential in column E_{ion}.

TABLE 2.1: Ion concentration, ratio and charges. From [3].

Ion	*Out*	*In*	*Ratio*	E_{ion}
	mol	mol		mV
K^+	5 m	100 m	1:20	-80
Na^+	150 m	15 m	10:1	62
Ca^{++}	2 m	0.2 µ	10,000:1	123
Cl^-	150 m	13 m	11.5:1	-65

The ability of one ion to cross the membrane in comparison to other ions can be expressed as relative permeability (RP). Ions with high RP have greater impact on the membrane potential, and the RP can thus serve as a weight factor for each ion with respect to the final potential.

While the Nernst equation only considers one ion, the Goldman equation incorporates all ions by using the RP factor for each ion. The Goldman equation can thus be used to calculate the total membrane potential:

$$V_m^r = \frac{RT}{F} \ln \left(\frac{\sum_i^N P_{M_i^+} [M_i^+]_{\text{out}} + \sum_j^M P_{A_j^-} [A_j^-]_{\text{in}}}{\sum_i^N P_{M_i^+} [M_i^+]_{\text{in}} + \sum_j^M P_{A_j^-} [A_j^-]_{\text{out}}} \right) \tag{2.2}$$

In equation (2.2), each monovalent cation **M** and anion **A** is summed with the RP as weight factor. Using that the main contributors to the resting membrane potential V_m^r is Na^+ and K^+, the Goldman equation can be simplified to:

$$V_m^r = (61.54)\ln\left(\frac{P_{K^+}[K^+]_{\text{out}} + P_{Na^+}[Na^+]_{\text{out}}}{P_{K^+}[K^+]_{\text{in}} + P_{Na^+}[Na^+]_{\text{in}}}\right) \tag{2.3}$$

At rest the membrane is 40 times more permeable to K^+ than Na^+. By inserting this factor into (2.3) the resting potential can be calculated to $-65\,\text{mV}$ for an environment at $37\,^\circ\text{C}$

The action potential

The action potential (AP) can be divided into two main phases; rise (depolarization) and fall (repolarization & refractory), depicted in Figure 2.3.

Threshold is the potential required for the vg-Na^+ channels to open. When they do, a rapid influx of sodium is initiated in a positive feedback fashion. The more sodium that flows in, the more the membrane will depolarize. This is evident in Table 2.2 by observing the relative permeability of sodium in the rise phase.

TABLE 2.2: The relative permeability during the first states of the action potential. From [3]

Relative Permeability		
State	K^+	Na^+
Rest	40	1
Rise	40	400
Fall	100	1

As an example, the membrane potential can be estimated using the Goldman equation and the relative permeability. In the rise phase, Na^+ is 10 times more permeable than K^+, and by combining this with the concentrations in Table 2.1 into 2.2, we obtain

$$V_m^e = (61.54)\ln\left(\frac{1_{P_{K^+}}5_{[K^+]_{\text{out}}} + 10_{P_{Na^+}}150_{[Na^+]_{\text{out}}}}{1_{P_{K^+}}100_{[K^+]_{\text{in}}} + 10_{P_{Na^+}}15_{[Na^+]_{\text{in}}}}\right) \tag{2.4}$$

which calculates to 110 mV. Adding the resting potential, the final voltage is given by $-65\,\text{mV} + 110\,\text{mV} = 45\,\text{mV}$. This voltage coincides with the peak observed in Figure 2.3.

During the rise phase the open channels are ng-K^+ and vg-Na^+. In the falling phase the vg-Na^+ inactivates while some additional vg-K^+ channels open. The concentration changes rapidly in the reverse order and the potential drops, i.e the membrane hyper-polarizes. A very important sub-phase of the hyper-polarization is observed in Figure 2.3 as the refractory period. This is the result of a lager time constant of the vg-K^+ channels, which holds the vg-Na^+ at an inactivated state until the resting potential is re-established. This function limits the "firing" rate of the AP to the time constant of the vg potassium channel (approx 1000/sec, [3]).

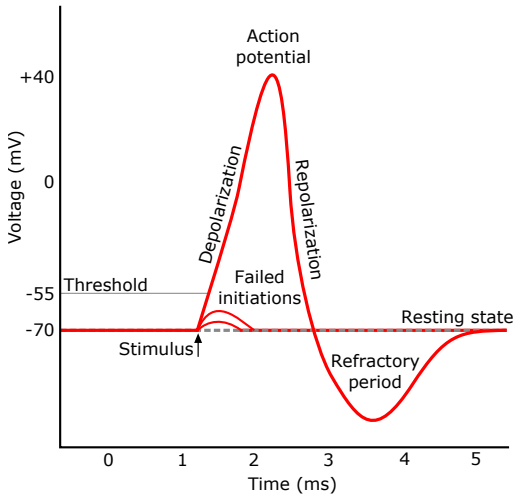

FIGURE 2.3: The Action Potential is a result of different time constants for (predominately) the Na^+ and K^+ permeabilities. The depolarizing phase is driven by the Na^+ influx, and the repolarization by K^+ influx and Na^+ efflux. The refractory preiod is a result of the slower time constant of the K^+ efflux, from [3]

2.1.3 The Hodgkin-Huxley model

The Hodgkin-Huxley model is a clever model which relates the membrane mechanics and action potential to passive circuit elements. The model represents a patch of neural membrane, which is useful when analysing the internal effects of an external applied potential or current, shown in Figure 2.4.

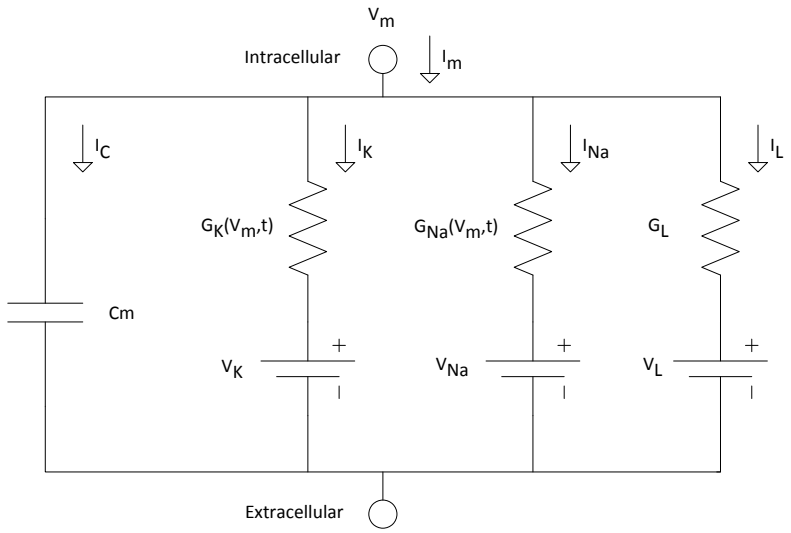

FIGURE 2.4: The Hodgkin-Huxley Model where C_m is the membrane capacitance, G_K and G_{Na} the non-linear conductances, and I_L the leakage current, from [3]

The first branch of the Hodgkin-Huxley model is the membrane capacitance current C_m. The conductance of the sodium and potassium channels is represented by G_{Na} and G_K respectively, with their associated Nernst equlibrium in V_{Na} and V_K. These conductances are dependent on both membrane potential and time, thus highly non-linear. The leakage current I_L represents all currents that do not flow through the other three branches. By using Kirchhoff's current law, the membrane density I_m can be expressed as

$$I_m = I_c + I_{ion} \tag{2.5}$$

where the ionic current is

$$I_{ion} = I_{K+} + I_{Na+} + I_L \tag{2.6}$$

which is the sum of the potassium, sodium and leakage contributions. Then for the complete membrane

$$I_m = I_c + I_{K+} + I_{Na+} + I_L \tag{2.7}$$

and by substituting each conductance with Ohm's law and the capacitor current with is derivative form, the membrane current is expressed as

$$I_m = C_m \frac{\mathrm{d}V_m}{\mathrm{d}t} + G_K(V_m - V_K) + G_{Na}(V_m - V_{Na}) + G_L(V_m - V_L) \tag{2.8}$$

where G_K and G_{Na} are functions of the membrane potential and time.

2.2 The electrode-tissue interface

The interface between the electrode and tissue gives rise to several processes that must be taken into consideration when applying stimulus to the electrode. These processes set the boundary for safety and efficiency of the stimulation, and is therefore a very important factor for the system architecture.

The Electrode-Tissue Interface (ETI) is reviewed in this chapter with the aim to

- Understand the principles of the two types of current flow at the interface
- Identify parameters essential to efficiency and tissue stability
- Develop an electrical interface model for electrical PNS stimulation

It is recommended to see the Apprendix B for a quick reference in electrochemical terms prior to the next sections.

2.2.1 Interacting with the biological electrolyte

Electrical stimulation of nervous tissue is possible by manipulating the biological charge carriers known as ions. The metal electrodes used for neural stimulation may take different forms based on the application, but will always be compromised of a noble metal with two or more terminals. The purpose of the electrode is to facilitate a transition in charge carriers, i.e. from electrons in the electrode metal to ions in the extracellular fluid, and vice versa.

The electrodes are inserted into the extracellular fluid (ECF) in close proximity to the axon membrane. The distance between the conducting surface of the electrode to the target axon poses an additional resistance, which may be significant for non-intrusive electrode types.

In Figure 2.5 the most predominant ions from Table 2.1 of the ECF is isolated together with a reference electrode (RE), working electrode (WE) and counter electrode (CE). The reference electrode is defined to have a zero electrode potential relative to the WE and CE. The working electrode is the stimulating electrode.

An equilibrium potential is established at the electrode surface when submerged into a solute, where the potential strength depends on the type of metal. Since a differential potential (electrochemical cell) is established if the WE and CE are made of two different metals, the electrodes used for neural stimulation is of the same metal to cancel out the potential: $E_{Cell} = E_{Cathode} - E_{Anode} = 0$.

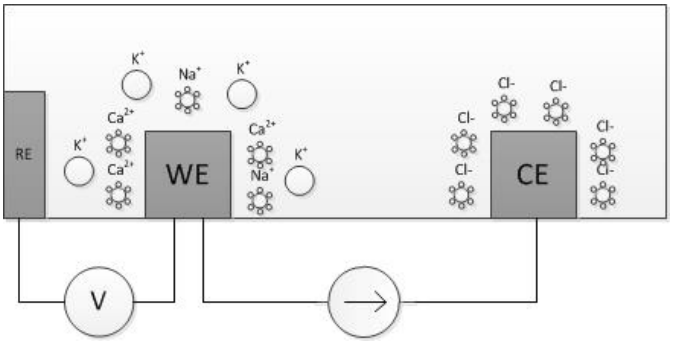

FIGURE 2.5: An example of the arrangement of the most predominant ions when current is applied between the working electrode and counter electrode.

Ions in the electrolyte will start to move toward the electrodes when the WE and CE is connected by a current source. In Figure 2.5 the WE will be negatively charged and thus act as a cathode, while the CE will act as the anode. Anions in the solution (Cl^-) will therefore go towards the anode, and the cations (K^+, Ca^{2+} Na^+) towards the cathode.

The immediate polarization of the electrodes will allow a transient of current, but a net current depends on a charge transfer between the electrodes and the electrolyte. Three electrochemical effects will affect the flow of current: the electrode-ion capacitance, a charge transfer resistance, and a solution resistance (limitation of ion flow in the solution) [2].

The total resistance (solution resistance and charge transfer resistance) will limit the current and elevate the potential at the electrode with a factor E. The overpotential η is observed by the voltmeter in Figure 2.5, and is the difference between the electrode potential and its equilibrium potential:

$$\eta \equiv E - E_{eq} \tag{2.9}$$

The overpotential η will be referred to in later sections.

2.2.2 Interface basics

There are two possible types of current flow at the interface:

Non-faradic - a redistribution of charge at the interface, reorientation of solvent dipoles or adsorption/desorption at the electrode surface (often referred to as the pseudo-capacitance)

Faradic - the exchange of electrons from the conductor to an ion or vice versa, with an associated electrochemical reaction

Non-faradic current flow includes electrostatic charge storage and "capacitive" charge transition, and is therefore often termed an electrical double layer. The term double layer originates from the fact that the electrostatic charge storage effect is opposed by a layer with opposite charge.

2.2.3 The electrical double layer

Non-faradic current flow is the optimal way for charge injection as it introduces a low-impedance path at the electrode-tissue interface. Non-faradic current flow is associated with reorientation of solvent dipoles, movement of electrolyte ions, and adsorption/desorption of specific species. These three elements make up the Electrical Double Layer (EDL) and are listed below:

1. **Redirection** of polar molecules, such as H_2O
2. **Redistribution** of charge in the electrolyte: the double layer capacitance
3. **Specifically adsorbed** species at the surface, also known as the pseudo-capacitance

It may be confusing to the reader to distinguish between the electrical double layer (EDL), and the double layer capacitance (number 2 in the above list). The EDL is the complete double layer effect that incorporates the 3 sources of charge storage. The double layer on the other hand only considers the double layer effect from the ion redistribution and dipole molecules in the solution (1 and 4 in Figure 2.2).

Redirection of polar molecules in an aqueous electrolyte as the ECF implies flipping the polar water molecules. Electrostatic charge is freed by redirecting these molecules. The first element of the surface capacitance is therefore the solvent dipole (H2O) which forms at the innermost layer at the electrode surface.

Redistribution of charge will give rise to a transient transfer of electrons as the metal ions in the electrolyte combine with the electrode (4 in Figure 2.6). The

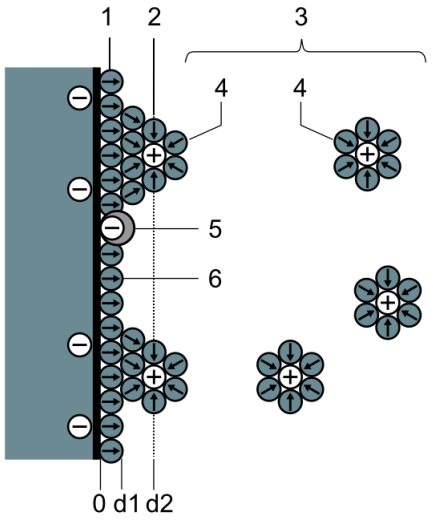

FIGURE 2.6: The double layer, composed of 1. IHP, 2. OHP 3. Diffuse layer, 4. Solvated ions with their hydration shell, 5. Specifically adsorbed ions (pseudo-capacitance), 6. Electrolyte solvent molecules (H_2O). Note that 1-3 are the planes of charge, while 4-6 are specific species in the solution. From [3]

following plane (2) is the Outer Helmholtz Plane (OHP), and is simply a plane of opposite charge, acting as counterions in the electrolyte. These two layers of opposite polarity is together known as the electrical double layer (DL).

The double layer has its capacitance from charge stored electrostatically by a molecular dielectric. The double layer is created from a plane of attracted ions which have a more loosely connected plane of charge (diffuse layer) in a distance from the first layer. This plane acts as a layer of counterions to the first layer.

While the double layer and the directionality of the solvent dipoles stores charge electro-statically, the pseudo-capacitance "stores" charge by electron transfer via adsorption/desorption at the conducting surface. The pseudo-capacitance is a complex phenomenon and is therefore discussed in a separate section below.

2.2.4 Pseudo-capacitance

Pseudo-capacitance is a feature of the conducting surface in the electrode. The interface between reactant species and the conducting surface results in a capacitive effect with very high capacitance due to adsorption at the surface. The pseudo-capacitance shares the same geometric surface as the double layer (5 and

4 in Figure 2.2.3), but may have 10 to 100 times more capacitance compared to the double layer, Conway et al. [4]. Supercapacitors are based on this effect to achieve capacitances in the area of hundreds to thousands of farads. One can say that electrodes with pseudo-capacitance utilizes supercapacitor-like performance.

The principle behind the pseudo-capacitance is partly revealed by the name: it is a capacitive charge storage, but does not hold the same properties as a true capacitance. While a true capacitance works by charge stored electrostatically (as the double layer), the pseudo-capacitance is a result of a reversible faradic reaction that does not break any chemical bonds. The product species from the reaction may therefore be adsorbed to the electrode surface and recover to its original state without the intermediate state as an activating complex. This is crucial, as the product species must stay close to the conducting surface to be available for the reverse reaction, and can not be allowed to diffuse away.

Reactions that facilitate the pseudo-capacitance includes hydrogen plating (Reaction 2.12) as well as reversible oxide formation and reduction (Reaction 2.14 and 2.13 respectively).

Pseudo-capacitance is important for charge injection as it will significantly lower the impedance at the ETI, thus providing a charge transfer at much lower overpotential η. The overpotential is associated with irreversible faradic reactions by e^{η} (as electrolysis of water), and large capacitive values for the pseudo-capacitance will therefore bring the overpotential within the range of safe operation (e.g. the water window). Electrical models for the ETI presented in Section 2.3.4 illustrate how the pseudo-capacitance can reduce the overpotential.

The pseudo-capacitance is depending on the real surface area (RSA) and the geometric surface of the conducting surface, as well as the reactant species that adsorbs to the surface [2]. The RSA is determined by multiplying the roughness factor of the metal with the geometric surface area, which can be considerably elevated by the use of oxide layers as iridium oxide. Some electrode technologies as the Activated Iridium Oxide Film (AIROF) electrode (Troyk et al. [5]) is based on the utilization of iridium oxide.

2.2.5 Faradic charge transfer

Contradictory to the charge storage of the electrical double layer, the faradic charge transfer may be considered as an element of charge dissipation. Faradic charge transfer is a result of a chemical reaction at the electrode surface, where this reaction always will reduce or oxidise a reactant. This reaction introduces a risk to the tissue stability as reaction products may diffuse away from the electrode, furthermore altering the local environment or entering the bloodstream. The general way to handle this problem is to reverse the current before the product species have time to diffuse away, and thus recover the reaction product back to their non-threatening original state.

It is important to understand the process of faradic charge transfer as it may result in tissue and/or electrode damage. The net faradic current can be expressed as [3]:

$$i_{net} = i_0 \left\{ \frac{[O]_{(0,t)}}{[O]_{(\infty)}} e^{(-\alpha n f \eta)} - \frac{[R]_{(0,t)}}{[R]_{(\infty)}} e^{((1-\alpha) n f \eta)} \right\} \tag{2.10}$$

which relates the net current i_{net} to the current exchange density i_0 and an exponential function of the overpotential $e^{K\eta}$ with a constant $K = \pm\alpha\frac{F}{RT}\eta$, as well as the concentration of an reactant M at the electrode surface $\frac{[M]_{(0,t)}}{[M]_{(\infty)}}$ where $[M]_{(\infty)}$ is the bulk concentration and $[M]_{(0,t)}$ the concentration at a distance (x=0) from the electrode surface as function of time.

Equation 2.10 is an extension of the Tafel equation where both the anode and cathode is included. The Tafel equation relates the electrochemical reaction rate to the overpotential, where α is the charge transfer coefficient, T the absolute temperature, R the gas constant, and F the Faraday constant. The sign of α indicates if the reaction is anodic or cathodic for plus and minus respectively.

Equation 2.10 expresses three important elements of faradic charge transfer. First, the current exchange density i_0 is the "background current" which always exists

at each electrode. It is this current that maintains the electrode potential, and as observed in the equation, a larger exchange current density lowers the total impedance, by the ability to inject more current at a lower overpotential η

The second factor is the available reactant M for the redox reaction. As evident in the equation, a reduction in available reactants must be countered by a higher overpotential to sustain the same current. Third is the overpotential itself, which is related to the net current by an exponential factor. Small changes in the overpoential will therefore result in large changes to the net current.

Faradic charge transfer will always be associated by a reduction or oxidation of the ion that accepts or loses electrons respectively. With a platinum-iridium electrode in a solutions such as the ECF, the redox reactions may take the following forms, from [3]:

Reduction: Cathodic processes (electrons passed from electrode to electrolyte):

Reduction of water:

$$2\,H^+ + 2\,e^- \longleftrightarrow H_2\uparrow + 2\,OH^- \quad (2.11)$$

Hydrogen atom plating:

$$Pt + H^+ + e^- \longleftrightarrow Pt{-}H \quad (2.12)$$

Platinum oxide formation and reduction:

$$PtO + 2\,H^+ + 2\,e^- \longleftrightarrow Pt + H_2O \quad (2.13)$$

Iridium oxide formation and reduction:

$$2\,IrO + 2\,H^+ + 2\,e^- \longleftrightarrow Ir_2O_3 + H_2O \quad (2.14)$$

Oxidation: Anodic processes (electrons passed from electrolyte to electrode):

Oxidation of water:

$$2\,H_2O \longrightarrow O_2\uparrow + 4\,H^+ + 4\,e^- \tag{2.15}$$

Platinum corrosion:

$$Pt + 4\,Cl^- \longrightarrow [PtCl_4]^{2-} + 2\,e^- \tag{2.16}$$

Cloride gas evolution:

$$2\,Cl^- \longrightarrow Cl_2\uparrow + 2\,e^- \tag{2.17}$$

These processes are initiated from the activation energy resulting from the overpotantial. To keep faradic reactions at a minimum, it is favourable to keep the overpotantial as low as possible.

2.3 Challenges in electrical excitation

2.3.1 Tissue stability

There are three main topics with regards to tissue stability that recurs consistently in the literature:

- Charge balance
- The "water window"
- Mass action theory

Charge balance and the water window are both related to the electrolysis effect that occurs at the electrode surface. The mass action theory on the other hand is related to a degeneration in neural response due to over-stimuli of the neurons.

Charge balance

When injecting charge into the ECF there will always be some sort of faradic reaction at the electrode surface, i.e. a redox reaction at each conducting surface. While it is top priority to avoid irreversible faradic reactions, it is beneficial to utilize the capacitive effect of reversible faradic reactions, i.e. as pseudo-capacitance.

Charge balance refers in short to obtain net zero electrolysis products, ensuring that no reaction continues more in one direction than the other. The key factor is to make the electrolysis products of the reactions go back to their original form, thus keeping the net electrolysis products to equal zero. Any accumulation of such products may harm the surrounding tissue by altering the pH value or entering the bloodstream [2].

It is generally accepted that keeping the stimulus free from any DC current is a primary goal for obtaining charge balance, even though it is mentioned by Merill [2] that zero net current does not necessary equal zero electrolysis products.

The water window

The water window is defined as the upper and lower allowed potential excursions at the interface, where if violated, a faradic reaction will start to reduce or oxidise water.

Water is abundant in a solution as the ECF, and the reaction will therefore not become mass transport limited [2]. The consequence is evolution of hydrogen and oxygen gas at the electrodes (reaction 2.11 and 2.14 respectively) where an abundance of reaction molecules will sustain the reaction as long as a continuous flow of charge is present. Hydrogen and oxygen evolution are both highly irreversible reactions, and result in a significant impact on the pH level.

It is therefore crucial to stay within the water window when injecting charge into the tissue. The boundaries of the water window can be analysed using a Cyclic Voltammetry (CV). A CV for platinum and iridium film is shown in Figure 2.7,

conducted by Lee et al. [6]. The plot shows that the water window for both metals is in the range of $-0.65\,\mathrm{V}$ to $0.8\,\mathrm{V}$, which is a limit that recurs consistently in the literature. It is also interesting to observe the enhanced surface charge capacity for the iridium film compared to the platinum film, resulting in the higher current density for the iridium at lower potentials.

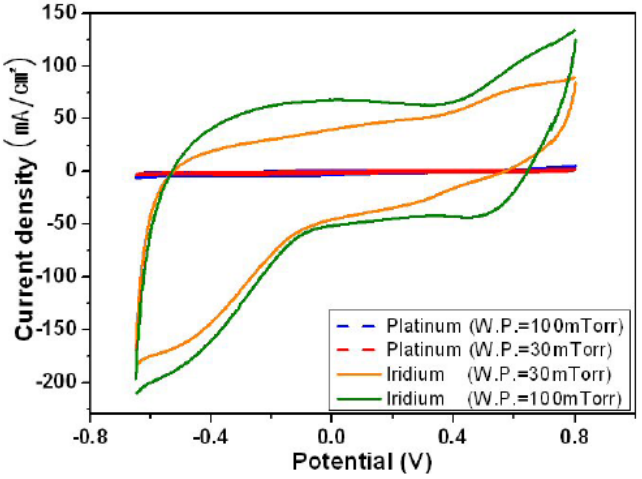

FIGURE 2.7: Cyclic voltammogram of platinum and iridium film. Measured in 0.9% NaCl solution at $100\,\mathrm{mV\,s^{-1}}$, from [6]

Mass action theory

The mass action theory originates from the observation that neurons which are firing over an extended period of time will lose their ability to be excited electrically. The theory suggest that the culprit is from changes in the local environment by depletion of oxygen or glucose, or changes in ionic concentration [2].

Agnew et al. [7] found axons in the peripheral nerve to degenerate if stimulated with frequencies at 50 Hz, while damage were absent in stimulation frequencies at 20 Hz. The effect was named EAD: Early Axonal Damage, and was a result of prolonged stimulation where the axons lost the ability of electrical excitability due to severe stress for several hours. Agnew concluded that EAD could be greatly reduced by using interrupted stimuli (e.g. 5 seconds on, 5 seconds off) if higher stimulating frequencies was required.

2.3.2 Generating the action potential

The simplest electrode type for stimulation of peripheral nerves is the cuff electrode shown in Figure 2.8. The electrode in this example is bipolar; is has two terminals and is similar to the setup in Figure 2.5 when the reference electrode is omitted.

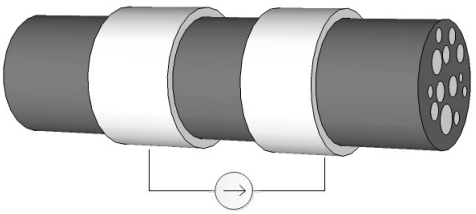

FIGURE 2.8: The simplest configuration for a bipolar cuff electrode. The cuff wraps around the nerve at two sites and conducts current in axial direction.

The cuff electrode has two layers, where the outer layer is made of an insulating material (often silicone) and the inner layer of a conducting material (often platinum). A simple model that relates the ion dynamics at the electrode is shown in Figure 2.9, where all layers of the nerve are omitted to directly analyse the potential difference over the axon membrane (axolemma) and the ECF.

The membrane at rest holds a negative potential difference with respect to the outside of the membrane. When the working electrode (cathode) in Figure 2.9 is active, the positive ions (cations) will attract to the surface. The secondary effect is that all ions further away from the cathode will be of opposite polarity, and thus the ions close to the axolemma will be of negative charge. The differential potential over the membrane is now lower as both the inside and the outside of the membrane has a negative potential, which results in depolarization of the membrane. For a sufficient current density it will depolarize the membrane to threshold, and generate an action potential locally in this area.

The action potential is therefore generated by charging the membrane capacitance C_m in the Hodgkin-Huxley model (Figure 2.4) from the injection of current in the ECF. In other words will an applied voltage to the electrode not couple the AP

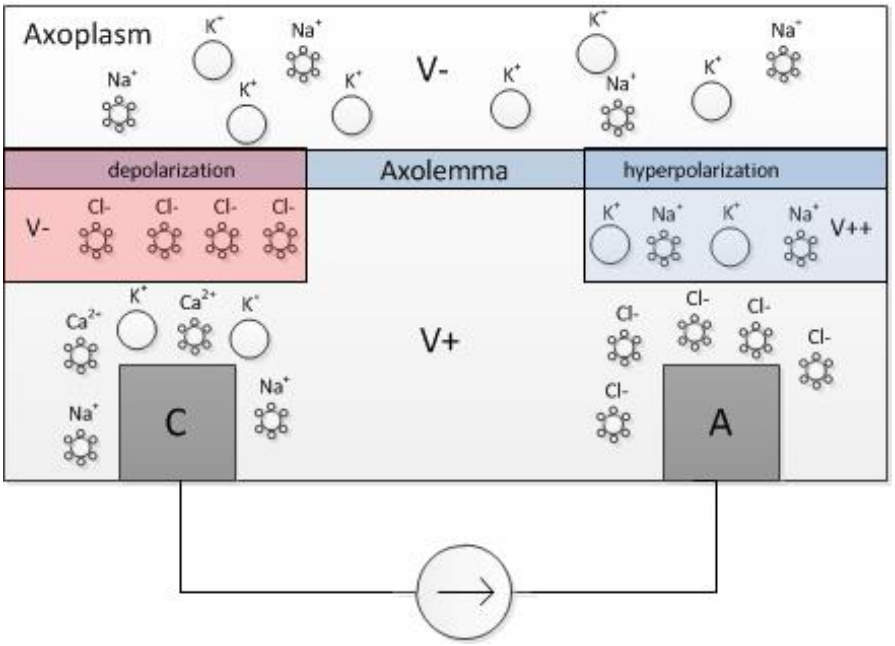

FIGURE 2.9: Electrical excitation of the neuron by redistributing the ions outside the axon membrane. The figure is simplified to include a small selection of ions with their hydration shells.

directly, as the voltage is not ion specific, and cannot access the ionic current in the membrane.

The contrary effect to the cathode happens at the anode, as anions will attract to the the electrode terminal, and cations will be present close to the membrane. The differential potential over the axonlemma is now said to be hyperpolarized, i.e. more negative than in the resting state.

This hyperpolarization is similar to the natural refractory period of the action potential (AP, Figure 2.3), and shares the same AP blocking property (anodic blockage) [2]. The anode is thus blocking the AP from conduction in cathode to anode direction, and the placement of the electrodes is therefore important upon implementation. The principle is illustrated in Figure 2.10.

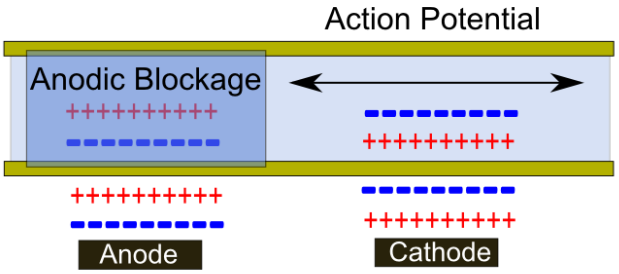

FIGURE 2.10: The propagating action potential is blocked in the anodic direction to produce an UPAP - Unidirectionally Propagating Action Potential.

2.3.3 Stimulating waveforms

The stimulating waveform, also referred later to as Microstimulating Output (MSO), must be efficacious for AP generation and be stable for tissue damage and corrosion of the electrode. The most common waveforms is shown in Figure 2.11.

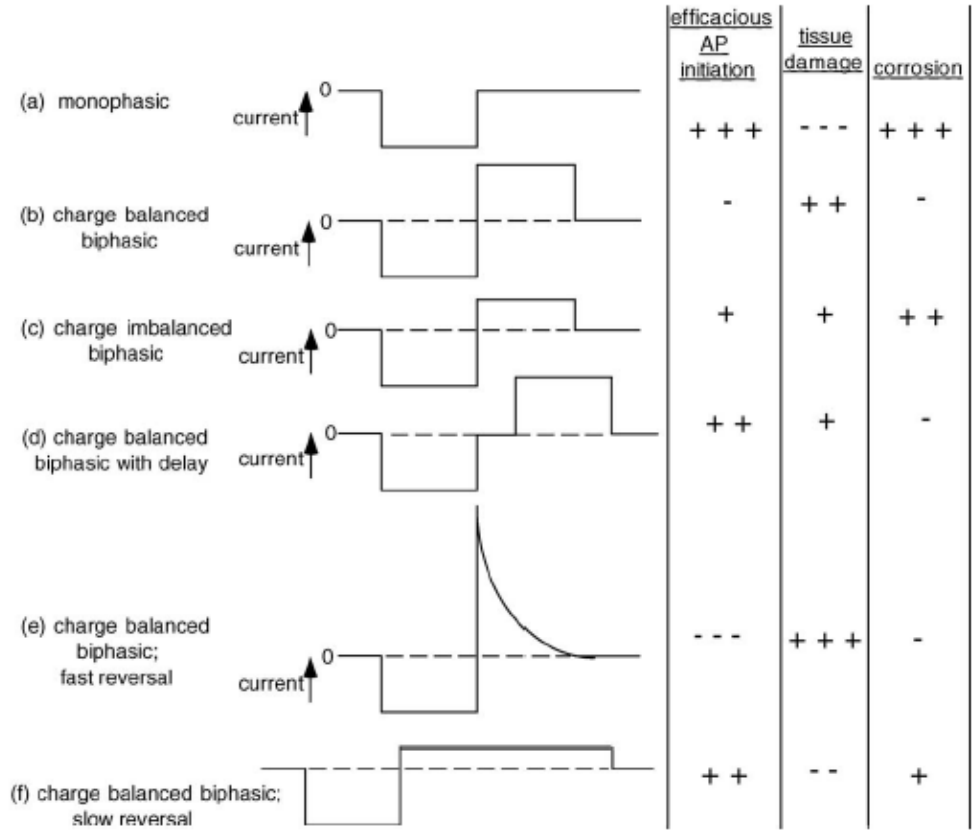

FIGURE 2.11: Comparison of stimulating waveforms. The markings "+++" indicates best performance and "- - -" the worst. Figure from [2]

The "standard" and simplest waveform is shown in (a): the monophasic pulse. This waveform is a cathodic pulse first followed by a long period where the electrodes are disconnected from the stimulator. This facilitates a slow reversal of species at the electrode surface, but the problem is that the overpotential may not go completely back to the pre-pulsed electrode potential, and a "ratcheting" of potential may occur over time. The overpotential may then drift outside the water window, resulting in severe tissue damage.

All the other waveforms (b)-(f) are basically an extension of the monophasic pulse, where the second phase is intended to correct for the problems with (a) using a reversal in current shortly after the first stimulus.

The charge balanced biphasic pulse (b) is a simple way to ensure that the injected charge is sufficiently reversed. The problem here however, is that the anodic phase follows directly after the cathodic, thus reducing the efficiency as some neurons may not have had the time to meet threshold. A second problem is that the anodic amplitude is very high, where faradic processes is associated with oxidation (corrosion) of the electrodes in the anodic phase.

The imbalanced biphasic pulse (c) reduces the most positive potentials and the associated electrode corrosion.

In (d), an open potential interphasic delay (IPD) is used between the cathodic and anodic phase, providing more efficient AP generation. This pulse does still have a high anodic potential, which may lead to corrosion.

In (e) it is shown a rapid reversal in the anodic phase driven by the natural discharge of the EDL when shorting the leads together. This is beneficial for the tissue as the reactant species go back to their original form before they have time to diffuse away, without driving the reaction with an externally applied potential. Since the EDL capacitance is completely discharged for a sufficiently long discharge period, a train of succeeding pulses will not result in an elevated potential over time (the so-called "ratcheting" effect) and thus ensure that the potential stays

within the water window. However, as there is no IPD, the AP generation can be negatively influenced by the rapid discharge.

The charge balanced biphasic pulse in (f) is efficient and good for corrosion as the anodic potential is low. The slow reversal is however not good with respect to the tissue, as the anodic potential may be insufficient for proper reactant reversal.

Proposed optimal waveform

An optimal pulse was proposed in [3] based on the stimulation waveforms that combines the best features of each type, shown in Figure 2.12. This waveform is intended to have a standard cathodic first pulse followed by an interphasic delay and a short circuit of the cathode and anode. A circuit where the the cathode is shorted to the anode is termed an exhausting scheme [2], and ensures that the electrode potential is quickly brought back to the equilibrium potential to avoid diffusion of reactant species.

The benefits of a such waveform is the monophasic efficiency, low anodic potential with low corrosion, and ensuring charge balance if the electrodes are shorted for a long period of time.

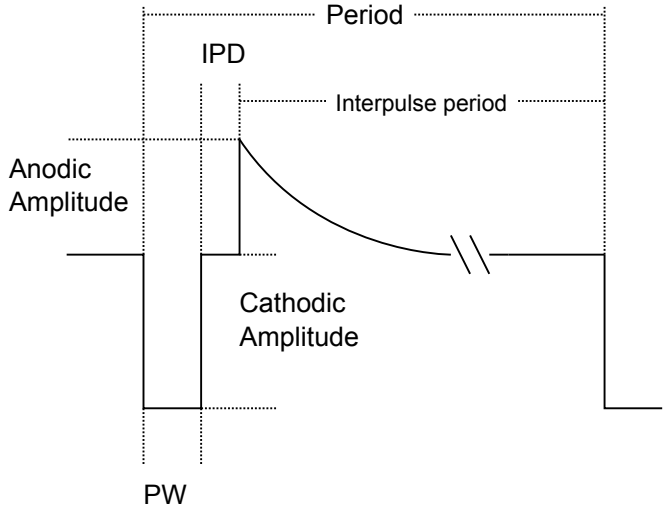

FIGURE 2.12: Suggested MSO for optimal current injection. The cathodic phase is followed by a an interphasic delay before the anodic phase is driven by the natural discharge in the ETI with peak limitation. Taken from [3].

2.3.4 Electrical model

There are several different models for the electrode-tissue interface in the literature. The most common models are shown in Figure 2.13, where (a) is the detailed model with specific branches for each process at the interface and (b) is a simplified version of (a). The model in (a) incorporates a Warburg element Rw for the diffusion in the solute in addition to the ETI processes. The model in (b) is the most common model when not studying specific processes at the interface, and the overpotential can then be approximated to equal the voltage over Rf, i.e. $\eta \approx V_{(Rf)}$.

The model (b) is present at each electrode terminal. The overpotential can then be expressed in terms of the applied voltage V_{MSO} by voltage division over Rs. If Z_{ETI} represents the parallel branch of Rf and $Cedl$, the following relationship can be derived:

$$\eta = \frac{V_{MSO}}{\frac{R_s}{Z_{ETI}} + 2} \tag{2.18}$$

Equation 2.18 shows that the overpotential is reduced for large $Cedl$ values by lowering the interface impedance since $Z_{ETI} = \frac{R_f}{1 + sR_fC_{edl}}$. It is hypothesized that the solution resistance R_s is much larger for peripheral nerves using cuff electrodes, compared to an interface for the CNS. The reason is that the distance between the electrode terminals is much greater, as well as the layers of connective tissue shown in Figure 2.2 restricts current flow. This explains how it it possible to apply up to 11 V over the terminals without exceeding the water window, as most of the voltage drops over the solution resistance and not the interface. Stimulating systems found in the literature for CNS stimulation usually has an output voltage bounded directly by the circuitry to stay within the water window, indicating a low solution resistance.

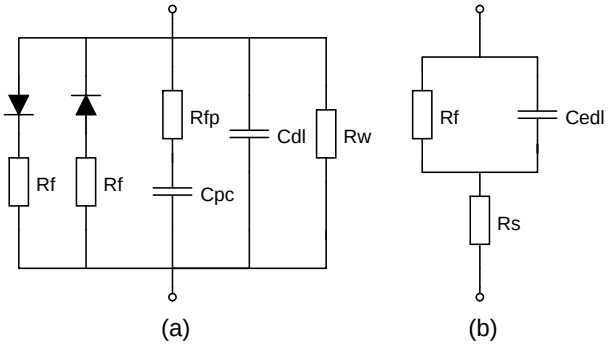

FIGURE 2.13: The electrical model (a) incorporates in the faradic reactions driven by an activation potential in the diodes in series with the Rf resistance. The pseudocapacitance is modelled in the branch consisting of Rfp and the capacitance Cpc. The double layer is reprented by Cdl. The resistance Rw is the Warburg element, modelling the diffusion in the solute. The model (b) is a simplified model where the Warburg element is omitted, all faradic processes summed in Rf, and all capacitive in $Cedl$. This model also includes the solute (ECF) resistance, Rs.

2.4 Design considerations for a neural stimulator

2.4.1 Tissue stability

The water window is defined as the safe range of voltage deviation at the interface, approximately $-0.65\,\mathrm{V} < \eta < 0.8\,\mathrm{V}$. The applied potential V_{MSO} can thus not exceed the impedance reduction by the pseudo-capacitive property of the electrode.

An exhausting scheme ensures that there is no potential build-up (ratcheting) at the interface, and helps holding the potential within the water window (Figure 2.11 (e)).

The charge balance should be close to zero, resulting in no bias current (DC component). A residual DC level of $250\,\mathrm{nA\,mm^{-2}}$ was found to be safe for stimulation in the auditory nerve [8], and $1.16\,\mu\mathrm{A\,mm^{-2}}$ for skeletal muscle stimulation [9] with values adjusted for electrode surface and stimulus frequency. The DC limit for PNS stimulation using cuff electrodes is assumed to lie in between these limits.

A distant ground is present via the tissue-device capacitance. This is a problem if one electrode is active without the counter electrode, as the distant ground may force the interface potential outside the water window. The potential over the electrode terminals must therefore be zero at all times when the device is not stimulating the tissue, i.e. having the terminals disconnected from the circuit or shorted together. If the problem is solved by isolating the electrodes from the rest of the circuit, it is assumed that the associated leakage current should be in the low nA range based on the study conducted by Huang et al. [8]. The information concerning a distant ground was provided by Luke Theogarajan.

Current controlled system The MSO should derive from a current controlled system delivering a fixed current density to the interface. The charge injected into the tissue is monitored since $q = \int_{t_0}^{t_1} i(t)\,dt$ where $t_1 - t_0$ is the duration of the stimulus. Contrary, a voltage controlled system (VCS) will have an output changing with the tissue growth and fibrosis, resulting in an uncontrolled overpotential at the interface.

The anodic phase should not have an increasing amplitude following the discharge if using the exhaustive scheme in Figure 2.11 (e). The reason is that the natural discharge will follow the rate of reversal and diffusion in the solute. If a larger current output is present after this discharge, the result may be that new reactants is consumed in a process which is not the reverse of the cathodic, possibly resulting in tissue damage.

2.4.2 Efficiency

Interphasic Delay (IPD) is important for not degrading the action potential. The delay is in the µs range, and is a period where the electrodes is disconnected from the circuit between the cathodic and anodic phase.

Cathodic first pulses is found to be most effective for generating the action potential. The preceding anodic phase must be delayed with the IPD.

The configuration for a VNS application must be with the cathode proximal to the brain. It is therefore crucial to map which conducting surface that is connected to which conductor at the electrode pin. It was confirmed by a clinical engineer at Cyberonics that the m102 MSO is indeed evoking UPAP's.

Load switching to avoid distant ground problems

The rectangular shape of the cathodic pulse is equivalent to switching a load on and off due to the steep edges. Load switching is always comprised of an pass element (often a MOSFET due to the low ON resistance), a driver to control the pass element, the load, and a "hot" rail with relatively high voltage, shown in Figure 2.14. The high side configuration in (b) is obligatory for a neural stimulator to avoid distant ground problems.

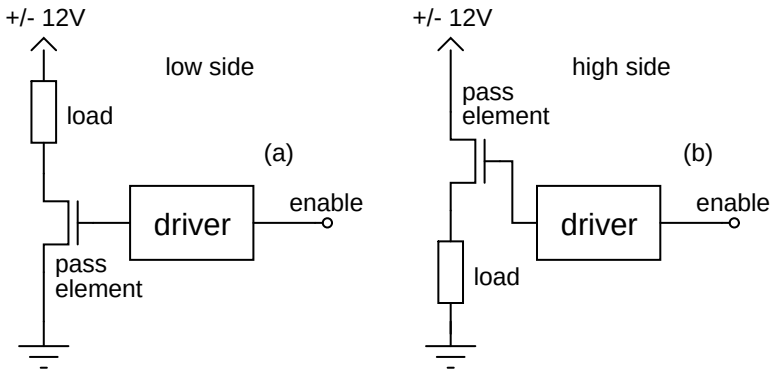

FIGURE 2.14: A low side switch is shown in (a), and a high side in (b). A low side configuration is unacceptable for a neural stimulator as the power rail is connected directly to the neural tissue, as a distant ground will let some current pass uncontrolled into the tissue, possibly resulting in damage and electrode corrosion. The high side switch is necessary to provide zero voltage over the load at times with no pulsing. This topology is however more complicated, as the driver must handle the voltage variations over the load.

Chapter 3

System requirements analysis

This chapter defines a high level system architecture based on the requirements from the end user together with the findings in Chapter 2. The end user requirements analysis is in large part based on the measured output from the Cyberonics m102 stimulator shown in Figure 3.1. The result is the system design specification with an associated modular architecture given in Section 3.3.

The design specification is the blueprint for the system design and implementation in Chapter 4.

FIGURE 3.1: The Cyberonics m102 Vagus-Nerve Stimulator, which is the device that the end user requested in 1/2 of the size. The m102 stimulator has a volume of 14.7 cm^3. From [10]

3.1 Device requirements

The requirements given by the end user:

1. **Features**
   (a) Device compatible with the Cyberonics 304 electrodes
   (b) Device implantable for use in laboratory rats
2. **Output**
   (a) 2 mA @ 30 Hz - 500 µs pulse width
   (b) Capable of loads up to 5 kΩ
3. **Size**
   (a) Maximum encapsulated size 1/2 of the Cyberonics m102
   (b) Maximum height 7 mm
4. **Operation**
   (a) Minimum device life: 3 months
   (b) Option of recharging or replace power source
   (c) Device Duty Cycle (DDC) @ 18 %: 60 sec ON / 5 min OFF *
   (d) Event feedback to the operator
      i. Nerve is properly connected to electrodes
      ii. Device is close to end of service

** Duty cycle is calculated by dividing stimulation time (programmed ON time plus 2 seconds of ramp-up time and 2 seconds of ramp-down time) by the sum of the ON time and OFF time* - From the m102 technical information [11].

3.2 Requirements analysis

General analysis

Features: To comply with req. 1a the electrodes must be connected to an ETI model and the output measured. This is to map the microstimualting output (MSO) for the design of an compatible driving circuit. An electrode pin connector must be designed for connecting the 304 leads to the PCB.

To be implantable for req. 1b, the device must be encapsulated in an implementation grade bio-compatible material such as a noble metal (e.g. titanium) or a bio-compatible silicone/epoxy.

Ouput: The specified output given by the end user is the programmed values for the m102 stimulator. The MSO measurements must reveal any eventual deviations in these values as the real output may vary from the values given in the manual (2 mA @ 30 Hz, 500 µs PW). The real measured values will complete req. 2a.

To comply with req. 2b the available voltage over the load must be at a minimum of 10 V for a pure resistive load (worst case scenario).

Size: The specified size gives leeway for several different configurations of the main components (battery, PCB and electrode connector). The shape should not have any sharp edges, and a round shape is therefore favourable. To comply with req. 3a the main component must be arranged in a way that minimize space.

To comply with req. 3b the main components should not be stacked unless made very thin.

Operation: To comply with req. 4a the total power requirement must be estimated using the device duty cycle together with the minimum device life. This should be achievable when the necessary modules are identified.

The power source should be a replaceable battery to keep the design as simple as possible. The battery can be changed when either removing or disconnecting the encapsulating layer, to comply with req. 4b.

A module for timing of the output is necessary to comply with req. 4c.

Requirement 4d demands a sensing circuit to detect load impedance and battery state which is passed on to the operator. The event feedback to the operator is mechanically restricted by the encapsulation, and a wireless solution will add unnecessary complexity to the design. Feedback via sound is possible using a small piezoelectric buzzer, but a visual feedback via LED(s) will be a a more compact solution. In that case the encapsulating layer must be tested for sufficient transparency.

System specific analysis

List of requirements that must be analysed in detail:

Req. 1a: Identify a compatible driver for the 304 electrodes. The driver that generates this output is defined as the Stimulating Front End (SFE).

Req. 2a: Identify the parameters of the stimulating output (MSO).

Req. 4b: Suggest an eligible power source based on req. 4c.

The following sections will cover the detailed analysis of the items in the above list. The rest of the requirements is analysed and defined directly in the system design specification in Section 3.3.

Analysis is performed with req. 2a first, following req. 1a and then req. 4b.

3.2.1 Req. 2a: m102 MSO analysis

The results from Moen [3] is presented to obtain the fundamental MSO parameters. The Cyberonics model 102 stimulator was measured for the associated MSO.

Setup

The measuring setup is shown in Figure 3.2 and 3.3. The data was copied into MATLAB by a Handyscope HS3, measuring current over a 1 kΩ resistor. Algorithms were written to identify periodicity, net current and variance by using the "Signal Processing Toolbox" in MATLAB.

Sampling rates from 96 kHz to 3 kHz were used, depending on which part of the signal that was analysed. The sampling rate for each measurement is specified in the respective plot.

The output of the stimulator was analysed and limited to two cases of load composition: capacitive/resistive and pure resistive.

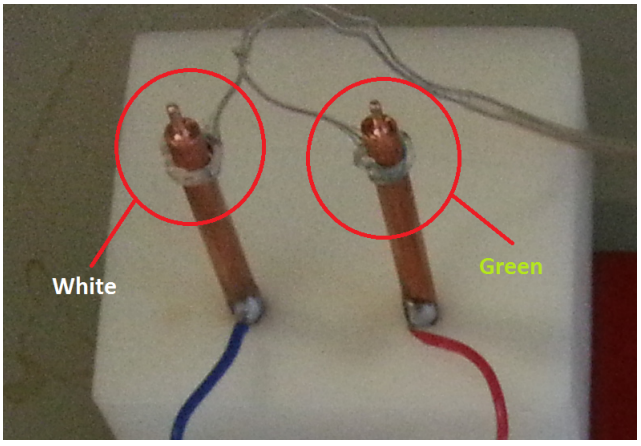

FIGURE 3.2: The electrodes were attached to two copper rods for proper contact with the conducting surface. A thin thread is incorporated into the electrode silicone and serves as a convenient support upon implementation. The thread is coloured in green and white, indicating the cathode and anode respectively. Though difficult to see on the picture, the white electrode is on the left, and the green on the right.

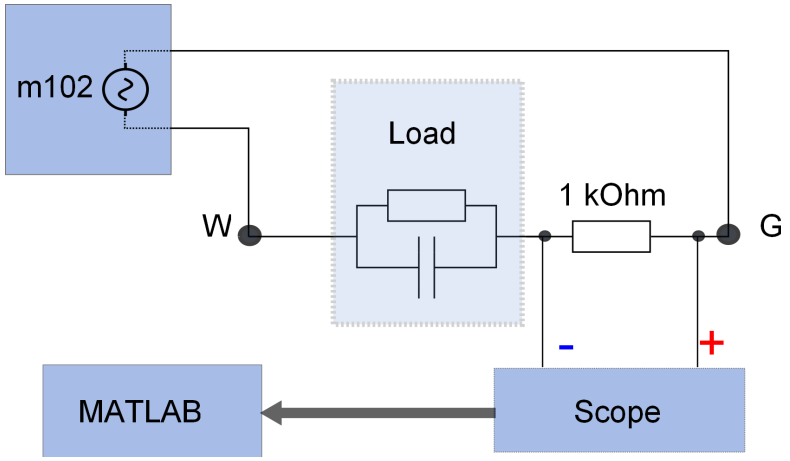

FIGURE 3.3: The scope measured over a 1 kΩ resistor in series with the ETI model. Note that the measuring resistor acts as an equivalent solution resistance to the complete load.

TABLE 3.1: The parameters of the Cyberonics stimulator model 102 stimulating output. The stimulator was programmed to output a stimulus of 2 mA @ 30 Hz - 500 µs PW

Parameter	Description	Value
Biphasic pulse	Yes	"Exhaustive" scheme
Zero net current	No	15 µA
Interphasic delay (IPD)	Yes	22 µs
Consistent cathodic amplitude	Yes	2 mA
Consistent pulse period	Yes	34 ms

The load values were based on studies on the ETI impedance by Laaziri et al. [12]. A range of loads were tested and narrowed down to two different configurations shown in Table 3.2. In the first configuration the load was purely resistive, emulating a condition where the ETI has no electrical double layer. In the second configuration the load was a parallel circuit of a resistance and capacitance with values matching [12], but simplified for an easier test environment.

The 1 kΩ resistor used for the current measurement provided a convenient scaling of 1:1 mA/V. The measuring resistor emulates the solution/tissue resistance.

The identified parameters are listed in Table 3.1. The net current (charge balance) was expected to be zero as to avoid any electrolysis products. The positive bias current was therefore very surprising.

TABLE 3.2: The two loads used. Note that the loads is placed in series with the 1 kΩ measuring resistor.

Loads used for output analysis Descriptor	Resistance Series	Resistance Parallel	Capacitance Parallel
PR - Pure Resistive	2 kΩ	∞	0
COM - Complex	0	2 kΩ	100 nF

Measurements results and parameter identification

The measurement shown in Figure 3.4 reveals that the MSO has two phases of stimulation when pulsed over the COM load. The output is composed of a cathodic first pulse followed by an interphasic delay (IPD, shown in Figure 3.5), and then the anodic phase. The anodic phase is not a "true" anodic phase, as it is merely a result of a discharge of the accumulated charge in the cathodic phase (shorting the leads together, the so-called exhaustive scheme). Since there is a small positive current flowing in this phase, the output is considered biphasic. The cathodic pulse width, current bias, interphase delay, and frequency of the MSO was measured to be consistent.

The results is summarized in Table 3.1 and specifies requirement 2a. The conclusion is that the requirement of the stimulating output (2 mA @ 30 Hz - 500 µs) is consistent, except that the IPD and the anodic phase with the net current is not described. This is the subject for req. 1a in the next analysis.

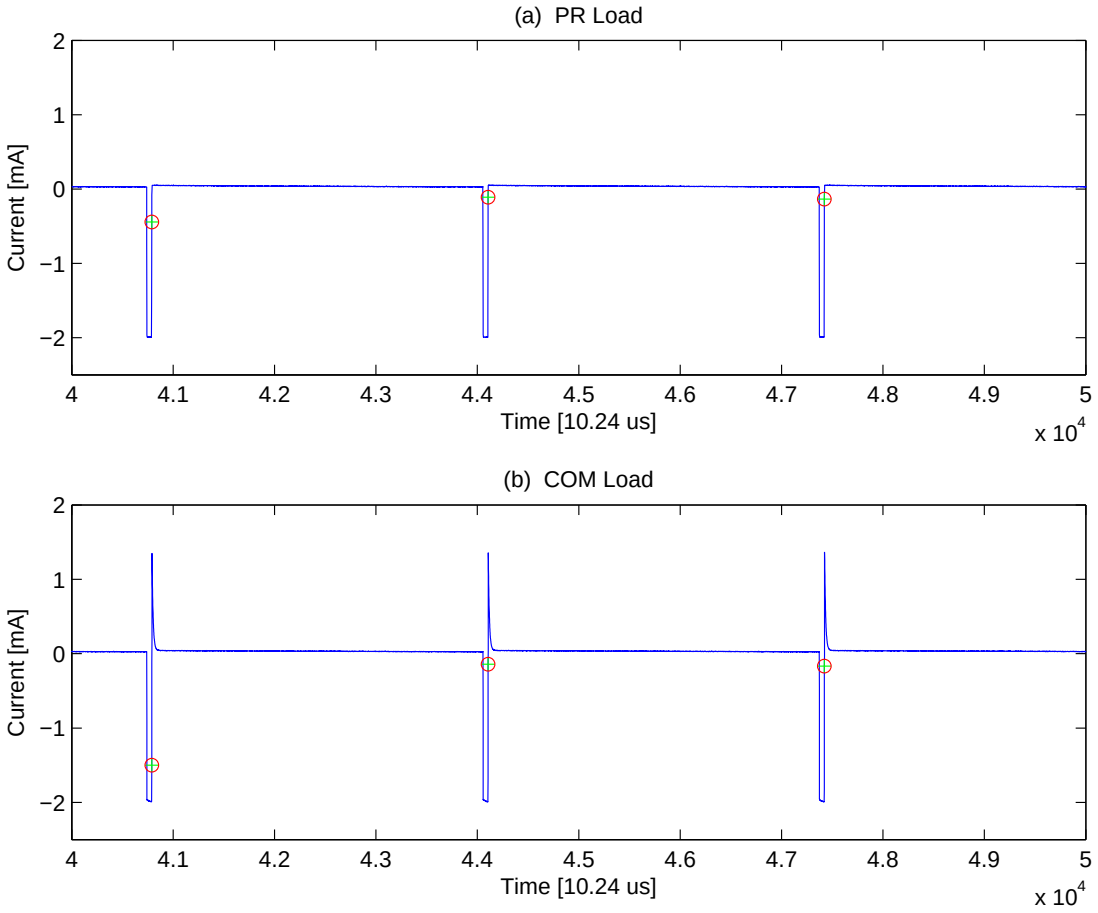

FIGURE 3.4: Data sampled at 97.6 kHz @ 12 bit and captured 31 periods. The green cross indicates the starting point for the measured period, while the red circle is the end point. For two unequally placed points there will be a slight measuring error. However, the error can be neglected as the transients are very steep.

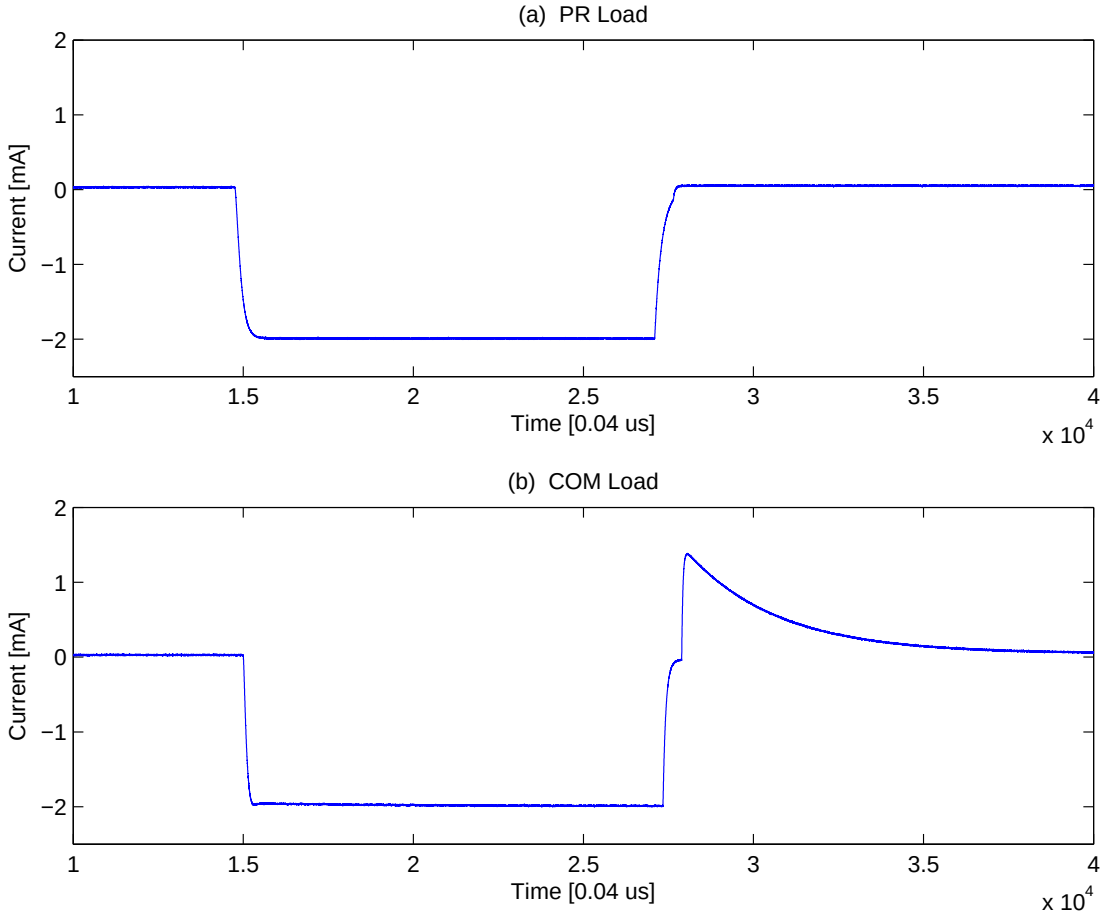

FIGURE 3.5: Data sampled at 3.125 MHz @ 16 bit and captured 1 period. The high sampling rate reveals an interphasic delay between the cathodic and anodic phase, seen as a "dip" at x $\approx$ 2.7.

3.2.2 Req. 1a: Extended m102 MSO analysis

The m102 stimulator was tested on the PR and COM load in Table 3.2, with the same setup as in Figure 3.2 and 3.3. The full range of available stimulating amplitudes were used. A range of capacitances were also used for a fixed stimulating amplitude of 2 mA. The measurements were conducted to answer the following questions:

1. Is the net current dependent on the stimulating (cathodic) amplitude?
2. Is the net current constant for a given stimulating amplitude for varying loads?

The answer to these questions may reveal information about **why** there is a net current (no charge balance), and **how** a similar driving circuit can be designed to be compatible with the electrodes. Recall that a net current results from the absence of charge balance, and that charge balance was found to be an important parameter for tissue stability in Chapter 2, Section 2.4. It is therefore crucial to identify why the net current is deployed, and if it is found essential to the design, how the design can support this feature.

Measurement results

In Figure 3.6 the complete range of stimulation amplitudes was measured over a fixed resistive load. The anodic phase shows a close to natural decaying Resistor-Capacitor (RC) slope with very large time constant, where the amplitude levels have a tendency to be grouped together in 3 separate groups, listed in Table 3.3.

The grouping indicates deviation in the charge balance as the cathodic pulse have constant separating levels, shown in Figure 3.7 (a). Figure 3.7 (b) emphasizes this, as the integral of each stimulating amplitude over the cathodic phase converges into the three levels of charge listed in Table 3.3.

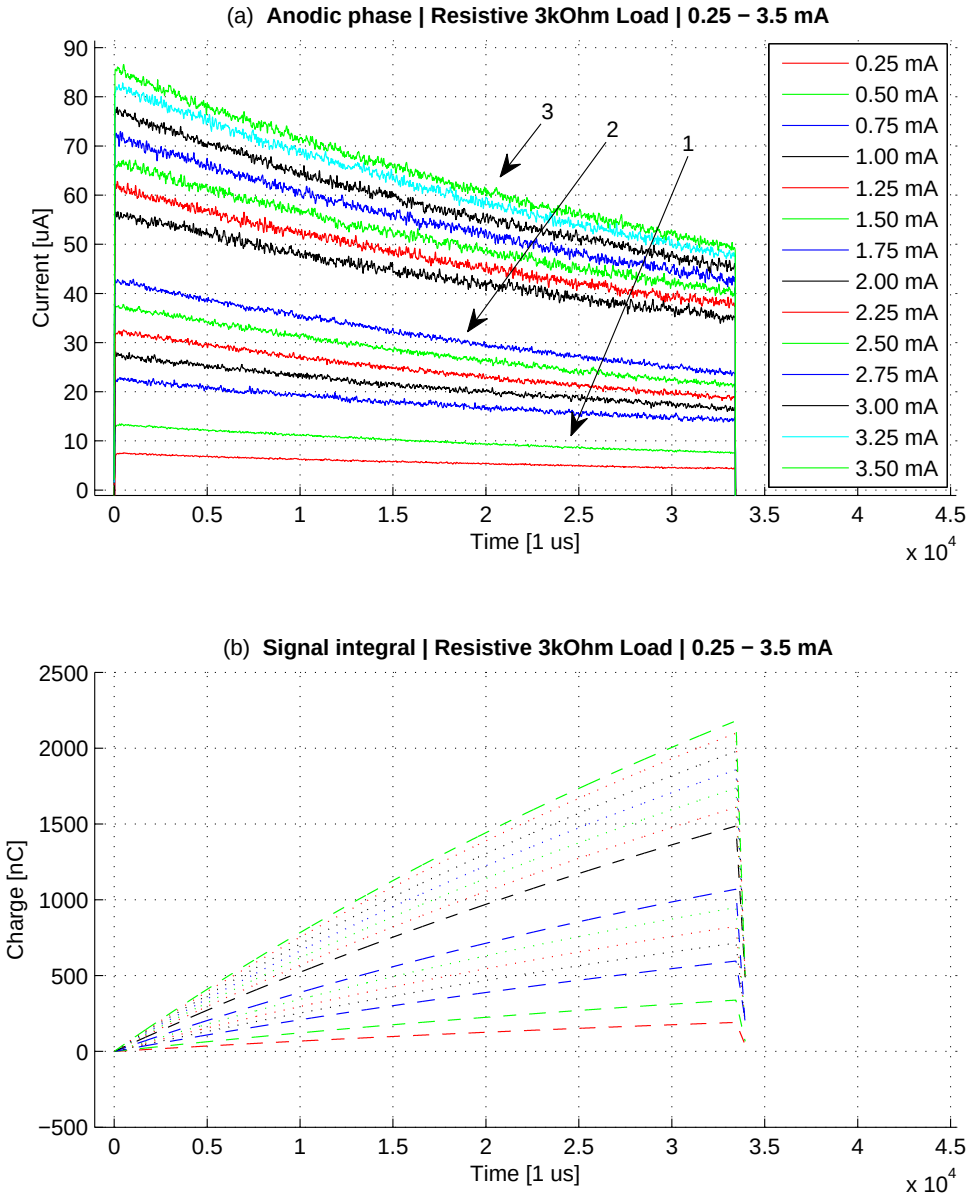

FIGURE 3.6: The anodic current slopes with the corresponding cathodic amplitude in the label. Note that the order of the label entities are inverted with respect to the anodic slopes as they are mapped to the cathodic phase. A closer look at the anodic phase reveals that the anodic current is decaying with a close to exponential slope. The anodic current amplitudes is grouped in three groups, which is unexpected as the corresponding cathodic amplitudes have a constant separation of 0.25 mA.

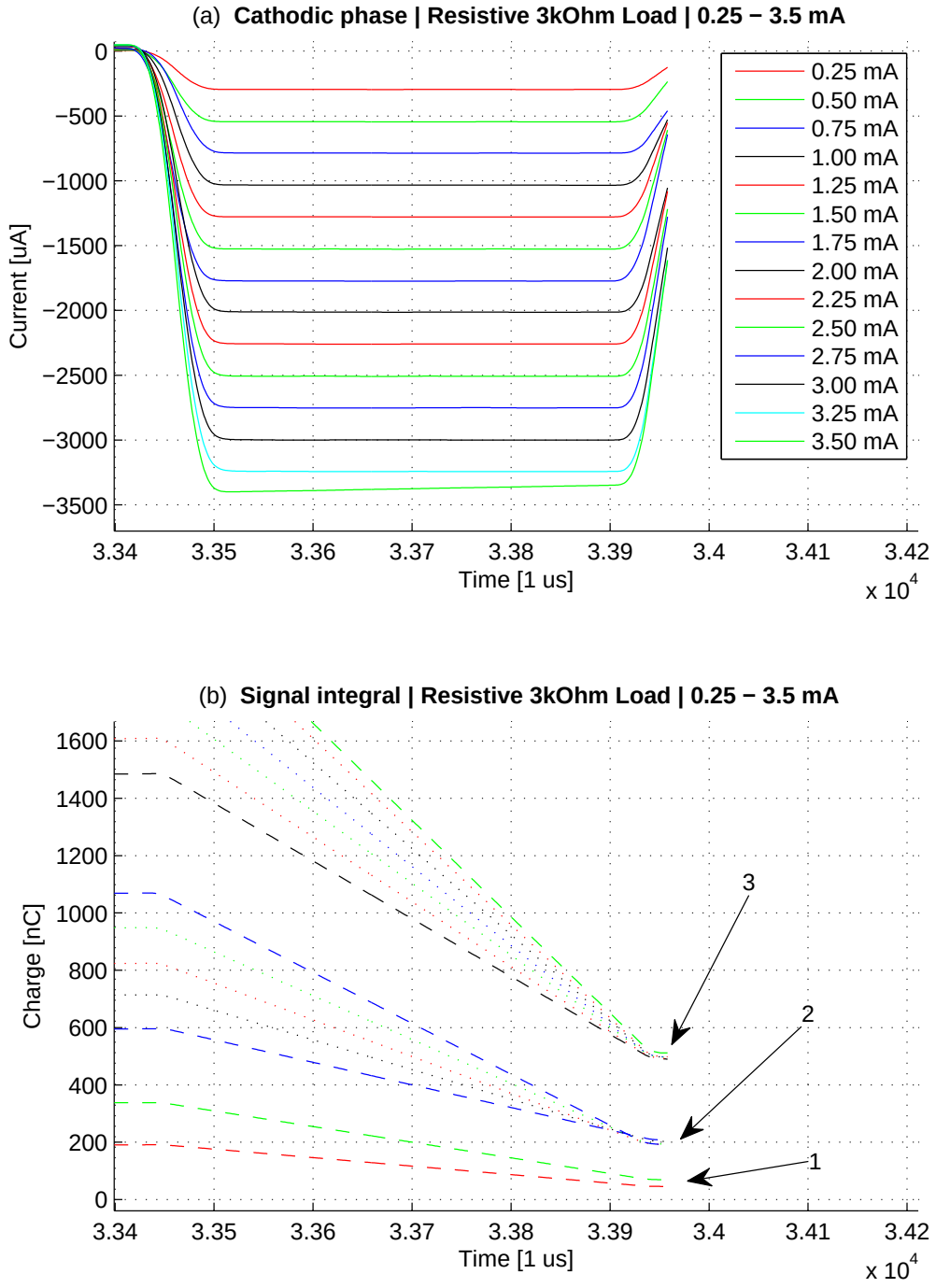

FIGURE 3.7: The cathodic phase for the full range of stimulation amplitudes are shown in (a). Note that the stimulator output is saturated in the 3.5 mA amplitude and does not meet the programmed reference. The corresponding integral is shown in (b). Data is low-pass filtered with a factor of 140 for the MATLAB Savitsky-Golay filter.

This information answers the first question asked: If the net current depends on the cathodic amplitude, as it clearly does, since the charge is not constant for all cathodic amplitudes. The net current, or charge imbalance, actually depends on the cathodic amplitude for three different groups. This observation implies that the net current has a clear purpose in the output, and that the grouping of the charge references is implemented into the stimulator's design.

The data in Table 3.3 shows how the different groups of cathodic amplitude is related to imbalance in charge, resulting in a corresponding net direct current (DC) when divided on the 33 480 µs anodic period.

TABLE 3.3: Data from Figure 3.6/3.7. The stimulator was programmed to output the full range of amplitudes @ 30 Hz. The outputs were found to be grouped in three distinctive groups based on charge imbalance / net DC bias, as well as the anodic amplitude level.

Group	Cathodic amplitude	Charge imbalance	net DC
1	0.25 mA to 0.5 mA	46 nC and 60 nC	1.3 µA and 2 µA
2	0.75 mA to 1.5 mA	192 nC to 207 nC	≈ 6 µA
3	1.75 mA to 3.5 mA	490 nC to 511 nC	≈ 15 µA

Since it is clear that the output should have an imbalance in charge, it is valuable to know exactly how close this imbalance must be to the measured groups. The charge levels are summarized in the bar graphs in Figure 3.8, where the top left graph shows the cathodic amplitude in (a) and the corresponding charge increment in (b). The latter is difficult to analyse, and is therefore enlarged in the top right graph, where each cathodic charge increment is mapped to the lowest and highest amplitude, in 1 to 14 respectively. The amplitudes from 8 to 14 (group 3) are further enlarged in the lower graph to show the differences in total charge (net DC). The largest amplitude in 14 (3.5 mA) appears to stand out from the other amplitudes as it has a larger net charge. This is linked to the smaller cathodic charge increment in the upper right graph, and points towards that the anodic phase does not incorporate deviations in the cathodic phase, thus resulting in a more positive net current for a lack in charge at cathodic phase.

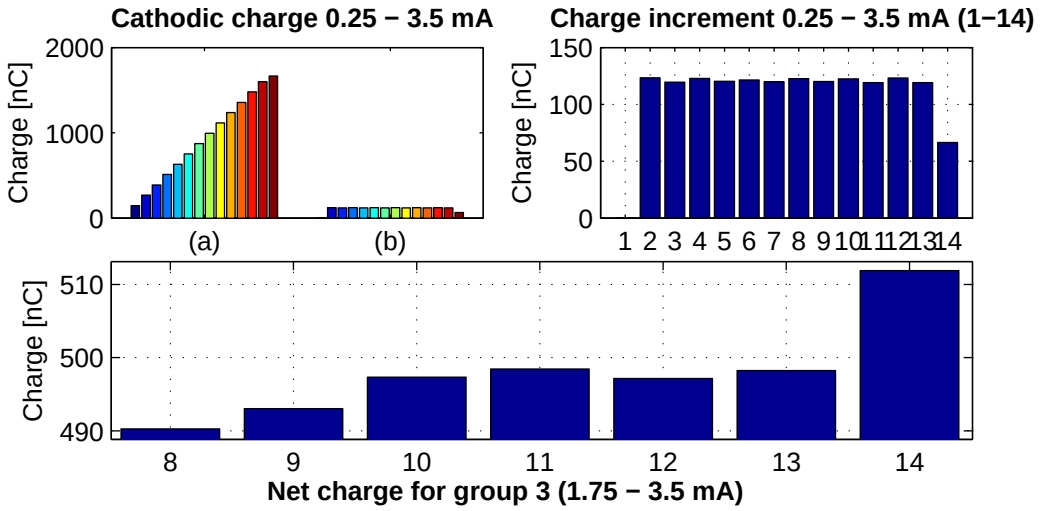

FIGURE 3.8: Data from Figure 3.6/3.7. The charge increment for the 3.5 mA pulse is close to 50% of the mean, which is a result of a saturated output. The charge increment in the right pane is an enlargement of the data (b) in the left pane. The left pane (a) shows the total cathodic charge for the amplitudes from 0.25 mA to 3.5 mA. The lower pane is an enlargement of the charge for amplitudes 8-14.

A closer look at Figure 3.7 (a) for the 3.5 mA amplitude reveals that the cathodic output does not meet reference, which may be due to saturation in the stimulator. This explains why the bar graph in Figure 3.8 shows a distinct difference for the 3.5 mA amplitude (14).

The next step is to measure if the net charge is regulated, i.e. if variance in the load does not influence the net charge. Figure 3.9 (b) shows that the net charge (cathodic + anodic) is held constant. The range of capacitive loads is shown with their anodic discharge in (a). The close to constant cathodic waveform is shown in (c). The measurements prove that there are two control systems: one that controls the amplitude in the cathodic phase, and one that controls the net charge by regulating the anodic amplitude.

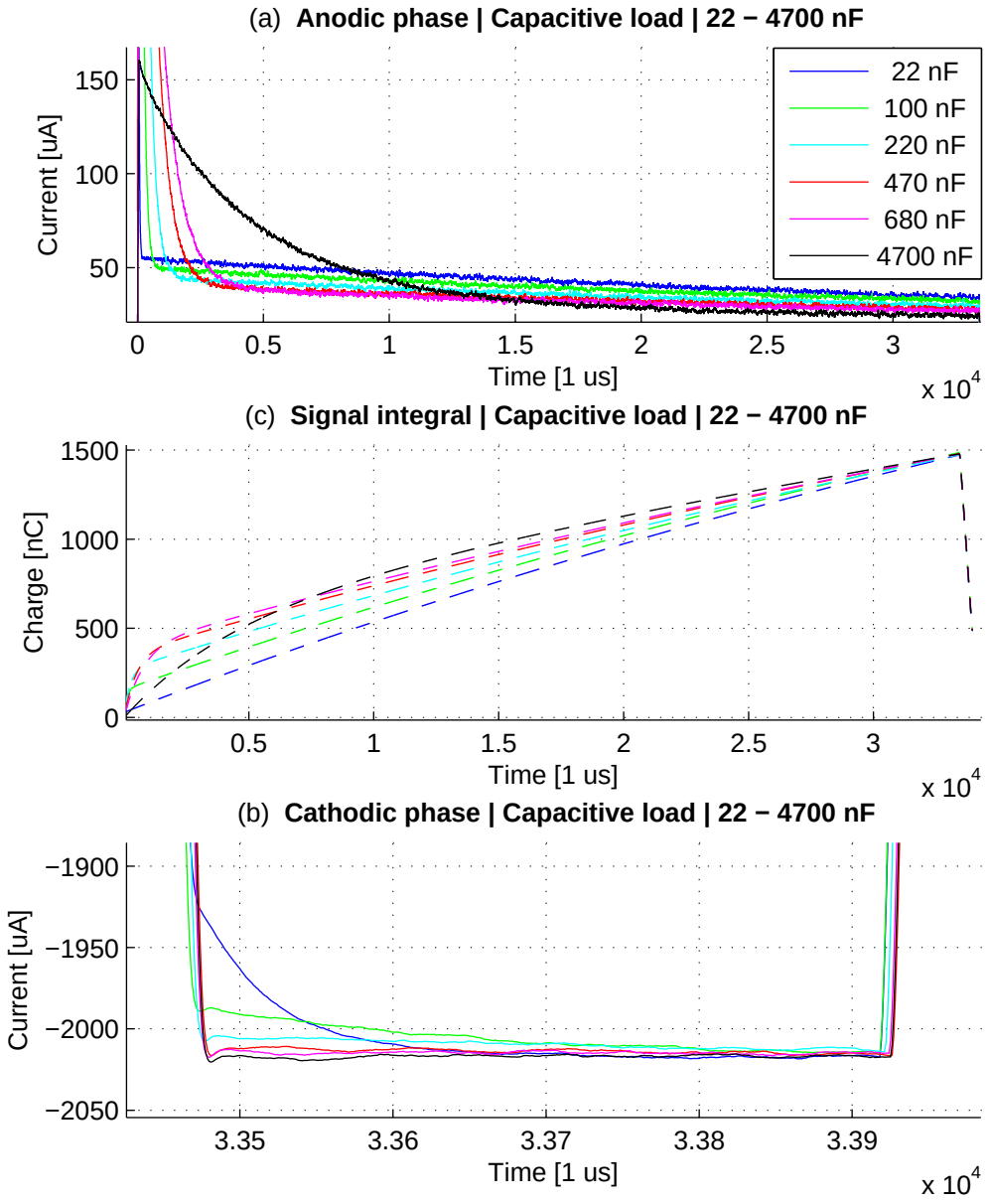

FIGURE 3.9: The stimulator was programmed to output 2 mA @ 30 Hz. The anodic discharge is shown in (a), where the 4700 nF slope clearly shows how the extra charge is compensated for by lowering the anodic amplitude midway in the anodic phase. This is also evident in the corresponding integral lines in (b). The 22 nF load discharges quickly, and is then at an early state held positive with a slope similar to the one found in the case with a pure resistive load (Figure 3.6). In (c) it is shown that the cathodic pulses are consistently rectangular except for the 22 nF load. Data is low-pass filtered with a factor of 39 for the MATLAB Savitsky-Golay filter. Note that the x axis is not synchronized.

Discussion and conclusion

The results answer the asked questions:

1. The net current depends on the stimulating (cathodic) amplitude, but only for three groups. The net current is thus not directly coupled to the stimulating amplitude, indicating some slack for the reference level.

2. For different load impedances both the cathodic amplitude and the net current is constant, indicating that the anodic charge is regulated towards a reference level.

The net current and charge regulation will be discussed separately in the following paragraphs.

Net DC

The net DC is surprising as it defies the general aim in the literature to not have a net DC as to avoid accumulation of electrolysis products. The net current is although small, and may be small enough to stay within a safe level. From the summary of discoveries in Chapter 2:

"A residual DC level of $250\,\mathrm{nA\,mm^{-2}}$ was found to be safe for stimulation in the auditory nerve [8], and $1.16\,\mu\mathrm{A\,mm^{-2}}$ for skeletal muscle stimulation [9]"

The 304 electrode has a conducting surface of $5\,\mathrm{mm^2}$ (Table 3.4), making the highest measured net DC (from Table 3.3) have a density of $3\,\mu\mathrm{A\,mm^{-2}}$. This is above the safe level for skeletal muscle which is believed to have a larger tissue resistance than a peripheral nerve, and the net DC does not seem to be within a safe level for a similar MSO.

TABLE 3.4: The Cyberonics 304 leads specification. The electrode material is given in "Conductor material". Values are taken from the m102 technical information [11]. The geometric surface area (GSA) was given by a clinical engineer at Cyberonics by request. Iridium is known to increase the hardness of the metal structure, as well as to increase the real surface area (RSA) [2]. The latter effect is often utilized by coating the electrodes with a layer of iridium oxide (Petrossians et al. [13]).

Lead model	304
Insulation	Silicone
Resistance	120 Ω to 180 Ω pin to electrode
Conductor material	Platinum Iridium
Conducting surface	$5\,\mathrm{mm}^2$

However, the DC limits in [8] and [9] are from a true biphasic asymmetrical waveform, similar to the waveform in Figure 2.11 (c). The measured m102 MSO waveform is closer to (f) which has the properties of an exhaustive scheme, and the DC limits may therefore not be comparable as they describe two different waveforms and stimulating schemes.

It is hypothesized that the net DC "pre-charges" the electrical double layer as to utilize a high surface charge capacity in the conducting surface. The cathode will in that case be covered with reactant species ready to accept charge as the net DC goes in the anodic direction. The double layer ion gradient will also be charged over time if this is the case, and efficiently elevate the instant capacitance as reactants are placed close to the conducting surface. The DC bias may therefore be a mechanism for creating a larger capacitance at the interface and thus a larger window for safe operation as the impedance is lowered (Eq. 2.18), and furthermore keep the overpotential within the water window for high current densities.

Charge regulation

The control system for the charge regulation is assumed to be matched with the material and technology of the Cyberonics 304 leads, and must therefore be incorporated into the design together with the tolerated deviation in charge / net DC.

To detect the tolerated charge deviation in the cathodic and anodic phase, the cathodic and net charge for the output measured in Figure 3.9 is listed in Table 3.5. The mean cathodic charge was calculated to be 980 nC with a deviance of +/- 6 nC, suggesting that the cathodic charge injection should not vary with more than 12 nC.

TABLE 3.5: The net charge from Figure 3.9. The deviance from mean in the cathodic phase was found to be +/- 6 nC. The net charge results from integration over both phases, and is therefore influenced by the deviations in the cathodic phase. Values are calculated from an averaging of 1 second, capturing 30 pulses.

Load (nF)	Cathodic charge (nC)	Net charge (nC)
22	973	497
100	974	483
220	981	484.5
470	984	488
680	985	486
4700	986	484.5
Mean	980	

To detect the charge margins for the anodic phase, the cathodic deviance was subtracted from the net charge, listed in Table 3.6. The values show that the net charge reference is at 487.5 nC with a charge deviance of 11.5 nC.

It is concluded that the cathodic and anodic phase should be regulated towards 980 nC and 487.5 nC respectively, with a maximum charge deviance of 12 nC for both phases.

TABLE 3.6: Data from Figure 3.9. The deviance from mean in the cathodic charge is subtracted from the net charge from Table 3.5 to obtain the real deviance in anodic charge. The most extreme deviance from mean in the anodic phase was found to be - 11.5 nC. Values are calculated from an averaging of 1 second, capturing 30 pulses.

Load (nF)	Cathodic deviance (nC)	Anodic charge (nC)
22	-7	490
100	-6	476
220	+1	485.5
470	+4	492
680	+5	491
4700	+6	491.5
Mean	980	487.5

Compatible SFE

A principle drawing of a possible realization of the driving circuitry is shown in Figure 3.10. The cathodic pulse is generated when s1 is in top position and s2 closed. When the cathodic phase is over, S2 is opened to initiate the interphasic delay. When s2 is closed and s1 connected to Ia the anodic phase is initiated, where the electrode terminals are "shorted" together using a low output impedance current source.

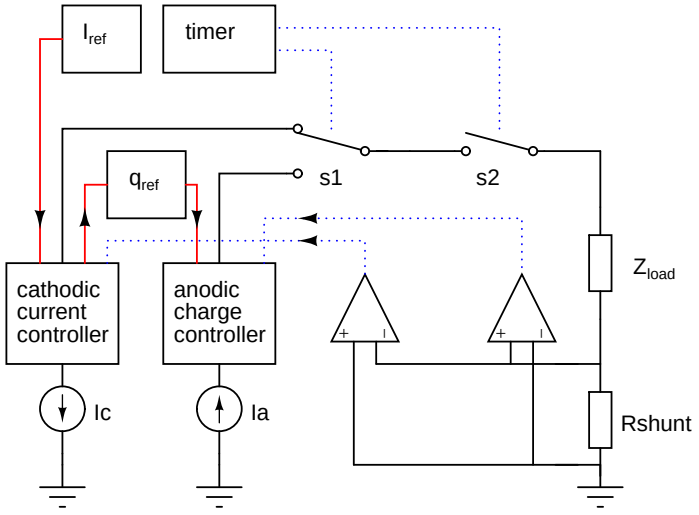

FIGURE 3.10: A suggested driving circuitry for required MSO. The timer toggles the two current sources (s1) and sets the interphasic delay (2). The current reference is loaded into the cathodic current controller, which passes a corresponding set-point for the net charge in the anodic charge controller. Current is measured bi-directionally over *Rshunt* with two inversely coupled amplifiers.

3.2.3 Req. 4b: Power estimation

Requirement 2b demands that the MSO must have voltage compliance to stimulate the load at the highest measured impedance (5 kΩ) for an output at 2 mA. It is therefore a minimum to have 10 V compliance over the load.

It is assumed that this voltage conversion using a DC-DC converter together with the dissipation in the tissue are the main contributors to power loss. The purpose of the following paragraphs is therefore to get a crude picture for the power demand in the stimulating circuitry (SFE) including the tissue to specify requirement 4b.

Power dissipation in tissue

To match with studies using the same ETI model and tissue resistance [8][9][12] as well as measured impedance values from [3], the tissue resistance is assumed to be 3 kΩ in average over the course of implementation (3 months). The end user specification of 2 mA @ 30 Hz is used as a reference for the calculations. From Table 3.7 it is clear that the cathodic stimulation dominates in power consumption, and that the total dissipation is approximately 70 mW h

Power dissipation in converter

In [3] a solution was proposed where the PCB is placed on top of a single coin cell with a lithium / manganese dioxide chemical system, such as the CR2016. These

TABLE 3.7: Estimated loss for a 3 kΩ load pulsed with 2 mA @ 30 Hz at a device duty cycle at 18%. The extra charge which is recovered from the ETI upon shorting in the anodic phase is not included in the calculations. This is a minor increase in performance and is therefore omitted to be on the safe side.

Phase	Cathodic	Anodic
ON_{hours}	5.9	379
Current	2 mA	45 µA
Load	3 kΩ	3 kΩ
Dissipation	70.9 mW h	0.78 mW h

cells have a nominal voltage of 3 V. Taking into account that there is some voltage drop for the SFE, it is assumed that a 3 V to 12 V conversion is necessary.

A switching type of DC-DC boost regulator will be a good candidate for the application as they easily handle the four fold conversion. These regulators, as the Linear Technologies LT8410, LT1617, have an efficiency of about 70-80% for similar applications.

The CR2025 is proposed as an eligible power source as it has approximately 110 mA h available for the application. Studying the CR2025 datasheet in Figure 3.11 it is clear that the voltage for a pulsing application with peak at 6.8 mA drops quickly down to 2.7 V. Swtiching regulators may have peak drain of over 30 mA, and it is assumed that the voltage may early drop down to 2.5 V. Using this voltage together with a 70% efficiency for the converter, the power dissipation for pulsing the tissue is estimated to be approximately 100 mW h or 40 mA h @ 2.5 V, listed in Table 3.8.

TABLE 3.8: Estimated loss for a 3 kΩ load pulsed with 2 mA @ 30 Hz at a device duty cycle at 18%. The loss in efficiency from the voltage conversion calculated with 70% efficiency, and the voltage source is assumed to have an average value of 2.5 V

Dissipation	Tissue	Converter
Watt	≈70 mW h	≈100 mW h
Ampere	-	40 mA h

Maximum current draw

Switching converters are known for quite large current peaks drawn from the source. Too large peak drains from the battery may significantly reduce the available power [14]. An estimate of the maximum peak drain from the CR2025 will therefore be useful when selecting a converter and choosing a suitable capacitor bank at the input stage.

As observed in Figure 3.11 the capacity is reduced when a larger amount of current is drawn from the battery, which is an effect termed the *rate capacity effect* [14].

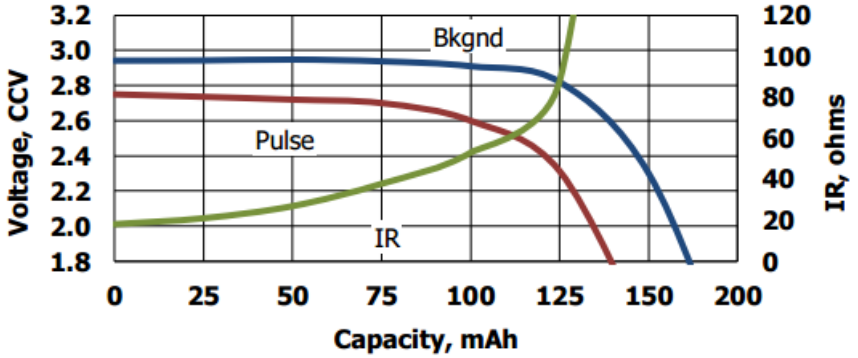

FIGURE 3.11: The Energizer CR2025 is a good candidate for the application as it has more than twice the capacity needed for pulsing the tissue. It also has the right dimensions for an implantable device. The red line in the plot is based on 2 seconds pulsing x 12 times/day with a 400 Ω load, 6.8 mA @ 2.7 V and is therefore a decent estimate for the true capacity for the application. Note that the "Bkgnd" drain is from a continuous 15 kΩ load, i.e. 0.193 mA @ 2.9 V, which is the optimal drain rate for this battery. Data is taken from Energizer CR2025 Datasheet.

This is countered by the *recovery effect*, which is the ability for the battery to recover some capacity for intermittent discharges in pulsing applications. These effects occur in all types of batteries, but their time constants and slope varies among the chemical systems.

In the white paper SWRA349 from Texas Instruments, the capacity of the CR2032 was tested for a pulsing application with high amplitudes. The test case that put most strain on the battery was 30 mA for 1 ms. The report found that 15 mA drain vs 30 mA drain reduced the capacity by 9%.

The CR2025 has the same chemical system, but a significantly smaller capacity than the CR2032. It may therefore have lower limits on maximum power draw. The 30 mA peak draw is proposed as an absolute maximum for the battery to avoid unacceptable rate capacity effects.

3.3 System design specification

This section will give a bottom up approach for defining a modular architecture for the system. The Cyberonics m102 stimulator used for the measurements has

an architecture which is designed for implementation in humans for up to 15 years [11]. An application for animal testing where the period of implementation is considerably less (<6 months) and where the animals are euthanized at the end of the experiment gives more leeway with regards to tissue stability and associated design margins.

Parameters associated with tissue degeneration on a long term perspective is therefore subject to more liberal limits than those measured in the m102. The modular specification will however aim towards the same or more precise limits than measured to be on the safe side. Deviations will be up for discussion if they prove to be unnecessary complicated to implement with respect to the available resources.

3.3.1 Modular architecture and interfaces

The system requirements is completed with the four proposed modules listed below. See Figure 3.12 for a reference.

SFE Stimulating Front End: Stimulating output generator module for both the cathodic and anodic phase of stimulation. This will be the realization of the proposed MSO driver in Figure 3.10. The module will have three submodules, the SFE-C for the cathodic phase, SFE-A for the anodic phase, and SFE-TC for timing and control of the output.

CU Control Unit: Routes communication between HDI, PU, and SFE. Reference level for stimulus amplitude (if programmable) may be loaded from HDI to SFE from this module. Impedance detection from the SFE may be communicated back to the HDI. Critical events from Power Unit may result in the CU to shut down the entire system.

PU Power Unit: Battery monitoring, power rail protection and power saving. Puts entire system into low-power mode via the CU. Enables the system either via an impedance sensing function passed from the SFE, or by a input via the HDI.

HDI Human-Device Interface: Operator feedback on specified events (req. 4(d)i, 4(d)ii) and programming interface and/or device enable function.

The estimated 70 mA h available in the CR2025 battery is distributed at each module's operational time, shown in Table 3.9. This gives a picture on the maximum instant current draw for each module, and is thus a requirement in the design

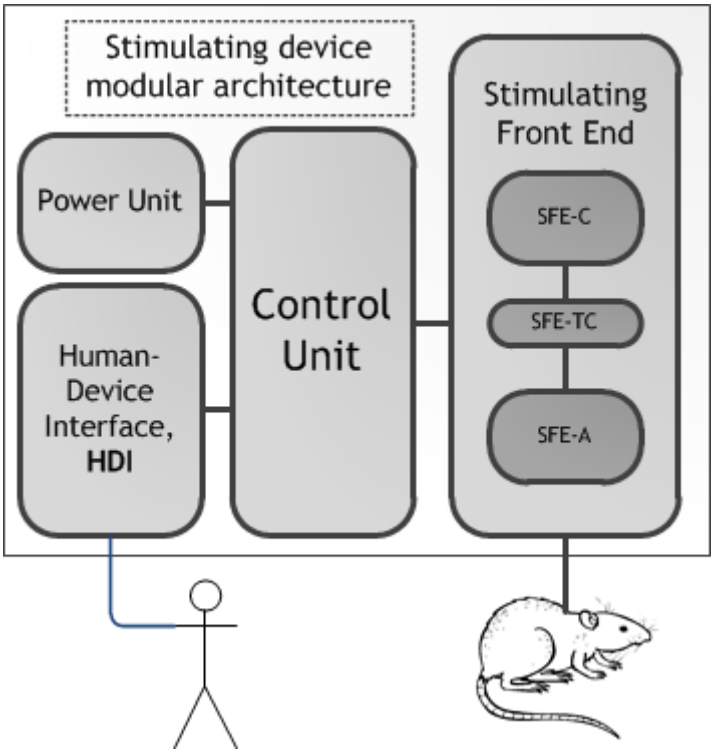

FIGURE 3.12: A simple modular architecture to cover the fundamental requirements of the system. Note that the module interfaces are not specified at this stage.

TABLE 3.9: Estimated allocation of mA h pr module for a cut-off voltage at 2.5 V for the coin cell CR2025. The instant current draw is multiplied with the operation time for the respective module. The SFE-TC module uses the CU module and therefore doesn't have an individual current draw.

MODULE	Active hours	Instant	Total
SFE-C	5.9	1 mA	6 mA h
SFE-TC	384.9	-	-
SFE-A	379	58 µA	22 mA h
CU	2160	18.5 µA	40 mA h
PU	2160	0.46 µA	1 mA h
HID	2160	0.46 µA	1 mA h
TOTAL	-	32.4 µA	70 mA h

of the respective module if the CR2025 is to be used. The power source can be reconsidered if these limits prove to be unrealistic later in the design phase.

Stimulating Front End

The SFE can be divided into three sub-modules shown in Figure 3.12.

The SFE-C module generates the cathodic pulse with the same specification as the output measured in Figure 3.13. The cathodic pulse is constrained by the values in Table 3.10 which were found by analysing the worst case performance of the output seen in Figure 3.13. The pulse is strictly limited on overshoot as this is hypothesized to be a serious issue as the current density then could exceed the "pre-charged" capacitance obtained by the anodic current bias. The error margin is calculated from the deviance in injected charge in Table 3.5.

TABLE 3.10: The limiting parameters for the SFE-C module.

SFE-C	Maximum value
Falling edge	26 µs
Rising edge	20 µs (min IPD)
Ripple	27 µA
Overshoot	47 µA
Error	1.22% (12 nC)
Current usage	1 mA

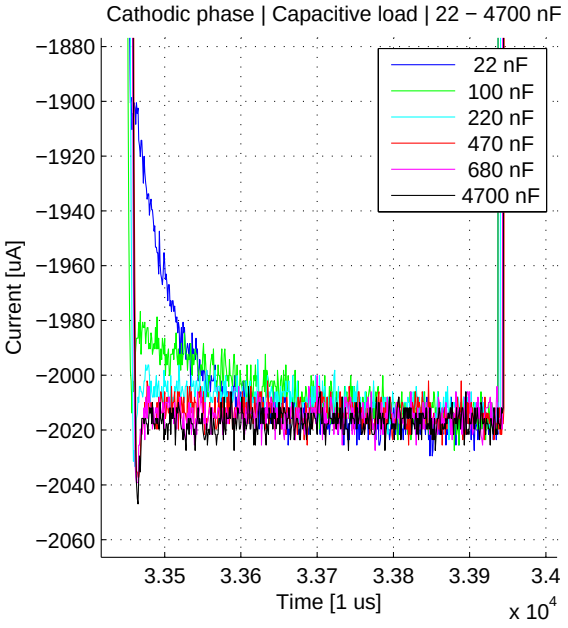

FIGURE 3.13: Cathodic raw data for capacitive loads.

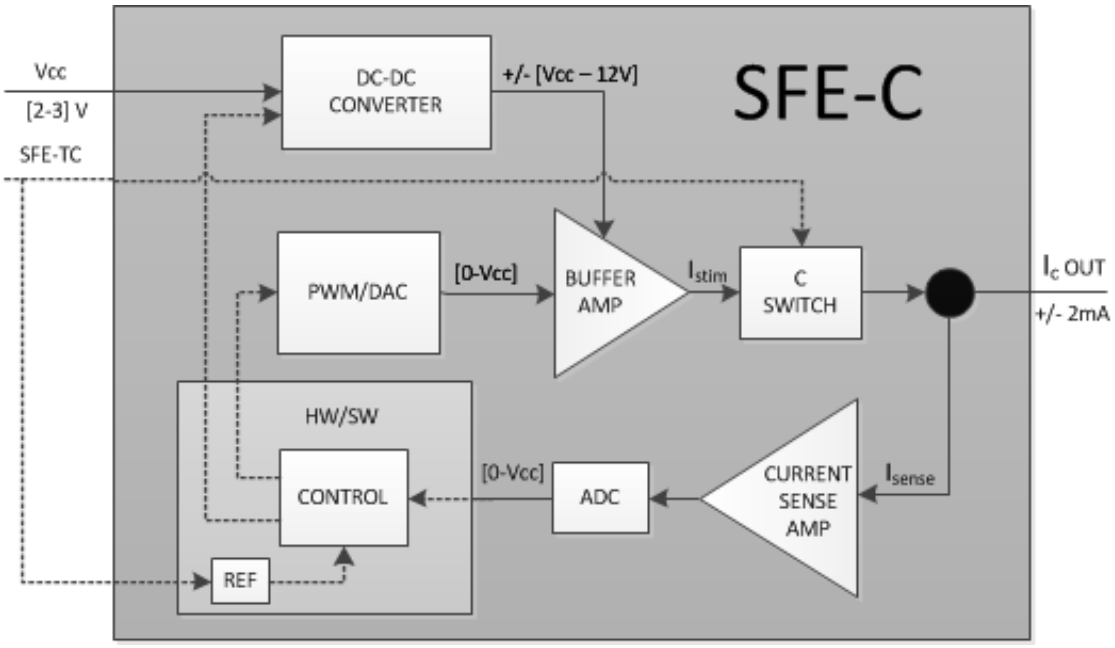

FIGURE 3.14: The modular architecture for the SFE-C module. The dotted lines indicate discrete signals and register data. The specified interface is a 2 V to 3 V input voltage to a +/- 2 mA constant current source. The sign depends on the sign for the SFE-A module, and is inverted with respect to the SFE-A.

The SFE-A module must discharge the accumulated charge from the cathodic phase and regulate the net charge to a set reference level. The SFE-A module operates for a significantly longer period than the SFE-C (67 times longer) and must therefore be very conservative with regards to power consumption. The discharge is an important feature for avoiding ratcheting of the potential, resulting in the over-potential to travel outside the water window.

It is hypothesised that the discharge peaks in Figure 3.15 are limited by the output impedance of the stimulator. This makes sense since high anodic peaks are to be avoided to suppress electrode corrosion (Section 2.3.3).

Measurements and simulation revealed that the output impedances were dynamic in the range 0 kΩ to 4 kΩ. The impedance was zero for the largest capacitance. For the smallest capacitance the peak measured appears lower in amplitude due to aliasing. The error margin is calculated from the deviance in injected charge in Table 3.6.

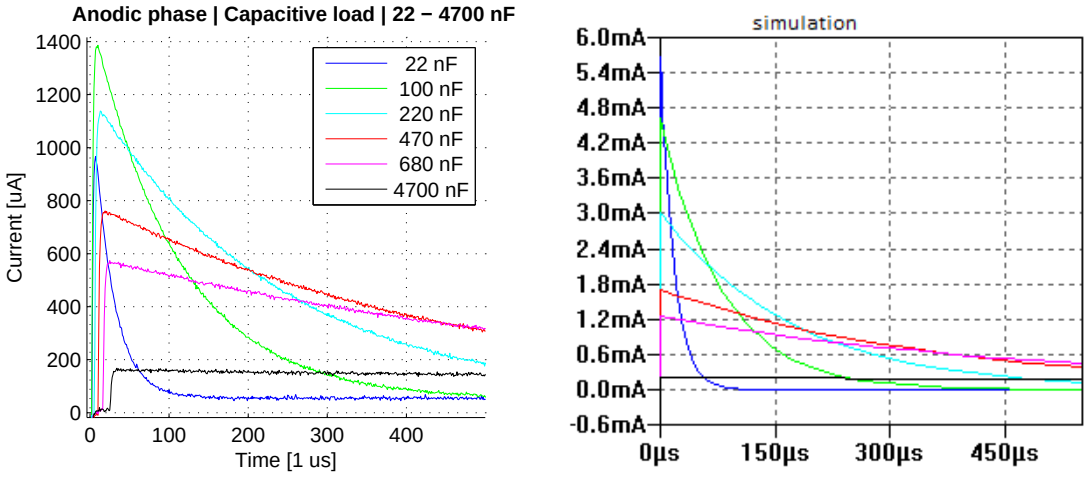

FIGURE 3.15: Measurements (left pane) and simulations (right pane) for the anodic discharge. The simulation is matched with the same colors for each capacitance. The anodic discharge in the simulations is performed with appoximilately zero output impedance (50 Ω, see Appendix A Figure A.3) The simulation shows that the peak value for the largest capacitance is the same (200 µA), while the smaller capacitances clearly is discharged over a larger impedance. The peak for the smallest capacitance appears less than the others due to aliasing in the measurements. Due to the loss of information by the aliasing the maximum peak is unknown. It is clear that the discharge for smaller capacitances is regulated, and matching values for the output impedance was in the range of 0 kΩ to 4 kΩ. The maximum peak for the SFE-A module should be restricted to the highest measured peak to stay on the safe side.

TABLE 3.11: The limiting parameters for the SFE-A module.

SFE-A	Maximum value
Peak amplitude	1.4 mA
Pk-Pk ripple	15 µA
Error margin	2.5% (12 nC)
Output impedance	0 kΩ to 4 kΩ
Current usage	58 µA

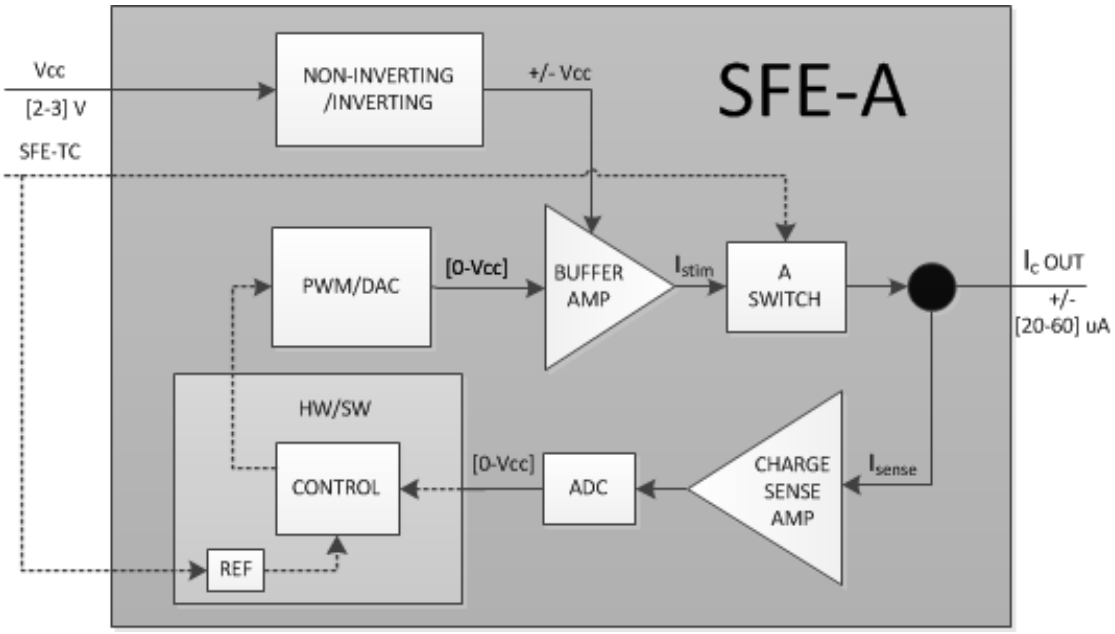

FIGURE 3.16: The modular architecture for the SFE-A module. The dotted lines indicate discrete signals and register data. The specified interface is a 2 V to 3 V input voltage to a +/- 20 µA to 60 µA dynamic current source. The sign depends on the sign for the SFE-C module, and is inverted as compared to the SFE-C. The output value originates from the 2 mA slope in Figure 3.6.

The SFE-TC must control timing of the pulse width, interphase period and interpulse period. The module also loads the reference level, enables, and toggle the switch driver for the SFE-C and SFE-A. The module operates in software and interfaces with the other HW modules via discrete output ports from the MCU.

The module runs the SFE-A in a "sense" state with low output to detect if there is a load connected to the electrodes. The SFE-A is chosen for this task to avoid start-up currents for the converter associated to the SFE-C module for every "sense" check. A sense current at 20 µA in the µs range is believed to not put the tissue at risk. The module informs the CU of this event in software.

TABLE 3.12: The specification for the SFE-TC module. Values from the analysis in Moen [3]

SFE-TC	Specification	Max deviation
Pulse width	500 µs	2 µs
Period	3400 µs	4.4 µs

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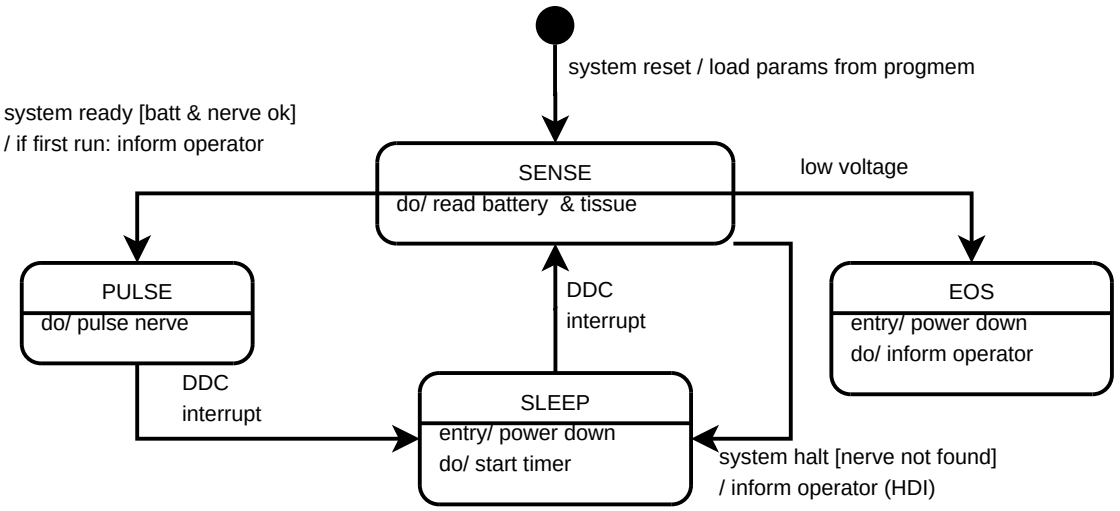


FIGURE 3.17: The modular architecture for the CU module is described using a state diagram where each "module" is a state.

Control Unit

The control unit is necessary to route information between the other modules, and is therefore a module implemented in software. The functionality of the control unit describes the complete system as a state machine, shown in Figure 3.17.

The control unit can be easily implemented using a low power microcontroller (MCU). Power efficient MCU's have a power-down current consumption below 1 µA. By using this value together with calculation of the time in sleep (Table 3.13) the current consumption in active mode is given for 40 mA h available capacity in Table 3.14. The MCU must thus operate in active mode at 57 µA or below.

The Atmel ATtiny 1634 is a good candidate for the CU module. It has a current consumption of 57 µA @ 2.7 V in idle mode (1 MHz). Idle mode is a power saving mode where the CPU is disabled, but peripherals as the ADC and hardware-PWM can still be running. The ATtiny 1634 uses 1.5 µA @ 2.5 V (25 °C) in power-down with the watchdog active, exceeding the limit for the sleep mode by 9 mA h. It should therefore be focused on current consumption in the other modules in the development phase to prevent choosing a larger battery. The candidate MCU is good to have in mind when developing the other modules, as this chip has peripherals or interfaces that interact with the whole system.

TABLE 3.13: Operation time calculated for 3 months with 18% device duty cycle

	Total	Active	Sleep
Hours	2160	385.5	1775.5

TABLE 3.14: The maximum current consumption for the Control Unit. Values are rounded to nearest half.

CU	Instant	Total
Active	57 µA	≈ 22 mA h
Sleep	1 µA	≈ 18 mA h
Both (average)	≈ 18.5 µA	40 mA h

Power Unit

The power unit module is responsible for the well-being of the battery as well as monitoring the minimum allowed voltage at the power rails. This is important as integrated circuits have a minimum operating voltage, and if violated may result in unpredictable behaviour or severe faults. Furthermore, this may lead to failure in the SFE and put the stability of the tissue at risk.

The PU can be implemented by using a single comparator such as the LTC1540 in a low-battery detect circuit, using 1.4 µA active current, shown in Figure 3.18. The current consumption can be further reduced by using the control unit to enable/disable the circuit.

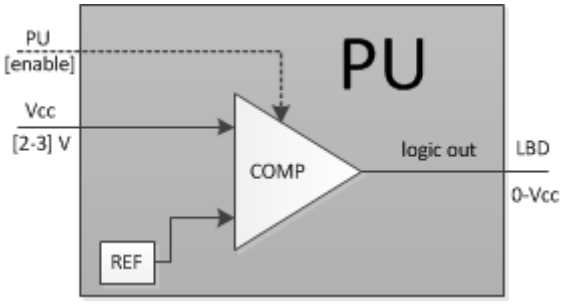


FIGURE 3.18: The modular architecture for the PU module is described using a low power comparator.

Human-Device Interface HDI

simple solution is to inform the operator of required event using one LED, with different blink pattern indicating the various events. The device is then enabled at power-up prior to encapsulation, resulting in no need for the HDI to take any inputs.

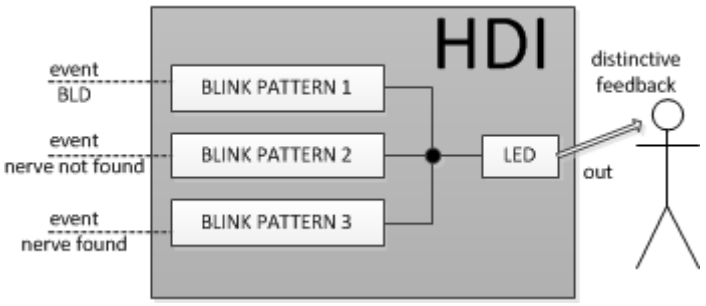


FIGURE 3.19: The modular architecture for the PU module is described using a single LED. The events are software generated, and the LED is powered by a single MCU I/O port. The Battery Low Detect (BLD) is passd from the PU via the CU. The others are passed from the SFE-TC.

Software interfaces

The software interfaces concern the CU and SFE-TC module. The CU passes one of three events to the HDI, loads the control reference to the SFE-TC, and reads from SFE-TC if a load is found by the SFE-A module.

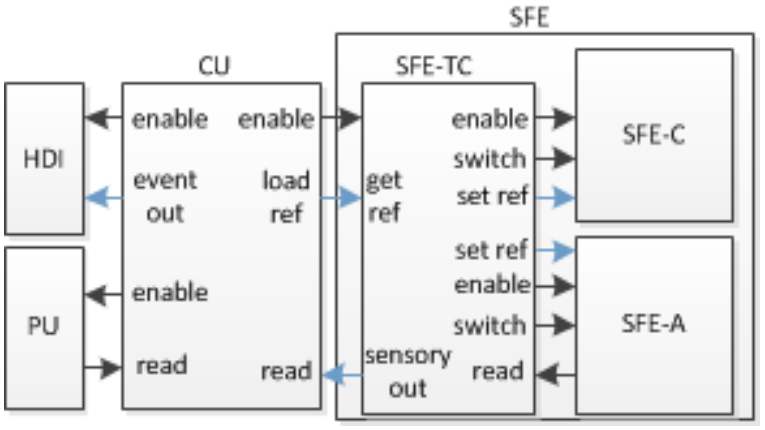


FIGURE 3.20: The software modules are the CU and SFE-TC. Their interfaces are marked in blue.

The SFE-TC passes the reference from the CU to the SFE-C and SFE-A module. The load sensing from the SFE-A is passed to the CU via the SFE-TC.

3.3.2 Traceability matrix

The requirements traceability matrix is based on the system-level requirements from the end user, shown in Table 3.15.

TABLE 3.15: The system traceability matrix for use when verifying and backwards tracing the functionality for the HW and SW modules.

Req. ID	System requirement	Design specification	Test requirement	Test ID
1a	Compatible with 304 leads	SFE	SFE-C ref. 1.22% max. dev. SFE-A ref. 2.5% max. dev. Sufficient discharge: no measured ratcheting of potential. SFE-TC period 34ms / IPD 20us	T-1
2a	2mA @ 30Hz - 500us PW	SFE-C	Falling edge max 26us. Rising edge max 20us. Max ripple 27uA. Max overshoot 47uA	T-2
2b	5kO load	SFE	2mA cathodic amplitude measured with a 5kO resistive load	T-3
4a	3 months life	Eligible power source	Battery capacity within measured device current consumption, which must be measured for active and sleep mode and multiplied with DDC values.	T-4
4c	DDC @ 18%	CU / SFE-TC	Use a timer and verify that the ouput is active for 1 min and off for 5 min.	T-5
4di	Sense load	SFE-A	Device feedback when load connected to test station using the 304 leads.	T-6
4dii	Alert EoS	PU	Device feedback when the prototype is powered by a variable voltage source where the voltage is lowered under a defined cut-off level.	T-7

Chapter 4

System design and implementation

This chapter describes the process, method and results of the system design. The development was based on the modular structure, prioritizing each module by their importance. The core module is the SFE-C which the rest of the modules was built around in the shell structure shown in Figure 4.1.

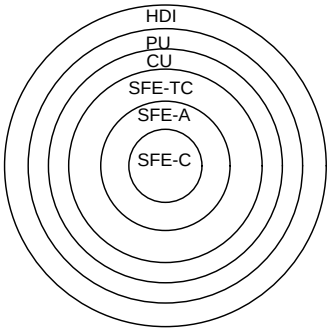


FIGURE 4.1: The importance of the modules based on their dependence.

Three possible solutions to the stimulating front end was evaluated prior to the design phase, given in Section (4.2). The focus was on developing a design which is configurable beyond the end user specifications, e.g. to have options for a range of stimulation parameters via simple adjustments to HW or SW.

4.1 Design process

The primary goal of the design phase was to complete all the modules within their specification, i.e. *modular features and overall current consumption*, and secondary use components available in small packages to obtain a design that later can be miniaturized.

The design of the SFE-C and SFE-A is the main focus in the design as the other modules are relatively trivial to develop. Both of the modules were tested with the switch and switch driver first, and control second, using the load models shown in Figure 4.2. The DC-DC converter associated to the SFE-C module was tested preliminary to each design. To save time, most of the components were selected from Linear Technologies and simulated with LtSPICE. Components from other vendors were prototyped and tested immediately.

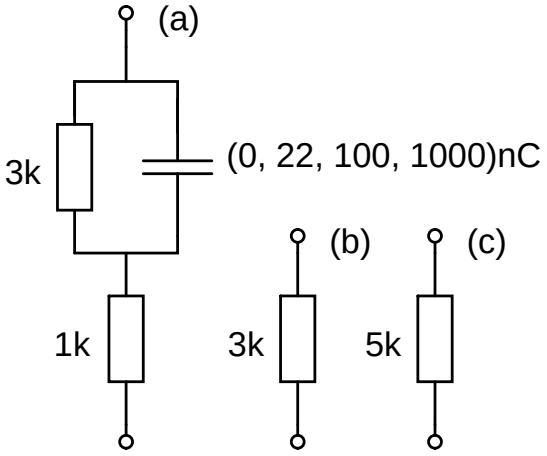


FIGURE 4.2: Load (a) was used for testing the regulation, (b) and (c) for driver testing and calculating power consumption.

Three different overall solutions to the SFE module are proposed in the following section (4.2), with associated pros and cons to each solution. Extensive effort was put into the first solution, but was discarded due to complications for the SFE-A module. The work is still presented in Section 4.3 as some of the findings are used in Section 4.4 where the design was completed based on the second solution, and prototyped in Section 4.5.

4.2 SFE design alternatives

4.2.1 Dual supply: Inverting DC-DC converter

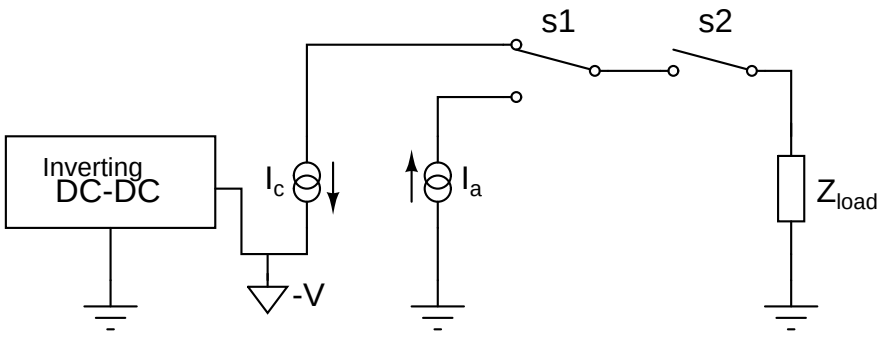


FIGURE 4.3: A principle circuit of the dual supply solution with inverting DC-DC converter. A SPDT (Single Pole Double Throw) switch (s1) selects the cathodic and anodic current source (I_c and I_a respectively). A SPST (Single Pole Single Throw) switch (s2) decouples the load from the circuit for the interphasic delay.

Pros

- Simple design
- Small overall footprint
- More options for op-amp design (when converter is active)

Cons

- Negative supply switch driver
- Less inverting converter options on the market

This circuit is based on a buck-boost DC-to-DC converter which generates a negative rail for the cathodic driver. This design is simple, as it allows the load to always be connected to ground, i.e. tying the anode directly to ground. The solution demands few components which should result in a small overall footprint.

Note that switch s1 must take the form as a Single Pole Double Throw (SPDT) switch, while s2 is a Single Pole Single Throw (SPST). These switches can be realized using low on-resistance and fast MOSFET transistors biased in the correct operating mode. Challenges for this design may be a limited selection of inverting (buck-boost) converters as well as switch drivers for the negative rail.

4.2.2 Single supply: Switching poles

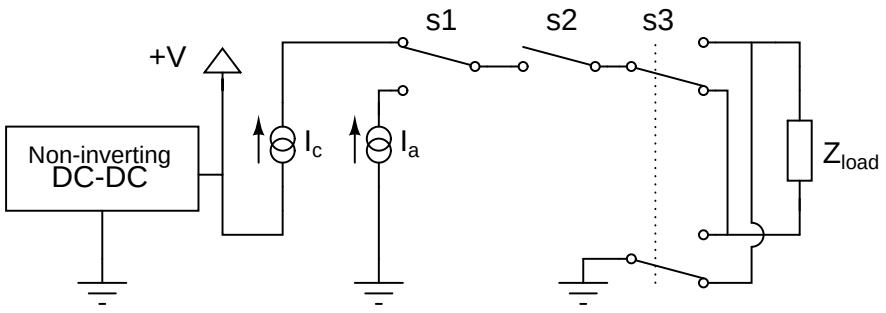


FIGURE 4.4: A principle circuit of the single supply solution with non-inverting DC-DC converter. Switch s1 changes between the cathodic and anodic current source (I_c and I_a respectively). Switch s2 decouples the load from the circuit for the interphasic delay, and switch s3 switches the electrode polarity.

Pros

- Positive supply switch drivers
- More converter options

Cons

- 3x SPDT switches + 1x SPST
- Complicated circuitry
- Larger footprint

This circuit is based on a regular boost converter which is available at most vendors. This is beneficial, as it is easier to find a component which is closer to optimal for this application. The switch drivers may also be simpler as all rails are positive, but on the other hand there must be quite a few of them which takes up valuable footprint.

The switch s3 is a DPDT (Double Pole Double Throw) configuration which can be made up by two SPDT switches sharing the same control signal

4.2.3 Single supply: Virtual ground

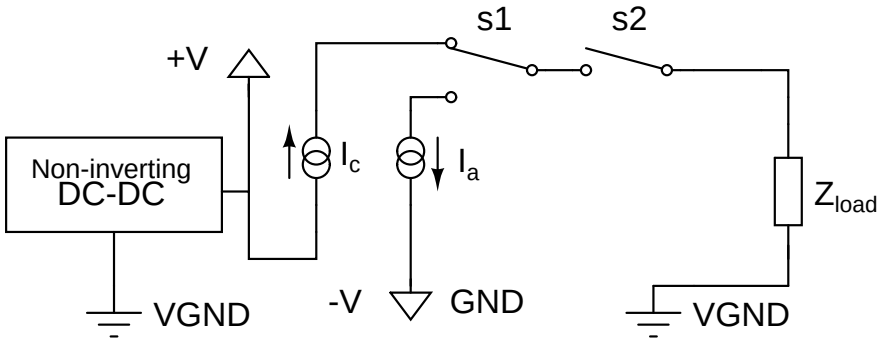


FIGURE 4.5: A principle circuit of the virtual ground dual supply solution with non-inverting DC-DC converter. Switch s1 changes between the cathodic and anodic current source (I_c and I_a respectively). Switch s2 decouples the load from the circuit for the interphasic delay. Both the cathodic current source and the load must be placed on the virtual ground rail, where a stability issue arises if these two have uneven potential (current will flow even when the current source is inactive). The anodic current source is driven by the virtual ground potential, and sinks current to the real ground which is relatively negative.

Pros

- More options for op-amp design (when virtual ground is active)
- More converter options

Cons

- Virtual ground stability
- Complicated circuitry
- Larger footprint

This circuit has the same advantage as the previous with more options for boost converters. It also has the advantage similar to the first circuit with a dual supply for driving op-amps. The challenge is however to have a stable low-power virtual ground with small footprint. Also, the switch s2 becomes more complicated as both electrode terminals must have the same potential when not pulsing the load (e.g. in the interphasic delay). Virtual ground must therefore be terminated whenever the other electrode terminal is inactive to avoid small leakage currents into the tissue.

4.3 Simulation: Inverting DC-DC design

The design based on an inverting DC-DC converter seemed at first to be the most promising solution with respect to simplicity and overall footprint, and was therefore the design that was aimed for. The LT1617-1 buck-boost converter from Linear Technologies was found to be the most suitable component for the application, as it had Simulation Program with Integrated Circuit Emphasis (SPICE) simulation code integrated in the software LtSPICE and met all the requirements from the modular specification. The converter is available in a 5-lead Small Outline Transistor (SOT-23) package which is suitable for both prototyping and the final design.

4.3.1 SFE-C

Converter

The performance of the converter was tested first. The simulation results in Figure 4.6 shows that the start-up current draw from the battery is 45 mA, which is above the 30 mA limit suggested in Section 3.2.3, which would strain the battery if the converter is enabled prior to each cathodic pulse. A larger input capacitor (C3) bank would reduce the peak current, but the total value would have to be 50 µF or larger, which takes up significant footprint. The "standby" current draw was found to be minimized by reducing the number of switch initiations when the converter is disconnected from the load.

The standby current was reduced to 42 µA including the converter's quiescent current which leaves no more than 16 µA available for the SFE-A module (Table 3.9). The LT1617 converter operates down to an input voltage at 1 V, which may add an extra 10 mA h of battery capacity if the other components can handle such a low voltage as well. The optimization method and result is given in Appendix A Section A.

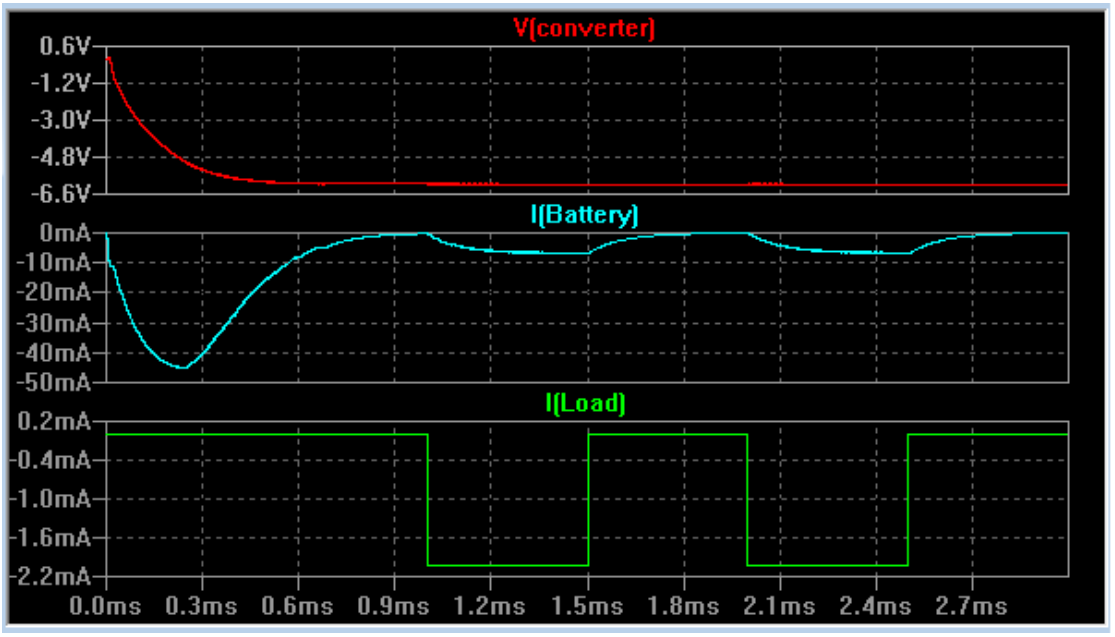


FIGURE 4.6: The inrush battery drain lasted 0.6 ms, and peak draw per pulse was 8 mA for a 3 kΩ load. When testing with 5 kΩ load (−10 V). The efficiency was 87.1% @ 3 kΩ and 87.9% @ 5 kΩ

The LT1617 converter for the inverting solution was concluded to be a feasible component, either running for each cathodic pulse with a large capacitor bank, or by running the whole pulse period (cathodic+anodic) by reducing the standby current. The converter should have several voltage levels for the varying load. This will save unnecessary power loss in switching the load as less overhead voltage drops over the pass element.

Switch and driver

An nMOS transistor was chosen as a pass element due to the low Rds(on) resistance. The Siliconix Si1555DL transistor in the simluation has Rds(on) @ 500 mΩ and has a gate charge as low as 1 nC, resulting in low power loss when switching.

The driver must keep V_{g1} above $V_{th} + V_{neg}$ to open M1, and below to close. Controlling the gate directly with the MCU's I/O pins is thus not possible without breaking the MCU.

The proposed switch driver is shown in Figure 4.7 in the schematics. A pMOS transistor (M2) with its source tied to the positive supply driven by low input at

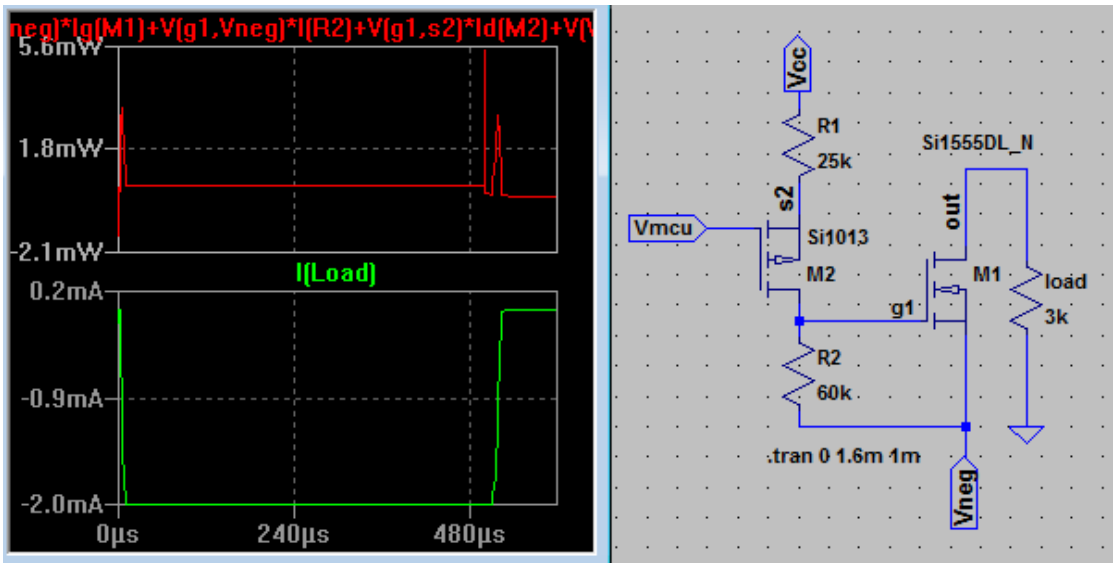


FIGURE 4.7: The driving circuitry for the cathodic switch (s1c). The average power dissipation was 400 µW for all consuming components, shown in the upper pane in red. The falling edge was 8 µs and rising 15 µs for worst case performance, which is within the modular specification. Note that LtSPICE puts a capital letter first on components in the plot.

the gate Vmcu will then enable the transistor M2 and then set transistor M1 gate (g1) to the voltage division between R1 and R2. The performance of the switch is within specification with regards to falling/rising edges and power consumption.

Regulation and power consumption

The regulation of the cathodic phase must be fast and accurate. Analog regulation can be made very fast as it is not bandwidth limited. The problem with analog regulation is the need for calibration with voltage and temperature deviations.

A current mirror was tested first. Cascode current mirrors can achieve output impedances at several hundred mega ohms, and will therefore be close to constant over a varying load with little need for calibration. The problem is that the mirror ground is the negative supply, which varies depending on the load. The reference current will therefore also vary with the negative rail, resulting in unpredictable regulation. A buffered voltage reference would solve this problem, but the solution was discarded as the overall footprint became too large.

A simple analog solution is possible by regulating the V_{g1} gate voltage the the M1 transistor directly, shown in Figure 4.8. The bias resistor R4 sets the Q1's base current in the correct operating range. The base current is then amplified over emitter and collector, effectively sinking current from V_{g1} .

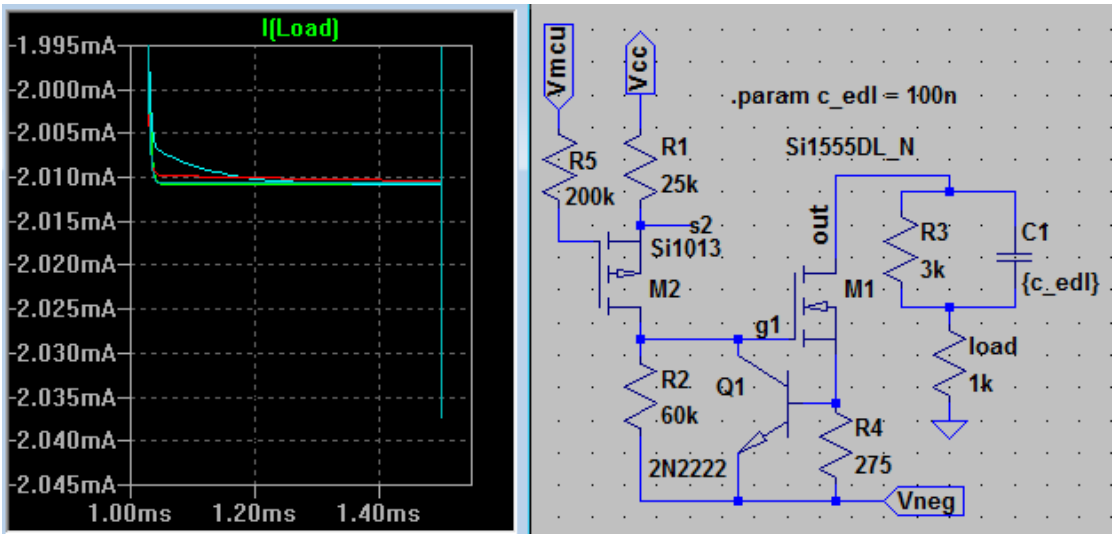


FIGURE 4.8: Acceptable regulation performance. The overshoot is less than the 47 µA limit. The power dissipation is dominated by M1 and M2, adding to an average at 1 mW in total. Steeper edges would benefit switching loss as less time is spent in the transistor's ohmic range, but this severely affects the overshoot due to the parasitic body capacitance in the nMOS.

The bias resistor R4 dampens the discharge rate over M1 as well, resulting in less gate access from the parasitic capacitances. This is often a serious problem for switching applications using MOSFET's, as rapid voltage transients applied to the drain goes via the body-drain capacitance C_{bd} and then trough the gate-body capacitance C_{gb} to access the gate, thus amplifying the voltage transient trough the transistor.

The disadvantage with this solution is power dissipation in R4, as well as the need for calibration due to the varying Vcc supply. This can however be solved by either replacing the Vcc rail with a constant voltage source, or a secondary digital regulation applied to the Vmcu port (PWM/DAC). The size of the bias resistor adds 9% more resistance to the load , equal to 3.6 mA h additional current draw, which is within the allocated current limit to this module (Table 3.9).

SFE-C Evaluation

TABLE 4.1: The performance of the SFE-C module is well within the required limits.

SFE-C	Limit	Performance
Falling edge	26 µs	15 µs
Rising edge	20 µs (min IPD)	8 µs
Ripple	27 µA	10 µA
Overshoot	47 µA	40 µA
Error	2.6%	≈ 0.1%
Current	1 mA	0.96 mA

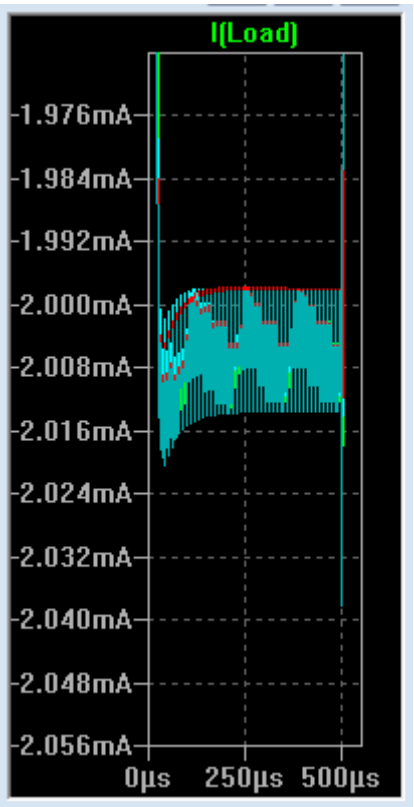


FIGURE 4.9: Cathodic pulse simulated with a 100khz PWM signal, 15% duty cycle via a first order LP-filter.

The SFE-C module performs within the specification. A PWM regulated output is shown in Figure 4.9 confirming that a digital control system can be added for better regulation. The instant current consumption for each pulse adds up to 0.96 mA which is within the 1 mA limit. The injected charge error for the different load capacitances were too low to be measured accurately in LtSPICE, indicating that it at least is far within the required limits. The main contributor to any deviance will then be from the PWM regulation.

The SFE-C regulative design does not have feedback to the converter at this stage. A non-inverting operational amplifier (op-amp) must be added as well as a shunt resistor to complete the module specification. The negative rail introduces some variations to the common mode voltage for such measurements. The op-amp

design was postponed to a later phase, and the SFE-A module was evaluated in beforehand.

4.3.2 SFE-A

The SFE-A can be driven directly from the battery voltage as the maximum required output is 60 µA, which for a 5 kΩ load results in 300 mV compliance.

Switch and driver

The main challenge for the anodic switch driver is to keep the switch closed while the connected rail goes negative in the cathodic phase.

One possible solution is shown in Figure 4.10 where the pass element is a pMOS transistor with the source connected to the positive rail, and drain connected to the negative rail. This setup works because the drain will never go more positive than the source, and thus won't put the body diode in forward-bias (which would be the case for an nMOS transistor).

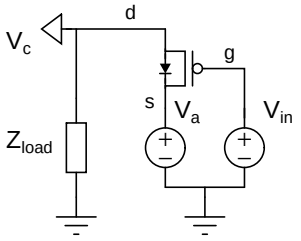


FIGURE 4.10: A pMOS as pass element for the SFE-A module. V_c is the negative rail, which is connected directly to the drain.

The problem with this solution is that the cathodic pulse is directly connected to the transistor drain. The fast cathodic switching will force significant current when accessing the gate via the substrate body capacitances.

Replacing the pMOS with a pBJT eliminates this problem as they have significantly less parasitic capacitances. Simulation with the same setup resulted in peaks in the nA range. The problem with a BJT is that it does not operate as an ideal switch for the anodic discharge. For this reason the BJT is infeasible for the application. It was later found that the Phillips BSS84 pDMOS transistor proved

to be resistant for the rapid voltage change, and simulations gave a maximum peak of 12 µA which was considered safe for the application.

Regulation and power consumption

The regulation for the SFE-A module includes two steps: 1. discharge the tissue capacitance with peak regulation, and 2. output current in the µA range, controlled towards a charge reference. The overlap between these two stages can be initiated by the controller.

A natural discharge is easily realized by tying the gate to ground, but a serious problem arises when doing this. The voltage V_a in in Figure 4.10 must be above threshold to hold the pMOS in the right operating range, which for this transistor is 2.1 V. This will add too much voltage over the load, which only needs 300 mV for maximum current.

The pMOS must discharge the capacitance with a source at maximum 300 mV, eliminating the possibility of a pMOS after all, since they at the lowest have threshold voltages right below 1 V. Considering that nMOS is not an option either, the required functionality for the SFE-A module was not accomplished in this circuit solution.

4.3.3 Conclusion

The shorting function of the SFE-A module was not accomplished. The design based on the inverting poles (Figure 4.4) would eliminate the problem with the pMOS as an nMOS could be used instead.

4.4 Simulation: Switching pole design

The Vishay DG4051A 3x SPDT multiplexer was found to be a good solution for the design as it is available in a small 1.8 x 2.6 mm Mini Quad Flat No-leads (mQFN) package. This design eliminates the demand for switch drivers and may reduce the overall footprint considerably.

As with the first design, the boost converter was tested first. The LT8410 boost converter was found to be a very good match for the application.

4.4.1 SFE-C

The LT8410 outperforms the LT1617 by having a lower footprint (2x2 mm DFN), much lower current limit (25 mA), and draws only 8.5 µA quiescent current. The efficiency of the two converters is close to identical in simulation, Figure 4.11.

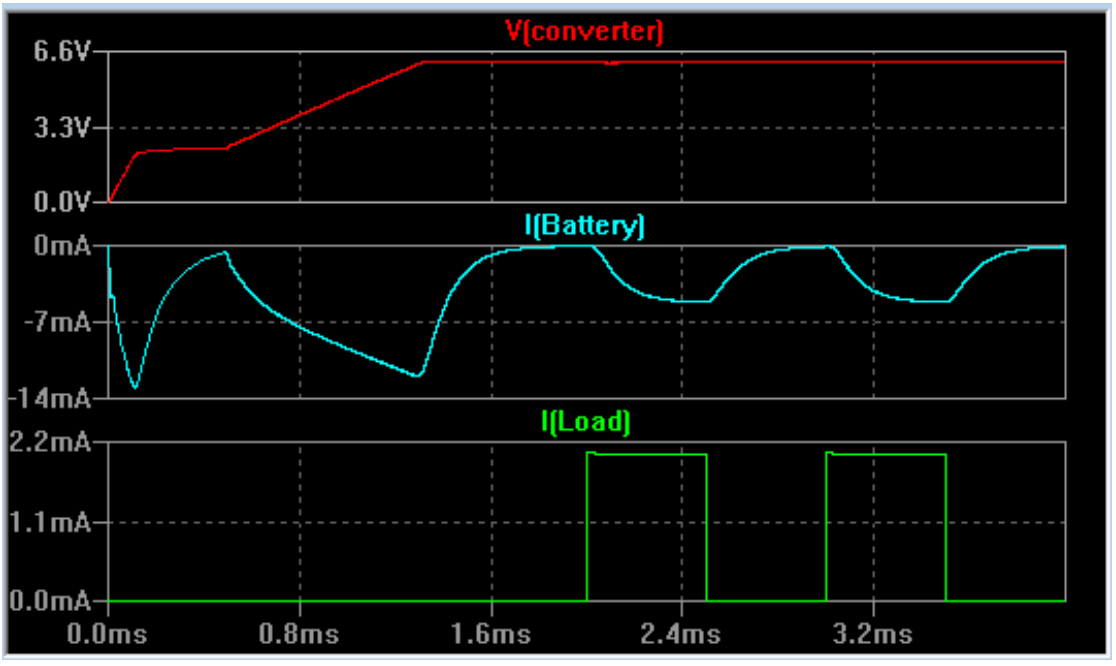


FIGURE 4.11: The inrush battery drain lasted 1.6 ms with peak draw at 14 mA, and peak draw per pulse was 6 mA for a 3 kΩ load. When testing with 5 kΩ load (10.5 V) the inrush battery drain lasted 2 ms with peak draw at 10.2 mA, and peak draw per pulse was 11 mA. The efficiency was 86.6% @ 3 kΩ and 86.5% @ 5 kΩ.

The disadvantage of the LT8410 that the driving voltage can be a minimum of 2.5 V, and the converter can therefore not utilize the extra 10 mA h. The start-up is also 1 mA longer. The peak current at start up and pulsing is on the other hand at a maximum of only 50% of the proposed 30 mA limit, which should result in significant savings in battery capacity. By using the same optimization as with the LT1617, the LT8410 current draw was reduced to 25 µA in standby mode, including the quiescent current.

Switch and driver

The TSSOP16 version of the DG4051A chip were soldered on to a prototyping PCB and tested together with a 12 V source and control signal from an AVR microcontroller.

The measured voltage over the load shows that the switch performs well within specification, and was measured to have rising and falling edges below 100 ns, shown in Figure 4.12. The converter output was connected to the MUX supply to protect the MUX pins.

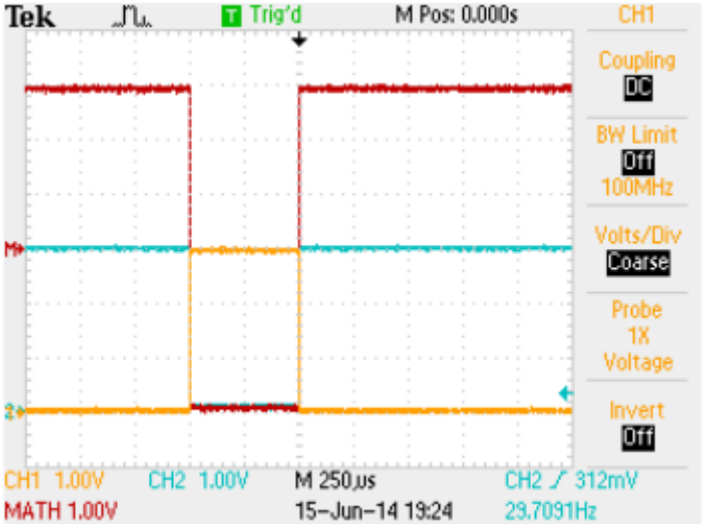


FIGURE 4.12: The Vishay DG4051A TSSOP16 version was mounted to a proto board with a configuration emulating switch s3 in Figure 4.3. The plot shows the measured voltage over a resistive load with falling and rising edges below 100 ns.

Regulation and power consumption

With the positive supply it was tempting to give the current mirror a new try. The BJT transistor BCV61 from NPX comes in a thermally coupled dual SOT143 package, ideal for constructing current mirrors. The SPICE simulation code provided by NPX was loaded into LtSPICE. A cascode current mirror in an improved Wilson configuration was found to be necessary to achieve sufficient output impedance for stable regulation, shown in schematics in Figure 4.13. The results was however not satisfactory due to a 500 µA overshoot in the initial cathodic phase, shown in the plot in Figure 4.13. Testing with a prototype circuit revealed the same results as in the simulation, and the BJT current mirror solution was therefore discarded.

Direct regulation using a controlled voltage to the feedback pin of the boost converter was also tested. Simulations with step responses revealed that the converter did not have sufficiently fast response to regulate the narrow 500 µs cathodic pulse.

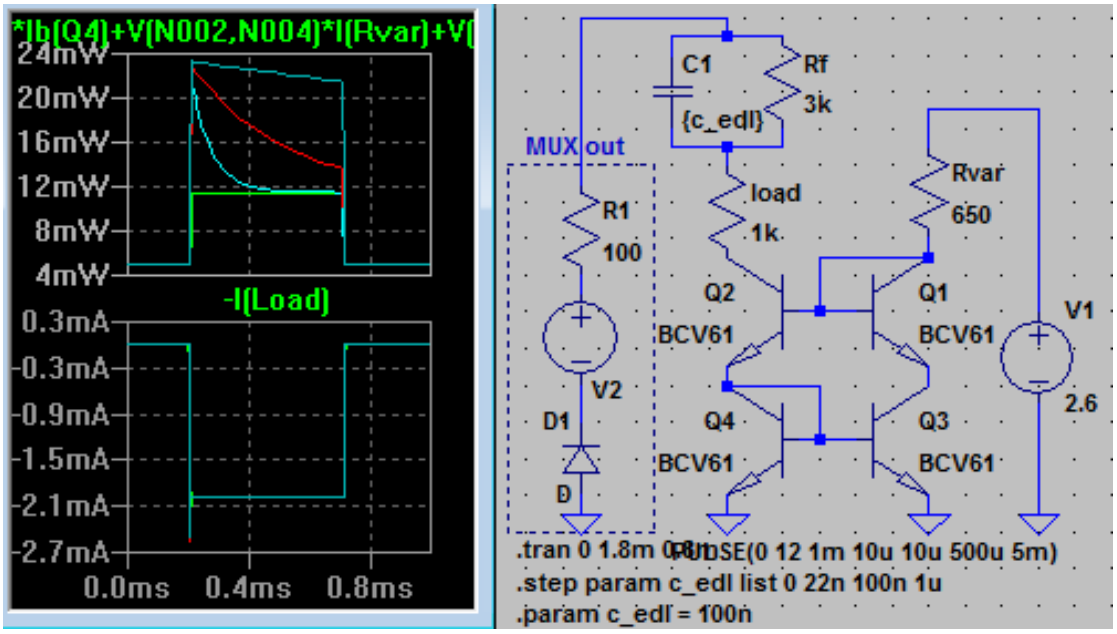


FIGURE 4.13: The improved Wilson current mirror had very robust regulation except a 500 µs overshoot following the falling edge, shown in the lower pane to the left. The MUX output is at 12 V, which is excess for the load requirements, especially for higher capacitances. This is shown in the upper pane to the left, where the 22 nF capacitance is shown in light blue, and the 100 nF and 1000 nF in red and dark blue respectively. The plot shows that the mirror consumes the excess overhead voltage.

Several different regulators were tested, but they all suffered from the same overshoot as in Figure 4.13. The problem was caused by gate access via parasitic capacitances when the load capacitance were introduced.

After some trial and error, a very stable solution was found by utilizing the slew rate in a non-inverting op-amp with the feedback pin directly to a grounded shunt resistor. The op-amp will then regulate the output to force the feedback voltage at the same voltage as the input without common mode issues. By using a 100 Ω shunt resistor, the input has to be at 200 mV to drive 2 mA trough the load.

The LT1784 was found to be a good match for the application with a single supply voltage range up to 18 V and slew rate at 2.2 V µs^{-1}, shown in Figure 4.14 (b). Although the schematics give the impression of a large footprint, the LTC6255 and LT1784 combined takes the same area as the cascoded current mirror.

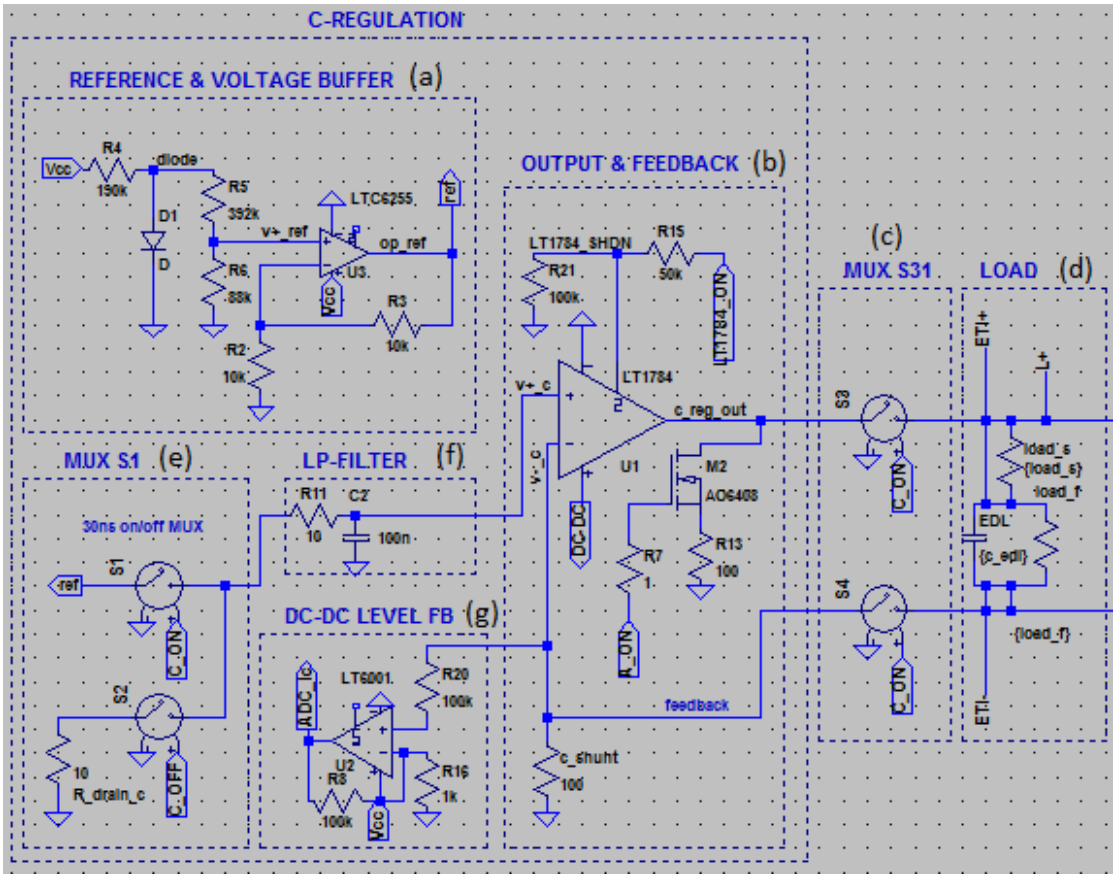


FIGURE 4.14: A stable regulation of the cathodic phase using two op-amps and the multiplexer switches.

The stability for this solution demands a stable reference voltage, which rules out the use of voltage division directly from the battery source. The problem was solved by using a stable analog reference, shown in Figure 4.14 (a). This part of the circuit maintains a stable 200 mV reference close to independent of Vcc variations, depending on the choice of diode. For a Vcc variation of 2.8 V to 2.4 V the corresponding output current deviated with 21 µA using an ideal diode, shown in Figure 4.15. PWM regulation is a possible option as well, and can be connected to the positive input of the reference buffering op-amp (U3). A PWM generated reference will give more options for changing the stimulating current. This could also be obtained by using a programmable gain op-amp instead.

The MUX S1 (e) charges and drains the positive input to the LT1784 via a first order LP filter which is tuned for the full range of possible load capacitances. The LT1784 is enabled and disabled at the SHDN pin by the LT184_ON signal. The M2 transistor acts as a drain to keep the c_reg_out output (b) voltage low when the MUX S31 (c) switch is closed. This is necessary as the start up phase of the amplifier generates a small output voltage. The load is pulsed by enabling the MUX S31 (c) switch, resulting in a feedback voltage over the c_shunt (b) resistor. The circuit is stable for both Vcc variations and load capacitance variations, deviating with 10.5 nC and 5.1 nC respectively (Figure 4.15 and 4.16).

The power consumption of the circuit is dominated by the LT1784 amplifier, shown in Figure 4.17. The plot shows that for higher EDL capacitances, the required voltage output is lower. For a fixed voltage supply, the excess voltage will be dissipated in the amplifier. The overall loss is however constant when combining the power dissipation in the tissue and the amplifier. The interesting observation is that for EDL values above 1 µC the required voltage output can be significantly lowered, giving options for power optimization by regulating the converter output accordingly.

The LT1784 dominates the power consumption in the circuit, consuming 3.3 mW alone and 3.6 mW with all the peripherals. This is for a 3 kΩ load and 6.5 V

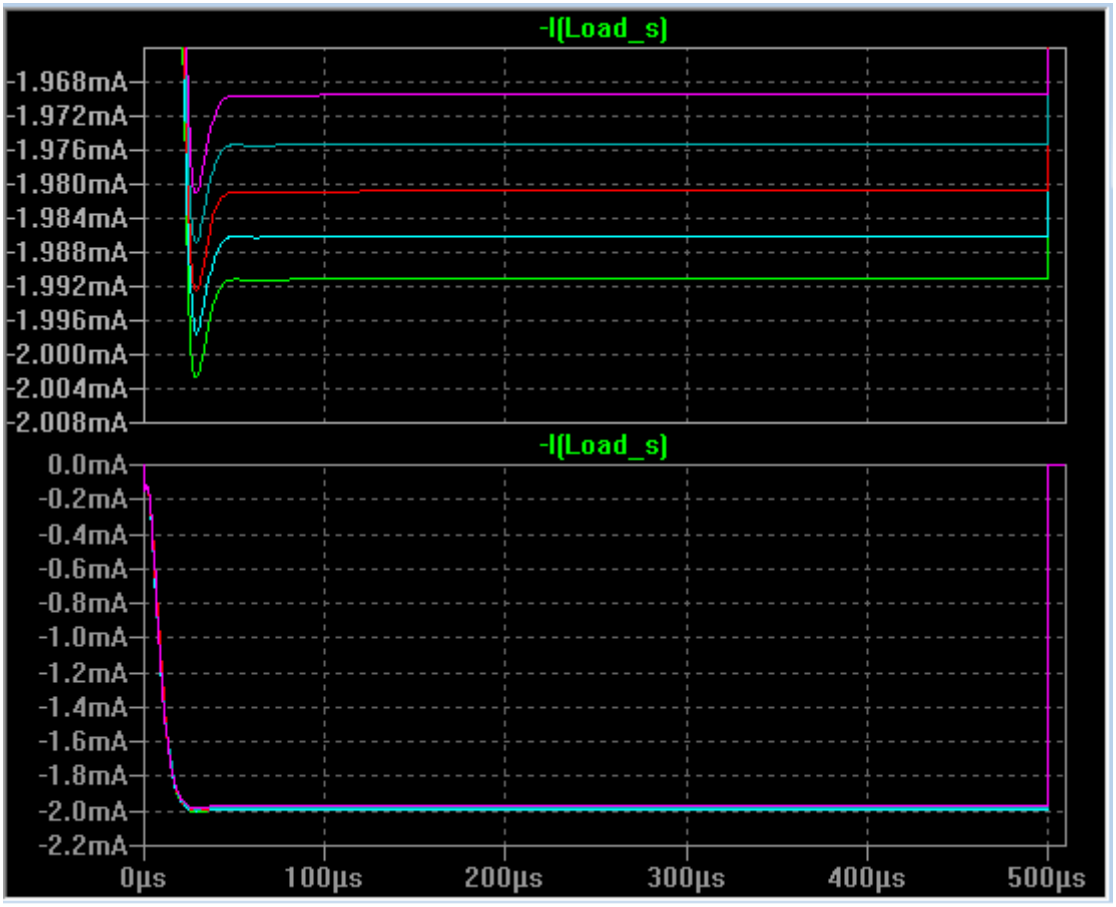


FIGURE 4.15: For a Vcc variation of 2.8 V to 2.4 V the corresponding output current deviated with 21 µA, shown in the top pane. The deviation equals to 10.5 nC charge deviation. The lower pane is zoomed out to shown the falling and rising edge.

optimized supply level, and may therefore be higher in a real implementation, depending on the available converter levels.

The SFE-C pulse in tested in Figure 4.15 for variations in the Vcc supply voltage, which is a problem when the battery voltage is decaying. The upper and lower plot shows the same information, but the upper is zoomed into the reference level and reveals the Vcc deviation from 2.8 V to 2.4 V in the green and purple line respectively. The deviation equals to 10.5 nC, which is within specification.

In Figure 4.16 the regulation is tested for variations in the EDL capacitance. Similar to the previous plot, the upper and lower graph shows the same information, but the upper is zoomed into the reference level. The deviation for EDl variations is less than with Vcc variations.

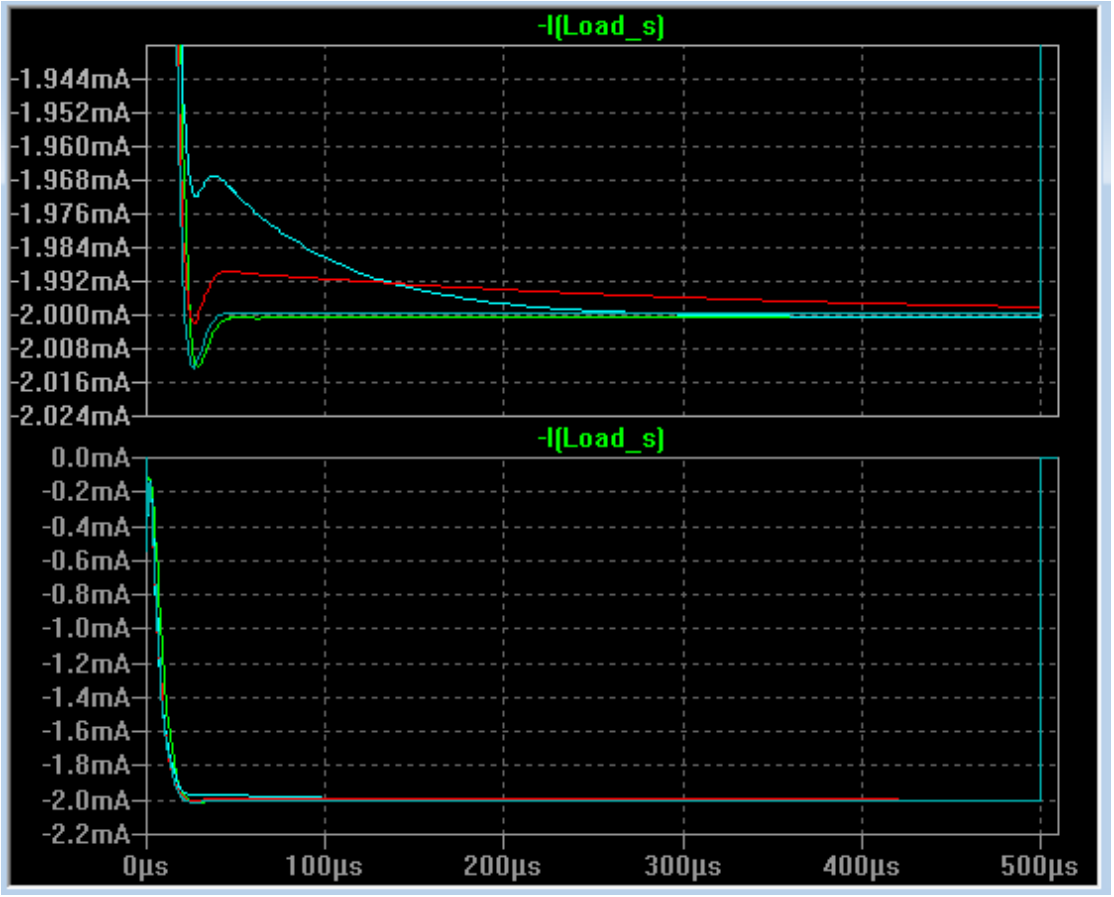


FIGURE 4.16: For a EDL capacitance variation of 0 nF, 22 nF, 100 nF and 1000 nF the corresponding charge deviation is 5.1 nC shown in the top pane. The lower pane is zoomed out to shown the falling and rising edge.

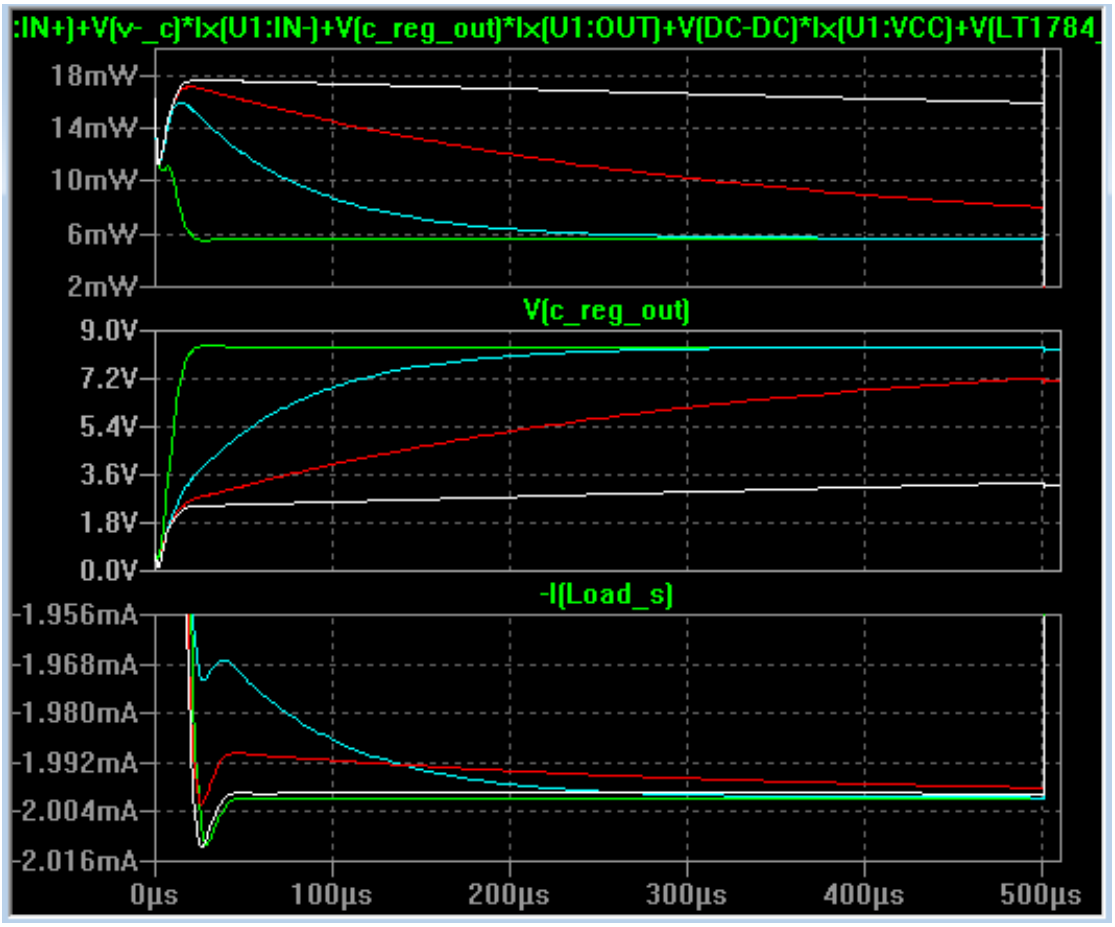


FIGURE 4.17: The current consumption in the LT1784 amplifier for EDL values at 0 nF, 22 nF, 100 nF and 1000 nF in green, blue, red and white respectively, shown in the top pane. The mid pane V(c_reg_out) is the voltage output from the amplifier. The lower pane shows the regulated current over the resistive load at 4 kΩ, requiring 8 V compliance for the required current. The amplifier is powered with a 9 V supply in this case, but can operate close to the voltage compliance due to a rail-to-rail operation (+500 mV).

SFE-C Evaluation

TABLE 4.2: The performance of the SFE-C module is within the required limits except the current consumption.

SFE-C	Limit	Performance
Falling edge	26 µs	24 µs
Rising edge	20 µs (min IPD)	1.5 ns
Ripple	27 µA	0 µA
Overshoot	47 µA	13 µA
Error	1.22%	1.07%
Current	1 mA	1.44 mA

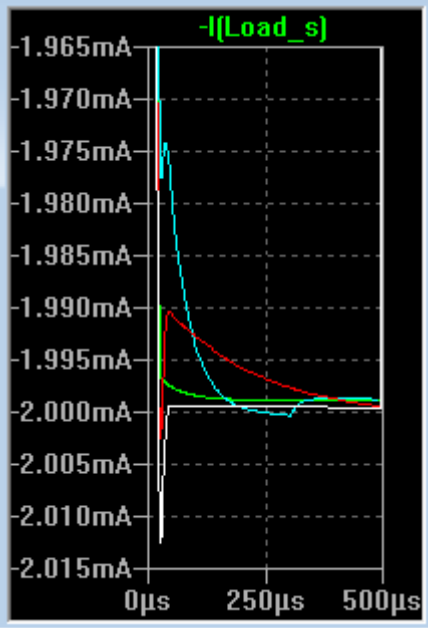


FIGURE 4.18: Cathodic pulse for the different EDL values showing a maximum overshoot at 13 µA

The SFE-C module performs within the specification, except for the current consumption. The overall performance, and especially the regulation, was very good. Despite the high current consumption it was reasonable to proceed to the SFE-A design as the current consumption for the rest of the modules can either be reduced, or the battery changed. Note that the main contributor to charge deviation was variation in the Vcc supply voltage.

The rapid rising edge results from disabling the LT1784, and provides a smart solution to the interphasic delay with the associated output disconnect, resulting in isolation for the positively charged side of the load.

4.4.2 SFE-A

Regulation and power consumption

The multiplexer eliminated the need for switches with drivers, and the SFE-A module is thus only concerned with the regulation. As mentioned in the inverting DC-DC design trial, the SFE-A module must handle EDL discharge as well as total charge control. A complete analog solution would be very power efficient since the MCU could be in sleep mode for the whole period, but the regulation proved too difficult to implement. This is due to the fact that the anodic phase cannot have a control input larger than the previous input, resulting in a decaying slope, or at most, a flat slope (Recall the anodic phase in design considerations 2.4).

The complete SFE-A module is shown in Figure 4.19, where the input is a 7.813 kHz PWM signal applied to the PWM port at the section marked 3-O. LP FILTER (a), which is a third order LP filter necessary for keeping the ripples within the required level. The filtered output is amplified through the Q1 NPN transistor and scaled with the R1 resistor in the current buffer (b). The buffering is provided by the Q2 PNP transistor, resulting in very high output impedance, which is necessary as the EDL discharged loads the output. The current buffer will also act as a constant current source, regulating the output current very tightly independent of the load characteristics. The nMOS M3 transistor shunts away excess voltage when the switch MUX S32 (e) is closed to avoid large inrush current when the switch opens. This is necessary as the filter delay is over 1 ms, and the output must therefore be active during the cathodic phase. The discharge of the EDL capacitance is provided by the diode D2 in (c) and is peak limited by the resistor a_shunt in (f), which also performs the feedback measurement via the integrating op-amp.

The control problem could be solved with a simple algorithm based on knowledge of the remaining time of the anodic period. The measured charge is then

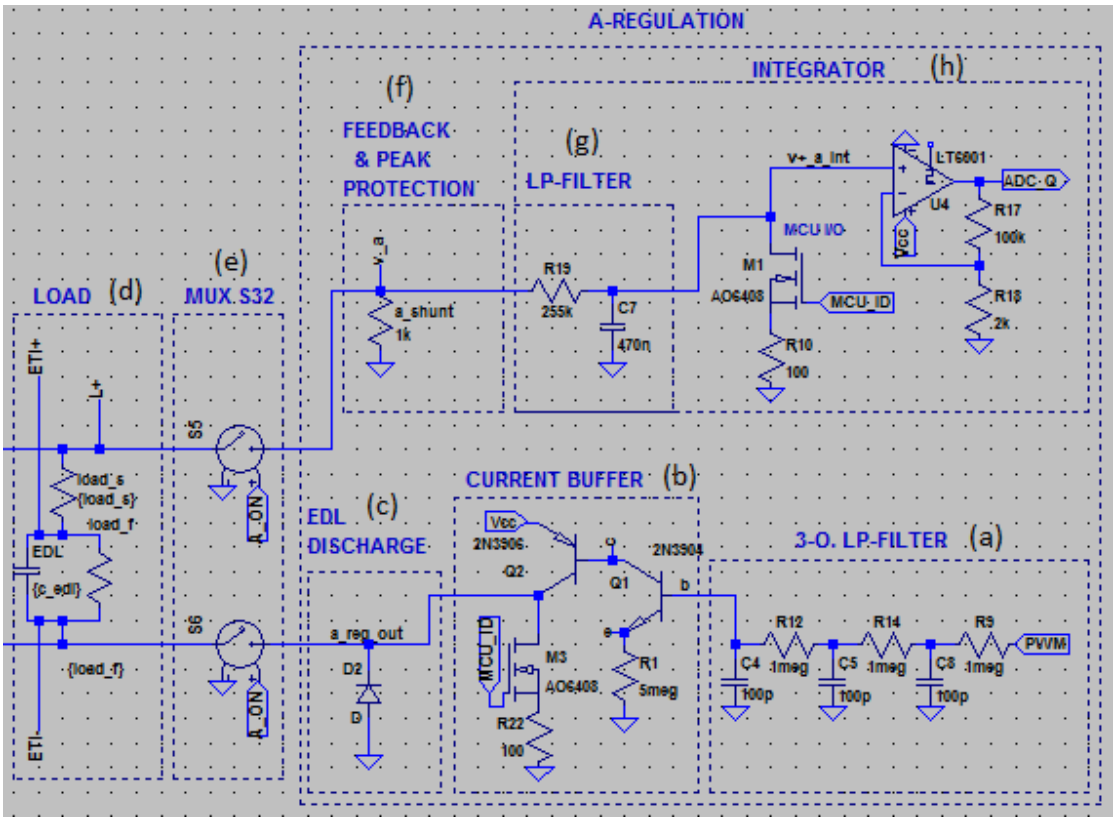


FIGURE 4.19: A third-order LP filtered PWM signal is buffered trough a NPN PNP BJT current buffer (b) and passed to the load when the MUX S32 (e) switch enables the output. A measuring resistor a_shunt (f) passes the voltage representation of the current to an integrating op-amp (h), and serves at the same time the purpose of peak reduction, hence the large value. Note that the integrator is not a true integrator, but has a LP filter (g) tuned to have an approximately linear response for the application. This is to save footprint, as a true single-supply integrator would demand an additional op-amp as inverting buffer. The EDL discharge using a diode is not an optimal solution due to the diode drop. The worst case scenario may be that the EDL do not discharge at all for very large capacitances.

subtracted from the reference charge and divided on the remaining time, resulting in an updated average output current. This will work since the output is buffered, hence there is a stable proportional relationship between control input and load current. A substantial effort was put into the code for the MCU that would perform this operation at low CPU frequency to stay within the current consumption requirement. It was found that the CPU used 1673 ms to perform the necessary binary division at 1 MHz. The results were the same when using a PI controller tuned with a settling time lower than the pulse period. The conclusion was that a controller based on heavy CPU operations is too costly power-wise for

the application.

A novel solution is to map the 2 mA slope for the resistive load shown in Figure 3.6 to a corresponding PWM output. This is then the default output with no capacitance in the load, and enables the controller to run in open-loop until charge deviance is measured. A disturbance is still present due to Vcc variations for the PWM output, but can easily be compensated for by reading the Vcc value from the PU module. Vcc variation affects the total charge 30 times more in the anodic phase compared to the cathodic, and is therefore crucial to incorporate into the system. The current output to the load is mapped to the PWM ON time and Vcc decay by the equation

$$i_{(\mu A)} = K_{u0} + K_u \cdot ON_{(\mu s)} - K_v \cdot VCC_{(mV)} \tag{4.1}$$

where the ON time is in the range 50 µs to 80 µs for a PWM period of 128 µs (7 bit resolution @ 1 MHz) and VCC decay from 3 V to 2.4 V. K_u is determined by the resistor R1 in Figure 4.19 (b). Values from simulation gives $K_{u0} = 22$, $K_u = 0.9$ and $K_v = 0.22$. The unknown variable is then the extra charge which is injected into the system from the EDL discharge. This disturbance is guaranteed to settle within 4 ms, and for this period the system will run in open loop using a PWM map, and save power by releasing the CPU. The CPU performs Algorithm 1 when active, where the error is always positive as the PWM map at $t = 4$ ms will have an instant current output which will exceed the maximum Vcc charge drop. Note that the error is not added to ensure small decrements in control output as well as to save CPU computation. The algorithm will converge to a reference charge Q_{ref} for a sufficient number of samples N. Simulation in Atmel Studious 6.0 revealed that each sample in the for loop takes up to 50 µs due to the ADC delay, and that the reference is met within ten samples.

The current consumption of the SFE-A module is shown in Appendix A, Figure A.5. The average consumption for all components were simulated to 20 µW. The real consumption must however be measured accurately in the prototype phase.

Algorithm 1 Anodic charge control

while $t < 4\,\text{ms}$ **do**
  $u_{DC} \leftarrow PWM_{map}$ ▷ open loop with u_{DC} as the PWM duty cycle
end while
$V \leftarrow VCC_{PU}$ ▷ get Vcc level from PU module
for i:=1 to N **do**
  $Q_t \leftarrow ADC_{int} \cdot K_q$ ▷ read value from integrator mapped to nC with K_q
  $t_\Delta \leftarrow t_p - t$ ▷ t_p is the full anodic period
  $Q_p \leftarrow t_\Delta \cdot (K_{u0} + K_u \cdot u_{DC} - K_v \cdot V)$ ▷ calculate final charge using eq. 4.1
  $e_q \leftarrow Q_p - Q_{ref}$
  if $e_q > e_{tol}$ **then** ▷ where e_{tol} is the tolerated charge error
    $u_{DC} \leftarrow u_{DC} - K_p$ ▷ where K_p is the gain
  end if
  Sleep for $t_S > t_d$ ▷ where t_d is the LP filter delay
end for

SFE-A Evaluation

TABLE 4.3: The performance of the SFE-A module is within the required limits except the peak limitation.

SFE-A	Limit	Performance
Amplitude	1.4 mA	2 mA
Ripple	15 µA	1 µA
Error	2.6%	≈ 0.1%
Output Z	0 kΩ to 4 kΩ	1 kΩ
Current	1 mA	1.44 mA

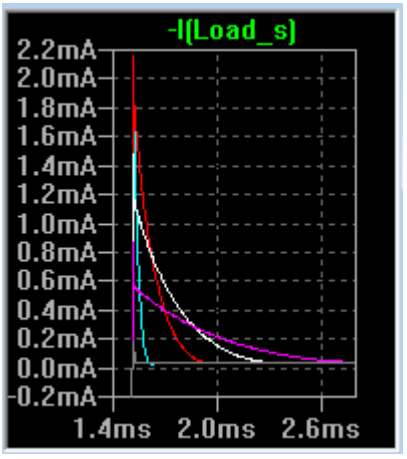


FIGURE 4.20: EDL discharge for the SFE-A module

A good solution for the SFE-A module has been found. The solution is based on a LP filtered PWM input, which is buffered and regulated using an integrating op-amp. The requirements are within specification except the EDL discharge peak, but this is assumed to be lower in the real implementation as the simulated peak is not dampened trough the MUX. The current consumption is simulated to be above the allowed limit, which must be further tested in the prototype phase.

4.4.3 SFE-TC, CU, PU and HDI

The SFE-TC module manages the MUX control and enabling/disabling of active components. The module also runs the SFE-A control algorithm, and is solely implemented in software.

The CU module enables the other modules by MCU I/O lines.

The PU module is extremely simple and is realized by using a single op-amp and a voltage division from the Vcc voltage. The PU serves two purposes: 1. Alert the CU if VCC voltage is below critical level, and 2. Update the Vcc parameter for the SFE-A PWM regulation.

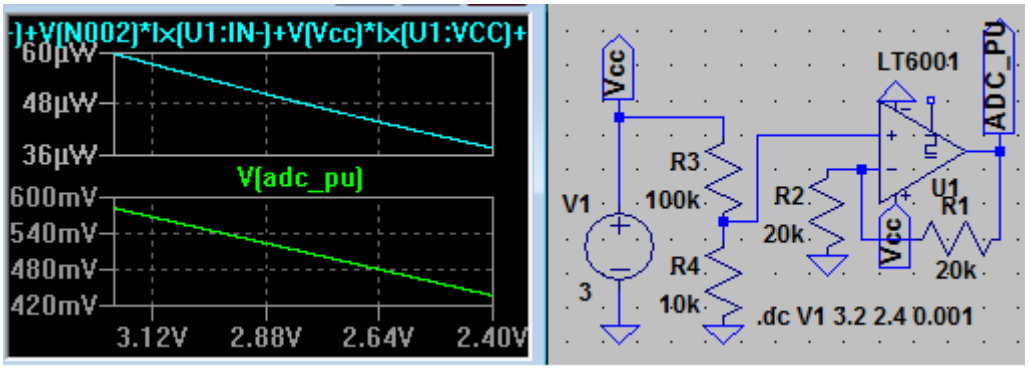


FIGURE 4.21: The PU module is simply a non-inverting op-amp. The ground to resistor R4 and the positive supply for the op-amp can be connected to the MCU I/O pins, for tri-state and ground respectively. This will result in virtually zero power consumption, as the circuitry only has to be powered for brief moments (20 µs) for the ADC to complete one conversion. The plot V(adc_pu) in lower left pane is the op-amp output versus Vcc voltage from 3.2 V to 2.4 V. The upper pane is the power consumption for the circuit.

If the PU is read for every device duty cycle (every 5 min), the total time for the device life is below 1 s, and the power consumption dominated by the ADC is negligible.

4.5 Prototyping and measurements

The complete SFE module was assembled on a breadbord with the associated components soldered to prototyping PCB's, shown in Figure 4.22.

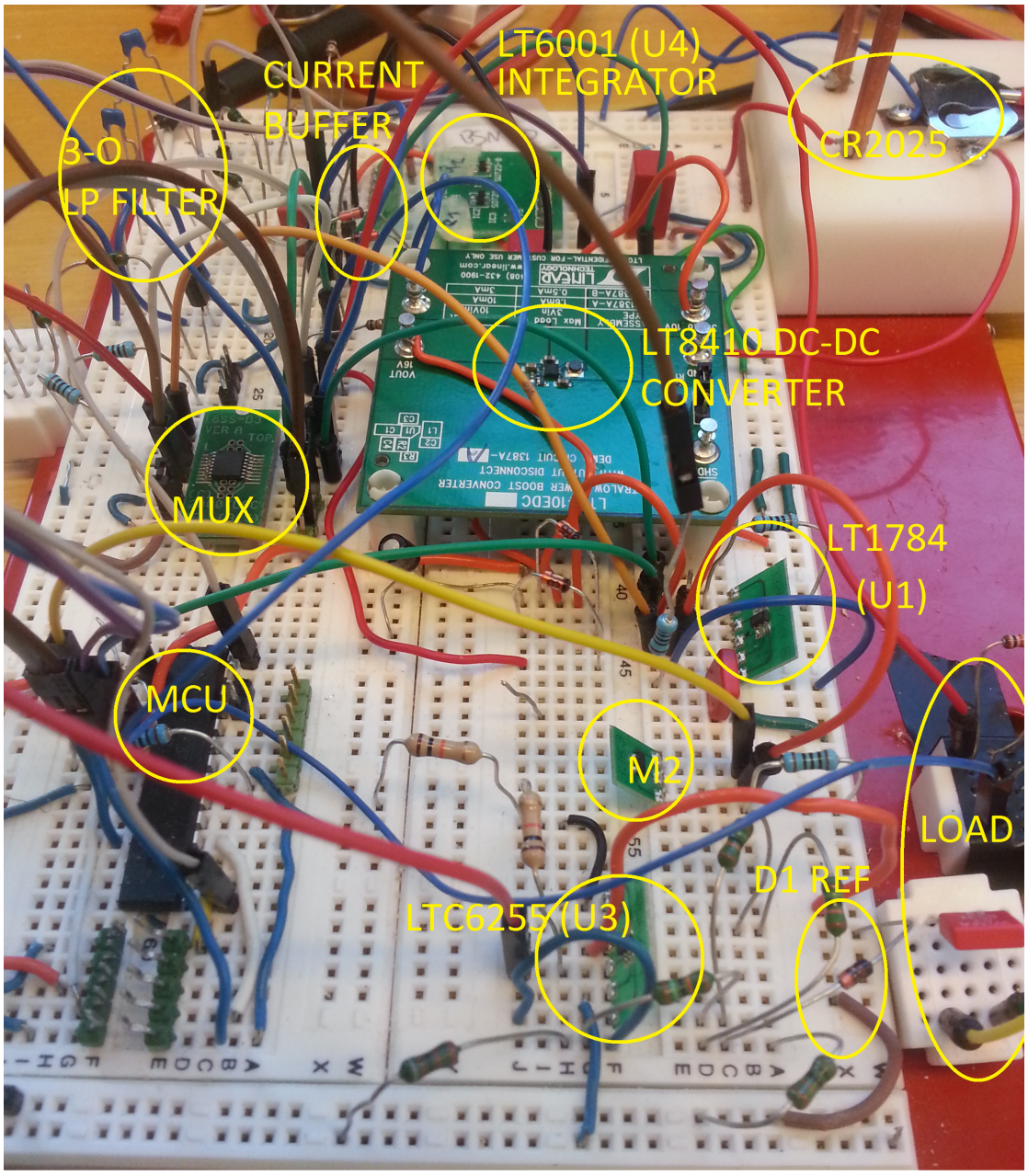


FIGURE 4.22: The complete prototype mounted on a breadboard. The wires are subject to noise which may affect the measured output. Some of the circuit components are not marked as they are not visible. The complete Bill Of Materials (BOM) list contains 6 integrated circuits (by using dual packages), 11 capacitors, 29 resistors, 1 diode, 1 inductor, 1 LED, 4 MOSFET's and 2 BJT transistors. By using the smallest packages available for the integrated circuits and the 0402 package for most resistors and capacitors, the estimated total footprint is at 100 mm^2. This is 1/3 of the available space on a circular PCB with a diameter at 20 mm, and should provide sufficient room for traces, inductor and the larger capacitors on a single sided PCB.

The SFE-TC and CU module was written in C code for the Attiny 48 MCU. The code was restricted to the test of the prototype. The complete code with optimization is thus subject to future work when the circuit is to be miniaturized.

The PU module was measured to perform as predicted in the simulation prior to the SFE measurements.

Regulation

The cathodic pulse was first measured over a 4 kΩ resistive load, shown in Figure 4.23. The cathodic phase is shown in (a) with a falling edge at 20 µs and rising edge at 7.5 µs. The overshoot was at 45 µA, which is close to the limits from the requirements. Charge deviation was measured to 11 nC for variations in Vcc voltage at 2.8 V to 2.4 V. The pulse is shown in Figure 4.24 for a capacitance at 220 nF. For the full range of capacitances the charge deviation was 8 nC as predicted in the simulations, and the charge deviation is thus dominated by Vcc variations.

The interphasic delay was measured to 20 µs, shown in Figure 4.23 and 4.24 (c). The IPD were constant independing of load.

The SFE-A module was tested in the same manner, and measurements were performed to calibrate the controller. The integrator output was not settled until 14 ms had passed, and the PWM was therefore set to run for 14 ms. The net charge in the measurements were consistent at 400 nC when the cathodic deviation was subtracted, which is a value easily changed for updated constants, shown in 4.23 and 4.24 (d). The charge deviance was similar to the measured deviance in the m102 stimulator, indicating that the measuring equipment may be the main contributor to the deviance. The anodic phase is shown in 4.23 and 4.24 (b) for the resistive and capacitive load respectively. Note that the ripple is distorted due to noise in the measurements. The EDL discharge spike were significantly lower than in simulation, shown in Figure 4.24 (b). This is assumed to be due to damping when the signal passes trough the multiplexer. A small peak is also

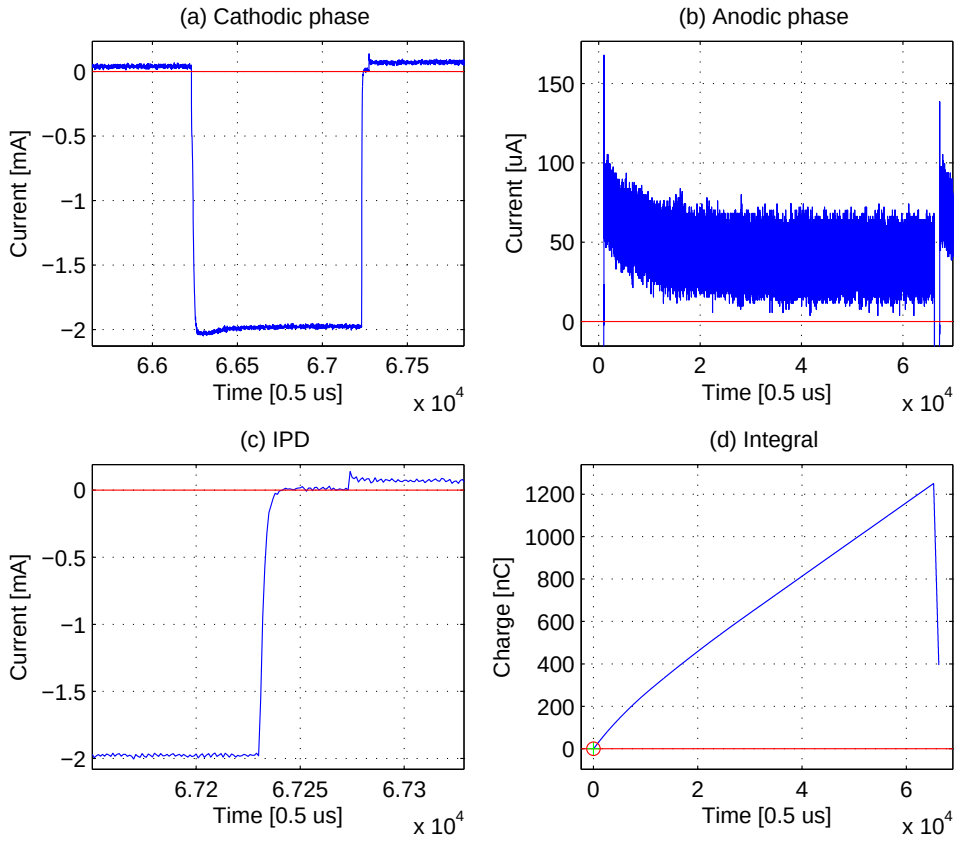


FIGURE 4.23: The output pulse for a resistive load at 4 kΩ in total. The cathodic phase in (a) has the same performance as in simulation. The anodic phase in (b) has a more aggressive slope compared to the m102 stimulator. This is due to the values in the PWM map, which can be configured differently. The interphasic delay in (c) is at 20 µs. The total charge in (d) is regulated to 400 nC which is easily configured to the reference with some calibration.

present for the resistive load, shown in Figure 4.23 (b). This is assumed to originate from accumulated charge at the a_reg_out node due to insufficient drain of the M3 transistor (Figure 4.19 (c)).

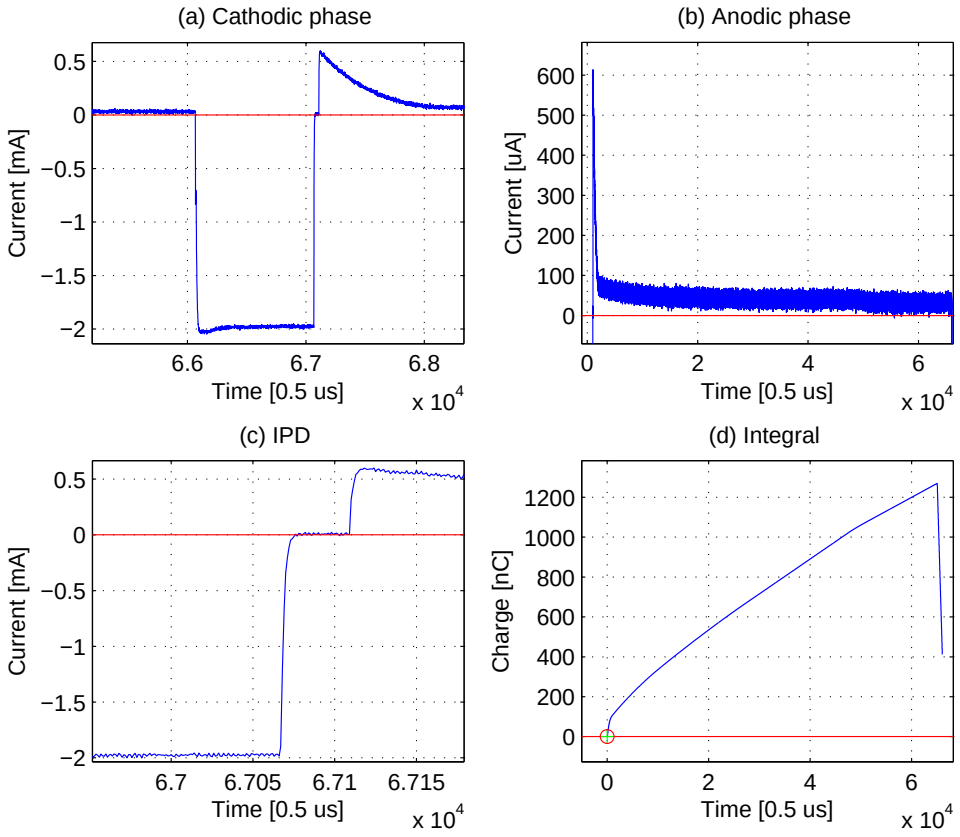


FIGURE 4.24: The output pulse for a capacitance at 220 nF in parallel with a 3 kΩ resistor. The cathodic phase in (a) has the same performance as in simulation. The anodic phase in (b) discharges the EDL with a peak within specification. The regulation of the anodic phase is apparent in the close to the end where it "dips" slightly. The interphasic delay in (c) is at 20 µs. The total charge in (d) is regulated to 400 nC which is easily configured to the reference with some calibration.

Power consumption

All modules were performing within specification down to a Vcc level of 2.4 V with a 100 mV margin. For 6 hours of continuous pulsing, the Vcc level was an average of 2.8 V. The testing was performed on the CR2025 battery from Energizer. It is assumed that the circuit will operate at a worst case average at 2.7 V, resulting in 337 mW h total capacity.

The performance is given in Table 4.4. The SFE-A module has an idle power dissipation at 104 µW where over 80% is lost in the current buffer. When the SFE-A is active (active CPU and ADC), the power dissipation is 4.2 mW mainly

TABLE 4.4: Measured power dissipation for for each module at cut-off voltage at 2.4 V for the coin cell CR2025 is estimated to a total power dissipation. The SFE-TC power dissipation is included in the SFE-C and SFE-A. The measurements is performed with having the DC-DC converter run for the whole pulse period, which was 7 times more power efficient.

MODULE	Active hours	Instant	Total
SFE-C	5.9	18.36 mW	108.3 mW h
+ DC-DC idle	379	0.13 mW	50 mW h
SFE-TC	384.9	-	-
SFE-A	379	720 µW	273 mW h
CU	384.9	4.05 µW	1.9 mW h
PU	-	30 µW	19 nW h
HID	-	13.5 mW	3.75 µW h
DISSIPATED			433 mW h
CAPACITY			337 mW h

due to dissipation in the ADC. With no code optimization, the active period is 5 ms, resulting in a total draw at 720 µW.

With optimization for the SFE-C module, 2.14% power can be saved if the DC-DC level op-amp (U3) is used once for every device duty cycle. The PU module can be optimized to run for 1 ms once each hour, dissipating 30 µW at each run. For the whole device life this adds up to not more than 2.2 seconds in total, resulting in an average dissipation at 19 nWh

The HID module can be optimized using a 5 mA pulse for 1 ms. The device should be able to use less than 1000 pulses, resulting in 3.75 µW h in total dissipation.

The total power consumption exceeds the capacity in the CR2025 battery with 128%, calculated in Table 4.4. The CR2032 has about 200 mW h additional capacity, and should therefore be used instead.

4.5.1 Mechanical design

Electrode connector

The connector for the 304 leads have the measured dimensions as depicted in Figure 4.25. The Conductor 2 was measured to be connected to the green electrode in Figure 3.2, and is thus the positive terminal for the SFE module output (L+ in the schematics, Figure 4.19).

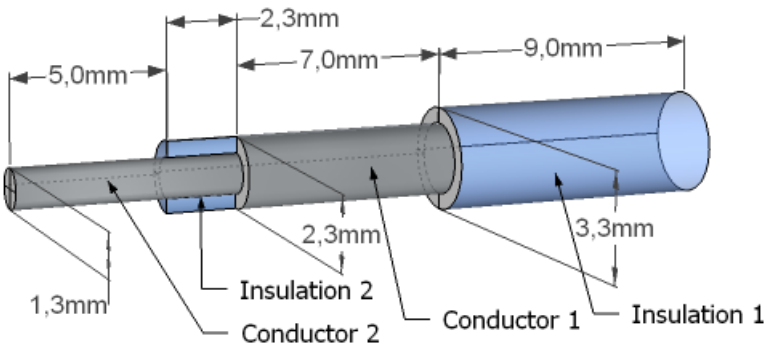


FIGURE 4.25: The electrode connector pin dimensions. The conductors must be mapped to the anode/cathode to avoid anodic blocking in the stimulating direction. The device encapsulation may cover "Insulation 1" completely or partially depending on the best solution. The electrode leads extends from the right end of "Insulation 1" via a silicon tube at 2 mm in radius. This tube is coiled up under the skin of the animal and connects to the vagus nerve. To avoid current leakage into the tissue, the surface "Conductor 2" must be completely covered by encapsulating mass. This restricts the device length/width for a minimum at approximately 20 mm when allowing some margin in both ends.

Configuration

A possible configuration of the final PCB together with the electrode pin with connector and the CR2032 battery is shown in Figure 4.26. The configuration is based on the use of a very thin PCB, where the total height including components is at 1.3 mm. The encapsulating layer can not be thicker than 1.25 mm to stay within specification on the top and bottom side.

The lowest feasible total volume is estimated to 3.5 cm^3, taking into account the battery brackets and the electrode pin. The Cyberonics m102 is at 14.7 cm^3, which

results in a possible size reduction down to 1/4 of the m102's size. This is half the size of the required size reduction, and is very satisfactory.

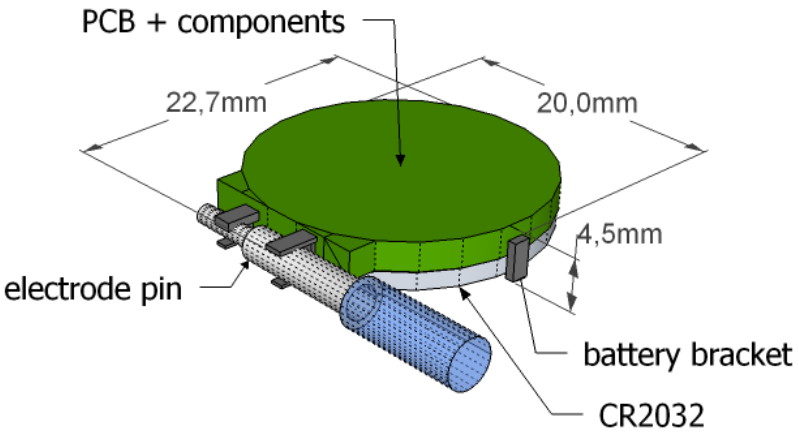


FIGURE 4.26: The height of the device is the crucial parameter, and can be at minimum 4.5 mm for the CR2032 battery, using a very thin PCB and low profile components.

Encapsulation

The complete device must be encapsulated in a material that enables the user to change the power source, as well as to stay biocompatible. The biocompatibility depends on the classification on the material, which must be of USP Class VI and adhere to the device components.

Master Bond Inc. have a range of biocompatible epoxies and silicone adhesive systems for implementation grade medical devices. The EP21LVMED two part epoxy was tested for a solution where the epoxy encapsulated the device, but leaves a section for insertion of the battery. To be able to free the electrode from such a solution it would be necessary to use the Sygnus electrode connector from Ballseal, shown in Figure 4.27.

A simpler solution would be to encapsulate the complete device with silicone, having the electrode pin and battery connected to the device upon molding. The Masterbond silicone SIL151MED was tested for water intrusion and easy removal,

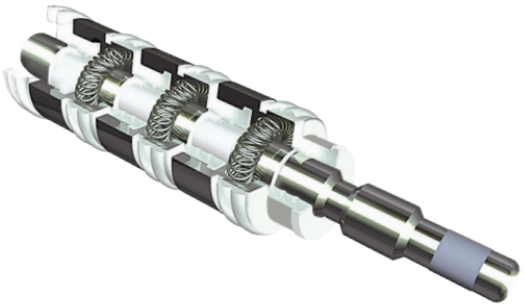


FIGURE 4.27: A completely biocompatible connector system measuring 3.5 mm in outer diameter. From the Sygnus implantable contact system manual, [15].

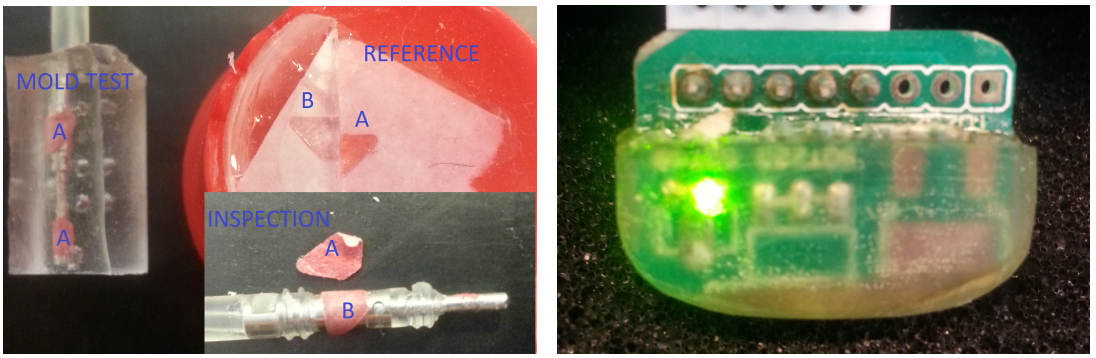


FIGURE 4.28: Left: The sealing for the silicone was tested against the 304 electrode connector pin using a moisture indicator paper, where the area marked A in the reference is exposed to water. The mold test were performed with the silicone submerged in saline solution for 3 months. The inspection indicated that there was no water intrusion. This was predicted as the silicone adhered strongly to the electrode tube silicone. Right: The HDI module was tested for visibility trough the Masterbond EP21LVMED biocompatible epoxy. A 5 mA pulse for 1 ms was found to be the optimal output for good visibility and low power dissipation.

shown in Figure 4.28 to the left. A moisture indicator paper was attached to the electrode pin conductors and inserted into a mold with the silicone. The sealing was then tested by being submerged in saline solution for 3 months. The result was that the silicone was completely sealed and fairly easy to remove, and is thus a simple and effective method for encapsulation.

Although the HDI module is extremely simple to implement in hardware, it is difficult to know the required current pulse necessary to have a visible light trough the semi-clear epoxy without testing. A 5 mA pulse for 1 ms was found to be the optimal output for good visibility and low power dissipation, shown in Figure 4.28 to the right.

Chapter 5

Discussion

From the requirements analysis and the literature study, it was concluded that the Cyberonics 304 leads are utilizing a microstimulating output (MSO) which is not described in the literature. The measured MSO opposes the generally accepted aim to avoid a net DC flowing in the tissue. It was hypothesized that the net DC was enhancing the pseudo-capacitance in the electrodes, and thus contributing to tissue stability by lowering the interface impedance. This corresponds with the proposed equation 2.18 where the interface overpotential is lowered as a result.

The information presented in this thesis can be used to develop a nerve stimulator for use in small animal models, compatible with the Cyberonics 304 leads. The waveforms discussed in Figure 2.11 may also be obtainable by small changes to software or hardware, resulting in a design which can be compatible with other types of electrodes as well. The standard exhaustive waveform (e) is for an example obtained by simply disabling the regulation in the SFE-A module.

The presented design is however restricted to a prototype nerve stimulator. The final design must be miniaturized, where issues may arise due to noise from the switching DC-DC regulator. The software should be optimized to reduce current consumption, and a pMOS transistor should be used to discharge the EDL capacitance to avoid limitations by the relatively large diode drop. Also, some fabrication and molding is necessary to complete the mechanical design.

5.1 Assessment of system compliance

5.1.1 Module level

The module compliance is verified by evaluating the test requirements in the traceability matrix, Table 3.15. The test ID with results is given below:

T-1: ✓ Charge deviation was measured within limits for the SFE module. No ratcheting of potential was measured. Timing was within limits.

T-2: ✓ SFE-C rising and falling edges, ripple and overshoot was measured within limits.

T-3: ✓ The SFE could pulse a 5 kΩ load with 2 mA constant current.

T-4: ✓ An eligible power source were found using the CR2032 coin cell.

T-5: ✗ The device duty cycle is subject for future work as it is not an essential feature to test in this prototype stage.

T-6: ✓ The SFE was able to detect if a load was connected.

T-7: ✓ The PU module responded satisfactory to voltage variations.

5.1.2 System level

1 - Features: The MSO is compatible with the Cyberonics 304 electrodes by utilizing the pseudo-capacitance with an anodic current bias, thus keeping the overpotential within the water window and providing safety with respect to the tissue. The prototype can be miniaturized and encapsulated to an implantable device for use in laboratory rats.

2 - Output: The output is within specification and verified on module level.

3 - Size: The possible overall estimated size is half of the required size, and is well within the specification.

4 - Operation: A replaceable power source was chosen to have capacity for more than 3 months. Event feedback to the operator was tested to perform within specification.

The performance of the SFE module is summarized in Table 5.1. The SFE is the essential module for the overall design, and depends on the PU module for proper operation. The PU module was in the initial design phase defined to output a logic signal related to whether the battery voltage was above or below a defined limit. However, the actual implementation demands that the PU output is proportional to the battery voltage. Explicit interfaces for the software modules is not given as this is subject to future work, and will follow an eventual implementation of the proposed state machine for the CU module. The design and implementation of the SFE module was the main focus in this thesis, and was completed within requirements if powered by the CR2032 battery.

TABLE 5.1: The performance of the SFE prototype module. The current consumption for the SFE-A module was not within the proposed limits for a CR2025 battery, but the overall power dissipation is within limits for a CR2033 battery which is estimated to have 520 mW h available capacity.

Parameter	Limit	SFE-C	SFE-A	Ver.
Falling edge	26 µs	15 µs	-	✓
Rising edge	20 µs (min IPD)	7.5 µs	-	✓
Ripple	C = 27 µA A = 15 µA	20 µA	15 µA	✓
Overshoot	47 µA	45 µA	0.6 mA	✓
Error	C = 1.22% A = 2.5%	1.1%	1.6%	✓
Power	520 mW h	158 mW h	273 mW h	✓

Chapter 6

Conclusion

This thesis describes a novel prototype design of an implantable nerve stimulator primarily for use in VNS applications, compatible with the bipolar 304 leads from Cyberonics Inc. The stimulator is designed with commercially available components, resulting in a low-cost and portable solution. A modular architecture describes the system with respect to specifications given by end user and limitations from a literature study.

It is concluded that an implantable nerve stimulator for VNS applications can be designed with a four fold size reduction compared to the VNS stimulators available for human use, resulting in a more optimal solution for use in small animal models.

Chapter 7

Future work

Optimization

The circuit design is completed with components with options for very small packages, and can therefore be miniaturized without any change to the general design. The circuit should however be optimized. The EDL discharge diode (D2) should be changed with a pMOS transistor with gate and source connected to the load, and drain to ground. The discharge will then go trough the body diode which has very little voltage drop. The transistor will also block the output from the current buffer to not be shorted to ground via the same mechanism. The complete SFE schematics including this optimization is shown in Appendix A Figure A.4.

The software for the MCU should be optimized for low power operation, and could probably run on a lower clock frequency than 1 MHz.

Calibration

The PCB should be calibrated for an environment at 37 °C + internal heating. To perform this the PCB must be encapsulated with a heat sensor, and placed in a 37 °C environment. As the PCB does not have room for heat sinks nor any

air cooling, the circuit is prone to additional heating, which will be registered by the temperature sensor. The necessary constants for the system can be identified when the operating temperature is settled.

EMC

The PCB should be tested for EMC due to the 700 kHz noise from the DC-DC converter, which may result in significant noise for the op-amps and ADC conversion when the circuit components is placed on the final PCB.

Encapsulation

Battery brackets and electrode connector brackets must be fabricated, and should be of a biocompatible material in case of leakage. A mold form must be designed for easy and fast encapsulation of the main components, and should be constructed in a non-stick material such as Teflon.

Documentation

A user manual should be supplied to the end user, providing information on normal operation, troubleshooting, battery replacement and molding.

Appendix A

LtSPICE Schematics

Inverting DC-DC converter optimization

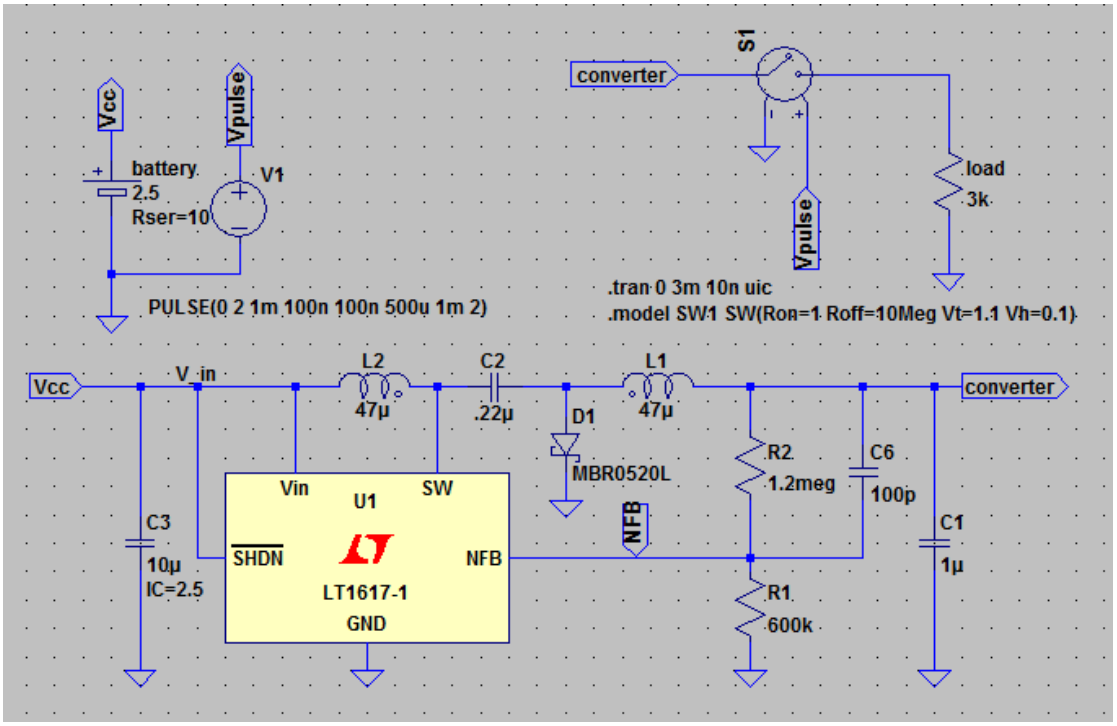


FIGURE A.1: Simulation model for LT1617-1. R1 and R2 is configured for an output at $-6\,\mathrm{V}$

The switching period is approximately given by the time constant $\tau = C1 \cdot (R1 + R2)$. The period between switching in "standby" mode was therefore greatly

reduced by large values for R1 and R2. The C1 capacitor could not be chosen too large due to associated in-rush currents at start-up.

The quiescent current for the converter is 20 µA. The "standby" current for the complete pulsing period was optimized to 22 µA, and was a result of the necessary switch initiations to keep the output voltage over C1 at the reference level (6 V).

Non-inverting DC-DC converter

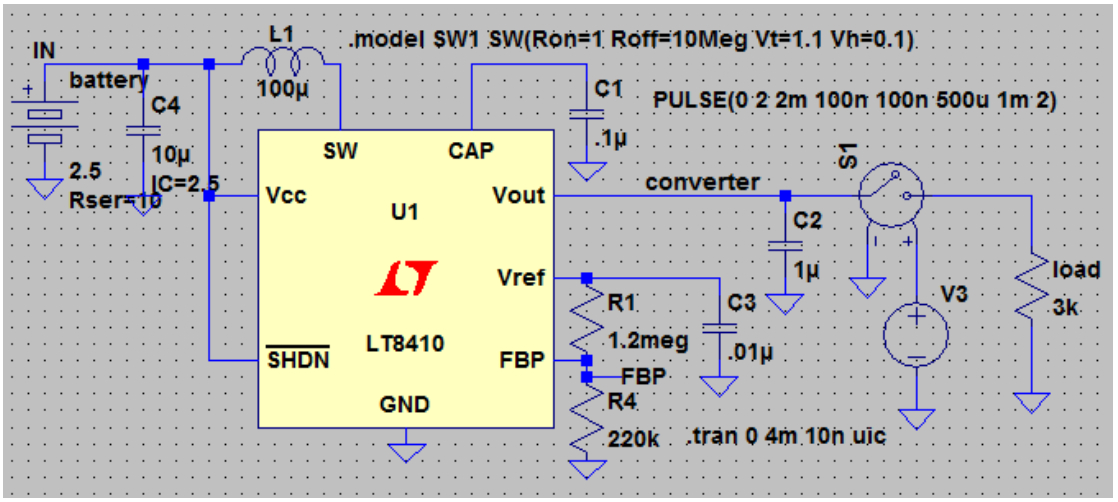


FIGURE A.2: Simulation model for LT1617-1. R1 and R4 is configured for an output at 6 V and with large feedback resistor values for low standby current.

SFE-A impedance simulation

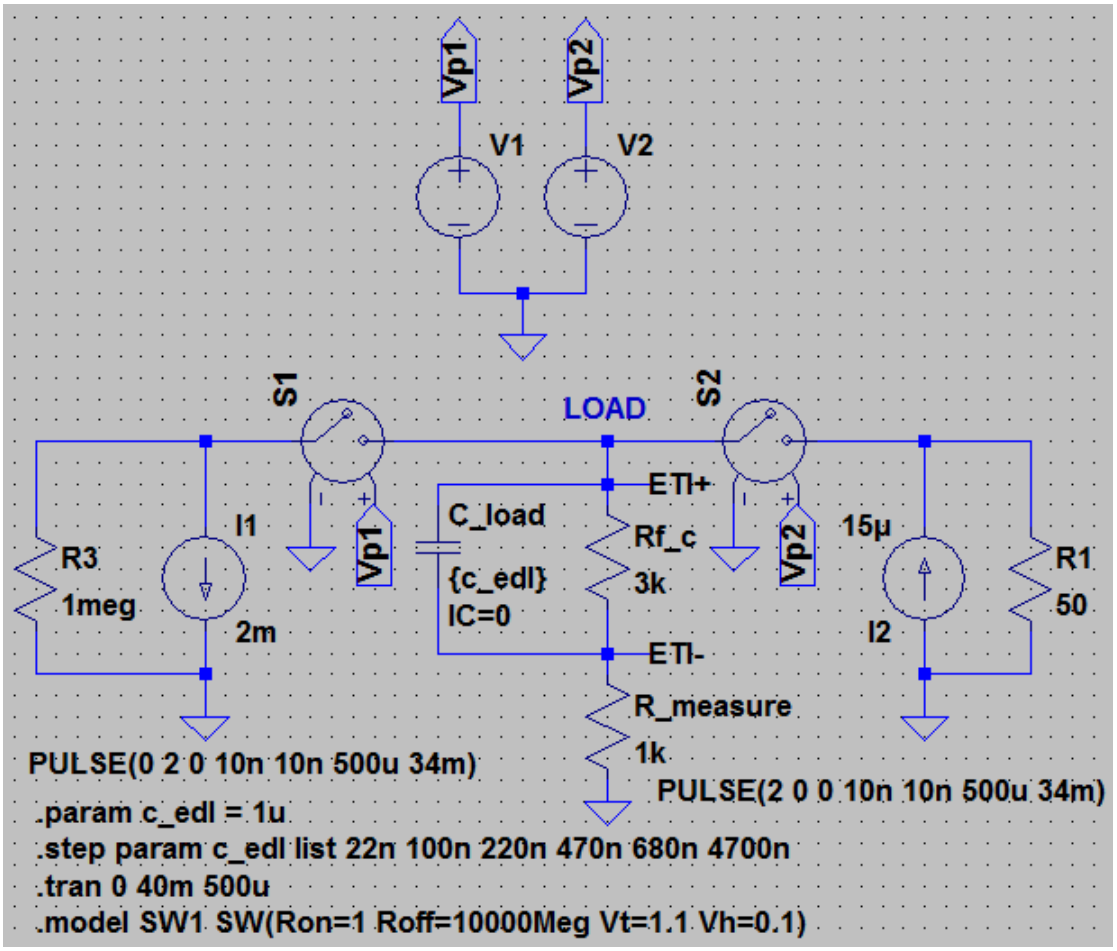


FIGURE A.3: The simulation model used for the anodic discharge

Complete SFE schematic

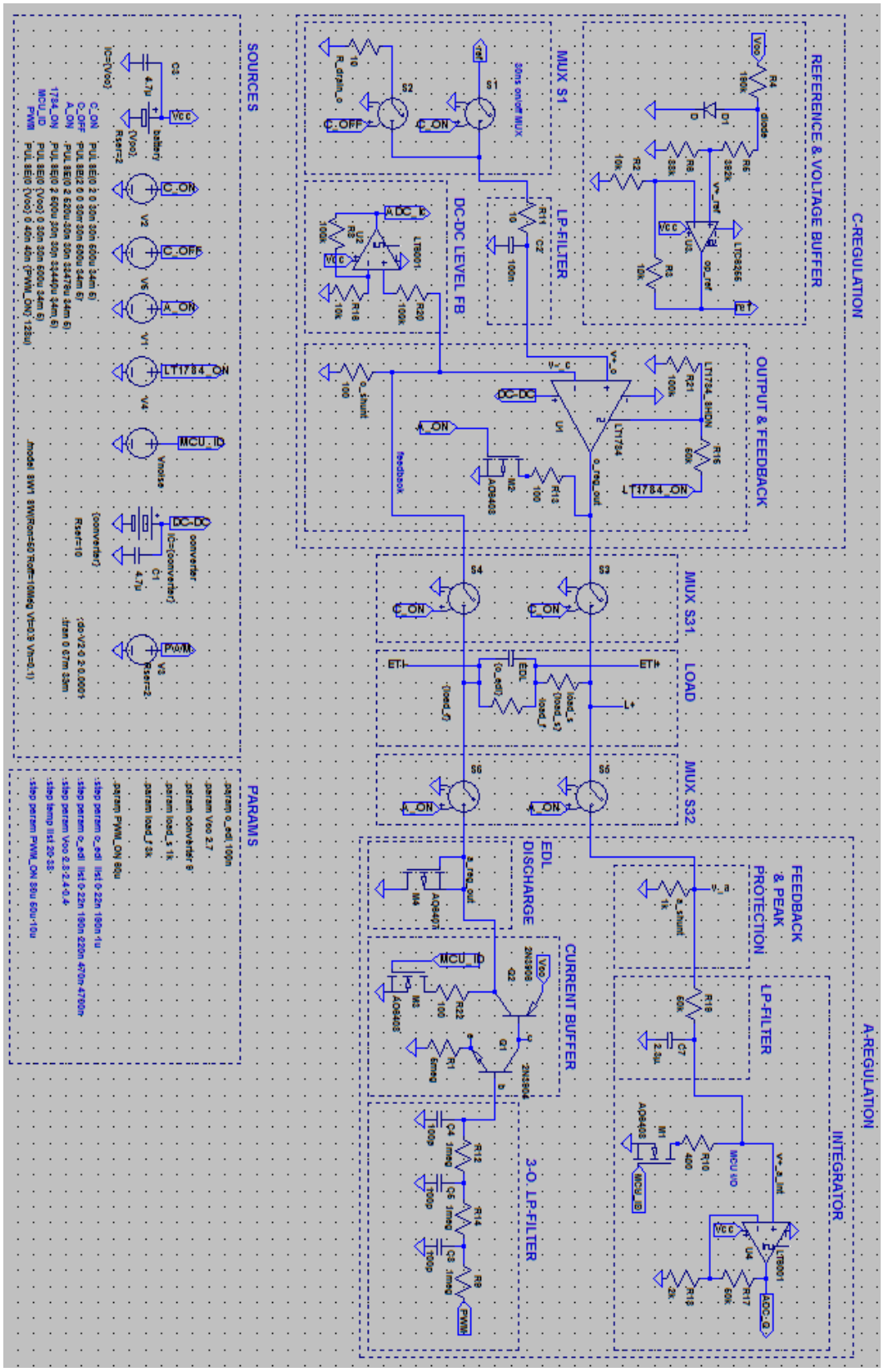


FIGURE A.4: The complete schematic for the SFE module with optimized EDL discharge unit.

SFE-A power consumption

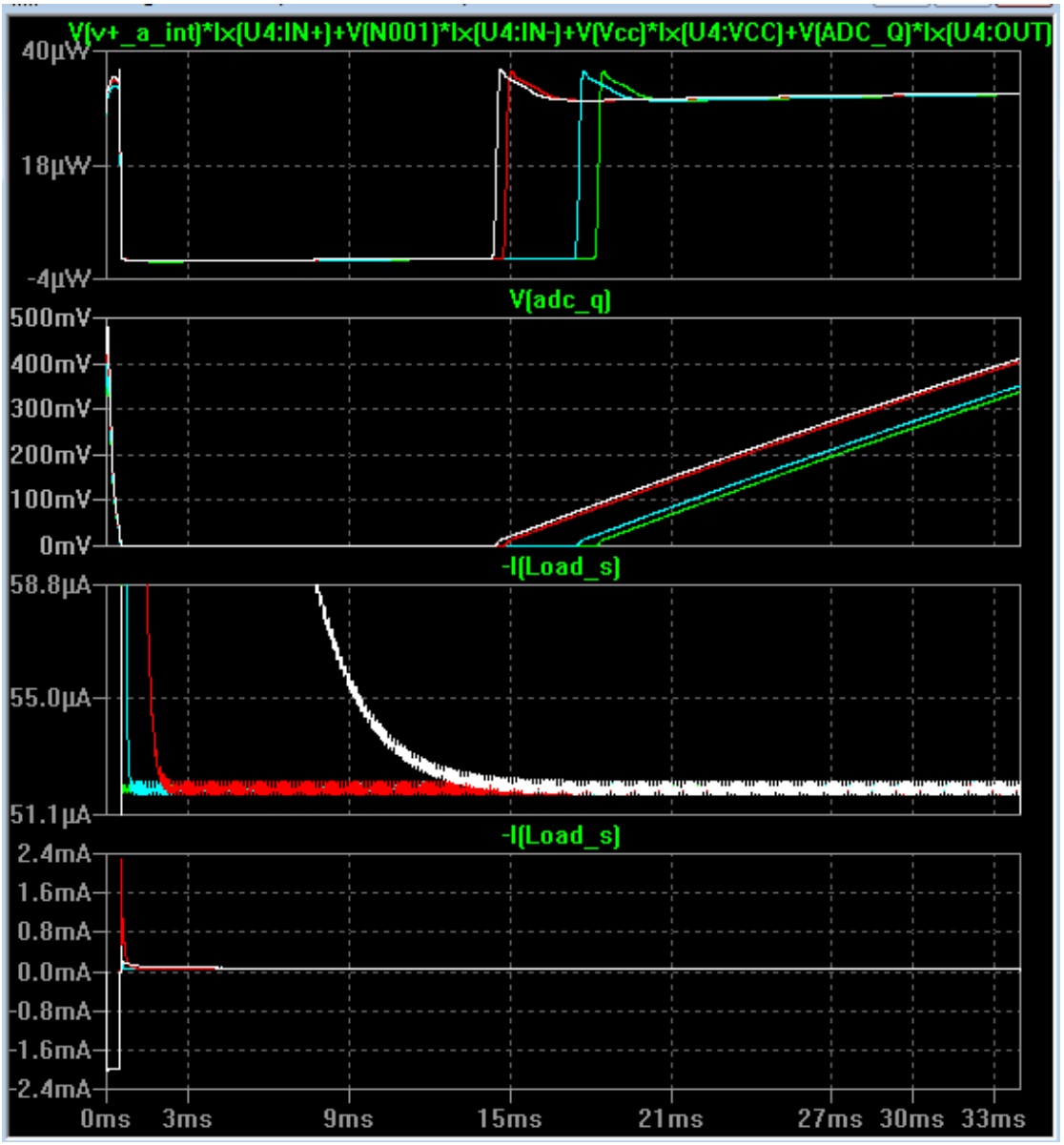


FIGURE A.5: The complete SFE-A module is simulated for EDL values at 0 nF, 22 nF, 100 nF and 1000 nF in green, blue, red and white respectively. The top pane shows the power consumption, where the integrating amplifier is the main consumer together with the current shunt in the R22 resistor. Some power is also lost in the peak limiting measuring resistor, and the average dissipation for these components is 20 µW. The plot V(adc_q) shows the linear output for the integrator, which is scaled to 3 mV nC^{-1}. The red and white line coincides due to the diode drop in D2, which is affecting the larger capacitance more and is not an optimal solution. The two lower graphs shows the EDL discharge and the current bias level.

Appendix B

Electrochemical terminology

A few but important terms in electrochemistry is given here as a reference for concepts discussed in Chapter 2. All terms is taken from the International Union of Pure and Applied Chemistry (IUPAC) Compendium of Chemical Terminology [16] and rewritten with simpler language.

Activating complex is the intermediate structures that are created midway in a reaction from reactant to product. One can say that the activating complex is a "soup" of reactant species with their chemical bounds broken.

Diffusion-controlled reaction is a reaction that is faster than the rate of reactant delivery. The reaction rate is thus controlled by the delivery rate of the reactants. (The term is referred to as a **mass transport limited** reaction in Merill [2])

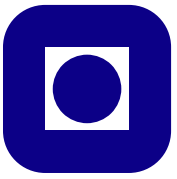
Solvation shell (hydration shell or hydration sphere for aqueous solutions) is the surrounding layer of solvation molecules which acts as a solvent by covering the solute species. A simple example is the sphere of water molecules that sorrounds metal ions in aqueous solutions. The sphere is described by the formula $[M(H_2O)_n]^{z+}$ where the solvation number n idicates the number of solvation molecules (H_2O) attached to the solvent. The electrical charge z is from the ion charge, e.g. 2 for Ca^{2+} and indicates the bond strength between the metal ion and water molecule.

Cyclic Voltammetry (CV) provide details regarding electron transfer kinetics and transport properties of the electrolysis reactions. In a cyclic voltammetry a potential is applied between a working electrode (WE) and a counter electrode (CE), and the resulting current is measured between the working electrode and a reference electrode (RE) (often a silver chloride electrode, Ag/AgCl, due to the close to zero impedance in Na/Cl solutions). The potential over the WE and CE is applied as a triangular ramp with a slope measured in $\mathrm{mV\,s^{-1}}$, which usually makes up the x axis in a CV and is referred to as the scan rate. The y axis is the current from the WE to the RE, and indicates that that a reaction is active with reaction rate equal to the measured slope, given a sufficiently high scan rate [17].

Appendix C

Assignment description

NTNU - Norwegian University of Science and Technology
Faculty of Information Technology,
Mathematics and Electrical Engineering
Department of Engineering Cybernetics



Master Thesis

Student Name: Lars Lyse Moen

Course: Engineering Cybernetics

Title (Norsk)): Design og implementasjon av en elektrisk nervestimulator

Title (English): Design and implementation of an electrical nerve stimulator

Supervisor: Associate Professor Øyvind Stavdahl

Assignment received: 09.01.2014

Assignment delivered: 05.07.2013

Trondheim, August 2014

Description:

Neural stimulation is used for treatment of various medical conditions. In the Peripheral Nervous System (PNS), neural stimulation can be used for drop foot neuroprosthetics (gait abnormality), Vagus Nerve Stimulation (VNS) for epilepsy and depression, and in the Central Nervous System (CNS) for Parkinson's seizure supression. Neural stimulation applied to other conditions as obesity (VNS) is currently subject to heavy research. However, the available devices for such research is developed for human use only. This causes unnecessary complications when testing in smaller animals due to the physical size of the devices, and can further cause biased data due to post operational stress. The motivation for this project is to design a functional circuit, suitable for use in small animal models, that later can be developed into an implantable device used by researchers with ease.

The following tasks were to be completed:

1. Identify major challenges in electrical excitation of neural tissue, and discuss what requirements these challenges imply for the design of a neural stimulator.

2. Perform a detailed requirements analysis. Describe a modular architecture for the stimulator system based on the analysis. The architecture model shall be traceable with respect to the specifications extracted from the analysis, so that each requirement can be traced to the relevant module(s) and vice versa. Define module interfaces explicitly.

3. To the extent possible, perform a detailed system design and implementation, and assess the system's compliance with the specifications at the module and the system level. At this prototype stage, certain requirements may be ignored if properly justified (e.g. the circuits do not need to be miniaturized if this contributes to progress and reduces overall project risk).

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