Merits of SiC MOSFETs for high-frequency soft-switched converters, measurement verifications by both electrical and calorimetric methods

S. Tiwari[a], J. K. Langelid[b], T. M. Undeland[a], and O.-M. Midtgård[a]

[a]Norwegian University of Science and Technology, 7491 Trondheim, Norway;

[b]EFD Induction AS, N-3701 Skien, Norway

ARTICLE HISTORY

Compiled March 12, 2019

ABSTRACT

This paper quantifies the soft switching loss of a 1.2 kV SiC MOSFET module via a calorimetric method in a 78 kW full-bridge resonant inverter switched at approximately 200 kHz. By switching the SiC MOSFET just before the zero crossing of the current (inductive mode) during turn-off and at perfect zero voltage during turn-on, this converter resulted in a square wave output voltage and a sine wave output current as well as yielded an efficiency of roughly 99 %. Then, a simplified laboratory setup, including only a half-bridge series resonant inverter topology with split DC-link capacitors and an LC load, was built such that a real inverter operation was emulated, and thereby, turn-off loss was measured via an electrical method. A discrepancy of approximately 10 % is found between the two loss measurement methods, and the possible source for this difference is discussed. Furthermore, a standard double pulse test was also performed in an inductive clamped buck converter for measuring the hard switching loss via an electrical method. Finally, a comparison of losses obtained from the hard versus soft switched topologies at the same load current was accomplished, which verifies the substantial benefits of soft switching (sine wave current) over hard switching (square wave current). Thus, the merits of SiC MOSFETs for high frequency soft switched converters are demonstrated, which is the main contribution of this paper.

KEYWORDS

Silicon Carbide (SiC); MOSFET; Resonant converter; Conduction losses; Switching losses; Soft switching; Hard switching; Efficiency

CONTACT S. Tiwari. Email: subhadra.tiwari@ntnu.no

1. Introduction

In the medium voltage class, 1.2 kV - 1.7 kV, silicon (Si)-based power devices, particularly, Si IGBTs, have been the primary choice for power electronic devices for the last several decades. In fact, Si MOSFETs exhibit high on-state losses in this voltage class, impeding them from being commercially available. Typically, the highest operating frequency of the state-of-the-art Si IGBTs for soft switched applications is 100 kHz [1]. However, when switched above a certain frequency, the on-state loss of a Si IGBT increases with an increase in frequency because the time required for it to return to deep saturation is not sufficient; therefore, dynamic conduction loss occurs [2]. For instance, in [3], such a phenomenon is shown to be dominant when the switching frequency is above 30 kHz.

On the other hand, silicon carbide (SiC)-based power devices have demonstrated significant potential, especially in high voltage, high efficiency, high power density, and high temperature areas where Si devices confront some fundamental performance boundaries. This is primarily because of the inherent limitations of Si material properties over those of SiC [4–6]. Employing SiC, unipolar devices, such as power MOSFETs, are feasible in the same or higher voltage classes. Indeed, SiC has a 10 times higher breakdown electric field compared to Si, enabling devices with lower on-state losses, potentially lower by a factor of 1/500 to 1/1000, than those for Si at the same voltage ratings [7]. In addition, SiC unipolar devices do not exhibit a tail current. Nonetheless, the on-state losses depend only on the junction temperature and not on the switching frequency for these majority carrier devices [3], which are the obvious reasons for their preference in high frequency soft switched operations, such as high power LLC resonant type and SMPS applications.

Considering the facts about unipolar and bipolar devices discussed in this section, this paper investigates the switching performance of a 1.2 kV half-bridge SiC MOSFET module, which is different from the standard SiC MOSFET module, described in Section 2. There are several publications on loss measurements with the hard switching of devices [8,9]; conversely, only a few publications exist regarding soft switching [2,10–12]. This paper examines the chosen device under both hard and soft switching conditions. Such a comprehensive investigation of the SiC MOSFET module has not been presented before to the best of the authors' knowledge. Illustrating the importance of switching slightly above the resonance, this paper

quantifies the loss in a 78 kW full-bridge resonant inverter switched at approximately 200 kHz via the calorimetric method discussed in Section 3. Section 4 quantifies the turn-off loss in a simplified laboratory setup via an electrical method. Here, the central intent is to delineate the importance of using an appropriate inverter topology for the correct assessment of switching loss. Apart from this, the turn-off losses imposed in the SiC MOSFET by the two chosen topologies are compared. The results illustrate a clear message that even at the same switching current, the resonant converter has significant advantages over the hard switched one, which is evaluated for the first time in this paper as one of the main contributions. Thereafter, a summary of the measurement results is presented along with a discussion in Section 5. Partly, this section compares the soft switching energy loss measured by two methods as another main contribution of this work. Finally, Section 6 lists the major conclusions.

2. Device under study

A 1.2 kV SiC MOSFET module, FCA150XB120, from Sanrex is the device under test (DUT) in this study. Both the MOSFET and the diode chips are fabricated on a single chip in this module, so this MOSFET is also called DioMOS, the concept of which was proposed in 2011 [13]. On the other hand, in a standard SiC MOSFET module, a MOSFET and anti-parallel diode chips are fabricated separately. Table 1 shows the major differences between the selected SiC MOSFET module and the standard SiC MOSFET module (CAS120M12BM2) as specified in the respective data sheets [14,15]. Note that each of these modules has similar voltage and current ratings. Compared to Si MOSFETs, SiC devices have a relatively lower gate-to-source threshold voltage ($V_{gs,th}$). Though the input and output capacitances are lower in SiC, dv/dt is higher. Accordingly, suficient charge can be coupled to the gate loop through the Miller capacitance during turn-off. If a negative gate voltage and a closed couple driver layout are not in place, this coupled charge can easily exceed the $V_{gs,th}$ boundary and cause malfunction of the device. However, the data sheet of the DioMOS indicates relatively higher $V_{gs,th}$ compared to the standard SiC module, which is particularly attractive from an application standpoint. Authors believe that once these devices are mass produced, the prices become moderate and all applications will consider using them. Currently, these devices are used in high-end applications, such as induction heating equipment, which is presented in this work.

Table 1.: Major differences between a SiC DioMOS and a standard SiC MOSFET module.

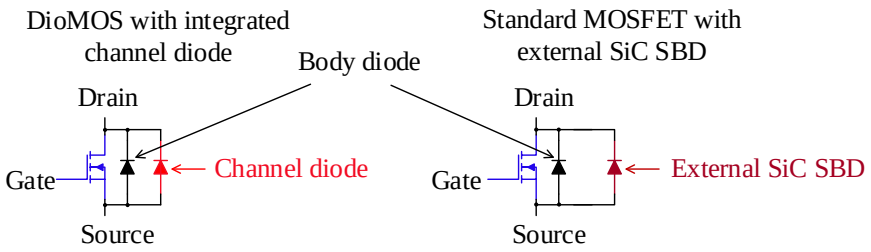
Parameters / Module	DioMOS FCA150XB120, Sanrex	Standard SiC MOSFET CAS120M12BM2, Wolfspeed
$V_{gs,th}$ (V)	4.5	2.6
$R_{ds,on}$ $(m\Omega)$	5.3 @ I_{ds} = 150 A, V_{gs} = 20 V	13 @ I_{ds} = 120 A, V_{gs} = 20 V
$R_{th,jc}$ (°C/W)	0.120	0.125
Bonding	Solder	Wire
Module package size	30 x 93 x14	62 x 106 x 30

(a) DioMOS module. (b) Standard SiC MOSFET module.

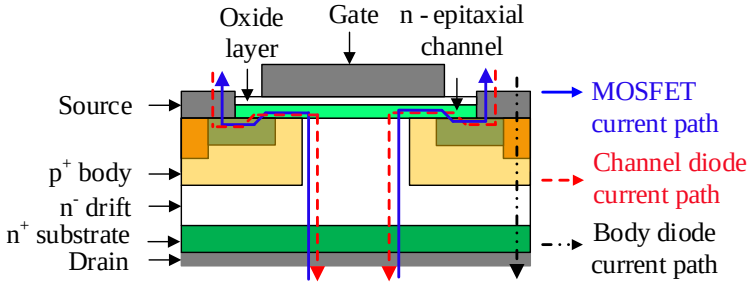
Figure 1.: Photographs of DioMOS and standard SiC MOSFET modules.

Also listed in the Table 1 are $R_{ds,on}$, the on-state resistance, and $R_{th,jc}$, the junction-to-case thermal resistance of the MOSFET. In addition, the package size of the former module is smaller than that of the latter module because the external anti-parallel diode chip paired with the MOSFET chip is not necessary [13]. Moreover, the solder bonding technique is employed for the former module, whereas that for the latter is the wire bonding type. Fig. 1 shows photographs of the DioMOS and standard SiC MOSFET modules. Fig. 2 a) shows the circuit symbols for the DioMOS versus standard SiC MOSFET, and Fig. 2 b) shows a cross-sectional view of the SiC DioMOS [18].

Compared to the standard vertical power MOSFET, the device structure is mostly similar in the DioMOS, except that the latter consists of an ultra-thin, highly doped n - type epitaxial layer and a highly doped p^+ - body region. Different possible current paths are shown in Fig. 2 b), where the arrows in solid blue, dashed red and dash-dot-dot black legends correspond to the MOSFET, channel diode and body diode current paths, respectively. The current paths in the DioMOS, namely, the MOSFET and body diode current paths, are exactly identical to those in the standard power MOSFET. Nonetheless, there exists an additional current path through the channel diode in the DioMOS.



(a) DioMOS with an integrated channel diode and standard MOSFET with an external SiC SBD. The channel diode of the SiC DioMOS functions almost the same as the external SiC SBD.



(b) A cross-sectional view of the SiC DioMOS with the thin channel layer. It has a higher doping concentration of the channel layer and the body region compared to the standard SiC MOSFET.

Figure 2.: a) Circuit symbols showing the DioMOS versus standard SiC MOSFET. b) A SiC DioMOS structure showing the current paths through the MOSFET, channel diode and body diode.

3. Calorimetric loss measurement in a full-bridge resonant inverter

In the following section, a typical system configuration of a voltage-fed series resonant generator for induction heating application, as depicted in Fig. 3, is evaluated. Subsection 3.1 introduces the application along with its operating principle. Further, the importance of switching above the resonance is illustrated through current commutation sequences using MATLAB simulation in Subsection 3.2. Finally, in Subsection 3.3, the calorimetric loss measurement of the inverter part is presented to find the merits of using SiC MOSFETs for such an application.

3.1. System configuration and working principle

Before delving into the working principle of induction heating welders, it is important to discuss the system configuration considered in this study. As seen in Fig. 3, the voltage source inverter consists of 2 half-bridge SiC MOSFET modules with anti-parallel diodes, the DC

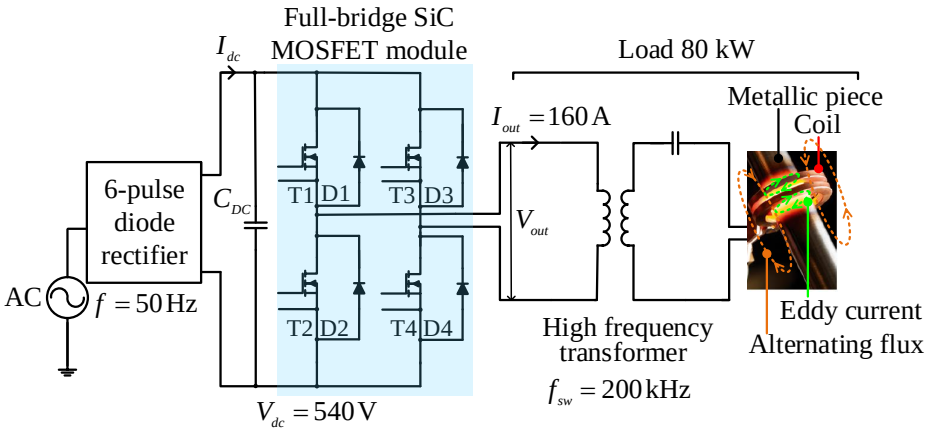


Figure 3.: A complete schematic diagram of the experimental setup for induction heating application. A compensation capacitor is in series with the load inductor (together they act as a current source) and is fed by the voltage source inverter. A metallic piece is placed inside the coil, encompassing the magnetic field without touching the coil as a contactless heating process. The input power of the inverter is measured in the DC-link (V_{dc} is measured by a precision voltmeter and I_{dc} by an LEM current sensor).

power for which is fed through a six-pulse diode rectifier connected to a 400 V, 50 Hz power supply. The abbreviations used in the schematic are as follows. I_{dc}: DC-link current, V_{dc}: DC-link voltage, V_{out}: output voltage and I_{out}: output current. The load is composed of a compensating capacitor, a heating coil, and a metallic piece to be welded. Basically, when the coil is subjected to a high frequency sinusoidal current generated from the inverter, a time-varying magnetic field is induced in it. Consequently, the metal piece is heated by two physical phenomenons, eddy currents and magnetic hysteresis. Eddy currents oppose the magnetic field the work piece is subjected to and produce heating via the Joule effect, and this is the primary heat source. Furthermore, the magnetic field causes dipoles of the ferromagnetic material to oscillate when the poles change their polar orientation every cycle, thus creating an additional heat due to friction referred as hysteresis loss. Depending on the application, the AC frequency is controlled to regulate the penetration depth into the work piece. SiC MOSFETs have potential to switch extremely fast and are very promising components for next generation high frequency induction heating generators. By utilising the benefit of the skin effect, these generators can be used for surface heating of relatively small parts or tubes with small diameters, where only a thin layer of the surface should be hardened or welded.

3.2. *Inductive versus capacitive mode of switching - Consequence in terms of loss*

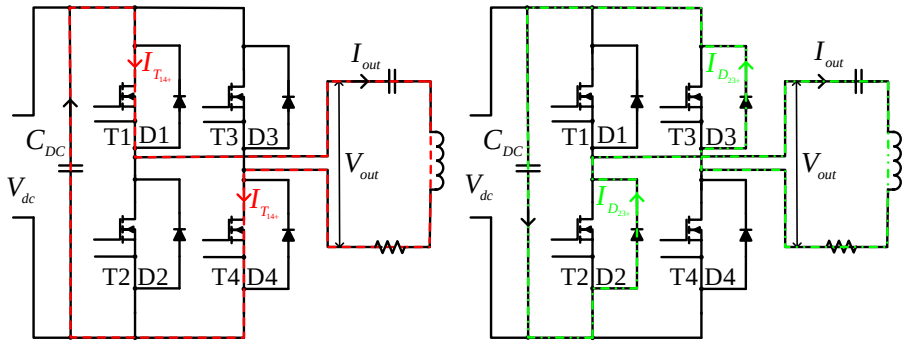
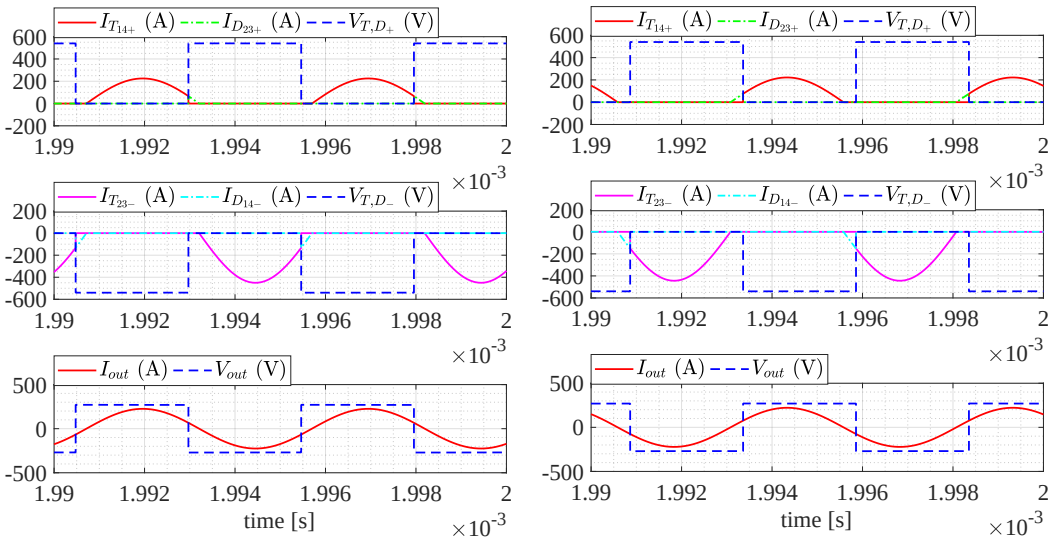


Figure 4.: Exemplification of the current flow during the positive polarity of the load current.



(a) Inductive mode switching, $f_{sw} > f_r$.

(b) Capacitive mode switching, $f_{sw} < f_r$

Figure 5.: Illustration of inductive and capacitive switching modes in a series resonant converter. In the former mode, the turn-on of diodes and turn-off of switches are hard, but the turn-off of diodes and turn-on of switches are soft. However, the converse is true in the latter mode, leading to a higher switching loss, particularly that from the reverse recovery of diodes. This is why the former mode is adopted in this paper over the latter.

When a converter is switched at resonant frequency (f_r), the maximum power can be transferred. Nevertheless, the real-world system has a very low chance to operate at perfect resonance because the focal point can shift due to small changes in the load or subtle inaccuracies in the control parameters. As a consequence, in normal operation, the converter works

slightly above or below the resonance. Therefore, this subsection aims to study the sequence of the commutation process during the inductive (above resonance) versus capacitive (below resonance) switching modes. Thus, the full-bridge inverter configuration, shown in Fig. 3, is simulated in MATLAB. The inputs for simulation are as follows: V_{dc} = 540 V, the resistance of the metallic piece is chosen such that I_{out} = 160 A, and the inductance of the coil and compensating capacitance are tuned to acquire the desired f_r. Fig. 4 shows the current flow during the positive polarity of the load current, where the current through transistors T1 and T4 is labelled as $I_{T_{14+}}$ and that through D2 and D3 is marked as $I_{D_{23+}}$. In a similar manner, $I_{T_{23-}}$ and $I_{D_{14-}}$ are the currents in the respective transistors and diodes during the negative polarity of the load current, as symbolised in the simulated waveforms presented in Fig. 5.

The plots show that while operating above the resonance (Fig. 5 a), diode turn-on and switch turn-off feature hard switching, while diode turn-off and switch turn-on exhibit soft switching. While operating under the resonance (Fig. 5 b), on the other hand, the converse of the former sequences holds true. The forward recovery of the diode is much smaller compared to the reverse recovery, so switching slightly above the resonance is preferable (to avoid turn-off losses associated with the diodes), and this approach is adopted in this paper.

3.3. Laboratory measurements

First, it is essential to highlight that a low inductive switching loop is the key factor for utilising the fast switching potential of a SiC MOSFET and maintaining the safety, particularly during failure. Hence, a DC-link busbar is constructed with a stripline-terminated capacitor, as depicted in Fig. 6. The switching frequency is fixed to 187 kHz, and the inverter losses are measured calorimetrically at approximately 78 kW of input power. Fig. 7 displays the oscilloscope waveforms with the output voltage and current. In the calorimetric method, the inverter is placed over the water-cooled heat sink, assuming that all the heat dissipated by the inverter is removed through the cooling system. When switched just above the resonance, the turn-on loss is absent (details explained in Section 3.2), thus the total loss comprises the turn-off switching loss and conduction loss. Thereafter, by subtracting the conduction loss from the total loss, the turn-off loss is computed. Various electrical parameters, namely, I_{dc}, V_{dc}, and I_{out}, thermal parameters, namely, the inlet and outlet water temperatures (T_{in} and T_{out}, respectively), and the water mass (m) are monitored and listed in Table 2.

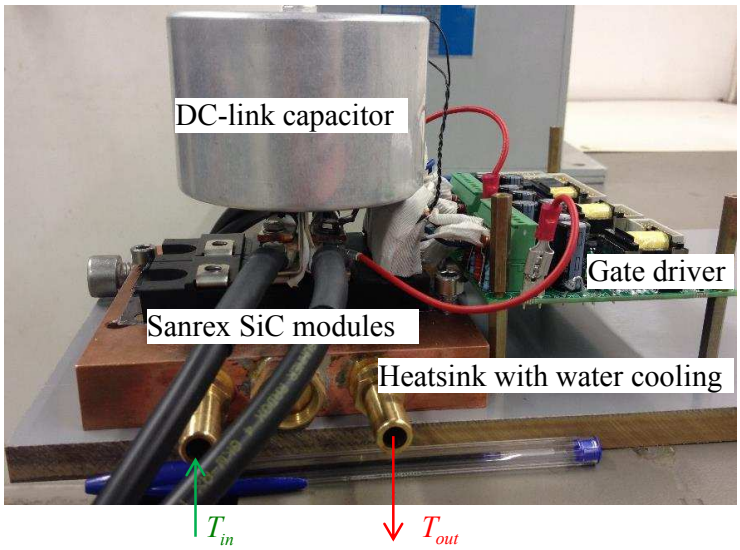


Figure 6.: Part of the experimental setup showing a low inductive busbar connection for a full-bridge inverter with a water-cooled heat sink for calorimetric loss measurement.

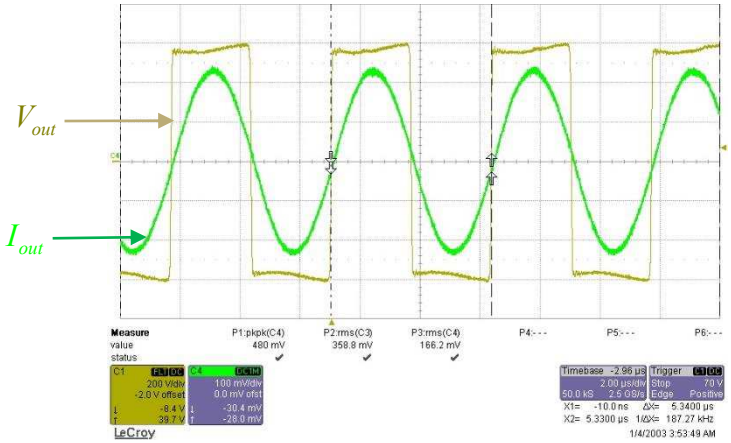


Figure 7.: Illustration of a sample of inverter output voltage and current with a full PWM control scheme. The gate voltage is + 20 V / - 5 V, and the gate resistance is 2.85 Ω.

Table 2.: Summary of the measured parameters at 78 kW input power.

Measured parameters	I_{dc} (A)	V_{dc} (V)	I_{out} (A)	T_{in} (°C)	T_{out} (°C)	m (g/min)
Values	142.8	545	160.3	15	17.5	2.990

Table 3 presents a summary of the calculated parameters. Using Equations 1 to 7, the corresponding parameters in each row are computed. The abbreviations used in the equations

Table 3.: Summary of the calculated parameters for approximately 78 kW of input power.

Calculated parameters	Values	Equations	Eq. no.
P_{in} (kW)	77.82	$P_{in} = V_{dc} \cdot I_{dc}$	1
Q (W or J/s)	521.5	$Q = m \cdot s \cdot (T_{out} - T_{in})$	2
η (%)	99.33	$\eta = \frac{P_{in} - Q}{P_{in}}$	3
P_{cond} (W)	89.93	$P_{cond} = \left(\frac{I_{out}}{\sqrt{2}}\right)^2 \cdot R_{ds,on}$	4
P_{sw} (W)	40.44	$P_{sw} = \frac{Q}{4} - P_{cond}$	5
$E_{off-sp-calori}$ (μJ/A)[a]	3.60	$E_{off-sp-calori} = \frac{P_{sw}}{f_{sw} \cdot I_{ds}}$	6
ΔT (°C)	15.64	$\Delta T = R_{th,jc} \cdot \frac{Q}{4}$	7

[a]Note that $E_{off-sp-calori}$ is computed for a drain current of 60 A, which is the turn-off switching current in a full bridge.

are as follows: P_{in}: input power of the inverter, Q: total power loss of the inverter, s: specific heat capacity of water (4.186 $J/g/^{\circ}$C), η: efficiency of the inverter, P_{cond}: conduction power loss per switch, P_{sw}: switching power loss per switch, $E_{off-sp-calori}$: specific turn-off energy loss per switch, and ΔT: temperature rise from the junction to the case. The measured efficiency of the inverter is approximately 99 %, the conduction loss per switch is 89.93 W with $R_{ds,on}$ being 7 $m\Omega$ (at the operating temperature), and the temperature rise is 15.64 °C (at the given $R_{th,jc}$ of 0.120 °C/W).

3.4. Accuracy analysis

As ΔT and m (in Equation 2) can be the sources of inaccuracies in calorimetric loss measurement method, the inlet and outlet temperatures are measured using an analogue thermometer with $\pm$ 0.05 °C accuracy. For the water flow measurement, first, the outlet water is run into a bucket over a specified time (2 minutes), second, the water in the bucket is measured via a postal weight with 0.01 kg resolution. Thus, the volumetric flow is calculated by dividing the weight of water and measurement time. Note that the water flow is controlled by connecting the inlet of heatsink directly to water faucet (the temperature of water is less than room tem-

perature, RT). The air temperature close to the heatsink is measured by pt100 with resolution of < 0.01 °C and was found to be $\leq$ RT all the time.

For the highly efficient converters, it is challenging to achieve accurate ΔT measurements with standard flow rates as that used in industrial applications. Therefore, to maintain an adequate measurement accuracy, ΔT should be kept high, thus it is essential to maintain a low water flow rate without sacrificing a good heat transfer coefficient from water to heatsink. This is achieved via smaller cross-sectional area of cooling channel in heatsink, which will basically aid increasing the speed of water. Of special note is that the measured data is an average of 10 consecutive recordings for avoiding possible errors.

4. Electrical loss measurement in a half-bridge inverter

In this section, the significance of using an appropriate inverter topology for the correct assessment of the switching loss is investigated. Two different topologies studied include a half-bridge series resonant inverter with split DC-link capacitors and an LC load, which has a sine wave output current, and a half-bridge inductive clamped load without split DC-link capacitors. For a fair comparison between the topologies and the switching losses, the same gate driver board as that used during the calorimetric loss measurement method is employed during the electrical method.

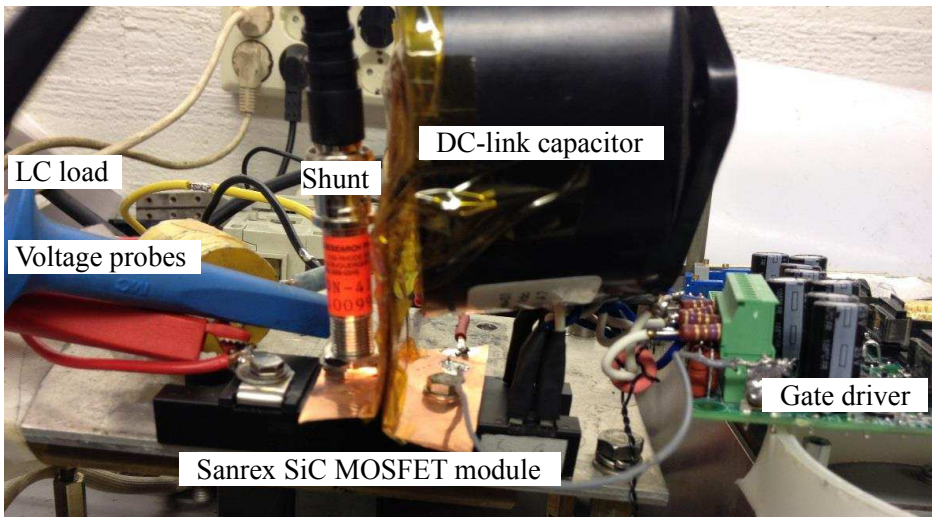
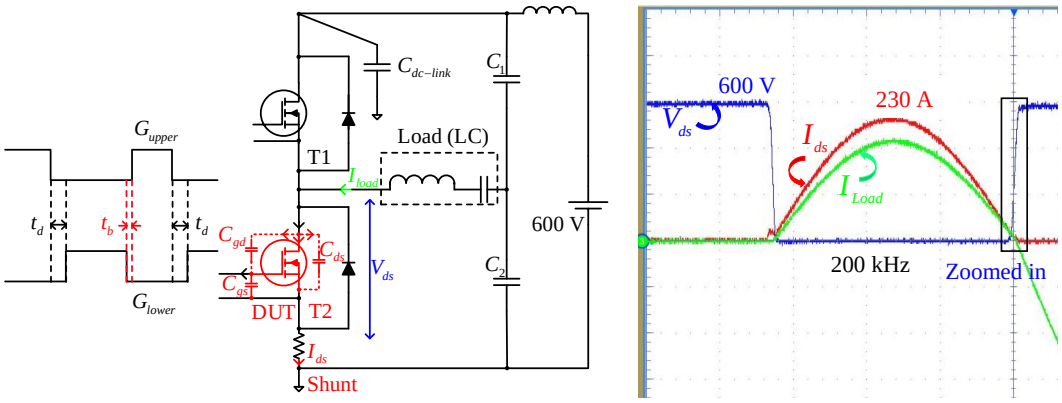


Figure 8.: Laboratory setup with a low inductive DC-link. The drain current and drain voltage are measured by a high bandwidth, low inductive shunt, and a differential probe.

To be specific, the same gate voltage (+ 20 V / - 5 V) and gate resistance (2.85 Ω) are maintained in each hardware setup. Additionally, the gate driver board is assembled at similar distances in each method, which is clearly visible in Fig. 6 and Fig. 8. For realising a low switching loop stray inductance, the DC-link is made with a planar busbar, except for the termination parts needed to facilitate the module connection. A current viewing resistor (CVR), also called a shunt resistor, SSDN-414-01 (400 MHz, 10 mΩ) from T & M research [19], is used for measuring the drain current. The CVR is mounted directly on one of the screw terminals of the SiC MOSFET module, as illustrated in Fig. 8.

4.1. Split DC-link capacitors with an LC load

As discussed in Subsection 3.2, in an inductive switching mode, there are losses associated with the turn-off of the active switch and the forward recovery of the diode. As the latter part is negligible, the only significant loss is in the device that turns off.



(a) Half-bridge circuit with split DC-link capacitors and an LC load.

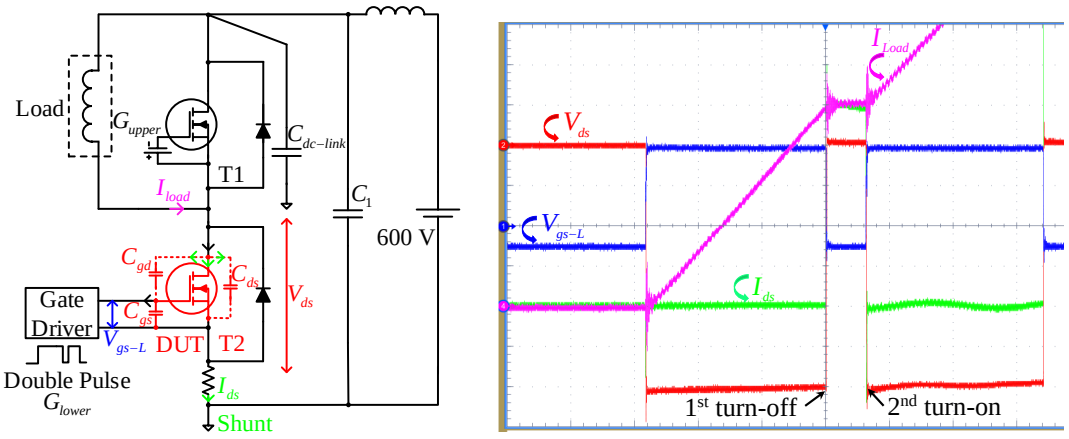
(b) Typical soft switched waveforms.

Figure 9.: Illustration of a circuit diagram for soft switching loss measurement, where a lower transistor (T2) is the DUT and the load is formed by a series inductor and capacitor in a), and an example of a typical soft switched waveform, where the turn-off instant is the key point of interest and is annotated by a rectangle in b). During the turn-off of T2, current flows through its channel and charges the output capacitor (C_{ds} and C_{gd}). A shunt resistor measures the summation of these two currents, marked as (I_{ds}). Note that only the MOSFET channel current causes loss in the device, but it is not possible to measure the current separately in the lab.

To emulate the real inverter operation, as shown in Section 3, a simplified laboratory setup is built, comprising only a half-bridge series resonant inverter topology with split DC-link capacitors and an LC load, as shown in Fig. 8; the schematic diagram is shown in Fig. 9 a), and the output voltage and current waveforms are shown in Fig. 9 b). Noteworthy are the shapes of the drain voltage (V_{ds}) and load current (I_{Load}), which are square and sine waves, respectively, replicating those in a real application circuit.

4.2. Single DC-link capacitor with an inductive clamped load

In a typical power semiconductor data sheet, only the hard switching loss is provided [14–17]. However, the circuit parasitics and topology impact the measured loss. In the quest to keep the parasitic parts constant both internally in the device and externally in the busbar and connections, the same experimental setup as employed in Subsection 4.1 is used for hard switching loss measurement, whereas the load is altered with an inductor clamped across the upper MOSFET, and the DC-link capacitors are not split any more, as shown in Fig. 10.



(a) Clamped inductive load test circuit.

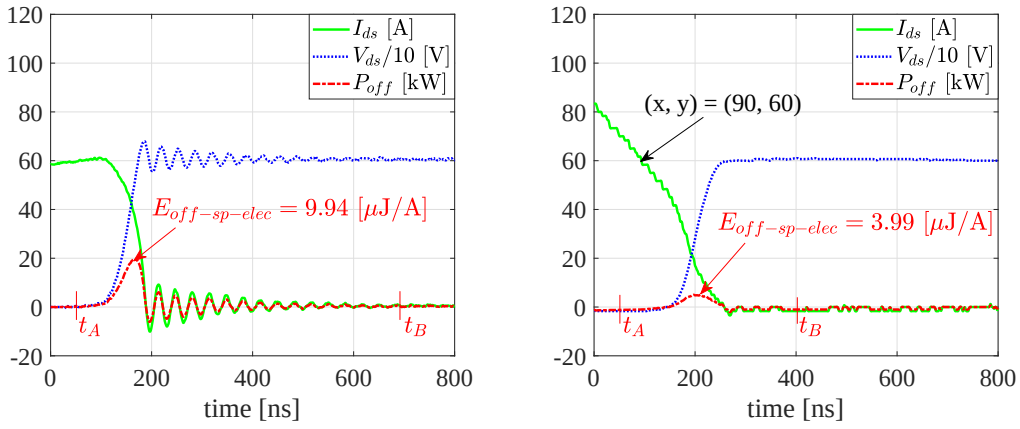
(b) Example of typical DPT waveforms.

Figure 10.: Illustration of a circuit diagram for hard switching loss measurement, where a lower transistor (T2) is used to switch a diode-clamped inductive load primarily as a step-down dc-dc converter in a), and an example of a double pulse test waveform, where the key point of interests are the 1st turn-off and 2nd turn-on events, as indicated in b), for analysing the switching performance of the DUT at approximately equal current.

For accessing the stress in the DUT, two pulses are sent, while the gate and source of an upper transistor (T1) is supplied with - 5 V to ensure that it is turned off all the time. Fig. 10 b) displays the typical test waveforms, where the first turn-off (at the end of the first pulse) and the second turn-on (at the beginning of the second pulse) are the key point of interests because the DUT switching transients can be captured under similar voltage and current conditions. The gate voltage (V_{gs-L}), the drain-to-source voltage (V_{ds}), the drain-to-source current (I_{ds}) of transistor T2, and the current through the load inductor (I_{Load}) are indicated in Fig. 10 a) and b). By regulating the width of the first pulse and the DC-link voltage, the desired load current is achieved. Each time, only two pulses are applied, and the DUT is switched only twice; thus, the device junction temperature increase due to switching loss is negligibly small.

4.3. Comparison of switching losses with sinusoidal current versus square shape current

Fig. 11 shows example waveforms illustrating the difference between resonant switching and hard switching. For a fair comparison, these waveforms are recorded at the same load currents (60 A), R_g (2.85 Ω) and V_{gs} (+ 20 V, - 5 V).



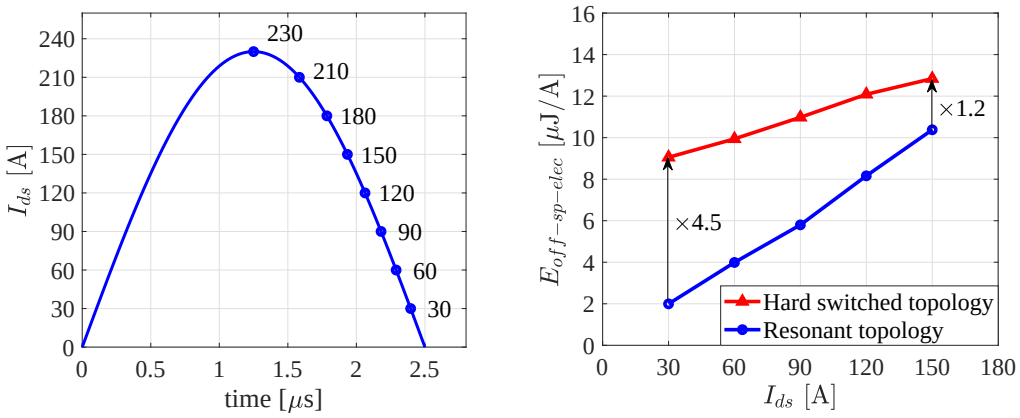
(a) Turn-off transient with sine wave current switching.

(b) Turn-off transient with square shape current switching.

Figure 11.: a) Illustration of turn-off transients under sine wave current and square wave current switching conditions at the same load current. The former exhibit little or no oscillations, while oscillations are present in the latter. Specifically, the turn-off energy loss is 2.5 times lower for resonant topology than that for the hard switched inverter, showing the ample benefit of the former topology and control scheme.

It is clearly visible that the sinusoidal switching waveforms have lower ringing compared to those for the square wave switching. While comparing the switching losses, it is important to show how they are computed. Hence, in this work, the turn-off power (P_{off}) curve is integrated from t_A to t_B, as indicated in Fig. 11 a) and b), and the specific turn-off losses per switch ($E_{off-sp-elec}$) are found to be 3.99 μJ/A for sine wave switching and 9.94 μJ/A for square wave switching at a load current of 60 A.

To acquire a full overview of switching losses at different current levels with the two different topologies, the $E_{off-sp-elec}$ versus drain source current is plotted in Fig. 12 b). It is worth mentioning that in either of the topologies, the required turn-off current level is acquired by adjusting the on-time and the DC-link voltage. To be more precise regarding the resonant switching, the peak value of the load current is fixed at 230 A, and thereafter, the turn-off instants are varied (by adjusting the on-time), as defined in Fig. 12 a). Aside from this, the switching frequency is set to 200 kHz according to the application requirements. Depending on I_{ds}, $E_{off-sp-elec}$ varies from 2 μJ/A to 10.8 μJ/A with the resonant topology and from 9 μJ/A to 12.8 μJ/A with the hard switched topology. Thus, using the hard switching loss for designing thermal management and estimating the power rating of the resonant converter



(a) Definition of turn-off current during soft switching.

(b) Switching loss in hard versus resonant topology.

Figure 12.: a) Illustration of the turn-off current in the soft (resonant) switching case. The peak value of the load current is set at 230 A, and the turn-off instants are varied. b) Comparison of the switching loss between the hard (square wave current) and soft (sine wave current) switching. Switching with square wave current leads to higher turn-off losses, a factor of 1.2 (150 A) to 4.5 (30 A) depending on the load current, compared to that with sine wave current.

Table 4.: Summary of the specific turn-off loss measurements in three different topologies and normalisation with regard to electrically measured loss in a half-bridge resonant inverter.

Case	Inverter Topology	Method	Specific energy loss (μJ/A)	Factor wrt b)
a)	Full-bridge resonant	Calorimetric	$E_{off-sp-calori}$ = 3.60	0.9
b)	Half-bridge resonant	Electrical	$E_{off-sp-elec}$ = 3.99	1.0
c)	Inductive clamped	Electrical	$E_{off-sp-elec}$ = 9.94	2.5

leads to a significant error, as the turn-off switching in the latter occurs at the minimum possible current (lower current regions). The difference in losses between the two topologies is more pronounced towards lower currents, which is mainly because of two reasons. First, at lower current, there is lower dv/dt, which causes the output capacitance of the MOSFET to work better as a turn-off snubber compared to a higher current. Second, the MOSFET channel is closed to current earlier in the turn-off process with lower dv/dt.

5. Summary and discussion

Table 4 summarises the specific turn-off energy loss per switch measured in three different inverter topologies along with the normalisation with reference to the electrically measured loss in a half-bridge resonant inverter. Note that the listed values are measured at the switching current of 60 A, and the gate driving waveforms are maintained as similar in each case for a balanced comparison. The specific energy loss is lower by a factor of 0.9 in case a) and is higher by a factor of 2.5 in case c) compared to that in case b), the respective reasoning of which is enumerated below separately.

Case a) As can be seen from Table 4, the specific energy loss measured via the electrical method is higher by 9.7 % compared to that measured via the calorimetric method. For the sake of explaining this difference, the turn-off process and the measurement method should first be clarified. In either Fig. 9 or Fig. 10, the current routing during the turn-off process is shown. In the electrical loss measurement method, the drain current and the

drain voltage are measured using high bandwidth probes and an oscilloscope. After compensating for possible probe delays, these collected switching waveforms are multiplied and integrated over the defined time limits to obtain the switching energy loss in MATLAB. Looking closely into the turn-off process, the drain current used for the loss calculation is the sum of the following two currents: a) the current passing through the MOSFET channel and b) the current diverted for charging the output capacitance (C_{gd} + C_{ds}). However, the real power loss in the MOSFET is caused by the channel current only because the current that charges the device output capacitor does not generate any Joule heating and should not be accounted for as a part of the turn-off switching loss. The MOSFET channel current cannot be measured separately in the lab, so the electrical approach to loss measurement overestimates the switching energy loss, explaining the reason for the loss differences in question. This is also illustrated through simulation using a physically based device modelling approach in [20,21]. In such a simulation, there is the possibility to measure the current shared by the MOSFET channel and the output capacitor independently.

Case c) As discussed in Subsection 4.3, the sine wave current switching showed a principal advantage over square wave current switching. At an I_{ds} of 60 A, $E_{off-sp-elec}$ during resonant switching is lower by a factor of 2.5 compared to hard switching, as indicated in Table 4. Apparently, the resonant topology showed a much smaller turn-off energy loss compared to hard switched throughout the whole current range, with the advantage being more enhanced towards the lower current region. Moreover, this gives a clear message that the hard-switching losses from the data sheet should not be used when designing a resonant switched converter.

6. Conclusion

The major conclusions derived from this paper are listed below.

i) A resonant full-bridge inverter with SiC MOSFETs yields an efficiency of approximately 99.3 % at a switching frequency of roughly 200 kHz using a calorimetric loss measurement method. For induction heating application, SiC MOSFETs not only fulfil

the application demand but also save energy, thus enabling two benefits.

ii) A simplified measurement setup comprising a half-bridge SiC MOSFET, split DC-link capacitors and an LC load is used for measuring the turn-off loss via an electrical method, which is 9.77 % higher compared to that obtained using a calorimetric method. Two possible reasons for these differences are as follows: First, the drain current through the MOSFET during the electrical measurement is smaller than the measured value because a part of the measured current is charging the MOSFET output capacitor. Second, factors causing losses, for example, forward recovery of free-wheeling diodes, layouts, and wires, are neglected.

iii) Keeping the stray inductance, gate drive resistance, voltage and location the same as those in the soft switching loss measurement setup and changing the load to an inductive clamped type as in a typical double pulse test methodology, the hard-switching loss is measured electrically. The turn-off switching losses between these two topologies are compared, revealing that the resonant (sine wave current) switching technique achieves remarkably lower loss compared to the hard (square wave current) switching operation, a factor of 2.5 times lower at 60 A. Thus, the authors have two recommendations. First, adopt sine wave switching whenever feasible (as per the application) because this reduces the switching loss as well as EMI, which further enables higher switching frequencies, efficiencies, and power densities. Second, use an appropriate circuit topology for the correct assessment of loss, especially for a resonant inverter, where the turn-off is aimed towards the lower current region. Otherwise, estimation of loss for a sine wave switched converter using the measurements from the hard switched topology leads to much higher errors at lower currents compared to higher currents, which potentially entails wrong sizing of the heat sink and limits the power of the converter.

Acknowledgement

The authors would like to thank The Research Council of Norway and 6 industry partners who sponsor this project: EFD Induction, Siemens, Eltek, Statkraft, Norwegian Electric Systems, and Vacon.

References

[1] E. J. Dede, J. Jordan and V. Esteve, "State-of-the art and future trends in transistorised inverters for induction heating applications," Proceedings of the Fifth IEEE International Caracas Conference on Devices, Circuits and Systems, 2004., 2004, pp. 204-211.

[2] J. K. Johansen, F. Jenset and T. Rogne, "Characterization of high power IGBTs with sinewave current," in IEEE Transactions on Industry Applications, vol. 30, no. 5, pp. 1142-1148, Sep/Oct 1994.

[3] P. Ranstad, H. P. Nee, J. Linnér and D. Peftitsis, "An Experimental Evaluation of SiC Switches in Soft-Switching Converters," in IEEE Transactions on Power Electronics, vol. 29, no. 5, pp. 2527-2538, May 2014.

[4] R. Singh and M. Pecht, "Commercial impact of silicon carbide," in IEEE Industrial Electronics Magazine, vol. 2, no. 3, pp. 19-31, Sept. 2008.

[5] J. Millán, P. Godignon, X. Perpiñá, A. Pérez-Tomás and J. Rebollo, "A Survey of Wide Bandgap Power Semiconductor Devices," in IEEE Transactions on Power Electronics, vol. 29, no. 5, pp. 2155-2163, May 2014.

[6] J. Rabkowski, D. Peftitsis and H. Nee, "Silicon Carbide Power Transistors: A New Era in Power Electronics Is Initiated," in IEEE Industrial Electronics Magazine, vol. 6, no. 2, pp. 17-26, June 2012.

[7] M. Östling, R. Ghandi and C. M. Zetterling, "SiC power devices - Present status, applications and future perspective," 2011 IEEE 23rd International Symposium on Power Semiconductor Devices and ICs, San Diego, CA, 2011, pp. 10-15.

[8] K. Vechalapu, S. Bhattacharya, E. VanBrunt, S. H. Ryu, D. Grider, and J. Palmour, "Comparative Evaluation of 15 kV SiC MOSFET and 15 kV SiC IGBT for Medium Voltage Converter under Same dv/dt Conditions," IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. PP, pp. 1-1, 2016.

[9] S. Tiwari, O. -M. Midtgård, and T. M. Undeland, "SiC MOSFETs for future motor drive applications," in 2016 18th European Conference on Power Electronics and Applications (EPE'16 ECCE Europe), 2016, pp. 1-10.

[10] C. Cases, J. Jordan, J. M. Magraner, V. Esteve, E. Dede, E. Sanchis, et al., "Characterization of IGBT devices for use in series resonant inverter for induction heating applications," in Power Electronics and Applications, 2009. EPE '09. 13th European Conference on, 2009, pp. 1-8.

[11] D. Rothmund, D. Bortis, and J. W. Kolar, "Accurate transient calorimetric measurement of soft-switching losses of 10kV SiC MOSFETs," in 2016 IEEE 7th International Symposium on Power

Electronics for Distributed Generation Systems (PEDG), 2016, pp. 1-10.

[12] S. Tiwari, J. K. Langelid, O. -. Midtgård and T. M Undeland, "Soft switching loss measurements of a 1.2 kV SiC MOSFET module by both electrical and calorimetric methods for high frequency applications," 2017 19th European Conference on Power Electronics and Applications (EPE'17 ECCE Europe), Warsaw, 2017, pp. P.1-P.10.

[13] M. Uchida, N. Horikawa, K. Tanaka, K. Takahashi, T. Kiyosawa, M. Hayashi, et al., "Novel SiC power MOSFET with integrated unipolar internal inverse MOS-channel diode," in Electron Devices Meeting (IEDM), 2011 IEEE International, 2011, pp. 26.6.1-26.6.4.

[14] "FCA150XB120 (DS1) Preliminary Datasheet," Sansha Electric Mfg. Co., Ltd, 2014.

[15] "CAS120M12BM2 Datasheet," Cree, Inc., 2014.

[16] "BSM120D12P2C005 Datasheet," Rohm, Inc., 2014.

[17] "SKM400GB125D Datasheet," Semikron, Inc., 2007.

[18] A. Ohoka, N. Horikawa, T. Kiyosawa, H. Sorada, M. Uchida, Y. Kanzawa, et al., "40 mΩ / 1700 V DioMOS (Diode in SiC MOSFET) for High Power Switching Applications," in Materials Science Forum, 2014, pp. 911-914

[19] "Current Viewing Resistor (CVR)," T & M Research Products, Inc.

[20] Y. Xiong, S. Sun, H. Jia, P. Shea and Z. John Shen, "New Physical Insights on Power MOSFET Switching Losses," in IEEE Transactions on Power Electronics, vol. 24, no. 2, pp. 525-531, Feb. 2009.

[21] X. Li, L. Zhang, S. Guo, Y. Lei, A. Q. Huang and B. Zhang, "Understanding switching losses in SiC MOSFET: Toward lossless switching," 2015 IEEE 3rd Workshop on Wide Bandgap Power Devices and Applications (WiPDA), Blacksburg, VA, 2015, pp. 257-262.