REV 1.1

TECHNICAL DESCRIPTION

iTRAX03-S GPS Receiver

This document describes the electrical connectivity and main functionality of the iTRAX03-S hardware

September 6th, 2005

Fastrax Ltd.

CHANGE LOG

Rev.	Notes	Date
0.1	Preliminary documentation	2004-11-09
0.2	Updated GPIO behavior, added chapter 5.	2005-04-19
1.0	Added Application Board documentation	2005-08-31
1.1	Added pin description table in chapter 7.	2005-09-06

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COMPLEMENTARY READING

The following reference documents are complementary reading for this document. All operating and firmware related documentation is also available at the iSuite^{TM} 3 SDK web site ***isuite.fastrax.fi***

Ref. #	File name	Document name
1		iTrax03 Prochure
2	PRO_NMEA.html	Fastrax NMEA Protocol Specification
3	uN8130T_UM.pdf	uN8130 User's manual

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1.   GENERAL DESCRIPTION

The iTrax03-S is an OEM GPS receiver module, which provides the iTRAX03 (*ref #1*) receiver functionality with an internal 8Mbit Flash memory and which has a tiny form factor 16.2x18.8mm.

The module provides complete signal processing from antenna to serial data output in either NMEA messages or in proprietary iTALK binary protocol. A second serial port is also available for custom purposes. The module requires a dual power supply at +2.7…+3.3V and GPS antenna input signal. Serial data and all I/O signals levels are CMOS compatible.

The iTRAX03-S module interfaces to the customer's application via versatile I/O and supports also several peripherals for iSuite3 SDK users including a timer input, a pulse measurement input, a high speed SPI-bus and a MMC bus. All the peripherals have a shared functionality for SDK users with the General Purpose Input/Output (GPIO).

The antenna input supports passive and active antennas and provides also an internally generated antenna bias supply.

This document describes the electrical connectivity and main functionality of the iTRAX03-S hardware.

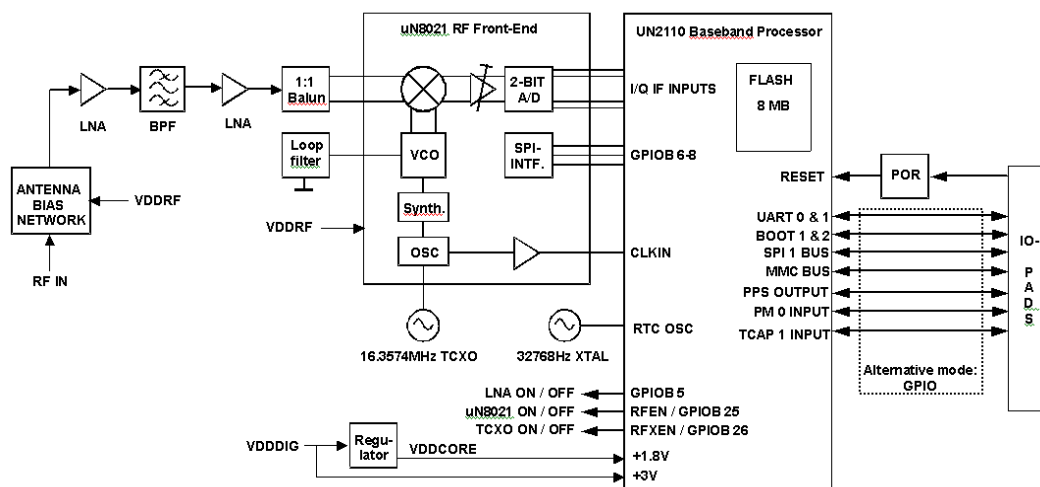## 1.1 Block diagram

Figure 1   Block diagram

1.2 Frequency Plan

Clock frequencies generated internally at the iTRAX03 receiver:

- 32768 Hz real time clock

- 16.3574 MHz master clock

- 1574.40 MHz local oscillator of the RF down-converter

2.   SPECIFICATIONS

2.1 General

Table 1   General Specifications

Receiver	GPS L1 C/A-code, SPS
Channels	12
Update rate	1 Hz default (fix rate configurable)
Supply voltage range, VDDRF	+2.7V…+3.3 V, low ripple 2mV(RMS) max.
Supply voltage range, VDDDIG	+2.7V…+3.3 V
Power consumption	100 mW typical (without Antenna bias)
Antenna net gain range	0…+32 dB
Antenna bias voltage	Same as VDDRF
Antenna bias current	Must be limited externally by VDDRF supply to 150mA max.
Operating and storage temperature	-40ºC…+85ºC
Serial port configuration	Port 0: NMEA (default), iTALK optional Port 1: iTalk
Serial data format	8 bits, no parity, 1 stop bit
Serial data speed	600, 1200, 2400, 4800, 9600, 14400, 19200, 28800, 38400, 57600, 115200, 230400, 460800, 921600 baud. NMEA: 4800(default), iTalk: 115200(default).
I/O signal levels	CMOS compatible: low state 0.0…0.3xVDDDIG; high state 0.7…1.0xVDDDIG
I/O sink/source capability	+/- 4 mA max.
PPS output	1 pulse per second (*ref 2*), CMOS compatible
Accessory I/O (shared functionality with GPIO)	Capture Timer, Pulse Measurement Input, SPI-bus, MMC bus

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2.2 Absolute maximum ratings

Table 2 Absolute maximum ratings

Item	Min	Max	unit
Operating and storage temperature	-40	+85	ºC
Power dissipation		500	mW
Supply voltage, VDDDIG	-0.3	+3.6	V
Supply voltage, VDDRF	-0.3	+3.6	V
Current on any I/O pin except antenna input	-30	+30	mA
Current output on antenna input	0	+150	mA
Input voltage on any input connection	-0.3	VDDDIG + 0.3	V

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3.   OPERATION

3.1 Operating modes

After power up iTRAX03-S boots from the internal flash memory for normal operation. Modes of operation:

- Navigating/Idle mode

- Sleep mode

- Programming mode

3.2 Navigating/Idle mode

The iTRAX03 receiver enters navigating mode after power up. It will by default start navigation automatically after power up/reset in auto start mode. Auto start mode means that all available aiding information will be used.

The module runs as long as the power supply is available.

Idle mode means that the navigation is stopped but the processor remains still active. Navigating/Idle mode is also referred as **Normal** Mode.

The standard firmware supports versatile configuration of various operating configurations, e.g. Logging position data etc., for further details see *ref 2*.

The navigation can be stopped by sending a proper NMEA or iTALK message, see also *ref 2*.

3.3 Sleep mode

The Sleep mode means a low power operation during which no other activity other that the internal real time clock (RTC) is present. The module enters Sleep mode via a special control message (*ref #2*) or by the On/Off Control input.

The exit from Sleep mode to Normal mode happens either after

- the elapsed time or

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- a RS232 break signal or a dummy input character to selected serial port (the low input state should exceed 20ms) or

- interrupt from the On/Off Control input (low-to-high transition)

- interrupt from the Wake Up Control input (toggle input)

Since the internal RTC keeps the GPS time estimate, the module performs the fastest possible navigation start, depending on the availability of valid satellite/position data.

3.4 Programming mode

The module enters Programming mode by two methods: HW-booting or upgrading the firmware on-the-fly by a dedicated NMEA or iTalk command, see *ref 1*.

The on-the-fly upgrading requires only a serial port and the downloading will be started by sending a special command and the utility running on the host will send the new firmware to the processor.

HW-booting is utilized by keeping the Boot control input (GPIOB22) at low state during power up or system reset. Now the GPS module boots from the serial data Port 0, sends hex 55 (U) string at 9600 baud and waits the for the boot loader commands from the host (an application running on the host). This mode is required when there is no existing firmware stored to the internal Flash memory or when the previous firmware is corrupted.

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4. CONNECTIVITY

4.1 Connection assignments

The I/O connections are available as soldering pads on the bottom side of the module. These pads are also used to attach the module on the motherboard in the application. All the unconnected I/O should be left open (floating).

Table 3 Connections

Contact	Signal name	I/O	Alternative GPIO name	Signal description
1	TCAP1	I/O	GPIOA11	Capture timer 1 input
2	BOOT1	I/O	GPIOB22	Boot 1 control input
3	SPI1XCS0	I/O	GPIOB10	SPI1 chip select 0; Power Good control input
4	SPI1SDO	I/O	GPIOB14	SPI1 data output, On/Off control input
5	GND	I/O	-	Ground
6	SPI1SDI	I/O	GPIOB15	SPI1 data input, Wake Up control input
7	SPI1CLK	I/O	GPIOB13	SPI1 data clock
8	GND	-	-	
9	XRESET	I	-	Asynchronous system reset, active when low
10	BOOT2	I/O	GPIOB21	Boot 2 control input
11	GND	-	-	Ground
12	SPI1XCS2	I/O	GPIOB12	SPI1 chip select 2, UI indicator C (Fix available)
13	MMCCMD	I/O	GPIOA13	MMC command signal, UI indicator B
14	VDDRF	I	-	Power supply for analog parts

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Contact	Signal name	I/O	Alternative GPIO name	Signal description
15	GND	-		
16	TXD1	I/O	GPIOA3	UART 1 async. output
17	TXD0	I/O	GPIOA1	UART 0 async. output
18	RXD0	I/O	GPIOA0	UART 0 async. input
19	RXD1	I/O	GPIOA2	UART 1 async. input
20	GND	-	-	Ground
21	MMCCLK	I/O	GPIOA12	MMC clock signal
22	GND	-	-	Ground
23	GND	-	-	Ground
24	RFIN	I/O	-	Antenna signal input, Antenna bias voltage output
25	GND	-	-	Ground
26	GND	-	-	Ground
27	MMCDAT	I/O	GPIOA14	MMC data signal, UI indicator A
28	VDDDIG	I	-	Power supply for digital parts
29	PM0	I/O	GPIOA5	Pulse measurement input 0
30	PPS	I/O	GPIOA7	1PPS signal output
Contact	Signal name	I/O	Alternative GPIO name	Signal description

4.2 Power supply

The iTRAX03 module requires two separate power supplies: VDDRF for the RF parts and the VDDDIG for digital parts and I/O.

The VDDRF must be linearly regulated having a low ripple 2mV(RMS) max, typical current drain is 24 mA in normal (navigating) mode without the antenna bias current. Note that the VDDRF is also provided internally at the Antenna input as an active antenna bias.

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NOTE

VDDRF supply current should be limited ex-
ternally below 150 mA max.

NOTE

VDDRF supply voltage should have a low
ripple 2mV(RMS) max.

The VDDDIG supply may be shared with any available supply that
meets the specified voltage range, typical current is 12 mA in normal
(navigating) mode but it may peak up to 40 mA for short durations.

4.3 Reset

The reset input XRESET is an active low asynchronous reset. The
processor boots after the low-to-high transition. The XRESET input
contains an internal voltage detector to force reset when VDDDIG is
below +2.5V. For normal operation the XRESET input can be left un-
connected.

4.4 Watchdog

The processor contains a watchdog peripheral, which resets the
processor if not refreshed frequently enough. Basically the watchdog
is a 16-bit counter with enabling, disabling and restarting controls.
The watchdog counter is clocked with the frequency of 128 Hz.

4.5 Shared functionality

All the I/Os have a shared functionality with the main functionality or
with a General Purpose I/O (GPIO). Each signal is named according
to the main functionality but also the secondary functionality is listed
as the Alternative GPIO for iSuite3 SDK users.

With the standard firmware there are dedicated GPIO connections,
which are: Boot Select, UI Indicators and control inputs that shall be
described in the following chapters.

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4.6 Dedicated GPIO

4.6.1 Boot Select

The boot source is defined in the internal boot ROM sector by using the BOOT1 and BOOT2 (GPIOB22 and 21 respectively). After power up or after system reset these contacts are first configured to pull-down mode for 300 clock cycles (10 µs), after which their values are read and the boot is processed according the following table.

Table 4   Boot select

BOOT1	BOOT2	I/O	Boot source
high	high	I	External boot sector (Flash), in case of failure continue with SPI1 boot
high	low	I	External boot sector (Flash), in case of failure continue with UART Port 0 boot
low	high	I	SPI1 boot
low	low	I	UART Port 0 boot

After power up the Boot select should be kept low at least 100 ms.

In Normal mode the Boot Select should be kept low for at least 30us after XRESET low-to-high transition.

The standard firmware supports only the boot from internal Flash memory (normal operation) or boot from UART Port 0. Thus only the BOOT1/GPIOB22 is needed for proper setting the Boot Select.

NOTE

To ensure normal operation during system reset and power on, the BOOT1 input (GPIOB22, contact #2) requires an external pull-up resistor connected to VDDDIG, e.g. 4.7 kohm.

Respectively the BOOT2/GPIOB21 (contact #10) should be left open or connected to pull-down resistor, e.g. 4.7 kohm.

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4.6.2 UI Indicators

With the standard firmware there are three GPIO outputs reserved as a driver for User Interface (UI) Indicators. These outputs can be used e.g. to drive LEDS, which gives information on the state of the receiver.

Table 5 UI Indicators

UI Indicator	Contact number	I/O	Operation: High ratio %	Signal description
A	27	O	Continuously low state	Power Off or Sleep mode
A	27	O	Short blink 20	Normal mode, Navigation stopped
A	27	O	Long blink 80	Normal mode, Navigation started
B	13	O	Continuously low state	Navigation stopped or not tracking satellites
B	13	O	Short blink 20	Tracking satellites but not enough information to calculate pseudo-ranges
B	13	O	Long blink 80	Pseudorange information available but not navigating
B	13	O	Continuously high state	Navigating, Valid fix
C	12	O	Low state	No valid fix
C	12	O	High state	Valid fix available

The UI Indicators are updated synchronously at 1 Hz rate. The high state duty cycle is either 0% (Continuously low state), 20% (Short blink), 80% (Long blink) or 100% (Continuously high state).

UI indicator C indicates when a valid fix is available.

4.6.3 On/Off control input

With the standard firmware the module can be controlled to Sleep mode by the On/Off control input (SPI1SDO / GPIOB14, contact #4) or by a specific serial command. During Sleep Mode only the real time clock is running and the current consumption is reduced to about 20 uA.

Note that the worst case delay from the On/Off Control high-to-low transition to achieve Sleep mode and reduced current drain is 300 ms. The standard firmware stores the last known good position (LKG) and any Log data to the internal Flash memory before entering the Sleep mode.

Table 6   On/Off control

On/Off Control contact 4	I/O	Signal description
High state	I	Normal (navigating) mode, delay from Sleep mode 3 ms
Low state	I	Sleep mode, delay from Normal mode 300 ms max.

NOTE

With the standard firmware the On/Off control input has an internal pull-up resistor 100kohm connected to VDDDIG and the signal can be left unconnected for normal operation. Note also chapter Sleep mode &I/O.

4.6.4 Wake Up control input

With the standard firmware the module can be wake up from sleep state by the Wake Up control input (SPI1SDI / GPIOB15, contact #6). Wake Up input is normally used only when the module has entered sleep state using the specific serial command.

Wake up interrupt is generated by toggling the Wake Up control input; in case of a pulse the pulse length should be at least 20 ms.

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Table 7   Wake Up control

Wake Up Control contact 6	I/O	Signal description
High to Low	I	Wake up from sleep state, Low state at least 20ms
Low to High	I	Wake up from sleep state, High state at least 20ms

NOTE

With the standard firmware the Wake Up control input has an internal keeper circuit and the signal can be left unconnected for normal operation. Note also chapter Sleep mode &I/O.

4.6.5 Power Good control input

The standard firmware (3.11) does not support this feature.

4.6.6 Sleep mode and I/O

During Sleep mode all the dedicated GPIO are configured to inputs with internal 100kohm pull-down resistors. There is one exception: the On/Off control input is configured to 100k pull up resistor in case the sleep state is entered via a proper command to any of the serial Ports.

4.7 Antenna input

The module supports passive and active antennas. The antenna input impedance is 50 ohms. During normal (navigating) operation, the input provides also a bias supply, which is the same level as the VDDRF supply. During idle or sleep state the antenna bias is switched off.

The maximum tolerated antenna bias current is 100mA, which is current limited only by the external regulator supplying VDDRF. It is re-

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quired that the VDDRF supply current is limited externally to150 mA max.

NOTE

> Passive antennas with a short-circuit to GND should be DC blocked externally with a 18pF…1nF serial capacitor.

4.7.1 Active GPS antenna

The customer may use an external active GPS antenna for e.g. in mobile or indoor usage. It is suggested the active antenna has a net gain *including cable loss* in the range from +6 dB to +32 dB.

4.8 PPS output

The PPS output provides a pulse-per-second signal, which can be used for timing purposes. For details of operating modes check documentation: iSuite^{TM} 3 SDK Protocols – NMEA (*ref 2*).

4.9 UART

The device supports UART communication via Port 0 and Port 1. With the standard firmware the Port 0 is configured to NMEA by default and secondary to iTALK protocol. The Port 0 is used also when the device is booting from the serial port. With the standard firmware the Port 1 is configured to iTALK by default.

I/O levels form the serial ports are CMOS compatible, not RS232 compatible. Use an external level converter to provide RS232 levels when needed. Refer to *ref 2* for supported data speeds.

4.10 SPI-bus

The SPI1 bus (master) is available for SDK users enabling high speed synchronous serial SPI communication.

4.11 Capture timer

One general-purpose timer TMG1 is available for SDK users with a custom firmware. It has a configurable prescaler and clock cycle counts. The clock input is limited to internal sources and there is a

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capture mode to count external events. Each timer also has a programmable delay, referenced to the internal epoch pulse (TME). This makes it possible to have a specified delay between interrupts generated by the internal TME epoch, TMG0, and TMG1. For details see *ref 3*.

4.12 Pulse measurement input

One measurement (PM0) input is available for SDK users with a custom firmware. PM0 input can be used to measure with great accuracy how long an input stays high or low. For details see *ref 3*.

4.13 MMC bus

The MMC bus is available for SDK users with a custom firmware. The MMC unit implements a standard 3-wire Multi Media Card serial bus interface and provides control and data register for easy usage of the bus. Both stream and block mode data transfers are supported. The CRC is calculated automatically for transmitted commands and data blocks, also received responses and data blocks are checked for correct CRC. The MMC unit has a 64-bit data buffer and is capable of stopping bus clock to prevent buffer overflow and underflow situations. For details see *ref 3*.

4.14 Mechanical dimensions and contact numbering

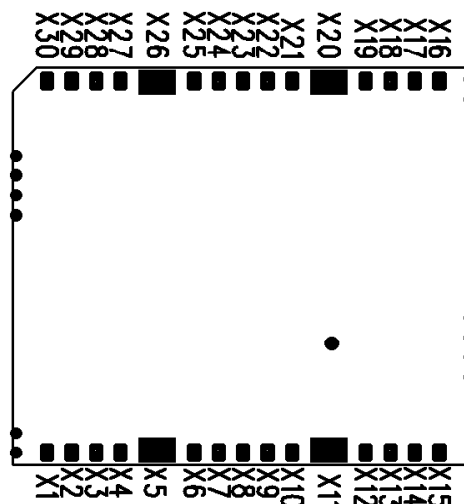Module size is 16.2mm (width) x 18.8mm (length) x 3.1mm (height max). General tolerance is ±0.1mm.

Figure 2   Contact numbering, top view.
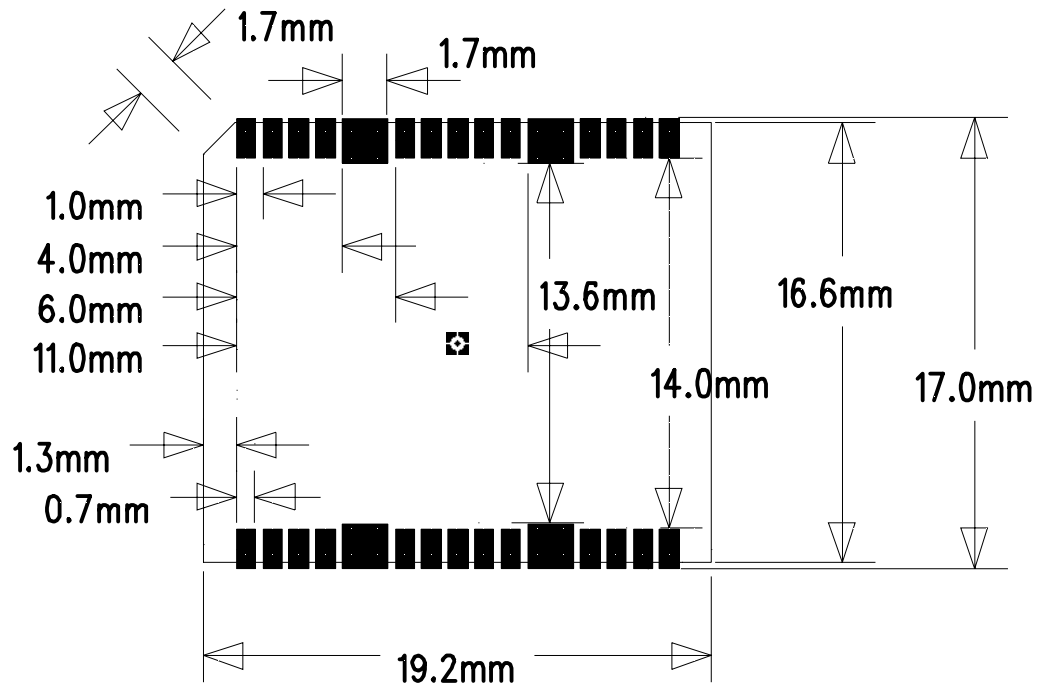
4.15 Suggested pad layout

Figure 3   Suggested pad layout and occupied area, top view.

5. MANUFACTURING

5.1 Assembly

The iTrax03-S module supports only assembly and soldering in a re-flow process on the top side of the PCB.
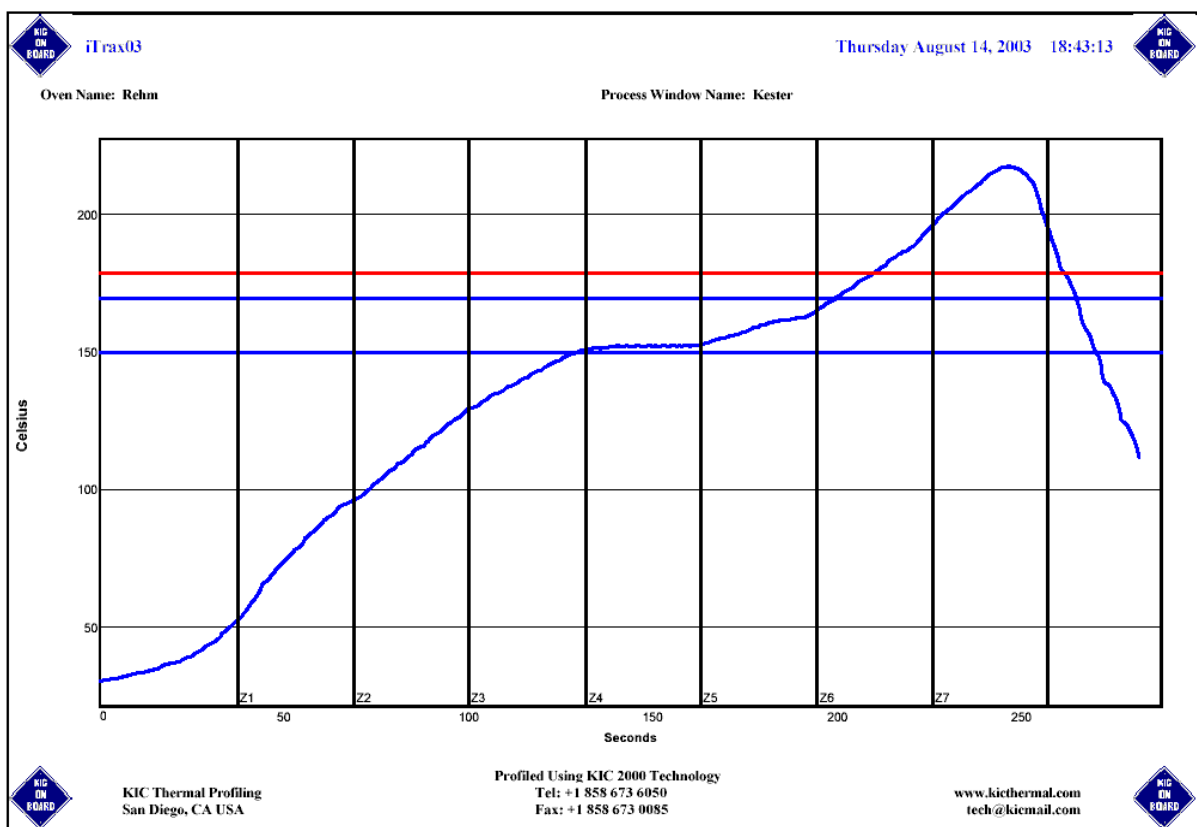
5.2 Suggested Reflow soldering profile

Figure 4   Suggested reflow soldering temperature profile.

5.3 Moisture sensitivity

Note that the iTRAX03-S is moisture sensitive at MSL 3 (see the standard IPC/JEDEC J-STD-020B). The module must be stored in the original moisture barrier bag or if the bag is opened, the module must be repacked or stored in a dry cabinet (according to the standard IPC/JEDEC J-STD-033A). Factory floor life in humid conditions is 1 week for MSL 3.

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6. REFERENCE DESIGN

The idea of the reference design is to give a guideline for the applications using the iTRAX03-S GPS module. In itself it is not a finished product, but an example that performs correctly.

In the following two chapters the reader is exposed to design rules that he should follow, when designing an iTRAX03-S in to the application. By following the rules one end up having an optimal design with no unexpected behavior caused by the PCB itself. In fact these guidelines are quite general in nature, and can be utilized in any PCB design related to RF techniques or to high speed logic.

6.1 Minimum Application Circuit Diagram

The Minimum Application supports communication through the UART Port 0 (NMEA or iTALK). Other required signals are the antenna input, supply voltage for VDDRF and VDDDIG, a pull-up resistor for the BOOT1 control.

The low drop-out linear regulator (LDO) U2 supplies +2.8 V voltage to the RF and analog parts (VDDRF) and the digital supply (VDDDIG) is taken directly from the main supply, which in this case is from +3.0 to +3.3 V due to the small drop-out voltage across U2. The linearly regulated power supply is needed for VDDRF, because the maximum allowed ripple voltage for VDDRF is 2 mV(RMS). The external regulator U2 can be omitted, if such a supply is available that meets the specified ripple voltage.

All the digital signals are routed away from the module through series resistors (R2, R3). In this way the local oscillator (LO) signal leakage that is present in the I/O contacts of the GPS module is suppressed. Although the LO leakage is very small at the IO contacts of the module, it may still interfere the GPS reception, especially when the antenna is located very near to these signal routes.

For the same reason capacitors C1 and C2 should be connected very close to the module's with short traces to I/O contacts and to ground plane.

Additionally, there must be another capacitor (C3: 4.7uF or bigger) from VDDDIG to the ground. This capacitor can be located further away. If some specific signal from the iTRAX03 is not needed, it can be left open by default.
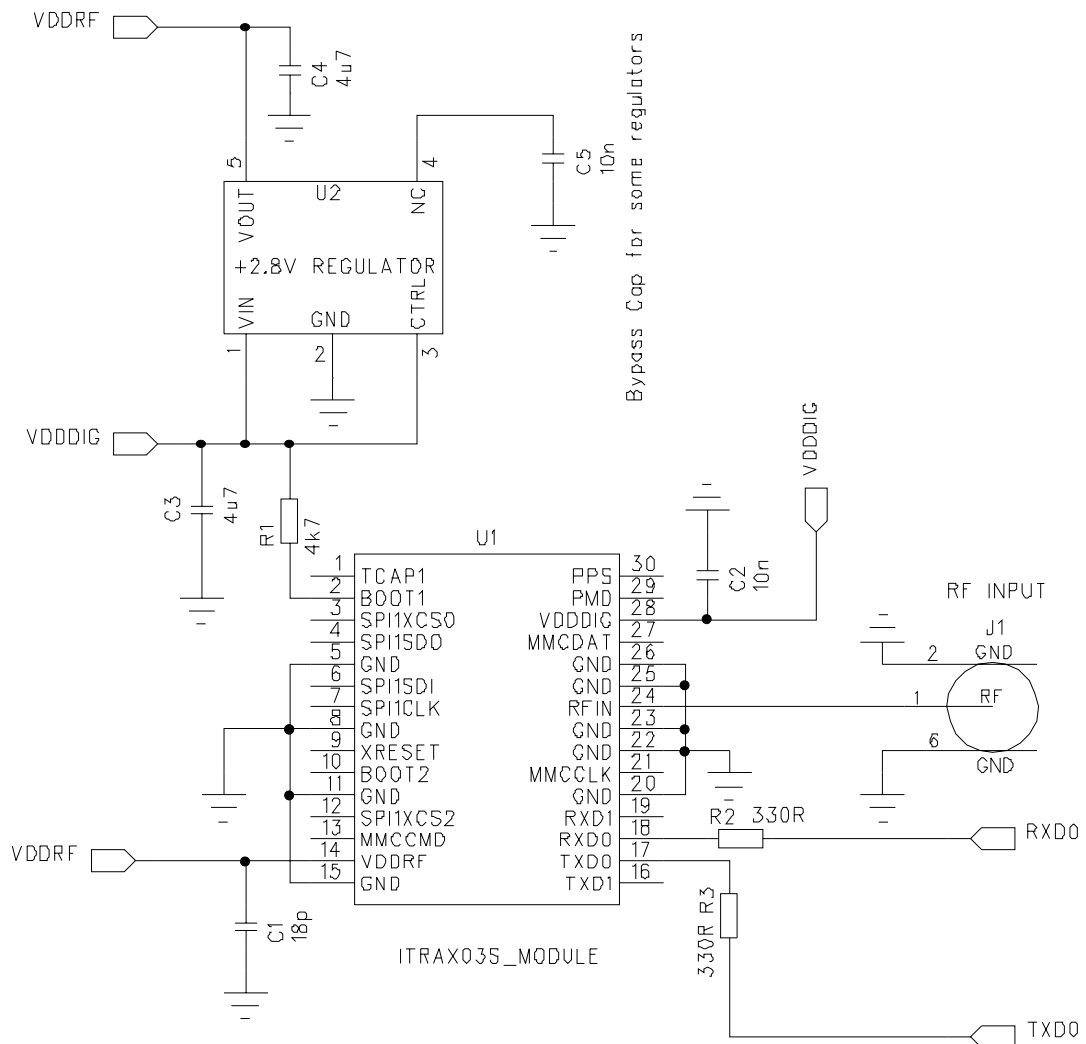
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Figure 5   Minimum Application Circuit Diagram.

Note that there is a DC voltage present at the RF input, when the module is operating in Normal mode. This voltage is equal to VDDRF. If a passive antenna with a short-circuit to the GND is used, an external series DC block capacitor (18pF) must be used for the RFIN signal line.

6.2 PCB layout issues

The suggested 4-layer PCB build up is presented in the following table.

<div align="center">

Table 8   Suggested PCB build up

</div>

Layer	Description
1	Signal + Ground with copper keep-out below iTRAX03-S
2	Ground plane
3	Signal + Ground or VDD plane
4	Signal (short traces) + Ground

Routing signals directly under the module should be avoided. This area should be dedicated to keep-out to both traces and to ground (copper), except for the via holes, which can be placed close to the pad under the module. If possible, the amount of VIA holes underneath the module should be also minimized.

For a multi-layer PCB the first inner layer below the iTRAX03-S is suggested to be dedicated for the ground plane. Below this ground layer other layers with signal traces are allowed. It is always better to route very long signal traces in the inner layers of the PCB. In this way the trace can be easily shielded with ground areas from above and below.

The serial resistors at the I/O should placed very near to the iTRAX03-S module. In this way the risk for the local oscillator leakage is minimized. For the same reason by-pass capacitors C1 and C2 should be connected very close to the module's with short traces to IO contacts and to the ground plane. Place the GND via hole as close as possible to the capacitor.

Connect the GND soldering pads of the iTRAX03-S to ground plane with short traces to via holes, which are connected to the ground plane. Use preferably two via holes per GND pad.

The RF input should be routed clearly away form other signals, this minimizes the possibility of interference. The proper width for the 50 ohm transmission line impedance depends on the dielectric material

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of the substrate and on the height between the signal trace and the first ground plane. With FR-4 material the width of the trace shall be two times the substrate height.

A board space free of any traces should be covered with copper areas (GND). In this way, a solid RF ground is achieved throughout the circuit board. Several via holes should be used to connect the ground areas between different layers.

Additionally, it is important that the PCB build-up is symmetrical on both sides of the PCB core. This can be achieved by choosing identical copper content on each layers, and adding copper areas to route-free areas. If the circuit board is heavily asymmetric, the board may bend during the PCB manufacturing or reflow soldering. Bending may cause soldering failures.

7. ITRAX03-S APPLICATION BOARD

The application board provides the iTrax03-S connectivity to the Evaluation Kit or to other evaluation purposes. It provides a single PCB board equipped with the iTrax03-S module, two regulators, an MCX antenna connector and a 2x20 pin Card Terminal connector.

7.1 Card Terminal I/O-connector

The following signals are available at the 40-pin Card Terminal I/O connector J2.

Pin	Signal name	I/O	Alternative GPIO name	Signal description
1	TXD1	O	GPIOA3	UART 1 async. output
2	GND	-	-	Ground
3	RXD1	I	GPIOA2	UART 1 async. input
4	GND	-	-	Ground
5	TXD0	O	GPIOA1	UART 0 async. output
6	GND	-	-	Ground
7	RXD0	I	GPIOA0	UART 0 async. input
8	GND	-	-	Ground
9	VCC	-	-	Power input
10	GND	-	-	Ground
11	PPS	O	GPIOA7	1PPS signal output
12	GND	-	-	Ground
13	XRESET	I	-	Active low async. system reset
14	FCLK	O	GPIOA4	Pre-divided clock output of UART 1
15	SPI2XCS2	O	GPIOB21	SPI2 chip select2, (2nd boot select)
16	SPI2XCS3	I/O	GPIOB22	SPI2 chip select3, Boot Select
17	GND	-	-	Ground
18	TCAP1	I	GPIOA11	Timer TMG1 capture input

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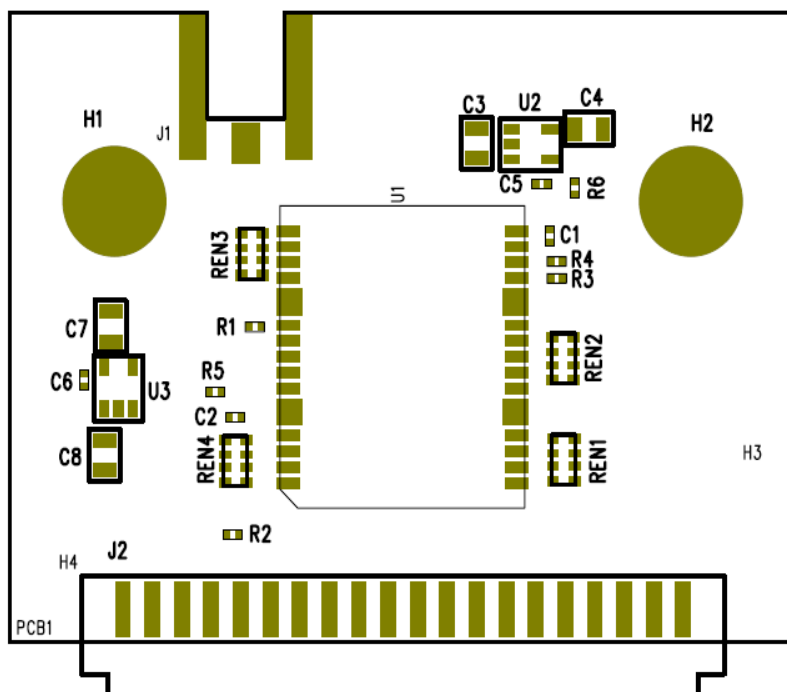| Pin	Signal name	I/O	Alternative GPIO name	Signal description
19	TIN0	I	GPIOA8	Timer TMG0 external clock input
20	TIN1	I	GPIOA10	Timer TMG1 external clock input
21	GND	-	-	Ground
22	TCAP0	I	GPIOA9	Timer TMG0 capture input
23	PM1	I	GPIOA6	Pulse measurement input 1
24	PM0	I	GPIOA5	Pulse measurement input 0
25	GND	-	-	Ground
26	MMCCMD	I/O	GPIOA13	MMC command bus, UI indicator B
27	SPI1XCS0	O	GPIOB10	SPI1 chip select 0
28	MMCCLK	O	GPIOA12	MMC clock output
29	SPI1CLK	O	GPIOB13	SPI1 clock
30	MMCDAT	I/O	GPIOA14	MMC data bus, UI indicator A
31	GND	-	-	Ground
32	SPI1SDO	O	GPIOB14	SPI1 data output
33	GND	-	-	Ground
34	SPI1SDI	I	GPIOB15	SPI1 data input, Wake-up input
35	GND	-	-	Ground
36	SPI2CLK	I/O	GPIOB16	SPI2 clock, output in master mode
37	GND	-	-	Ground
38	SPI2SDI	I	GPIOB18	SPI2 data input, On/Off control inp.
39	GND	-	-	Ground
40	SPI1XCS2	O	GPIOB12	SPI1 chip select 2, UI indicator C
Pin	Signal name	I/O	Alternative GPIO name	Signal description

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NOTE

All I/O signals are routed at the Card Terminal connector J2 following the iTrax03 naming with one exception: the signal named SPI1XCS2 (iTrax03-S pin 12, signal UI_C) is not available at the iTrax03 Application Board and thus this signal is routed to the pin 40 at J2, which follows the iTrax03 standard firmware operation (UI indicator C).
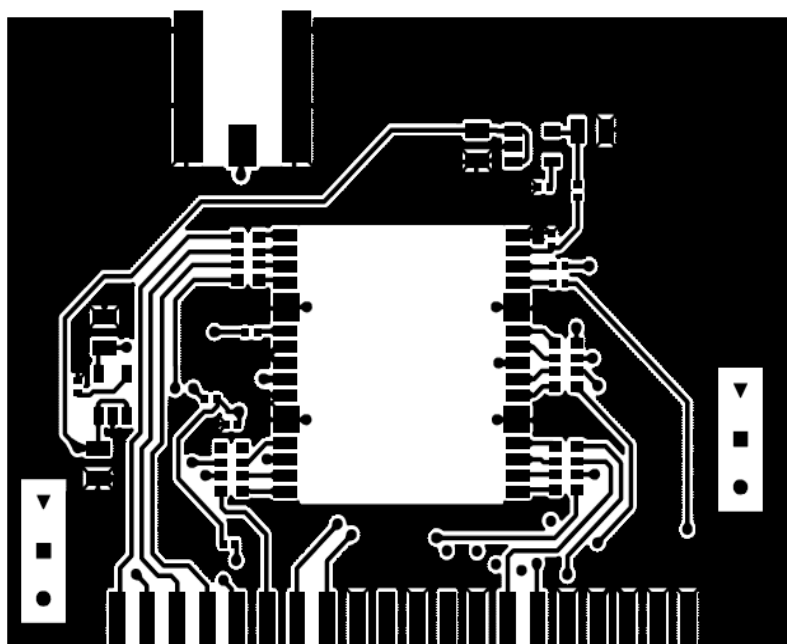
7.2 Bill of materials

Item	Qty	Reference	Part Name	TECHNICALDESCRIPTION
1	1	C1	C/0402/NPO/18P/50V/T5P,18pF	18pF 50V 5% NP0 0402
2	3	C2 C5-6	C/0402/X7R/10N/50V/T10P,10nF	10nF 50V 10% X7R 0402
3	4	C3-4 C7-8	C/0805/X5Y/4U7/6V3/T5P,4u7F	4,7uF 6,3V X5Y 0805
4	2	H3-4	FIDUCIAL,FIDUCIAL	FIDUCIAL, Circle, rectangle, triangle
5	2	H1-2	HOL/M3.0	
6	1	J2	J/2X20/EDGE, Pitch 2.0mm	SAMTEC EMT-120-01-S-D
7	1	J1	J/MCX/PCB,CON/BNC_90DEG_PCB	50 Ohm male MCX connector PCB
8	1	U1	MODULE/IT3S0A00,MODULE/IT3S0A00	MODULE IT3S0A00, itrax03S rev. A
9	1	PCB1	PCB/AP3S0A00,PCB/AP3S0A00	Application Board for iTrax03S
10	2	R5-6	R/0402/0R,0R	0R 0402
11	3	R1 R3-4	R/0402/220R/5P,220R	220R 5% 0402 63mW
12	1	R2	R/0402/4K7/T5P,4.7k	4.7k 5% 0402 63mW
13	4	REN1-4	RA/4X220R/ARV241,4X220R	4 x 220R ARV241
14	2	U2-3	U/REG/2V8/TSOT5,LDO2V8	Regulator

Fastrax

7.3 Circuit drawing

AppBoard iTRAX03-S

CIRCUIT DIAGRAM

FASTRAX

Dwg no AP3S0B01 Rev B

7.4 Assembly drawing, Top side

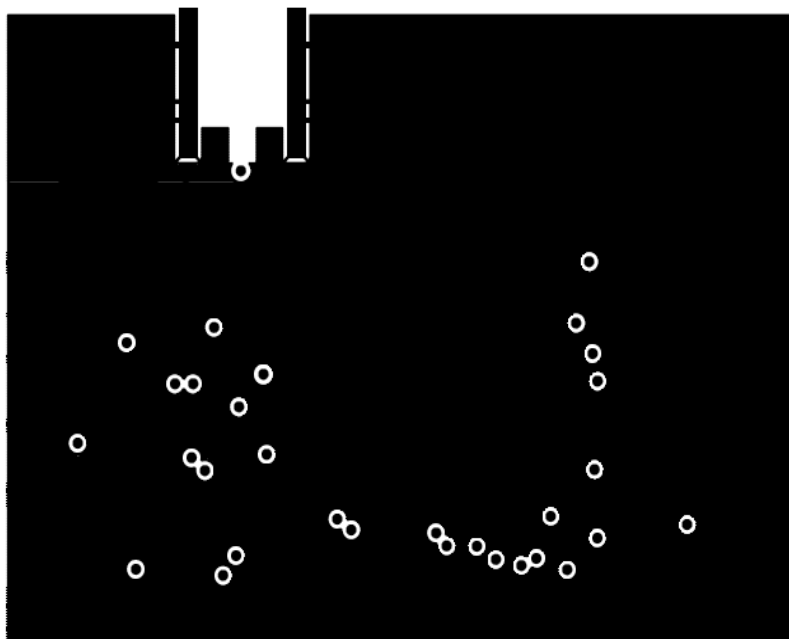## 7.5 Artwork, layer 1 (Top)

Fastrax

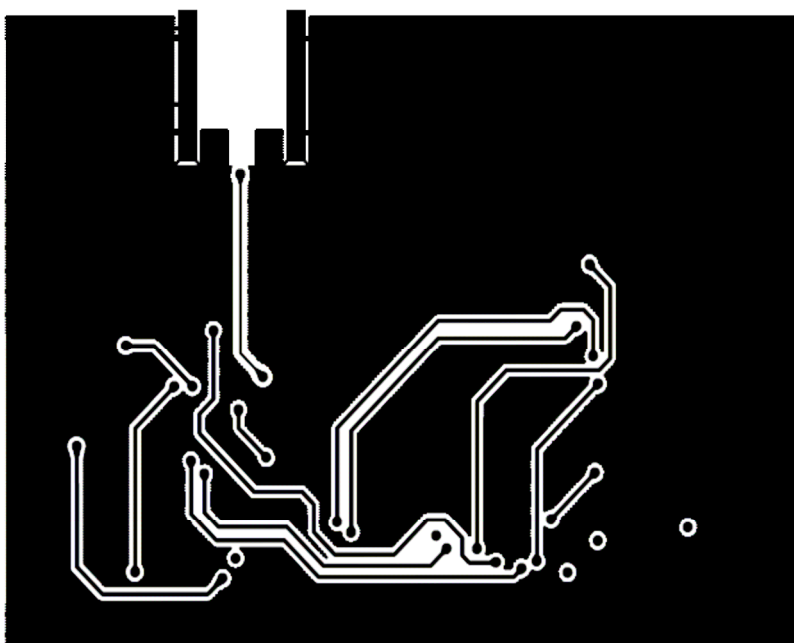## 7.6 Artwork, layer 2

7.7 Artwork, layer 3

7.8 Artwork, layer 4