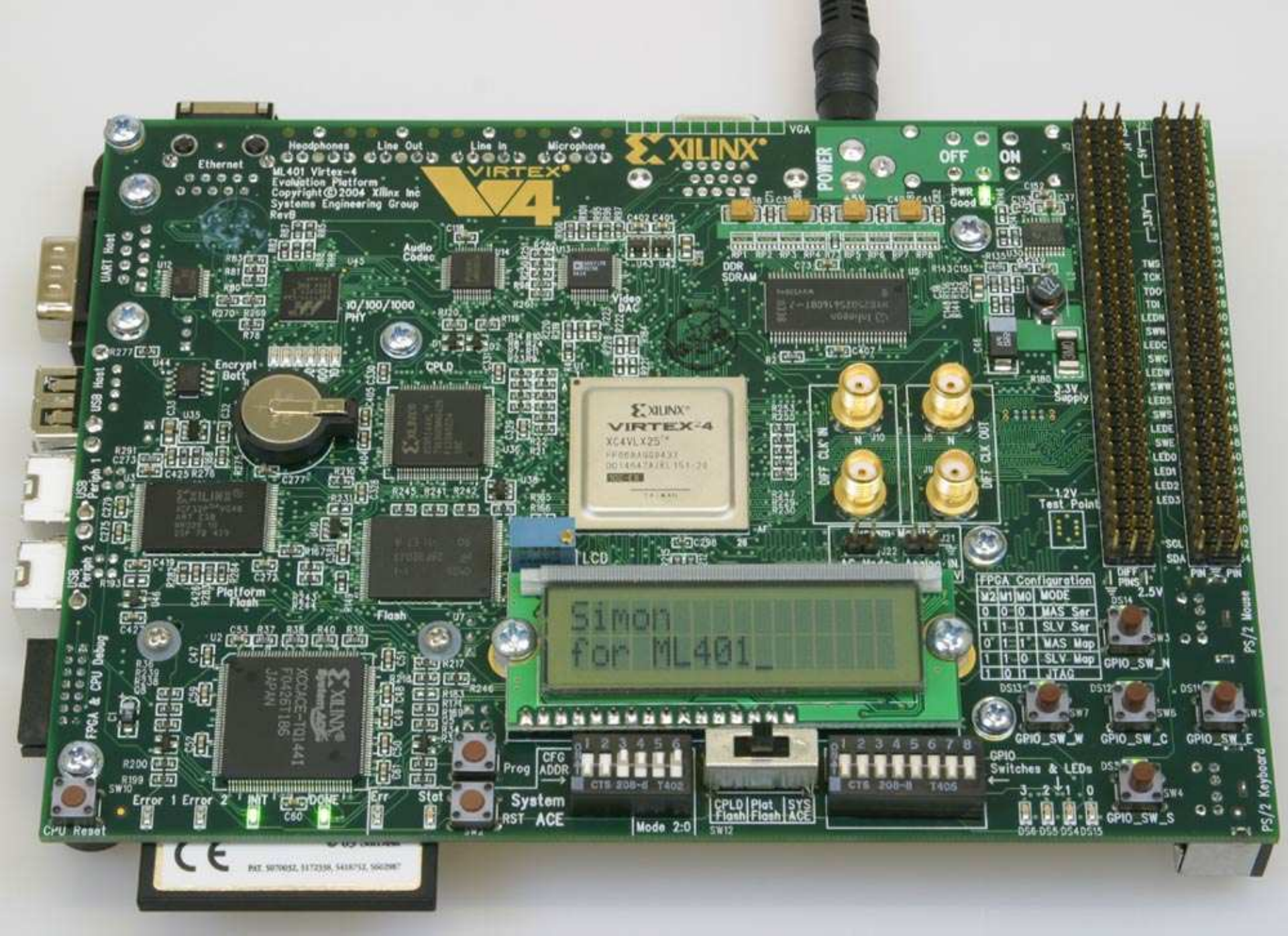
Headphones
Line Out
Line In
Microphone
VGA
Ethernet
ML401 Virtex-4
Evaluation Platform
Copyright © 2004 Xilinx Inc
Systems Engineering Group
RevB
XILINX
VIRTEX
V4
POWER
OFF
ON
PWR Good
UART Host
Audio Codec
Video DAC
DDR SDRAM
10/100/1000 PHY
USB Host
Encrypt Batt
CPLD
XILINX
VIRTEX-4
XC4VLX25
DIFF CLK IN
DIFF CLK OUT
3.3V Supply
1.2V Test Point
LCD
Simon
for ML401_
FPGA Configuration
M2 M1 M0 MODE
0 0 0 MAS Ser
1 1 1 SLV Ser
0 1 1 MAS Map
1 1 0 SLV Map
1 0 1 JTAG
TMS
TCK
TDO
TDI
LEDN
SWN
LEDC
SWC
LEDW
SWW
LEDS
SWS
LEDE
SWE
LED0
LED1
LED2
LED3
SCL
SDA
PS/2 Mouse
PS/2 Keyboard
USB Periph 1
USB Periph 2
FPGA & CPU Debug
Platform Flash
Flash
2.5V
GPIO_SW_N
GPIO_SW_W
GPIO_SW_C
GPIO_SW_E
GPIO_SW_S
GPIO Switches & LEDs
Prog
CFG ADDR
System RST
ACE
Mode 2:0
CPLD Flash
Plat Flash
SYS ACE
Error 1
Error 2
INT
DONE
Err
Stat
CPU Reset