

LEON3MP Design Configuration

Synthesis

Clock generation

Processor

AMBA configuration

Debug Link

Peripherals

VHDL Debugging

Save and Exit

Quit Without Saving

Load Configuration from File

Store Configuration to File

Processor

Processor

y

n

Enable LEON3 SPARC

1

Number of processors

Integer unit

Floating-point unit

Cache system

MMU

Debug Support Unit

Fault-tolerance

VHDL debug settings

Main Menu

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Integer unit

Integer unit

8

SPARC register windows

Help

y

n

SPARC V8 MUL/DIV instructions

Help

5-cycles

Hardware multiplier latency

Help

y

n

SPARC V8e SMAC/UMAC instructions

Help

y

n

Single-vector trapping

Help

1

Load delay

Help

2

Hardware watchpoints

Help

y

n

Enable power-down mode

Help

00000

Reset start address (addr[31:12])

Help

OK

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