Hardware-in-the-loop testing of impedance protection with compensation of fault impedance and DG infeed current

Konstantin Pandakov[1] ✉, Charles Mawutor Adrah[1], Zou Liu[1], Hans Kristian Høidalen[1], Øivind Kure[1]

[1]*NTNU, Trondheim, Norway*
✉ *E-mail: konstantin.pandakov@ntnu.no*

Abstract: The standard impedance protection deployed in distribution networks can malfunction due to underreach errors caused by fault impedances and remote infeed currents from embedded generators (becoming more and more widespread). This paper introduces a compensation method aiming at elimination of these issues and enhancement of relay dependability. As an advantageous outcome, compensated measurements can be utilised for accurate fault location. The method is verified on ABB RED 670 relay in the loop with an OPAL-RT real-time simulator. As the method is based on multi-point measurements, the test setup also contains a communication network emulator for modelling network delays and imperfections. The laboratory tests verify applicability of the method with proper appearance of the tripping signals from the relay. The fault location results based on synchronised data show overreaching inaccuracy rising with fault resistance. Though communication network delays and imperfection of the channels lead to underreaching, it has been revealed that not strict requirements for data synchronisation can be applied to specific measurements.

1 Introduction

In the previous work by the authors in [1], it was shown that impedance protection in medium-voltage (MV) networks is vulnerable to non-zero fault impedances leading to under-reaching problems. Moreover, distributed generation (DG) might aggravate the situation. For reliable operation, compensation of these challenges is required.

Many methods proposed in literature for transmission systems can be adopted to MV networks in order to protect feeders with DG. For example, the authors in [2] describe the one-end and the two-end methods for impedance correction in the presence of the remote infeed; the study in [3] performs the two-terminal compensating algorithm for ground faults; the adaptive direct underreaching transfer trip protection scheme for the three-terminal line is demonstrated in [4]; application of synchrophasors in the multiterminal network with fault resistance evaluation is shown in [5]; the study in [6] represents the pilot protection method without strict requirements for synchronisation.

Distribution networks have complex topology with tapped loads that can make the methods developed for high-voltage grids unreliable. Study of impedance relaying in MV systems with DG mainly focuses on its feasibility [1], adaptive settings [7], or communication-based methods [8]. Compensation of DG impact on fault location is examined in [9]. In general, lack of studies dedicated to solution of underreaching problems due to non-zero fault impedances and DG infeed currents is observed. The resistive nature of the low fault impedance (arcing fault) can be handled by quadrilateral characteristics; however, in case of high resistance (contact with an extraneous object) or in the presence of strong remote infeed currents with reactive component, it becomes difficult.

The current work proposes a method solving this issue and improving performance of a feeder impedance relay during inter-phase faults (ground faults are out of the scope). Firstly, it introduces a simple and general compensation strategy utilising multi-point measurements (from an interconnected generator and a far-end substation). It compensates a fault impedance and infeed currents from the generator during impedance measurements that (in addition to elimination of underreaching problem) gives possibility for fault location. Secondly, the paper demonstrates its verification by the means of hardware-in-the loop testing with a real-time simulator involving a communication network emulator.

The last one allows studying of issues related to imperfections of the communication network.

2 Description of the compensation strategy

The current paper considers the T-configuration (see Fig. 1) – the DG is interconnected through a short line to the main feeder. For the compensation strategy, the following measurements are supposed to be available: interphase voltage V_s and current I_s (both are phasors) at the substation calculated as $V_s = V_{ph1} - V_{ph2}$ (ph1 and ph2 are phases affected by fault) and $I_s = I_{ph1} - I_{ph2}$. Analogously, measured at the remote substation: V_r and I_r, and at the DG: V_{DG}, I_{DG}.

Taking prefault measurements, the initial network with the load outfeeds is replaced by two equivalent lines with impedances determined as

$$Z_1 = \frac{V_s - V_{DG}}{I_s}$$
$$Z_2 = \frac{V_{DG} - V_r}{I_r} \tag{1}$$

When fault occurs (indicator will be discussed further), the following procedure is initialised:

i. It is initially considered that fault takes place in the first equivalent line, then the following system of equations is valid:

$$\begin{cases} V_{f1} = V_s - k_1 Z_1 I_s \\ V_{f1} = V_{DG} - (1 - k_1) Z_1 (I_{DG} + I_r), \end{cases} \tag{2}$$

where parameter k is a relative distance from the sending end of the line, V_f is voltage at the faulty point. Index 1 denotes the first line. V_{f1} is determined from (2) and fault impedance $Z_{f1} = V_{f1}/(I_s + I_{DG} - I_r)$ can be calculated.

ii. Fault in the second equivalent line is then considered, and similarly

$$\begin{cases} V_{f2} = V_r + (1 - k_2)Z_2 I_r \\ V_{f2} = V_{DG} - k_2 Z_2 (I_{DG} + I_s) \end{cases} \quad (3)$$

From these equations, V_{f2} and k_2 are determined, as well as fault impedance $Z_{f2} = V_{f2}/(I_s + I_{DG} - I_r)$.

iii. Finally, compensated impedance Z_{cps} seen from the substation can be computed with the following conditions:

$$\text{if } |Z_{f1}| \le |Z_{f2}|, \quad \text{then } Z_{eps} = \frac{V_s - V_{f1}}{I_s} = k_1 Z_1$$

$$\text{if } |Z_{f1}| > |Z_{f2}|, \quad \text{then } Z_{eps} = \frac{V_s - V_{f2} - \Delta V_{DG}}{I_s} \quad (4)$$

$$= Z_1 + k_2 Z_2,$$

where $\Delta V_{DG} = k_2 Z_2 I_{DG}$ is additional voltage drop during impedance measurements on the second equivalent line caused by current from the DG.

As we see, the smallest Z_f is used for selection of the correct faulty equivalent line (no added errors). The compensated measured impedance at the substation Z_{cps} directly shows exact fault location in terms of the line impedances without significant errors from the DG and a non-zero fault impedance.

Since the developed compensation method utilises interphase measurements, it can equally be applied for double-phase, double-phase-to-earth (in high impedance grounded systems only) and three-phase faults. For simplicity, only the last type is demonstrated. The performed strategy is tested on the laboratory setup described in the next section.

3 Laboratory setup

The test case network is illustrated in Fig. 1. Its model has been realised in Simulink®, and all model parameters are described in Table 1. Fig. 2 shows the full laboratory setup for verification of the proposed method. The previously developed hardware-in-the-loop testing platform [10] is expanded with a communication network emulator [11]. Real-time simulations of the network with the DG are executed in OPAL-RT® (50 μs time step). Measurements from the DG and the remote substation are formed
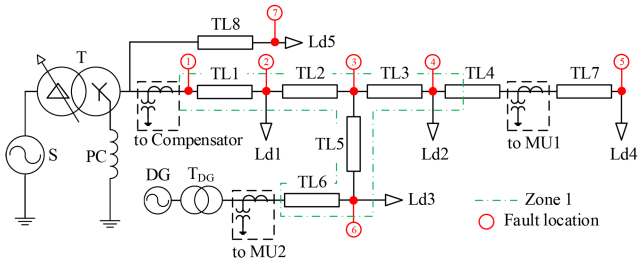
as sample values (SVs) in the merging units (MU1,2) using the standard IEC 61850 for sending to the emulator through Ethernet cable (Eth1). The emulator models time delays and data loss in the SV streams imitating real-time communication links and sends them back to the real-time simulator (Eth2) through the SV subscriber. The MUs and the subscribers have 4 kHz sampling rate, quality of SVs is set as good.

The compensator accomplishes the compensation strategy described in Section 2, namely: it determines phasors from the obtained SV, calculates $Z_{f1,2}$, $V_{f1,2}$, ΔV_{DG} and compensated voltage $V_{cps} = V_s - V_{f1}$ or $V_{cps} = V_s - V_{f2} - \Delta V_{DG}$, and finally it converts V_{cps} into an instantaneous signal. This signal together with the measured current at the substation are formed as SV in MU3 and sent to impedance relay ABB RED 670® (the physical path is Eth3 → the switch → fibre optic cables→the relay). Finally, the GOOSE messages from the relay can be used to trip the feeder (the relay → fibre optic cables → the switch → Eth4).

The relay settings are: Zone 1 (seen from Fig. 1) has positive sequence interphase impedance $11.5 + 11.5i\ \Omega$ and 20 ms time delay (fuse-saving strategy), Zone 2 is $17.3 + 17.3i\ \Omega$ (covers whole feeder) with 40 ms time delay. The quadrilateral relay characteristics have preset fault resistance 10 Ω (expected maximal arc resistance estimated on Warrington's formula [12] is 7.5 A).

Faults are applied in seven different locations as shown in Fig. 1 with low resistances (up to 10 Ω justified above) and high (up to 100 Ω) imitating a falling tree (probable situation in distribution networks). The fault is cleared after 100 ms (breaking operation takes several periods).

The compensator is initialised ($V_{f1,2} \ne 0$, $\Delta V_{DG} \ne 0$) if rate of change of impedance measured at the substation becomes less than −2 Ω/ms and magnitude of the impedance is <80% from measured several cycles before (comparison with a prefault value). The compensator is blocked ($V_{f1,2} = 0$, $\Delta V_{DG} = 0$) if the same conditions are valid for measurements at the remote substation (prevention of non-selective tripping).

4 Results and discussions

4.1 Synchronised measurements and ideal communication channel

For any fault conditions (with or without the compensator) at location 7, the tripping signals do not appear because the tripping zones of the relay are forward-directional. Hence, this case is not considered.

Fig. 3 shows a typical example for illustration of the signals in MU3 (phase voltages and currents sent to the relay) and the GOOSE subscriber (the tripping signals obtained from the relay) with and without the compensator functions. Fault at time 0, at location 1 with resistance 10 Ω is applied.

As it is possible to see from Fig. 3a, resistance 10 Ω leads to an underreaching problem: the tripping signals are absent. Fig. 3b demonstrates application of the compensating strategy and, as a consequence, appearance of the tripping signals with the time
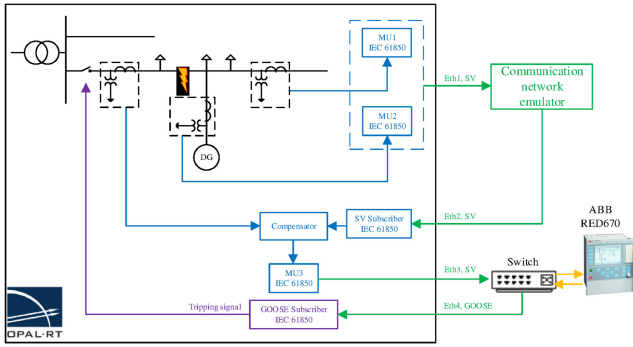

Fig. 1 *Test case network*

Table 1 Network parameters

Simulink model/parameters	
S	three-phase source, 66 kV, 50 Hz, 0.055 H (source inductance)
T, T_{DG}	three-phase transformer (two windlings), 50 Hz, Rm = 500 pu, Lm = 500 pu (ideal model)
	T: 20 MVA, Windling 1 [66 kV 0.0045 pu 0.09739 pu], Windling 2 [22·1.05 kV 0.0045 pu 0.09739 pu]
	T_{DG}: 3 MVA, Winding 1 [6.6 kV 0.0066 pu 0.06336 pu], Winding 2 [22 kV 0.0066 pu 0.06336 pu]
PC	14.7459 H
TL1 – TL8	three-phase PI section line, 50 Hz, [r1 r0] = [0.36 0.5] Ω/km, [l1 l0] = [1.146 5.093] mH/km, [c1 c0] = [10.137 4.794] nF/km
	line length, l in km: $l_{TL1} = l_{TL2} = l_{TL3} = l_{TL4} = 10$, $l_{TL5} = l_{TL6} = 0.5$, $l_{TL7} = l_{TL8} = 1$
Ld 1 – Ld5	three-phase parallel RLC load, delta configuration, 22 kV, 50 Hz, power factor 0.98, Qc = 0
	active power P in MW: $P_{Ld1} = P_{Ld2} = P_{Ld3} = 3$, $P_{Ld4} = 0.5$, $P_{Ld5} = 1$
DG	synchronous machine, 3 MVA, 6.6 kV, 50 Hz, [Xd Xd′ Xd″ Xq Xq″ Xl] = [2 0.22 0.2 1.4 0.2 0.18] pu, [Tdo′ Tdp″ Tqo″] = [4 0.025 0.1] s
	(open circuit), Rs = 5 × 10⁻³ pu, [H(s) F(pu) p] = [1 0 2]
	excitation system: IEEE type 1 (default parameters), hydraulic turbine and governor: default parameters

Fig. 2 *Laboratory setup: the hardware-in-the-loop testing platform with emulator of communication links*
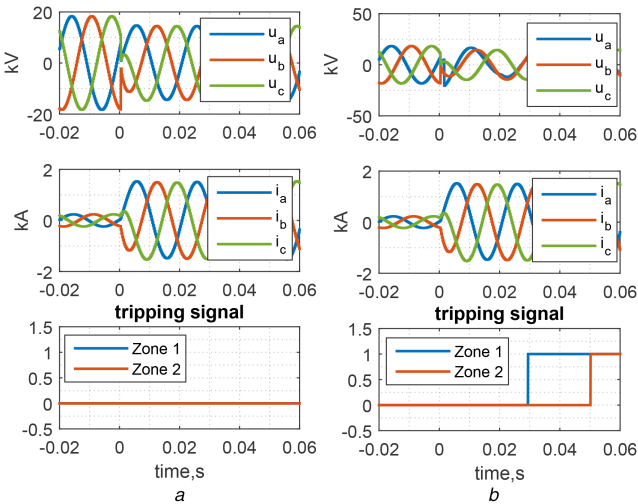

Fig. 3 *Phase voltages and currents sent to the relay, as well as the corresponding tripping signals from the relay*
(a) Without, *(b)* With compensation

Fig. 4 *Fault location error for zero fault resistance*
(a) Without, *(b)* With the compensator

Fig. 5 *Fault location error with the compensator for fault resistance*
(a) 10 Ω, *(b)* 100 Ω

delays. They are greater than the set values (20 ms for Zone 1 and 40 ms for Zone 2) due to inherent operation time of the impedance protection (about 10 ms). Delays in the physical paths (cables, switch) are negligible.

Similarly, all fault locations are tested. Fault resistances up to 10 Ω do not introduce any problems for the given quadrilateral tripping zones, whereas higher fault resistances (up to 100 Ω) make the tripping signals disappear. Involvement of the compensator improves the situation: the tripping signals from Zones 1 and 2 appear for faults at locations 1–4, 6; the tripping signal from Zone 2 only is present for faults at location 5.

It is of interest to see the impact of the method on a measured impedance in comparison with an actual (fault location error). Fig. 4*a* shows errors in km (calculated separately on the basis of the real and the imaginary part of the measured impedance for comparison) for faults at locations 1–6 with zero impedance. A sample of the measured impedance for error calculation is taken as the tripping signal from Zone 1 appears. A positive error might cause relay underreaching, negative-overreaching. It is seen that locations 4 and 5 have the biggest underreaching errors due to the impact from the DG.

Fig. 4*b* demonstrates influence of the compensator: it significantly decreases the error at location 4 (based on the real part); however, it slightly increases the errors at other locations (especially based on the imaginary part). An error at location 5 is not given because the compensator is inherently blocked and it will be the same as in Fig. 4 will be the same as in Fig. 4*a*.

Fig. 5 demonstrates errors for fault resistance 10 and 100 Ω for the compensated measurements. It can be observed that with the higher fault resistance the errors are bigger because impact of load currents becomes significant; therefore, the errors rise from locations 2 to 4. It is worth noting that the proposed compensation strategy leads to a situation where the measured impedance at the
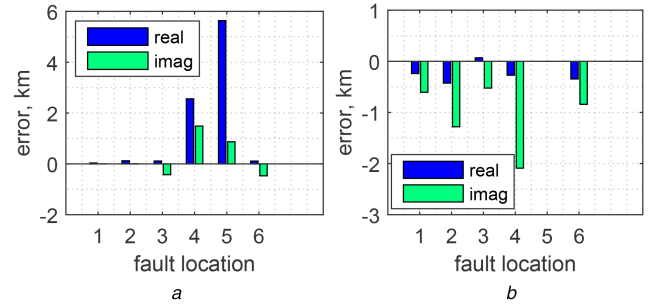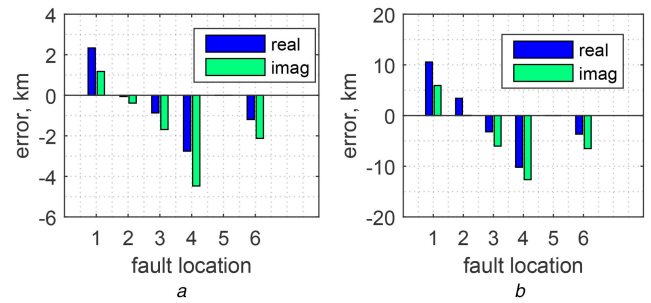
substation during fault at location 6 will be equal to the measured impedance during fault at location 3 regardless lengths of line TL5 and TL6. Error at location 1 is always positive that means that the relay preserves directional capability.

Finally, for the synchronised SV, fault locator based on the real part of the impedance gives more precise results.

4.2 Non-synchronised measurements and unideal communication channel

In this section, with the help of the communication network emulator, different imperfections of the communication channels are investigated and their impact on the proposed compensation strategy.

4.2.1 Constant time delays: Two cases are illustrated in Fig. 6: 0.5, 1 and 5 ms time delays are imposed upon SV received from the remote substation or DG. Fault is applied at location 2. The presence (1) and absence (0) of the tripping signals are shown as well as '[Zone 1 Zone 2]'.

For the case with the delays from the remote substation, Fig. 6*a*, the errors are small (all tripping signals appear) and dependency on the time delays is insignificant (for the real part). However, there is impact from the higher fault resistance seen as an increase of the errors.

For the case with the delays from the DG, Fig. 6*b*, the errors become considerably bigger and there is prominent dependency on the time delays. Influence of the fault resistances is also significant. As a consequence of either real or imaginary-based errors increase, not all tripping signals are present. It imposes strict requirements on synchronisation of SV from the DG with the substation measurements.

Since constant time delays can be compensated in advance, it is of interest to examine variable latencies.

4.2.2 Variable time delays: This subsection shows tests with variable time delays set as a random value (normal distribution) in the range between 1 and 5 ms for SV from the remote substation and 0.1–0.5 ms for the DG. Faults are applied in locations 1–4, 6 (30 consecutive faults for each location) with resistances 10 and 100 Ω.

Fig. 7*a* demonstrates distances calculated (on the basis of the real and the imaginary part of the measured impedance) from the
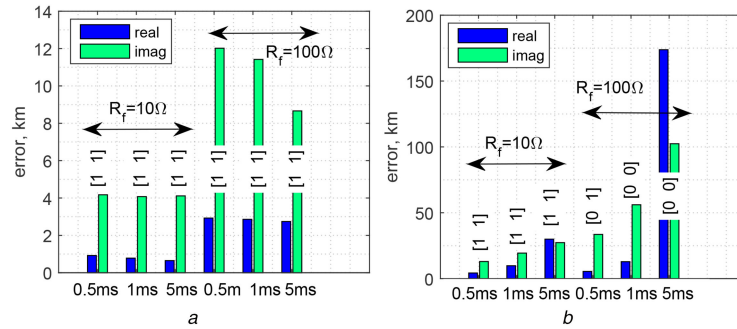
Fig. 6 *Fault location error with the compensator for different fault resistances and time delays set for SV from*
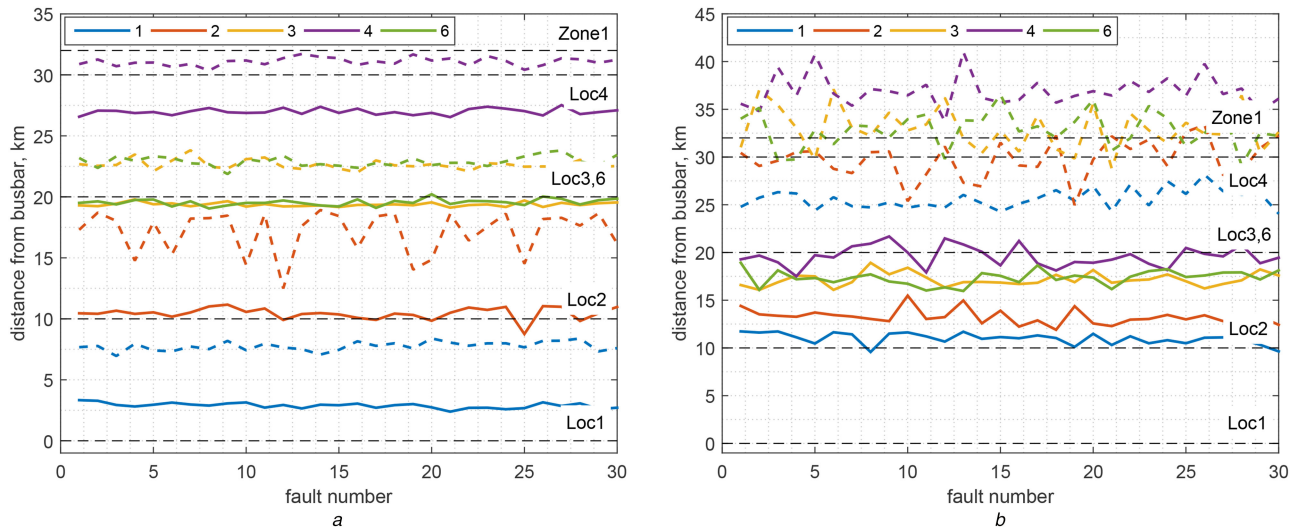*(a)* Remote substation, *(b)* DG

Fig. 7 *Calculated distances from the substation to fault (30 incidents for each location) based on the real (solid lines) and the imaginary (colour dashed) part with random delays*
(a) Low-ohmic faults, *(b)* High impedance faults. The black dashed lines are actual distances

substation to the low-ohmic faults. Comparing the values with the actual distances (the black dashed horizontal lines), we can notice that the real part gives more precise results for the faults at locations 1–3, 6, whereas for location 4 it is the imaginary part. Locations 3 and 6 are hardly differentiated due to the compensation method. Since all curves are under the line corresponding to Zone 1, all tripping signals properly appear.

Fig. 7*b* show the results for the high impedance faults. The fault location errors are considerably increased for location 1 and 4 (the real part). The dashed lines (the imaginary part) for locations 3, 6, 4 are mostly above the Zone 1 line that leads to disappearing of the tripping signal from Zone 1.

Such type of analysis can be used by utilities for estimation of impedance protection dependability (with the compensator) in case of jitters on communication paths and the absence of synchronised signals (disappearing of GPS signals, no access to the sky).

To sum up, communication time delays up to several milliseconds can compromise the method because they affect accuracy of impedance measurements especially in case of high impedance faults.

4.2.3 Data loss: This subsection demonstrates impact of the non-ideal communication links on the compensation strategy. The emulator models a network loss scenario where an arriving SV is dropped with a certain probability. Fig. 8 shows the fault location errors ('r' stands for values calculated on the basis of the real part, 'i' – for imaginary) for 30 consecutive 10-Ω faults applied at location 3 for two probabilities: 20 and 80%. Data loss is set separately for SV coming from the remote substation (Fig. 8*a*) and from the DG (Fig. 8*b*).

From both figures, it can be seen that 80% probability of data loss leads to bigger deviation in the errors. For SV from the DG, it might cause significant location errors and under-reaching

problems for the protection, Fig. 8*b* (80% case). The low probability does not have considerable influence on the method.

5 Conclusion

The current paper proposes the new protection method against interphase faults allowing compensation of non-zero fault impedances and remote infeed currents. The main advantages are increase of impedance relaying dependability in the MV feeder with the interconnected generator and possibility of accurate fault location. The main disadvantage is the requirement of the communication channels. The main outcomes of the presented research are as follows:

- The compensator helps reliably to produce the tripping signals with the synchronised data from the remote substations. It has inherent overreaching inaccuracy (measured impedance is less than actual) increasing with fault impedance.
- For faults behind the relay and in Zone 2, the compensator is not initialised preserving good directionality and selectivity.
- For estimation of fault location, the real part of the measured impedance must be utilised for better precision. Without additional measurements, faults on lateral brunches cannot be discriminated by the method.
- Unsynchronised SV from the remote substations lead to underreaching errors and may threaten protection dependability (especially for faults at the end of Zone 1). In such case, errors rise with time delays and fault resistance, and the biggest impact is observed if SV from the DG come with a latency.
- Time delays do not have negative influence for faults taking place outside of Zone 1 (absent of accidental unintentional tripping).
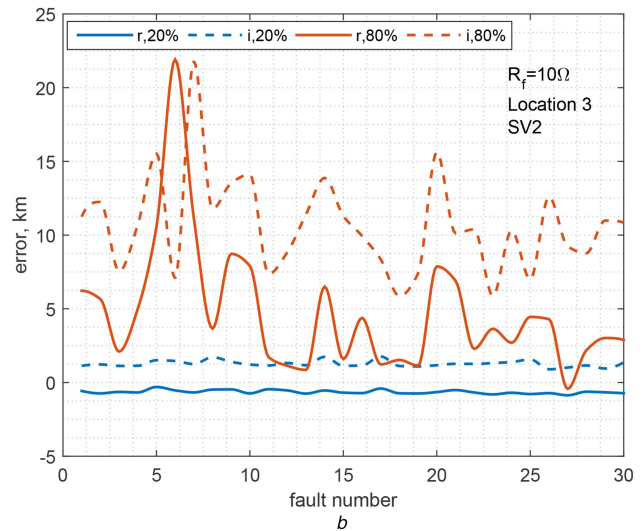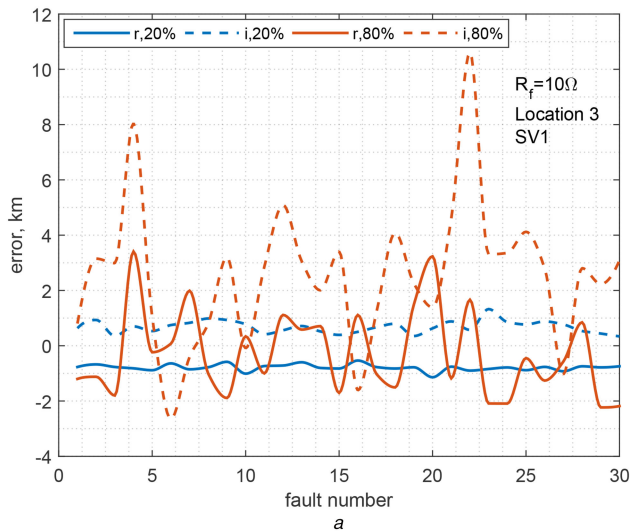
Fig. 8 *Fault location errors for low-ohmic fault at location 3 with 20 and 80% data loss probability set for SV from*
(a) Remote substation, *(b)* DG

- It is essential for faults in Zone 2 because the compensator is blocked in such case by the signal from the remote substation: it can arrive with a delay; however, tests have revealed that the method is still secure if Zone 1 has a sufficient operation time delay.
- For better performance of the protective method in case of high impedance faults, at least SV from the DG must be synchronised. It is stipulated by current inrush of the synchronous generator and, consequently, it might not be required for inverter interfaced DG (depends on control scheme), as well as for measurements coming from the passive part of the grid.
- High probability of data loss in the communication channels leads to underreaching errors and jeopardises protection reliability. Sufficient attention must be paid to the link from the DG since its quality has an essential impact.

These outcomes are valid for the applied three-phase faults. In the future work, double-phase faults will be presented with a more developed network including variable unbalanced loads.

6 References

[1] Pandakov, K., Høidalen, H.Kr., Marvik, J.I.: 'Implementation of distance relaying in distribution network with distributed generation'. 13th Int. Conf. Development in Power System Protection 2016 (DPSP), Edinburgh, Scotland, United Kingdom, 7–10 March 2016, pp. 1–7

[2] Saha, M.M., Izykowski, J., Rosolowski, E., *et al.*: 'Adaptive line distance protection with compensation for remote end infeed'. IET 9th Int. Conf. Developments in Power System Protection 2008 (DPSP), Glasgow, Scotland, United Kingdom, 17–20 March 2008, pp. 1–6

[3] Makwana, V.H., Bhalja, B.R.: 'A new digital distance relaying scheme for compensation of high-resistance faults on transmission line', *IEEE Trans. Power Deliv.*, 2012, **27**, (4), pp. 2133–2140

[4] Sarangi, S., Pradhan, A.K.: 'Adaptive direct under-reaching transfer trip protection scheme for the three-terminal line', *IEEE Trans. Power Deliv.*, 2015, **30**, (6), pp. 2383–2391

[5] Al-Emadi, N.A., Ghorbani, A., Mehrjerdi, H.: 'Synchrophasor-based backup distance protection of multi-terminal transmission lines', *IET Gener. Transm. Distrib.*, 2016, **10**, (13), pp. 3304–3313

[6] Yutao, Q., Anwei, C., Lvyi, S., *et al.*: 'A pilot protection method of T-connected transmission lines'. IEEE Int. Conf. Power and Power and Renewable Energy (ICPRE), Shanghai, China, 21–23 October 2016, pp. 1–4

[7] Ma, J., Li, J., Wang, Z.: 'An adaptive distance protection scheme for distribution system with distributed generation'. 5th Int. Conf. Critical Infrastructure (CRIS), Beijing, China, 20–22 September 2010, pp. 1–4

[8] Huang, W., Nengling, T., Zheng, X., *et al.*: 'An impedance protection scheme for feeders of active distribution networks', *IEEE Trans. Power Deliv.*, 2014, **29**, (4), pp. 1591–1602

[9] Marvik, J.I., Høidalen, H.K., Petterteig, A.: 'Localization of short-circuits on a medium voltage feeder with distributed generation'. 20th Int. Conf. Exhibition on Electricity Distribution (CIRED 2009) – Part 1, Prague, Czech Republic, 8–11 June 2009, pp. 1–4

[10] Liu, Z., Høidalen, H.K.: 'An adaptive inverse time over-current relay model implementation for real time simulation and hardware-in-the-loop testing'. 13th Int. Conf. Development in Power System Protection 2016 (DPSP), Edinburgh, Scotland, United Kingdom, 7–10 March 2016, pp. 1–6

[11] Adrah, C.M., Kure, Ø., Liu, Z., *et al.*: 'Communication network modeling for real-time HIL power system protection test bench'. IEEE PES PowerAfrica, Accra, Ghana, 27–30 June 2017, pp. 1–6

[12] Andrade, V.D., Sorrentino, E.: 'Typical expected values of the fault resistance in power systems'. 2010 IEEE/PES Transmission and Distribution Conf. Exposition: Latin America (T&D-LA), Sao Paulo, Brazil, 8–10 November 2010, pp. 1–8