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Register-Aware Optimizations for Parallel Sparse Matrix-Matrix Multiplication

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Abstract General sparse matrix-matrix multiplication (SpGEMM) is a fundamental building block of a number of high-level algorithms and real-world applications. In recent years, several efficient SpGEMM algorithms have been proposed for many-core processors such as GPUs. However, their implementations of sparse accumulators, the core component of SpGEMM, mostly use low speed on-chip shared memory and global memory, and high speed registers are seriously underutilised. In this paper, we propose three novel register-aware SpGEMM algorithms for three representative sparse accumulators, i.e., sort, merge and hash, respectively. We fully utilise the GPU registers to fetch data, finish computations and store results out. In the experiments, our algorithms deliver excellent performance on a benchmark suite including 205 sparse matrices from the SuiteSparse Matrix Collection. Specifically, on an Nvidia Pascal P100 GPU, our three register-aware sparse accumulators achieve on average 2.0x (up to 5.4x), 2.6x (up to 10.5x) and 1.7x (up to 5.2x) speedups over their original implementations in libraries bhSPARSE, RMerge and NSPARSE, respectively.

Keywords Sparse matrix · Sparse matrix-matrix multiplication · GPU · Register

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1 Introduction

General sparse matrix-matrix multiplication (SpGEMM) operation multiplies a sparse matrix A with a sparse matrix B and generates a resulting sparse matrix C. This is an essential building block in a number of applications such as algebraic multigrid methods [1], shortest path algorithms [2], breadth first search algorithms [3], and Markov cluster algorithms [4]. It is also an important kernel in the GraphBLAS standard [5,6]. As a result, fast algorithms for parallel SpGEMM received much more attention in recent years [7–23].

The most basic way to calculate SpGEMM is the row-by-row method proposed by Gustavson [24] that multiplies each row of A with the whole matrix B for the corresponding row of C. So the SpGEMM computation becomes a combination of a number of sparse vector-matrix multiplications, i.e., so-called sparse accumulators, which is different with the sparse matrix-vector multiplication [25–28]. Because the rows are independent of each other, they can be easily parallelized on modern many-core processors. Since GPUs provide higher computational power in terms of the theoretical peak floating-point operations and memory bandwidth, several SpGEMM algorithms, in particular various sparse accumulators, have been proposed for GPUs [7,8,11,29, 30]. Moreover, to achieve better load balancing, several studies [11,29] create a couple of tens of bins and then group rows requiring the similar number of floating point operations into the same bin.

The compute for each row includes traversing nonzeros a_{ij} of the ith row of A and accumulating all nonzeros in the jth rows of B into the ith row of C. To efficiently accumulate the nonzeros from different rows of B, different sparse accumulators have been developed. The dense-based [31], sort-based [7, 32], heap-based [29], merge-based [30] and hash-based algorithms [8,11,33] are representative methods. All methods can be applied to bins of different sizes. For bins accumulating a small number of nonzeros (in general no more than 512), the compute can be completed in on-chip shared memory for fast processing. On the other hand, the longer bins have to be finished in global memory due to the limited size of the shared memory.

Besides shared memory and global memory, thread registers have proven to be another very efficient alternative memory level to build fast algorithms. Li et al. [34,35] pointed out that register reuse and communication are crucial for more fine-grained GPU execution model. Rawat et al. [36] used GPU registers for improving various stencil computations. However, for SpGEMM computation, although the overhead associated with the global memory accesses can be reduced to a certain extent by performing the shared memory-based sorting or hashing operation on the sub-matrices [9,30], an efficient utilisation of the GPU registers for SpGEMM is not foreseeable and the best performance is not achieved yet.

Motivated by the underuse of registers in recent SpGEMM algorithms, we in this paper propose three register-aware algorithms, i.e., sort-, merge- and hash-based, to improve the performance of SpGEMM, in particular for matrices including bins of moderate sizes (i.e., the number of intermediate products

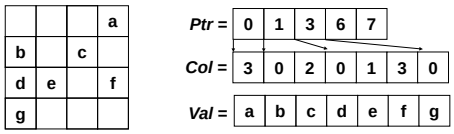


Fig. 1: A sparse matrix and its CSR format.

is smaller than 512). Specifically, we use register to load entries from global memory and store intermediate products calculated into shared memory, then load them back to registers to work in a load balanced way and to implement new primitives for fully using various in-register communication schemes.

The main contributions of this paper include proposing three register-aware SpGEMM algorithms, relying on the sort-, merge- and hash-based sparse accumulators, respectively, and achieving significantly improved performance over state-of-the-art libraries. Specifically, on an Nvidia Pascal P100 GPU, our three register-aware sparse accumulators achieve on average 2.0x (up to 5.4x), 2.6x (up to 10.5x) and 1.7x (up to 5.2x) speedups over their original implementations in libraries bhSPARSE [18], RMerge [30] and NSPARSE [11], respectively.

2 Background

2.1 Sparse Matrix

To avoid storing and calculating zeros, some matrices can be stored in their sparse form. The most widely used storage scheme is the so-called Compressed Sparse Row (CSR) format. Figure 1 shows a sparse matrix and its CSR storage. The CSR format consists of three arrays, namely Val, Col and Ptr. The Val array stores values, and the Col array stores column indexes of the nonzero entries. The third array Ptr records the starting storage position (or offset) of each row in the arrays Val and Col, thus the number of the nonzero entries in the ith row of matrix can be calculated by $Ptr[i+1] - Ptr[i]$.

2.2 SpGEMM and Sparse Accumulator

SpGEMM operation $C = AB$ multiplies two sparse matrices A and B, and obtains a sparse matrix C. Figure 2 gives an example. It can be seen that SpGEMM can be calculated row-by-row, and can be parallelized easily since rows are independent of each other. As a result, the SpGEMM operation becomes a group of sparse vector-matrix multiplication[1] $c = aB$, where c and a are sparse vectors of C and A, respectively.

[1] This should not be confused with sparse matrix-vector multiplication (SpMV), which multiplies a sparse matrix with a dense vector and obtains a dense vector.

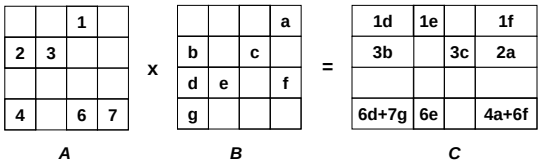


Fig. 2: An illustration of the SpGEMM operation.

This $c = aB$ operation is also known as sparse accumulator. Based on the expression, the computation of each output row c converts to the sum of the intermediate products, namely the rows of B that are selected and scaled by the nonzero elements of a. For example, when we compute the last row of C in Figure 2, we multiply the first element of the last row of A, i.e. $a_{30} = 4$, by the $0th$ row of B, i.e., $b_0 = \{a\}$, obtaining one intermediate product $c_{33} = 4a$. Then we multiply the second element of the last row of A, i.e. $a_{32} = 6$, by the $2nd$ row of B, i.e., $b_2 = \{d, e, f\}$, and obtain three intermediate products $c_{30} = 6d$, $c_{31} = 6e$, and $c_{33} = 6f$. Finally, we multiply the last element of the last row of A, i.e. $a_{33} = 7$, by the $3rd$ row of B, i.e., $b_3 = \{g\}$, to obtain $c_{30} = 7g$. For getting the last row of C, these intermediate products with the same column indexes need to be summed up. Specifically, two intermediate products $6d$ and $7g$ are summed up into c_{30}, and $4a$ and $6f$ are summed up into c_{33}. Otherwise the intermediate products without the same column indexes only need to insert themselves to the final results of c. In this case, c_{31} only needs an insertion.

2.3 Three Implementations of Sparse Accumulator

There are three typical algorithms, i.e., sort-based [7,29], merge-based [30], and hash-based [8,33,11], for implementing sparse accumulator. Also using the last row in Figure 2 as an example, sort-based sparse accumulator first sorts the five intermediate products $\{4a\}$, $\{6d, 6g, 6f\}$ and $\{7g\}$ according to their column indexes to obtain a sequence $\{6d, 7g, 6e, 4a, 6f\}$ and calls a segmented sum primitive to sum up values in the same segment (with the same column index) to obtain the final results $\{6d + 7g, 6e, 4a + 6f\}$.

The merge-based sparse accumulator runs in multiple iterations, and each iteration vertically merges one element of the resulting sparse vector. In our case, the first round merges $\{4a\}$, $\{6d\}$ and $\{7g\}$, and calculates out $\{6d+7g\}$. In the second round, $\{4a\}$ and $\{6e\}$ are merged and $\{6e\}$ is computed out. In the final round, $\{4a\}$ and $\{6f\}$ are merged into $\{4a + 6f\}$.

The hash-based sparse accumulator takes advantage of the hash functions to fast locate the positions of $\{4a\}$, $\{6d, 6g, 6f\}$ and $\{7g\}$ and to accumulate the values with the same column indexes. If conflict occurs, linear probing can be used for finding out an empty position for inserting the entry and the procedure will ensure to finish if memory space is enough large.

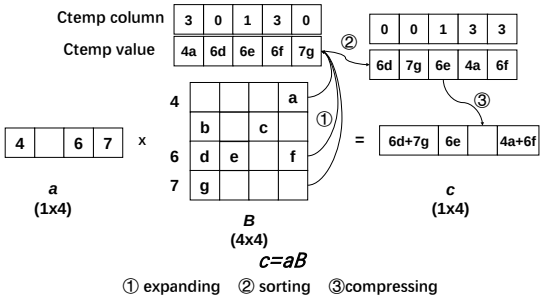


Fig. 3: Original sort implementation.

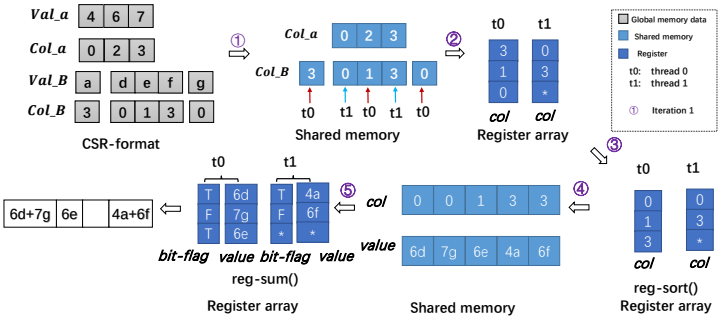


Fig. 4: Our `reg-sort` method.

The three methods are plotted in Figures 3, 5 and 7, respectively, and will be further explained along with our register-aware optimizations later on.

3 Methodology

3.1 Reg-sort: Register-Aware Sort-based Sparse Accumulator

Sort-based sparse accumulator [7,29] shown in Figure 3 has three phases: expanding, sorting and compressing. The expanding phase first generates the intermediate products, namely the rows of B that are selected and scaled by the nonzero elements of a, stored in two arrays $Ctemp\,column$ and $Ctemp\,value$ in shared memory. The second sorting phase sorts the intermediate products in the two arrays according to the $Ctemp\,column$ index in shared memory. The last compressing phase sums the values with the same column index. It can be seen that in the original implementations, all operations should be completed in shared memory, since entries stored in random locations need to compare, move and sum up.

Fortunately, there are still some patterns can be exploited. Hou et al. [32] pointed out that sorting network can be implemented more efficiently by using an N-to-M pattern that uses N threads to sort M entries inside registers. Also,

Blelloch et al. [37] developed a vectorized method for parallel segmented sum which is also used in SpMV computation [38]. We utilise the two methods in GPU registers for our sparse accumulator. To our knowledge, this is for the first time that the two methods are implemented for GPU registers.

Figure 4 shows five steps of our `reg-sort` algorithm for completing the same work in Figure 3, i.e., calculating $c = aB$ for the last row of the matrix in the Figure 2. We here use two threads to compute, and each thread has three registers allocated. We in the first step fetch and compute the corresponding intermediate products $\{4a\}$, $\{6d, 6g, 6f\}$ and $\{7g\}$ into the shared memory. In the second step, each thread fetches data from the shared memory to its own register vectors. Specifically, thread 0 gets column indexes $\{3, 1, 0\}$, and thread 1 gets $\{0, 3\}$. Then in the third step we use the N-to-M sorting network pattern for sorting the data in the register. Here the thread shuffle instructions are heavily used for comparing and moving entries between threads. After this step, the two threads store $\{0, 1, 3\}$ and $\{0, 3\}$ in their registers, respectively. Then in the fourth step, the column indexes are stored back to shared memory. In the fifth step, we load the values to register in a transposed pattern, meaning that the two threads now have $\{6d, 7g, 6e\}$ and $\{4a, 6f\}$, respectively. To label which values are to be summed up, we allocate an extra bit-flag register vector for each thread to support the parallel segmented sum. In this example, the bit-flag array has a TRUE flag at the beginning of each same column index segment, and has a FALSE otherwise. So the two threads now have $\{T, F, T\}$ and $\{T, F\}$, respectively. In the procedure of segmented sum, each thread first sums up values in the local segments, and communicate with the other thread to get values across different threads. Finally, the values summed up will stored in the positions with bit-flag TRUE. After the five steps, those values are stored to the global memory directly since their positions are already known.

Compared with the original method, the time consuming operations including sorting and compression are now all calculated inside registers. Though shared memory is still needed to use for exchanging data between the above steps, there is no need to use it for heavy computes and data movement.

3.2 Reg-merge: Register-Aware Merge-based Sparse Accumulator

Figure 5 shows the merge-based sparse accumulator. This method has two stages. The first stage is dividing the matrix A into small sub-matrices, if the maximum row length of the first matrix is smaller than the warp size 32, this row will be performed in the shared memory. The second stage is using one warp to multiply the sub-matrices by the second input matrix B.

We still take the last row of the matrix in Figure 2 as an example. Suppose we have four threads in one warp. Since the warp size is larger than the row length of a, the first stage of dividing the matrix into sub-matrices is not required. In the second stage, the rows of B corresponding to $\{4, 6, 7\}$, i.e., $\{a\}$, $\{d, e, f\}$ and $\{g\}$, are merged at first. The process of merging is sequential. Each thread needs to compute the minimum column index of the output row

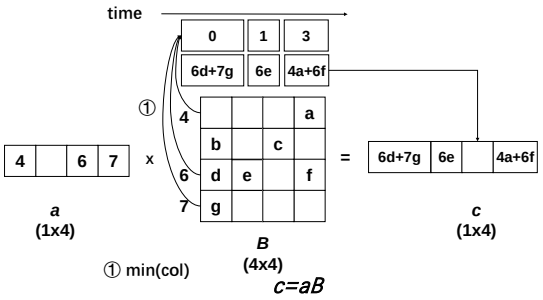


Fig. 5: Original merge implementation.

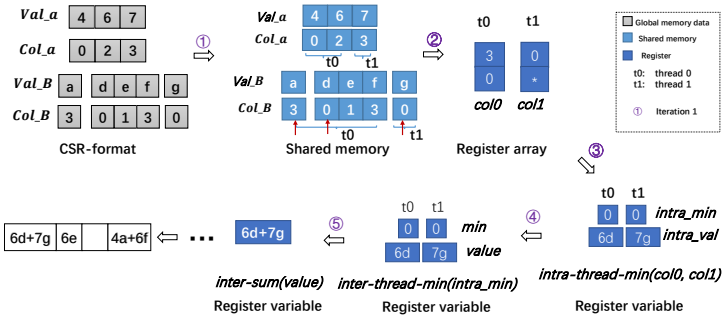


Fig. 6: Our `reg-merge` method.

c, namely $\{0\}$ in this case. Then the value of the corresponding column index $\{0\}$ of each thread is summed up using the register shuffle instructions, and the first entry $\{6d+7g\}$ is obtained. Then in the second iteration, the second entry of c is acquired. After the third iteration, all of the entries of c is obtained. This method has a disadvantage that the first stage, i.e., dividing the first input matrix into sub-matrices, consumes relatively high cost in the whole process of SpGEMM. For reducing the cost of the first stage, we devise `reg-merge` method to use more registers to make more work done in each thread. As follows we illustrate how the register merge-based algorithm computes the output row $c = aB$ using the threads within a warp.

Figure 6 shows our `reg-merge` method by using the last row of the case in Figure 2 of Section 2.2. At first the data is fetched from global memory to shared memory. The first two elements of a and the corresponding two rows of B is assigned to thread 0, and thread 1 processes the last element of a and the corresponding last row of B. In the second step, each thread fetch two column indexes of its corresponding data from shared memory to its own register vectors, which lengths are 2 in this example. For thread 1, it only has one element, so its second value of the register vector is INTMAX. Then, each thread performs an $intra - thread - min(col0, col1)$ function to obtain the private minimum column index $intra\_min$ of each private register

vector, i.e., 0 for thread 0 and 0 for thread 1 in this case. At the same time, each thread gets the scaled corresponding intermediate products for each $intra\_min$ column index, i.e., $6d$ for thread 0 and $7g$ for thread 1. Next, each thread performs $inter{-}thread{-}min(intra\_min)$ function to get the minimum column index across the threads at the same warp. The minimum column index across the two threads are stored to the register variable min of each thread and the corresponding scaled values are stored to the register variable $value$. The $inter - thread - min()$ function is implemented by the GPU register shuffle instructions and each thread can get the minimum value of each thread at the same time in the same variable names. After that, in the fifth step, using the $inter - sum(value)$ function, each thread can obtain the reduction sum of the two threads, i.e., $6d + 7g$, the first element of the output c. The $inter - sum()$ function is also implemented by the GPU register shuffle instructions and each thread can acquire the same reduction sum of the two threads. Using the same process, we can obtain the other two elements of c, i.e., $6e$ and $4a + 6f$. Then computing the row of C is completed.

Compared with the original method, the time consuming operations including dividing the matrix into sub-matrices in the global memory is now completely eliminated and all of the intermediate products are calculated inside registers.

3.3 Reg-hash: Register-Aware Hash-based Sparse Accumulator

Hash-based sparse accumulator [8,33,11] shown in Figure 7 also has three phases. The first phase is the hashing operations. It allocates a memory space of the size of the number of intermediate products, namely the rows of B that are selected and scaled by the nonzero elements of a, as the hash table. It uses the column index of these intermediate products as the key, and is able to leverage different hash methods to implement SpGEMM. For the values with the same key, the scaled values need to be summed together to get one entry of the output c. All of these operations are completed in the shared memory using the atomic function $atomicCAS()$ to sequentially access the same position of the hash table for each thread. After the hash operations, it needs to shrink the hash table to a dense state, i.e., putting the three effective values $\{4a + 6f, 6e, 6d + 7g\}$ to the first three positions of the hash table as shown in Figure 7. At last, sort the values of these elements of c according to their column indexes to obtain the final compressed storage format. In this case, we take two threads to accomplish the computing of the row. The hash operations need four iterations: 1) thread 0 puts $\{4a\}$ and thread 1 puts nothing to the hash table; 2) thread 0 puts $\{6d\}$ and thread 1 puts $\{6f\}$ to the hash table; 3) thread 0 puts $\{6f\}$ and thread 1 puts nothing to the hash table; 4) thread 0 puts $\{7g\}$ and thread 1 put nothing to the hash table.

In our register-based hash `reg-hash` algorithm, we optimize the data allocations of each thread, rather than implementing the hash table in registers. Also, we take the example of $c = aB$ in Section 2.2 to illustrate the process

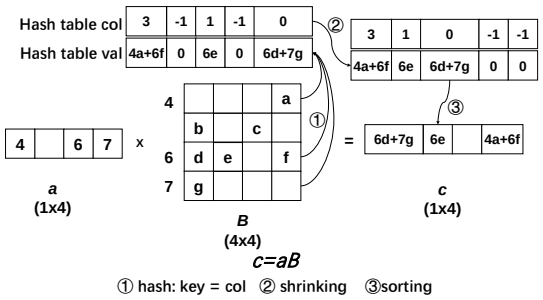


Fig. 7: Original hash implementation.

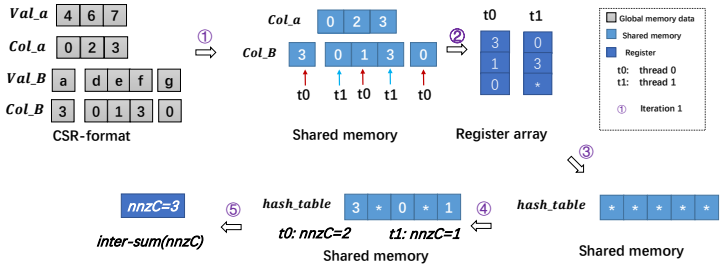


Fig. 8: Our `reg-hash` method.

of our `reg-hash` algorithm, as shown in Figure 8. In this case, we use two threads to compute $c = aB$. Each thread has a register vector with the size of three. At first, we load data from the input matrices to the shared memory as shown in the first step of Figure 8. After that, each thread fetches data from the shared memory to its own register vectors alternately. Thread 0 gets the column index data {3}, {1}, and {0} to its register vectors, and thread 1 gets the column index data {0} and {3} to its register vectors. The computing of the indexes is a bit more complex. We need to compute both the index of the shared memory tables and the register arrays precisely. In the third steps, the hash table shared by the two threads in the shared memory is initialized. Then, each thread fetches the data from its register arrays to perform the hash operations of the hash table in the shared memory. The hash operations need three iterations: 1) thread 0 puts{3} and thread 1 puts {0} to the hash table; 2) thread 0 puts {1} and thread 1 puts {3} to the hash table; 3) thread 0 puts {0} and thread 1 puts nothing to the hash table. The number of times of accessing shared memory is less than that of the original hash method, leading to the performance improvement. Each thread has its private register variable $nnzC$ to record the partial number of nonzeros of the output c for each thread. For the hash operations, the $nnzC$ with the same key of each thread, namely the same column index, is only accumulated once for each threads. We use the atomic function $atomicCAS()$ to guarantee accuracy of parallel hash operations. At last, in the fifth step, the same function $inter - sum(nnzC)$

of `reg-merge` is performed by each thread to obtain the total sum of partial number of nonzeros of the output c, i.e., $nnzC$ of each threads. Finally, the real size of c is acquired. We use the `reg-hash` to compute the size of the output matrix.

Compared with the original hash method, though shared memory is still needed to use for hash operations, the total number of shared memory hash operation can decrease significantly, since now the intermediate products are well organized and accumulated into their final positions in a load balanced way.

3.4 Implementation Details

For the computation of each row of C, the numbers of the floating point operations, twice the number of intermediate products, can vary greatly because of the various sparsity structures of the two input matrices A and B. To achieve load balanced calculation on GPUs, we create a couple of bins and then groups rows requiring the similar number of floating point operations into the same bin. Here we focus on the rows having intermediate products between 0 to 512. We divide those rows into nine bins according to their intermediate products. The number of intermediate products is $0-2$ for bin0, $3-4$ for bin1, $5-8$ for bin2, $9-16$ for bin3, $17-32$ for bin4, $33-64$ for bin5, $65-128$ for bin6, $129-256$ for bin7, and $257-512$ for bin8.

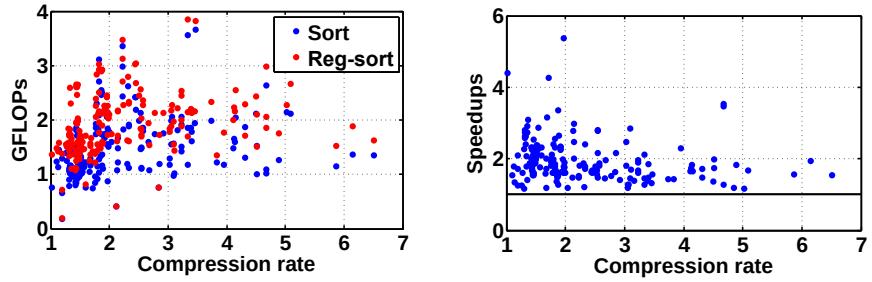
The register number for each method used in each thread is different. For `reg-sort` and `reg-hash`, each thread uses the register vector with the size of 8. For `reg-merge`, each thread can use the register vector with the size of 2, 4, 8, 16 or 32, depending on the length of the rows of the first input matrix of SpGEMM.

4 Evaluation

The experimental evaluation is conducted on an Nvidia Pascal P100 GPU (3584 CUDA cores and 16GB HBM2 memory) hosted by an Intel Xeon server. The programs are all compiled by CUDA v8.0 and Intel C/C++ compiler v18.

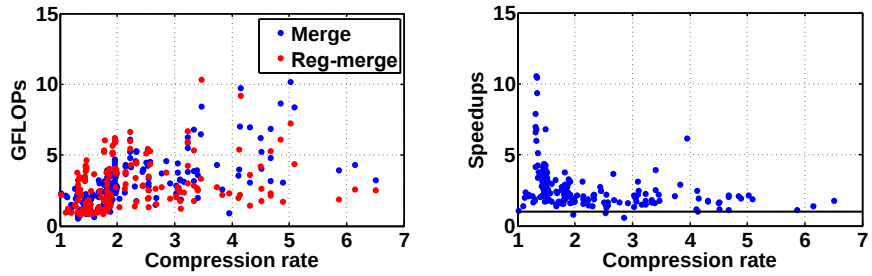
As for the benchmark suite, we first select 956 enough large matrices used in our previous work [16] (with the number of nonzeros no less than 100K and no more than 200M) from in total 2757 sparse matrices in the SuiteSparse Matrix Collection [39]. For SpGEMM operation, we also calculate $C = A^2$ to align with the existing work [7,11,29,30]. Furthermore, to clearly show the effectiveness of the participating algorithms, we select 205 matrices which with over 95% of their rows are small enough (calculating no more than 512 intermediate products in the rows of C) to use on-chip memories.

Our algorithms are compared with three state-of-the-art SpGEMM methods in bhSPARSE [29], RMerge [30] and NSPARSE [11] on GPU. Figures 9, 10 and 11 show the overall performance (their left side) and kernel performance (their right side) of the three methods and our register-aware optimization



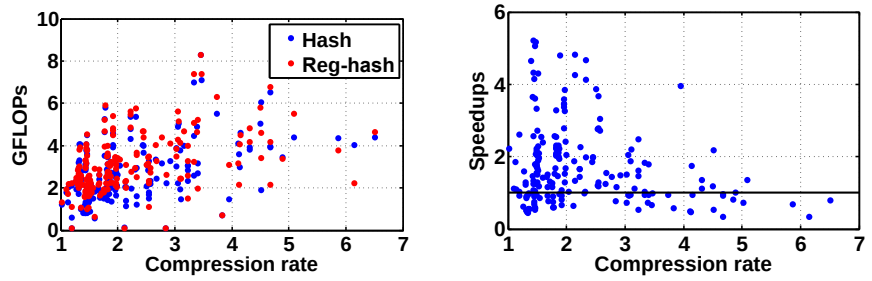
(a) Overall performance. (b) Kernel speedups.

Fig. 9: The performance and speedups of the `reg-sort` method.



(a) Overall performance. (b) Kernel speedups.

Fig. 10: The performance and speedups of the `reg-merge` method.



(a) Overall performance. (b) Kernel speedups.

Fig. 11: The performance and speedups of the `reg-hash` method.

methods, respectively. The overall performance is evaluated in terms of GFLOPs (floating point operations per second) in double-precision, and the kernel performance is shown in speedups of our sparse accumulators over their original implementations. The x-axis is the factor *compression rate* denoting the ratio of the number of intermediate products and the number of nonzeros of the output matrix C.

In Figures 9a, 10a and 11a, it can be seen that the performance of our register-aware optimization in general brings better performance over bhSPARSE, RMerge and NSPARSE. We obtain average 1.3x (up to 2.0x), 1.1x (up to 5.4x), and 1.2x (up to 2.7x) speedups for the overall performance over the three methods, respectively. In the `reg-sort` method, the speedups mostly come from the fast in-register implementations of sorting network and segmented sum. Matrices *Baumann*, *ncvxqp3*, and *wathen120* obtain the speedups of 2.0x, 1.9x and 1.9x, respectively. For `reg-merge`, the improvements of the performance mainly comes from assigning more work to each thread, and reducing the expensive global and shared memory accesses. Matrices *netherlands_osm*, *road_central* and *great-britain_osm* obtain 5.4x, 5.2x, and 4.7x speedups, respectively. As for `reg-hash`, the improvement of the performance is most from more balanced workload when performing the hash operations. Matrices *ASIC_100ks*, *al2010* and *id2010* obtain the speedups of 2.7x, 2.3x, and 2.3x, respectively.

Figures 9b, 10b, and 11b compare the pure performance of sparse accumulators including load and store cost between global memory and on-chip memory and compute overhead. In other words, it is the execution time of all CUDA kernels to finish an SpGEMM operation. Overall, our three implementations obtain average speedups 2.0x (up to 5.4x), 2.6x (up to 10.5x), and 1.7x (up to 5.2x) over bhSPARSE, RMerge and NSPARSE, respectively. Those kernel speedups are higher than the full SpGEMM, since the complete SpGEMM algorithm also includes binning, memory allocation and possible data copy overhead. In detail, for `reg-sort`, matrices *Baumann*, *ch7-8-b5*, *ncvxqp3* obtain the highest speedups 5.4x, 4.4x, and 4.3x, respectively. For `reg-merge`, matrices *europe_osm*, *road_usa*, *road_central* obtain the highest speedups 10.5x, 10.4x, and 9.3x, respectively. For `reg-hash`, matrices *id2010*, *al2010*, *co2010* obtain the highest speedups 5.2x, 5.2x, and 5.1x, respectively. It is also worth to note that kernel performance of `reg-sort` and `reg-merge` is almost constantly better than the original method, while `reg-hash` is not always better than the original one. The reason is that some matrices already bring rather good load balancing and adequate floating point operations. Thus the load balanced computations may lead to lower performance.

5 Related Work

There has been much work focusing on **parallel SpGEMM algorithms**. Bell et al. [1] developed the ESC (expanding, sorting and compressing) method, and Dalton et al. further improved it for better locality [7] and better load balancing [40]. Liu and Vinter [29] grouped rows into 37 bins and utilized various sorting algorithms, i.e., heap sort, bitonic sort and mergepath sort, for different bins. Gremse et al. [30] merged rows of B in a vertical way. Demouth [8] for the first time used hash table for sparse accumulator, and both Pham et al. [33] and Nagasaka et al. [11] took load balancing into consideration in hash methods. Deveci et al. [23] used hash methods on KNL and GPUs.

Moreover, Buluç et al. [12], Azad et al. [13], Ballard et al. [14], Akbudak et al. [10] and Nagasaka et al. [20] proposed various novel SpGEMM algorithms for many-core x86 processors and distributed memory machines. Besides, for the sparse matrix problem, the memory bandwidth is also an important factor to analyse [41].

Additionally, **GPU registers** have been proven to be an effective tool for implementing faster execution models and algorithms. For example, Li et al. [34,35] pointed out that register reuse and communication are crucial for more fine-grained GPU execution model. Rawat et al. [36] demonstrated that various stencil computations can be accelerated through GPU registers. Xie et al. [42] designs a framework to allocate the registers by analyzing the lifetime of variables.

In spite of the previous efforts, register-aware optimization is still not well studied for SpGEMM algorithms. Compared to the existing literature, our work presented in this paper exploits GPU registers to improve three representative sparse accumulators, i.e., sort, merge and hash, in various SpGEMM algorithms and achieves significant speedups on modern GPUs.

6 Conclusion

We in this paper have proposed three register-aware optimization techniques to improve performance of SpGEMM. The three newly implemented sparse accumulators covered representative parallel primitives, i.e., sort, merge and hash, and demonstrated significant speedups over their original implementations. To our knowledge, this is for the first time that registers are fully utilised for accelerating SpGEMM on massively parallel architectures. In the future, we would like to explore the relationship between the features of sparse matrices and the three different spare accumulators, and exploit the data reuse of SpGEMM [43]. Furthermore, we are interested in performing our algorithms to the real world applications using existing autotuning technologies [44,45].

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