Challenges of SiC MOSFET Power Cycling Methodology

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Keywords

«Silicon Carbide (SiC) », «MOSFET», «Power Cycling», «Reliability»

Abstract

This paper investigates the power cycling methodology for reliability testing of SiC metal-oxide-semiconductor field-effect transistors (MOSFETs). Dedicated test benches were designed and built to study this issue. The results indicate that power cycling of SiC MOSFETs is affected by threshold voltage instability. A proposal for reducing the influence of the latter is also given. This is done by adding an additional gate pulse to the device under test, in order to achieve an average bias of zero during one cycle of the power cycling experiment.

Introduction

The potential advantages of SiC power semiconductors, compared to their Silicon (Si) counterparts, have been shown in the literature. These include, among others, higher operating temperature, higher voltage ratings for a given chip thickness and higher thermal conductivity [1], as well as, faster switching speeds [2]. On the other hand, the more than three times higher Young's Modulus of SiC over Si renders SiC devices much stiffer [1]. This can potentially reduce the lifetime of the device; however, this also depends on the other utilized materials in the packaging. Thus, it is imperative to test reliability before wide-spread use of SiC devices can be established. Due to being one of the most attractive SiC devices currently commercially available, only the SiC MOSFET will be considered in the investigations presented in this paper.

The accelerated lifetime power cycling test is well established in order to assess the reliability of Si IGBTs. This makes the method interesting for assessing reliability of new components such as the SiC MOSFET. Only a few power cycling experiments with SiC devices have been performed in the literature [3-6]. However, a suitable common practice of the method needs to be established for the SiC MOSFET.

This paper investigates the methodology for performing power cycling of SiC MOSFETs. The $V_{SD}(T)$-method [4] is used to estimate the device junction temperature. It is shown that the power cycling procedure should be refined due to potential drift of the threshold voltage of the device. Threshold voltage instability has been a known issue for SiC MOSFETs [7]. Despite improvements in devices, threshold voltage instability must still be taken into account during testing and design. In this paper, the threshold voltage instability and appropriate power cycling methodology for SiC MOSFETs are presented. In particular, the utilized experimental set-ups are described, whereas various reliability

assessment results of SiC MOSFETs are presented and discussed. Finally, a proposal on how the test methodology might be modified in order to reduce the influence of the threshold voltage drift on the power cycling test is also proposed.

Theory

Threshold Voltage Instability

The early SiC MOSFET generations were highly affected by the threshold voltage instability. Although recent generations have shown an improved performance in this regard, they are still vulnerable to threshold voltage variations [7]. The physical mechanisms responsible for the instability are not fully understood, yet charging and neutralization of near-interfacial oxide traps via tunneling is believed to be the main mechanism [7]. The instability consists of a drift of the threshold voltage after application of a gate-source bias. The polarity of the bias determines the direction of the drift, whereas the magnitude and duration affects the magnitude of the drift. The temperature at which the bias occurs also affects the instability [7].

Power Cycling Test

Accelerated power cycling is a lifetime stress test that can be used to assess reliability of packaging and lifetime of power semiconductor devices [3]. The Device Under Test (DUT) is cycled until the device reaches one of the following two failure criteria [8, p 392]: Increase in the on-state voltage of the DUT right before the load current through the device is switched off, $V_{DS,warm}$, by 5 %, or increase in the thermal resistance of the DUT, R_{th}, by 20%.

As it is not possible to measure the junction temperature directly without destroying the semiconductor packaging, an indirect measurement method is necessary. By utilizing a thermo-sensitive electrical parameter (TSEP), the junction temperature is estimated by utilizing the dependency of an electrical parameter on temperature. One possible TSEP is the source-drain voltage of the MOSFET [4]. This method is called the $V_{SD}(T)$-method and estimates the junction temperature by measuring the voltage drop across the source-drain terminals when a small, constant current is conducted through the body diode. As the estimated temperature is not the actual junction temperature, it is termed the virtual junction temperature, T_{vj}.

The $V_{SD}(T)$-method may only be utilized if the current flows exclusively through the PN junction formed by the body diode. If a portion of the current flows through the channel of the MOSFET, the method would not be applicable. More specifically, this portion of the current would change in the event of a drift of the threshold voltage. Furthermore, since the body diode has a negative temperature coefficient while that of the channel is positive, a change in temperature would lead to a different current distribution between the two. Hence, even without threshold voltage drift, a constant current through the body diode cannot be sustained if the channel conducts a part of the current. To ensure that the channel is completely closed, a sufficiently negative gate-source voltage needs to be applied.

Herold et al. have experimentally shown that $V_{GS} = -6\,\mathrm{V}$ is the voltage at which the channel of the MOSFET is completely closed [4]. However, due to the potentially different gate structure layouts between SiC MOSFET manufacturers, the value at which the channel is completely closed may vary. Before utilizing the $V_{SD}(T)$-method with a specific SiC MOSFET, it is thus necessary to determine at which V_{GS} the channel turns off. When the entire current flows through the internal diode, the slope of the source-drain voltage as a function of temperature is constant. This holds because the voltage across a pn-junction experiencing a constant current is linearly dependent on temperature [8, p.96]. Thus, by evaluating the following expression:

$$\frac{\partial}{\partial V_{GS}} \frac{\partial V_{SD}(T)}{\partial T} = 0, \tag{1}$$

it is possible to determine when the channel is completely closed. To evaluate this, consider Fig. 1, in which the derivative of $V_{SD}(T)$ with respect to temperature is plotted as a function of V_{GS}. Clearly, the derivative of the curve is only zero for $V_{GS} < -6.5$ V, which thus necessitates a gate-source voltage less than this value in order to ensure that the channel is closed for this particular device. Similar investigations can also be performed for various types of SiC MOSFETs.

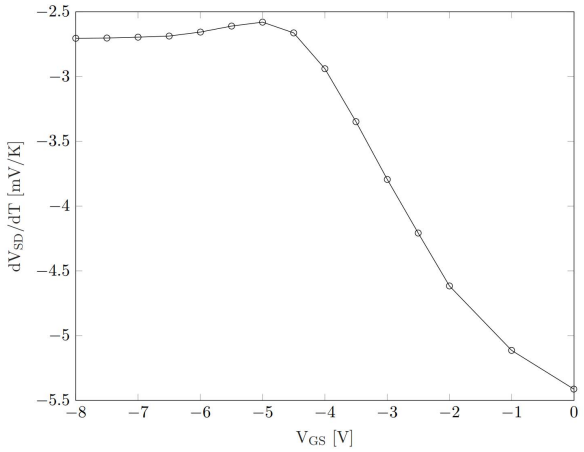

Fig. 1: Slope of $V_{SD}(T)$ plotted as a function of V_{GS}.

Experimental Set-Up

Threshold Voltage Measurement

The threshold voltage was measured using the constant current method [9]. A constant current of 300 μA was utilized, in accordance with [10].

Power Cycling Test Bench

A dedicated power cycling test bench was built for power cycling discrete packages. The schematic diagram for the test set-up is shown in Fig. 2. The load current I_{load} was supplied by a PS 91000-30 power source. For the design of the auxiliary switches S_1 and S_2, four parallel-connected IXFK 120N20P Si MOSFETs were employed, each having a current rating of 120 A. The DUT was the Cree C3M0075120K SiC MOSFET. This is the latest generation SiC MOSFET available and it is expected to have a reliable and representative performance for the state-of-the-art technology.

The operating principle of the test bench is as follows. S_1 and S_2 switch the load current between the bypass branch on the left and the branch containing the DUT. The left branch provides a path for I_{load} to flow when S_2 is off. The sensing current source, I_{sense}, feeds the constant current needed to estimate the junction temperature while the DUT is turned off. The diode D_i prohibits I_{load} from flowing through the sensing current branch. It consists of several series-connected small signal diodes such that their voltage drop is larger than the maximum attainable voltage over the DUT.

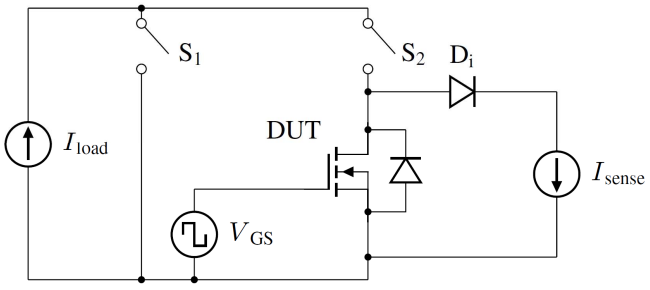

Fig. 2: Schematic diagram of the test bench for performing power cycling of SiC MOSFET.

To use the $V_{SD}(T)$-method, the DUT needs to be switched. In particular, it needs to switch to sufficiently negative values of V_{GS} to ensure that the sensing current passes through the body diode. As mentioned above, the channel was found to be completely closed at $V_{GS} = -6.5$ V at room temperature. The datasheet specifies a limit of $V_{GS} = -4$ V for having a constant gate bias, while $V_{GS} = -8$ V was the minimum rated gate-source voltage when switching the device at a minimum of 1 Hz [11]. Clearly, switching with $V_{GS} = -4$ V would not ensure the channel to be completely closed, so a lower V_{GS} would need to be used. On the other hand, in order to obtain the desired temperature swing, switching faster than 1 Hz would not be feasible either. However, the authors believe that the datasheet limit of switching of $V_{GS} = -8$ V at 1 Hz minimum is included to minimize drift of the threshold voltage. It was, therefore, chosen to add a margin of 1.5 V and use $V_{GS} = -8$ V in order to ensure that the channel was completely closed. The margin would ensure that the channel stays closed despite threshold voltage drift or change due to temperature increase.

Five power cycling tests were completed. All tests were performed under the operating conditions summarized in Table I. In this table, ΔT_{vj} is the temperature swing of the virtual junction temperature, $T_{vj,min}$ is the minimum virtual junction temperature, t_{on} is the on-time of the DUT, and t_{off} is the corresponding off-time.

Table I: Power Cycling Test Parameters

ΔT_{vj}	$T_{vj,min}$	t_{on}	t_{off}	I_{load}
80 °C	44 °C	500 ms	1600 ms	28.4 A

Results

Development of on-state voltage

A typical development of $V_{DS,warm}$ is shown in Fig. 3. $V_{DS,warm}$ is normalized with respect to the initial value at cycle 0. The blue graph corresponds to the actual measurements, while the red line is a zero-phase digitally filtered measurement, which has been added in order to identify the trend more easily.

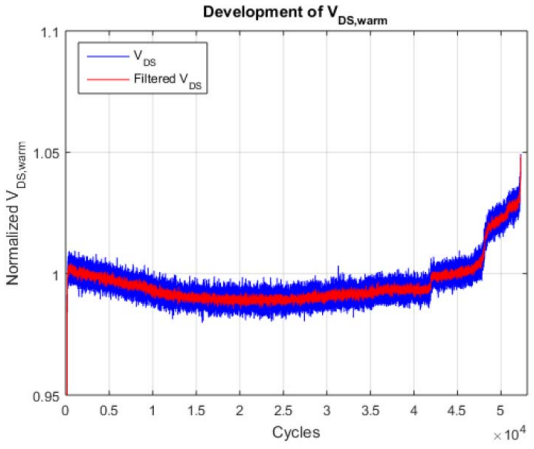

Fig. 3: Development of normalized $V_{DS,warm}$

All devices are assumed to have failed because of bond-wire lift off, due to the observed increase of $V_{DS,warm}$ by 5 %. Moreover, all DUTs have experienced similar characteristic steps in the parameter shortly before failure, which is observed at around 42000 and 48000 cycles, as shown in Fig. 3. On the other hand, R_{th} did not degrade at all, indicating that the interconnecting substrate materials did not experience significant degradation. The initial reduction in $V_{DS,warm}$ that is visible in Fig. 3, was experienced by all DUTs. Even though the magnitude of the reduction was fairly small, and in particular in the order of 1-2% of the initial $V_{DS,warm}$ value, the reduction was clearly visible. The reduction of the

on-state voltage caused a corresponding reduction in the dissipated power of the DUT, which ought to be considered in the general power cycling test of SiC MOSFETs.

The initial reduction of $V_{DS,warm}$ was unexpected and was assumed to be caused due to a negative shift of the threshold voltage. In order to evaluate this hypothesis a new power cycling test was performed with a virgin device. For this device the power cycling test was running until the reduction of $V_{DS,warm}$ was visible. Then, a positive bias was applied to the gate for a prolonged period of time to induce a positive threshold voltage shift. Finally, the power cycling test was started again with the same DUT. If $V_{DS,warm}$ had significantly increased, it would, thus, indicate that the power cycling test was affected by the threshold voltage instability.

Fig. 4 illustrates how $V_{DS,warm}$ developed during the modified test. The test ran for 19190 cycles before it was stopped. Up until then, a similar reduction in $V_{DS,warm}$ was observed as for the other devices. The DUT was biased at $V_{GS} = 15$ V for 4 hours, before the test was resumed. This only gave a slight increase in $V_{DS,warm}$. It was, therefore, decided to stop the test, and repeat the bias, however this time for 42 hours.

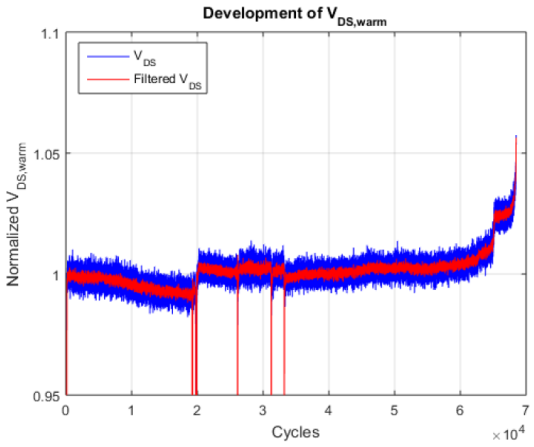

Fig. 4: Power cycling test that was stopped after 19 000 cycles to test dependency of threshold voltage drift

Upon resuming the power cycling test, $V_{DS,warm}$ jumped to values larger than the initial value, thus indicating that the drift of the threshold voltage was affecting the on-state voltage.

Fig. 4 also displays three dips in $V_{DS,warm}$ after 20000 cycles, which occurred due to erroneous test interruptions. These are not relevant for the test. Finally, a step in $V_{DS,warm}$ is observed shortly before it was tripped by an increase of 5% at the cycle 68481.

Characterization Test

The gate-source threshold voltage, $V_{GS(th)}$, was characterized before and after each power cycling test. The results from this characterization test is summarized in Table II for five different test objects. A reduction between 10% and 34% of $V_{GS(th)}$ from the initial values was evident for all devices. The threshold voltage was thus clearly decreasing as a result of the power cycling test.

Table II: $V_{GS(th)}$ Before and After Power Cycling of 5 Different Test Objects

$V_{GS(th)}$ Before	2.384 V	2.068 V	1.984 V	1.632 V	1.951 V
$V_{GS(th)}$ After	1.570 V	1.691 V	1.791 V	1.473 V	1.615 V

Discussion

The initial reduction of $V_{GS(th)}$ indicates that the device conductivity is affected by the power cycling test. Devices from different batches were tested, showing the same response. It is therefore believed that this initial reduction is related to the device structure design itself and not due to faulty manufacturing. The characterization test has shown that $V_{GS(th)}$ was substantially reduced for all DUTs. This observation, combined with the bias test, supports the hypothesis that the initial reduction in $V_{DS,warm}$ is caused by the drift of $V_{GS(th)}$.

The initial reduction in $V_{DS,warm}$ causes a new operating point for the power cycling test. The lowered voltage drop leads to reduced power dissipation in the DUT, thus reducing $T_{j,max}$. This is unfortunate, as it complicates the reproducibility of the test, as well as determining the actual ΔT. In addition to this, the DUT may achieve a longer lifetime due to the initial $V_{DS,warm}$ reduction. This increase in lifetime is due to both lower ΔT and hence lower device stress, as well as the increased margin to the failure criteria of a 5% increase of $V_{DS,warm}$. However, when a device fails as a result of an increase in $V_{DS,warm}$, it has typically experienced characteristic step-wise increases in the parameter toward the end of the test. These correspond to bond-wire lift-off [12]. This process speeds up once an increasing share of the bond-wires are lifted off, as each of the remaining bond-wires need to carry a larger portion of the load current. Hence, if an initial reduction of $V_{DS,warm}$ occurs, the number of cycles to failure is not necessarily substantially increased. However, it should still be taken into account, as the sum of increased lifetime could skew the comparison of results between different power semiconductor devices.

Based on these results, this paper proposes a refinement of the power cycling procedure when dealing with SiC MOSFETs intended to mitigate the drift of $V_{GS(th)}$. Since the duration of the bias plays a key role regarding the drift magnitude [7], one step toward reducing the drift $V_{GS(th)}$ during power cycling tests could be to switch such that the DUT experiences equally long positive and negative bias during one test cycle. This method can be described using the following expression:

$$\int_0^{T_p} \text{sign}(V_{GS}) = 0 \tag{2}$$

Devices undergoing power cycling tests often experience longer off-times than on-times in order for the devices to cool down. Furthermore, for SiC MOSFETs, the negative gate voltage must be very low to use the $V_{SD}(T)$-method. Consequently, a negative shift of $V_{GS(th)}$ is likely, as exemplified in this experiment. Thus, to fulfill equation (2), it is suggested to switch the device on during the off-time. This is of course only a feasible option as long as there is another auxiliary switch that can prevent the load current from flowing in the branch containing the DUT. An example of a possible switching sequence for the circuit in Fig. 2 is shown in Fig. 5. This figure shows the switching sequence of the two auxiliary switches and the DUT. The turn-on of the DUT between the time points 0 and t_1, including the needed dead-time, is also shown. In the conventional power cycling method, the DUT would be off between the time instants t_1 and T_p. The additional on-pulse from t_2 to t_3 is thus added to the conventional approach. By including this time interval and adjusting its pulse length, expression (2) can be fulfilled, thus mitigating the negative drift of $V_{GS(th)}$. The same principle can be used when several devices are being tested simultaneously, yet this increases the complexity of the switching.

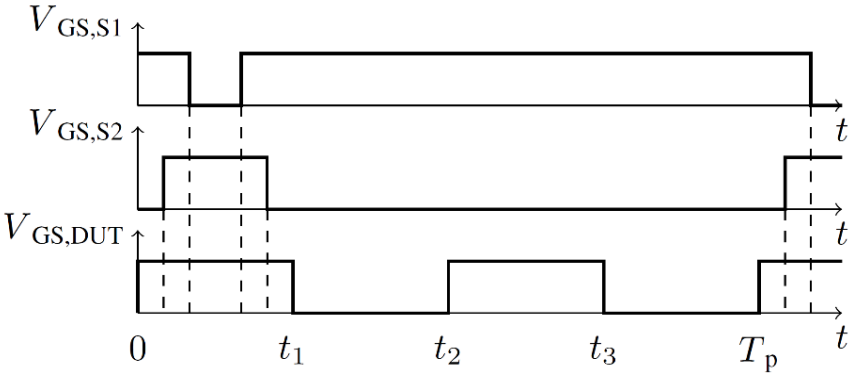

Fig. 5: Possible switching sequence pattern for reducing the threshold voltage drift in power cycling test of SiC MOSFETs.

Although the mentioned switching sequence may lead to reduced instability of $V_{GS(th)}$, the standards for performing power cycling of SiC MOSFETs ought to be reviewed in order to ensure consistent failure criteria between tested devices. One option could be to set the limit of an increase of $V_{DS,warm}$ to 5% from the lowest level that the parameter reaches. In Fig. 3 this limit would thus be roughly 0.985, and hence the end of life failure criteria would be 1.03425. The values for ΔT_{vj} and $T_{vj,min}$ ought then to be the corresponding values for when $V_{DS,warm}$ is at its lowest level. Either way, this is an issue that should be dealt with in order to ensure a consistent methodology for performing power cycling of SiC MOSFETs.

An important note from this particular experiment is that the DUT violated the datasheet specifications for V_{GS}, as previously explained. It is, therefore, possible that the observed drift would be smaller if nominal values were used instead, which would have reduced the observed effect on the power cycling. However, the results indicate that if drift of the threshold voltage occurs, the power cycling results are affected. Hence, a way of handling the threshold voltage instability in power cycling ought to be discussed in any case, and the choice of gate bias do not falsify the results.

Conclusion

This paper has reviewed the methodology for power cycling tests of SiC MOSFETs. The results of power cycling indicate that not only did the devices experience a drift of the threshold voltage, but also, this drift was large enough to cause an initial change in the operating point of the power cycling test. The latter complicates performing the test at a given stress level, as well as comparing the results to power cycling of other power semiconductors. The drift of the threshold voltage is a result of the negative voltage bias during device turn-off. The bias is necessary to accurately estimate the junction temperature. Hence, ways of refining the methodology for performing power cycling of SiC MOSFETs have been proposed and presented.

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