Driver stage implementation with improved turn-on and turn-off delay for wide band gap devices

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Acknowledgements

The authors acknowledge the funds received through the Norwegian Research Council grant 243711 that enabled this work.

Keywords

≪Switching losses≫, ≪Converter circuit≫, ≪Silicon Carbide (SiC)≫, ≪Gallium Nitride (GaN)≫, ≪Wide bandgap devices≫

Abstract

This paper presents a driver topology intended for WBG devices with the goal of improving the switching performance. In particular, the initial delay time of the switching transient was targeted. In high power and high frequency bridge converters, the dead time causes output voltage waveform distortion and increases losses. Shorter delay time leads to shorter dead time requirement. Simulations show that the delay time can be minimised by correctly implementing the suggested driver stage. For the experimental validation, an improvement of 6-8 ns was demonstrated while keeping the same $\mathrm{d}i/\mathrm{d}t$ and $\mathrm{d}v/\mathrm{d}t$ as a conventional gate driver. The improvement increases with increasing gate resistance.

Introduction

As silicon devices are approaching their theoretical limits, the development and implementation of wide band gap devices (WBG) are accelerating. The use of WBG allows for power electronic converters with lower losses and higher power density with lowered system cost. The key enabling factor for this improvement is the reduced switching losses of WBG devices. As WBG devices are unipolar and have smaller parasitic capacitances, the switching speed can be considerably faster compared to silicon devices of similar rating. However, faster switching speed inherently increases the EMI signature [1].

The goal of the gate driver is to ensure fast switching speeds while at the same time avoiding exceeding the safe operating area of the component. Furthermore, the driver control affects the EMI generation of the converter. At the same time, the gate driver can be affected by EM noise and needs to be designed with immunity to such disturbances. Focus on minimising stray inductance in both the power loop and gate loop is critical to achieving fast switching and avoiding switching oscillations. Advanced gate driving techniques are required in order to fully utilise the potential of WBG devices [2]. An overview of driver stages for SiC devices is given in [3]. Most of these drivers are of the conventional gate driver type. There exists many suggestions for more advanced drivers, in particular for WBG devices. In [4], a three step turn-on and turn off is demonstrated for a 1200 V SiC MOSFET. Controlled boosting the gate current during transient is also shown in [5]. Integration of advanced driving techniques into the driver IC has been demonstrated [6, 7]. Two other publications showcase setups with a higher level of complexity by

Table I: Gate charge needed for different transitions of the switching waveform. The values are from the datasheet of a commercial SiC MOSFET (C3M0075120K), 25 °C, 20 A load and 800 V dc-link voltage.

Delay time	Current transition	Voltage transition	Enhancement
8 nC	5 nC	22 nC	17 nC

incorporating a large number of programmable stages [8, 2]. This allows very flexible gate waveforms. In [8], the gate voltage waveform is adapted according to the current feedback. However, only switching waveforms of a Si IGBT are shown. [2] has a similar implementation with higher resolution to control the switching transient of a 650V GaN eHEMT.

In this paper, three different driver stage topologies are compared, of which one is a suggestion from this paper. Comparison is done by simulations in LTSpice using component models of the WBG devices. In contrary to many publications, more focus is set on the delay time of switching transient; however, $\mathrm{d}i/\mathrm{d}t$ and $\mathrm{d}v/\mathrm{d}t$ are also compared. The targeted application for this paper is high power and high frequency bridge converters employing SiC MOSFETs. In half or full bridge converters, there is a dead time requirement to avoid short circuit. During the dead time, the current runs in the freewheeling path. The main drawback during freewheeling is voltage waveform distortion and increased losses. These effects become increasingly important for converters operating at higher switching frequency.

Theory on switching transients

Turn-on transient

The four steps within a switching transient of a unipolar device are listed below, in the order of appearance during a turn-on event. The sequence is reversed for a turn-off event.

1. Turn-on delay time, $\left[\, \mathrm{V}_{neg}, \mathrm{V}_{th} \,\right]$
2. Rising drain current, $\left[\, \mathrm{V}_{th}, \mathrm{V}_{plateau} \,\right]$
3. Falling drain-source voltage, $\approx \mathrm{V}_{plateau}$
4. Changing on-resistance enhancement, $\left[\, \mathrm{V}_{plateau}, \mathrm{V}_{pos} \,\right]$

The associated voltage level between gate and source are also listed. V_{neg} and V_{pos} is the negative and positive driving voltage, V_{th} is the threshold voltage and $\mathrm{V}_{plateau}$ is the Miller plateau voltage level. Instead of voltages, the needed charge could be presented instead. An example of the charge required for each step is shown for a commercial SiC MOSFET in Table I. Hence, to pass a switching transition, sufficient charge is fed to the gate terminal. The capacitance seen from the gate driver and the relation to the drain current and voltages for each step is discussed below.

Time delay

The turn-on delay is defined as the time from the gate starts to be charged until the drain current starts to rise, which is when the gate voltage reaches the threshold voltage, V_{th}.

$$t_{delay,on} = ln\left(1 - \frac{V_{th} - V_{neg}}{V_{pos} - V_{neg}}\right) \cdot \tau \tag{1}$$

where τ equals $R \cdot C$. R is approximately equal to $R_{g,ext} + R_{g,int} + R_{driver,int}$, the external gate resistor, the internal gate resistor, and the internal driver buffer stage resistance, respectively. C is approximately equal to the gate input capacitance. (1) shows that the delay time increases with increasing threshold voltage, resistance or capacitance. Since the expression in (1) contains the nominal driving voltage levels, the turn-on delay becomes larger when using negative driving.

Similarly, the turn off delay is defined as the time from the gate starts to be discharged and until the drain-source voltage starts to increase.

$$t_{delay,off} = ln\left(\frac{V_{pos} - V_{plateau}}{V_{pos} - V_{neg}}\right) \cdot \tau \tag{2}$$

The turn-off delay will decrease with increasing plateau voltage, but increase with resistance and capacitance.

Current rise and voltage fall

The second and third step of the switching transient concerns the drain current and the drain source voltage. The drain current is changing as the gate voltage is rising and the device channel is opening. During this transition, the gate current is again mainly charging the gate source capacitance. The gate current control the change in drain current during this transition [9, Chapter 22].

$$\frac{\mathrm{d}i_D}{\mathrm{d}t} = g_m \cdot \frac{\mathrm{d}V_{GS}}{\mathrm{d}t} = g_m \cdot \frac{i_g}{C_{GS}}, \qquad V_{GS} \in \left[V_{th}, V_{plateau}\right] \tag{3}$$

Similarly, the gate current controls the $\mathrm{d}v_{DS}/\mathrm{d}t$ while the gate voltage is at the plateau voltage. During this transition, the gate current is mainly charging the gate-drain capacitor [9, Chapter 22].

$$\frac{\mathrm{d}v_{DS}}{\mathrm{d}t} = \frac{i_G}{C_{GD}} \tag{4}$$

In summary, the gate current controls both $\mathrm{d}i/\mathrm{d}t$ and $\mathrm{d}v/\mathrm{d}t$.

Channel enhancement

For the last transition, the channel resistance is further decreased as the gate voltage rises to the nominal drive voltage. During this step, the gate current is again mainly charging the gate source capacitance. However, the timing requirements and the impact on the switching losses are less influential.

Turn-off transient

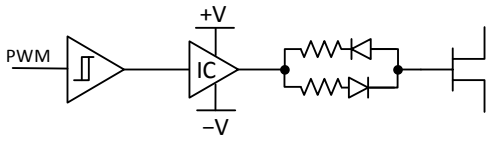
In the turn-off event, the order of events is reversed. The enhancement period will act as a turn-off delay time. The needed charge for the delay time for turn-off is typically higher than for the turn-on, as can be seen by comparing the difference in charges listed in Table I.

Comparison of gate driver topologies

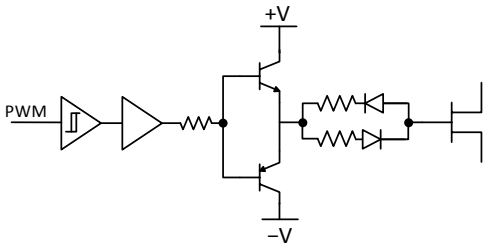
Three different implementations of the gate driver stage is seen in Fig. 1. The conventional type (Fig. 1a) consists of a single buffer IC that contains the pre-drivers and amplifying stage. This driver often allows for different turn-on and turn-off resistances. The totem pole driver with discrete amplifying transistors is shown in Fig. 1b. Here, the signal buffer acts as a pre-driver. Again, separate turn-on and turn-off resistors can be set. The topology seen in Fig. 1c is suggested in this paper. It consists of a buffer IC with complementary outputs and an amplifying stage using MOSFETs. The voltage level of the amplifying stage could be different from the nominal driving voltage. As will be shown, the suggested topology introduces new degrees of freedom that can be used to improve the switching performance. Details of the design of the suggested topology is given in next section.

Goals of the gate driver can be stated in the following prioritised order

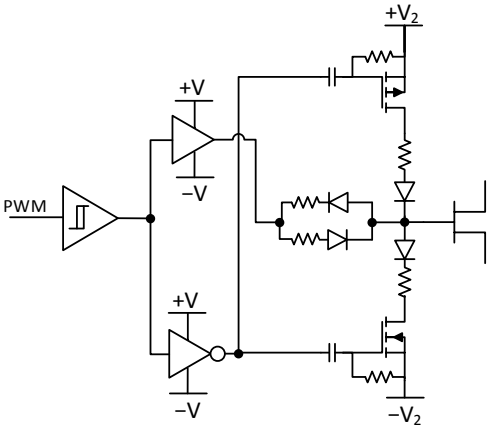
1. The driver supplies the nominal driving voltages, V_{pos} and v_{neg}, in steady state.
2. The driver supplies sufficient gate current to achieve the target switching times.
3. The driver minimises unwanted effects like oscillations and over-shoot.



(a) Conventional gate driver.



(b) Totem pole gate driver.



(c) Suggested gate driver topology.

Fig. 1: Circuit diagrams for the compared driver stage implementation.

Table II: Timing values of commercially available gate driver ICs as stated in their datasheet. Rise and fall times are given for a 1.5 nF load. Delay times are given for room temperature.

Component	Current rating	Rise time	Fall time	On delay	Off delay
IX4428	± 1.5 A	13 ns	11 ns	22 ns	28 ns
IXD_609	± 9.0 A	6 ns	5 ns	35 ns	39 ns

Nominal driving voltages

The nominal driving voltage is ensured by selecting the driving voltages, V_{pos} and V_{neg}, to the nominal voltage levels. This is given by the component manufacturer and, hence, does not constitute a degree of freedom in the design.

Supplied gate current

Since the voltage level of the driver is often given, the gate current is shaped by changing the gate resistor value. With a simple gate driver, the gate driver design has only a single degree of freedom, the turn-on or the turn-off gate resistors, that affects both current and voltage waveforms. By looking at the charge requirements for these two steps in Table I, the current transition is observed to need less charge than the voltage transition.

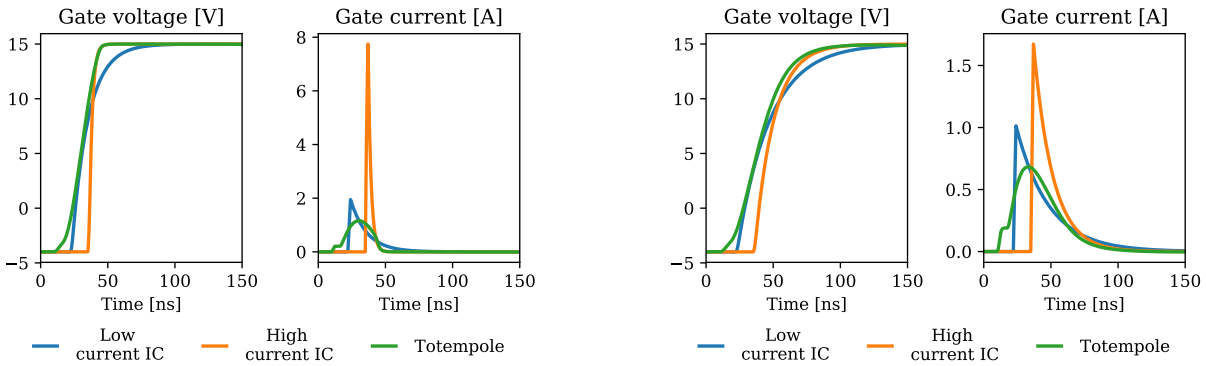
The internal resistance of the buffer will also influence gate current level, especially for high power devices. When choosing a driver IC, there are several choices to make that will force the designer to compromise on performance. A low current driver IC will be able to supply the right driving voltage, but the current output is limited. To switch faster, the current rating of the driver will need to be increased. At the same time, higher current rating will usually lead to higher delay time for the IC. This is due to the increased internal capacitance of the ICs with higher current rating. An example of two similar ICs with different current rating and their timing values are shown in Table II. The IC with high current rating also has an increased signal delay.

Another way of increasing the current rating of a driver stage is to make a discrete amplifier stage, typically a totem pole circuit as shown in Fig. 1b. The total signal delay becomes the sum of the delay of the buffer stage and the totem pole switches. Such a totem pole topology is implemented for a SiC MOSFET in [10], resulting in approximately 40 ns signal delay added to the buffer stage.

A simple comparison of the three solutions, low current IC, high current IC and totem pole stage is done. Fig. 2a shows the performance when charging a capacitive load of 5 nF with a series resistor of 1 Ω. The low current IC starts charging earlier than the high current IC, but due to the high current capability,

the latter reaches the final voltage earlier. The totem pole starts to charge the load even earlier, but has internal time delays before the full current capability is reached.

However, when driving SiC MOSFETs, the internal gate resistance of these devices have a big influence on the gate waveform. In general, most commercially available SiC MOSFETs have high internal gate resistance. For the test object used in this paper (C3M0075120K), the input resistance is 10.5 Ω. Fig. 2b shows the same comparison between the three gate drivers with a series resistor of 10 Ω. It is observed that the low internal resistance of the high current IC is less influential due to the high internal gate resistance of the SiC MOSFET.



(a) Comparison of buffer stages when using 1 Ω series resistance.

(b) Comparison of buffer stages when using 10 Ω series resistance.

Fig. 2: Comparison of driver stage implementations with an RC load.

Minimising unwanted effects

Other unwanted effects related to the switching transient include switching delay, noise generation, voltage over-shoot, and oscillations. In some applications, requirements for maximum $\mathrm{d}i/\mathrm{d}t$ and $\mathrm{d}v/\mathrm{d}t$ might be set. An example would be motor drives, where the insulation limits the maximum $\mathrm{d}v/\mathrm{d}t$.

A simple and common way of addressing these effects is to increase the gate resistance, resulting in a slower switching transition. As seen from (1) and (2), this would lead to increased signal delay.

Suggested driver topology

The suggested driver stage implementation shown in Fig. 1c, consists of two main parts, the conventional drive circuit and the boost drive circuit. Although the complexity is increased with this topology, the structure gives several degrees of freedom that can allow for better switching transients.

The buffer IC is a fairly low current IC consisting of both a non-inverting and an inverting buffer. The non-inverting buffer is connected to the gate with the conventional turn-on and turn-off resistance values. This branch is intended to supply a relatively low gate current and ensure the steady state gate voltage, V_{neg} and V_{pos}. In addition, there is a boosting stage that is controlled by the non-inverting buffer. The boosting stages for turn-on and turn-off are identical, and hence only one side will be explained.

The boosting MOSFET is turned on quickly via the series capacitor. The gate and capacitor charge is then discharged through a parallel resistor, turning the boosting MOSFET off again before the next switching event. The results is that the boosting MOSFET delivers a current pulse in the time period defined by the mentioned components. The resistance in series with the drain of the boosting MOSFET defines the amplitude of the current pulse from the boosting stage. The pulse waveform can now be designed in two ways depending on the secondary voltages, V_{neg2} and V_{pos2}.

$\mathbf{V_2}$ = V

If the secondary voltage is equal to the driver voltage, the boosting stage behaves like an amplifying stage, similar to the totem pole stage of the gate driver in Fig. 1b. The advantage of the suggested structure is a lowered delay time compared to using a high current IC.

Table III: Simulation results of different driver topologies when driving a commercial SiC MOSFET (C3M0075120K) with a 15 A load current and 600 V dc-link voltage. Peak derivative values are given.

		Buffer IC		Totem pole	Suggested	
		Low current	High current		Fast charging	Delay time improvement
Delay	Turn-on	49 ns	52 ns	46 ns	41 ns	48 ns
	Turn off	54 ns	60 ns	55 ns	50 ns	53 ns
Losses	Turn-on	9.1 µJ	5.8 µJ	6.7 µJ	5.9 µJ	9.1 µJ
	Turn off	3.7 µJ	2.8 µJ	3.4 µJ	2.8 µJ	3.6 µJ
dv/dt	Turn on	−104 V/ns	−166 V/ns	−147 V/ns	−164 V/ns	−104 V/ns
	Turn-off	114 V/ns	135 V/ns	121 V/ns	135 V/ns	116 V/ns
di/dt	Turn on	6 A/ns	8 A/ns	7 A/ns	8 A/ns	6 A/ns
	Turn off	−12 A/ns	−15 A/ns	−13 A/ns	−15 A/ns	−12 A/ns

$|\mathbf{V_2}| < |\mathbf{V}|$

If the secondary voltage is lower than the driving voltage, the diode in series with the boosting MOSFET blocks the boosting circuit when the gate voltage is equal to the secondary voltage level. Hence, the current pulse length can be designed to be voltage dependent instead of depending on the boosting MOSFET timing. This is an advantage when driving very fast WBG devices. The boost stage delivers a large gate current spike that finishes as the gate voltage reaches the Miller plateau or the threshold voltage. This function is used to decrease the delay time of the switching transient without affecting the di/dt or dv/dt.

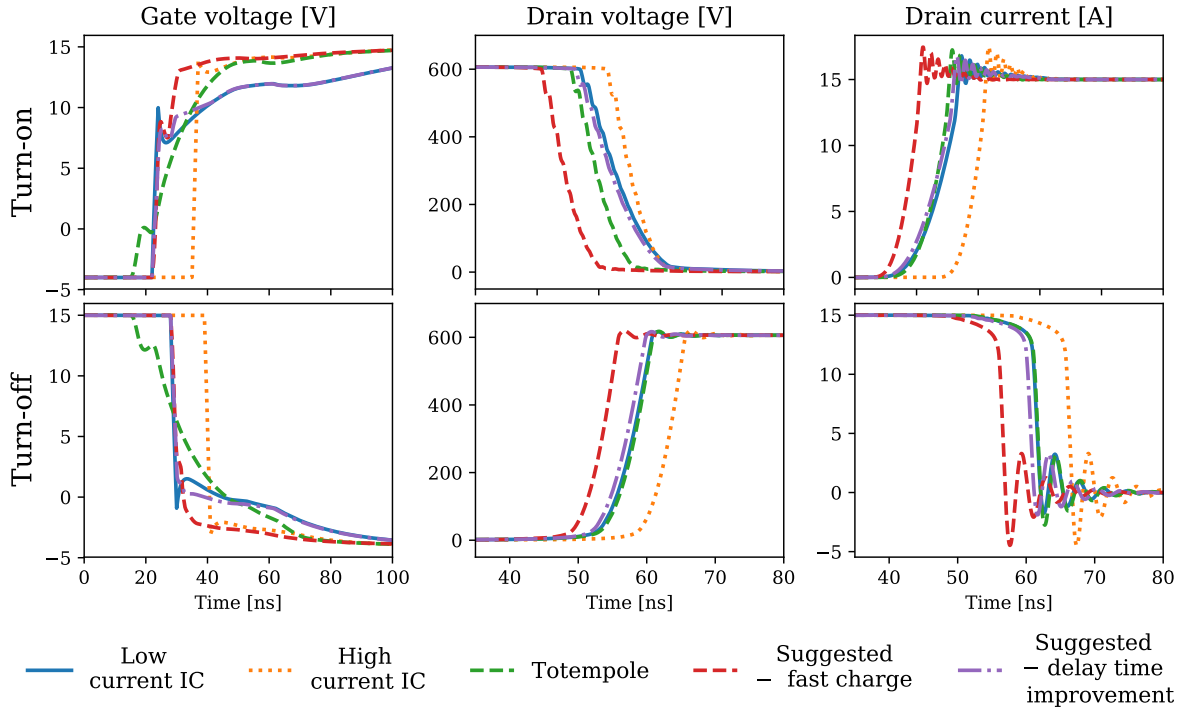


Fig. 3: Simulation waveforms of different driver topologies when driving a commercial SiC MOSFET (C3M0075120K) with a 15 A load current and 600 V dc-link voltage.

Simulation results and experimental validation.

The driver topologies are compared using simulation in LTSpice. The drivers supply gate current to a SiC MOSFET (C3M0075120K), for which the SPICE model supplied by the manufacturer is used. The SiC MOSFET is switching a 15 A load with a dc-link voltage of 600 V. Two use cases are defined for the suggested driver topology where the goal is to minimise the delay time. First, the suggested topology is configured to charge the gate as fast as possible and give the same switching characteristics as a high current IC. In the second case, the suggested topology is configured to give the same switching characteristics as the low current IC and only give delay time improvement. Simulation are carried out with a 1 Ω gate resistor, which can be considered the worst case for the suggested driver topology in terms of performance gains.

The switching waveforms for turn-on and turn-off are seen in Fig. 3. The switching characteristics are given in Table III. As expected, the low current IC gives lower delay time than the high current IC, while the latter gives higher $\mathrm{d}i/\mathrm{d}t$ or $\mathrm{d}v/\mathrm{d}t$ resulting in lowered switching losses. The totem pole driver is somewhere in between the two. The suggested topology can deliver the same current as the high current IC with lowered delay time, approximately 10 ns. In the second case, the suggested topology decreases the delay time for the low current IC case while keeping the same $\mathrm{d}i/\mathrm{d}t$ or $\mathrm{d}v/\mathrm{d}t$. However, in this case the improvement is in the range of 1 ns.

Although the improvement by using the boost stage is not pronounced in the simulation case, this is application dependent. The effect of the suggested driver will be larger when used for devices without internal series resistors or for applications where current and voltage switching speed must be limited. In circuits were the switching transients need to be slowed down, the performance gain of the suggested topology will increase. As such, the presented simulation case can be considered a worst-case scenario.

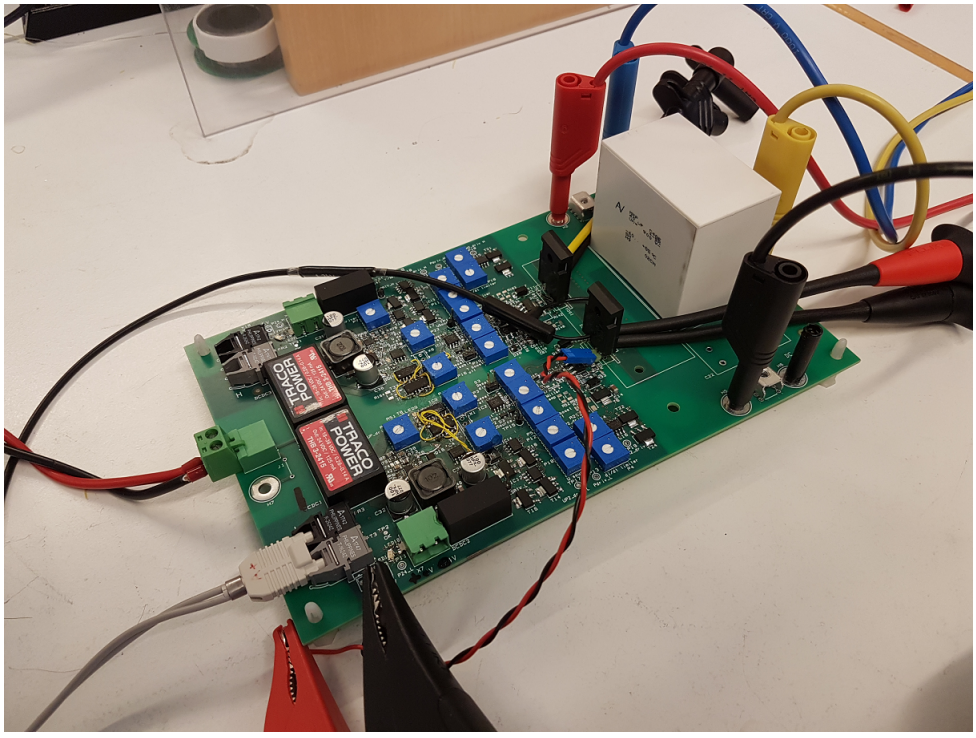
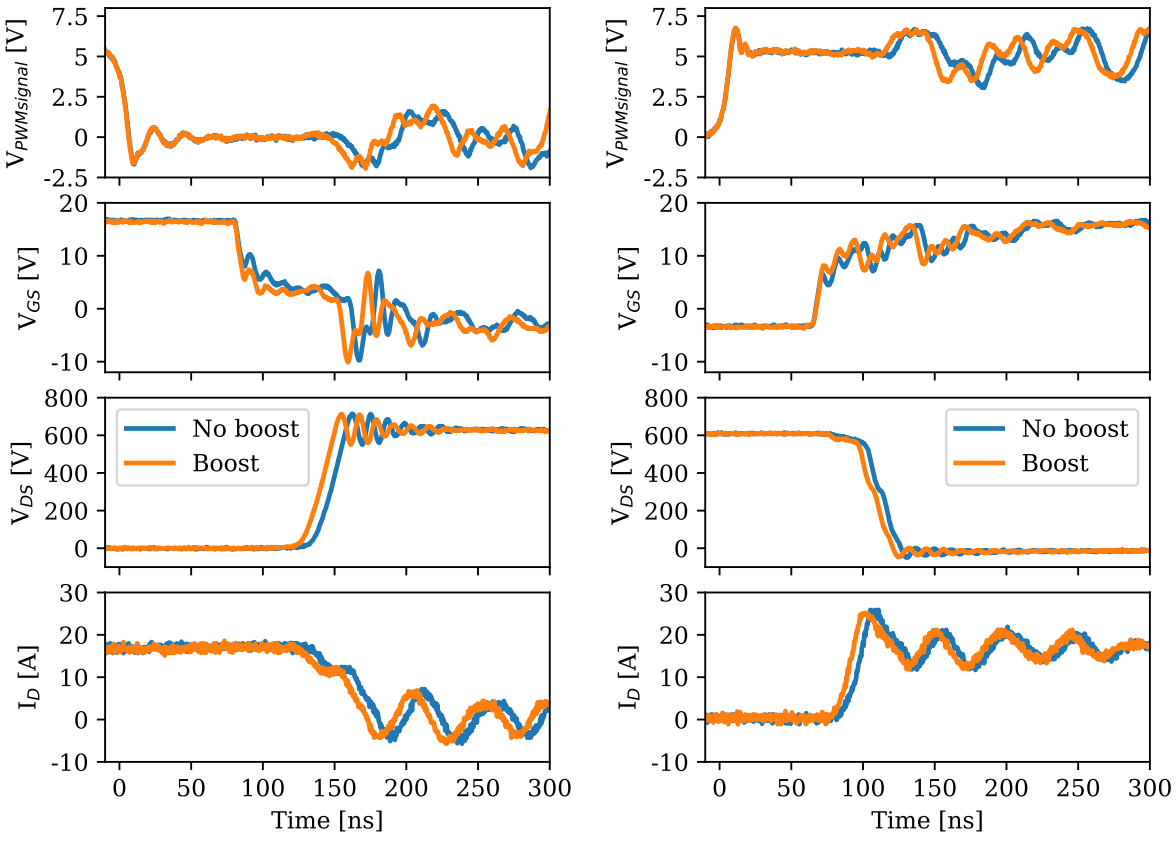


Fig. 4: Photo of the driver board implementation.

A PCB containing the suggested driver structure and half bridge power circuit was developed to give an experimental validation of the concept. The board is seen in Fig. 4. The driver board design allows for simple changes to operation point and is not optimised in terms of layout. Two configurations were tested with an external gate resistor of 18 Ω. In the first configuration, switching is done without any boosting and all the gate current was supplied by the buffer IC. In the second configuration, the driver

boosted the turn-on and turn-off by the boosting circuits. The secondary driving voltages are tuned to decrease the delay time while avoiding to affect the $\mathrm{d}i/\mathrm{d}t$ and $\mathrm{d}v/\mathrm{d}t$. The secondary driver voltages were changed to 10.5 V and 2.5 V from the nominal driving voltages of 15 V and −4 V.

The waveforms for the turn-on and turn-off are seen in Fig. 5. The edge of the PWM signal from the controller is used as a common reference point in time. The main values are shown in Table IV. As can be seen, the driver is able to decrease the delay time while the switching transient is fixed to the same $\mathrm{d}i/\mathrm{d}t$ and $\mathrm{d}v/\mathrm{d}t$, hence validating the concept. In Fig. 6, a comparison between the measured and simulated waveforms are compared. For simplicity, only the turn-off is shown. The simulation model is modified with the experimental values for driving voltages, dc-link voltage, load current and gate resistance. A good coherence is observed for the gate and drain voltages. The simulated drain current has, however, a much steeper change than the measured value. An oscillation is observed in the gate signal at the same time instant. These two effects are likely related to an inductive coupling between the two source connections of the test object that is not correctly modelled in simulation. However, the simulation and experimental waveforms give a good representation of the achievable reduction in delay time for the suggested driver topology.



(a) Turn-off

(b) Turn-on

Fig. 5: Experimental waveforms of the suggested driver with and without boosting.

Table IV: Measurement results comparing the suggested driver with and without boosting.

		No boosting	Boosting
$\mathrm{d}v/\mathrm{d}t$	Turn on	$-34.5\,\mathrm{V/ns}$	$-33.4\,\mathrm{V/ns}$
	Turn-off	$34.4\,\mathrm{V/ns}$	$33.8\,\mathrm{V/ns}$
$\mathrm{d}i/\mathrm{d}t$	Turn on	$1.6\,\mathrm{A/ns}$	$1.6\,\mathrm{A/ns}$
	Turn off	$-1.0\,\mathrm{A/ns}$	$-0.9\,\mathrm{A/ns}$
Delay improvement	Turn-on		$-5.6\,\mathrm{ns}$
	Turn off		$-7.6\,\mathrm{ns}$

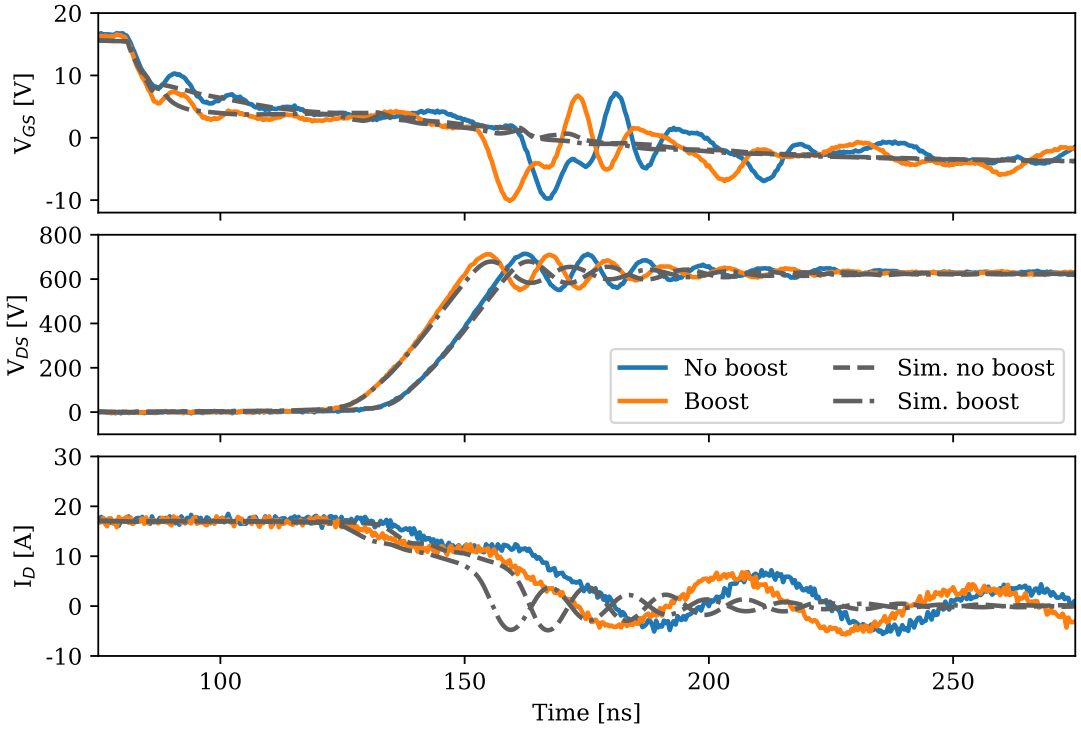


Fig. 6: Comparison of experimental and simulated waveforms for use case of 18 Ω gate resistor with and without boosting.

Conclusion

This paper has presented a driver topology intended for WBG devices and compared it with two conventional driver topologies. The goal of the new driver is to improve the switching performance. In particular, the initial delay time of the switching transient that was targeted. Simulations show that delay time can be minimised by correct implementation of the driver stage. The suggested topology has more degrees of freedom than conventional driver stages and, hence, can be used to achieve high gate current or lowered delay time without affecting the $\mathrm{d}i/\mathrm{d}t$ and $\mathrm{d}v/\mathrm{d}t$. The delay time improvement increases with installed gate resistance. For the experimental validation, an improvement of 6-8 ns was demonstrated.

References

[1] N. Oswald, P. Anthony, N. McNeill, and B. H. Stark. An Experimental Investigation of the Tradeoff between Switching Losses and EMI Generation With Hard-Switched All-Si, Si-SiC, and All-SiC Device Combinations. *IEEE Transactions on Power Electronics*, 29(5):2393–2407, May 2014.

[2] H. C. P. Dymond, J. Wang, D. Liu, J. J. O. Dalton, N. McNeill, D. Pamunuwa, S. J. Hollis, and B. H. Stark. A 6.7-GHz Active Gate Driver for GaN FETs to Combat Overshoot, Ringing, and EMI. *IEEE Transactions on Power Electronics*, 33(1):581–594, January 2018.

[3] D. Peftitsis and J. Rabkowski. Gate and Base Drivers for Silicon Carbide Power Transistors: An Overview. *IEEE Transactions on Power Electronics*, 31(10):7194–7213, October 2016.

[4] A. P. Camacho, V. Sala, H. Ghorbani, and J. L. R. Martinez. A Novel Active Gate Driver for Improving SiC MOSFET Switching Trajectory. *IEEE Transactions on Industrial Electronics*, 64(11):9032–9042, November 2017.

[5] K. Yamaguchi, K. Katsura, T. Yamada, and Y. Sato. Comprehensive evaluation of gate boost driver for SiC-MOSFETs. In *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, pages 1–8, September 2016.

[6] R. Grezaud, F. Ayel, N. Rouger, and J. C. Crebier. A Gate Driver With Integrated Deadtime Controller. *IEEE Transactions on Power Electronics*, 31(12):8409–8421, December 2016.

[7] Rok Vrtovec and Janez Trontelj. Advanced gate control system for power MOSFET switching losses reduction with complete switching sequence control. *Journal of Microelectronics, Electronic Components and Materials*, 46(4):12, 2016.

[8] H. Obara, K. Wada, K. Miyazaki, M. Takamiya, and T. Sakurai. Active gate control in half-bridge inverters using programmable gate driver ICs to improve both surge voltage and switching loss. In *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, pages 1153–1159, March 2017.

[9] N. Mohan, T. M. Undeland, and W. P. Robbins. *Power Elecotronics: Converters, Applications, and Design*. John Wiley & Sons, Inc, third edition edition, 2003.

[10] J. Liu, Y. Wang, Z. Zheng, Z. Peng, and Y. Li. Comparison of two gate drivers for SiC MOSFETs on switching performance and over current protection. In *2017 20th International Conference on Electrical Machines and Systems (ICEMS)*, pages 1–5, August 2017.