An insight into geometry and orientation of capacitors for high-speed power circuits

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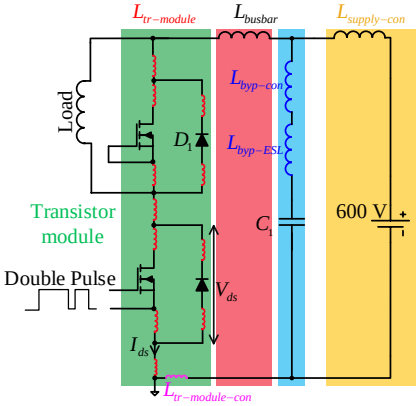
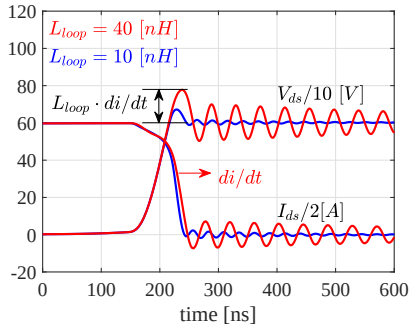
***Abstract*—SiC transistors can switch extremely fast. Often turn-off di/dt is reduced to limit the turn-off over voltages due to the stray inductances in the commutation loops. Thus, the potential low switching losses are not met. One of the benefits of designs with SiC devices is the possibility of low switching losses and therefore high switching frequencies. This opens for the paradigm shift in power electronics. For utilizing the fast switching potential, a low inductive circuit layout of the commutation loop consisting of the transistor, diode, connections and the DC-link capacitor is indispensable. Low inductive transistor case and busbars are analysed by the authors before. Employing low stray inductance DC-link capacitors is a must for realizing the low stray inductance designs. The methods used to connect the DC-link capacitors to the system, such as the busbar, is equally important. The paper analyses the geometry and orientation of the DC clamping capacitor for minimizing the SiC transistor turn-off over voltages. In addition, by reviewing the commercially available low inductance DC-link capacitors with different physical size and terminations, this paper presents the design of a DC-link for a 100 kW full-bridge AC-DC-AC converter. Two approaches; first, measuring the parasitics of the components themselves, such as capacitor and transistor module by impedance analyser; and second, computing the parasitics of the bussing structure and connections via FEA tool; are adopted throughout this work. Based on this, the breakdown of the total switching loop stray inductance contributed by each parts is illustrated, from which the major conclusions are drawn.**

I. Introduction

In a diode-clamped inductive load buck converter, as shown in Fig. 1 a), transistor current basically stays constant until its voltage has reached the supply voltage. Then the current will commutate via the free-wheeling diode (D_1) to a DC protection capacitor (C_1). The parasitic inductances of the commutation loop are: internal in the components themselves; for instance, in the semiconductor devices (denoted by red coils), and in the C_1 ($L_{byp-ESL}$); and in the busbar (L_{busbar}) [1]. Additionally, the method to connect these components to the busbar also shares a considerable portion of stray inductances, and are indicated by $L_{tr-module-con}$ and $L_{byp-con}$. During the turn-on process, these parasitic inductances are charged and during the turn-off process, they are discharged. The transistor turn-off over voltage can be expressed as: $L_{loop} \cdot di/dt$, where di/dt is dictated by the transistor properties and its gate drive. A typical turn-off transient with two different loop inductances (L_{loop}) is shown in Fig. 1 b), which illustrates that higher the L_{loop}, higher is the over voltage, and lower is the current slew rate [2]. It is noteworthy that voltage overshoot is increased although di/dt is reduced, the reason being much higher increase in L_{loop} than the decrease in di/dt. Furthermore, for the same L_{loop}, this over voltage is more amplified for SiC transistor compared to Si transistor because the former switches extremely fast. For example, di/dt per chip area is measured to be 5.1 A/ns/cm^2 in SiC MOSFET and 2.2 A/ns/cm^2 in Si IGBT, i.e., di/dt is higher by a factor of 2.3 in SiC MOSFET compared to Si IGBT [2]. Often, SiC is slowed down to the level of Si to operate it safely with a penalty of higher switching losses. Thus, it is crucial to design a low inductive layout to fully utilize the fast switching potential of SiC transistor.



(a) A diode-clamped inductive load circuit.



(b) Turn-off transient.

Fig. 1. a) Buck converter with various possible stray inductances in the loop, b) turn-off transient illustrating the importance of having lower L_{loop}.

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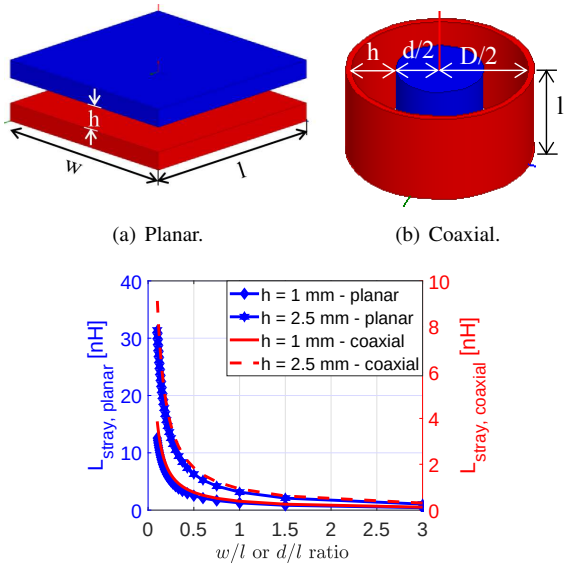
In low power electronics area, there exist several application notes and publications about low inductance capacitors [3], [4]. However, there is limited literature about those in high power electronics area. In [5], internal inductance of DC-link power capacitors are addressed, but the method to connect them are not covered. To begin with, this paper presents the impact of physical dimensions of capacitors on the stray inductances in Section II. Thereafter, Section III reviews the current available low inductance DC-link capacitors with different physical dimensions and terminations, and measures the $L_{byp-ESL}$ associated with them using impedance analyser, E4990. For a fair comparison, the normalization is done with 2 different parameters; first, with respect to the highest capacitance value, and second, with respect to the largest ripple current possessed by the selected capacitors. Then, the 3D FEM models are built for axial and circular terminated capacitors in Section IV and Section V, respectively. Ansys Q3D tool is used for extracting the parasitics of the required bussing structures and plotting the current density distribution. Additionally, by illuminating the two different orienting methods for capacitors, this paper provides guidelines on designing and orienting them such that $L_{byp-ESL}$ and $L_{byp-con}$, as labelled in Fig. 1 a), are minimum, where the main contribution of this paper lies.

Moreover, a 100 kW AC-DC-AC converter is simulated in MATLAB for finding the current stress in the DC-link capacitor in Section VI. Dimensioning of the DC-link capacitance for satisfying the defined voltage ripple is also included in this section. Employing each of the low inductive type of capacitors under study, 5 DC-link busbars are built and simulated in Q3D. Subsequently, the parasitic inductances encompassed by various part, such as $L_{tr-module-con}$, $L_{byp-con}$, and power supply connection ($L_{supply-con}$) are accessed. For providing a comprehensive overview of the proportion of stray inductances incorporated by different parts, inductances internal to the components themselves, for example, capacitor and transistor module are measured by impedance analyser. An example of a complete busbar employing an optimal capacitor solution, in terms of cost and loop inductance factors, is also demonstrated. Looking into the current density distribution plot in the busbar, two different phenomenons can be ascertained: a) the parts that are bypassed, and b) the most stressed parts construing the major current flow. Finally, Section VII presents the most important conclusions.

II. Capacitor Geometry

In this section, the stray inductance of a planar and coaxial structures are studied through basic physics based expressions, as given by Equation 1 and Equation 2 respectively [6], [7] where, μ_r is the relative permeability of the medium and μ_0 is the permeability of the free space ($4\ \pi\ \times\ 10^{-7}$ H/m). For the better clarity, the dimensions used in equations are depicted in Fig. 2 a) and b) where; w is width, l is length for planar structure and d is diameter of the inner conductor, D is inner diameter of the outer conductor for coaxial structure. Fig. 2 c) shows the plot of stray inductance (L_{stray}) versus w/l (or d/l) ratio for these structures. Apparently, there is the highest reduction in L_{stray} for w/l (or d/l) ratio upto 1, which suggests that this ratio should be ≥ 1. In addition, closer the opposite plates, lower is the inductance. Nonetheless, for the same separation between the opposite plates, the coaxial structure gives lower L_{stray} than the planar structure.



(a) Planar. (b) Coaxial.

(c) L_{stray} plot with varying w/l or d/l ratio.

Fig. 2. a) and b) example of planar and coaxial structures, and c) plot of L_{stray} illustrating the highest reduction in it for w/l (or d/l) ratio upto 1. Clearly, smaller the h, lower is the L_{stray}. For the same h, L_{stray} is lower for the coaxial structure compared to the planar structure.

$$L_{stray,\ planar} = \mu_0 \cdot \mu_r \cdot \frac{l \cdot h}{w} \tag{1}$$

$$L_{stray,\ coaxial} = \frac{\mu_0 \cdot \mu_r}{2\pi} \cdot ln\left(\frac{D}{d}\right) \cdot l \tag{2}$$

III. Selection of Low Inductance DC-Link Capacitors

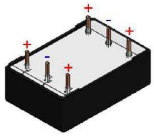
In this section, a brief description of the selected low inductance DC-link capacitors is presented. Fig. 3 depicts the photograph of these capacitors, namely, DCL capacitor, MKR capacitor, Ring capacitor, Coaxial capacitor and Ceralink capacitor. The first four are film type and the last one is a Ceramic type with different dielectric material than in a classical ceramic capacitor. In reference [5], it is mentioned that the capacitance increases with increasing voltage in the dielectric used for ceralink type, while the opposite is true in the class 2 ceramic materials used for multilayer ceramic capacitors. Mostly, the mechanical interface of capacitors are decided by their voltage and current ratings. For a fair comparison, the capacitors with equal voltage ratings (900 V) are chosen. The electrical specification of the selected capacitors is shown in Table I. The capacitance and ripple current rating (I_{ripple}) are from datasheet, where the latter is taken for 85 °C [8], [9], [10], [11]. The effective series inductance ($L_{byp-ESL}$) is measured using an impedance analyser, E4990.

(a) DCL.

(b) MKR.

(c) Ring.

(d) Coaxial.



(e) Ceralink.

Fig. 3. Photograph of five different commercially available low inductance capacitors, where a) is DCL capacitor (45 mm separation between the opposite screws), b) is MKR capacitor (24 mm separation between the opposite pins), c) is Ring capacitor, d) is Coaxial capacitor, and e) is Ceralink capacitor (7.62 mm separation between the opposite pins).

TABLE I
ELECTRICAL SPECIFICATION OF LOW INDUCTANCE DC-LINK CAPACITORS.

Capacitor type & parameters	Capacitance (μF)	I_{ripple} (A) @85°C	$L_{byp-ESL}$ (nH)	Cost (e)
DCL	150	50	14.85	18
MKR	95	45	4.85	25
Ring	215	175	10.2	170
Coaxial	20	20	6.7	10
Ceralink	5	25	3.5	52

TABLE II
PARAMETERS NORMALIZED TO CAPACITANCE OF RING CAPACITOR.

Capacitor type & parameters	No. of capacitors	I_{ripple} (A)	$L_{byp-ESL}$ (nH)	Total cost (e)
DCL	2	100	7.42	36
MKR	3	135	1.61	75
Ring	1	175	10.2	170
Coaxial	11	220	0.61	110
Ceralink	43	1075	0.08	2236

TABLE III
PARAMETERS NORMALIZED TO RIPPLE CURRENT OF RING CAPACITOR.

Capacitor type & parameters	No. of capacitors	Capacitance (μF)	$L_{byp-ESL}$ (nH)	Total cost (e)
DCL	4	600	3.71	72
MKR	4	380	1.21	100
Ring	1	215	10.20	170
Coaxial	9	180	0.74	90
Ceralink	7	35	0.50	364

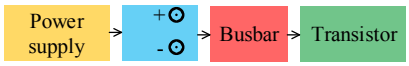
Considering $L_{byp-ESL}$ of a single capacitor, Ceralink has the lowest value followed by MKR, Coaxial, Ring, and DCL. Prominently, Ceralink has the largest ripple current per capacitance amongst all. It should be underlined that the cost is evaluated based on distributors 1000 quantity. In order to guarantee a fairer comparison, the capacitance of each capacitors is normalized with respect to that of the Ring capacitor, and the results are enlisted in Table II. Note that the number of capacitors are rounded up to the next whole number. The remaining parameters in Table II, i.e., I_{ripple}, $L_{byp-ESL}$, and total cost are calculated based on the rounded value of capacitor. As can be observed, a new order of capacitors ascending with regard to $L_{byp-ESL}$ is Ceralink followed by Coaxial, MKR, DCL and Ring. As Ceralink has the lowest capacitance amongst all, 43 of them have to be connected in parallel to meet the same capacitance requirement as that given by the Ring. Consequently, this solution becomes the most expensive of all those considered for the time being (this scenario might change in future as Ceralink is an emerging technology and the price is likely to drop).

Further, in the quest for a more balanced comparison, the ripple current of each capacitors is normalized with respect to that of the Ring capacitor, and the outcome is catalogued in Table III. It should be asserted again that the number of capacitors are rounded up and the remaining parameters are calculated accordingly. When normalized with ripple current, the number of parallel capacitors and the total cost comprised by each types of capacitor are closer compared to those when normalized with capacitance. Interestingly, the new order of capacitors as per the $L_{byp-ESL}$ remained unaltered in either of the normalization approaches.

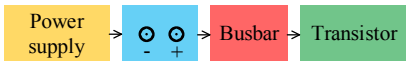
IV. AXIAL TERMINATED CAPACITORS

Section III focussed on the selection of low inductance DC-link capacitors and the measurement of the inductance imposed by their geometries, while this section primarily focusses on the simulation of the inductance associated with the bussing connections made with each capacitor types. In particular, the orientation of capacitors while mounting them on the busbar is investigated to study their impact on the $L_{byp-con}$. Fig. 4 shows 2 directions, defined as, 0° and 90° for mounting capacitors. In 0° case, the opposite terminals are located at equal distance to the transistor while they are not in 90° case.

Additionally, by specifying 3D geometry, material properties (such as copper for busbar and Mylar for dielectric), and the desired output, Q3D extractor generates the necessary impedance matrices which can be represented by the lumped element circuit model. Details on the basics about modelling of busbar with this tool is described in the previous work [12], and the same approach is employed in this work as well.



(a) 0° oriented capacitor terminals.



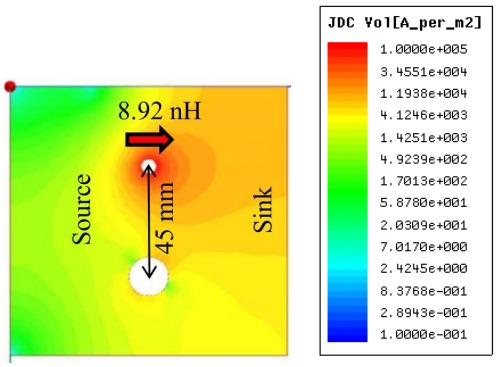
(b) 90° oriented capacitor terminals.

Fig. 4. Definition of orientation of capacitor. In 0° case, opposite terminals are located at equal distance to the transistor while they are not in 90° case .

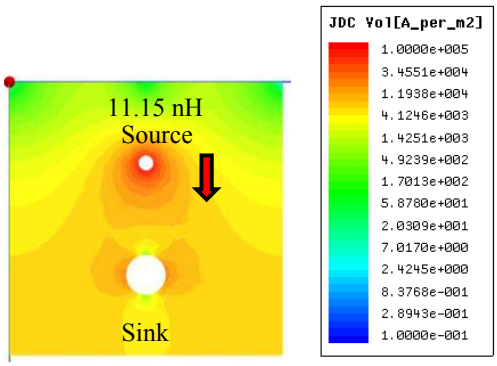
TABLE IV
SUMMARY OF INDUCTANCES FOR AXIAL TERMINATED CAPACITORS.

Capacitor type	L_{11} (nH)	L_{22} (nH)	L_{12}, L_{21} (nH)	$L_{byp-con}$ (nH)	Reduction (%)
DCL 45 mm, 0°	13.576	13.585	9.117	8.925	19.991
90°	6.187	20.743	7.887	11.155	
DCL 25 mm, 0°	12.967	12.968	10.635	4.665	13.818
90°	9.047	16.903	10.268	5.413	
MKR 24 mm, 0°	11.529	11.123	8.979	4.692	32.798
90°	8.352	17.403	9.386	6.982	
Ceralink 7.62 mm, 0°	11.469	10.437	10.375	1.156	3.906
90°	12.298	10.977	11.036	1.203	

Note: Safety clearance of 5 mm and dielectric thickness of 0.4 mm are considered throughout the simulation.

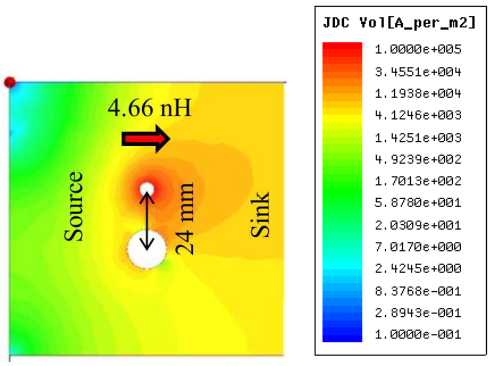


(a) 45 mm seperation with 0°.

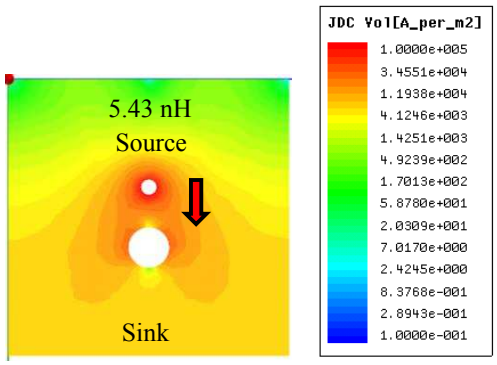


(b) 45 mm seperation with 90°.

Fig. 5. Simulated busbar for DCL capacitor with 45 mm separation between the opposite screws. Orientation in a) has lower loop inductance than in b).



(a) 24 mm seperation with 0°.

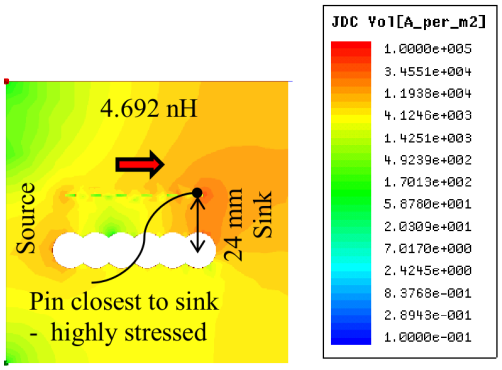


(b) 24 mm seperation with 90°.

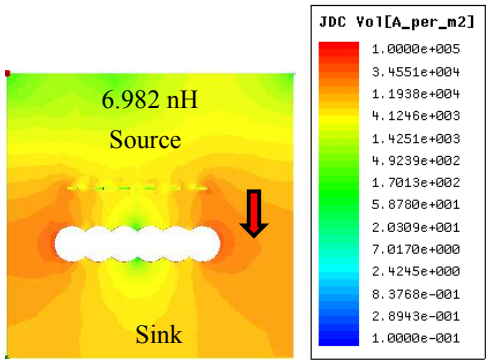
Fig. 6. Simulated busbar for DCL capacitor with 24 mm separation between the opposite screws. Orientation in a) has lower loop inductance than in b).

A. DCL capacitor

Fig. 5 depicts the simulated busbar for DCL capacitor with 45 mm separation between the opposite screws, where a) is with 0° orientation and b) is with 90° orientation along with the corresponding $L_{byp-con}$ labelled in the respective current density plots. The current flows from the capacitor (source) to the load (sink) and is indicated by an arrow head. Self-inductances (L_{11} and L_{22}) of the opposite plates are almost equal in the former case, while there is a large difference between those in the latter case, and the results are summarised in Table IV. It is worth emphasizing that 0° case showed about 20 % lower $L_{byp-con}$ compared to 90° case. This is because of the fact that there is a stronger flux linkage between the opposite plates in the former orientation compared to the latter. DCL capacitors are also available with 24 mm separation distance and the current density plot is shown in Fig. 6 a) with 0° orientation and b) with 90° orientation. Simulation showed that smaller the distance between the opposite screw holes, lower is the $L_{byp-con}$. Capacitors with 24 mm separation showed about 47 % (0°) and 51 % (90°) lower $L_{byp-con}$ compared to those with 45 mm separation. Closer the opposite screws, better is the magnetic field cancellation, which is the reason behind this result. Thus, mounting of capacitors is critical especially when the distance between the opposite screws are larger, as inferred from the analysis in this subsection.

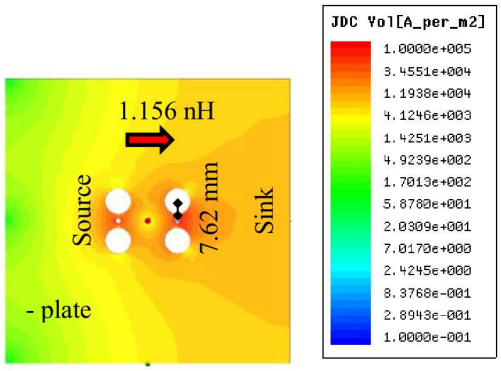


(a) 0° orientation gives equal self-inductances.

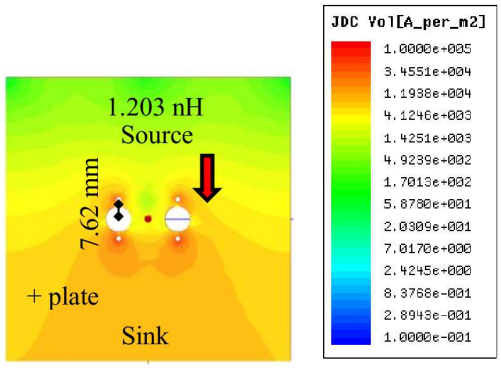


(b) 90° orientation gives unequal self-inductances.

Fig. 7. Simulated busbar for MKR capacitor with 24 mm separation between the opposite pins. Fig. a) has lower loop inductance compared to Fig. b). Q3D simulation shows that the pin closest to the sink is highly stressed in the capacitor orientated in 0°, while in the one with 90° orientation, the pins which are towards the extreme left and right sides of the sink are the most stressed ones.



(a) 0° orientation gives equal self-inductances.



(b) 90° orientation gives unequal self-inductances.

Fig. 8. Simulated busbar for Ceralink capacitor with 7.62 mm separation between the opposite pins. Orientation in a) has lower loop inductance than in b). As Ceralink capacitor with 900 V rating is made by series connection of 2 capacitors, the negative plate is shown in a) while the positive in b).

B. MKR capacitor

Fig. 7 a) and b) shows the current density distribution in the busbar with MKR capacitor which are placed at 0° and 90°, respectively. In the busbar with 0° orientation of capacitor, the pin which is closest to the sink is highly stressed, while in the one with 90° orientation, the pins which are towards the extreme left and right sides of the sink are the most stressed ones. In fact, in the former orientation, the capacitor which is closest to the load provides the lowest impedance path for the current or it is utilized the most, compared to the ones placed further apart. In the latter orientation, on the other hand, the clearances for the opposite pins block the direct current path, and thereby a detour is taken. It should be noted that the loop inductance is lower by about 33 % in the case with 0° compared to the one located at 90°, the detail results are listed in summary Table IV.

C. Ceralink capacitor

Fig. 8 a) and b) displays the current density distribution for Ceralink capacitor which are placed at 0° and 90°, respectively. SP900 series [10] of Ceralink capacitors are made by series connection of 2 capacitors, the negative plate is shown in a) and the positive plate in b). End results regarding the orientation in Ceralink showed similar pattern as in DCL and MKR capacitors, that is, 0° mounting resulted in about 4 % lower $L_{byp-con}$ compared to that with 90°, the $L_{byp-con}$ of which are marked in the respective plots. These capacitors showed the lowest $L_{byp-con}$, as the opposite pins are closest of all (only 7.62 mm).

V. Circular Terminated Capacitors

Section IV mainly concentrated on simulating loop inductance associated with the bussing structure for axial terminated capacitors, while this section focusses on that for circular terminated capacitors. The impact of their placement in $L_{byp-con}$ is simulated for these capacitors as well, and it is found that the orientation in either directions gives equal outcome.

A. Ring capacitor

In the chosen Ring capacitor [9], 8 terminal pairs are evenly spaced around the circumference. It is large in volume and weight. The ratio of diameter (225 mm) to height (50 mm) is 4.5 ($\gg$1), resulting in low $L_{byp-con}$ for the given capacitance and ripple current rating. Fig. 9 illustrates the current density distribution and the associated $L_{byp-con}$ for it. Because of the larger separation distance between the opposite screws and larger clearances needed for screw holes, the ring type has larger loop inductance, as shown in Table. V.

B. Coaxial capacitor

In the Coaxial capacitor [11], 3 pin pairs are evenly spaced around the circumference. It is a PCB mounted type and has a relatively smaller physical size, termination pins and capacitance compared to the Ring capacitor. Manufacturer has chosen the diameter and height to be almost equal in order to realize low $L_{byp-ESL}$. The simulated busbar is illustrated in Fig. 10, and the details about inductance matrices is recorded in Table. V.

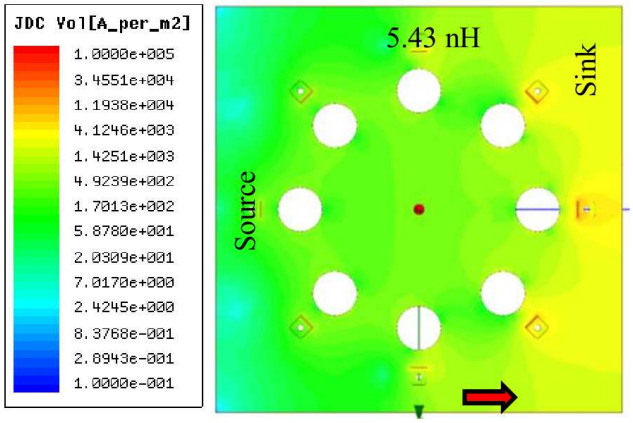


Fig. 9. Simulated busbar for Ring capacitor (SBE) resulted in equal $L_{byp-con}$ in either of the orientations. This capacitor is large in size and weight. The bussing structure and the clearance holes are also larger compared to the rest of the capacitors under considerations.

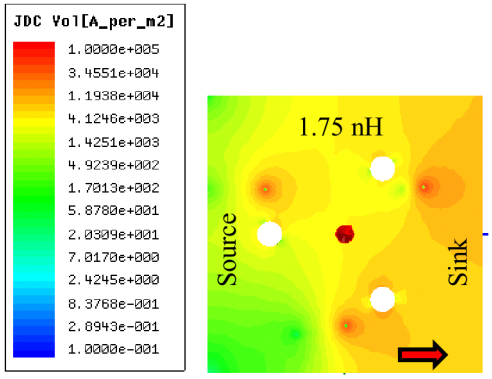


Fig. 10. Simulated busbar for Coaxial capacitor (FTCAP). Orientation in either directions give equal outcome. $L_{byp-con}$ is smaller compare to that of Ring capacitor because the opposite pin pairs are closer and smaller.

TABLE V
SUMMARY OF INDUCTANCES FOR CIRCULAR TERMINATED CAPACITORS.

Capacitor type	L_{11} (nH)	L_{22} (nH)	L_{12}, L_{21} (nH)	$L_{byp-con}$ (nH)
Ring	24.770	12.202	15.933	5.430
Coaxial	9.994	9.094	8.668	1.752

Note: Safety clearance of 5 mm and dielectric thickness of 0.4 mm are considered throughout the simulation.

VI. Design of DC-link for AC-DC-AC converter

In this section, there are three main objectives. First objective is about sizing of the DC-link capacitor in an AC-DC-AC converter, which is covered in Subsection VI-A. Second objective concerns in comparing the stray inductance constituted by various components and their connections, which is presented in Subsection VI-B. Third goal is exemplifying a DC-link busbar design employing Coaxial capacitor, and is included in Subsection VI-C.

A. Sizing the DC-link capacitor

A series resonant converter topology for an induction heating application is shown in Fig. 11. The DC-link capacitor (C_1) is stressed from two sides: rectifier and inverter. First, in order to find the ripple current share from the 6-pulse bridge rectifier side, a simulation is performed in MATLAB for a 100 kW converter with a DC-link voltage of 640 V. At 360 Hz (6 $\times$ 60 Hz, 60 Hz being the AC line frequency), the ripple current is simulated to be 7.2 A. Second, to find the ripple current comprise from the inverter part, the full-bridge series resonant inverter is switched at 300 kHz for an output current (I_{out}) of 180 A, which resulted in the ripple current of 80.5 A in the C_1. Adding the contribution from the rectifier part and the inverter part, the aggregate ripple current (I_c) capacity of capacitor becomes 87.7 A. Simultaneously, the DC-link capacitor should be sized such that the defined ripple voltage requirement ($<$10 %) in a converter is ensured. Simulation was performed with the capacitance of 180 μF which gave the ripple voltage of 45 V; 7 % of DC-link voltage. When used 35 μF of Ceralink capacitors, as obtained from the normalization in Section III, the ripple voltage will cross the defined ripple limit, the solution would be to connect additional 29 number of Ceralink capacitors. However, this solution would be the most expensive of all. On the other hand, all the remaining capacitors give the ripple voltage well below the defined margin.

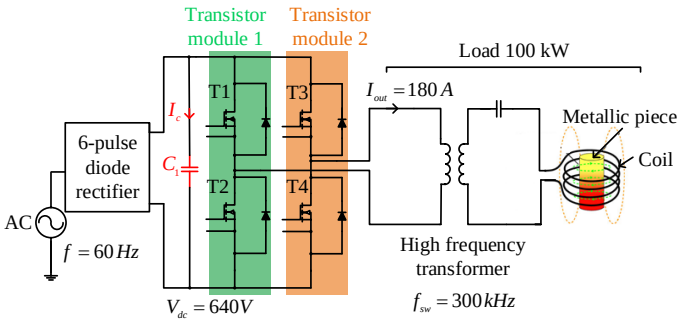


Fig. 11. Schematic diagram of AC-DC-AC converter for an induction heating application. Capacitor (C_1) is stressed partly from the front end 6-pulse diode rectifier and mostly from the 300 kHz switched series resonant inverter. For instance, for the given 100 kW converter, the front end current stress by 360 Hz component is simulated to be 7.2 A and the current stress from the inverter part is 80.5 A, so the total capacitor current (I_c) is 87.7 A. With capacitance of 180 μF, the ripple voltage resulted to be 7 % of DC-link voltage.

B. Comparison of stray inductance shared by various parts

In this subsection, FEM simulation is used to extract the stray inductance impressed by the connection of power supply, capacitor, and transistor module, however, the ones associated internal to the capacitor and the transistor module are measured by impedance analyser. 5 different 3D models of the DC-links are built employing each types of the selected capacitors. The number of capacitors are according to the normalization with respect to the ripple current capacity, as shown in Table III. It should be highlighted that $L_{byp-con}$ for the axial terminated capacitors are simulated with 0° orientation, as explained in Section IV. Further, for DCL capacitor, the case with 24 mm separation is chosen.

Table VI enlists the total switching loop stray inductance (L_{tot}) which is the composite of the stray inductance contributed by all the components and connections in the switching loop. For instance, adding the inductance comprised by the capacitor part ($L_{byp-ESL}$ + $L_{byp-con}$ = 0.74 + 0.55 = 1.29 nH) and the transistor module part ($L_{tr-module}$ + $L_{tr-module-con}$ = 15 + 5.96 = 20.9 nH), L_{tot} is reckoned to be 22.25 nH for the busbar with Coaxial capacitor. Note that FEM simulation was performed with and without the supply part, but the simulated results remained unchanged. This is obvious because the supply part of the busbar is bypassed. Since $L_{supply-con}$ is bypassed, it is not accounted while computing L_{tot}.

As can be observed from the table, the solution with Ring capacitor resulted to be the most inductive followed by DCL, MKR, Coaxial, and Ceralink. In the last column labelled as "Improvement" the percentage reduction in the total switching loop stray inductance compared to that when used Ring capacitor is shown. Besides, the share of module part and the capacitor part can be visualized by the bar chart in Fig. 12. Employing DCL and MKR capacitors, the total loop inductance is improved by about 31 % and 37 %, correspondingly, taking L_{tot} imposed by Ring capacitor as a reference. Similarly, using the solution with Coaxial and Ceralink capacitors, the loop inductance is improved the most; approximately 43 % and 44 %, respectively, compared to the loop inductance impressed by the Ring capacitor solution.

Likewise, from the bar chart, it is also clear that the majority of switching loop stray inductance is shared by the transistor module part. Apparently, the internal inductance of the transistor module is as much as that composed by the Ring capacitor in total. In fact, SiC MOSFETs are packaged in the same standard plastic package as used for Si IGBT modules, which is the reason for such a high inductance in the transistor module.

C. Exemplifying a DC-link busbar with coaxial capacitor

An example of the simulated DC-link busbar employing 9 coaxial capacitors in parallel is demonstrated in Fig. 13. This combination possesses the total ripple current capacity of 175 A. With the capacitance of 180 μF, the ripple voltage in the DC-link is 45 V as per the MATLAB simulation, which is 7 % of the total DC-link voltage (640 V). It is worth mentioning that for maintaining the ripple voltage within 10 %, the capacitance was chosen to be 180 μF which in turn ended up with double the ripple current capacity than that of the simulated value. Furthermore, it is noticeable from Fig. 13 that current density is higher towards the transistor module side (right side), indicated by the red colour, compared to the supply side, indicated by the blue colour. Observing this

TABLE VI
SUMMARY OF SWITCHING LOOP INDUCTANCE.

Capacitor type & parameters	$L_{byp-ESL}$ (nH)	$L_{byp-con}$ (nH)	L_{tot} (nH)	Improvement (%)
DCL	3.71	1.61	26.67	31.28
MKR	1.21	1.94	24.52	36.82
Ring	10.20	5.43	38.81	0
Coaxial	0.74	0.55	22.25	42.66
Ceralink	0.50	0.26	21.89	43.59

Note: L_{tot} = ($L_{byp-ESL}$ + $L_{byp-con}$ + $L_{tr-module}$ + $L_{tr-module-con}$) // $L_{supply-con}$.

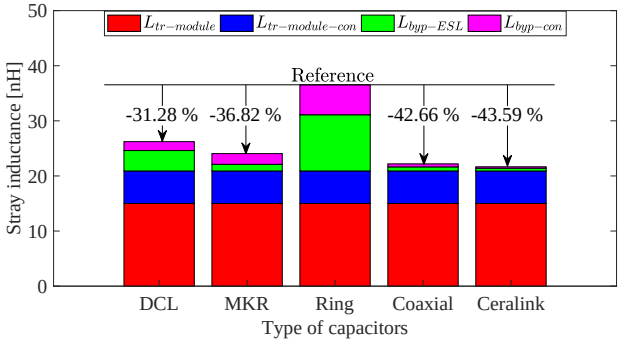


Fig. 12. Breakdown of switching loop stray inductance in a 100 kW AC-DC-AC converter. The legends in bar chart are: internal parasitic inductance of the transistor module ($L_{tr-module}$), stray inductance from the transistor module connection ($L_{tr-module-con}$), inductance associated internally in the capacitor ($L_{byp-ESL}$), and stray inductance from the bypass capacitor connection ($L_{byp-con}$). The stray inductance shared by $L_{tr-module}$ and $L_{tr-module-con}$ are the most critical ones and have to be further reduced.

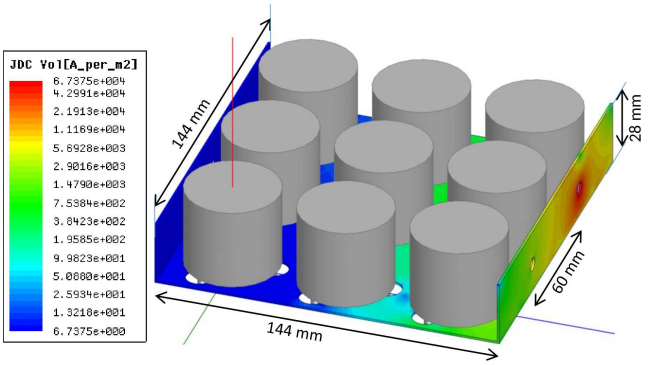


Fig. 13. Simulated DC-link busbar with 9 coaxial capacitors resulting in the total bussing stray inductance of 6.5 nH. Note that this DC-link has the total capacitance of 180 μF and ripple current capacity of 175 A. Clearly noticeable is the higher current density towards the transistor module connection side (right side), compared to the supply side (left side) indicating that the components away from the transistor module are bypassed, that is, capacitor closer to the switching device provides a low inductance path for switching transients.

pattern in the current density plot, it can be inferred that the components away from the transistor module are bypassed. To rephrase it, the capacitor closer to the switching device provides a low inductance path for switching transients.

VII. Conclusion

To conclude, for acquiring low inductive layout following guidelines are recommended. First, both the busbar and capacitor geometry should have width to length (w/l) or diameter to height (d/l) ratio ≥ 1 and the separation between the opposite plates as small as possible. For example, DCL capacitor with smaller distance between the screws showed lower connection inductance than that with larger distance. Second, the axial terminated capacitors should be oriented in the direction where the opposite plates have equal self-inductances, and thereby better cancellation of magnetic field. On the other hand, the circular terminated capacitors, such as ring and coaxial can be located in either directions.

Moreover, the designs of DC-link busbar for a 100 kW AC-DC-AC converter reveal that the busbar with Ring capacitor is the most inductive solution, followed by DCL capacitor, MKR capacitor, Coaxial capacitor, and Ceralink capacitor. Taking the total switching loop inductance imposed by the Ring capacitor solution as a reference, the improvement obtained by employing DCL, MKR, Coaxial, and Ceralink are: 31 %, 37 %, 43 % and 44 %, correspondingly. However, regarding the prices, the busbar with Ceralink capacitor is the most expensive, supervened by Ring, MKR, Ceralink, and DCL capacitors. Among the capacitors under considerations in this work, an optimal solution concerning two dimensions, namely, cost and loop inductances, is given by the Coaxial types.

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