Characterization of body diodes in the-state-of-the-art SiC FETs -Are they good enough as freewheeling diodes?

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Keywords

≪Silicon Carbide (SiC)≫, ≪MOSFET≫, ≪JFET≫, ≪Schottky diode ≫, ≪Reverse recovery≫, ≪Hard switching≫.

Abstract

This paper investigates the switching phenomenon of body diodes in the state-of-the-art discrete SiC FETs. A comparative performance evaluation of the body diodes in planar and double-trench SiC MOSFETs, and trench cascode SiC JFET is performed using standard double pulse test methodology. In addition, the switching characterization of planar discrete anti-parallel freewheeling SiC Schottky diodes is included. A series of key electrical parameters such as peak reverse recovery current, recovery time, dv/dt, and di/dt during first and second half of reverse recovery are experimentally measured in order to get an insight on the quality of these diodes.

1 Introduction

In power electronics applications, such as motor drives, synchronous rectifiers, phase shift PWM dc-dc power converters, an anti-parallel or a freewheeling diode is required across a semiconductor switching device to handle the current in the reverse direction. A MOSFET structure exhibits an intrinsic body diode which has a structure of PiN diode. In a SiC MOSFET, this PiN diode has a very high forward voltage drop (V_F = 4.8 V at V_{gs} = -5 V, I_F = 20 A, 25 °C [1]) because SiC has a wider bandgap energy (≈ 3 eV) compared to Si (≈ 1.2 eV). However, V_F in a SiC Schottky diode is much lower (1.8 V, I_F = 20 A, 25 °C) [2] as it is determined by the metal semiconductor barrier height instead of a p^+n junction barrier in the PiN diode [3]. There are mainly two types of Schottky diodes: the Schottky barrier diode (SBD), and the junction barrier Schottky diode (JBS). In the SBD, as the temperature increases, the Schottky barrier height lowers leading to the increase in the reverse leakage current [3]; thus the blocking voltage of commercially available SiC SBD is limited to 600 V. Therefore, JBS (hybrid diode) combines SBD-like on-state and switching characteristics and PiN-like blocking characteristics and is used as antiparallel diode in IGBT or MOSFET. This diode is also often referred as a merged PiN Schottky (MPS) diode. In order to further improve the static performance of Schottky diode (reduce forward voltage drop), the SiC trench SBD is under development [4], [5], [6].

There are different perspectives presented in literatures in different time frames. For example, in [7] the use of the body diode is not recommended; instead, an external Schottky diode is suggested because of its high V_F. In the other words, the PiN-structure of the parasitic diode in the SiC MOSFET was not optimized for lower losses. Then the datasheet of manufacturer would contain very limited information about the body diode and that limited information would be presented at low di/dt (for instance 0.1 A/ns) [8]. There has been continuous improvement in the performance of the body diode and the datasheet are also updated accordingly. In the synchronous rectifier operation, the MOSFET channel is turned on in the reverse conducting mode so that the major part of current flows through this channel and only a part through the body diode. In the other words, the MOSFET shunts the conduction phase current away from the body diode reducing the conduction losses caused by the high forward voltage drop. Results with such operation as for Si MOSFET was also presented for SiC MOSFET in [9]. Thereafter, Wolfspeed have updated their datasheet in second generation MOSFETs with higher di/dt of 2.4 A/ns [1] along with the third-quadrant characteristics as an addendum compared to its first generation MOSFET [8]. Looking further in various publications, eliminating the antiparallel diode and using only the improved body diode (that is turning on the channel) for increasing current capacity in SiC MOSFET module is presented in [10]. Reference [11] compared body diodes of Si and SiC MOSFETs focusing on the forward and gate characteristics. In [12], [13] the switching energy loss of SiC JBS is compared with that of the body diode in SiC MOSFET. Further, the switching and robustness of body diodes are studied in [14].

Since the quality of the body diode in the SiC MOSFET is continuously improved as per datasheet, it is crucial to examine the switching quality of the body diode of a new generation MOSFET by laboratory measurement. Understanding the behaviour of the body diode and Schottky diode helps to decide whether there is the need for an external diode or not. Besides, according to the author's knowledge, the reverse recovery of the body diodes in the overall FET family is not evaluated together to date. Particularly, dv/dt, and di/dt during first and second half of reverse recovery are discussed very little in the literatures. Therefore, in this paper the switching performances of the body diodes in a new generation SiC FETs: MOSFET (planar and trench types), JFET (cascode trench), are compared with the SiC Schottky diodes (planar). The dv/dt and di/dt associated with each devices are discussed thoroughly. All the devices under test (DUTs) are presented in Section 2. Following this is the methodology in Section 3. Section 4 demonstrates the hardware setup and measurement issues. Experimental results with a series of key electrical parameters such as peak reverse recovery current (I_{rrm}), recovery time (t_{rr}), dv/dt, and di/dt during first and second-half of the reverse recovery are presented and discussed in Section 5. Finally, Section 6 presents the most important conclusions.

2 Device under test

Table I shows a comparison of the most significant parameters, such as maximum breakdown voltage (V_{DSmax}), forward voltage drop (V_F or V_{SD}), forward current (I_F or I_{sd}), chip area, and device technology of the body diodes in planar [1], [15], [16] and trench [17] SiC MOSFETs, and planar [2] [6] SiC Schottky diodes used in the measurements. The body diode in the trench SiC JFET with cascode configuration [18], [19] is also listed in Table I in order to give a complete overview of diodes in FET technology. Fig. 1 shows the structures of SiC MOSFET with planar versus trench technology. Basically, trench structures improve the static performances of the devices [4].

3 Methodology

The double pulse test (DPT) methodology is used for accessing the dynamic performance of a body diode in a SiC MOSFET. Two pulses are sent to a control device (transistor T1) in a clamped inductive load circuit, as shown in Fig. 2 a), while the gate and source of the DUT are either shorted or supplied with - 5 V in order to ensure that the DUT is turned-off all the time, and hence, only the body diode is active in the circuit. Fig. 2 b) displays the typical test waveforms, where the first turn-off (at the end of the first pulse) and the second turn-on (at the beginning of the second pulse) are the key point of interests because the switching transients of the DUT can be captured under the similar voltage and current conditions. Channel 1 is the gate voltage of the transistor T1 (V_{gs-H}), Channel 2 is the anode

Table I: Key parameters of the investigated DUTs.

DUT	V_{DSmax} (kV)	V_F or V_{SD} (V) @ 25/150 °C	I_F or I_{sd} (A) @ 25°C	Die size (mm^2)	Technology
C2M0080120D	1.2	4.8/4.3 @ I_{sd} = 20 A	36 @ V_{gs} = -5 V	10.41	Planar MOSFET
C3M0065090D	0.9	5.8/5.4 @ I_{sd} = 20 A	23.5 @ V_{gs} = -4 V	3.53	Planar MOSFET
SCT3040KL	1.2	3.2/3.5 @ I_{sd} = 20 A	55 @ V_{gs} = 0 V	13.64	Trench MOSFET
UJC1206K	1.2	1.45/2.1 @ I_{sd} = 20 A	38 @ V_{gs} = 0 V	14.67	Trench JFET
C4D30120D	1.2	1.8/2.3 @ I_{sd} = 20 A	44	14.58	Planar JBS diode
SCS310AP	0.65	1.7/2.05 @ I_{sd} = 20 A	10	3.06	Planar JBS diode

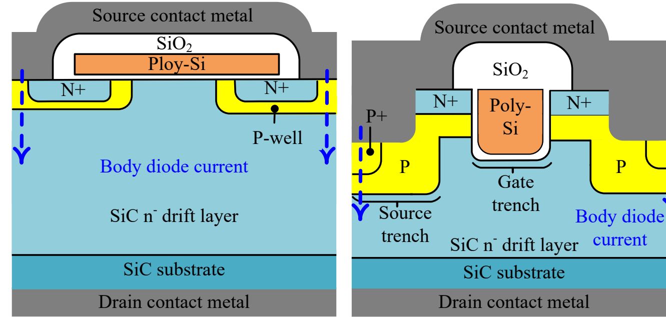
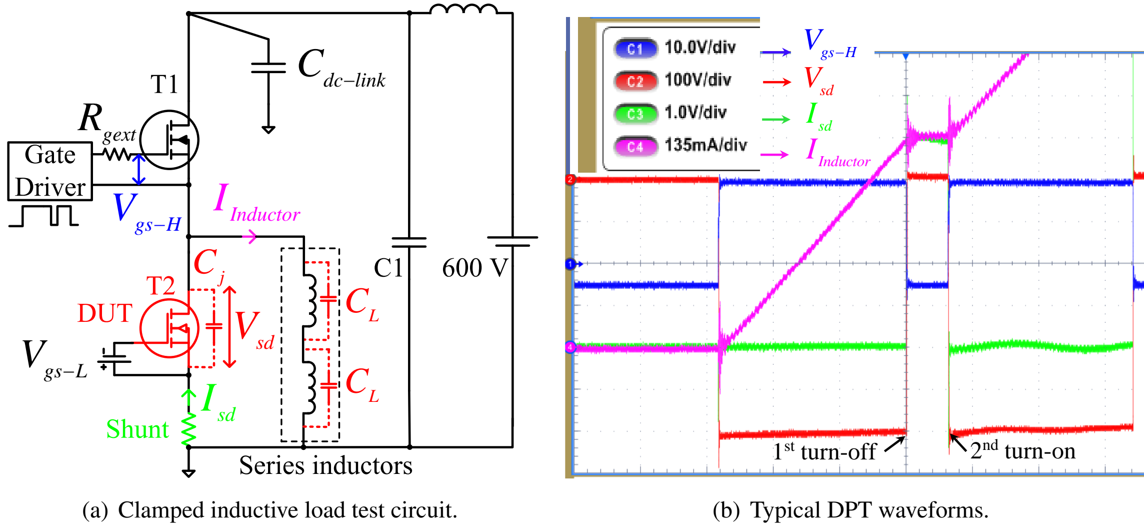


Fig. 1: Structures of planar (left) and double-trench: gate-source-trench (right) MOSFETs [4], [5].

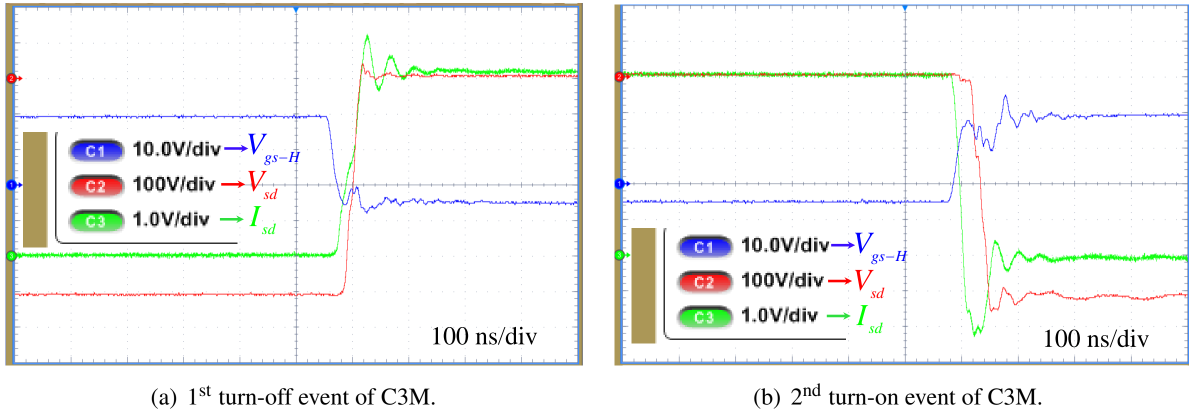


(a) Clamped inductive load test circuit.

(b) Typical DPT waveforms.

Fig. 2: Illustration of a clamped inductive load circuit for hard switching test of MOSFET body diode in a) and an example of a typical DPT waveforms in b) as labelled at different places in the circuit.

to cathode voltage of diode (V_{sd}), Channel 3 is the source to drain current (I_{sd}), and channel 4 is the current through load inductor ($I_{Inductor}$). By regulating the width of the first pulse and the dc-bus voltage, the desired load current is achieved. Each time only two pulses are applied and the DUT is switched only twice, and thus, the device junction temperature rise due to switching loss is negligibly small and the junction temperature can be controlled externally by hot plate. A gate voltage of 20 V is applied during turn-on and - 5 V during turn-off for the upper MOSFET. In order to use the passive probe and coaxial shunt for voltage and current measurements; respectively, with the same reference (grounding) as that of the oscilloscope, the body diode of low side transistor T1 is hard-switched. By varying the gate resistance (R_{gext}), the slew rates of the current and voltage across the DUTs are controlled. It should be noted that the internal resistance of T1 is 7 Ω. Detailed view of 1st turn-off and the 2nd turn-on events are displayed in Fig. 3.



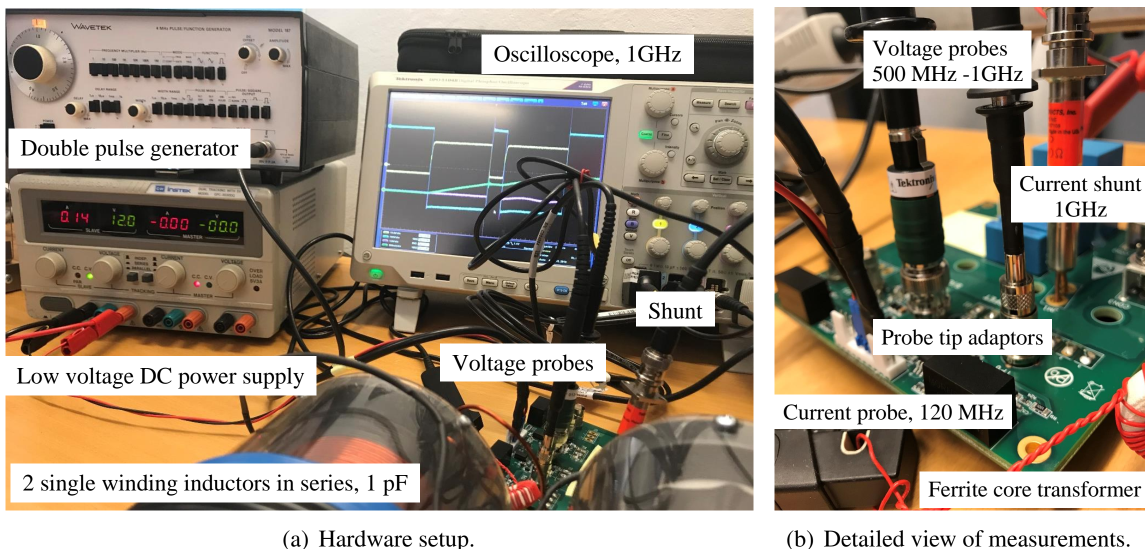
(a) 1st turn-off event of C3M.

(b) 2nd turn-on event of C3M.

Fig. 3: Illustration of the detailed view of the 1st turn-off and the 2nd turn-on events, as indicated in Fig. 2 b) for C3M MOSFET at 600 V and 20 A. For analysing the reverse recovery performance of the DUT, the 2nd turn-on instant, where the transistor is turned-on and the diode is turned-off, is the key point of interest which will be the focus in the upcoming sections of paper for different chosen DUTs.

4 Hardware setup and measurement issues

The complete laboratory setup with measurement is illustrated in Fig. 4. Double pulses are generated using a function generator. Two single-layer winding air core inductors are connected in series as an inductive load. The air core avoids the saturation, single-layer winding provides small stray capacitance (C_L), and the series connection further reduces C_L, and subsequently the true switching waveforms of the body diode are reflected. The equivalent stray capacitance of the load inductor is measured by an impedance analyser, E4990, and found to be 1 pF. Ground-lead inductance is another factor impacting the measurement accuracy of switching waveforms; as discussed in [20], [21]; because the typical ground-lead associated with voltage probe has an inductance and forms a series resonant network with the input capacitance of the probe. Therefore, a PCB probe tip adaptor is employed in order to reduce the ground-lead inductance, as shown in Fig. 4 b).



(a) Hardware setup.

(b) Detailed view of measurements.

Fig. 4: Laboratory setup showing the arrangement for current and voltage measurements of the body diode or freewheeling diode. The current is measured by a high bandwidth, low inductive current shunt; and the voltage is measured by a high bandwidth single ended probe with probe tip adaptor as displayed. Load current is measured with dc/ac current probe out of a 40 turns ferrite core transformer.

Table II: Equipments for voltage and current measurement.

Measured parameters	Equipment models	Bandwidth (MHz)
V_{gs-H}	Differential voltage probe, THDPO200, Tektronix	200
V_{gs-L}	Passive voltage probe, TPP1000, Tektronix	1000
V_{sd}	Passive voltage probe, P5100A, Tektronix	500
I_{sd}	Coaxial shunt, dc/ac, SDN - 25, 250 $m\Omega$, T & M Research	1000
$I_{Inductor}$	Split core current probe, dc/ac, TCP0030A, Tektronix	120
-	Oscilloscope, DPO5104B, Tektronix	1000

As SiC switches very fast, it is crucial to choose probes and oscilloscope with adequate bandwidth, the ones used for this work are enlisted in Table II. Further, the oscilloscope is calibrated and the voltage probes are compensated. The former is done in order to adjust the parameters of oscilloscope according to surrounding environment conditions, such as temperature, pressure, humidity, and the latter is performed to adjust the capacitance of voltage probes according to the input capacitance of the oscilloscope channel.

5 Experimental results

In this section, the reverse recovery characteristics of the various chosen DUTs are evaluated at different operating conditions including the forward current, turn-off voltage, and current commutating slope (di/dt). Further, this section is divided into 4 subsections. Subsection 5.1 compares planar versus trench SiC MOSFETs. Followed is the Subsection 5.2, which evaluates SiC Schottky diodes with different chip areas. Then, in Subsection 5.3, the switching performance of cascode SiC JFET is included. Finally, Subsection 5.4 compares the turn-off characteristics of all DUTs at two voltages: 400 V and 600 V.

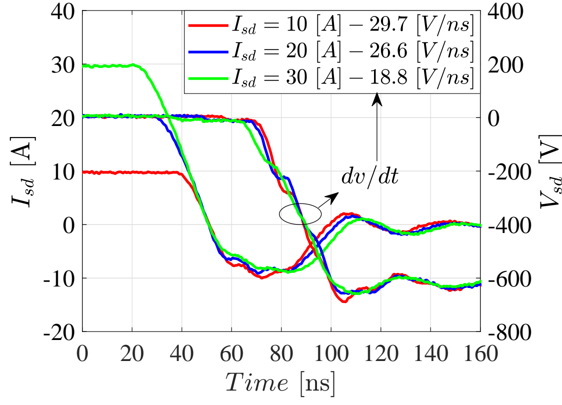
5.1 Planar (C3M) versus double-trench (SCT) MOSFETs

In this subsection, two technologies in SiC MOSFET: planar (C3M) versus double-trench (SCT) are compared. Fig. 5 shows the switching waveforms of body diodes in C3M versus SCT MOSFETs. Apparently, when I_{sd} through a body diode increases, I_{rrm} and t_{rr} are negligibly affected provided the same V_{sd}, as can be seen in Fig. 5 a) and b), unlike that in Si PiN diodes where these parameters significantly increase with increase in I_{sd} [22] indicating that there is a little or no charge storage mechanism in body diodes of these SiC MOSFETs. Indeed, there are essentially two reasons for smaller stored charges in SiC MOSFETs: first, the lower lifetime of the minority carrier, and second, the smaller physical area of the die, and hence, smaller area for stored charges in SiC compared to that in Si.

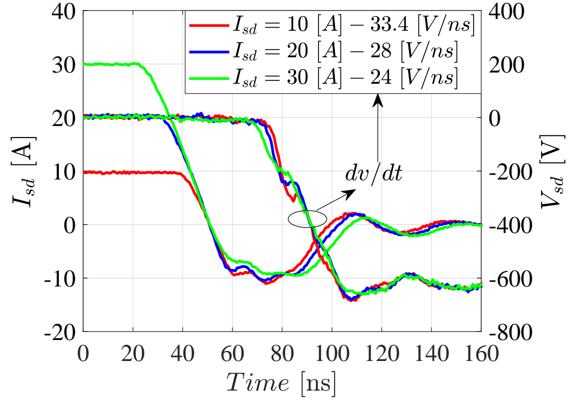
Further, it is also elucidated from Fig. 5 that lower the I_{sd}, the greater is the dv/dt. Note that dv/dt mainly concerns insulation strain. Examining the experimental results in Fig. 5 c) and d) at I_{sd} of 20 A, it is evident that both I_{rrm} and t_{rr} increase with supply voltage. Actually, higher energy (1/2 $\times$ C_{oss} $\times$ V_{sd}^2) is stored at higher voltage, and thus leads to higher charge, which is the reason for an additional area at higher voltage compared to lower voltage. As can be seen in Fig. 5 e) and f), the smaller gate resistance increases peak of I_{rrm} and di/dt_1. On closer observation, the body diode in SCT shows noticeable decrease in di/dt_1 with increase in R_{gext} than that in C3M.

5.2 Planar Schottky diodes (JBS) with different chip areas

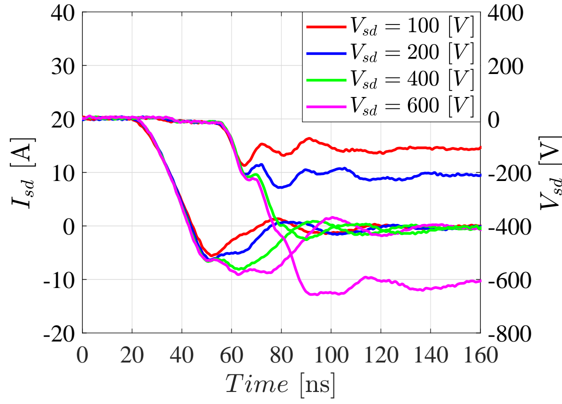
In this subsection, planar Schottky diodes with different chip sizes are compared. Fig. 6 reveals that SCS offers better reverse recovery performance than C4D which in fact is due to the smaller chip size of SCS, as enlisted in Table I. Measurements with SCS are shown up to 400 V because it has smaller voltage rating compared to C4D. It is observed that with the same R_{gext} of MOSFET, when the I_{sd} increases, dv/dt decreases in C4D whereas for the same conditions, the reverse is true in SCS.



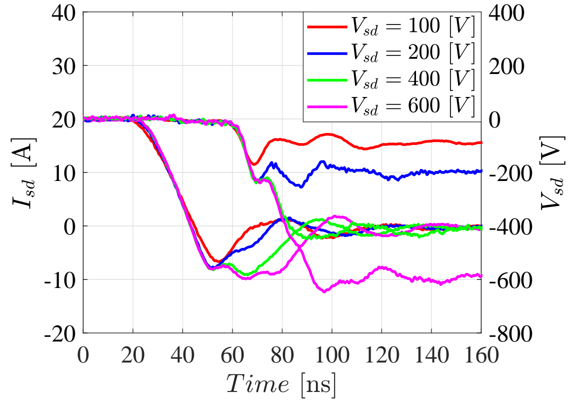
(a) Current variation in body diode of C3M at 600 V.



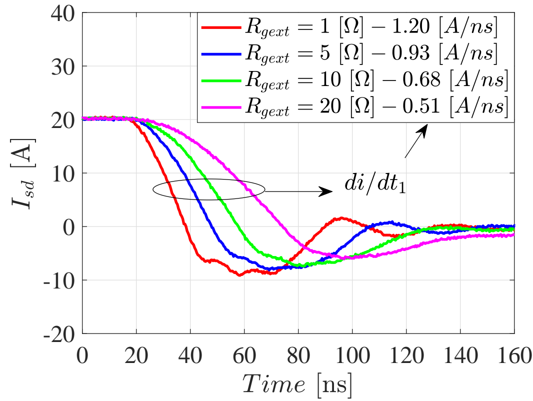
(b) Current variation in body diode of SCT at 600 V.



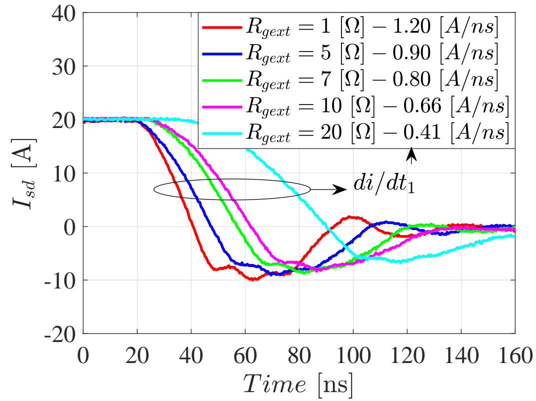
(c) Voltage variation in body diode of C3M at 20 A.



(d) Voltage variation in body diode of SCT at 20 A.



(e) R_{gext} variation in body diode of C3M at 600 V and 20 A.



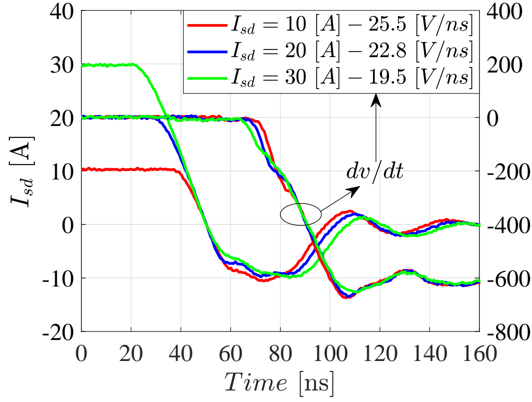
(f) R_{gext} variation in body diode of SCT at 600 V and 20 A.

Fig. 5: Current and voltage variation in the body diode of planar (C3M) versus double-trench (SCT) SiC MOSFETs illustrates that the recovery performances are similar in these devices, whereas gate resistance variation shows noticeable decrease in di/dt_1 in the body diode of SCT compared to those in C3M.

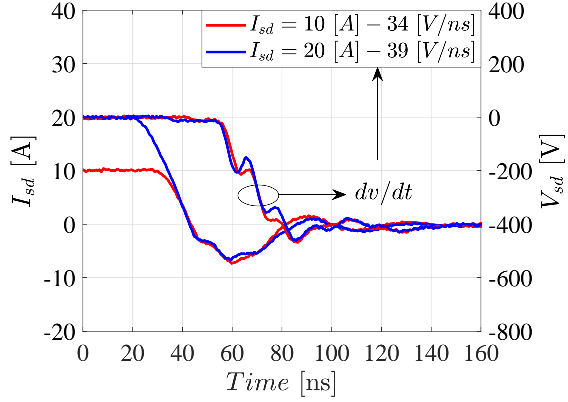
Table III shows the quantification of the key electrical parameters for SCS versus C4D from the laboratory measurements at R_{gext} of 1 Ω and two different V_{sd}: 100 V and 400 V. As shown, at 400 V, all the parameters including dv/dt, di/dt_2 (current slew rate during 2nd half of recovery), I_{rrm}, and t_{rr} are higher than those at 100 V. For the same V_{sd}, C_j in SCS is about 1.5 times smaller compared to that in C4D, and thereby the stored energy in the junction capacitance is about 1.5 times higher in C4D than in SCS. It is also observed that the dv/dt varies in the range of 20 V/ns to 39 V/ns in different diodes under considerations at 400 V.

Table III: dv/dt, di/dt_2, I_{rrm}, and t_{rr} of C4D and SCS at 20 A and 2 different voltages: 100 V, and 400 V.

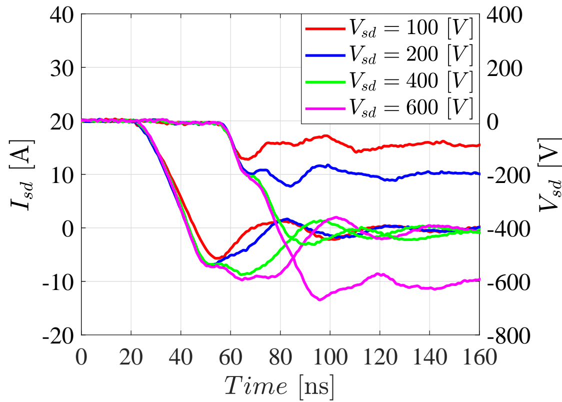
DUT	V_{sd} = 100 V					V_{sd} = 400 V				
	C_j (pF)	dv/dt (V/ns)	di/dt_2 (A/ns)	I_{rrm} (A)	t_{rr} (ns)	C_j (pF)	dv/dt (V/ns)	di/dt_2 (A/ns)	I_{rrm} (A)	t_{rr} (ns)
SCS310AP	90	19.7	0.29	2.46	24	48	39.0	0.36	6.66	43
C4D30120D	138	17.9	0.51	5.68	23	70	19.8	0.55	8.93	46



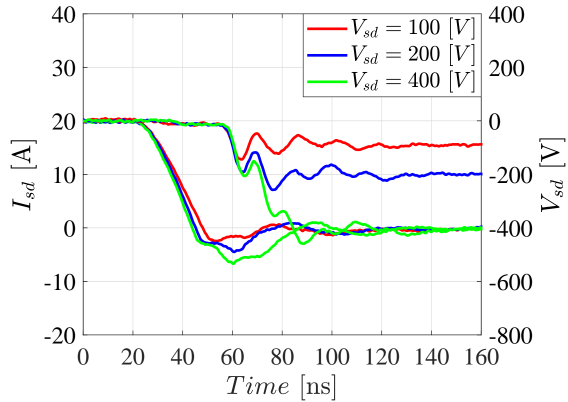
(a) Current variation in C4D at 600 V.



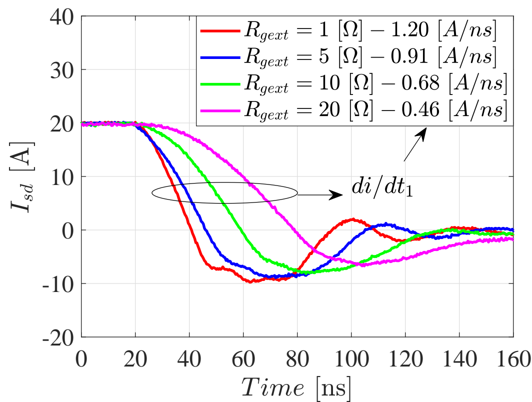
(b) Current variation in SCS at 400 V.



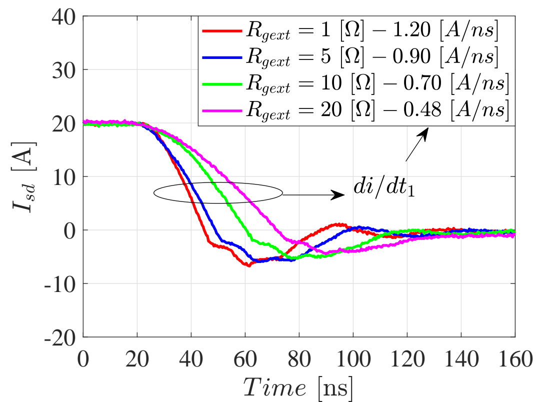
(c) Voltage variation in C4D at 20 A.



(d) Voltage variation in SCS at 20 A.



(e) R_{gext} variation in C4D at 600 V and 20 A.

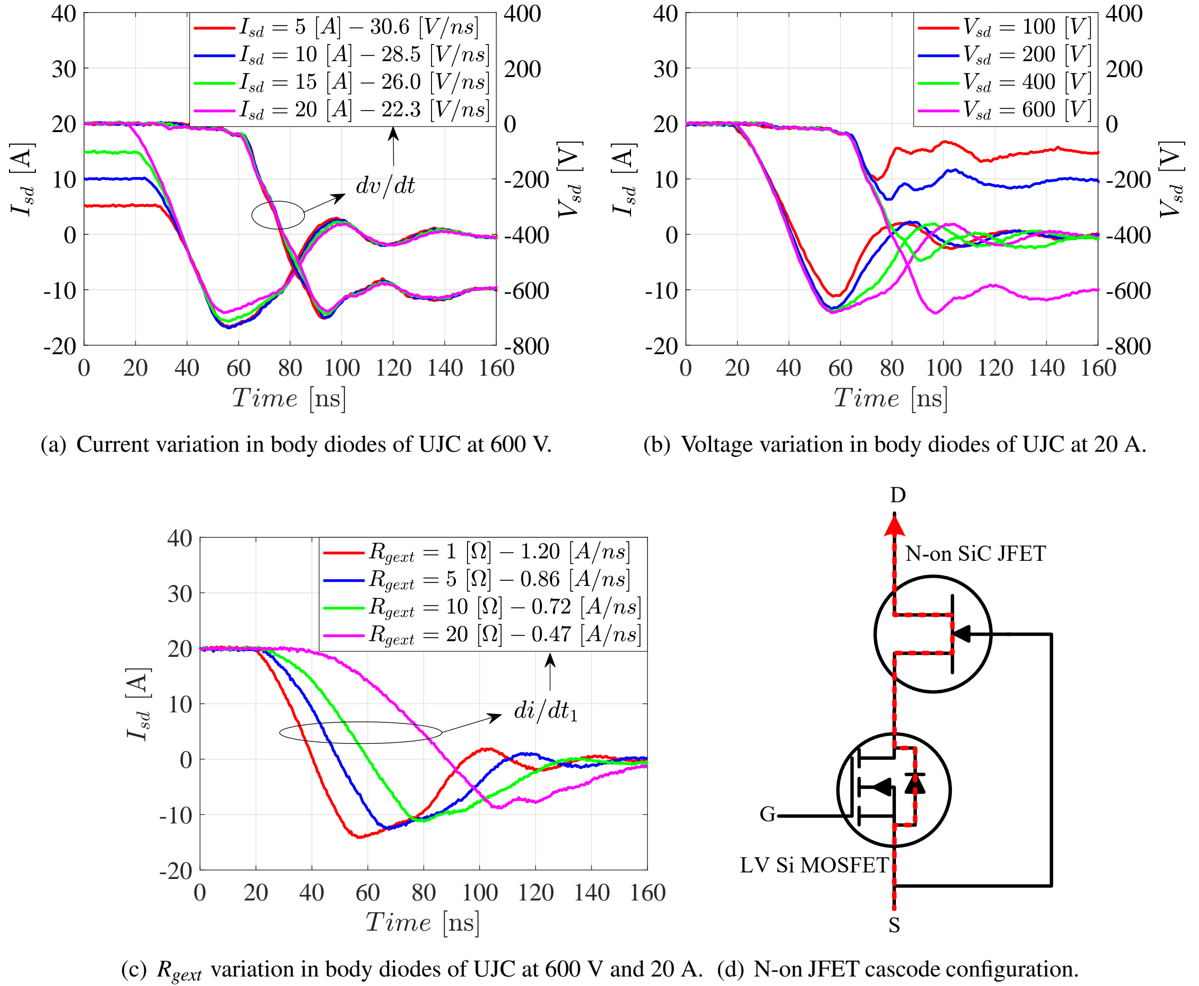


(f) R_{gext} variation in SCS at 400 V and 20 A.

Fig. 6: Impact of currents, voltages, and gate resistances variation in the Schottky diodes, C4D versus SCS, reveals that the reverse recovery performances are better in SCS.

5.3 Trench cascode JFET

In this subsection, the body diode in trench cascode JFET is discussed. Fig. 7 a) - c) depicts the turn-off switching performance of JFET. Clearly, it can be observed that the I_{rrm} in the body diode of SiC JFET decreases as I_{sd} increases and the opposite is true as V_{sd} or di/dt increases. It is worth mentioning that the trench SiC JFET does not contain a built-in body diode or any parasitic NPN transistor like in SiC MOSFET. However, during the reverse conducting mode, the body diode of low voltage (LV) Si MOSFET and the JFET channel provide current path, as routed by a red dashed line in Fig. 7 d), providing the same functionality like an anti-parallel diode.



(a) Current variation in body diodes of UJC at 600 V.

(b) Voltage variation in body diodes of UJC at 20 A.

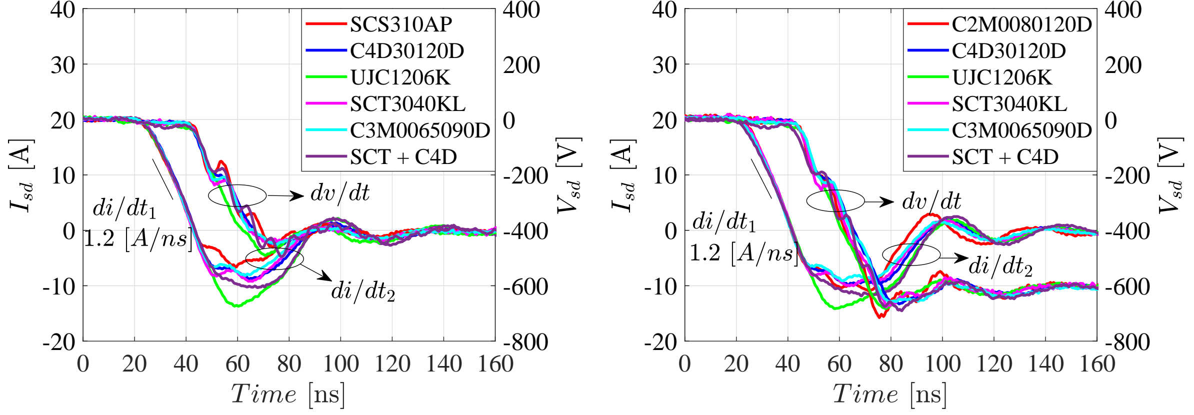
(c) R_{gext} variation in body diodes of UJC at 600 V and 20 A.

(d) N-on JFET cascode configuration.

Fig. 7: Current, voltage and di/dt variations in the body diode of trench SiC cascode JFET illustrate that as I_{sd} increases, I_{rrm} decreases; and as V_{sd} or di/dt increases, the I_{rrm} and the recovery area increases.

5.4 Comparison of DUTs at 400 V and 600 V

This subsection compares the turn-off voltage and current transients of all the DUTs. Fig. 8 shows the summary plots of all the DUTs switched at 25°C, R_{gext} of 1 Ω, and I_{sd} of 20 A for two different V_{sd}, namely, 400 V and 600 V. At the beginning or first-half of the reverse recovery di/dt_1 (governed by the upper transistor) is 1.2 A/ns, however, at the ending part or the second-half of it, di/dt_2 (mainly impressed by the diode technology) softens down for all the devices under consideration, and are shown in Table IV. The cascode SiC JFET possesses the highest I_{rrm} of all the cases under consideration, while the third generation SiC MOSFET, C3M0065090D, retains the lowest of all. It is clear from Fig. 8 that the recovery performance of body diode in SiC MOSFET is comparable to that of the SiC JBS diode. This is primarily a result of the very small minority carrier lifetime and thinner drift layer of SiC MOSFET, and thus, this leads to much smaller amount of stored charges in the device drift region.



(a) Plot of currents through diodes at V_{sd} of 400 V.

(b) Plot of currents through diodes at V_{sd} of 600 V.

Fig. 8: Comparison of the voltage and the reverse-recovery current of different diode technologies at 400 V a) and 600 V b). With R_{gext} of 1 Ω, di/dt_1 imposed by the circuit is 1.2 A/ns at both voltage levels, while di/dt_2 depends on the technology of diode, and circuit. The key electrical parameters such as dv/dt, di/dt_2, I_{rrm}, and t_{rr} are quantified and listed in Table IV for each of the DUTs.

In circuits where diodes conduct for longer periods, for instance, generator-side rectifier, an external anti-parallel SiC JBS is used to bypass the conduction losses contributed by the intrinsic diode of SiC MOSFET. Therefore, a case with a SiC MOSFET and an anti-parallel SiC diode (SCT + C4D, as indicated in Fig. 8) is also presented, which gives an impression that their combined impact increase the recovery loss compared to that of a case with a body diode only (marked by a legend SCT3040KL).

The t_{rr} and I_{rrm} depends on I_{sd}, V_{sd}, R_{gext} and junction temperature (not discussed in this paper), and are not provided for the same conditions in the datasheet, particularly when the devices are from different manufacturers. Moreover, dv/dt, di/dt_2, which are central parameters, are barely included in the datasheet. However, in this paper these parameters are compared at the same conditions, for instance, the same I_{sd}, V_{sd}, R_{gext}, and temperature (room temperature) for all the DUTs, and are presented in Table IV. As shown, dv/dt varies in the range of 21 V/ns to 37 V/ns at 600 V, which mainly involves insulation strain.

Table IV: dv/dt, di/dt_2, I_{rrm}, and t_{rr} of the investigated DUTs at 400 V and 600 V while keeping a constant di/dt_1 of 1.2 A/ns. Compared to 400 V, dv/dt, I_{rrm}, and t_{rr} are measured to be higher at 600 V.

DUT	V_{sd} = 400 V					V_{sd} = 600 V				
	C_j/C_{oss} (pF)	dv/dt (V/ns)	di/dt_2 (A/ns)	I_{rrm} (A)	t_{rr} (ns)	C_j/C_{oss} (pF)	dv/dt (V/ns)	di/dt_2 (A/ns)	I_{rrm} (A)	t_{rr} (ns)
C2M0080120D	100	28	0.53	9.80	44	85	30.4	0.66	11	47
C4D30120D	70	19.8	0.55	8.93	46	56	20.9	0.64	9.8	53
UJC1206K	100	21.0	0.73	13.74	46	90	24.9	0.68	14.2	55
SCT3040KL	120	28.5	0.63	9.20	52	90	31.1	0.54	10.2	53
C3M0065090D	70	25.6	0.40	8.13	45	60	26.3	0.51	9.2	52
SCT + C4D	190	34.9	0.70	10.34	47	146	36.7	0.75	11.8	55

6 Conclusion

Aside from the fact that a body diode in SiC MOSFET is of bipolar type, the switching characteristics are affected very insignificantly by the forward currents and commutation rates like in a unipolar SiC Schottky diode. Compared to the body diodes in SiC MOSFETs and unipolar Schottky diodes, the body diode in the cascode JFET showed higher peak reverse recovery current because the body diode in cascode structure is basically the combination of the body diode in low voltage Si MOSFET and the

channel of JFET. However, none of these diodes showed snappy behaviour and higher voltage overshoots as in Si PiN and fast recovery diodes. Thus, looking into the recovery losses of the body diodes in FET, SiC MOSFETs are better over cascode SiC JFETs while the converse is true in terms of the conduction losses. In particular, the body diode in a SiC JFET exhibits about the same conduction losses as the majority carrier Schottky diodes and 3-4 times lower compared to those of SiC MOSFETs. In addition, the comparison between the Schottky diodes reveal that diode with smaller chip area (SCS) has a better reverse recovery performance compared to that with larger chip area (C4D). In overall, as conduction losses are significant only during the dead time and the diodes normally are shunted by the transistor during the conduction phase, the body diodes of SiC FETs are good enough as freewheeling diodes. In future, similar evaluations will be performed for these devices at higher temperatures to reach a more concrete conclusion.

References

[1] C2M0080120D Datasheet, Cree, Inc., 2014.

[2] C4D30120D Datasheet, Cree, Inc., 2014

[3] F. Dahlquist, "Junction Barrier Schottky Rectifiers in Silicon Carbide", PhD dissertation, Department of Microelectronics and Information Technology, KTH Royal Institute of Technology, Stockholm, 2002.

[4] T. Nakamura et al., "High performance SiC trench devices with ultra-low ron," 2011 International Electron Devices Meeting, Washington, DC, 2011, pp. 26.5.1-26.5.3.

[5] Rohm, "New products under development: 3rd gen SiC MOSFET", 2014. [Online]. Available: http://www.rohm.com/documents/11303/2871848/3rd-gen-MOSFETs.pdf.

[6] SCS310AP Datasheet, Rohm, Inc., 2017.

[7] B. Callanan, Application considerations for silicon carbide MOSFETs, Power Electronics Europe, Cree, Inc., 2010.

[8] CMF20120D Datasheet, Cree, Inc., 2012.

[9] R. Callanan, J. Rice and J. Palmour, "Third quadrant behavior of SiC MOSFETs," 2013 Twenty-Eighth Annual IEEE Applied Power Electronics Conference and Exposition (APEC), Long Beach, CA, USA, 2013, pp. 1250-1253.

[10] M. Hayashiguchi, K. Hayashi, N. Hase and K. Ino, SiC MOSFET-Only Module Increases Current at Reduced On-Resistance in Power Electronics Europe, 2013.

[11] J. Jordàn et al., "A Comparative Performance Study of a 1200 V Si and SiC MOSFET Intrinsic Diode on an Induction Heating Inverter," in IEEE Transactions on Power Electronics, vol. 29, no. 5, pp. 2550-2562, May 2014.

[12] S. Bontemps, A. Basler and P. L. Doumergue, "Evaluation of the need for SiC SBD in parallel with SiC MOSFETs in a module phase leg configuration," Proceedings of PCIM Europe 2015; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, Nuremberg, Germany, 2015, pp. 1-7.

[13] D. Martin, W. A. Curbow, B. Sparkman, L. E. Kegley and T. McNutt, "Switching performance comparison of 1200 V and 1700 V SiC optimized half bridge power modules with SiC antiparallel schottky diodes versus MOSFET intrinsic body diodes," 2017 IEEE Applied Power Electronics Conference and Exposition (APEC), Tampa, FL, 2017, pp. 2297-2304.

[14] S. Jahdi et al., "An Analysis of the Switching Performance and Robustness of Power MOSFETs Body Diodes: A Technology Evaluation," in IEEE Transactions on Power Electronics, vol. 30, no. 5, pp. 2383-2394, May 2015.

[15] C3M0065090D Datasheet, Cree, Inc., 2015.

[16] V. Pala et al., "900V silicon carbide MOSFETs for breakthrough power supply design," 2015 IEEE Energy Conversion Congress and Exposition (ECCE), Montreal, QC, 2015, pp. 4145-4150.

[17] SCT3040KL Datasheet, Rohm, Inc., 2016.

[18] UJC1206K Datasheet, USCI, Inc., 2017.

[19] J. Hostetler, W. Simon, X. Huang, and A. Bhalla, "High current SiC devices", USCi, 2016. [Online]. Available: https://curent.utk.edu/files/3814/6098/8506/John_Hostetler_DOE_April_1.pdf.

[20] S. Tiwari et al., "Design considerations and laboratory testing of power circuits for parallel operation of silicon carbide MOSFETs," 2015 17th European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe), Geneva, 2015, pp. 1-10.

[21] "Technical Manual, ABC of probes", Tektronix Inc.

[22] S. Tiwari, O. M. Midtgård and T. M. Undeland, "SiC MOSFETs for future motor drive applications," 2016 18th European Conference on Power Electronics and Applications (EPE'16 ECCE Europe), Karlsruhe, 2016, pp. 1-10.