NTNU – Trondheim
Norwegian University of
Science and Technology

Fault Tolerant Modular Multilevel Converter

Investigation of a New Method for Fault Tolerant Control

Idun Runde Mosgren

Master of Energy and Environmental Engineering
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Supervisor: Lars Einar Norum, ELKRAFT

Norwegian University of Science and Technology
Department of Electric Power Engineering

Problem Description

To this day, there are several challenges towards fault tolerant control of the Multilevel Modular Converter. Published research in this field are few, but rapidly increasing. The student shall investigate the feasibility of a novel approach to continue operation after a component fault.

In the fault tolerant state, the line to line voltages should remain equal to the pre-fault condition. The student is expected to include theoretical evaluation and simulation testing. A hardware prototype should be built to verify simulation results.

The thesis work is collaboration with Siemens Energy in Trondheim.

Simulation Part

A simulation model with a constant DC-link and a passive load shall be constructed. The references will hereby be constant and only pulse width modulation and capacitor voltage balancing is needed for control.

Experimental Part

The experimental part will consist of reconfiguring a prototype available at NTNU. This shall be done in cooperation with the workshop at NTNU. The prototype shall be well documented to facilitate future use by others.

Assignment given: Trondheim – 22.01.14

Supervisor: Professor Lars Norum, Department of Electric Power Engineering

Co-Supervisor: Anandarup Das, Senior Development Engineer, Siemens Energy, Trondheim

Preface

Throughout the work with this thesis, I have gained experience in creating a simulation model, and building of a prototype. I have also learned about the process of developing a new method of control.

The achievements made during the work with this report would not have been possible without the help from numerous people. I would like to thank my Supervisor Lars Norum for the help he has given during the semester.My Co-Supervisor Anandarup Das has given me technical guidance, as well as advice regarding the writing process and prioritizing of tasks. He has also given me motivation and feedback for which I am grateful. I would also like to thank Hamed Nademi for his help during the start-up phase of the project.

The prototype has mostly been built by the workshop at NTNU. There have been many choices to make during the process, and their experience with laboratory work made the physical setup possible. Special thanks to Vladimir Klubicka, Svein Erling Norum, Bård Almås and Aksel Andreas Hanssen. I would also like to thank Kjell Ljøkelsøy for valuable inputs in the decision making process for the control signals' path.

I also thank my office mates Thomas, Martin, Erlend and Anne-Siri for cheering me on, and my NTNU friends and classmates for joyful years at campus. Last, but not least I thank my partner Alexander and my family for supporting me.

Idun Runde Mosgren

Trondheim, Norway 23.06.2014

Sammendrag

Denne hovedoppgaven har handlet om virkemåten av en flernivå frekvens-omformer (MMC), og feiltolerant kontroll av denne. MMC er en spenningsomformer (VSC) som er satt sammen av mange mindre moduler (SM). Teknologien rundt MMC utvikler seg raskt, og forskning pågår for å utvide bruksområdene. MMC er fordelaktig for å fortsette levering av kraft etter en feil fordi den er bygd opp av mange moduler. Hvis det har oppstått en feil i en SM, kan den kobles ut av kretsen.

Det har blitt utviklet en ny metode for feiltolerant-kontroll basert på en idé om å modifisere referanseverdiene som brukes til modulasjonen av omformeren. Dette for å oppnå balanserte linje til linje-spenninger. Metoden retter seg mot feil som oppstår i en av SMene. Hovedfordelen med denne metoden er at den bruker potensialet i de fasene som ikke har feil for å opprettholde de samme spenningsamplitudene som før feilen oppsto. Dette kan redusere kostnadene til omformeren.

Metoden, her kalt Referanse Modifikasjons Metoden (RMM), har blitt undersøkt både teoretisk, ved simulering og testing i laboratoriet. Teoretisk undersøkelse av den nye metoden, viser et klart potensiale. Verdien av metoden avhenger av antall moduler i omformeren. Mange moduler gir større gevinst. Under enkle datasimuleringer viser metoden til bra resultater. Spenningene og strømmene forblir balanserte med de samme amplitudene som før feil.

Verdien av RMM har vist seg å ha stort potensiale basert på resultatene i denne rapporten. I resultatene fra datasimulering og laboratorieoppsettet aviker den fundamentale spenningsamplituden med omtrent 15% ved normal kjøring. Avviket kan blant annet skyldes feilaktige antagelser om resistive tap i simuleringsmodellen. Da laboratorieoppsett ble kjørt med RMM, viste målinger forventede armspenninger. Fase spenningene er balanserte, men viser et amplitude avvik på 6-7% og linjespenningen 4-5% fra normal til RMM-kjøring. Det ble målt uventede topper i strømmene i den fasen med feil. Det er ikke antatt at disse toppene skyldes metoden men heller hvordan testen ble gjennomført. Videre undersøkelser burde bli gjort for å verifisere metoden I et laboratorieoppsett.

Summary

In this thesis work, fault tolerant control and operation of a Modular Multilevel Converter (MMC) has been investigated. The MMC consists of multiple Sub Modules (SM). The MMC technology is rapidly evolving, and research is ongoing to make it suitable for more applications. Uninterruptable power distribution is more crucial than ever due to an increasing dependence on electric power supply for several operations, and the cost related to blackouts. The modularity of the MMC is advantageous for uninterruptable operation. If one SM fails, it can easily be bypassed and the converter can continue to operate. For the MMC the availability is very high, although the amount of components leads to a lower reliability than some of the conventional multilevel converters.

A new fault tolerant control has been developed based on an idea of modifying the reference waveforms that is used in the modulation. This is to maintain balanced line to line voltages. The method addresses faults that occur within one of the SMs. The advantage of this method is that existing redundancies in the non-faulty phases is used to maintain the same voltage amplitudes as in the pre-fault state. This can potentially reduce the cost of the converter.

Investigation of the Reference Modification Method (RMM) has been done theoretically, by computer simulation and in the laboratory. Theoretically the RMM has proven valid. The commercial value of the method is assumed to depend greatly on the amount of SMs present in the design. The computer simulation results indicate that the voltages and currents remain balanced and with the same amplitudes as in pre-fault condition.

The RMM shows great potential based on the results in this report. Steady state values from simulation and hardware differ with approximately 15 %. This deviation is expected to be caused by underestimation of resistive losses in the hardware circuit. When the RMM was run on the hardware setup, arm voltage measurements showed the expected shapes and amplitudes. The phase voltages show a deviation by 6-7% from the steady state values and the line voltages a deviation of 4-5%. Unexpected arm current peaks in the faulty phase were observed. It is expected that these occurred due to how the test was conducted and not the method to be tested. Further investigation of the method should be done to verify the results in this report.

Theory is when you understand everything but nothing works.

Practice is when everything works but nobody knows why.

In our lab, theory and practice are combined;

nothing works and nobody knows why.

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Nomenclature

SYMBOL	PARAMETER	UNIT
ω	Angular frequency	rad s^2
α	Angle	rad or degrees
f	Frequency	Hz
ia	Phase A current	A
iu	Phase u current	A
in	Lower arm current	A
ip	Upper arm current	A
vc	Circulating current voltage drop	A
vcnu#	Voltage across Sub Module # in lower arm	V
vcpu#	Voltage across Sub Module # in lower arm	V
Vdc	DC-link voltage	V
iz	Circulating current	A
L	Arm inductance	H
C	Sub module capacitance	F
vao	Ideal phase A output	A
vcp	Sum sub module output, upper arm	V
vcn	Sum sub module output, lower arm	V
Wp	Stored energy in capacitors upper arm	J
Wn	Stored energy in capacitors lower arm	J
N	Amount of sub modules per arm	1
Uref	Reference voltage	V
Ts	Fundamental period	s
Va, new, min	Post fault ideal minimum voltage	V
VA	Phase A voltage	V
VB	Phase B voltage	V
VC	Phase C voltage	V
VAB	Line to line voltage A-B	V
VBC	Line to line voltage B-C	V
VCA	Line to Line voltage C-A	V

List of Abbreviations

ABBREVIATION	DESCRIPTION
AC	Alternating Current
AFTCS	Active Fault Tolerant Control Systems
CHMC	Cascaded H-bridge Multilevel Converter
DC	Direct Current
dq	Direct and Quadratic axis coordinate system
EMI	Electromagnetic Interference
FDD	Fault Detection and Diagnosis system
FFT	Fast Fourier Transform
FTC	Fault Tolerant Control
HBBB	H-Bridge Building Block
HIL	Hardware In Loop
HVDC	High Voltage Direct Current
IGBT	Insulated-Gate Bipolar Transistor
LSPWM	Level-Shifted Pulse Width Modulation
MMC	Modular Multilevel Converter
N	Number of SMs in Each Arm
NTNU	Norwegian University of Science and Technology
PFTCS	Passive Fault Tolerant Control Systems
PSPWM	Phase-Shifted Pulse Width Modulation
PWM	Pulse-Width Modulation
RMM	Reference Modification Method
RTI	Real Time Testing
SM	Sub Module
STATCOM	Static Synchronous Compensator
TRIAC	Triode for Alternating Current
VSC	Voltage Source Converter

Chapter 1

Introduction

1.1 Background

MMC is a Voltage Source Converter (VSC) which comprises multiple Sub Modules (SM). It is in use for High Voltage Direct Current (HVDC) applications and is advantageous because of the lower need for filter in contrary to conventional two level VSC. The multiple voltage levels produce a sinusoidal voltage with few lower order harmonic contributions. The MMC technology is rapidly evolving, and research is ongoing to make the MMC suitable for more applications.

Uninterruptable power distribution is more crucial than ever due to an increasing dependence on electric power supply for several operations, and the cost related to blackouts. The modularity of the MMC is advantageous for uninterruptable operation. If one SM fails, it can easily be bypassed and the converter can continue to operate. This property is very beneficial for installations where equipment is difficult to access. To fully benefit from this, a complex controller is required to detect the fault and continue to operate after bypassing the faulty SM It is also important to have an acceptable transient period to ensure that the other components in the converter are not damaged. For the MMC, the availability is very high although the amount of components leads to a lower reliability than some of the conventional multilevel converters.

1.2 Scope of Work

This study focuses on the change of Pulse Width Modulation (PWM) reference waveform as a mean to obtain a Fault Tolerant Control (FTC). The goal is to maintain balanced line to line voltages with the same amplitude as before the bypass.

The work to be done in this project can be divided into three parts; theoretical, computer simulation and physical experimentation. For all three parts, a thorough evaluation of steady state operation of the MMC will be performed. This evaluation has two goals; first, it is important to understand the steady state operation in order to develop a good fault tolerant control. Second, the results from the fault tolerant state should be compared to the steady state

results for verification of the control effectiveness. This thesis work will be based on the author's work in TET4520 Electric Power Technology, Specialization Project.

After a theoretical basis is developed, a MMC model will be developed and simulated. MATLAB Simulink and the SimPowerSystems toolbox will be used.

The results from the fault tolerant control by computer simulation will be evaluated before implementing the new method in the hardware setup. The reason for this is; first, it reduces the risk of over currents and voltages in the hardware caused by faults in the control algorithm. Third, it increases the credibility of the comparison between hardware and software results. Wrongly made simplifications and assumptions in a simulation model, will show more clearly if the results have been evaluated before the hardware results are gathered. The hardware setup will also be operated at low voltages first, to limit the risk of damage by over currents and voltages.

There exist several different MMC topologies, but this project will focus on the DC/AC double star chopper-SM type.The control system to be used for the setup is called dSPACE. Speedgoat was considered, but based on experience from a former master student it was disregarded [1]. The amount of SMs is restricted by the amount of digital outputs from the control system to be used for the hardware setup. In order to compare the simulation and laboratory results, the amount of SMs should be the same.

1.3 Report outline

The structure and general outline is:

Chapter 2: In order to investigate the fault tolerant behavior of the MMC, a general understanding of the operation principle is necessary, and is presented here. This chapter covers the fundamental aspects of the MMC.

Chapter 3: Introduction to fault tolerant control and presentation of relevant vocabulary. The mathematical description of the Reference Modification Method can be found here. A short description of the procedure to investigate the feasibility of the method is also included.

Chapter 4: The simulation model's parameters and results can be found in this chapter. The results are divided into one section for the steady state and one section for the fault tolerant state. The results are analyzed based on Fourier analysis.

Chapter 5: The construction and control system of the hardware setup is presented in this chapter. The construction of the hardware has been described in detail to ease use in future projects. Steady and fault tolerant state results are presented and discussed.

Chapter 6: A comparison of the results obtained from the simulation and the hardware setup is presented. The chapter is completed by a summary of possible sources of errors in this project.

Conclusions and Further Work: Outlines the important conclusions that can be drawn from the results obtained in this project. Further work on this topic is suggested.

Chapter 2

Principle of the

Fault Tolerant Modular Multilevel

Converter

Introduction

In this chapter, an overview of the steady state operation is presented. First, some of the main advantages and disadvantages with this topology are described in 2.1. Second, the circuit components and their dynamic behavior are presented in 2.2 and 2.3. Third, the control of switching signals and capacitor voltage balancing are explained in 2.4 and 2.5.

2.1 Advantages and Disadvantages for the MMC

There are multiple modular VSC topologies presented in literature. For this project the DC/AC double star chopper-SM type will be studied. When the name MMC is used in this report, it is implicit that it is referred to this topology. In literature, it is also called the M2C.

The MMC offers some advantages and unique features, and the most important for this thesis are presented as follows [2] [3].

- Its AC voltage has low harmonic contents due to harmonic cancellation among multiple Sub Modules (SM), and therefore the need for a filter is greatly reduced.

- The currents in MMC arm and DC link are continuous, and the DC link capacitor can be omitted.
- The switching frequency for each IGBT is lower than for conventional two-level VSC.
- In a DC link short circuit fault, only some of the SM capacitors are discharged and the discharging current is limited by the protection choke in the arms. Therefore the system recovers fast.
- The system can remain operative even when a few SM are out of order.

2.2 MMC Topology

The MMC topology is presented in Figure 2-1. As described in [4], the three-phase MMC can be divided into three legs, one for each phase. Each leg consists of two arms, the upper arm and the lower arm. The arms are made out of N SMs each, also called cells or modules, which for starters can be considered as controllable DC voltage sources. The output voltage of these sources is either 0 or v_C.

Ideally, v_C is equal for all SMs. Each arm can therefore be considered as an AC controllable voltage source which is visualized in Figure 2-2. Each source will produce a sinusoidal output with a DC offset. The amount of voltage levels that can be achieved in each arm is N+1 [5]. As described in [6], N SMs are inserted and N SMs are bypassed in one leg at any given time. The DC-link is parallel to the phase legs so the combined voltage across each leg is equal to the input DC-link.

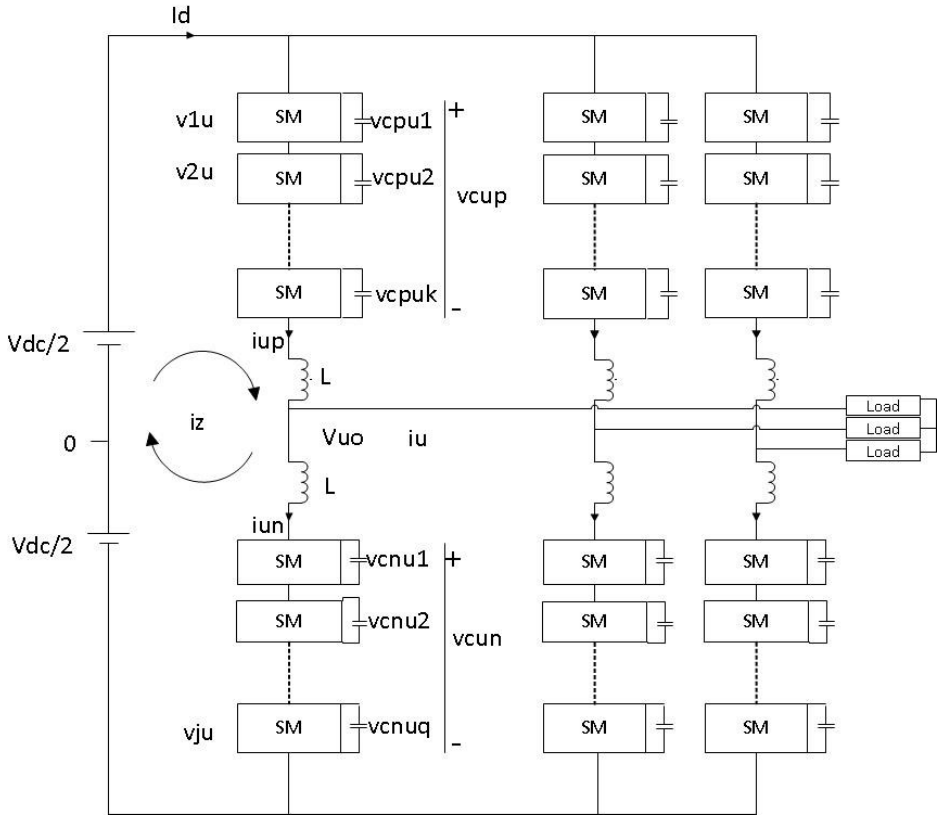

Figure 2-1 Three-phase MMC

By switching the SMs in the upper and/or lower arm, the output voltage is adjusted. The MMC is in use for the HVDC PLUS and the SVC PLUS technology delivered by Siemens [3]. A typical converter arrangement of 400MW would require more than 200 SMs. The SMs can be designed in different ways [7].

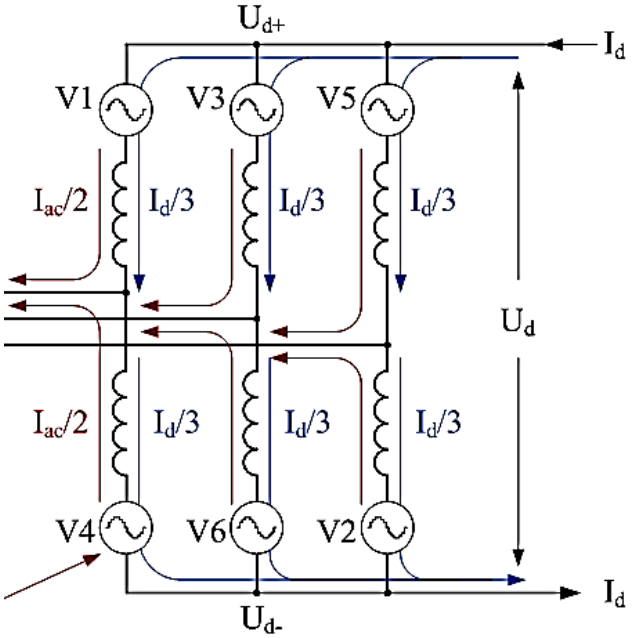

Figure 2-2 Controllable Voltages Sources [8]

In Figure 2-3, the output phase to ground voltage waveform of the MMC is presented. The sum of the SM voltages in the upper and lower arm is shown by the light green and dark green arrows. The voltage waveforms are the output of the visualized controllable voltage sources situated in each arm. The sum of the SM voltages in the upper arm and lower arm is equal to the input DC-link represented by the red arrows.

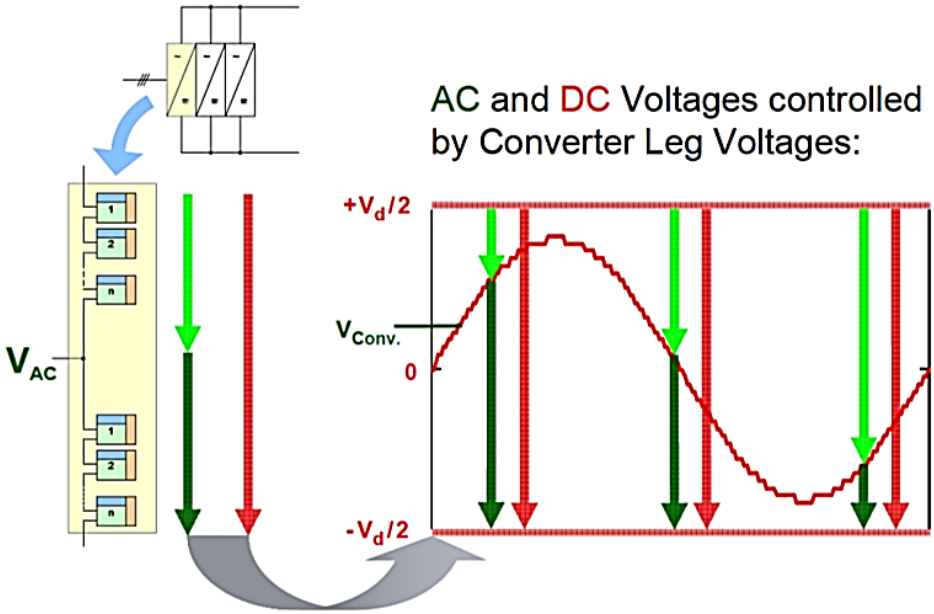

Figure 2-3 Modular Multilevel Converter Voltage Output of One Phase [3]

One SM consists off two IGBTs and one capacitor. To produce the sinusoidal waveform for each arm, the IGBTs are switched either ON or OFF to produce an output of either 0 or v_c. According to [3], there are three possible states for a SM, shown in Figure 2-4.

1) Default: Both IGBTs are switched off
2) State ON: IGBT1 switched ON and IGBT2 switched OFF
3) State OFF: IGBT1 switched OFF and IGBT2 switched ON

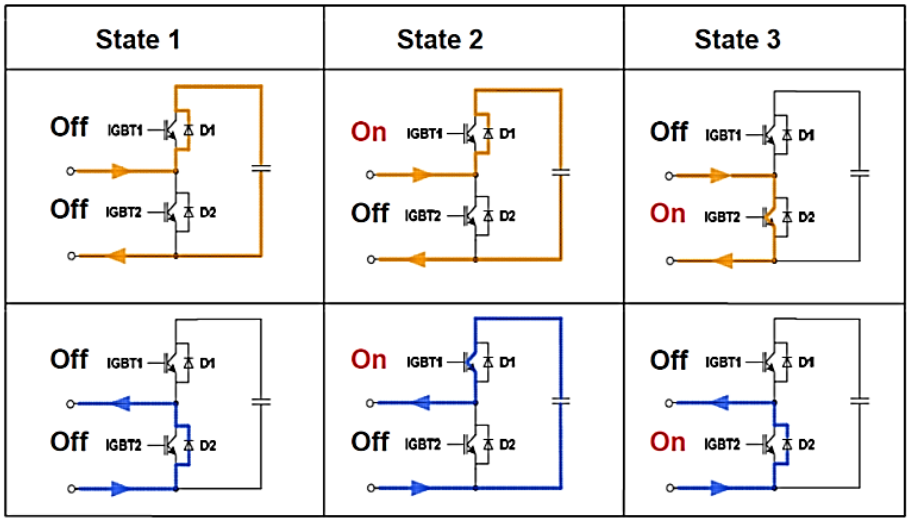

Figure 2-4 Different States for the Sub Modules [3]

The capacitor may charge when the current passes through the diode. Since the default state of many IGBT modules are equal to this state, the capacitors connected to them can charge even though the control signals are off. In state 2, the capacitor can charge or discharge depending on the current polarity. During steady state operation of the converter, the IGBT modules will be in state 2 or 3. For state 3, the current does not pass through the capacitor and the capacitor voltage stay constant. Because of these properties, the capacitor voltages require a balancing control, which is described in 4.1.1.2.

An inductance is connected in each arm. It is present to limit arm-current transients, current harmonics and fault currents. The inductors also have an inner resistance which will contribute to the converter losses [5]. Current transients may occur because of the time varying voltages across the capacitors leading to unequal leg voltages. There will also be resistive losses in the circuit due to wires and switching losses.

2.3 Mathematical Model

In order to describe the dynamic operation of the MMC, a mathematical model will be presented. The following equations describe the inductor currents relations and the capacitor voltages dynamics. The neutral point can be placed either between the lower arm and the DC-link or between two DC-links. Respectively, the first option can be seen in Figure 2-2 and the second option can be seen in the one-phase model in Figure 2-5. The mathematical description of the MMC is based on Figure 2-5. For simplicity it is assumed that the two DC-links are equal at all times and resistive losses are neglected. This mathematical model is based on basic circuit theory in addition to [5] and [9].

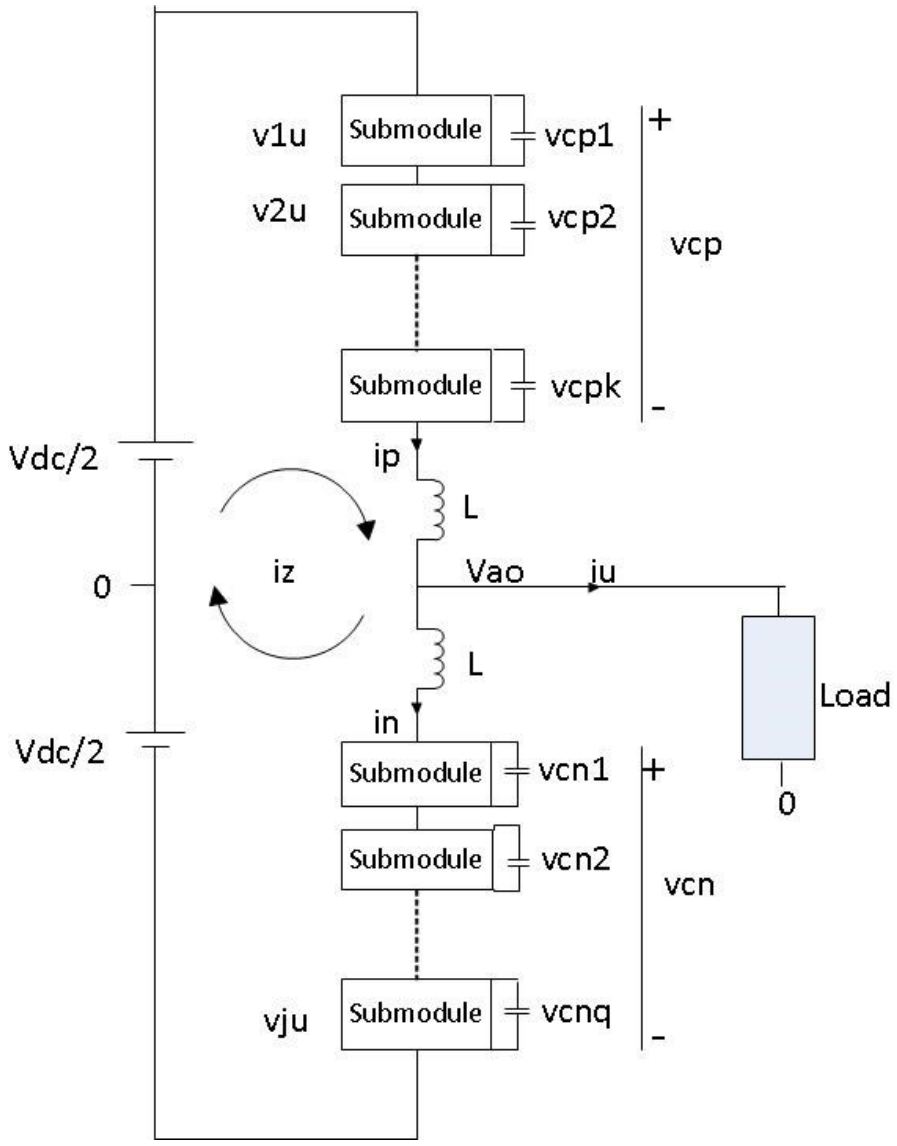

Figure 2-5 MMC, One Phase Circuit

2.3.1 Input and Output Currents and Voltages

According to [9] and Kirchoff's Current Law the arm and phase currents are given by Eq. [2.1] to [2.4].The notations are the same as Figure 2-5 where i_p is the upper arm current and i_n is the lower arm current. The circulating current is i_z and the output phase current is i_u.

$$i_p = \frac{i_u}{2} + i_z \qquad [2.1]$$

$$i_n = -\frac{i_u}{2} + i_z \qquad [2.2]$$

$$i_z = \frac{1}{2}(i_p + i_n) \quad [2.3]$$

$$i_u = i_p - i_n \quad [2.4]$$

Eq. [2.1] and [2.2] indicate that i_p and i_n are phase shifted with 180°. The magnetic fluxes from the i_u part will cancel each other out and the inductor only presents an inductance to the circulating current, i_z. The inductor will thus work to limit the circulating current as intended. The upper and lower arm currents will ideally contribute equally to the output phase current, see Figure 2-2. The DC-loop and the voltage drop caused by the circulating current is

$$V_{dc} = \sum_{j=1}^{\#j} v_{ju} + L\frac{d}{dt}(i_p + i_n) \quad [2.5]$$

$$v_Z = \frac{V_{dc} - v_{cp} - v_{cn}}{2} \quad [2.6]$$

where V_{dc} is the DC-link voltage, v_{ju} is the output voltage of SM number j, L is the arm inductance, v_Z is the voltage drop caused by the circulating current, v_{cp} and v_{cn} is the upper and lower arm sum capacitor voltage.

2.3.2 Inductor Currents

From the circuit in Figure 2-5, the following equations can be obtained

$$\frac{V_{dc}}{2} - v_{cp} - L\frac{di_p}{dt} = v_{a0} \quad [2.7]$$

$$-\frac{V_{dc}}{2} + v_{cn} + L\frac{di_n}{dt} = v_{a0} \quad [2.8]$$

where v_{a0} is the output phase voltage. From the summation of Eq. [2.7] and [2.8] and substitution of Eq. [2.3], the dynamic current equations are

$$\frac{L}{2}\frac{di_u}{dt} = \frac{v_{cn} - v_{cp}}{2} - v_{a0} \quad [2.9]$$

$$L\frac{di_z}{dt} = \frac{V_{dc} - v_{cp} - v_{cn}}{2} \quad [2.10]$$

2.3.3 Capacitor Voltages

Based on the energy storage in the capacitors, the relations are [5],

$$W_p = \frac{C}{2}\sum_{k=1}^{N}(v_{cpk})^2 \quad [2.11]$$

$$W_n = \frac{C}{2}\sum_{q=1}^{N}(v_{cnq})^2 \quad [2.12]$$

where W_p and W_n are the energy stored in the upper and lower arm, C is the SM capacitor, v_{cpk} and v_{cnq} is the SM capacitor voltage, numbered k and q, in the upper and lower arm. The time derivative of the stored energy per arm must equal the instantaneous input power to that arm;

$$\frac{dW_p}{dt} = C\sum_{k=1}^{N} v_{cpk}\frac{dv_{cpk}}{dt} = v_{cp}i_p \quad [2.13]$$

$$\frac{dW_n}{dt} = C\sum_{q=1}^{N} v_{cnq}\frac{dv_{cnq}}{dt} = v_{cn}i_n \quad [2.14]$$

The time derivative of the capacitor voltage will be different for each SM because they will be controlled with separate switching signals. On the other hand, the capacitors are considered to be large enough to keep the deviations from the reference value small. This is important to obtain balanced phase and line voltages. Each capacitor voltage can therefore be approximated to its mean value, which transforms the equations into,

$$\frac{dW_p}{dt} = C\sum_{k=1}^{N} v_{cpk}\frac{dv_{cpk}}{dt} \asymp \frac{C}{N}\sum_{k=1}^{N} v_{cpk}\sum_{k=1}^{N}\frac{dv_{cpk}}{dt} = \frac{C}{2N}\frac{d(\sum_{k=1}^{N} v_{cpk})^2}{dt} \quad [2.15]$$

$$\frac{dW_n}{dt} = C\sum_{q=1}^{N} v_{cnq}\frac{dv_{cnq}}{dt} \asymp \frac{C}{N}\sum_{q=1}^{N} v_{cnq}\sum_{q=1}^{N}\frac{dv_{cnq}}{dt} = \frac{C}{2N}\frac{d(\sum_{q=1}^{N} v_{cnq})^2}{dt} \quad [2.16]$$

The corresponding energy storage per arm is,

$$W_p = \frac{C}{2N}(\sum_{k=1}^{N} v_{cpk})^2 \quad [2.17]$$

$$W_n = \frac{C}{2N}(\sum_{q=1}^{N} v_{cnq})^2 \quad [2.18]$$

By substituting Eq. [2.13] and [2.14] into [2.17] and [2.18] the sum capacitor voltage in each arm is,

$$\frac{C}{2Ni_p}\frac{d(\sum_{k=1}^{N} v_{cpk})^2}{dt} = v_{cp} \quad [2.19]$$

$$\frac{C}{2Ni_n}\frac{d(\sum_{q=1}^{N} v_{cnq})^2}{dt} = v_{cn} \quad [2.20]$$

2.4 Pulse Width Modulation of the Modular Multilevel Converter

There are three main categories for PWM in high switching frequency applications [10], namely 1)Phase-Shifted PWM (PSPWM) 2) Level-Shifted PWM (LSPWM) and 3) Space Vector PWM (SVPWM). They can be implemented in many different ways, but the main concepts are explained here.

2.4.1 Phase-Shifted Pulse Width Modulation

The phase-shifted PWM, also called the Sub-harmonic PWM, has an advantageous low harmonic distortion in the AC voltage and current [2]. There is one triangular carrier per SM which is compared to a sinusoidal reference waveform, and the carriers are shifted 360°/N in phase [10]. One module in the upper arm and one module in the lower arm will have a carrier with the same phase. According to [11], this method is the best for the MMC.

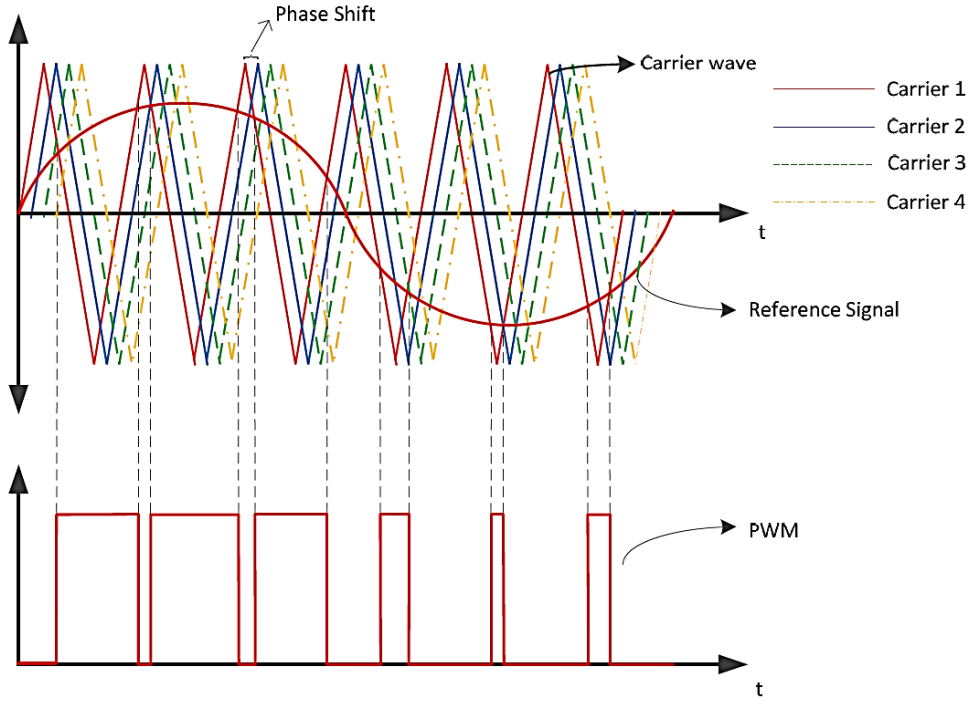

Figure 2-6 Phase-Shift Pulse Width Modulation for MMC [12]

2.4.2 Level-Shifted Pulse Width Modulation

The level shifted PWM is also called the Carrier disposition PWM [2]. One carrier per SM is required to control the pair of IGBT's [12]. The carriers have an amplitude of 1/N and can be arranged in mainly three ways; the phase disposition, the phase opposition disposition and the alternate phase opposition disposition. The different ways of arranging the carriers are presented in Figure 2-7.

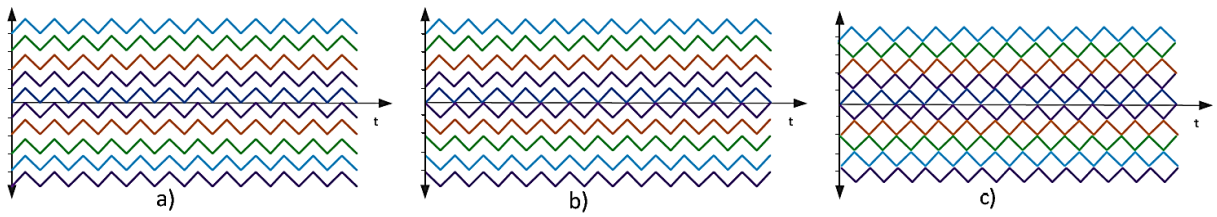

Figure 2-7 LSPWM. (a) Phase Disposition (b) Phase Opposition Disposition (c) Alternate Phase Opposition Disposition [12].

2.4.3 Space Vector Pulse Width Modulation

The space vector PWM is a well proven technique [12] and some modified techniques are also published [13]. In Figure 2-8 the voltage vectors are visualized. Each point in the figure represents a possible state for the converter, where N is the number of possible voltage levels.

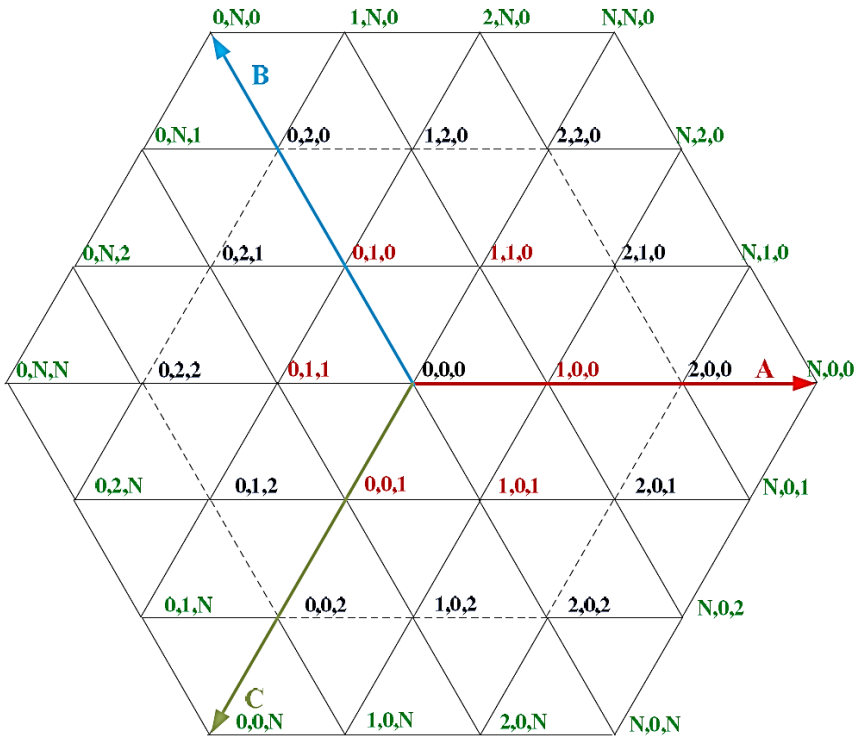

Figure 2-8 Space-Vector Pulse Width Modulation [12]

The multilevel space vector PWM is derived from the two level version where the reference voltage is decomposed into three vectors [14]

$$U_{ref}T_s = U_1T_1 + U_2T_2 + U_33 \quad [2.21]$$

$$T_1 + T_2 + T_3 = T_s \quad [2.22]$$

where U_{ref} is the voltage reference value, T_s is the period, $U_{1,2,3}$ is the partial voltages and $T_{1,2,3}$ is the partial time periods. For a five level converter, the method is visualized in Figure 2-9. This way of implementing the space vector modulation is not easily transferred to converters with many voltage levels. In [14] a new and better way for a large amount of voltage levels can be found.

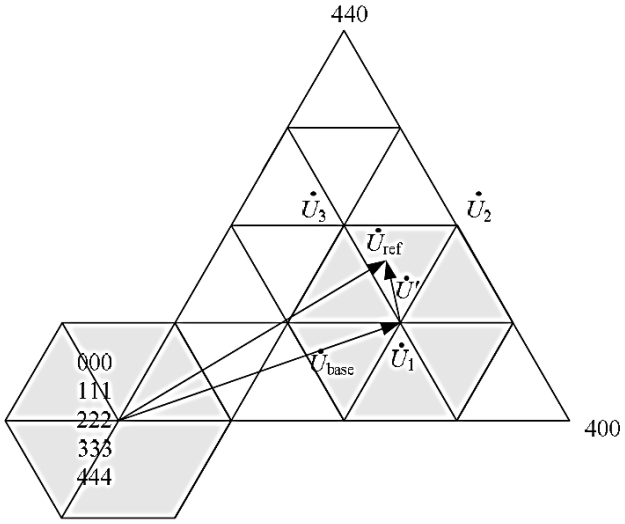

Figure 2-9 Conventional Reference Voltage Decomposition Based SVPWM [14].

2.5 Control of the Modular Multilevel Converter

The control of the MMC can be divided into [2];

- Basic VSC control: (1) Active power, and (2) Reactive power or AC voltage;
- DC link voltage control
- SM capacitor voltage control: (1) Overall control (average value=1 p.u.) and (2) Balancing (among every SM)
- Current control: (1) Circulating current eliminating and (2) Zero sequence current eliminating.

The MMC requires an active and reactive power control equal to conventional two-level VSCs. In order to control the power a conventional dq control could be used. The AC voltage should be controlled to a reference value so that the converter meets the demand.

The capacitor voltage is regulated based on the energy stored in the capacitors. If the voltage in the capacitors is too high, the amount of energy out of the converter should become higher than the amount of energy transferred in to the converter. This will reduce the stored energy in the capacitors and hence lower the capacitor voltage. Balancing the capacitor voltages can be done in several different ways, but the method described in [2] is implemented for the control in this project. In [2] there are three requirements that should be met to obtain balanced voltages. First, they should be balanced within each arm. Second, they should be balanced within each phase and third, they should be balanced among the phases. The voltage balancing method implemented in the simulation model and the physical setup is described in section 4.1.1.2.

Ideally, the upper and lower arm will contribute with half of the output current each. For a three phase converter, the zero-sequence current component will then be eliminated. The DC

current components should be kept equally distributed in the different phases if there is no voltage deviation between the phases. A circulating current control should also be included.

Chapter 3 Fault Tolerance by Reference Modification

Introduction

First, the main aspects of fault tolerant control are described in 3.1. The relevant vocabulary is presented and defined. In 3.2, a mathematical evaluation of the new method is presented. The advantages and disadvantages based on the theoretical description are also included here. The procedure to investigate the feasibility of the method can be found in 3.3. The procedure drawbacks are identified and discussed.

3.1 Fault Tolerance

A fault tolerant system can continue operation even when a fault is present. The power system is based on balanced three-phase circuits [15]. It is therefore crucial to obtain this condition after a fault. The definition for this condition is three sinusoidal voltages that have the same amplitude, but are displaced in phase by 120 degrees. Dependent on how the load is connected, this must be true for either phase voltages, line-line voltages or both. This chapter aim is to define the requirements for fault tolerant control, introduce a theoretical presentation and evaluation of the new method and identify the procedure to investigate the feasibility of the method.

A Fault Tolerant Control system (FTC) should accommodate component failures automatically [16]. It should therefore be a closed-loop control system which continues to operate according to the system requirements in the case of component malfunction. There are generally two types of FTCs systems; passive and active [16]. The Passive Fault Tolerant Control Systems (PFTCS) are designed in a way that makes them robust against certain faults that are known to occur. The Active Fault Tolerant Control Systems (AFTCS) react if a fault has occurred and reconfigure the control system, the circuit, or both, to continue to operate according to requirements. The PFTCS has limited fault-tolerant capabilities compared to the AFTCS. An overview of different AFTCS is given in [16]. Normally several different FTCs would be used in combination to achieve the best performance.

A proper FTC requires an effective Fault Detection and Diagnosis system (FDD) [16]. A FDD consists of a fault detection which is followed by fault isolation and identification. FFDs can be classified into two main categories; Model-based methods and Data-based methods (model-free). An FDD will trace back the cause and effect relations from the values that differ from the nominal. When the cause of change is found, the faulty part is properly diagnosed [17].

In literature, FDD for multilevel converters can be done in different ways [18, 19]. FTC for MMC has been solved traditionally by adding redundancy SMs or reducing the amount of voltage levels [20, 21].

3.2 Mathematical Description of the Reference Modification Method

The principle behind the Reference Modification Method (RMM) is to reconfigure the reference waveforms after a bypass of one or several SMs. An almost similar procedure can be found in [22]. The goal is to obtain balanced voltages with a component failure present. The loss of one SM in one arm will lead to loss of one voltage level. Each phase is coupled in parallel with the input DC link, so the sum of the capacitor voltages in one leg remains the same. For example, if one SM is bypassed in the upper arm of phase A, the voltage across the capacitors in this arm will increase because of this parallel coupling. This is avoided by modifying the reference waveform. The other arm in the same phase will have a new minimum voltage across it, in the ideal case, equal to

$$V_{A,new,min} = V_{dc} - \frac{V_{dc}}{N} \quad [3.1]$$

where V_{dc} is the input DC link and N is the amount of SMs per arm. To compensate for the reduced peak voltage in phase A, the references for phase B and C are lowered in this period, to obtain the same line to line voltages as the pre-fault state. The modification period is dependent on the number of SMs. Lower amount of SMs per arm, leads to larger modification area. The phase angles for the compensation period span from α_1 to α_2, and can be calculated like presented in Eq.[3.2]-[3.6]

$$V_{dc}sin(\alpha) = V_{dc} - \frac{V_{dc}}{N} \quad [3.2]$$

$$sin(\alpha) = 1 - \frac{1}{N} \quad [3.3]$$

$$\alpha = arcsin(1 - \frac{1}{N}) \quad [3.4]$$

Since the fault is in the upper arm:

$$\alpha_1 = arcsin\left(1 - \frac{1}{N}\right) + \pi \quad [3.5]$$

$$\alpha_2 = 2\pi - arcsin\left(1 - \frac{1}{N}\right) \quad [3.6]$$

Between α_1 and α_2, the reference value is fixed at $V_{A,new,min}$. To keep the line to line voltages equal to pre-fault condition, the phase to ground voltages for phase B and C have to increase by the same amount in the same time period. The new references for phase B and C is

$$V_B = V_{dc}\, sin\left(\alpha - \frac{2\pi}{3}\right) + (V_{A,pf} - \frac{V_{dc}(N-1)}{N}) \quad [3.7]$$

$$V_C = V_{dc}\, sin\left(\alpha + \frac{2\pi}{3}\right) + (V_{A,pf} - \frac{V_{dc}(N-1)}{N}) \quad [3.8]$$

The line to line voltages will then be

$$V_{AB} = (V_{dc} - \frac{V_{dc}}{N}) - V_{dc}\, sin\left(\alpha - \frac{2\pi}{3}\right) - (V_{A,pf} - \frac{V_{dc}(N-1)}{N}) \quad [3.9]$$

which is equal to

$$V_{AB} = V_{A,pf} - V_{dc}\, sin\left(\alpha - \frac{2\pi}{3}\right) \quad [3.10]$$

$$V_{BC} = V_{dc}\, sin\left(\alpha - \frac{2\pi}{3}\right) + V_{A,pf} + \frac{V_{dc}(N-1)}{N} - V_{dc}\, sin\left(\alpha + \frac{2\pi}{3}\right) - V_{A,pf} - \frac{V_{dc}(N-1)}{N} \quad [3.11]$$

which is equal to

$$V_{BC} = V_{dc}\, sin\left(\alpha - \frac{2\pi}{3}\right) - V_{dc}\, sin\left(\alpha + \frac{2\pi}{3}\right) \quad [3.12]$$

$$V_{BC} = V_{dc}\, sin\left(\alpha + \frac{2\pi}{3}\right) + V_{A,pf} - \frac{V_{dc}(N-1)}{N} - V_{dc}\, sin\left(\alpha - \frac{2\pi}{3}\right) - V_{A,pf} + \frac{V_{dc}(N-1)}{N} \quad [3.13]$$

which is equal to

$$V_{BC} = V_{dc}\, sin\left(\alpha + \frac{2\pi}{3}\right) - V_{dc}\, sin\left(\alpha - \frac{2\pi}{3}\right) \quad [3.14]$$

where $V_{A,pf}$ is the phase A voltage output in pre-fault condition. It can be seen that the line to line voltages remain the same as in the pre-fault condition. Figure 3-1 shows the neutral point deviation caused by the reference modification. Naf is the Neutral point after fault, and Npf is the neutral point pre fault. It can be seen that the phase A voltage value will decrease, but the line to line voltages remains the same. The effect of the reference modification depends on the relation between the neutral point in the load contra the neutral point of the DC-link. In case of a neutral point in the load which is not connected to the neutral point in the DC-link, the deviation in the phase A voltage might be absorbed by the neutral point voltage fluctuations.

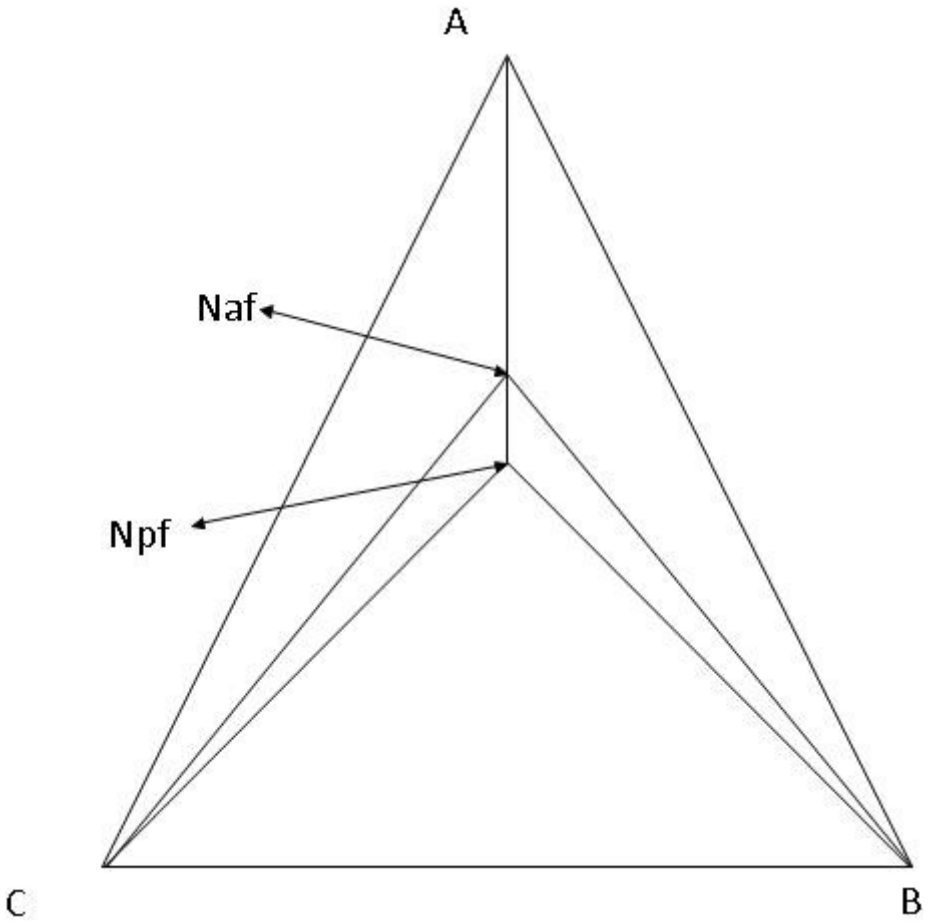

Figure 3-1 Neutral Point Deviation

3.3 Procedure to Investigate the Feasibility of the Reference Modification Method

In this report one method of FTC is investigated, It is assumed that the fault is properly diagnosed. It is also assumed that the faulty SM is quickly bypassed and that no components are damaged by the fault. To limit the scope of the project, only the case where the load neutral point is not connected to ground is investigated.

According to [23], an important feature of the MMC is that there is no need for low inductive bus bars in the topology. The SMs can therefore be connected with ordinary cables which are cost efficient and important for fault tolerant behavior. The relatively high stray inductance enables the central control to react on any fault condition in time. Secondary faults can then be prevented by shunting the faulted SM, and the arm can continue operating with one voltage level less.

In order to investigate the RMM, one simulation model of the MMC topology should be made. To isolate the effect of the reference modification on the line voltages, a constant DC-link and a constant passive load is assumed. First the reference waveforms after the modification should be analyzed. Important aspects in analyzing the results;

- can the SMs produce the modified waveform in all phases
- does the amount of SMs in the converter impact the feasibility as discussed in 3.2
- is the deviation from steady state satisfactory

If the computer simulation shows that the RMM could be viable, it should be tested on a prototype. When testing on a physical setup there are many possible sources of error. To ensure that the setup is controlled as intended, a detailed analysis of the control signals sent and their impact on the setup should be performed. This analysis should be completed for the steady state results before implementing the RMM on the setup, and later repeated for the fault tolerant state. The same control algorithm used for the simulation model is planned implemented on the physical setup if applicable. It is although assumed that some changes will be made to be able to run it in real-time. These changes could potentially affect the control signals impact on the setup compared to the simulation model.

To complete the investigation of the RMM, the simulation and hardware results should be compared. The comparison should be based on Fourier analysis and the shape of the current and voltage waveforms in all phases. Some of the simplifications and assumptions made in the computer simulation might be incorrect. The steady and fault tolerant state results for the simulation model should be compared to investigate these results isolated. This comparison should also be made for the hardware results. The deviation between these two analyses should be identified.

Chapter 4

Simulation Model of the MMC

Introduction

This chapter describes the simulation model that will be used in this report. First in 4.1, the model parameters, control and modulation in steady and fault tolerant state will be presented. In 4.2, the capacitor charging scheme used for the simulation model is presented. In order to avoid high charging currents, the capacitors should be charged prior to operation. In 4.3 and 4.4, the simulation results from steady state and FTC operation are shown.

4.1 Simulation Model Presentation

The model was built in Simulink and SimPowerSystems, a toolbox within the Simulink software used to model power circuits. Voltage and current measurements needed for the control is measured by SimPowerSystems blocks to interface with the Simulink block set. The model has the same topology as described in Chapter 2 and an overview is shown in Figure 4-1. Throughout this chapter, the labels presented in this overview will be used. The model parameters can be seen in Table 4-1.

The input DC-link is set to 250V leading to mean capacitor voltages of approximately 50V. The phase load is 40mH and 27.4 Ω, and the arm modulation index is 0.9. The triangular carrier has a frequency of 2100Hz, and the fundamental frequency is 50Hz. A resistor of 47kΩ is coupled in parallel with each SM capacitor to increase the time constant which can be approximated by

$$\tau \cong RC \cong 155s \qquad [4.1]$$

where R is the parallel resistance and C is the SM capacitance.

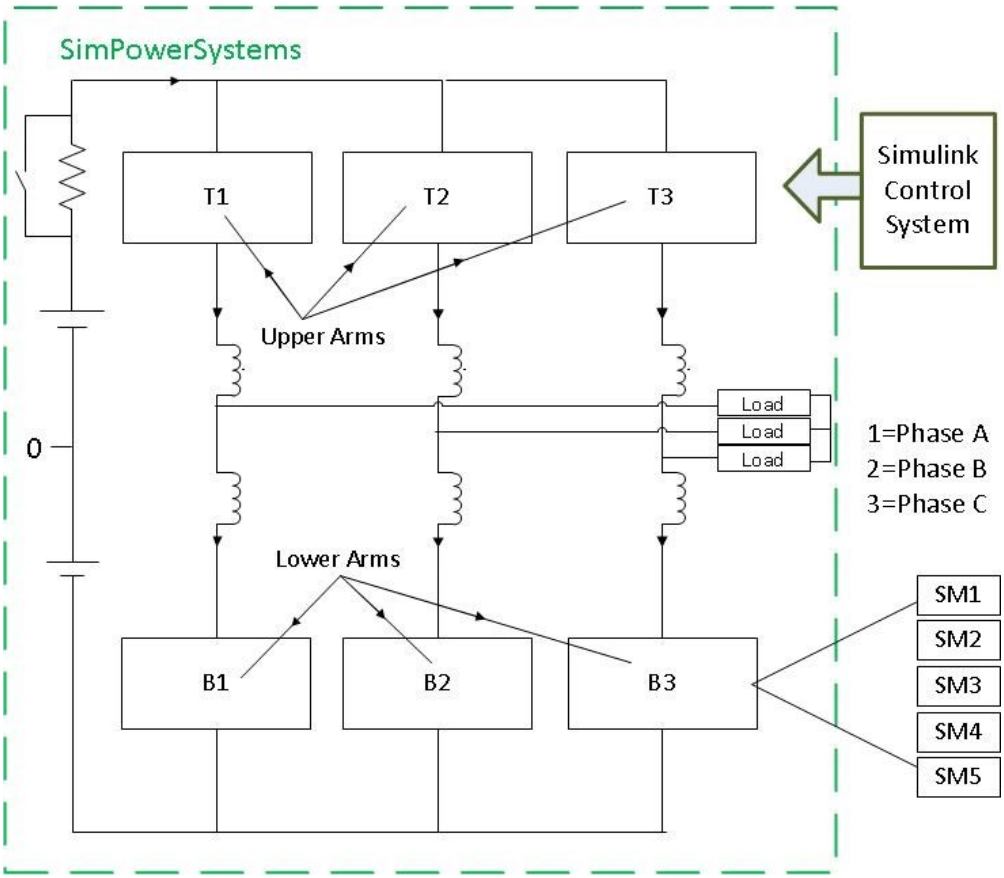

Figure 4-1 Overview, Simulation Model

Table 4-1 Simulation Parameters

PARAMETER	VALUE
Vdc	250V
R charge	68 Ω
Arm Inductance	1.2mH
Arm Resistance	1Ω
SM Capacitor	3.3mF
Capacitor Parallel Resistor	47kΩ
Load L	40mH
Load R	27.4Ω
Carrier Frequency	2100Hz
Fundamental Frequency	50Hz
Arm Modulation Index	0.95 and 0.9
Time Step	5μs

4.1.1 Control and modulation in the Simulation Model

A constant DC-link voltage and load are assumed. The reference waveforms are produced based on these constant values and no further control is included. In this section, the modulation method and capacitor voltage balancing for the simulation model will be presented. The reference waveforms for both steady state and fault tolerant state are included. The initial time step choices and verification of the model is based on [24].

4.1.1.1 Level-Shifted Pulse Width Modulation

The basic of the level-shifted PWM (LSPWM) is presented in chapter 2.4.1, and will here be described in detail for the simulation model. The advantage of using the LSPWM is that some of the harmonic components from the upper and lower arms cancel each other [25]. To obtain this, it is important to sample the reference waveform twice in each triangular carrier period to ensure synchronous switching of the modules. The reference waveforms are compared each peak and base of the triangular carrier. The phase voltage waveform consists of harmonics of the triangular carrier frequency sidebands and its multiples.

The reference waveforms are sinusoidal with an added DC-offset, and can be seen in Figure 4-2. The DC-offset is added due to the operation principle of the MMC which is explained in 2.2 and by KVL described in Eq. [1-2]. In Eq. [4.2] and [4.3], the arm inductance is neglected and v_{cp} is the upper arm reference, v_{cn} is the lower arm reference, and v_{a0} is the point where the phase load is connected.

$$\frac{V_{dc}}{2} - v_{a0} = v_{cp} \quad \textbf{[4.2]}$$

$$v_{a0} - \frac{V_{dc}}{2} = v_{cn} \quad [4.3]$$

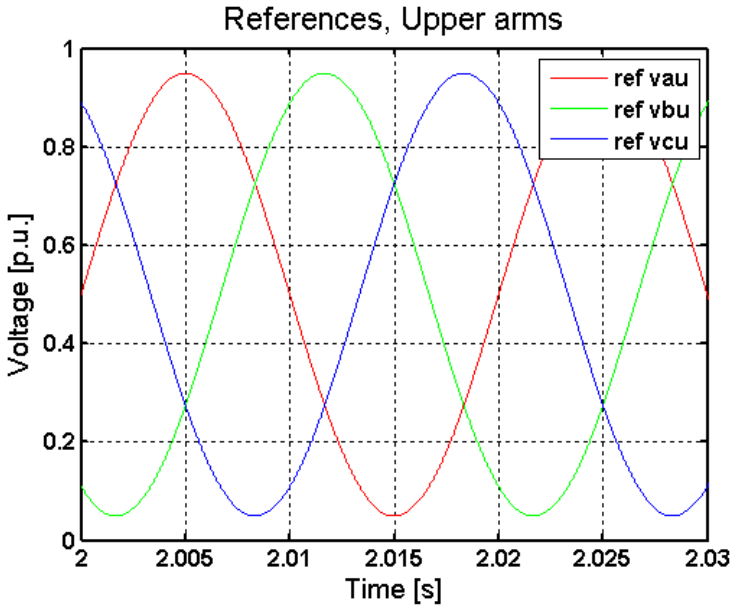

Figure 4-2 Arm References, Upper Arms

The Reference Modification Method (RMM) reference waveforms can be seen in Figure 4-3. The voltages in phase B and C are lowered in the time period where phase A can no longer deliver the pre-fault values. The amount of SMs in the circuit greatly influences the ability to use this technique. This can best be illustrated by Figure 4-4, where the modulation index is set to 0.95. Because of the low amount of SMs, phase B and C can not be lowered enough to compensate for the fault in phase A. If the amount of SMs were higher, the compensation period becomes smaller. This is very beneficial. The minimum points for phase B and C may then be outside of the compensation period and the possible voltage compensation in these phases becomes significantly larger. Based on these results, it is assumed that the amount of bypassed SMs that can be compensated for with this method is lower than 33 % of the total amount of SMs in the converter. This percentage yields for bypassed SMs in the same arm. If a larger amount is bypassed, the modulation index could be lowered in order to increase the redundancy in the circuit.

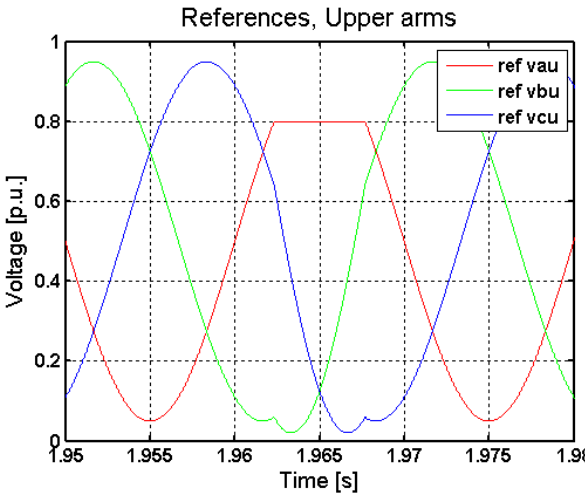

Figure 4-3 References, Upper Arms, RMM, M=0.9

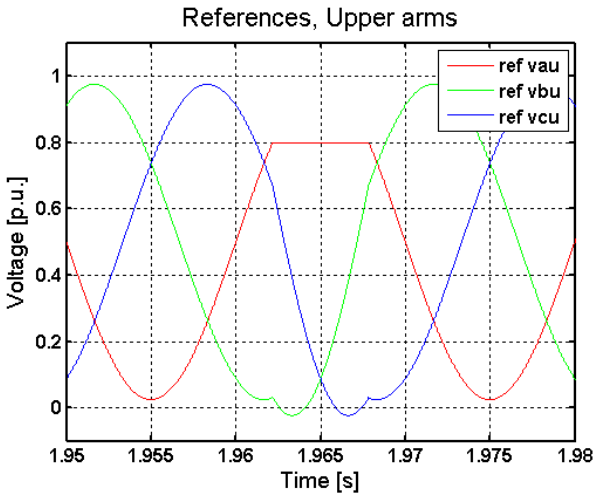

Figure 4-4 References, Upper Arms, RMM, M=0.95

These ideal waveforms are then compared to a triangular carrier to generate the PWM signals. With this method, only one triangular carrier is required. The operation of the SMs is described, in Table 4-2, for a converter with five SMs in each arm. ON means capacitor inserted in the circuit, and OFF means capacitor bypassed.

Table 4-2 Shift of Modulating Waveform and its Effect on SMs [25].

Magnitude of modulating wave	Level shift required	Number of SM ON	Number of SM OFF	Number of SM for PWM
0 to 1/5	0	0	5	1
1/5 to 2/5	1/5	1	4	1
2/5 to 3/5	2/5	2	3	1
3/5 to 4/5	3/5	3	2	1
4/5 to 1	4/5	4	1	1

The modulating waveform is shifted in magnitude, and scaled to fit the carrier of magnitude 1/n. For a converter with five SMs per arm, the magnitude becomes 1/5. As the modulating waveforms vary, the SMs are switched accordingly. One SM is used for PWM and the others are either fully OFF or fully ON.

When the sinusoidal signals have been produced, a common mode voltage could be added to each reference wave [25]. This addition would increase the utilization of the DC-link. The common mode voltage has half of the magnitude of the waveform that at any instant is in the middle of the three reference waves. The reference waves for the upper arm can be seen in Figure 4-5 where N equals four. However, due to the scope of this thesis, the common mode voltage will not be implemented in the model.

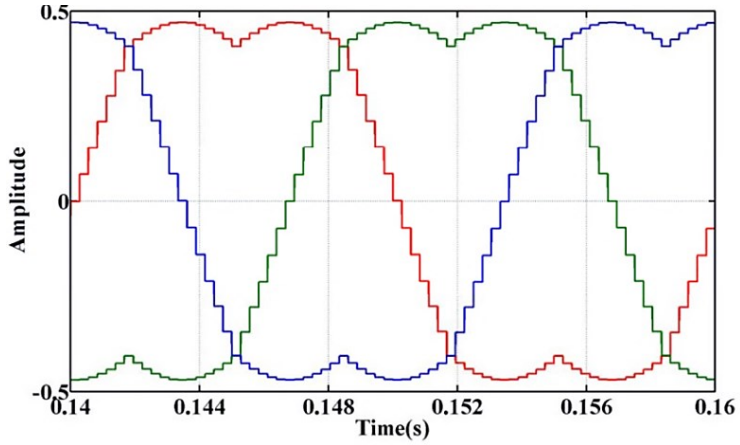

Figure 4-5 Reference Waveforms Level-Shifted Pulse Width Modulation [25]

4.1.1.2 Control of Capacitor Voltages

The arguments behind the need for of capacitor voltage balancing is presented in chapter 0 and the method implemented in this simulation model is based on [26] and presented here. The capacitor voltages are measured in order to apply the balancing algorithm. Then they are sorted by value to decide which SM should be switched ON, which should be switched OFF and which should be used for the PWM to maintain the voltages within a certain range.

For positive current, the capacitor charges if the SM is inserted in the circuit. Therefore, the SM with the lowest capacitor voltage should be switched ON, and vice versa. In Figure 4-6 and Figure 4-7, the capacitor voltage ripples are shown. It can be seen that the capacitor voltages in the simulation model are balanced. They oscillate around 50V for both steady state and fault tolerant state when the RMM is implemented.

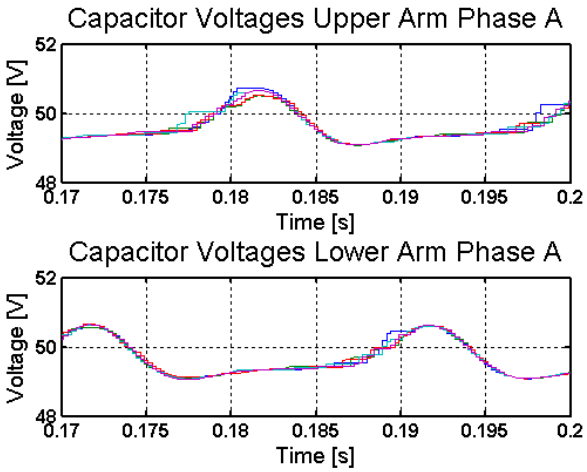

Figure 4-6 Capacitor Voltages, Phase A, Steady State

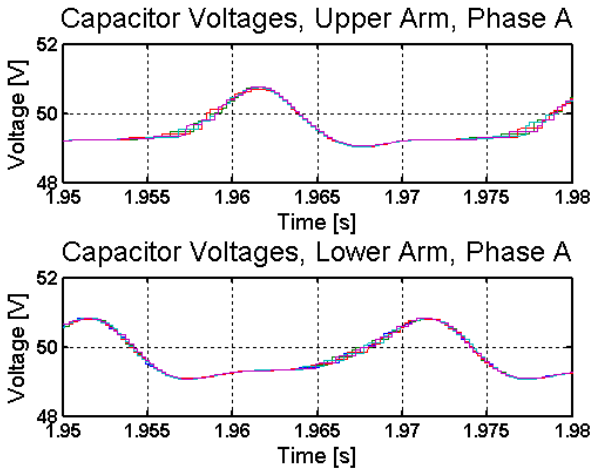

Figure 4-7 Capacitor Voltages, Phase A, RMM

4.2 Method for Charging and Discharging the Capacitors

The capacitors in the test setup must be energized before the modulating algorithm can be run. If it is started without charging the capacitors, the initial currents will be very high. In a simulation model, the capacitors can be set to an initial voltage value. In order to obtain more realistic results, a capacitor charging mechanism is added. It is also implemented as a safety precaution; to test the charging algorithm digitally before implementing it to hardware. The method used in this case is based on [27]. The upper arms and the lower arms are charged separately. In addition, a resistance for limiting the charging current is coupled into the circuit while charging. The charging speed is decided by the limiting resistance. When the charging scheme is complete, the resistance is short circuited. If the MMC was coupled to the grid, the capacitors could be charged from the AC side [28].To be able to charge the upper and lower capacitors separately, the following steps are performed:

1. Couple in the charging resistance
2. Couple in all capacitors in the upper arms
3. Start the simulation
4. When the upper arms capacitors have reached the set value, all the capacitors in the upper arms are coupled out of the circuit
5. All the lower arm capacitors are coupled into the circuit
6. When the lower arms capacitors have reached the set value, they are coupled out of the circuit
7. Optional: recharge the upper arms capacitors.
8. Couple the charging resistance out of the circuit.
9. Start normal mode

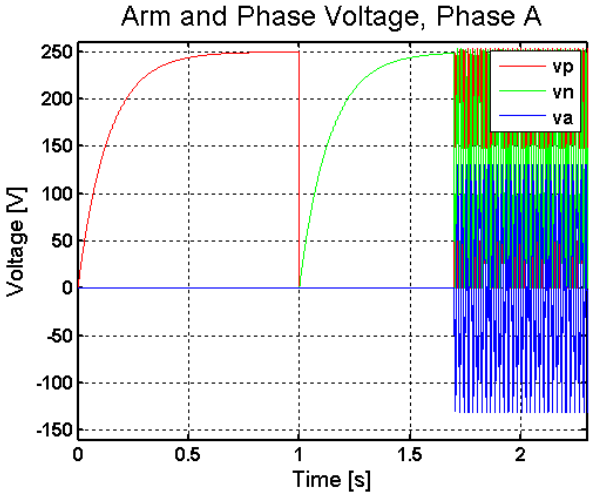

Figure 4-8 Arm and Phase Voltages in Phase A, Capacitor Charging

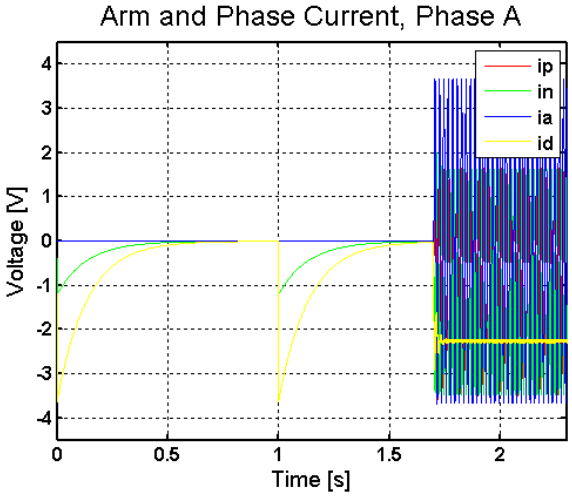

Figure 4-9 Arm and Phase Currents in Phase A, Capacitor Charging

In Figure 4-8 and Figure 4-9, it can be seen that the capacitors are charged in the manner described above. The graphs show vp, ip and vn, in which is upper and lower arm voltages and currents in addition to the phase voltage and current, va and ia. The upper and lower arm

currents are exactly equal because of the defined polarities given in Figure 2-5. The transition between charging mode and steady state is good and can be seen in Figure 4-10. The currents are all zero before the transition because the capacitors are fully charged.

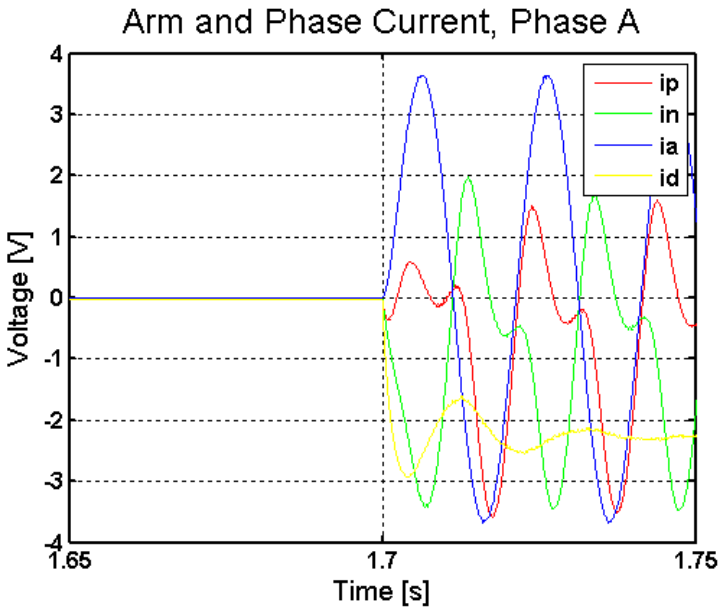

Figure 4-10 Arm and Phase Currents in Phase A, Transition to Steady State

4.3 Simulation Results Steady State

The steady state simulation results will be presented in this section. These results will further be compared with the results from the hardware setup in Chapter 6. The measured voltages and currents will be presented and the main results from Fourier analysis is shown.

4.3.1 Voltages in Steady State

The phase and line voltages can be seen in Figure 4-11. They seem balanced, and have the expected magnitude relations,

$$V_{Apeak} \sim \frac{V_{dc}}{2} \sim 125V. \,\&\, V_{ARMS} \sim 88V. \quad [4.4]$$

$$V_{ABpeak} \sim \frac{V_{dc}}{2}\sqrt{3} \sim 216V. \,\&\, V_{ABRMS} \sim 153V. \quad [4.5]$$

The Discrete Fourier block in Simulink is used to compute the fundamental frequency components for the steady state voltages, and the result can be seen in Table 4-3. The voltage magnitude are equal, and the phase shift is 120° for all phases and line to line voltages.

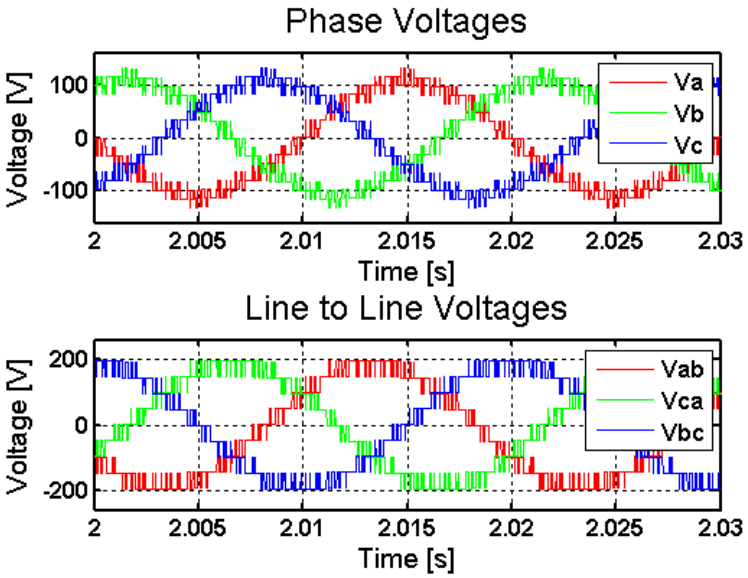

Figure 4-11 Phase and Line-Line Voltages, All Phases

Table 4-3 Fourier Analysis, Fundamental Frequency, Steady State

PARAMETER	PHASE A	PHASE B	PHASE C	LINE AB	LINE CA	LINE BC
Magnitude[V]	110	110	110	190	190	190
Phase Angle [°]	-179	61	-59	-149	-29	91
Phase Shift[°]	**A-B**	**B-C**	**C-A**	**AB-BC**	**BC-CA**	**CA-AB**
	120	120	120	120	120	120

In order to investigate if the modulation is working as intended, an overview of the harmonic spectrum is presented in Figure 4-12. The spectrum is dominated by the sidebands of the triangular frequency and its multiples as expected.

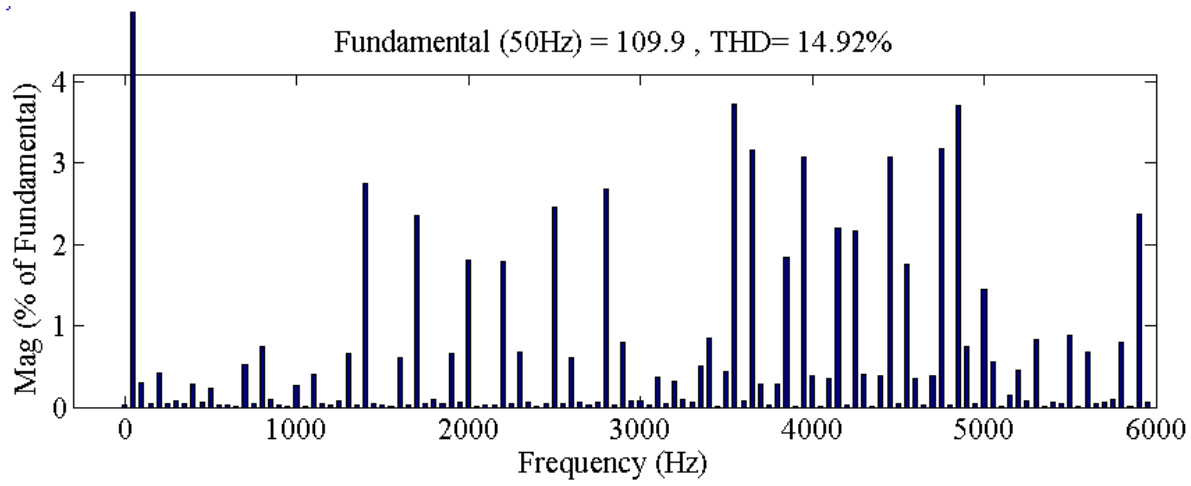

Figure 4-12 Fourier Analysis of Phase A Voltage, Steady State

In Figure 4-13, the upper(p) and lower arm(n) voltages in phase A are presented. The arm voltages have clearly five levels and are 180 degrees shifted with respect to each other. It can also be seen that the capacitor voltage ripple lead to a small change in the voltage, particularly in the peak arm voltage values. Figure 4-14 shows that the arm voltage follows the reference value.

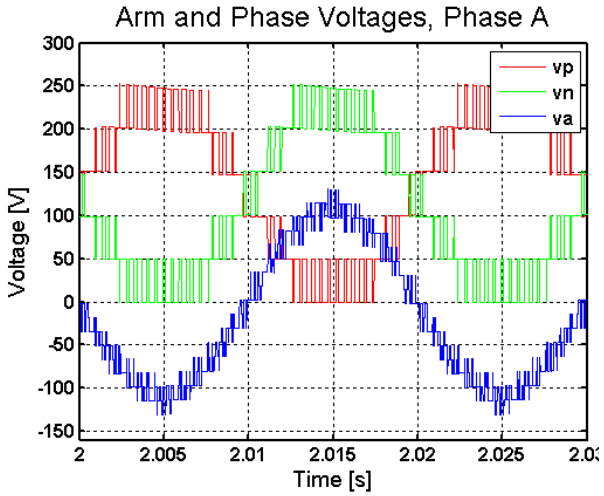

Figure 4-13 Arm and Phase Voltages, Phase A, Simulation Model

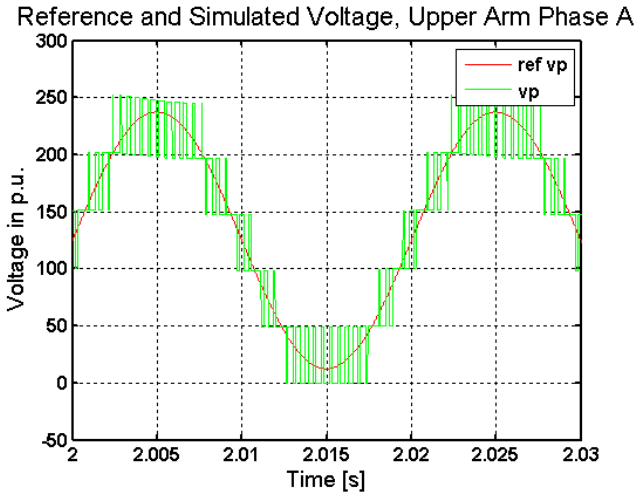

Figure 4-14 Arm Voltage and Reference Waveform, Upper Arm Phase A

4.3.2 Currents in Steady State

The phase currents are presented in Figure 4-15. They have equal magnitudes and the phase is shifted 120° for the fundamental component, see Table 4-4 for the fundamental frequency Fourier analysis. The arm and phase A currents can be seen in Figure 4-16. The second harmonic contribution from the circulating current is clearly present in the arm currents. This does not affect the output phase current; see the mathematical model in chapter 2.3.

Table 4-4 Fourier Analysis, Phase Currents, Fundamental Frequency, Steady State, Simulation Model

PARAMETER	PHASE A	PHASE B	PHASE C
Magnitude [A]	3.65	3.65	3.65
Phase Angle [°]	-23.8	-143.8	96.2
Phase Shift[°]	**A-B**	**B-C**	**C-A**
	120	120	120

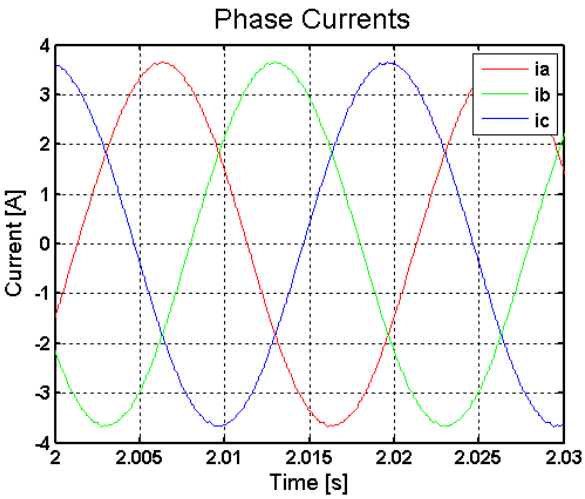

Figure 4-15 Phase Currents, Steady State, Simulation Model

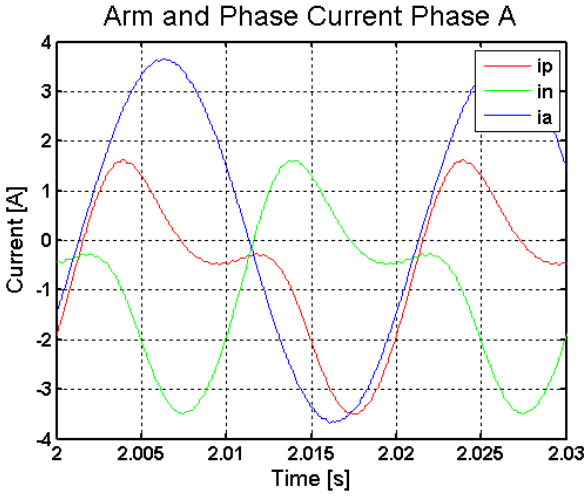

Figure 4-16 Arm and Phase Currents, Phase A, Steady State, Simulation Model

4.4 Simulation Results Fault Tolerant State

In this section, the circuit behavior after SM1 in T1 is bypassed will be investigated. The faulty system without RMM can be seen in Figure 4-17. The phase A waveform is distorted, and this distortion can also be seen in the line-line voltages. The Fourier analysis Is presented in Table 4-5, and it is clear that the voltages are unbalanced. The aim is to balance the voltages with RMM, and the results with this method are presented in the following sections. First the voltage measurements are presented, followed by the current measurements.

Table 4-5 Fourier Analysis, Fundamental Frequency, Fault, No RMM

PARAMETER	PHASE A	PHASE B	PHASE C	LINE AB	LINE CA	LINE BC
Magnitude[V]	114.9	116.0	106.1	205.0	188.4	190.3
Phase Angle [°]	-173.4	61.3	-56.5	-145.9	-23.6	90.9
Phase Shift[°]	**A-B**	**B-C**	**C-A**	**AB-BC**	**BC-CA**	**CA-AB**
	125.3	117.8	116.9	123.2	114.5	122.3

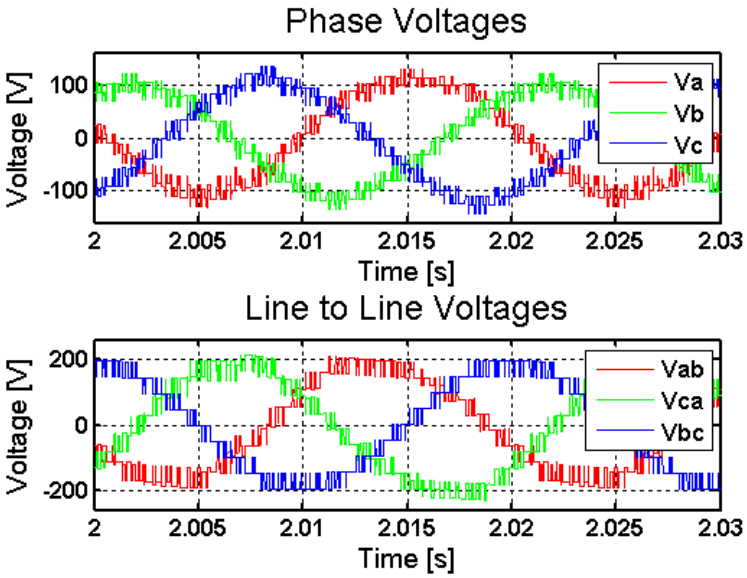

Figure 4-17 Phase and Line-Line Voltages, All Phases, One SM Bypassed, No RMM

4.4.1 Voltages in Fault Tolerant State

The voltage measurements obtained with the proposed RMM, see chapter 3.2, is implemented in the model. In Figure 4-18 the phase and line voltages is presented. There are some differences compared to the pre-fault condition. Firstly, it can be seen that in the compensated period, the PWM pattern in the graphs for phase A have a larger gap between each signal.

This is expected because the arm voltages in this period are constant, and the phase voltages are based on the arm voltages.

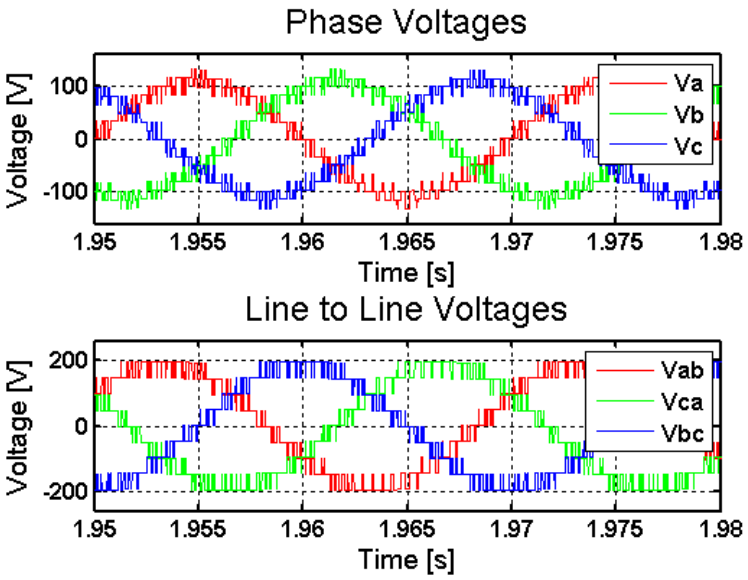

Figure 4-18 Phase and Line-Line Voltages, All Phases, RMM

As presented in 3.1, it is important to obtain balanced three-phase voltages. In order to investigate the obtained voltages, an FFT analysis of the fundamental frequency was performed. The results can be seen in Table 4-6 and Figure 4-19. The fundamental frequency components are balanced. The FTC has accomplished good results for both amplitudes and angles in all three phases for both angles and magnitudes. The graphs obtained by the Fourier analysis are included in Appendix 2.

Table 4-6 Fourier Analysis, Fundamental Frequency, RMM

PARAMETER	PHASE A	PHASE B	PHASE C	LINE AB	LINE CA	LINE BC
Magnitude[V]	110	110	110	190	190	190
Phase Angle [°]	-179.1	60.7	-59.1	-149.2	-29.0	90.8
Phase Shift[°]	A-B	B-C	C-A	AB-BC	BC-CA	CA-AB
	120.2	119.8	120	120.2	119.8	120

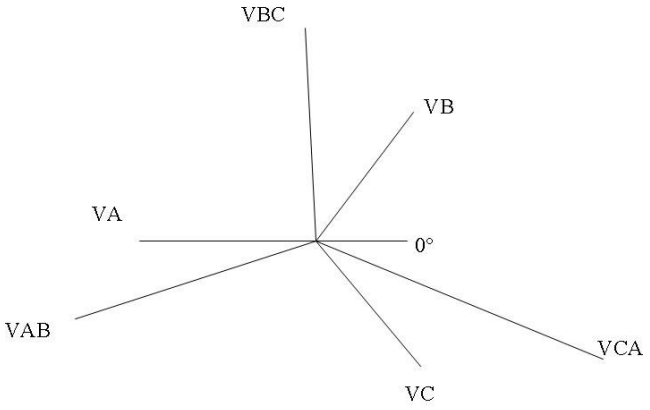

Figure 4-19 Three-Phase Angles, RMM

An overview of the harmonic spectrum for the output voltage in phase A can be seen in Figure 4-20. The figure shows that there are more harmonics in the fault tolerant state than for the steady state. Since the harmonic components have high frequencies, they can be filtered by a low pass filter. The harmonic spectrums for phase B and C can be found in Appendix 2. The harmonic components for these two phases stay below 1% of the fundamental component magnitude for frequencies below 1000Hz.

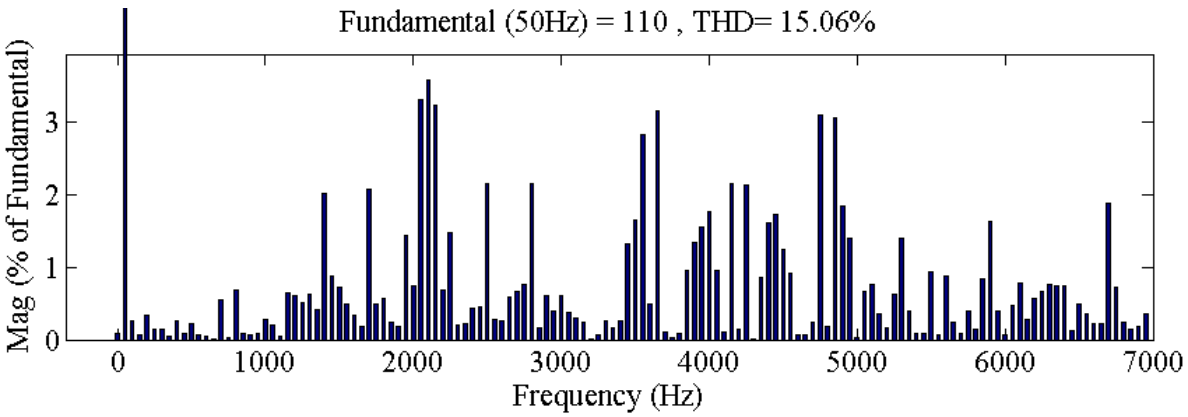

Figure 4-20 Fourier Analysis of phase A Voltage, RMM

The upper arm voltage in phase A will in this faulty condition only have four voltage levels and can be seen in Figure 4-21. This affects the lower arm voltage in phase A to also have four voltage levels. This is due to the input DC-link being parallel to the phase legs, see Eq. 3.

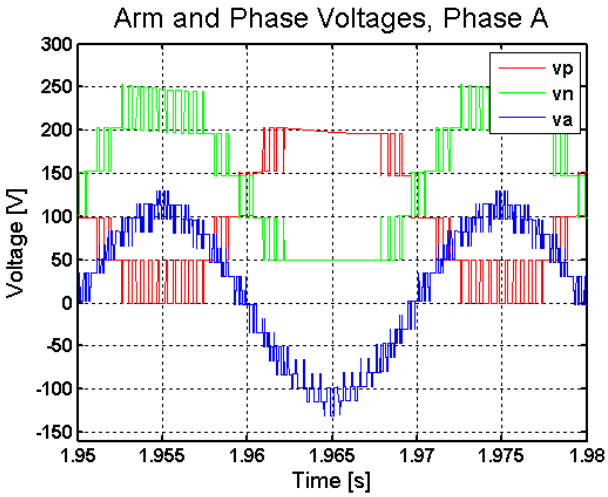

Figure 4-21 Arm and Phase Voltages, Phase A, RMM

In the simulated case, the load neutral point does not have the same potential as the DC-link neutral point. The difference in these two points is significant in the fault tolerant state, and can be seen in Figure 4-22. It is increased during the compensated periods, here around 1.965s.

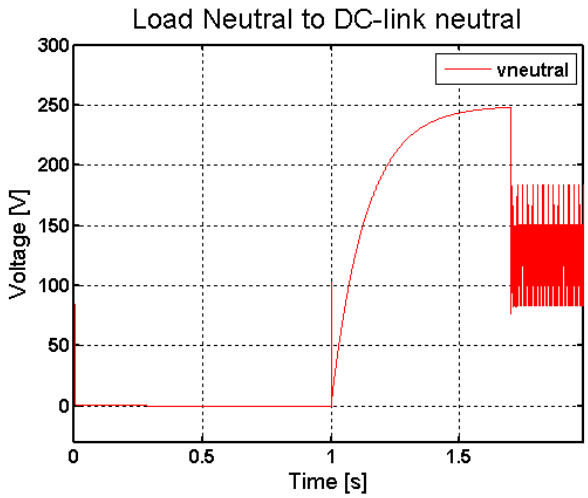

Figure 4-22 Load Neutral to DC-link Neutral, RMM

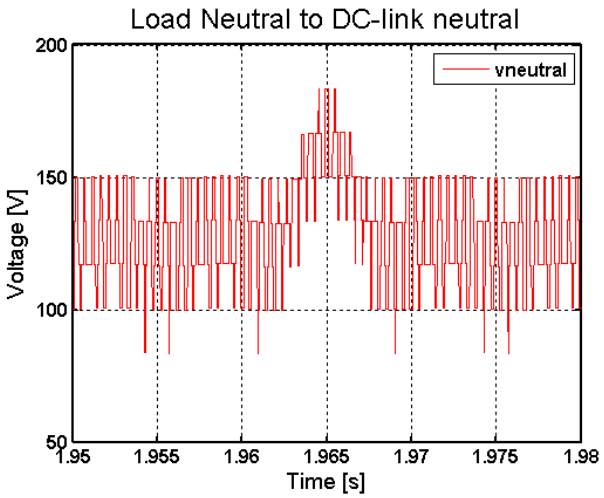

Figure 4-23 Load Neutral to DC-link Neutral, Detailed, RMM

4.4.2 Currents in Fault Tolerant State

Following are the current measurements results for the fault tolerant state. In Figure 4-24, the currents in all phases are presented. The Fourier analysis shows that the fundamental frequency amplitude for ic is 0.1A lower than for the two other phases. The phase shift range from 119.8° to 120.2°.

The currents in phase A can be seen in Figure 4-25. The arms currents are 180° phase shifted and have a large second order harmonic component similar to in steady state operation.

Table 4-7 Fourier Analysis, Phase Currents, Fundamental Frequency, Fault Tolerant, Simulation Model

PARAMETER	PHASE A	PHASE B	PHASE C
Magnitude [A]	3.65	3.65	3.64
Phase Angle [°]	-23.7	-143.9	96.3
Phase Shifts[°]	**A-B**	**B-C**	**C-A**
	120.2	119.8	120

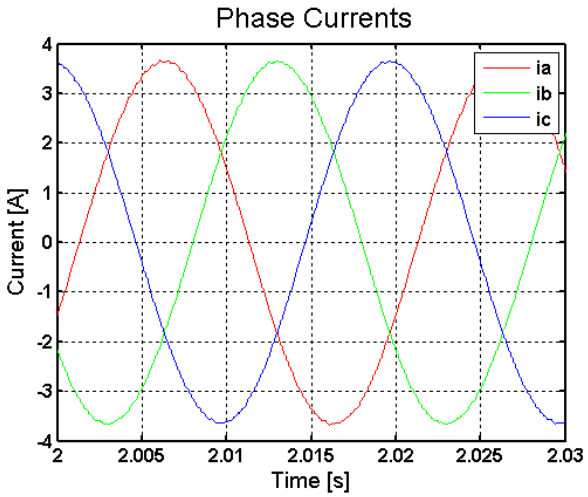

Figure 4-24 Phase Currents, RMM

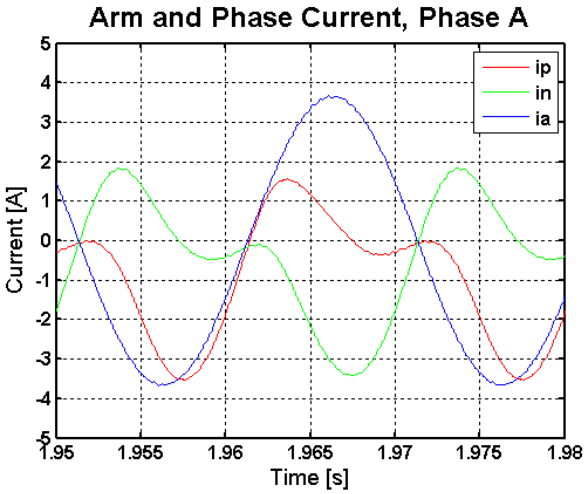

Figure 4-25 Arm and Phase Currents, Phase A, RMM

Chapter 5

Hardware Design and Tests

Introduction

In order to verify the simulation results in a physical setup, a prototype was built. In 5.1, an overview of the control connections and measurements will be presented. In subchapter 5.2, a further description of the control signals' path is included. The main circuit design is described in 5.3, followed by the hardware and software design considerations in 5.4 and 5.5. The control signals' behavior seen in ControlDesk is presented in 5.6. These are analyzed to ensure a proper operation in steady state, which results are described and discussed in 5.7. Last, the RMM results and analysis can be found in 5.8.

5.1 Hardware Design Overview

The setup was constructed with five SMs in each arm, but can easily be expanded to six. It has one input DC-link, a passive load and is controlled by dSPACE equipment. A graphical representation of the setup is shown in Figure 5-1. The notations presented in the overview will be used throughout this chapter.

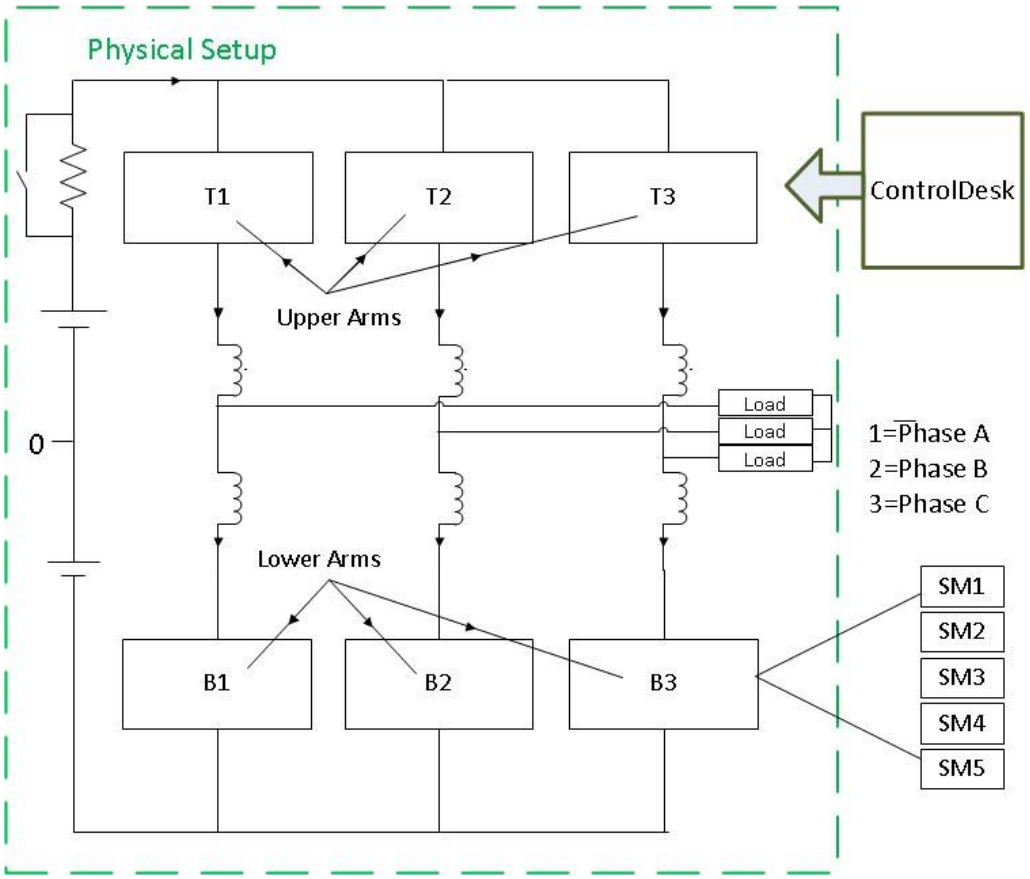

Figure 5-1 Hardware Overview

The hardware parameters are presented in Table 5-1. Most of the values are similar to the simulation model. The exceptions are the input DC-link when RMM is implemented, the load parameters which are 12.2Ω and 18.7mH and the time step which is 119.05µs. The DC-link is lowered for the FTC operation because of unexpected arm current peaks in the faulty phase. A mistake when adjusting the load parameters lead to the lower load impedance in the hardware setup than for the simulation model. The time limitations in this project caused the author to not run new tests with the planned impedance value. To compare the simulation and hardware results, the simulation fundamental frequency components was found with the same parameters as the hardware setup. These values can be found in chapter 6.1. The time step for the hardware control is set to 119.05µs because of the limited processor power for the dSPACE equipment. With this time step, the control signals are computed four times each triangular carrier period.

Table 5-1 Hardware Parameters

PARAMETER	VALUE
Vdc	250V/100V
R charge	68 Ω
Arm Inductance	1.2mH
Arm Resistance	1 Ω
SM Capacitor	3.3mF
Capacitor Parallel Resistor	47kΩ
Load L	18.7mH
Load R	12.2 Ω
Carrier Frequency	≅2100Hz
Fundamental Frequency	50Hz
Modulation Index	0.9
Time Step	119.05μs

Table 5-2 Hardware Components Identification

COMPONENT	ID
Multimeter Fluke 175	S03-0439
Oscilloscope Tektronix TDS 2014B	G04-0347
Differential Probes Tektronix P5200A	I06-0518, -0520, -0516
DC-link Voltage Source	R04-0161
Triaac REO	B01-0580
DC Power Supply GW Instek	B02-0460, -0459
Current measurement probes Fluke 180i 110s	104-0475, -0491, -0520, -0490, -0375, -0524, -0523, -0477
Host PC	P07-1342
Expansion Box dSPACE	P07-1987
Connector Panel dSPACE CLP1103	Borrowed from Narvik University & College.
Control Card DS1103	Borrowed from Narvik University & College.
Capacitors Kemet 400VDC	13350011
IGBTs Semikron	SKM100GB123D
Driver Interface Cards, Sintef	OFK HR 1345 HR
Gate Driver Cards Semikron	SKHI 23/12

COMPONENT	ID
Voltage Measurements Boards, NTNU	N/A
Current Measurement and arm inductors setup, NTNU	N/A
Resistive Load	K01-0146
Inductive Load	LR-9

5.2 Control Signals' Path

In order to control the IGBT switches, dSPACE control equipment was used. The interface between the dSPACE (DS1103) outputs and the IGBTs (SKM100GB123D) has several connections to ensure a safe and predictable operation. An overview of the control signals' path is presented in Figure 5-2. Each IGBT module requires four signals to operate the two transistors. A 15V gate signal will short circuit the transistor and -8V open the transistor. These signals are driven by the Gate Driver card (SKHI 23/12 R) which requires two control signals, one for each transistor. The signals to the Driver cards are 15V for short circuit and 0V for open circuit. These signals are supplied by the Gate Driver Interface cards (AN 13.12.xx).

Each interface card can drive three Gate Driver cards. It requires six inputs, two for each Driver Card. They have an implemented overrun logic for each pair of signals. This logic will automatically turn off (0V output) for the second output if the first output is positive (5V) This feature is exploited to limit the amount of signals sent from dSPACE. The second output in each pair is set to 5V continuously, and the first output controls whether the SM should be coupled in or out of the circuit. The Driver Interface cards have TTL (0-5V) inputs from the Distribution board (made by the workshop at NTNU). This board provides the continuous 5V signals, in addition to distribute the control signals sent by dSPACE. The cables from the distribution board to the gate driver interface cards are long, and the risk of interference is high. In the gate driver cards, a filter is included to reduce the effect of interference. If the converter is to be operated on high voltages, these cables should be shielded to avoid unpredictable operation.

The distribution board also provides the Enable signal required to operate the Interface cards. The interface cards have a built in protection against overvoltage and receives error signals from the Gate driver cards. If no error is present, they send an OK signal to the Distribution board. In the distribution board, a logic circuit is made to only send out the Enable signal if all 12 Interface cards send the OK signal. This way, the IGBTs will not switch if there exists an error signal in one of the Interface cards.

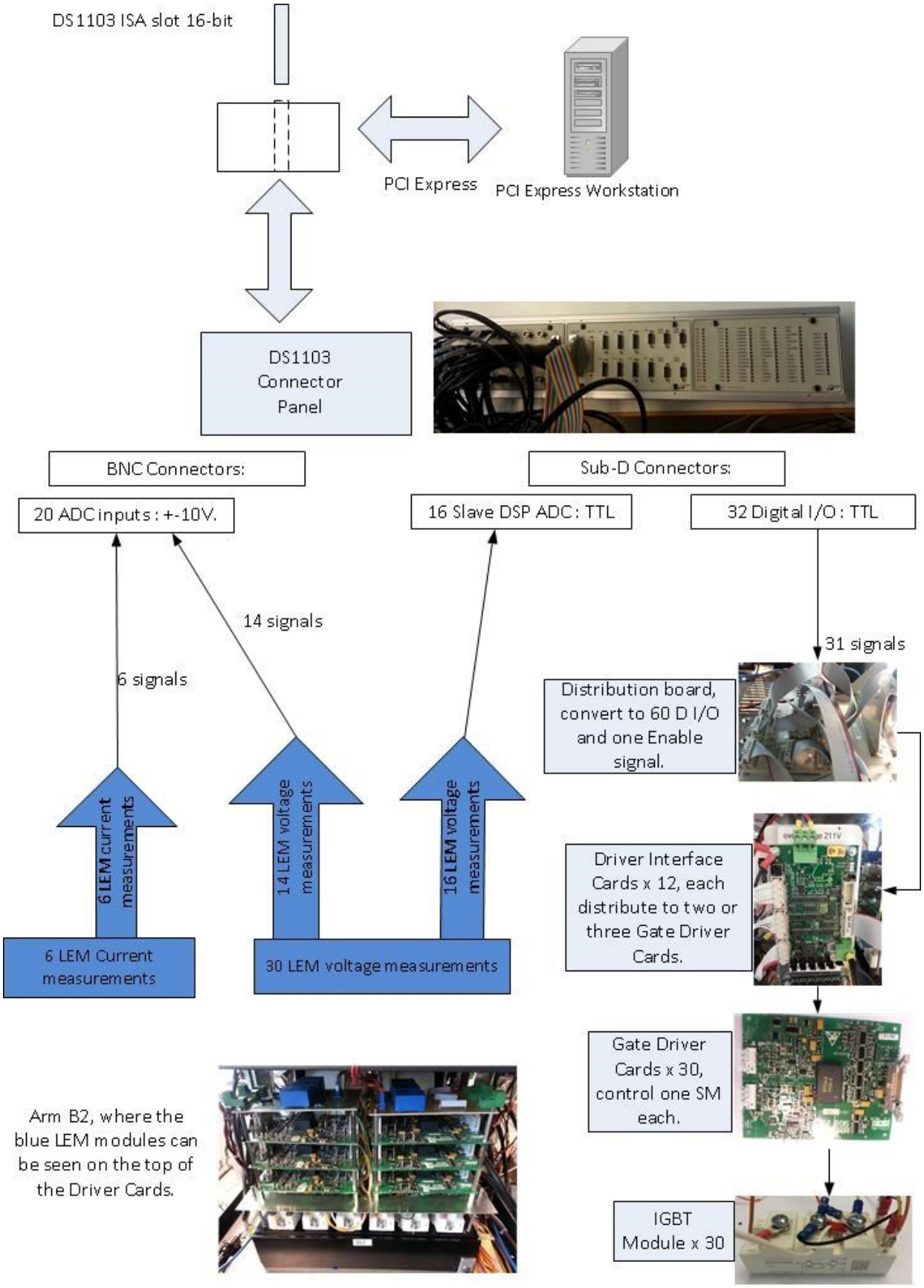

Figure 5-2 Overview of the Control Connections from dSPACE to IGBT

5.3 Main circuit design

In this subchapter, the main circuit design of the hardware setup will be presented. The design overview can be seen in Figure 5-4. The labels and colors in the Figure are consistent with the actual setup. The Common coupling points at the top (T) and Bottom (B) are coupled together in contactors driven by a 230V supply. In addition there is a contactor for the charging resistor. This contactor is driven by a separate switch, and is located between the positive side of the DC-link and the point T. The capacitors are coupled between point 2 (negative) and 3 (positive) on the IGBT modules, and have a rating of 400V. A parallel resistor of 47kΩ is connected in parallel to each capacitor. They are oversized for the voltage values used in this report, but the possibility to use the setup for higher ratings in the future was emphasized. The capacitors and the total test setup can be seen in Figure 5-3.

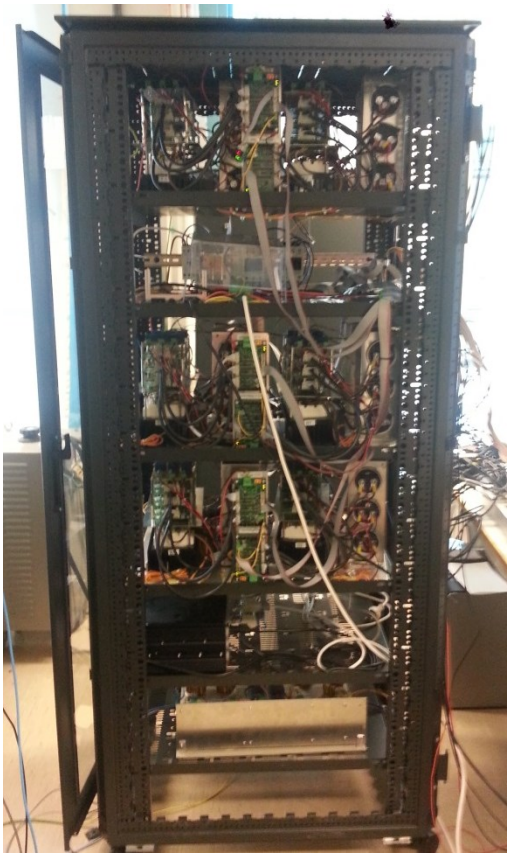

Figure 5-3 a) Capacitors, b) Total Test Setup

A relay is coupled to the arm currents measurements. If one of the arm currents exceeds 10 A., the DC-link will be turned off. This protection is mainly added in case of short circuit events or uncontrolled charging currents. This relay does not operate as expected and should be improved before higher voltages are implemented.

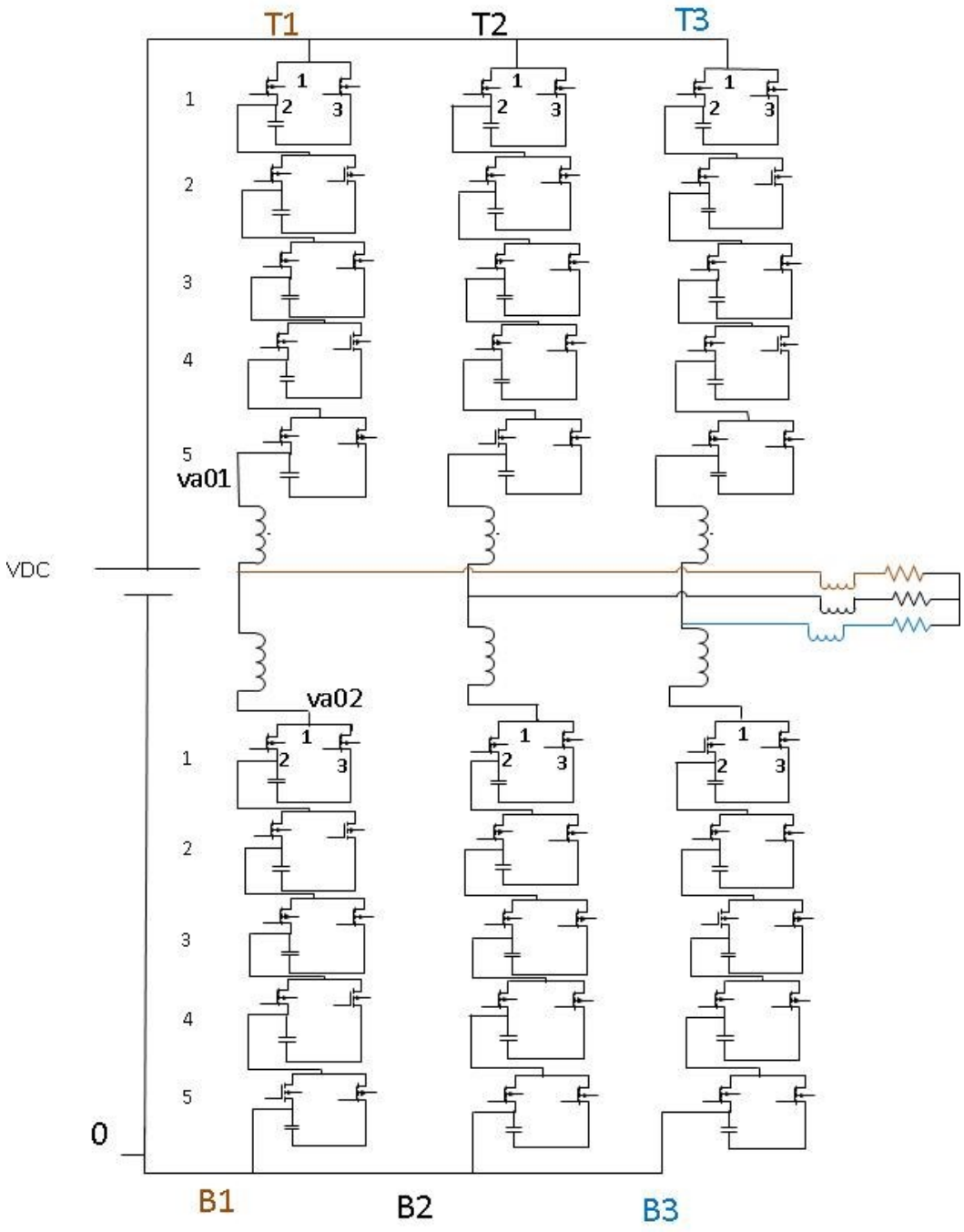

Figure 5-4 Overview Main Circuit Design

5.4 Hardware Design Considerations

During the construction of the hardware setup, there were many considerations to take into account. In this section these consideration will be discussed in order to facilitate further use or reconfiguration of the hardware setup.

A DS1103 from dSPACE was borrowed from Narvik University & College. In order to use this together with a modern host PC, an expansion box was ordered from dSPACE. This was necessary because the DS1103 had an ISA-slot interface towards the host PC. Modern PCs

use PCI or PCI express. The expansion box was ordered with PCI express, since this is the newest type of interface.

Another critical component to be purchased was the driver interface cards. The choice was based on the immediate availability of these cards, although they had a new design and was not tested before. Some modifications had to be made after testing to make the cards well-functioning for the setup. Also, the overvoltage trigger had to be lowered to about one third of the original value by short circuiting some of the resistances. To distribute the signals from dSPACE to the interface cards, a distribution board was made. Because of the time limitation, this was made by soldering wires to the proper pins of the outputs. The amount of wires was high, so the possibility of faults on this board was high. If the project had a longer time span, this board could have been made in a different way to lower the risk of faults.

The setup as it was when the rebuilding started did not have a proper description of the connections; this made the building process slower. To ease the future use of the hardware it was decided to document the connections and signal mapping during the design process. This document is given to the Department of Electrical Engineering at NTNU and hopefully it will also exist as a working document whenever changes are made.

5.4.1 Properties of dSPACE DS1103

The controller board DS1103 from dSPACE has a specific amount of in and outputs for the software/hardware interface. An overview of the signals used for this test setup is given in Table 5-3. The Master and Slave DSP are the names used for the two processors present in the board. The task partition between them can be seen in Figure 5-5.

Table 5-3 dSPACE Channels [29]

Channel Type	Number of Channels	Properties
Analogue to Digital Converter	Master: 20	• 16 multiplexed channels with 4 sample & hold A/D converters • 4 parallel channels each with one sample & hold A/D converter *8 A/D converter channels can be sampled simultaneously. conversion time: multiplexed: 1µs parallel: 800ns
	Slave DSP: 16	• 16 multiplexed channels
Digital In & out Ports	Master	• 32-bit parallel I/O *Each 8-bit group can be set to input or output(programmable by software)

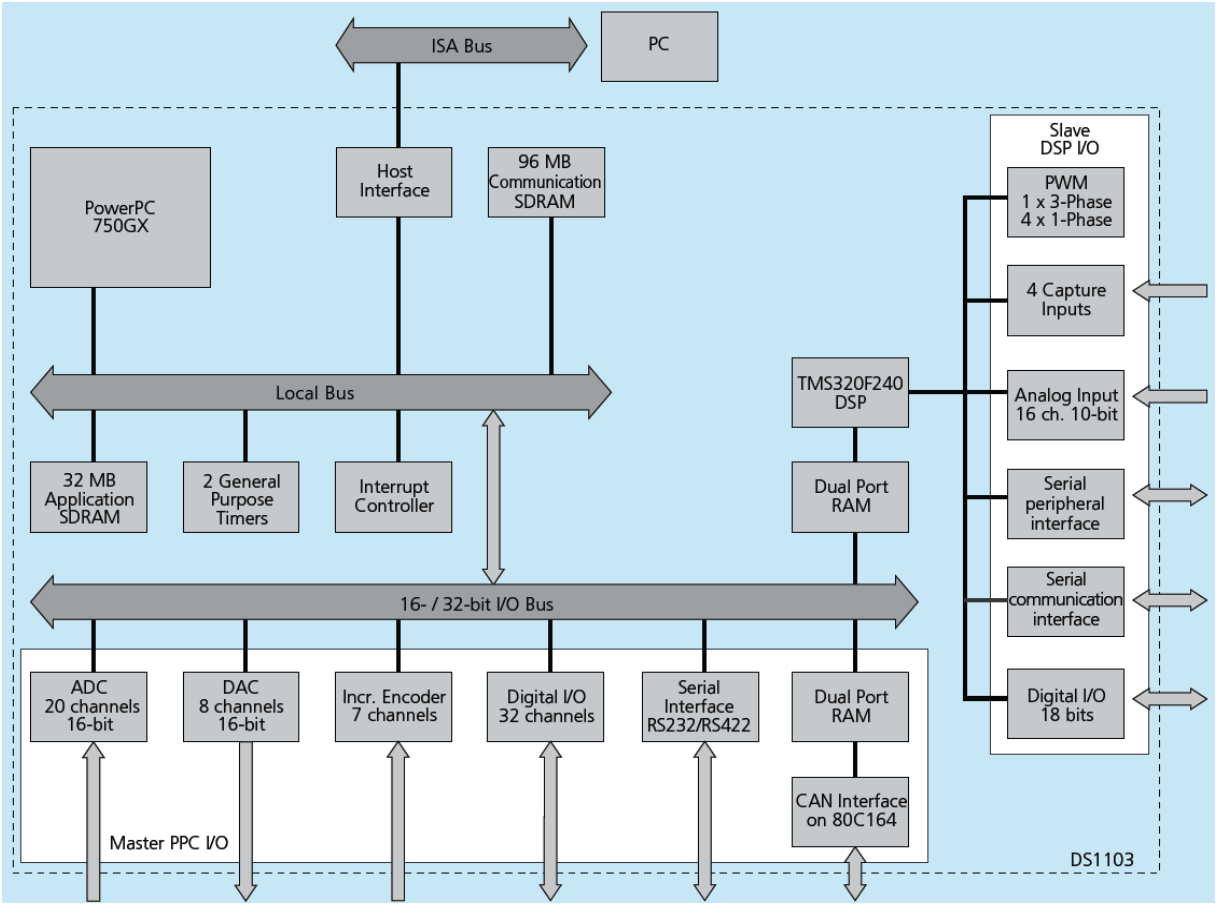

Figure 5-5 dSPACE DS1103 setup [29]

5.5 Software Design Considerations

In order to compile the Simulink control model into the dSPACE software, adjustments were required. The adjustments and considerations taken for the software are presented in this subchapter. First, the necessary changes to the Simulink model for real-time implementation are presented. Second, the required Simulink settings to optimize the control in ControlDesk are discussed. Third, the limitations for use were studied before installation of the required programs, and are gathered here to save time for future users.

5.5.1 Working in the dSPACE Environment

The transfer between the simulation environment and the real-time Hardware-In-the-Loop (HIL) led to several complications. The Simulink control system that was first constructed and simulated was not fit to run in real-time. To be able to use the control in real-time, the computation time had to be minimized. This was done in steps and with continuous testing of the system to ensure that the operation gave the same results as before the optimization. The procedure for minimizing the computation time followed the steps below, and was based on [30] and [1]:

- Discretize
- Active use of data types to reduce memory usage
- Reduce the amount of blocks by using vectors versus scalars
- Reduce the MATLAB fnc block computation time by reducing amount of loops and temporary variables.

To discretize the model, the solver, in the Simulation-Configure Parameters, is set to fixed step size and discrete. The use of different data types to reduce memory usage is a tradeoff between accuracy and speed. In MATLAB and dSPACE, the default variable data type is double. To shift between the data types, built in MATLAB functions can be used [31]. The different data types require specific memory space [32], and only the built in data types are supported for use in the Simulink environment. One exception is the Boolean data type, which can also be used. For a 64-bit MATLAB version, the data type double will require 64-bits, and the data type single only requires 32-bits. In this project it was chosen to implement the single data type for the reference waveforms, this was then simulated and compared with the double precision results. The results with the new data type were satisfactory. For the current and voltage measurements, the int8 data type was used, and Boolean was used for the signals sent to the transistors.

In order to reduce the amount of blocks, multiple signals are sent through the same blocks simultaneously. The Simulink blocks are made to perform mathematical operations on vectors. This was also an important optimization to perform in the MATLAB fnc. block which is a MATLAB function script within the Simulink model. This block requires more memory than the mathematical Simulink blocks, and should therefore be avoided to optimize

memory usage. For simplicity in constructing the model because of the time limitation, this block was nevertheless implemented in the model.

The output and input ports to the control was replaced by Real Time Interface (RTI) blocks to communicate with the dSPACE software for the hardware/Software interface. There are different blocks sets for the Master processor and the Slave DSP unit. The master digital in and out ports handle Boolean values of 8 bits grouped together. Each 8 bit group can be specified to be either inputs or outputs. It was originally decided to take in the OK signals from the Driver Interface cards to make sure that the Enable signal was not sent if one of the OK signals was not present. Since 30 outputs are required to drive the IGBT modules and one signal is required for the Enable signal, there would have been one input port left for the OK signal if they were not grouped together.

5.5.2 Simulink Settings for the ControlDesk Interface

In order to run the Simulink control system on the hardware, it is compiled to C code and loaded in ControlDesk. This is done by selecting Tools→Code Generation→Build Model in Simulink. The built file will save in the currently active MATLAB directory. To load the file in ControlDesk, a new experiment should be made. When this is done, the sdf file that was made during the build process should be dragged and dropped over the DS1103 icon in the Platform window. A more detailed description can be found in [33]. When the Simulink file is loaded, an interface can be designed by configuring ControlDesk to show the plots and variables desired by the user. In this interface, variables can be tuned during simulation.

To minimize the time step for the control system, some modifications was made before building the Simulink file. First, the Tasking mode, in the Configure Parameters-Solver, is set to Multitasking and second; the voltage measurements are gathered in an Atomic subsystem. This was done by selecting the subsystem parameters option, found by right clicking the subsystem, and selecting the Atomic Unit box. This type of subsystem operates independently from the rest of the model. This means that a separate time step can be defined. This was crucial for this particular setup because of the large amount of analogue signals. More details about Single and Multitasking mode can be found in [34].

The analogue input ports are time consuming for the processor to load. Since the capacitor values are quite large it is assumed that the voltage measurements can be sampled at a slower rate than the rest of the system and still obtain a valuable result. The DS1103 have a limited amount of analogue inputs, and most of them are multiplexed. The multiplexed channels in the Master part of DS1103 takes in four signals each. They will then sample the signals one by one; resulting in a slower measuring rate In the Slave DSP, there is one analogue channel that samples 16 multiplexed channels. If the voltage values vary in time significantly faster than they are loaded by the processor, this could cause problems for the voltage balancing algorithm. The processor loading time can also cause problems for the current measurements. If the measurements are not sampled within a reasonable time difference from when the

balancing algorithm switches the IGBTs, the capacitors can end up charging instead of discharging and vice versa.

Another important aspect is the amount of parameters that remain accessible and tunable during testing. This type of communication requires processor memory, and should be limited. One way to do this is by selecting both the “Inline Parameters” box and the “Signal storage reuse” box in the Configuration Parameters pane in the Optimization section. If some signals should remain tunable in ControlDesk, they can be defined by clicking on the Configure button next to the Inline Parameters option. If the code generation takes too long, it is possible to shorten this time by selecting the “Include only Simulink.Parameter and Simulink.Signal objects with global storage class” in the Code Generation-RTI variable description file options.

To further optimize the model, the pre-charging of the capacitors was made manual. Three parameters have to remain tunable, the Enable signal, the charging mode signal and a parameter that controls if the upper or lower arms are switched into the circuit for charging. The charging resistor is as described in chapter 5.3 switched in and out by a manual switch.

5.5.3 Compatibility Requirements for dSPACE Software 7.1

The software to use together with the DS1103 is the 7.1 release from dSPACE [35]. The newest MATLAB version that is compatible with this software is 2011a. The dSPACE software supports only 32-bit versions of MATLAB, Since a 64-bit operative system is used MATLAB automatically suggests to install the 64-bit version, so care must be taken during installation. Another installation requirement for all software to be used with the 7.1 version is pathways without parentheses [35].

Some of the Simulink blocks are unsupported by the dSPACE software. The most important ones are the Algebraic Constraint block and the MATLAB fnc block. The Embedded MATLAB Function block is in the newer MATLAB versions, also 2011a, called MATLAB fnc. With the software versions used for this test setup, this block compiled for dSPACE use.

A problem that could be encountered working with dSPACE is that an Embedded MATLAB Function block might convert the m-file to an S-Function. The S-Function might not compile depending on the operative system, or the MATLAB version that is used to run the software [36]. This problem can be solved by installing a bug fix from MathWorks.

5.6 Hardware in the Loop Functionality

In this section, the physical setup operation is verified by the measurements and switching signals present in ControlDesk. In 5.6.1 the current measurements are investigated. The current polarity at a given instant is very important for the balancing of the capacitor voltages. 5.6.2 the capacitor voltages are investigated by charging the upper and lower arms separately. In 5.6.3., the reference waveforms and control signals provided by the dSPACE equipment

will be shown. The currents and voltages in the different arms are labeled as shown in Figure 5-1. In each arm, the SMs are labeled 1-5 counting from the top of the arm and downwards. These notations are used throughout the section.

5.6.1 Current Measurements

In order to run the control successfully, the current measurements have to be correct. The behavior of the measurement modules has therefore been investigated, and will be presented in this section.

5.6.1.1 Verification of Measurement Modules

The currents are first measured with no voltage in the setup. The LEM modules which are integrated in the setup have a large AC offset, which can be seen in the Appendix 6. It is also clear that these measurement modules are affected by their own supply voltage. It is therefore chosen to replace these modules with current clamps.

To ensure that the supply for the current measurement modules does not supply voltage elsewhere, the same currents are measured with mobile meters. The results can be seen in Figure 5-6. With the new meters, there is no difference when the supply is turned on. In addition one of the new measurements is sampled by the oscilloscope, see Figure 5-7 and Figure 5-8. It can be seen that the supply voltage creates a small distortion in the current, but for the mobile meters, this distortion is so small that it is not visible when registered in ControlDesk. Based on these results, it was chosen to use the current clamps for the rest of the tests.

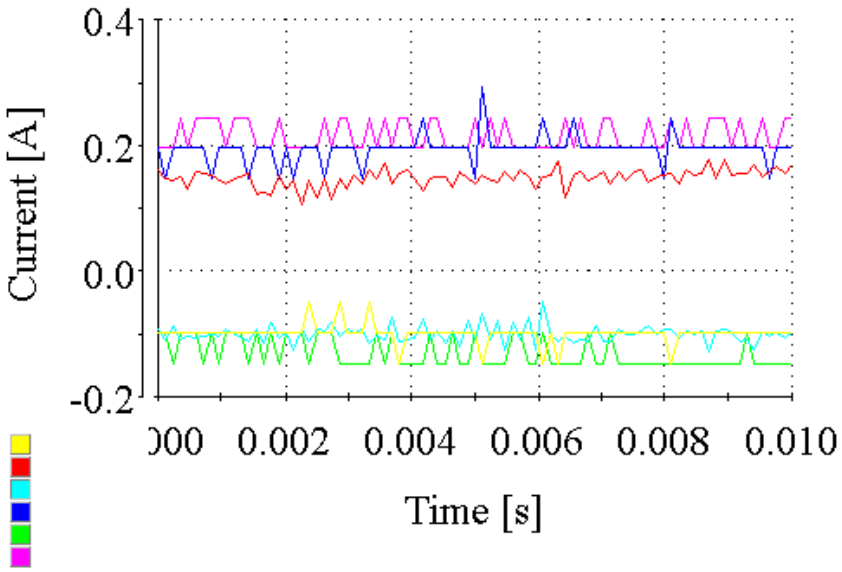

Figure 5-6 Current Measurements in T1(■), T2(■), T3(■), B1 (■), B2 (■) and B3 (■), Supply Voltage On

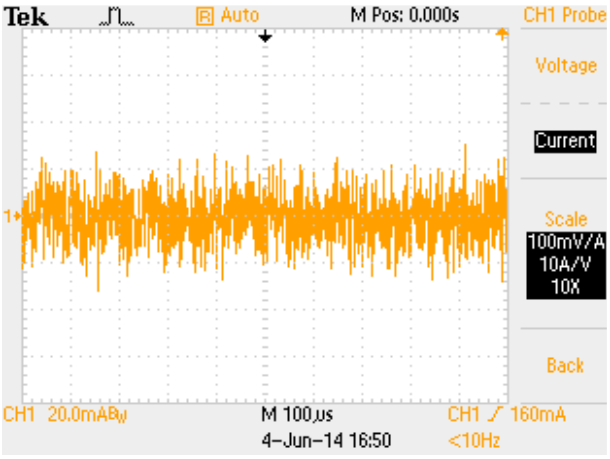

Figure 5-7 Arm Current with Voltage Supply OFF

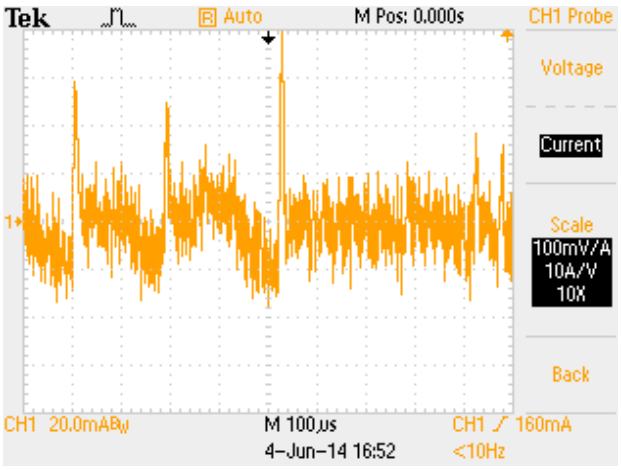

Figure 5-8 Arm Current with Voltage Supply ON

5.6.1.2 Current Measurements

The arm current measurements registrated by dSPACE are presented in Figure 5-9. It can be seen that they are 180° phase shifted with amplitude of approximately 5A. The period of these current waveforms corresponds to 50Hz.

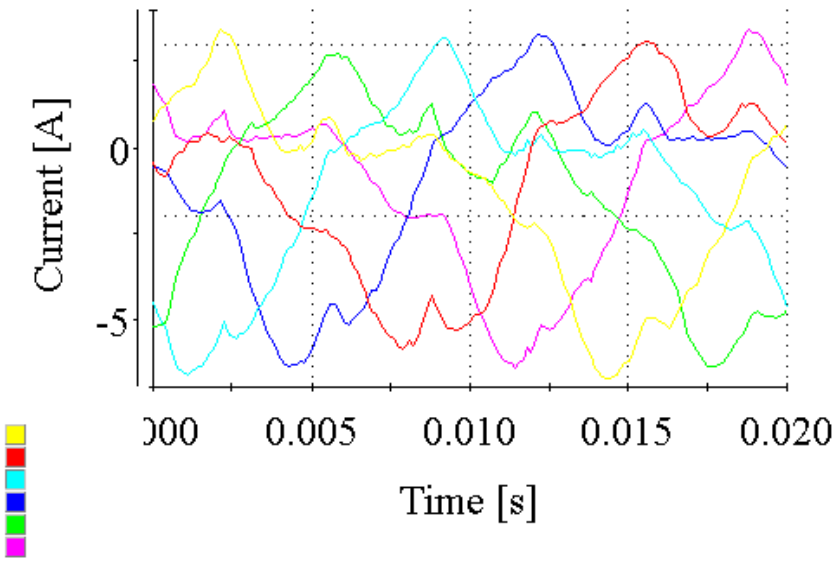

Figure 5-9 Current Measurements in T1(■), T2(■), T3(■), B1 (■), B2 (■) and B3 (■), Steady State

5.6.2 Capacitor Voltages

When the gate driver cards are energized, the capacitors charge to approximately 7V. Since they charge very slowly, it is assumed that they are charged by a the leak current from the gate driver cards. The IGBT modules have been tested separately to see if they switch

according to the signals sent by dSPACE. It has also been tested that the charging mechanism to couple in all the capacitors in the upper arm or all the capacitors in the lower arms gives the appropriate response.

The next step is to charge the arms separately by the DC-link. Since the voltages across the capacitors are around 7V. before the DC-link is turned on, the charging value is set to 20V. The DC-link input is therefore set to 100V. To limit the current, the charging resistor is coupled into the circuit. The charged capacitor voltage measurements can be seen in Figure 5-10. It can be seen that the lower arm voltages are measured to a higher start value than for the upper arms. This is because the lower arm voltages, in addition to cell 1 in phase C, are measured by the Slave DSP. Those measurements have a small offset value of 3.5V. This value is subtracted from the measurements before they are sorted in the balancing algorithm. It can also be seen that the voltages in the lower arms seems more balanced than for the upper arm. This is not the case. The lower arm voltages are measured by the Slave DSP which have a slower sampling time than the Master PPC. The result is smaller voltage ripples in the measurements. When the IGBTs are switches to discharge the capacitors, it takes some time before they do. This supports the assumption that the measurements can be sampled at a slower time step and that the time constant approximation is useful.

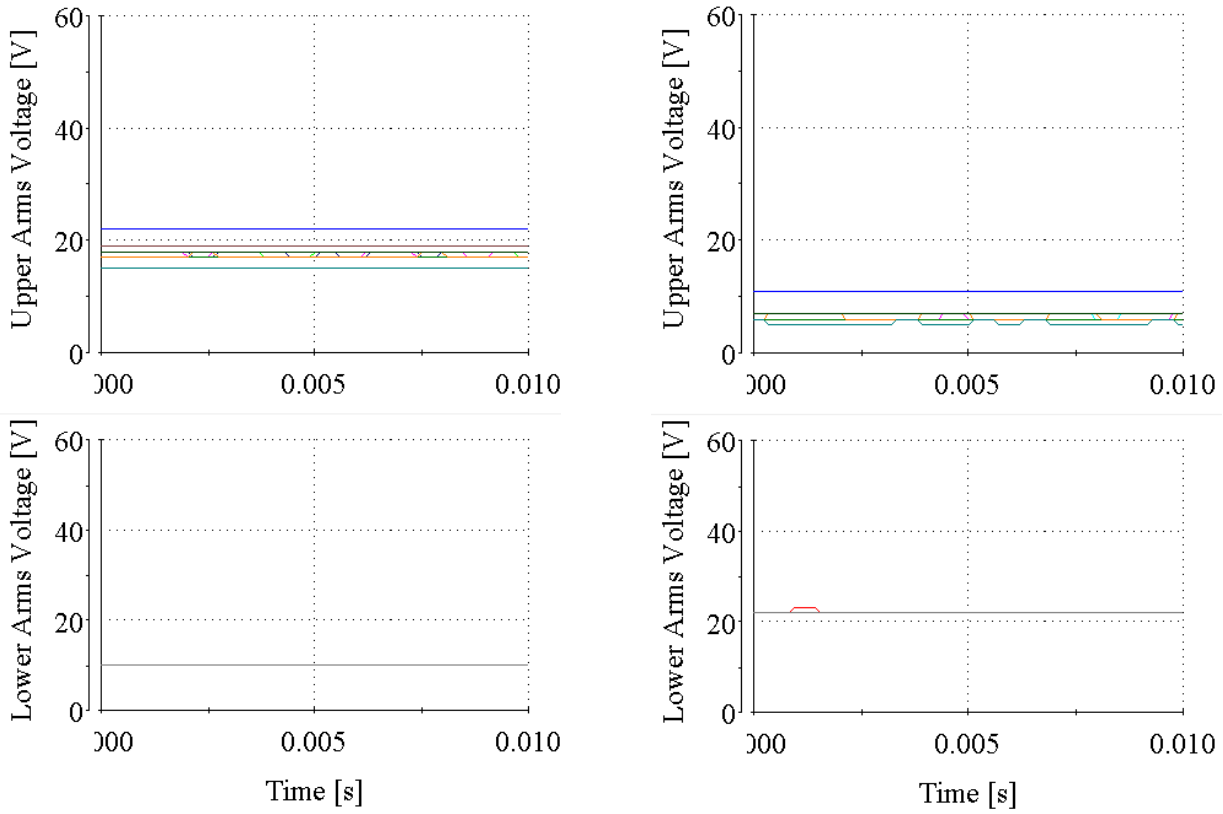

Figure 5-10 Capacitor Voltage charging a) Charged in Upper Arms b) Charged in Lower Arms

During steady state operation of the converter, the capacitor voltages are measured to be like shown in Figure 5-11.

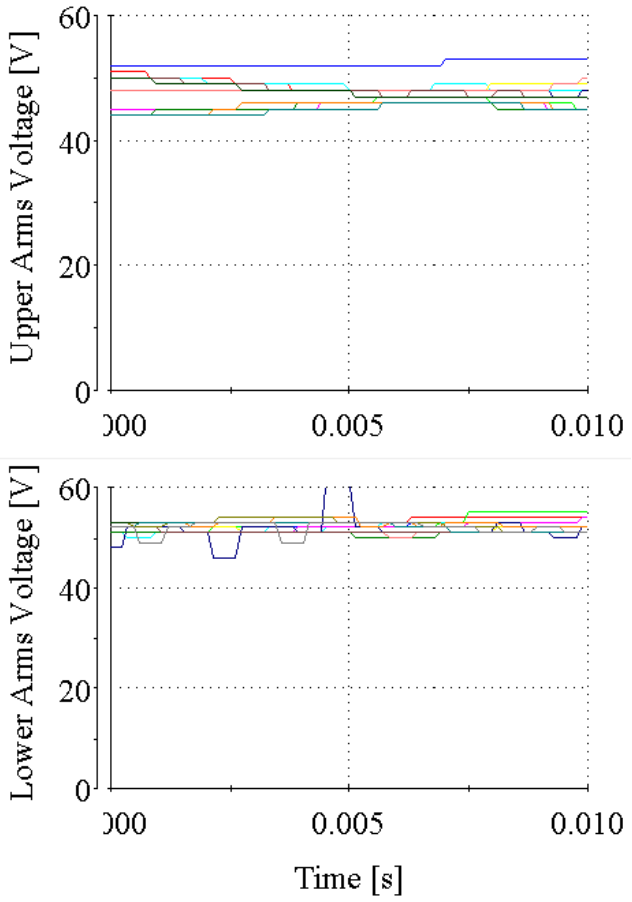

Figure 5-11 Capacitor Voltages, Steady State

5.6.3 Control Signals Provided by dSPACE

To investigate the operation of the converter, an analysis of the control signals is performed. The aim is to see if the control signals are affected by the current and voltage measurements as intended. The detailed analysis is focused on the upper arm in phase A which is labeled T1. The switching signals for the IGBTs are supplied by the dSPACE software interface. In this section both the steady state and the RMM signals will be presented.

The reference waveforms produced to compute the PWM signals are shown in Figure 5-6. In a), the reference waveforms for the fault tolerant state is presented, and the steady state references are shown n b). The change in the waveforms is based on the calculations in 3.2.

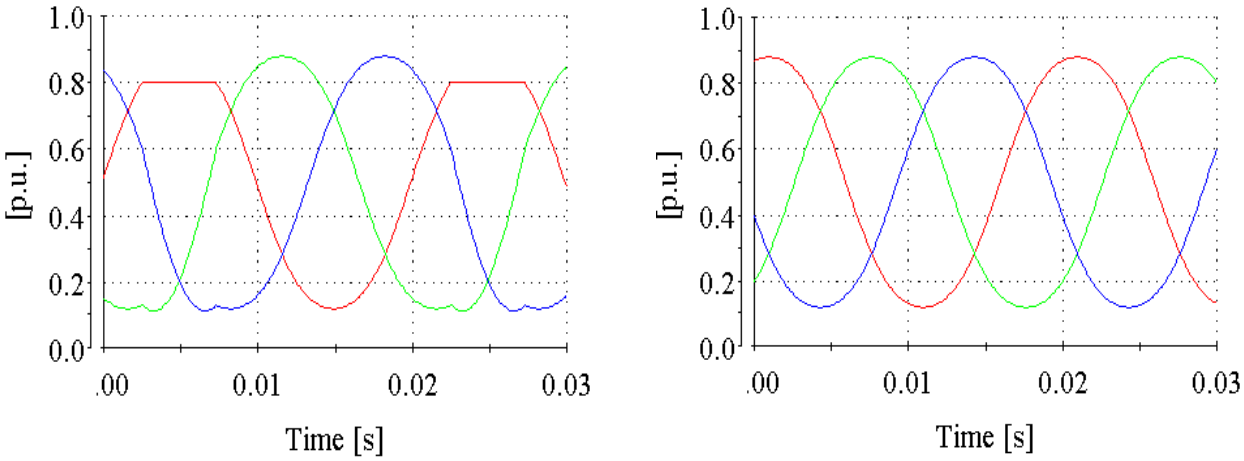

Figure 5-12 Reference Waveforms, a) RMM b) Steady State, T1 (■), T2 (■), T3 (■)

The triangular carrier waveform is set to a frequency of 2100Hz and can be seen in Figure 5-15 and Figure 5-16. To obtain the correct waveform, the repeated sequence block is used. The sequence is defined based on the time step of the model, and not the wanted frequency. This is to prevent distortion in the shape and amplitude of the waveform. The time step for the model is set to 119.05µs. The period of the waveform is set to four times this time step.

The carrier waveform is compared to the reference waveform to produce the PWM signals. The computation of the amount of capacitors that should be inserted in addition to reference waveform for T1 are plotted in Figure 5-13 for steady state The waveform is 50Hz, and it has the expected amplitude. The arm modulation index is set to 0.9, but since the arm references are scaled down and shifted by 0.5, the reference amplitude will change accordingly. It can be seen that the calculated amount of SMs inserted corresponds well with the reference waveform. In Figure 4-18 the same waveforms are plotted for the fault tolerant state. It is clear that the maximum amount of SMs inserted is reduced.

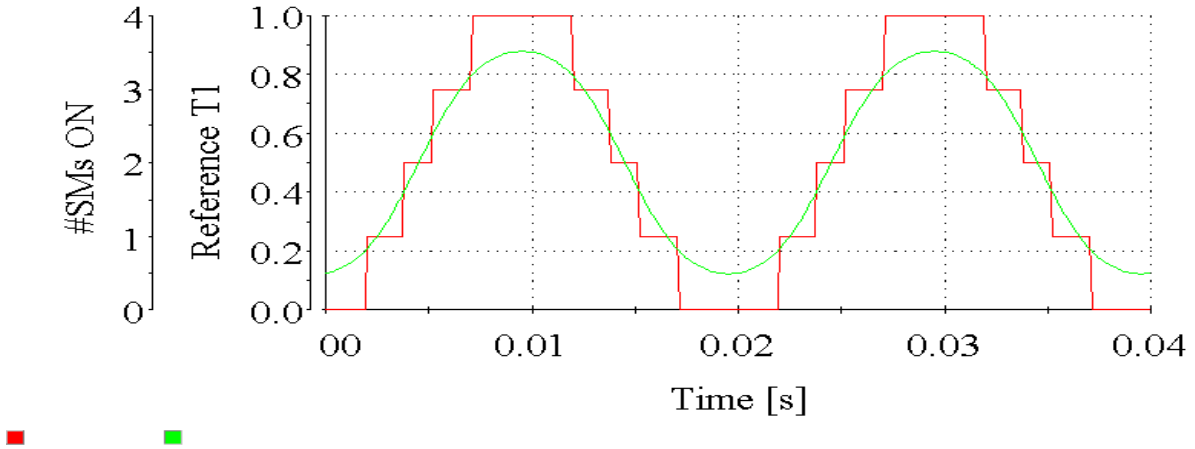

Figure 5-13 T1 Reference (■) and #SMs ON (■), Steady State

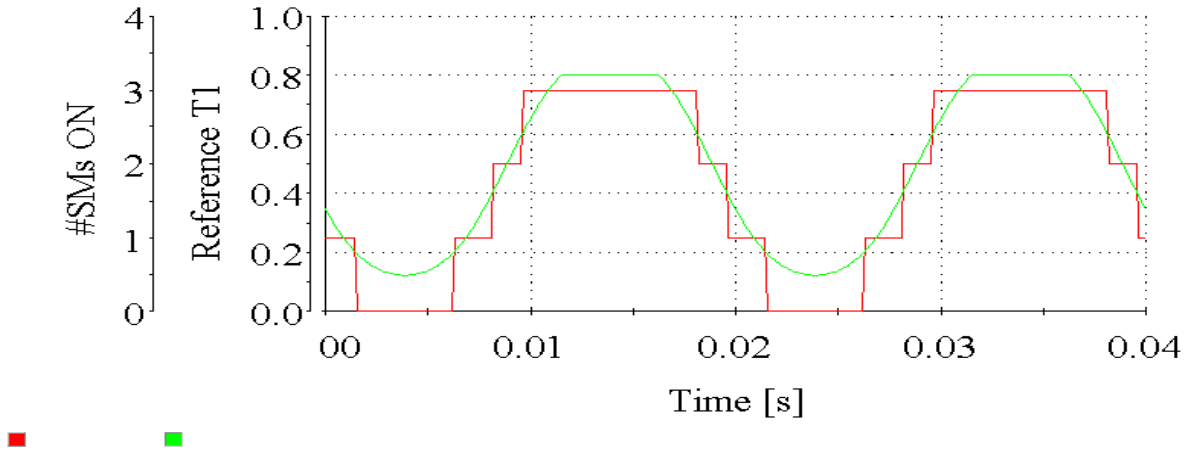

Figure 5-14, T1 Reference (■), #SMs ON (■), RMM

The PWM signals for the upper arm in phase A for steady state can be seen in Figure 5-15. In this plot, the green line is the PWM signals, the blue line is the reference waveform and the red line is the triangular carrier. It can be seen that the reference waveform amplitude is equal to the triangular carrier amplitude. In Figure 5-16, the PWM signal for fault tolerant state is shown. The peak of the reference waveform goes to zero when the fifth SM should have been switched with the PWM signals.

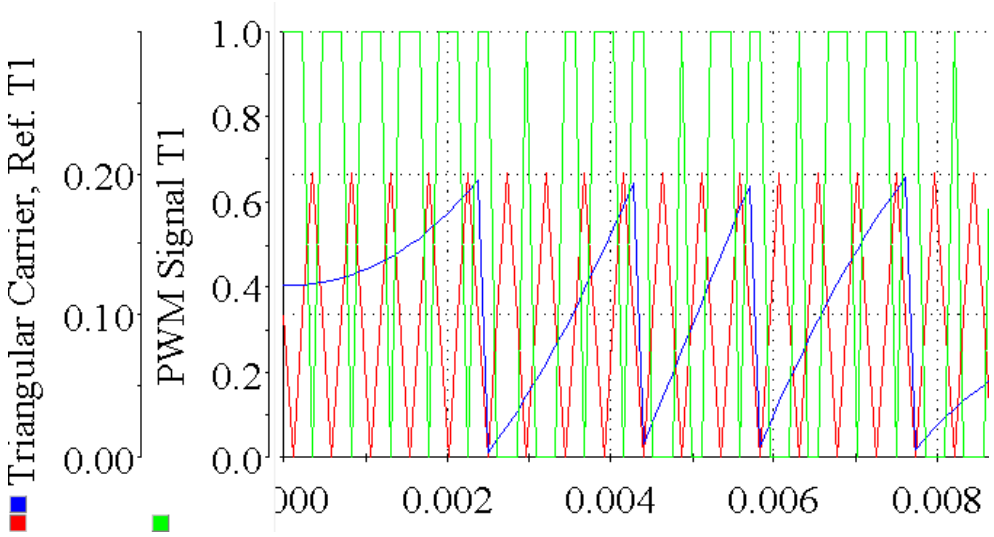

Figure 5-15 ■Triangular Waveform, ■Reference Waveform and ■PWM Signals, T1, Steady State

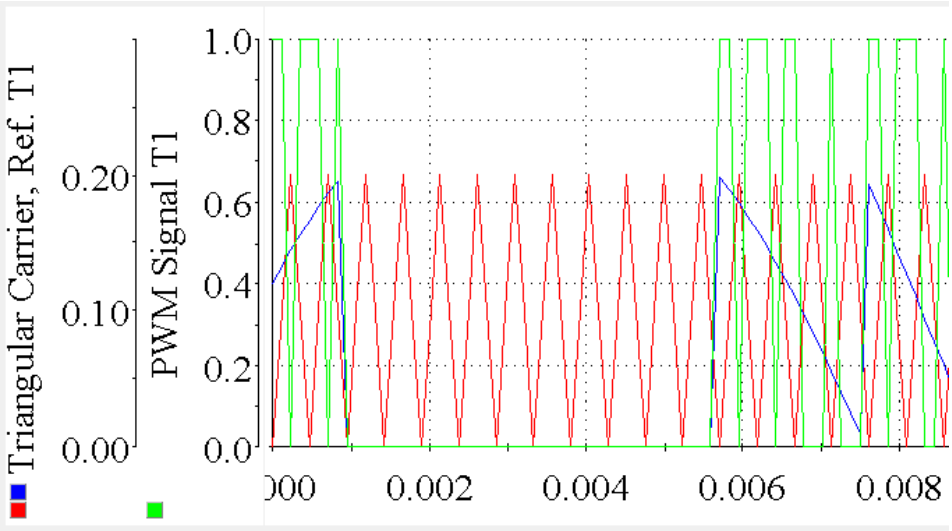

Figure 5-16 Triangular Waveform (■),Reference Waveform (■) and PWM Signals (■), T1, RMM

In Figure 5-17 the voltage measurements, control signals and current in T1 is presented. The color boxes shown in the y-axis represents the different SMs in T1. They are sorted from red to purple.. The red and purple color represents SM 1 and 5 respectively. The labeling of the converter circuit can be seen in Figure 5-1. In c), the current is plotted together with the signal for the amount of SMs to be inserted. For this analysis, only the polarity of the current is interesting. The data type chosen for the voltage measurements is int8. This means that the measurements will show as whole integers. In Appendix 5, the choice of PWM SM is shown together with the amount of SMs inserted and the control signal for SM1 in B1.

If the current is positive, it will insert the SM with the highest label number when equal voltage values are measured and vice versa. To reduce the number of switching done in the circuit, this algorithm should be changed to account for equal measurements. The balancing algorithm can be seen in Appendix 7. For further verification, more plots of these signals are included in Appendix 5.

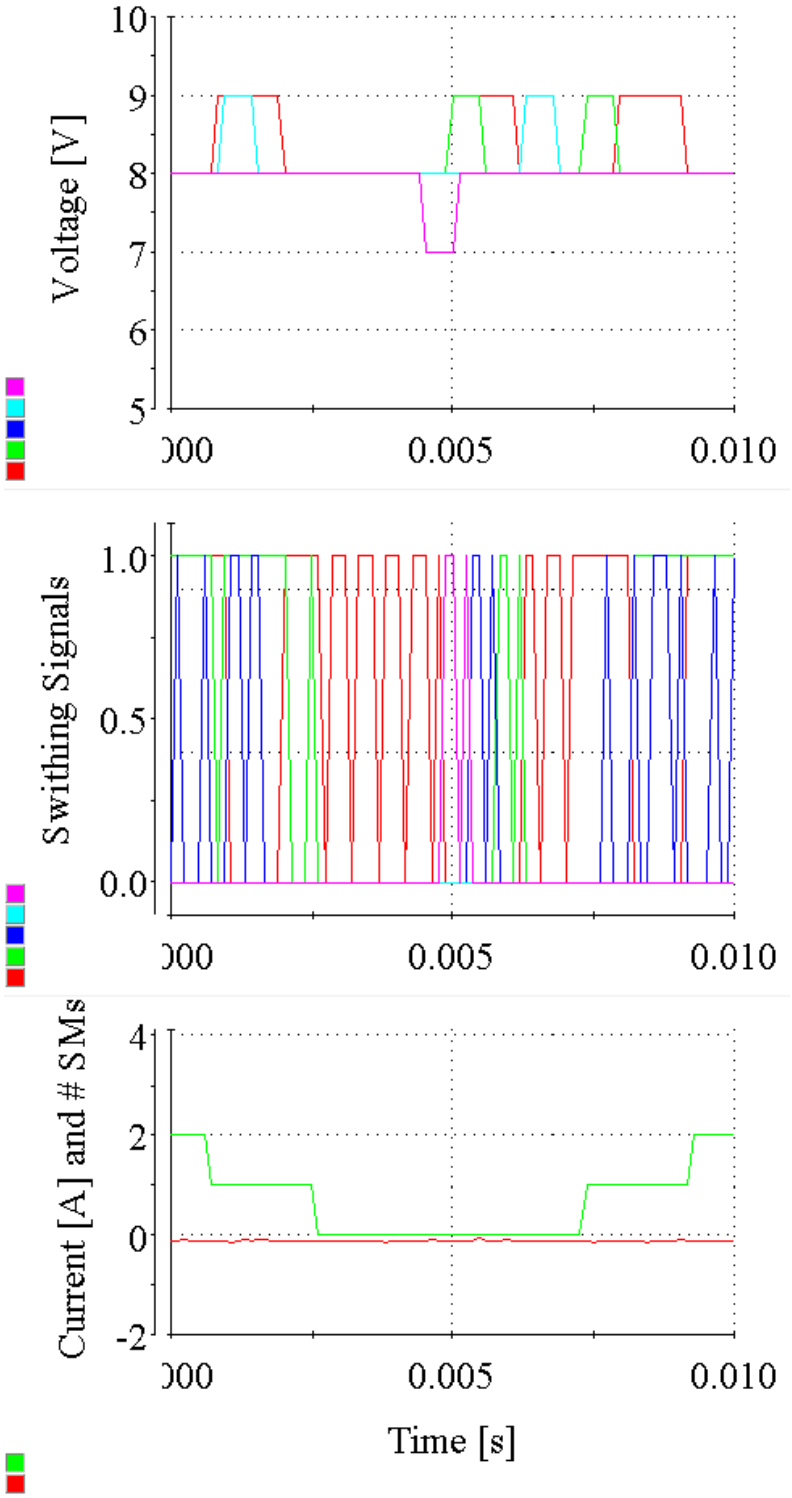

Figure 5-17 a) Voltage Measurements, b) Control Signals c) ■Arm Current and ■Amount of SMs to be inserted, T1

5.7 Hardware in the Loop Steady State Results

The measurements registered by the oscilloscope in steady state will be presented in this section. The input DC-link is set to 250V, and the phase load is 12.5Ω. Originally, the

resistive load should be 27Ω. One of the available resistances was coupled in and measured to be 9.12Ω. Without further testing, it was assumed that the resistances were equal, and three resistances were coupled in series per phase. In the process of analyzing the results, this mistake was revealed because of the high current measured and the high losses in the converter.

The load inductance was adjusted by measuring the phase shift between voltage and current with a three phase AC supply, the resistive load and the inductive load coupled in series. The resistive value used in this calculation was wrong, and the inductance was therefore set on 18.7mH instead of the planned 40mH. Because of the time limitations, the measurements were not done again with the planned parameters. Calculations based on basic circuit theory to confirm these arguments can be seen in chapter 6.1.

5.7.1 Voltages in Steady State

In this section the capacitor voltages will be investigated.Figure 5-18 shows the output phase voltages. The phase shift between phase A and B is 118.3°, phase B and C is 121.9° and phase A to C is 119.8. The amplitudes are approximately 100V and the phases are approximately 120° shifted. The fundamental frequency component of the phase and line to line voltages are shown in Table 5-4, whilst the Fourier analysis up to 7000Hz can be found in Appendix 3. The amplitudes differ with 1.1V at the largest. These differences are quite small and one central source of error is the voltage measurement modules. Since they are constructed to measure voltages up to 400V, the measurement error could be large for values around 50V. The voltage measurements error will affect the balancing algorithm to potentially insert the wrong SM considering the actual voltage values in the circuit. This will again affect the arm voltages, phase voltages and line to line voltages.

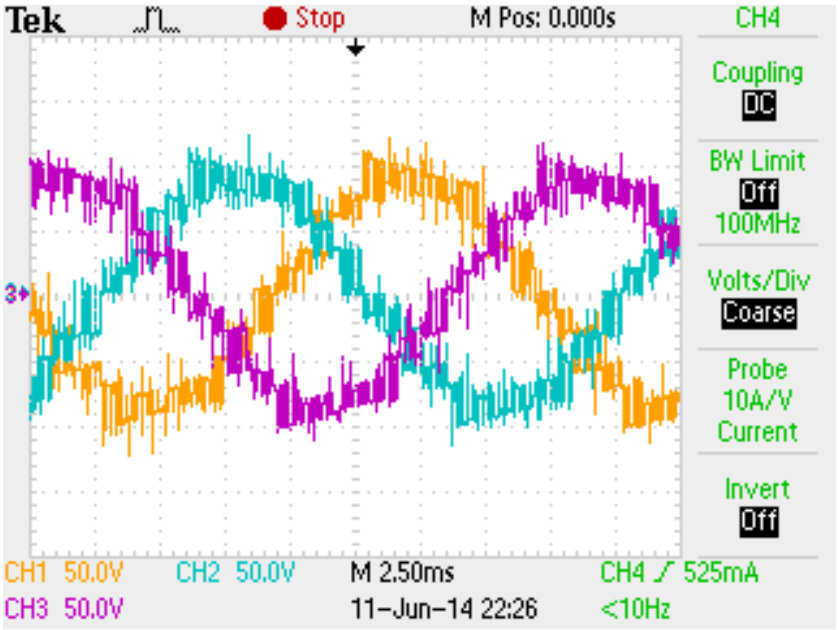

Figure 5-18 Phase Voltages, CH1:Va, CH2:Vb, CH3:Vc, Steady State, Hardware Setup

Table 5-4 Fourier Analysis, Fundamental Frequency, Hardware Setup, Steady State

PARAMETER	PHASE A	PHASE B	PHASE C	LINE AB	LINE CA	LINE BC
Magnitude [V]	90.6	91.5	91.7	158.1	158.4	155.6
Phase Angle [°]	105.2	-136.5	-14.6	132.8	12.1	-107.8
Phase Shift[°]	**A-B**	**B-C**	**C-A**	**AB-BC**	**BC-CA**	**CA-AB**
	118.3	121.9	119.8	120.7	119.9	119.4

The harmonic spectrum of phase A voltage is presented in Figure 5-19. It can be seen that the second and fifth order harmonic is significant. The reason behind and a solution to cancel them should be found for future use of this setup.

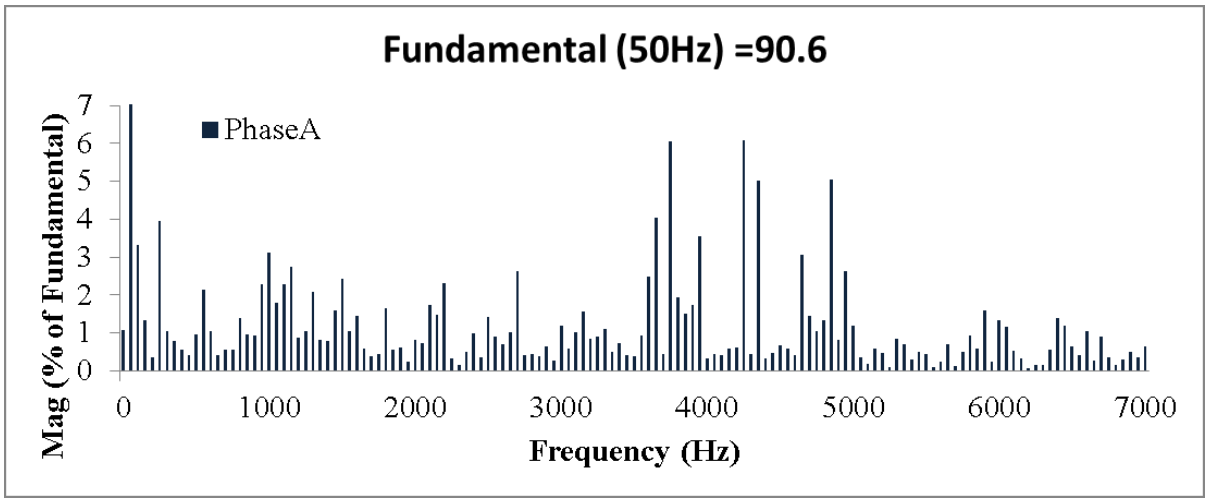

Figure 5-19 Harmonic Spectrum Phase A Voltage, Steady State, Hardware Setup

In Figure 5-20, the phase A and upper arm voltage is plotted. They are 180° phase shifted, and the levels in the arm voltage are approximately 50V. The value of each level is approximately similar which indicate balanced capacitor voltages. The phase A and lower arm voltage is presented in Figure 5-21. The lower arm voltage is in phase with the phase voltage.

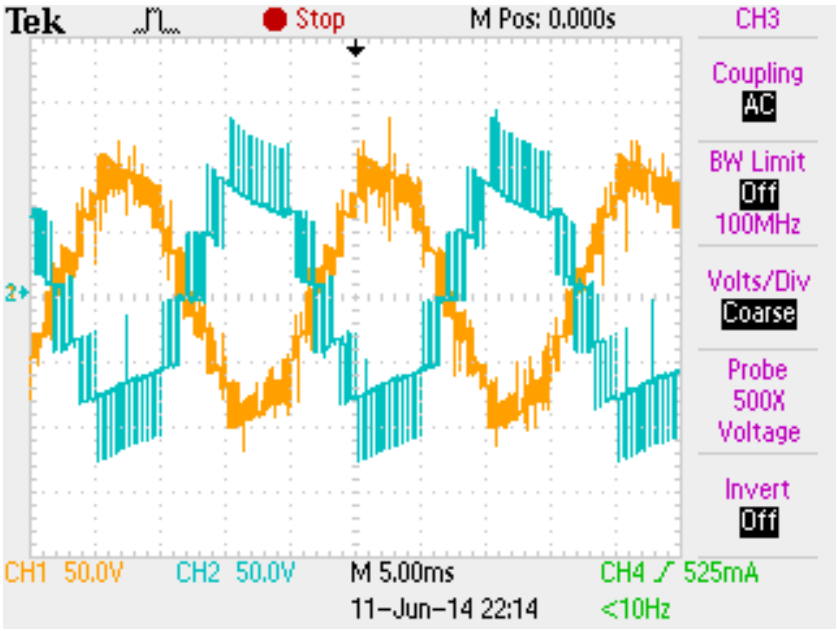

Figure 5-20 Upper Arm and Phase A Voltages, CH1:Va, CH2:vcp, Steady State, Hardware Setup

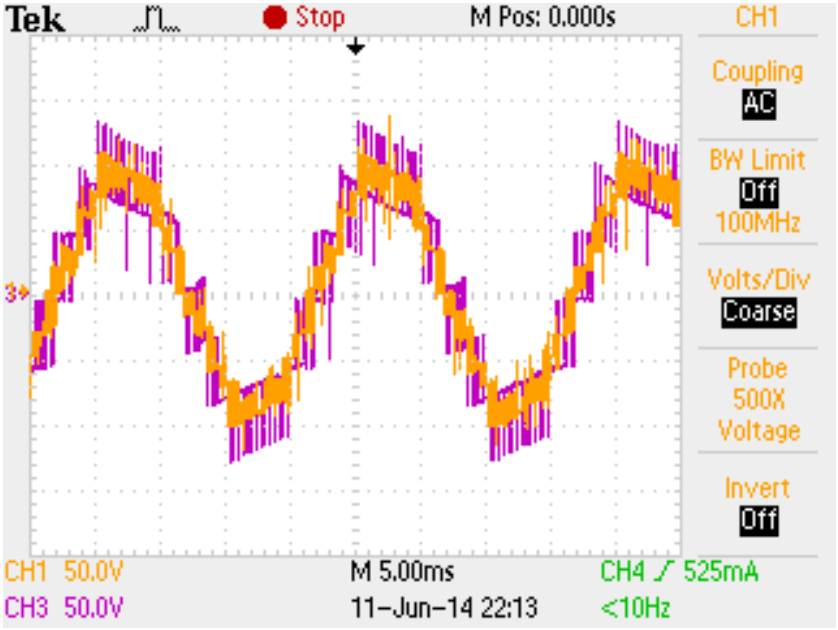

Figure 5-21 Lower Arm and Phase A Voltages, CH1:Va, CH3: vcn, Steady State, Hardware Setup

In Figure 5-22, the line to line voltages are shown. The different levels are more distinct for these measurements. The phase voltages are measured across the phase load. Since the load neutral point is different from the DC-link neutral point, the phase voltages will have more levels than the line to line voltages. The fundamental frequency components are presented in Table 5-4. The voltage amplitude vary between 155.6 and 158.4V, whilst the phase shift span from 119.4° to 120.7°.

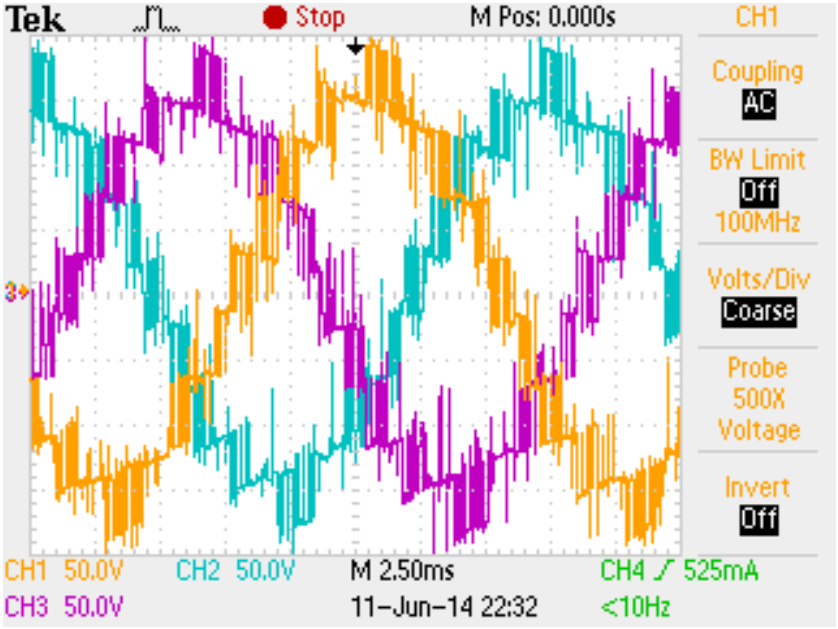

Figure 5-22 Line to Line Voltages, CH1:VAB, CH2:VBC, CH3:VCA, Steady State ,Hardware Setup

5.7.2 Currents in Steady State

The phase currents during steady state are presented in Figure 5-23. The shapes are sinusoidal, and they appear balanced. In order to evaluate the waveforms, the Fourier analysis of the fundamental component is presented in Table 5-7. The phase C current's amplitude is 0.1A lower than the two other phases, and the phase shifts varies from 119.3° to 120.9°.

Table 5-5 Fourier Analysis of Phase Currents, Fundamental Frequency, Steady State, Hardware Setup

PARAMETER	PHASE A	PHASE B	PHASE C
Magnitude [A]	6.7	6.8	6.7
Phase Angle [°]	97.3	-22.5	-143.4
Phase Shift[°]	**A-B**	**B-C**	**C-A**
	119.8	120.9	119.3

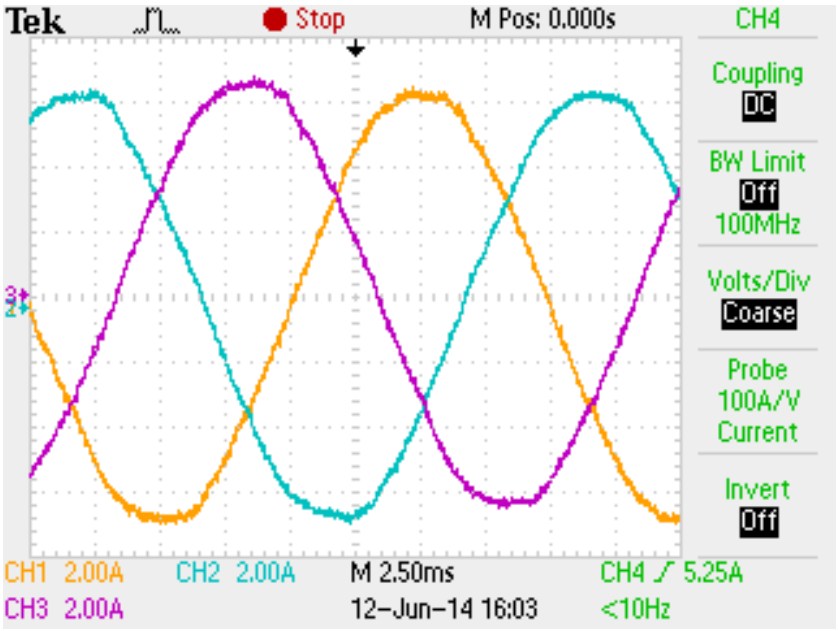

Figure 5-23 Currents, CH1:ia, CH2: ib, CH3: ic, Steady State, Hardware Setup

In Figure 5-24, the arm currents are presented. It is clear that the upper and lower arm currents are 180° shifted in relation to each other, but the shape is different from the simulation results. A Fourier analysis of the low order harmonic content of current in T1 is presented in Figure 5-25. The amplitudes of the harmonics are represented as the rate value compared to the fundamental. The fundamental component has amplitude 0.9A. It can be seen that the expected 2nd order harmonic has amplitude of 0.28. In addition, the 6th order harmonic has amplitude 0.26. Numbers for higher order harmonics are included in Appendix 3.

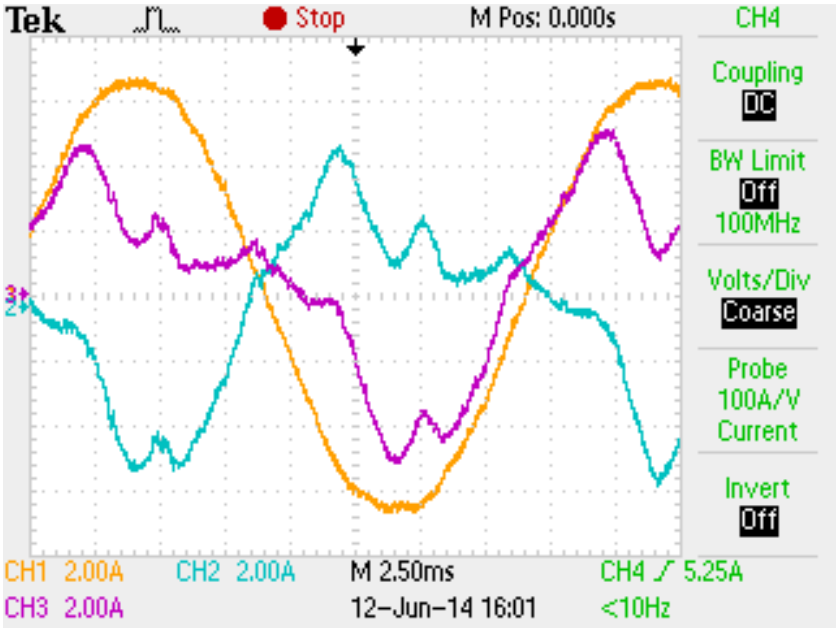

Figure 5-24 Phase A Currents, CH1:ia, CH2:ip, CH3:in, Steady State, Hardware Setup

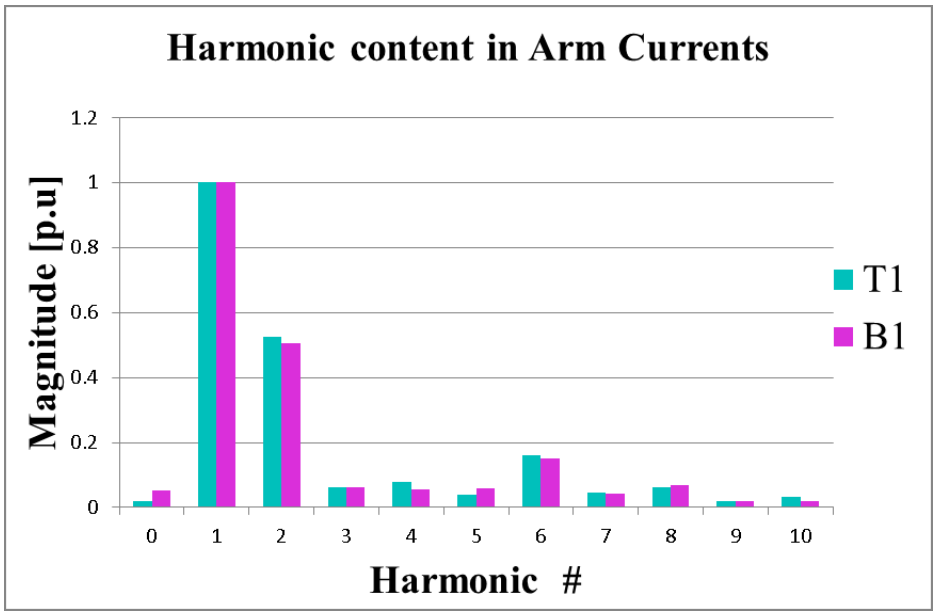

Figure 5-25 Harmonic Contents of Current in T1, Steady State , Hardware Setup

5.8 Hardware in the Loop Fault Tolerant State

In this section, the results from the hardware setup in fault tolerant state will be presented. To simulate a fault in SM1 in T1, the arm connection point is moved from point 1 on IGBT module 1 to point 1 on IGBT module 2. In Figure 5-26, the brown wire which enters in the lower right corner is connected to the second IGBT module instead of the connection marked I.

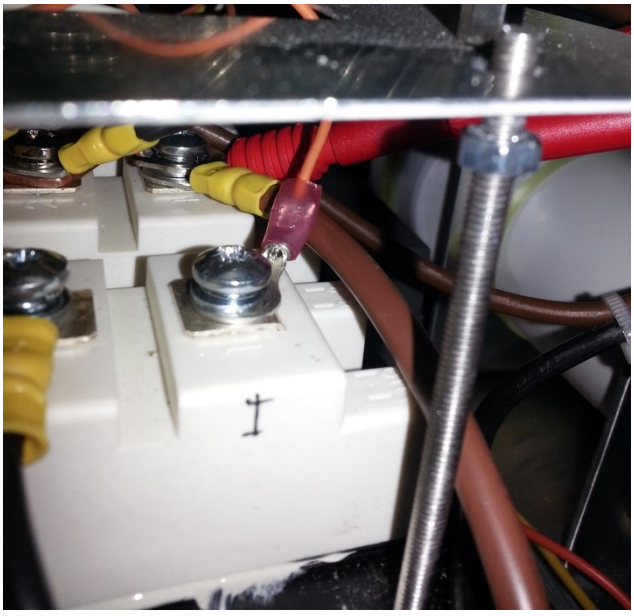

Figure 5-26 Bypass of SM1 in T1

Since some unexpected current peaks appeared, the setup was run with an input voltage of 100V. The mean capacitor value becomes approximately 20V. In Figure 5-25, the unexpected

current peaks are shown. Only the currents in phase A are affected, and the peaks are not periodic and the magnitude varies. One of the small peaks is shown here, but they can reach 10A in magnitude with 100V DC input. Since they are not periodic, they were not observed before the voltage supplies to the gate driver interface cards started to signal an error. They were no longer able to deliver enough current to the gate driver cards for input voltages above 200V. The overcurrent protection connected to the LEM modules is implemented to switch off the DC-link for currents above 10A, it is therefore confirmed that this protection is not working as intended.

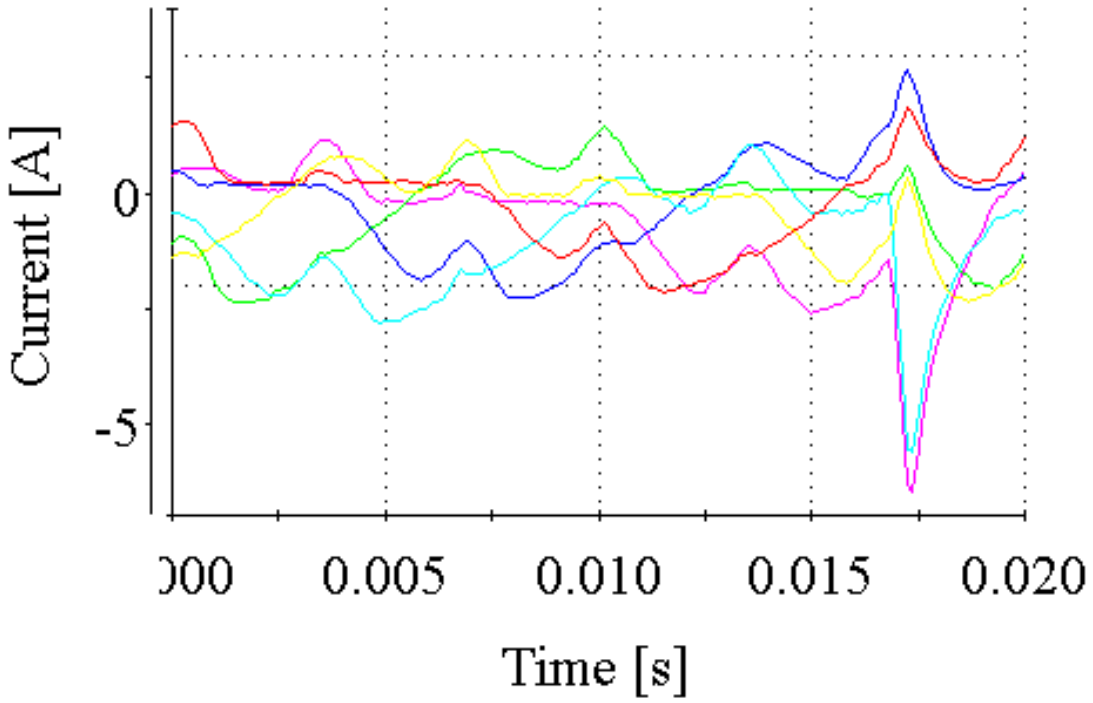

Figure 5-27 Current Measurements in T1(■), T2(■), T3(■), B1 (■), B2 (■) and B3 (■), Mobile Meters, Reference Modification

5.8.1 Voltages with Reference modification

In order to investigate the behavior of the RMM, the phase and line voltages are measured. The phase voltages can be seen in Figure 5-29. The amplitudes are approximately 40V and the phase shifts are close to 120°. The Fourier analysis of the fundamental frequency is presented in Table 5-6. The magnitude of the 50Hz component is around 34V. Figure 5-28 shows the harmonic spectrum of phase A up to 7000Hz. There are several lower order harmonic components that should be canceled in order to reduce losses in the circuit.

Table 5-6 Fourier Analysis, Voltages, Fundamental Frequency, Hardware Setup, RMM

PARAMETER	PHASE A	PHASE B	PHASE C	LINE AB	LINE CA	LINE BC
Magnitude [V]	34.0	33.9	34.5	60.2	60.3	59.8
Phase Angle [°]	83.9	-35.3	-155.5	137.2	16.7	-103.0
Phase Shift[°]	**A-B**	**B-C**	**C-A**	**AB-BC**	**BC-CA**	**CA-AB**
	119.2	120.2	120.6	120.5	119.7	119.8

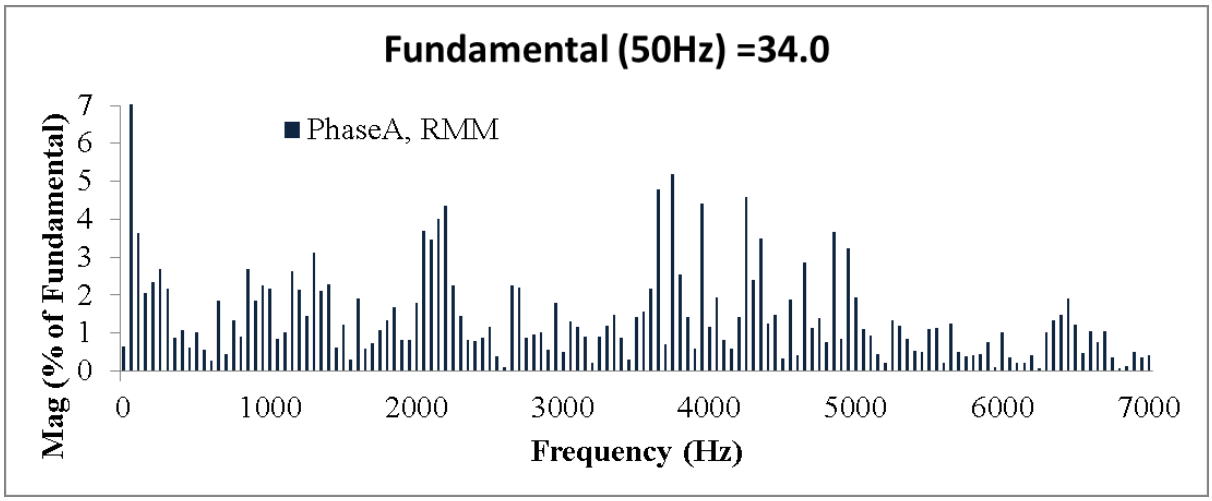

Figure 5-28 Harmonic Spectrum for Phase A, RMM, Hardware setup

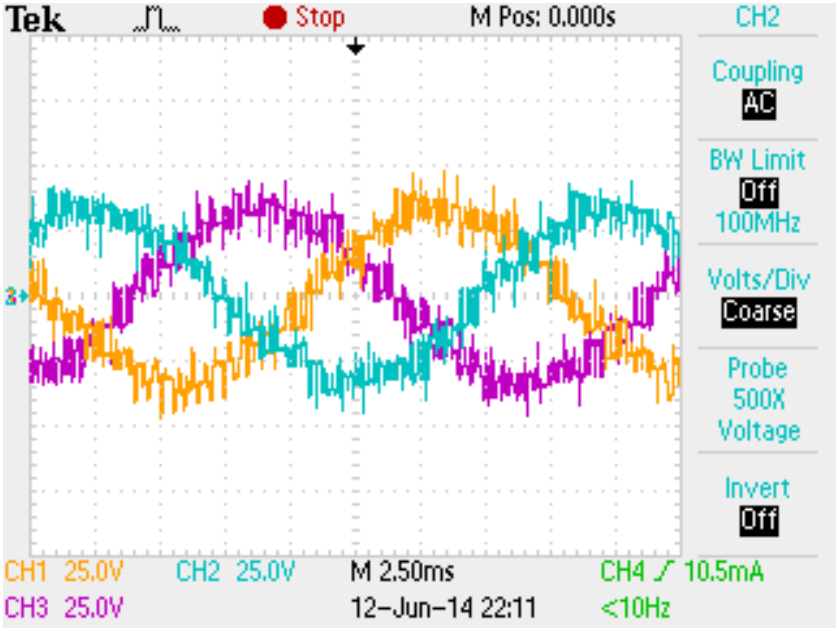

Figure 5-29 Phase A Voltages, Reference Modification

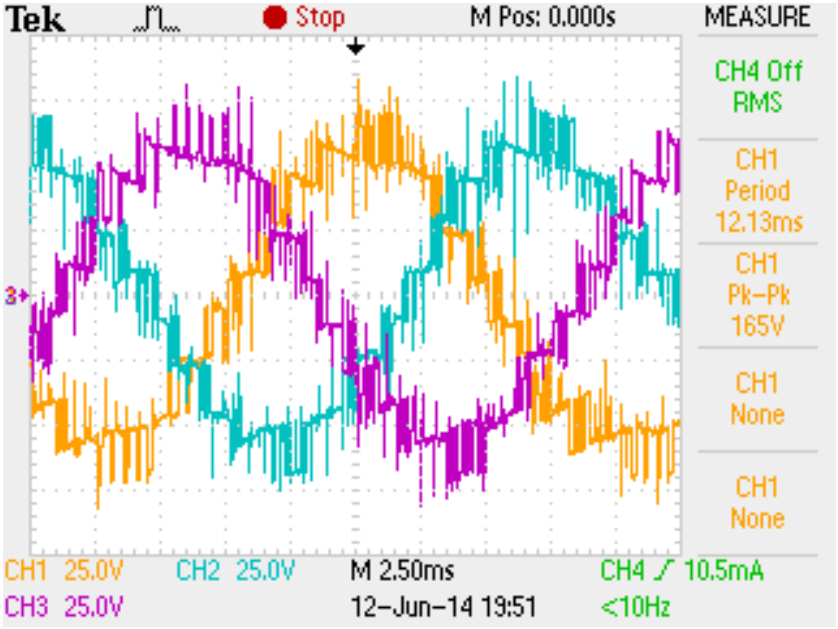

Figure 5-30 Reference Modification, Line to Line Voltages, CH1:VAB, CH2:VBC, CH3:VCA

Figure 5-31 shows the arm voltages in phase A and the phase A output voltage. It can be seen that the arm voltages now have four levels. The four levels are made by the remaining four SMs in T1. In B1, one voltage level is lost due to the parallel coupling of the DC-link, see chapter 3.2.

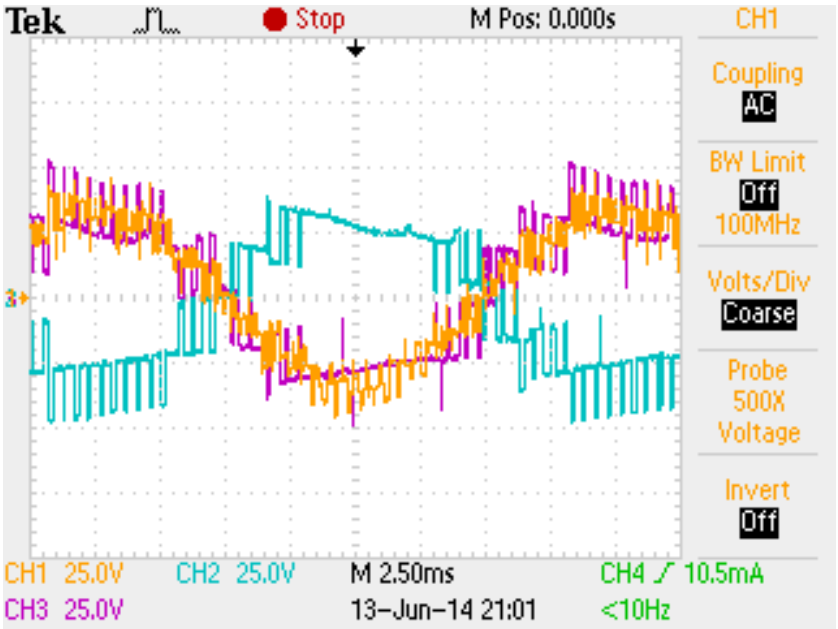

Figure 5-31 Reference Modification, Phase A Voltage, CH1:VA, CH2:vap, CH3:van

5.8.2 Currents with Reference Modification

Figure 5-32 dislpays the phase currents. They are approximately 120° shifted, and the amplitudes are visually equal. A Fourier analysis is performed to investigate the fundamental

frequency component. The magnitude and phase angle can be seen in Table 5-7, and more frequencies are included in the Appendix 4. The phase A magnitude is 0.1A higher than for the two other phases, and the phase shift differs with 3.8°.

Table 5-7 Reference Modification, Fourier Analysis of Phase Currents, Fundamental Frequency, Hardware Setup,

PARAMETER	PHASE A	PHASE B	PHASE C
Magnitude [A]	2.7	2.6	2.6
Phase Angle [°]	30.5	-89.1	152.6
Phase Shift[°]	**A-B**	**B-C**	**C-A**
	119.6	118.3	122.1

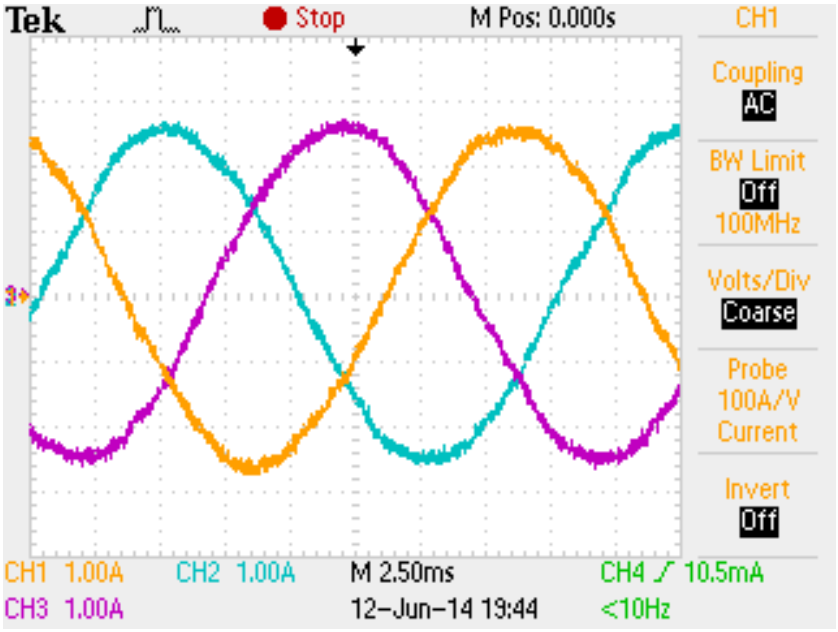

Figure 5-32 Reference Modification, Phase Currents, CH1: ia, CH2: ib, CH3: ic

In Figure 5-33, the currents in phase A are shown. Two measurements are included in order to show the difference in magnitude and the place within the period at which it occurs. In the graph to the left, the peaks appear after the phase current minimum, in contrary to the right where the peaks occur right before the phase current minimum. These peaks are not periodic, and several measurements were required to show them. In Figure 5-27, it can be seen that when there is a peak in the arm currents for phase A, the rest of the phase currents have a peak with the opposite polarity. This is expected based on KCL.

5.8.2.1 Arm Current Peaks Analysis

A Fourier analysis of the arm currents are performed, and can be seen in Figure 5-34. It is clear that they contain more harmonics compared to steady state. The harmonic content of the

current in T1 is much higher than for B1. The third order harmonic is particularly high with amplitude of 1.2. Although the arm currents are distorted, the phase current is not noteworthy affected. Possible sources of these peaks are;

- Voltage difference between phases or arms
- Circulating current harmonic caused by under dimension of arm inductors
- SM1 bypass is not correct
- Control code error
- Current leakage from SM1 gate driver card

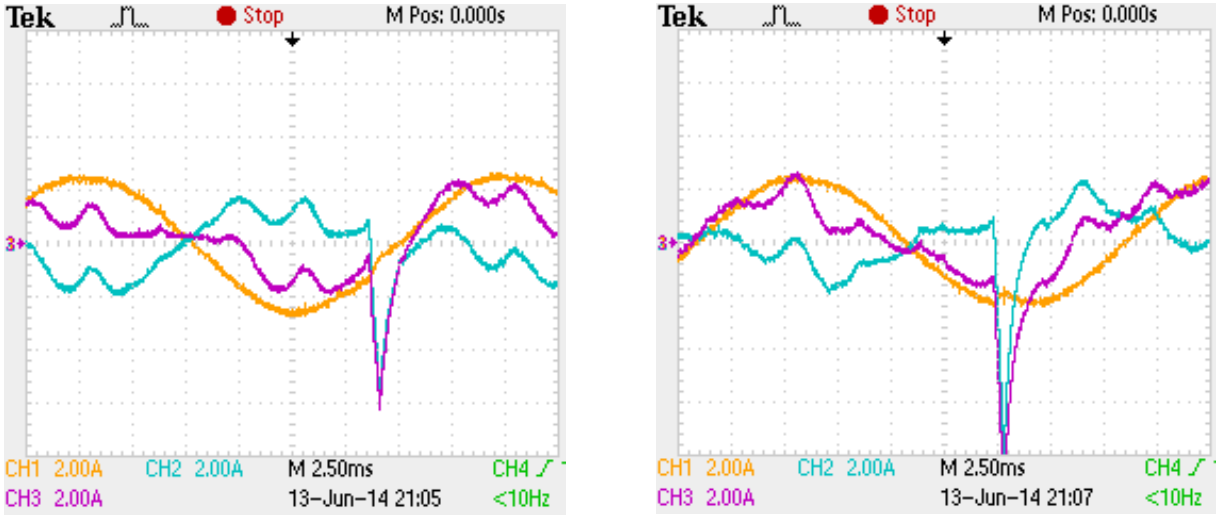

Figure 5-33 Reference Modification, Phase A Currents, CH1: ia, CH2: ip, CH3: in

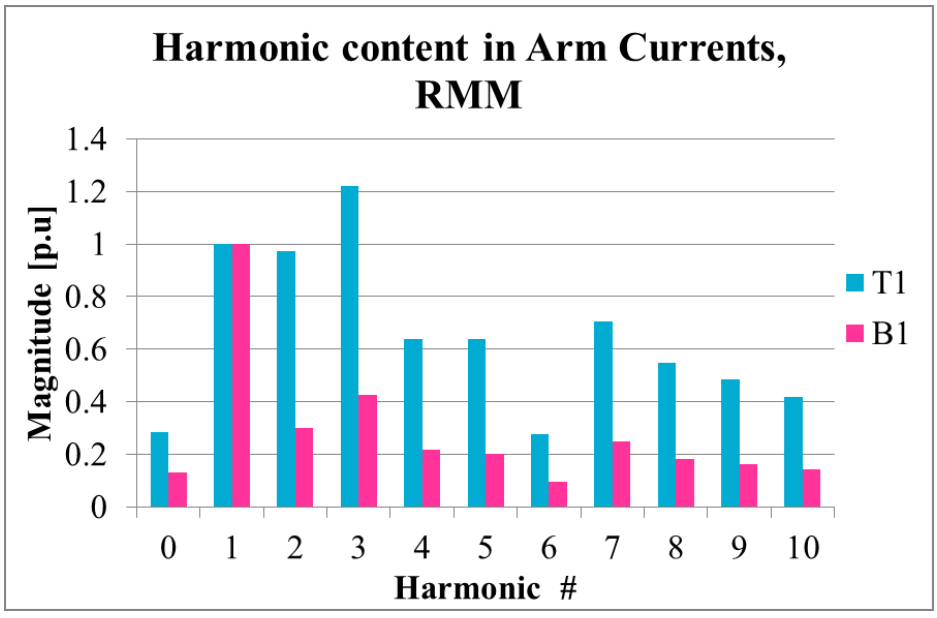

Figure 5-34 Harmonic Contents of Current in T1, RMM , Hardware Setup

The voltage supplies for the gate driver interface cards were no longer able to supply enough current for input voltages above 200V. A reason for this might be a leakage current from the gate driver cards into the circuit. Another possible source of error could be that the bypass of SM1 is not done in a proper way. The reason and a solution to limit these currents should be found in order to use this method for fault tolerant control.

In order to investigate the voltage difference between the two arms in phase A, the voltages across the arms were measured. The actual voltages across the arms have been measured previously, but the aim now is to evaluate if there is a major voltage difference between va_{01} and va_{02}. These two points were measured related to the DC link neutral, marked with the ground symbol in Figure 5-4. The voltages can be seen in Figure 5-35. The difference between these two voltages is very small and is not likely to cause the current peaks.

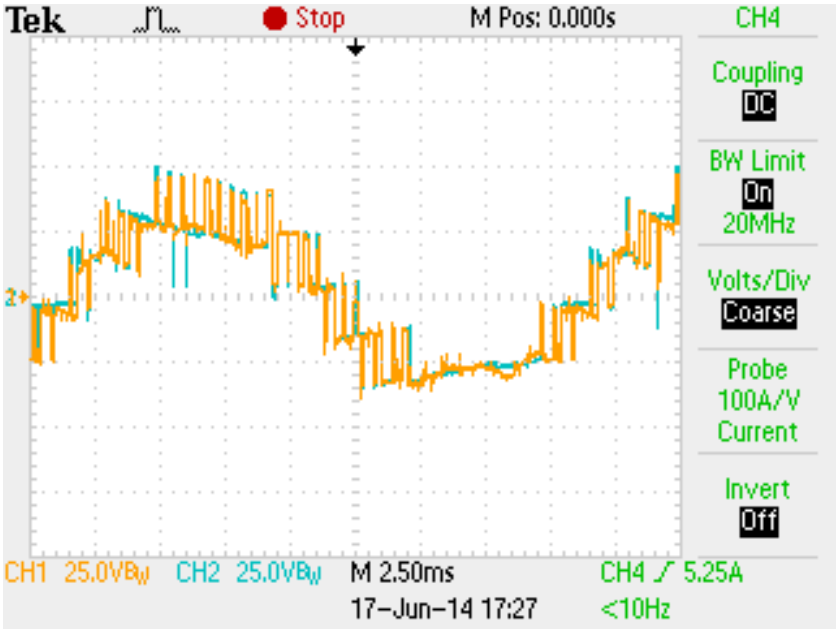

Figure 5-35 Arm Voltages, CH1:va_{01}, CH2:va_{02}

Figure 5-36 shows that the shape of the upper arm current changes in the period right before and right after one of the peaks. When higher order harmonics are present in the arm currents, the impedances for the capacitors and inductances present in the circuit changes

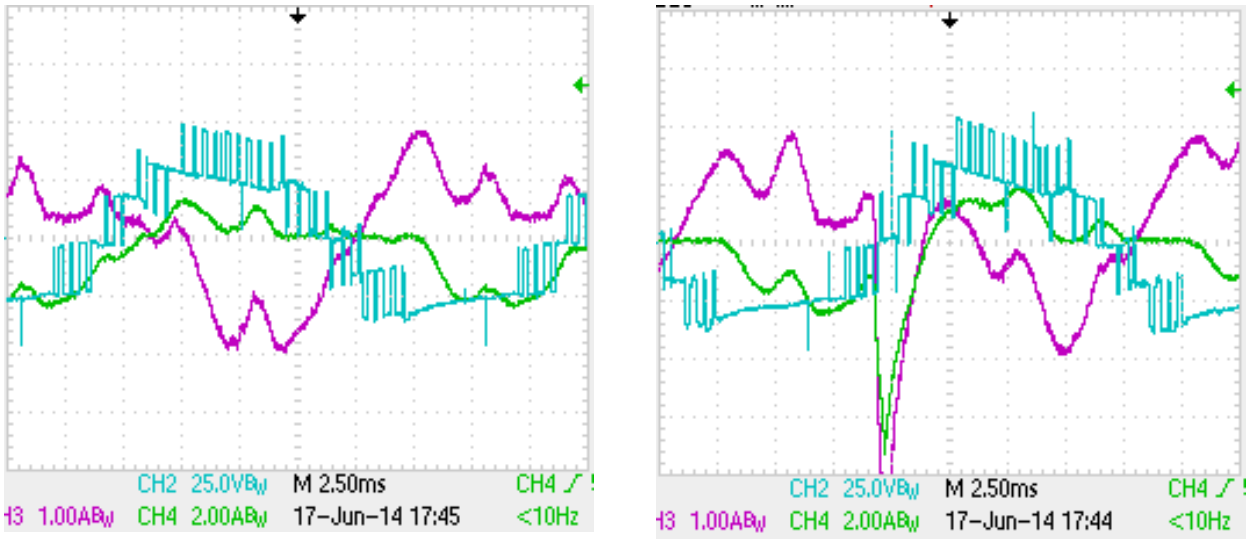

Figure 5-36 Arm Voltage and Currents, CH2: vcn, CH3:ip, CH4: in

The bypass of SM1 might not be correctly connected. The capacitor voltages with 100V. DC link and fault tolerant state are therefore investigated. It is expected that the capacitor voltage in SM1 will be approximately 7.5V. at all times. This is because it is charged by the gate driver interface card. Figure 5-37 shows that the capacitor voltage for SM1 has the expected value, and the rest of the voltages are balanced around 20V. Because the time constant of the SM circuit is approximately 155s, it is not likely that 7.5V in the capacitor can cause the arm current peaks.

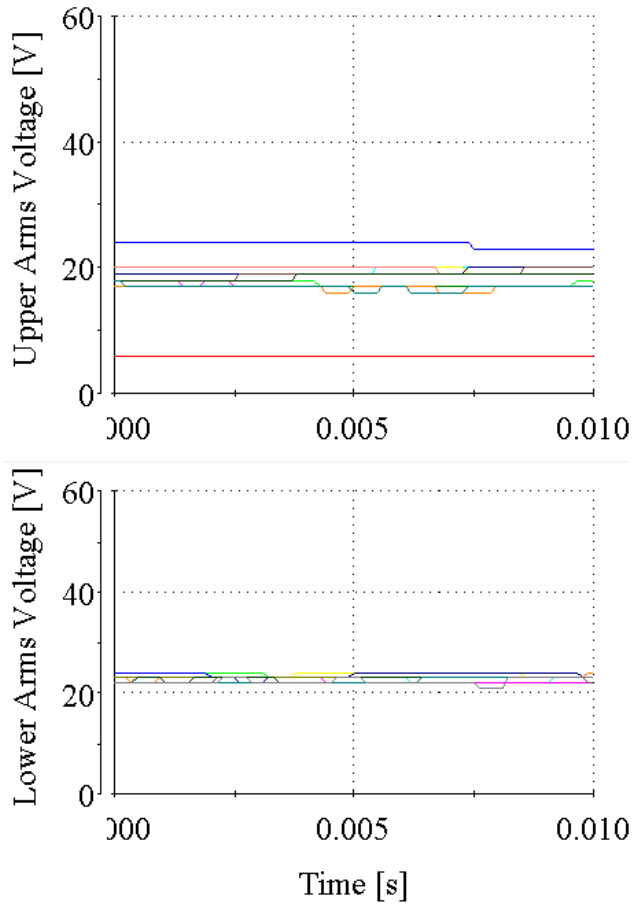

Figure 5-37 Capacitor Voltages during, RMM, 100V. DC

Figure 5-38 shows that before the current peaks appear, there is a deviation in the arm currents waveforms;

- negative current in B3 have a higher minimum point than the other currents at 0.0075s
- current in T2 have an even higher minimum point at 0.011s
- current in B2 stays positive for a long time
- current in T1 and B1 increase suddenly at 0.0175s

The current peaks increases very fast. This manner of increasing might be caused by a short circuit caused by the irregularities. Because of the time contraints of this project, the current peaks were not further investigated. For further work the control code should be evaluated to reveal if it is the reason for these peaks.

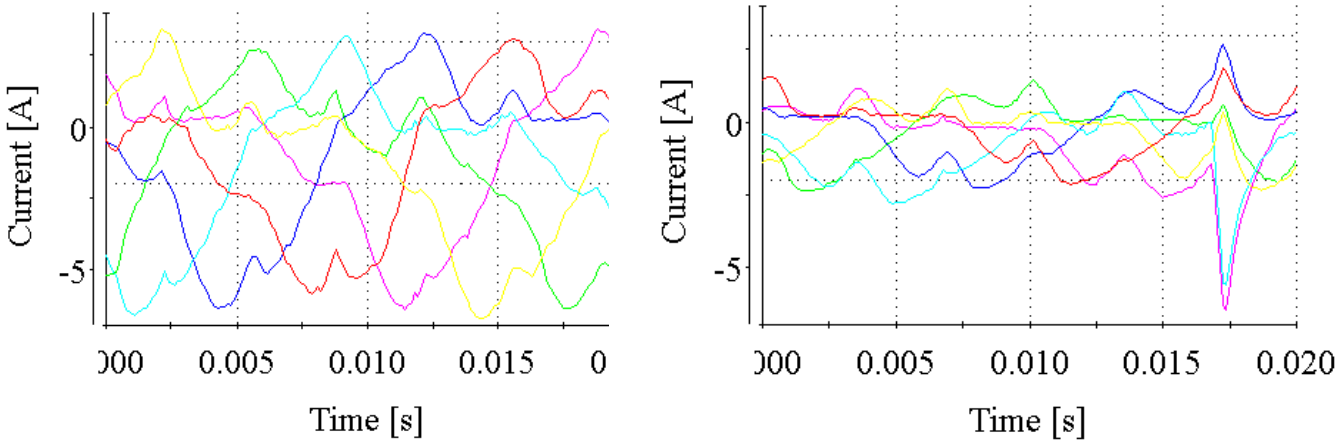

Figure 5-38 Arm Currents, a)Steady State, b) Fault Tolerant State, T1(■), T2(■), T3(■), B1 (■), B2 (■) and B3 (■),

Chapter 6

Comparison of Simulation and Hardware Results

Introduction

In this chapter, the simulation and hardware results will be compared. First a basis for comparison is presented in 6.1. In 6.2, a comparison between the steady state values and waveforms are presented. In 6.3, a comparison of the results with RMM implemented is included. In 6.4, the simulation results in steady and fault tolerant state is compared. This comparison is also done for the hardware results.

In order to evaluate the validity of the results obtained in this thesis, a discussion of the possible sources of error is presented in 6.5. In both a simulation and hardware setup, the accuracy of results have an impact on the validity, this is discussed in 6.6.

6.1 Comparison basis

The simulation model was run with the parameters presented in Table 4-1, and the hardware setup was planned to run with the same load equal to 27 Ω and 40mH per phase. The load resistance in the hardware setup was by mistake set to 12.3Ω The phase shift between current and voltage when the load was coupled in series with a three phase AC supply was 1.4ms which is equivalent to 0.4398rad when the fundamental frequency is 50Hz. The load impedance is calculated based on the measured currents and voltages in Eq. [6.1], [6.2] and [6.3], where V_{phase} and I_{phase} are the phase voltage and current and $|Z|$ is the phase impedance length.

$$\frac{V_{phase}}{I_{phase}} = |Z| \quad [6.1]$$

$$|Z|_{Simulation} = \frac{110}{3.65} = 30.56 = 27 + j13.01 \rightarrow 27\Omega \; and \; 41{,}4mH \quad [6.2]$$

$$|Z|_{Hardware} = \frac{90.6}{6.7} = 13.5 = 12.2 + j5.75 \rightarrow 12.2\Omega \; and \; 18.3mH \quad [6.3]$$

It can be seen that the voltage and current measurements corresponds well with basic circuit theory. In order to compare the simulation results with the hardware measurements, the simulation is run with the same parameters. The fundamental frequency components for the steady and fault tolerant state for phase voltages and currents will be presented here. These values will be used to compare with the Fourier analysis of the hardware measurements. Since the shape of the voltage and current waveform will be the same with these parameters, new waveforms are not presented. The result from the Fourier analysis is shown in Table 6-1 and Table 6-2.

Table 6-1 Fourier Analysis Steady State, 250V. DC-link 12.2Ω and 18.7mH

PARAMETER	PHASE A	PHASE B	PHASE C	LINE AB	LINE CA	LINE BC
Magnitude[V]	106.92	106.95	106.88	185.25	185.13	185.19
Magnitude[A]	7.74	7.74	7.74			

Table 6-2 Fourier Analysis Fault Tolerant, 100V. DC-link 12.2Ω and 18.7mH

PARAMETER	PHASE A	PHASE B	PHASE C	LINE AB	LINE CA	LINE BC
Magnitude[V]	42.83	42.72	42.55	74.2	73.91	73.73
Magnitude[A]	3.1	3.09	3.08			

6.2 Steady State Comparison

In this sub chapter, a comparison of the simulation model and hardware setup results in steady state will be presented. The simulation model was described and results presented in Chapter 4, whilst the hardware setup and results description was presented in Chapter 5. The comparison is focused on the Fourier analysis results. The main figures will be repeated here.

The phase and line to line voltages are repeated in Figure 4-11, Figure 5-22 and Figure 5-18. The time step in the simulation model is 5μs and 119.05μs for the hardware control. This means that for the simulation model, the PWM signals have a much higher precision than in the physical setup. The time step in the physical setup is the minimum for which the processor was able to compute the control signals in real time.

The phase and line voltages from the simulation can be seen in Figure 4-11, repeated below. The phase voltages have a slightly different shape than for the hardware results in Figure 5-18, repeated below. In the hardware result, the shapes of the peaks are more flat. A possible source of error could be that the load neutral point was grounded. If this was the case, the amount of voltage levels in the phase output would be five. The voltage levels are difficult to distinguish in Figure 5-18. If there were only five levels it is probable that the levels would be more distinct. In the laboratory, the load neutral is not grounded on purpose. One possibility is that since the chassis of both the resistive and the inductive load is grounded, this might impact the results since a ground current might be present. Other possible sources to this difference are the time step for which the control is run, or the oscilloscope measuring potential.

The line to line voltages in the simulation model also have a different shape than for the hardware results. In Figure 5-20, it can be seen that the amount of voltage levels in the line to line voltages are eight. This amount would be the same, either if the load neutral is grounded or not.

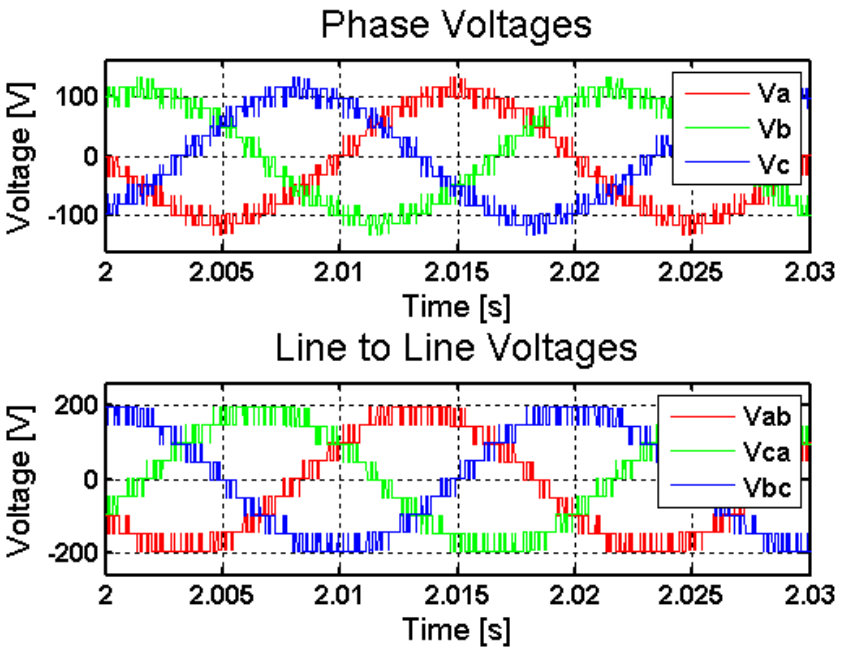

Figure 4-11 Phase and Line-Line Voltages, Steady State, Simulation Model

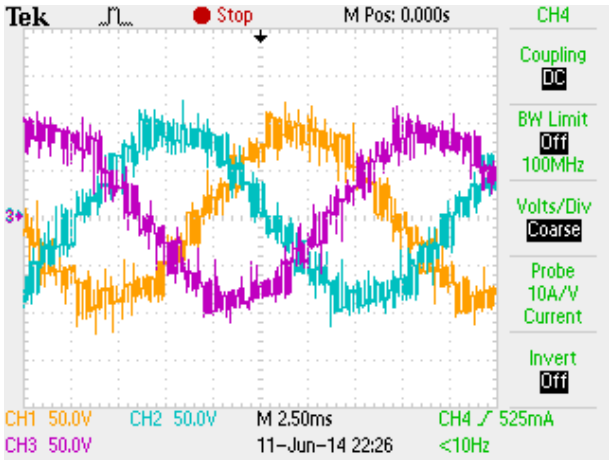

Figure 5-18 Phase Voltages, CH1:Va, CH2:Vb, CH3:Vc, Steady State, Hardware Setup

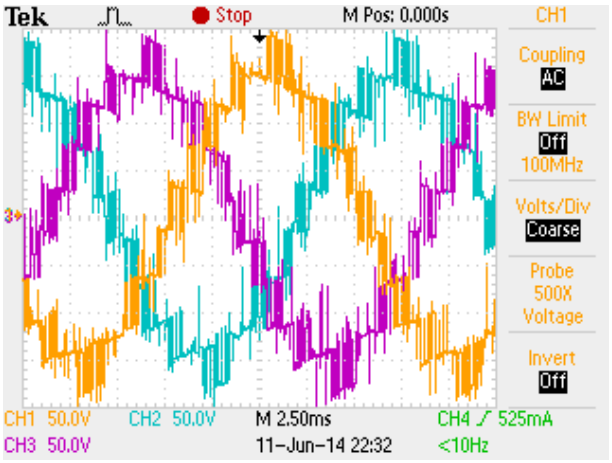

Figure 5-22 Line to Line Voltages, CH1:VAB, CH2:VBC, CH3:VCA, Steady State, Hardware Setup

In order to investigate the reason for the different voltage shapes, a comparison of the arm voltages is done. The simulation T1 and B1 arm voltage is shown in Figure 4-13. The arm voltages range between 0 and 250V whilst the phase voltage ranges between -125 and 125V. In Figure 5-20, the voltage across T1 and phase A in the hardware setup is shown. These voltages oscillate around the same neutral point. Since it is not possible with negative voltage across the capacitors, it is clear that the actual arm voltage should be shifted in magnitude. Based on these observations, the different shapes for phase and line voltages might be caused by the measurement potentials in the oscilloscope. To further investigate the reason behind this, the voltage between load neutral and DC-link neutral should be measured.

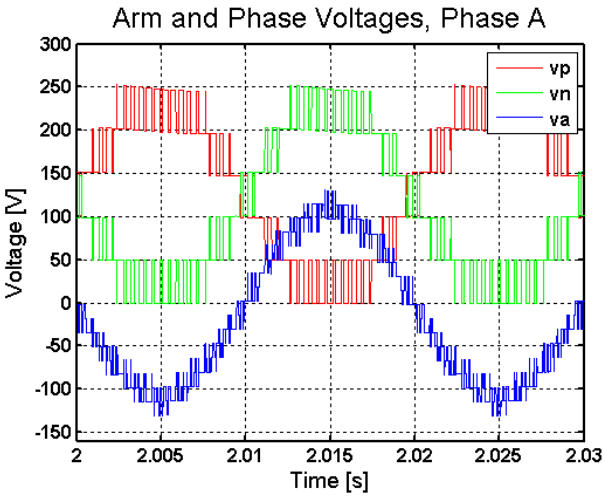

Figure 4-13 Arm and Phase Voltages, Phase A, Simulation Model

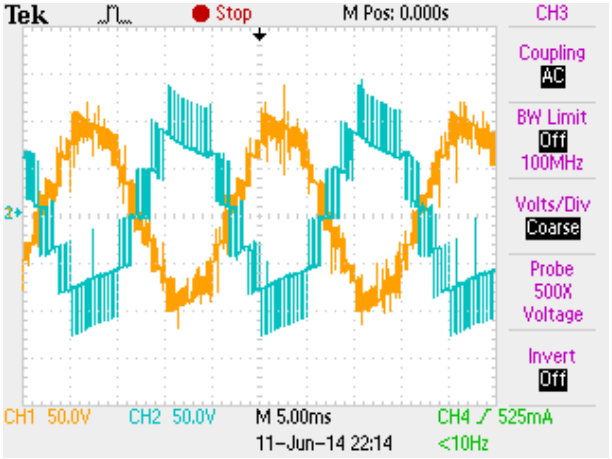

Figure 5-20 Upper Arm and Phase A Voltages, CH1:Va, CH2:vcp, Steady State

The voltages fundamental frequency magnitudes are compared and the result can be seen in Table 6-3. There is a magnitude difference of approximately 15 % between the simulation and hardware result. One of the possible sources of error is the estimated arm resistors added in the simulation model. This resistor is 1Ω. Based on these results, the resistive losses in the wiring might be larger than expected. Another central cause of error is the actual load inductance value inserted in the physical setup. An old step less adjustable inductance is used. Since it has an iron core, the available RLC meters was not able to supply enough current to magnetize the core. The inductance was therefore measured by the phase delay it caused when the three phases with load was connected directly to an AC voltage source. The phase angle was measured using the cursor function in the oscilloscope. Since the cursors are adjusted by hand, the phase angle measured could differ from the actual phase angle in the circuit. The inductance is very old, so leakage currents could exist and create a different inductance when higher voltage is applied. The inductance was measured with 70V 50Hz AC supply.

Table 6-3 Hardware Percentage Deviation from Simulation, Voltages, Fourier Analysis, Steady State

PARAMETER	PHASE A	PHASE B	PHASE C	LINE AB	LINE CA	LINE BC
Voltage Deviation	-15.3 %	-14.4 %	-14.2 %	-14.7 %	-14.4 %	-16.0 %
Current Deviation	-13.4 %	-12.1 %	-13.4 %			

The shapes of the phase currents are approximately equal, and can be seen in Chapter 4 and Chapter 5. The percentage change in amplitude between the simulation results and the hardware results can be seen in Table 6-3. The current increase between the two setups is approximately 13 %. The arm currents in the hardware setup have a larger 6^{th} order harmonic than in the simulation model. The cause of this component is probably that the arm inductance is not properly dimensioned for the setup. This should be investigated in further work on this topic.

6.3 Reference Modification Comparison

In order to investigate the behavior of the simulation and hardware setup with the RMM implemented, both the voltage and current measurements are compared in this subchapter. Unexpected arm current peaks in T1 were observed in the hardware setup, and the voltage is therefore limited to 100V in the DC-link.

The phase and line fault tolerant voltage measurements for the simulation model is repeated here in Figure 4-18. And the voltage measurements from the hardware setup are repeated in Figure 5-30 and Figure 5-31. The shape difference in the fault tolerant state is the same as described for the steady state in 6.2. The phase voltage waveforms for the hardware setup are not properly balanced. It can be seen that the particularly phase A is distorted for the lower voltage values. This is the RMM compensated period of the waveform. Because of the arm current peaks, the voltage waveforms were not expected to meet the requirements in the fault tolerant state.

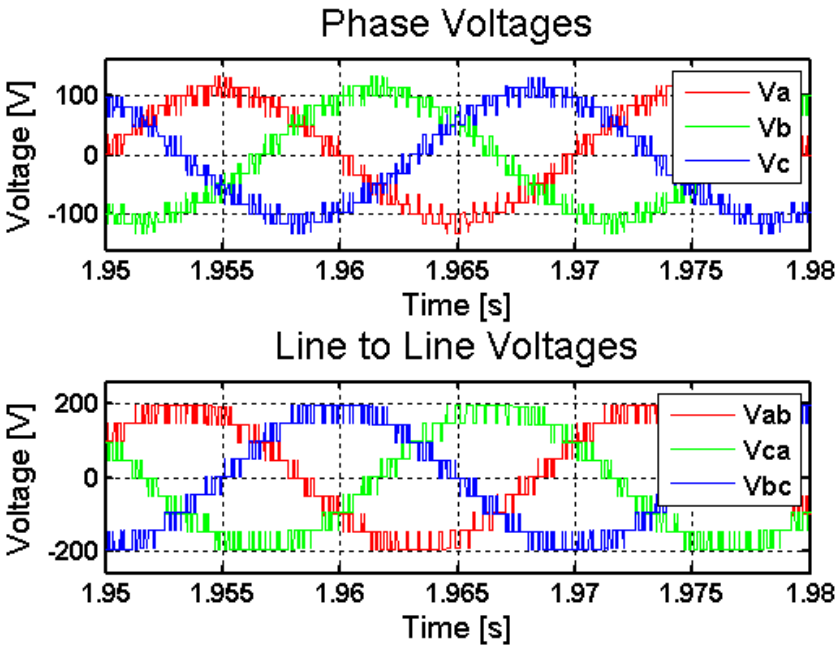

Figure 4-18 Phase and Line-Line Voltages, All Phases, RMM

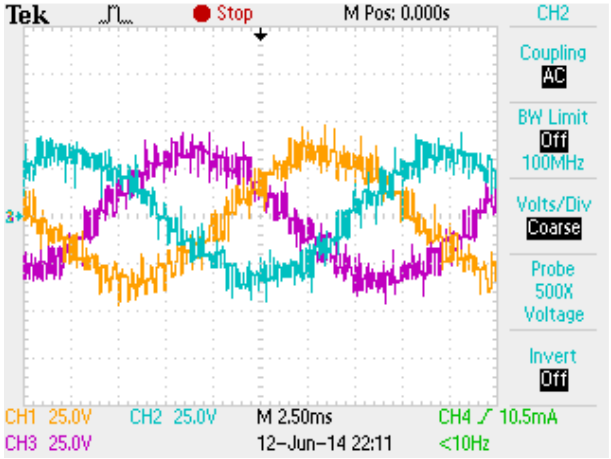

Figure 5-30 Phase Voltages, CH1: VA, CH2: VB, CH3: VC, Reference Modification

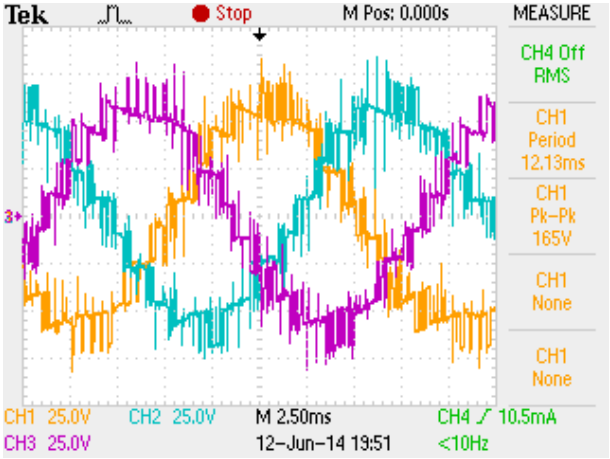

Figure 5-31, Line to Line Voltages, CH1:VAB, CH2:VBC, CH3:VCA, Reference Modification

The fundamental voltage difference between the simulation and hardware result is approximately 20 %, in contrary to 15 % for the steady state results. It is assumed that the main cause of the larger difference is the unexpected current peaks causing larger losses in the circuit.

Table 6-4 Hardware Percentage Deviation from Simulation, Fourier Analysis, RMM

PARAMETER	PHASE A	PHASE B	PHASE C	LINE AB	LINE CA	LINE BC
Voltage Deviation	-20.6 %	-20.6 %	-18.9 %	-18.9 %	-18.4 %	-18.9 %
Current Deviation	-12.9 %	-15.9 %	-15.6 %			

The arm voltage waveforms are similar for the simulation model and the hardware setup in fault tolerant state, and are therefore not repeated here. The comparison between phase current magnitudes is presented in Table 6-4. They deviate with approximately 15 %, but the deviation is lower for phase A. This result indicates that some of the arm current should have supplied the load is dissipated in the circuit. This dissipation can be seen in the arm current peaks, discussed in 5.8.2.1.

6.4 Comparison of Steady and Reference Modification State

In this section, the steady state results from both the simulation model and the hardware setup are compared with the fault tolerant state. The comparison is based on the fundamental frequency magnitude calculated by Fourier analysis. The simulation comparison is presented in Table 6-5. It can be seen that the difference in magnitude for the fundamental frequency is very small.

Table 6-5 Comparison Steady State versus RMM, Simulation Model

PARAMETER	PHASE A	PHASE B	PHASE C	LINE AB	LINE CA	LINE BC
Steady State [V]	110	110	110	190	190	190
RMM [V]	110	110	110	190	190	190
Deviation from Steady State	0. %	0 %	0 %	0 %	0 %	0 %

In order to compare the results in steady state with the results from the reference modification method, the magnitude values are scaled to the DC-link voltage level. The difference in magnitude based on this computation can be seen in Table 6-6, and is from 4.8% to 7.4 %. In a physical setup, the voltage level impacts more than just the voltage. One example is the wires resistances which increase with temperature. With an increased voltage, the current increases as a consequence. This leads to higher losses and higher temperature in the wires. This kind of analysis is therefore more reliable for simulation results. The voltage magnitudes decreased for all three phases, even though the arm current peaks are only present in phase A.

Table 6-6 Comparison Steady State versus RMM, Hardware Setup

PARAMETER	PHASE A	PHASE B	PHASE C	LINE AB	LINE CA	LINE BC
Steady State Magnitude/250	0.36	0.37	0.37	0.63	0.63	0.62
RMM Magnitude/100	0.34	0.34	0.35	0.60	0.60	0.60
Deviation from Steady State	-6.18 %	-7.38 %	-5.94 %	-4.81 %	-4.83 %	-3.92 %

6.5 Sources of Error in Simulation and hardware Setup

This section is included to summarize the sources of error for the tests done throughout this project. Sources of error are mentioned in the text when necessary. In order to give a better insight of the results validity, they are also reviewed in this subchapter.

The simulation model is made in Simulink and SimPowerSystems. During the work with this project, the mathematical equations behind these models have not been investigated. The models which the SimPowerSystems components are based on have a great impact on the validity of the results. The results could be valid for some applications, and not for others. Since a simple system with a DC-link and a passive load is investigated, it is assumed that the basis behind the software components is good enough for this purpose. It is also a well proven simulation tool.

Another possible source of error for the simulation results are the possibility of measuring in one location, and presuming the measurement is done at another. The risk of doing this is small because the voltage and current measurements are observed many times, and a possible mistake would probably be discovered.

The hardware setup has multiple sources of error. It is a complex setup with numerous wires and connections which could potentially have bad contact or be coupled to the wrong point. Many of the malfunctioning connections and wires were removed during the fault testing part of the project, however some can still remain. When the voltage measurement boards were included in the setup, they had several faults. One of them had a short circuit which led to an output of 14V. when only the supply voltage was connected. Similar faults can damage the control equipment, and attention should be paid to these cards in further use of the setup. Also, many of the soldered points in these cards have a bad contact. Faults in the voltage measurements may create a fault in the arm voltages which would propagate to the load voltage.

In order to have proper measurement values in the control system, they are coupled to BNC contacts and further to the dSPACE connector panel. Even though the measurements done by the LEM module cards and are correct, there could be interference between the signals before the measurements have reached the connector panel. The risk of interference would be higher

when the setup is run at higher voltage levels. Interference can also distort the control signals before they reach the IGBTs. To lower the risk of this, low-pass filters are included in the Gate Driver Interface cards. The cables between these cards and the distribution board carry digital TTL signals in flat cables. These cables are quite long, and the possibility for interference is quite large. For future use, shielding of these cables should be considered.

The values of the components included in the setup are also possible sources of error. The capacitors have not been used before in a setup, it is therefore assumed that the accuracy of these values is higher than for the other components. The arm inductors were used for the previous construction and there is a possibility that they have been affected by something during the time connected to the setup. The load components are old, and the actual values could differ more than usual for higher currents. The load resistor would heat up if the setup is running for a longer period of time. The load inductor value is set by adjusting the step less length of an air gap. To measure the inductance, a three phase AC source was connected in series with the load resistor and inductor. The phase angle was measured by oscilloscope, and the inductance calculated by this result. The phase angle is measured by using the cursor function, and adjusting by hand which is a large source of error. Since the air gap length is step less, it might vary if touched, with or without purpose.

6.6 Accuracy of Results

In order to discuss the accuracy of the simulation results, the deviation from the ideal reference waveforms to the actual output is investigated. This is performed by subtracting the reference waveform in the upper arm of phase A from the actual voltage measured across this arm in the simulation model. The result can be seen in Figure 6-1, to the left a) with a 250V. DC-link and load equal to 27Ω and 40mH and to the right b) with 12.2Ω and 18.7mH. The 50Hz component of this signal is found, by the Power Gui FFT Analysis Tool, to have a magnitude of 3.172 V for a) and 6.902V for b). It is clear that a larger inductance reduces the voltage ripple.

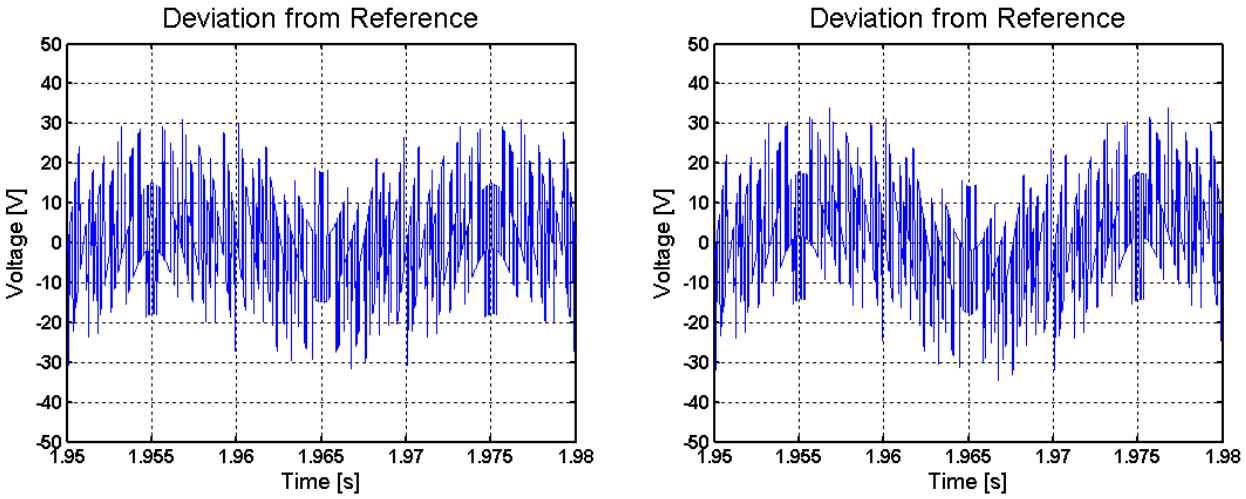

Figure 6-1 Deviation from Reference waveform, a) 27Ω and 40mH b) 12.2 Ω and 18.7mH, Phase A, Steady State, Simulation Model

The calculation of the deviation between the reference value and output value for the hardware setup is not performed due to time limitation. The accuracy of the hardware measurements is dependent on the measurement equipment. The equipment list is presented in Table 5-2 on page 43. The measurements taken by the oscilloscope used either a differential probe or a current clamp. Both types of measurements are affected by the length of the wire connected to the measuring point. A further analysis of the accuracy of the hardware setup should be performed to ensure the validity of the results.

Conclusions

The work on this thesis has included an investigation of the Modular Multilevel Converter (MMC). A new fault tolerant control method has been developed, based on an idea of modifying the reference waveforms to maintain balanced line to line voltages. The investigation of the method has been performed theoretically, by computer simulation and laboratory tests.

Theoretically the Reference Modification Method (RMM) has proven valid to the extent investigated in this report. The commercial value of the method is assumed to depend greatly on the amount of Sub Modules (SM) present in the design. For larger numbers of SMs, the period to be compensated becomes smaller per faulty SM. The amount of SMs that can be bypassed should be calculated in further investigation of the method. This number could be a percentage of the total amount of SMs in the converter. Based on the results in this thesis, this percentage will be smaller than 33%, for an arm modulation index equal to or greater than 0.95.

The computer simulation results indicate that the voltages and currents remain balanced when the new method of fault tolerant control was implemented. A detailed analysis of accuracy was not performed, but the measurements in the model showed no deviation for voltages $\pm 1V$. The steady and fault tolerant state phase and line voltages had equal magnitudes and a 120° phase shift for the fundamental frequency.

The load neutral point voltage potential deviation from the DC-link neutral is assumed to impact the phase voltages during fault tolerant state to a great extent. In the case investigated, the load neutral is not connected to ground. The fluctuations in the phase voltages are eliminated in the computer simulation results, and this is assumed to be related to the choice of ground point.

The prototype configured during the work with this thesis has given satisfactory results in steady state. Although, the harmonic spectrum for the phase voltages and arm currents should be improved in order to use the setup for verification of the method. The arm currents have a significant 6^{th} order harmonic component which is assumed to be caused by under dimensioned arm inductors. A detailed analysis of the accuracy of the hardware measurements should also be done in order to document the behavior of the converter.

Steady state values from simulation and hardware differ with approximately 15 %. This deviation could be caused by underestimation of the resistive losses in the hardware circuit, the 6^{th} order harmonic in the arm currents or the higher harmonic content in the output voltages. Other possible sources of error should also be investigated especially if improvements in these factors do not lead to a smaller or acceptable deviation.

The fault tolerant control was run on the hardware. The arm voltage measurements show the expected shapes and amplitudes in the faulty phase related to the control implemented. The phase voltages show a deviation by 6-7 % from the steady state values and the line voltages a deviation of 4-5 %. An unexpected peak in the arm currents in the faulty phase was observed. These peaks were not periodic, and had varying peak amplitude. They could be caused by either hardware or software errors. The hardware setup should be further investigated to reveal the cause behind these current peaks.

Further Work

This thesis work has investigated the feasibility of a new fault tolerant control method for component failures within the MMC circuit. Further work on this topic should involve evaluation of the simulation model. The control algorithm should also be tested in a model where the input and outputs of the converter is not constant. In addition an accuracy analysis should be performed in order to make further conclusions on the results obtained in this thesis.

The prototype parameters should be evaluated and improved in order to verify the method on this setup. Particularly, it is likely that the arm inductors do not have the proper inductance in relation to the rest of the setup. There are also some improvements to be made on the current and voltage sensors in order to obtain better accuracy in the results.

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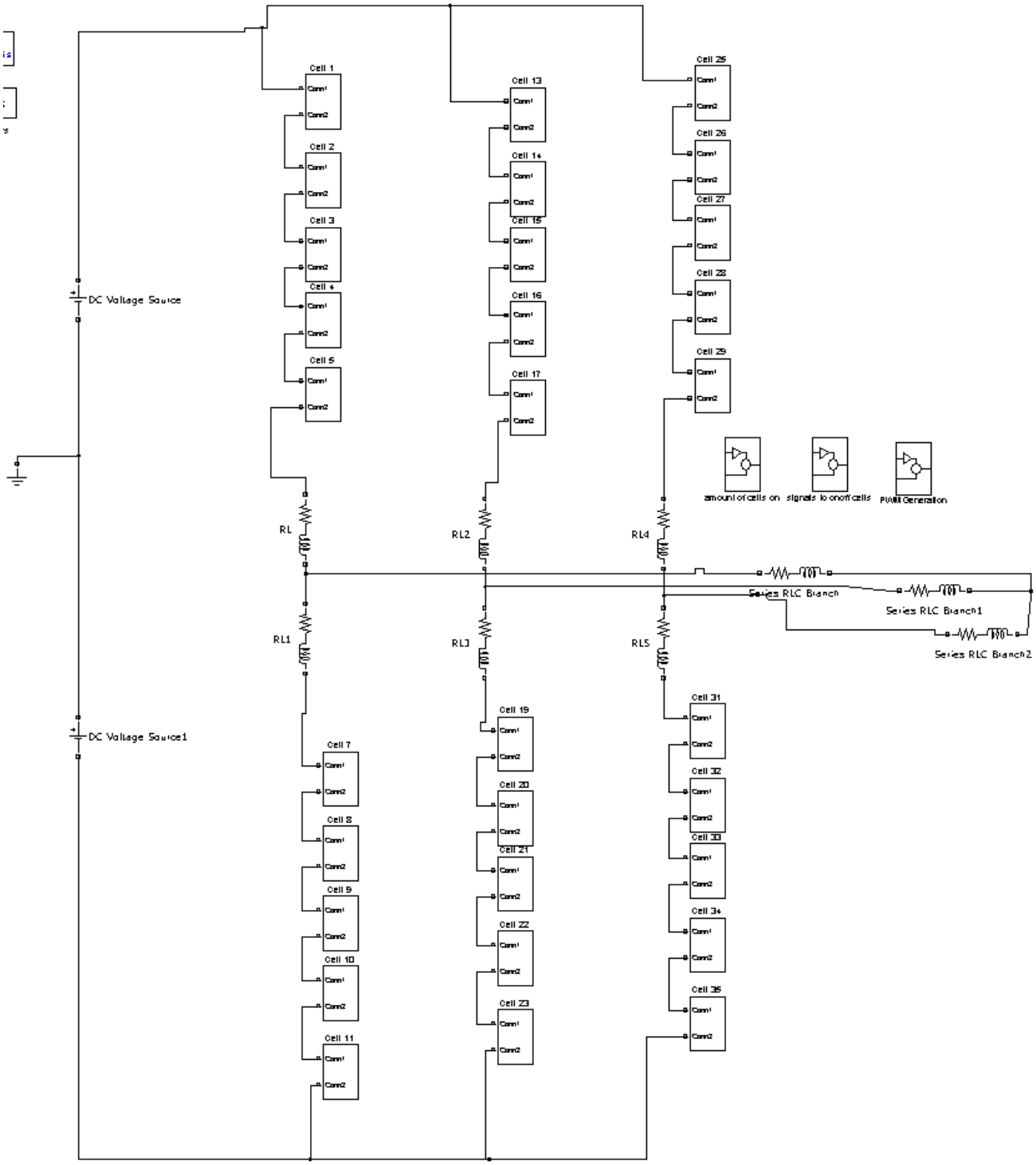
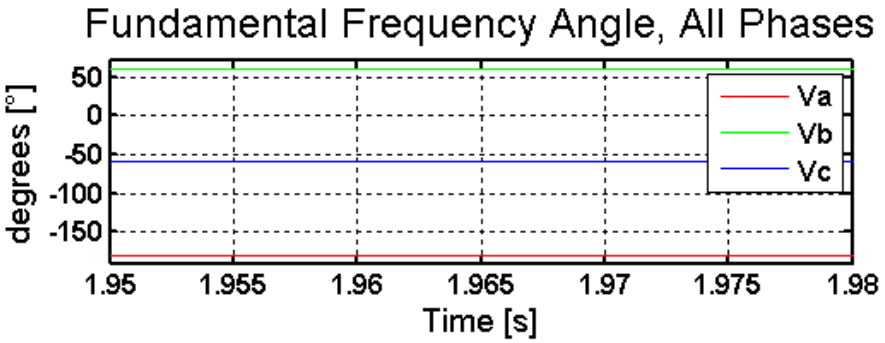
Appendices

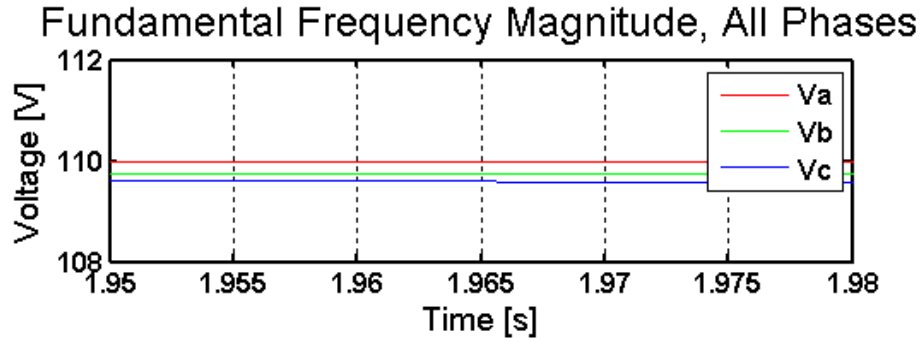
Appendix 1 Simulation Model Topology

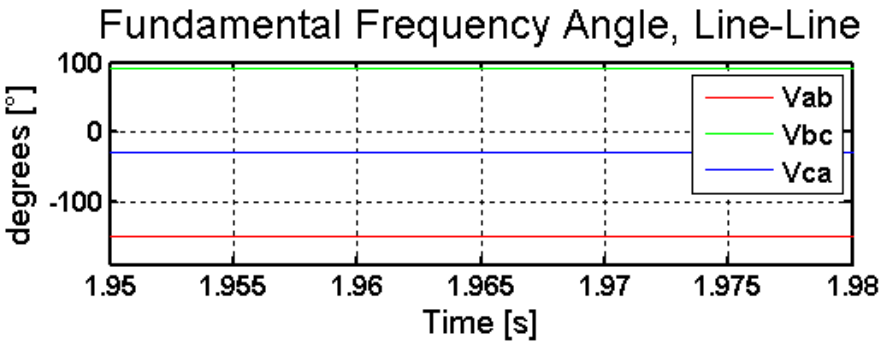


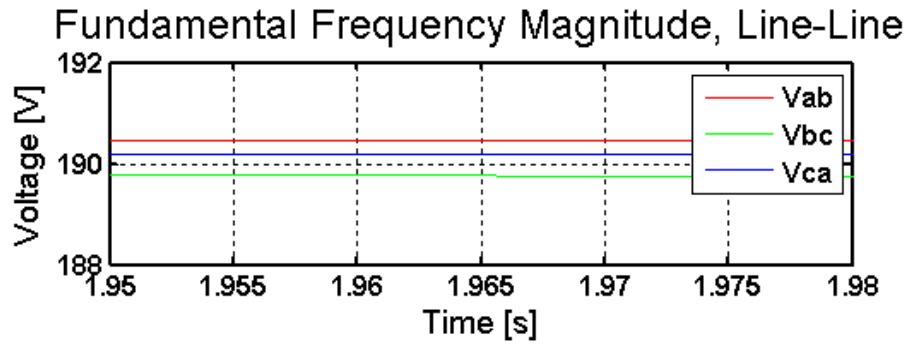
Appendix 2 Fourier Analysis of Simulation Results

Fundamental Frequency Phase Voltages and Line to Line Voltages, All Phases, RMM

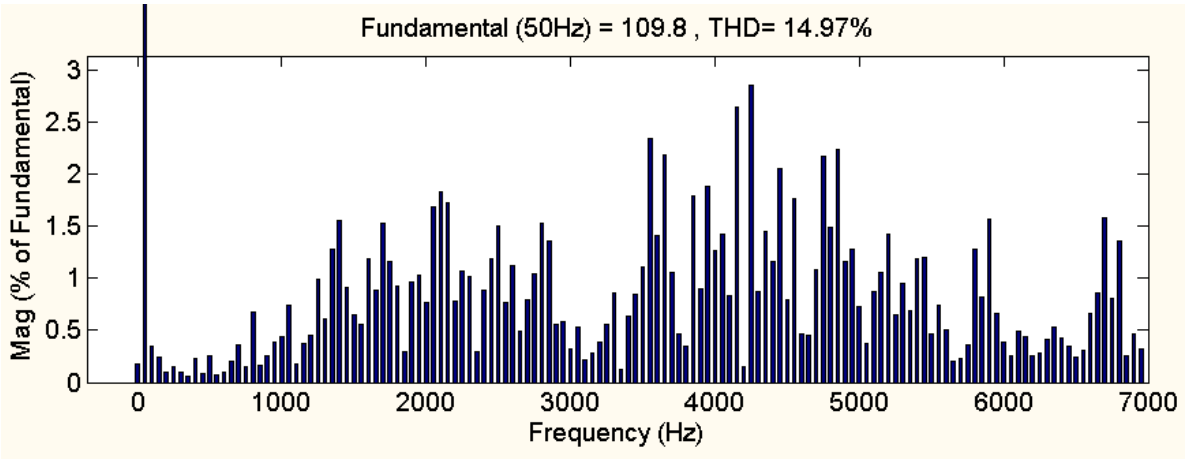




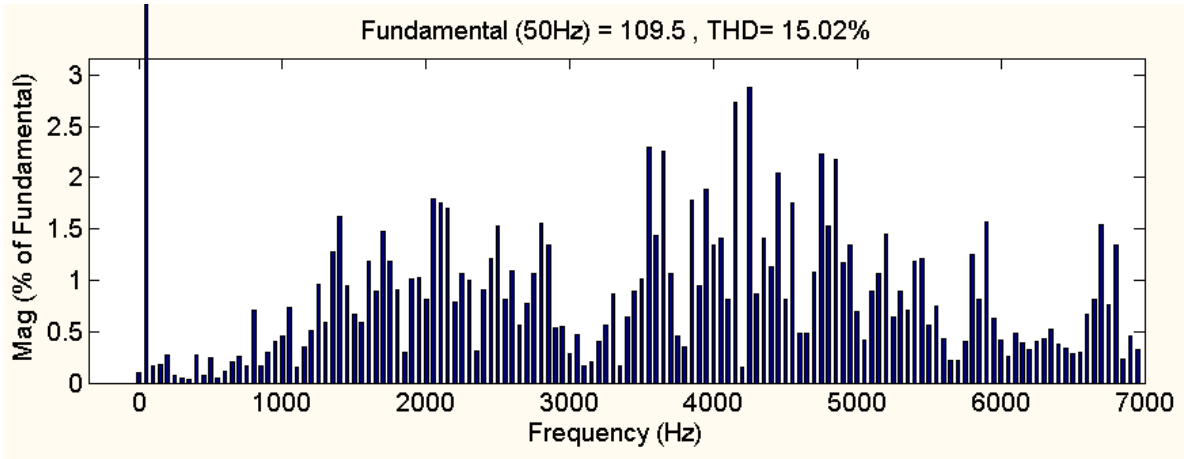




Phase B: Frequencies up to 7000Hz, RMM:



Phase C up to 7000Hz, RMM



Appendix 3 Fourier Analysis of Hardware Steady State

Voltages, Steady State, DC-link=250V. Hardware setup:

Steady State Hardware Result, 50 Hz Fundamental Frequency 250V. Dc-link and 27Ohms and 40mH load per phase													
		A		B		C		AB		BC		CA	
H	F	Mag.	Angle	Mag.	Angle	Mag.	Angle	Mag.	Angle	Mag.	Angle	Mag.	Angle
0	0	970	180.0	3358	180.0	5982	0.0	3420	180.0	6420	0.0	1258	180.0
1	50	90619	105.2	91454	-136.5	91688	-14.6	158092	132.8	158412	12.1	155562	-107.8
2	100	3020	-78.8	2466	66.2	1619	160.6	3042	-55.4	2979	-142.2	4398	81.4
3	150	1217	-81.6	1308	99.6	822	42.3	2338	-49.8	1659	-153.3	2709	102.8
4	200	323	-59.8	924	21.6	982	-179.6	3532	-117.9	1866	-24.5	3739	88.4
5	250	3590	-70.5	2657	164.5	2616	67.7	4941	-102.2	4461	13.8	4721	118.8
6	300	940	115.3	326	-129.0	621	-46.7	1618	-84.4	1698	152.6	2080	28.8
7	350	710	80.3	996	-147.6	1113	-7.4	2469	131.4	2808	24.6	2924	-94.3
8	400	516	-75.7	545	107.3	176	-169.8	1776	-64.2	1129	-177.4	1703	83.9
9	450	370	-8.9	458	26.8	880	-160.4	1007	-58.0	1021	-132.0	1249	105.5
10	500	867	-63.2	999	169.4	1293	70.7	1860	7.0	812	144.1	1417	-139.1
11	550	1937	-25.9	1689	-157.0	1365	108.9	3591	-58.0	2213	69.3	3039	161.7
12	600	962	-177.6	847	56.5	731	-49.4	631	68.2	1317	-119.8	630	60.8
13	650	379	124.2	289	86.8	757	-54.6	1305	64.2	1347	-83.4	647	162.7
14	700	508	-78.2	211	78.3	312	108.8	376	-1.6	1686	-135.1	842	62.4
15	750	515	-87.8	359	155.0	318	-35.1	1269	-33.0	2037	-177.0	845	4.1
16	800	1263	-36.3	925	-176.8	635	93.9	1879	22.2	1737	166.8	1550	-88.4
17	850	867	1.5	116	-119.4	826	-172.3	2695	-67.4	946	77.3	1573	137.9
18	900	847	156.4	593	94.2	1179	-41.9	877	-111.9	3117	-146.5	4702	40.8
19	950	2061	-0.2	2839	107.4	2962	-108.0	3687	-6.9	4304	-130.5	3818	98.5
20	1000	2821	-169.5	1807	-33.9	2209	50.9	3746	173.3	3262	57.2	3472	-62.7
21	1050	1632	-171.9	1012	-1.4	383	18.0	1899	164.3	811	46.1	2006	-39.7
22	1100	2068	-163.3	1201	13.0	704	20.2	1458	146.3	851	-142.2	1484	-13.0
23	1150	2484	-175.8	1703	34.9	1197	-25.9	3455	123.9	2578	-142.8	4060	-13.7
24	1200	794	5.8	2701	-98.7	2996	103.6	4449	-80.9	4080	69.5	1893	159.2
25	1250	947	-147.5	1179	-52.9	1358	99.0	2555	167.5	3693	40.2	3111	-96.8
26	1300	1895	-0.2	1866	134.0	1977	-117.1	3102	-5.9	2861	-125.7	3352	114.8
27	1350	740	0.9	489	111.9	391	-139.1	798	35.8	546	-129.1	810	146.6
28	1400	726	-3.8	640	173.6	765	157.3	1112	52.6	1254	-179.0	609	-74.1
29	1450	1454	-158.9	1702	72.7	1243	-63.2	1584	164.1	1442	-58.2	648	60.9
30	1500	2204	17.7	1422	-108.9	1905	161.5	2533	-67.9	4296	34.3	3675	172.0
31	1550	958	161.5	1521	-54.7	975	102.0	1975	-85.3	913	80.0	681	99.1
32	1600	1315	38.1	1134	150.8	1295	-106.4	2830	-27.8	1705	-129.5	3417	109.1
33	1650	537	35.2	210	45.1	978	-150.2	1637	-26.4	306	-133.3	1429	146.2
34	1700	346	-71.4	109	-156.2	192	122.9	657	-50.3	339	-162.6	708	142.7
35	1750	406	92.5	190	2.1	163	-38.4	1120	-31.0	378	66.0	1165	137.4
36	1800	1511	-77.6	1453	133.8	1338	44.7	2374	-173.0	2658	-58.9	2356	52.9
37	1850	509	-134.7	505	61.5	666	83.6	1039	-118.1	405	-73.9	1245	85.6
38	1900	552	48.9	1063	138.7	1443	-55.9	1093	-33.3	2486	-107.0	3430	82.1
39	1950	217	-15.5	499	-106.7	689	147.8	1303	-39.3	1028	145.8	772	126.4
40	2000	736	-151.0	935	-22.7	725	100.8	1621	-83.8	1683	106.7	415	27.3
41	2050	662	41.5	105	-105.1	685	-127.5	735	-5.1	400	-160.9	483	143.8
42	2100	1589	-39.4	1637	167.6	1123	67.9	2041	-173.7	2589	-64.1	2631	58.2
43	2150	1340	19.8	807	-144.4	55	-169.9	1792	-59.8	1400	-87.6	2951	109.4
44	2200	2104	-34.4	1394	49.5	2421	-171.7	3679	-92.2	4234	121.6	2418	-2.7
45	2250	305	-147.6	486	134.7	477	-0.1	322	75.8	1478	-109.9	1068	66.4
46	2300	139	-27.7	345	147.5	229	-142.1	508	35.7	705	-78.1	811	175.2

47	2350	451	34.1	206	-91.5	54	116.7	258	67.3	599	-110.6	411	86.7
48	2400	899	-9.6	748	-147.3	789	123.9	1712	-118.7	946	-17.8	2348	100.3
49	2450	320	70.9	193	129.7	642	-91.5	495	-77.1	849	115.9	692	-96.5
50	2500	1278	24.4	428	58.5	1740	-130.2	2816	-54.3	2767	143.0	746	21.9
51	2550	829	-123.8	685	96.4	559	-2.1	763	-148.2	968	-47.2	1242	71.3
52	2600	635	-139.5	523	28.7	375	35.5	661	-91.1	580	160.4	491	49.6
53	2650	930	134.2	629	166.9	1196	-25.1	1125	53.3	1223	-37.1	2188	177.1
54	2700	2374	137.0	1898	15.0	1804	-82.3	3518	10.0	2549	119.5	4101	-139.2
55	2750	386	-42.5	901	-139.5	884	77.7	762	147.2	2402	-64.4	2050	95.2
56	2800	392	77.6	1528	-131.0	880	36.8	1256	78.7	2646	-63.0	2547	132.5
57	2850	362	15.3	164	21.4	570	177.9	1027	-136.5	478	-36.7	871	56.9
58	2900	586	-13.9	63	-46.7	637	131.5	1169	-121.0	606	-88.8	1447	69.7
59	2950	260	91.0	1071	-143.9	839	4.7	173	103.7	1882	-8.5	1550	158.0
60	3000	1071	45.1	881	-118.0	474	156.0	1301	-135.0	2000	-12.7	1362	107.6
61	3050	535	167.1	191	140.0	308	-0.4	897	109.5	976	-114.4	727	103.7
62	3100	936	147.1	934	-72.1	832	8.8	1099	29.4	366	-56.9	1161	157.8
63	3150	1428	-43.9	1433	148.1	122	63.5	2575	-124.0	669	-23.8	2319	62.1
64	3200	776	24.5	489	-177.0	155	-58.5	1221	-121.8	351	14.4	1430	64.2
65	3250	828	-22.7	750	77.4	1062	-153.0	2466	-94.0	981	168.8	2447	52.0
66	3300	1014	40.1	423	-110.5	956	-143.4	1938	-96.1	698	23.5	1949	96.2
67	3350	459	-136.1	820	112.7	885	-28.8	558	43.6	1408	-176.6	1428	5.4
68	3400	676	53.9	692	176.9	572	-43.6	1086	-61.0	1647	-166.7	1702	31.9
69	3450	390	-55.1	363	-4.6	759	104.1	943	162.5	1271	-16.9	630	-128.0
70	3500	340	41.5	211	-138.6	76	-71.5	426	-103.5	222	79.1	461	128.8
71	3550	849	52.1	435	-86.5	439	-132.5	1735	-112.1	381	37.9	1549	64.3
72	3600	2261	54.1	1556	-78.6	1107	-157.7	3180	-107.8	1937	-4.3	3290	99.3
73	3650	3670	-122.3	4474	123.3	4283	-4.1	6306	48.4	8199	175.9	6687	-57.8
74	3700	402	35.6	2540	147.9	2958	-20.8	2710	-8.9	4888	-178.0	2369	22.7
75	3750	5476	-113.5	4468	12.6	4565	126.6	9198	119.5	7174	3.8	8552	-112.8
76	3800	1764	-111.9	1177	49.2	1413	93.8	2439	112.2	1165	13.7	2477	-109.1
77	3850	1379	-100.1	955	64.0	835	79.0	1482	124.9	480	5.5	1583	-72.8
78	3900	1579	-107.5	1111	90.3	919	65.8	2150	95.8	452	138.6	2192	-85.5
79	3950	3225	79.5	4187	-45.2	3405	-168.2	6276	-109.2	6231	5.7	6434	125.1
80	4000	309	38.3	589	-38.7	817	-173.6	297	164.9	1338	-15.2	822	176.9
81	4050	409	83.0	431	122.7	732	-71.7	939	-95.2	695	142.9	929	44.0
82	4100	382	-7.9	117	52.6	558	-171.2	418	159.6	542	48.5	617	-102.1
83	4150	541	-82.0	147	169.8	521	161.5	660	138.5	435	-13.7	263	-90.8
84	4200	552	-79.0	479	93.4	54	-27.2	505	131.9	467	-69.0	330	109.5
85	4250	5511	109.1	5416	-20.3	4985	-130.2	8519	-96.5	8856	13.3	8697	133.1
86	4300	399	-106.5	653	42.3	329	-145.9	238	-105.9	703	26.6	391	156.6
87	4350	4552	-58.3	5027	51.8	5304	-172.3	8615	161.2	9370	28.3	7850	-96.8
88	4400	308	-125.4	454	65.6	148	-142.0	223	-169.3	477	-2.5	883	97.6
89	4450	431	-137.0	441	13.5	326	23.8	397	143.7	345	-27.4	829	-117.8
90	4500	601	-168.3	542	15.8	266	82.3	106	-34.8	342	61.0	416	-46.9
91	4550	540	-3.7	76	-117.6	592	167.0	1430	138.9	1014	-72.9	442	9.3
92	4600	376	-153.3	828	17.6	309	-122.9	798	-166.3	650	25.5	490	-71.6
93	4650	2775	-33.2	2829	75.8	3266	-143.0	4900	-174.4	6382	46.3	4206	-82.0
94	4700	1328	166.1	259	-55.3	703	27.1	1869	-1.7	1088	-145.8	1444	130.1
95	4750	951	160.2	110	4.2	270	-30.4	2042	-18.7	1103	-123.5	1593	128.0
96	4800	1220	162.8	787	10.7	359	-0.9	2104	-44.0	336	81.4	1906	134.2
97	4850	4567	158.6	3848	28.4	3322	-65.3	6937	-61.2	5520	49.2	7797	158.6

98	4900	735	-71.8	1412	-131.5	1663	94.5	2077	84.8	3690	-126.3	2020	15.1
99	4950	2380	170.5	3201	-89.1	3562	61.8	5145	8.6	6013	-131.8	4296	96.3
100	5000	1082	-16.9	1199	113.0	1144	-139.6	2484	171.0	1673	45.5	1975	-68.6
101	5050	328	-25.8	618	112.4	514	-143.2	929	135.2	612	42.2	829	-95.2
102	5100	176	39.4	501	57.8	506	-127.3	424	122.6	426	119.3	1124	-65.4
103	5150	539	-153.3	623	46.3	499	-136.2	906	-94.3	864	4.2	601	126.1
104	5200	418	-36.2	570	-129.9	784	118.6	921	94.5	711	-119.1	645	-21.9
105	5250	89	-124.7	626	-92.0	735	67.5	1001	48.2	1655	-128.5	551	93.0
106	5300	766	-3.9	506	115.1	337	-139.8	1253	165.6	719	59.4	913	-48.7
107	5350	643	-78.8	843	122.6	332	10.0	867	-88.5	1131	8.2	851	144.6
108	5400	282	-36.7	98	-78.9	431	-174.2	871	116.4	838	-120.9	455	29.8
109	5450	457	-67.6	907	-13.0	1232	161.9	564	49.1	2244	-113.5	1391	55.1
110	5500	404	-106.0	600	143.1	387	-39.2	451	-26.1	1382	109.6	733	-98.4
111	5550	83	172.8	89	-10.1	294	31.0	766	63.1	476	-143.4	520	70.2
112	5600	222	-14.5	682	116.9	420	-79.1	770	153.9	504	0.1	871	-107.3
113	5650	626	35.4	329	-60.0	802	-129.9	1161	141.2	1100	-144.7	1267	-21.9
114	5700	110	-41.2	300	154.4	191	-146.9	96	-84.1	408	-49.8	468	128.7
115	5750	446	75.7	151	-172.0	208	-147.3	652	-170.6	645	-50.8	621	-1.1
116	5800	844	-88.3	567	130.2	706	11.7	931	50.1	970	122.2	589	-108.3
117	5850	529	28.6	813	-178.6	389	-3.7	877	-145.0	464	121.2	210	-14.1
118	5900	1449	-96.4	1252	30.8	1170	164.4	2327	68.3	2219	-72.4	880	164.1
119	5950	232	8.8	964	30.9	962	-153.0	1699	87.2	1703	-109.1	664	7.4
120	6000	1223	-62.7	898	121.1	405	152.2	1049	1.6	524	33.9	1190	164.6
121	6050	1050	-70.7	865	80.5	443	-167.0	1132	22.7	824	-102.3	1146	138.6
122	6100	488	137.4	424	-95.8	472	-7.0	593	-151.6	469	75.1	868	-36.0
123	6150	291	-120.0	472	25.4	85	62.1	551	94.2	299	156.2	603	-90.9
124	6200	65	-56.5	632	163.8	235	50.2	668	-170.9	850	58.5	210	-8.8
125	6250	140	-140.7	387	177.7	243	-38.0	1041	112.1	371	-90.4	328	-104.0
126	6300	153	-80.2	185	93.2	141	43.3	637	123.0	368	-84.8	731	-18.5
127	6350	505	-10.1	319	132.7	439	-171.1	193	177.4	792	-22.0	334	167.5
128	6400	1255	139.3	1030	-44.3	724	-76.0	2347	-174.7	1169	-42.6	1991	25.5
129	6450	1080	-148.3	567	31.2	256	-124.1	773	-47.0	1361	-49.2	2087	110.0
130	6500	596	137.5	513	163.4	225	24.1	1378	-171.5	840	49.0	1142	-76.2
131	6550	380	142.3	371	-49.7	488	-56.6	745	128.9	425	-113.3	457	1.2
132	6600	943	-25.6	977	-154.3	593	112.0	604	-52.4	1175	84.9	797	-125.9
133	6650	239	-4.2	472	-88.1	525	74.6	76	-69.2	918	66.7	296	92.7
134	6700	824	-15.6	638	164.4	690	-147.5	1430	20.8	1050	-138.3	1279	169.3
135	6750	327	-0.5	514	135.1	448	171.5	576	-18.1	126	-3.4	864	105.6
136	6800	143	-23.7	779	156.6	211	29.6	168	-18.7	512	164.8	497	-64.0
137	6850	279	31.9	228	-176.6	483	-153.8	335	163.0	413	-95.5	785	95.1
138	6900	450	-26.3	163	111.5	132	110.0	491	48.0	588	-14.2	309	66.4
139	6950	334	44.2	296	134.2	343	38.1	487	-162.2	637	-46.0	468	-17.1
140	7000	598	7.3	380	167.2	226	113.0	453	61.9	327	-160.0	430	145.4
141	7050	836	30.5	592	-130.3	41	59.7	475	-90.5	923	-24.9	935	120.3
142	7100	172	-126.4	796	86.5	819	-65.6	1082	110.2	822	-116.8	484	-103.4
143	7150	552	-4.1	472	125.3	620	-38.8	1219	6.3	1446	-155.0	841	59.3
144	7200	573	-164.6	518	-28.7	834	72.4	1452	168.8	997	24.9	736	-29.6
145	7250	146	136.1	19	27.7	417	78.9	418	110.7	731	169.3	700	11.2
146	7300	705	33.3	615	-109.9	356	8.0	648	100.4	715	-124.7	671	77.3
147	7350	332	-124.7	765	85.6	1036	-39.9	764	141.0	334	-60.7	426	-46.0
148	7400	377	60.6	284	-170.7	256	119.5	449	-108.3	1158	35.2	1356	175.5

Voltages, Steady State, DC-link=50V. Hardware setup:

Steady State Hardware Result, 50 Hz Fundamental Frequency 50V. Dc-link and 9.12Ohms load per phase													
		A		B		C		AB		BC		CA	
H	F	Mag.	Angle	Mag.	Angle	Mag.	Angle	Mag.	Angle	Mag.	Angle	Mag.	Angle
0	0	582	0.0	548	180.0	142	0.0	778	0.0	1070	180.0	805	0.0
1	50	14998	-11.3	14785	-132.9	14661	108.4	25759	-58.4	26195	179.5	25228	59.4
2	100	525	147.7	104	96.1	600	-39.7	260	97.7	867	57.8	1090	-113.5
3	150	105	-150.2	363	87.8	265	-90.0	459	64.0	194	163.5	513	-82.9
4	200	134	148.8	113	50.5	175	-74.2	707	104.0	609	-88.3	159	-19.0
5	250	600	100.5	550	-158.2	741	-32.2	1504	20.8	1655	138.2	1638	-95.3
6	300	152	78.4	179	-0.7	260	-144.7	670	-157.3	227	77.5	553	3.2
7	350	251	92.2	261	3.2	369	-132.5	488	-123.1	632	139.2	768	0.5
8	400	121	-164.0	99	99.9	144	-26.5	375	88.2	457	-64.8	199	174.4
9	450	79	-145.5	14	-139.7	91	28.5	131	-10.5	140	117.4	132	-118.3
10	500	189	154.7	89	-129.8	235	-1.2	136	-33.2	307	29.4	399	-168.2
11	550	342	107.6	288	-132.7	323	-22.6	524	-47.4	467	44.0	705	174.6
12	600	176	-68.4	169	59.0	158	173.0	389	123.7	260	-105.6	294	-10.8
13	650	93	-145.3	124	79.3	86	-56.9	267	-140.0	342	135.0	453	-8.9
14	700	42	-4.1	47	134.4	31	-84.3	145	62.7	150	-113.6	21	156.6
15	750	140	-155.6	39	118.3	146	3.8	180	79.8	438	-87.6	268	100.4
16	800	256	-142.5	149	-36.6	264	71.6	175	-103.1	242	-30.7	354	119.9
17	850	80	150.8	160	-145.2	218	13.0	43	-28.2	87	-72.4	127	120.5
18	900	112	-77.9	260	91.4	146	-99.5	464	59.0	228	-122.0	231	-123.9
19	950	476	-42.8	510	177.9	353	60.9	626	-50.2	828	179.0	659	46.8
20	1000	298	123.1	316	35.5	434	-103.7	708	105.3	523	-17.2	635	-122.9
21	1050	102	122.6	113	79.4	205	-80.7	400	77.1	195	-59.2	300	-128.5
22	1100	53	116.7	143	108.4	202	-72.0	398	71.5	74	-155.4	334	-98.8
23	1150	158	85.4	177	143.6	302	-66.1	583	66.2	191	175.7	544	-95.1
24	1200	425	-133.1	352	31.0	126	92.3	294	157.5	797	-42.5	563	128.9
25	1250	116	-125.0	151	78.7	71	-55.5	351	105.7	351	-31.8	255	-145.7
26	1300	235	21.3	195	-81.2	270	153.0	447	-107.8	367	131.4	420	21.3
27	1350	48	32.6	10	-61.4	43	-159.5	152	-167.8	61	-2.6	105	19.4
28	1400	79	-23.5	83	63.5	120	-160.2	163	146.6	102	-151.1	232	-6.8
29	1450	138	123.7	156	-113.2	145	10.4	246	-40.2	302	75.5	296	-151.6
30	1500	142	-54.9	244	43.9	260	-172.6	458	155.0	287	-67.5	306	15.5
31	1550	195	-86.6	110	121.7	115	63.8	142	39.9	341	-95.2	264	105.9
32	1600	135	57.4	145	-6.5	250	-155.9	268	-165.2	186	91.9	283	-22.1
33	1650	33	43.1	15	41.1	50	-134.0	130	158.7	56	-64.8	103	-7.9
34	1700	58	-14.5	52	66.8	86	-153.5	91	113.7	50	-141.1	78	-43.9
35	1750	73	-39.3	75	93.8	54	-159.8	48	107.6	70	-141.9	69	-12.1
36	1800	193	156.2	145	-76.5	161	19.8	267	-105.2	374	-5.5	408	135.6
37	1850	66	-54.0	9	-104.1	71	115.2	51	-99.0	85	-65.1	136	104.9
38	1900	66	129.7	187	34.2	192	-129.4	476	173.5	348	9.4	171	-45.2
39	1950	46	123.3	48	-4.8	41	-132.3	22	-117.9	70	79.7	44	-90.6
40	2000	56	99.4	91	-10.2	80	-150.2	168	-143.4	184	98.5	190	-23.2
41	2050	50	-43.1	50	146.8	16	60.8	154	17.3	63	37.2	211	-159.8
42	2100	214	-151.5	162	-46.6	231	65.6	265	-166.3	317	-41.0	282	89.6
43	2150	158	-150.7	7	-142.0	166	27.3	93	129.0	209	139.2	301	-43.8
44	2200	162	-21.9	209	-102.0	286	106.8	437	-78.6	413	131.8	229	33.5

45	2250	21	50.4	57	134.1	56	-73.4	148	112.6	146	-57.4	28	-95.1
46	2300	27	-89.5	28	67.9	9	163.2	25	152.3	40	-24.5	15	177.5
47	2350	23	-52.6	58	173.0	43	-4.3	28	-96.4	37	110.9	17	-71.4
48	2400	122	-108.5	86	-1.9	140	108.6	151	123.1	207	-109.7	182	23.0
49	2450	85	-96.9	63	122.6	56	31.5	52	15.7	109	-41.4	140	161.0
50	2500	60	-8.8	49	-63.2	104	141.7	127	-144.0	290	45.4	160	-130.0
51	2550	104	109.8	103	-161.2	153	-30.1	260	64.8	155	-154.8	183	-81.4
52	2600	68	-157.8	81	138.9	129	-16.9	161	69.6	84	13.9	219	-132.8
53	2650	112	60.6	102	-111.9	18	174.0	272	-34.5	181	-172.5	173	103.0
54	2700	209	153.5	241	-85.8	224	33.5	437	-43.9	307	65.3	452	179.1
55	2750	93	-1.1	83	128.6	89	-127.6	191	82.1	231	-133.8	153	-14.3
56	2800	140	-25.5	143	174.6	48	78.5	180	26.5	231	-124.4	120	105.4
57	2850	25	85.8	52	81.2	90	-110.6	117	132.5	23	-48.5	93	-49.2
58	2900	22	-5.1	48	153.6	28	-50.3	113	71.3	131	-130.9	50	-17.3
59	2950	144	68.4	22	-45.0	132	-123.2	60	-45.6	232	134.1	184	-45.1
60	3000	106	19.6	57	154.5	79	-130.0	137	39.8	192	174.9	134	-49.6
61	3050	26	127.1	45	-127.4	49	15.3	91	-123.3	91	-70.5	154	80.3
62	3100	95	24.9	95	-120.3	59	129.6	142	-51.3	182	-158.5	187	69.2
63	3150	206	-166.3	127	24.6	84	-8.8	113	35.0	193	46.3	314	-136.0
64	3200	67	178.4	39	67.6	60	-38.5	16	41.4	81	67.7	85	-114.7
65	3250	29	-7.1	75	-159.6	53	30.0	213	26.6	115	-107.0	147	172.3
66	3300	83	98.9	95	-167.4	130	-35.9	174	22.9	63	129.1	166	-136.3
67	3350	108	-113.8	58	30.6	66	91.0	86	138.6	167	-65.9	99	87.1
68	3400	65	-130.0	107	113.9	109	-31.7	79	31.1	19	-17.6	81	-156.7
69	3450	54	28.5	59	-93.0	58	132.4	65	-65.1	93	120.8	7	-48.1
70	3500	52	128.8	45	-144.2	73	-19.2	47	23.7	19	-20.4	62	-171.2
71	3550	36	171.7	36	-111.0	54	22.8	168	-18.5	35	139.8	126	169.4
72	3600	162	155.6	150	-125.4	242	7.9	313	-35.3	204	69.2	307	-179.1
73	3650	444	-41.4	397	90.1	362	-168.3	711	120.2	886	-115.7	777	15.0
74	3700	266	-65.7	269	135.6	100	27.7	264	48.0	546	-120.6	300	69.4
75	3750	501	89.8	490	-18.4	585	-149.8	949	168.0	763	54.2	953	-59.9
76	3800	95	63.9	82	13.1	165	-142.6	351	152.4	110	18.6	266	-45.0
77	3850	103	62.2	61	55.3	163	-128.2	258	121.9	70	-133.4	266	-45.6
78	3900	99	28.6	81	108.7	143	-120.5	239	140.9	89	-135.2	259	-18.5
79	3950	451	-152.6	447	-25.4	407	83.8	713	-95.8	765	26.1	725	152.2
80	4000	57	-136.6	58	17.6	24	98.1	90	178.3	86	12.5	38	-72.0
81	4050	70	131.9	66	-21.9	25	-122.2	75	-39.5	85	176.5	63	59.3
82	4100	26	170.3	38	-27.6	15	110.8	47	-165.7	72	31.1	15	-77.1
83	4150	50	0.0	24	70.0	55	-174.4	120	122.6	100	-122.1	88	-3.5
84	4200	28	66.2	36	167.6	49	-66.9	105	93.7	71	-116.6	69	-42.4
85	4250	576	-107.8	580	17.1	544	129.2	975	-156.2	915	-37.5	983	82.3
86	4300	10	-89.3	7	154.2	7	61.8	124	129.1	117	-64.9	31	34.2
87	4350	548	-143.7	624	93.4	562	-40.8	1040	79.3	952	-53.1	815	-162.3
88	4400	59	-176.8	42	1.9	16	20.9	118	-101.3	75	23.9	95	110.8
89	4450	102	-73.1	55	81.4	47	110.5	39	150.9	41	-117.9	50	45.6
90	4500	20	61.7	21	-147.6	24	-43.0	129	70.3	116	-137.9	46	-34.4
91	4550	21	43.7	45	91.3	63	-113.8	32	171.9	35	27.8	35	-107.0
92	4600	59	-64.6	99	106.7	41	-89.9	136	83.6	150	-112.9	47	-4.2
93	4650	297	-99.9	353	138.0	318	2.9	545	17.9	602	-119.8	408	118.8
94	4700	88	73.5	78	10.8	141	-145.2	214	162.1	100	46.6	200	-46.7

95	4750	67	52.1	27	54.5	100	-134.3	194	150.4	43	72.3	193	-34.7
96	4800	61	49.9	77	81.8	125	-119.3	256	126.1	106	-108.5	205	-27.4
97	4850	361	34.5	308	128.2	460	-110.2	684	111.8	575	-134.1	670	-18.2
98	4900	163	-178.7	175	-16.9	51	80.0	135	-123.5	354	38.2	231	-156.7
99	4950	309	165.9	316	28.6	231	-93.3	511	162.9	624	27.6	438	-99.7
100	5000	79	-37.8	95	-114.1	139	92.6	219	-34.8	148	-154.9	190	104.7
101	5050	10	-107.9	45	-75.7	47	78.3	60	-35.5	82	-150.9	70	81.0
102	5100	29	80.8	36	-114.5	7	11.7	84	-36.8	40	135.9	45	148.2
103	5150	13	119.8	38	-126.1	31	14.2	29	-7.1	47	-175.7	22	21.5
104	5200	61	-114.5	72	15.0	59	131.5	27	140.1	79	-54.8	53	113.4
105	5250	47	-134.0	58	50.1	13	-69.4	69	132.1	89	-17.7	59	-145.3
106	5300	25	-1.0	72	-56.9	96	122.2	62	-79.8	61	176.9	80	57.4
107	5350	65	-66.2	55	21.2	103	139.5	53	20.5	151	178.3	103	-8.0
108	5400	32	-55.1	44	-30.2	67	135.5	44	163.5	47	-82.1	67	36.3
109	5450	40	-12.7	87	-25.6	119	152.0	173	131.6	204	-47.0	27	148.1
110	5500	49	120.8	50	-113.1	38	-1.6	57	-34.9	71	97.0	64	-137.4
111	5550	5	-175.0	18	-141.4	9	21.6	65	-60.2	46	94.5	33	165.4
112	5600	32	135.1	43	-5.2	29	-159.2	123	-116.6	32	76.4	89	56.4
113	5650	72	175.2	32	-43.5	52	3.4	73	-172.2	91	-55.9	90	83.7
114	5700	7	30.3	32	19.5	43	-170.0	49	-80.3	65	142.0	40	-15.3
115	5750	22	12.9	30	36.3	50	-155.4	36	103.5	55	-151.4	55	-10.1
116	5800	57	155.3	49	-51.0	27	25.3	76	-65.3	73	59.2	54	177.6
117	5850	56	164.7	50	15.6	24	-103.3	20	-163.7	88	51.6	62	-107.5
118	5900	83	-68.8	84	-170.2	106	49.1	204	-12.8	188	-148.3	146	108.7
119	5950	68	-134.5	54	-24.2	66	75.0	54	104.0	144	-131.2	124	31.6
120	6000	1	25.6	30	119.6	27	-76.8	98	-25.7	26	64.4	93	168.8
121	6050	37	-166.6	63	62.6	50	-95.7	149	-17.7	53	-136.8	121	139.5
122	6100	53	28.8	55	-161.9	15	-48.6	101	150.4	23	120.9	125	-35.5
123	6150	48	27.3	33	-170.7	17	-135.1	24	144.4	55	174.0	85	-16.7
124	6200	27	-48.4	36	137.4	6	-25.8	70	-178.1	85	49.6	53	-88.4
125	6250	15	-97.6	26	96.8	2	81.9	40	162.6	47	29.5	46	-82.9
126	6300	24	-80.2	25	88.9	7	107.3	21	-77.4	32	-155.7	31	74.2
127	6350	34	-157.8	27	75.1	27	-48.8	27	-64.9	51	162.2	33	-1.2
128	6400	85	99.6	88	-105.3	33	-11.5	165	44.4	81	120.7	207	-109.3
129	6450	81	93.8	11	172.3	82	-96.6	55	-19.7	156	-51.3	214	136.7
130	6500	17	-54.0	19	121.0	6	-88.0	79	36.1	29	-90.8	50	-159.4
131	6550	26	-11.5	30	109.2	34	-119.5	79	75.9	10	-121.5	80	-106.2
132	6600	37	143.3	62	-75.2	41	50.8	71	-168.2	114	-57.5	103	101.1
133	6650	28	141.6	31	-14.9	9	152.4	22	177.7	54	-29.8	33	162.0
134	6700	50	-59.0	50	145.1	23	45.1	65	-156.2	49	150.7	117	7.0
135	6750	25	-53.9	8	173.5	23	110.8	21	-104.6	24	137.4	14	13.2
136	6800	8	14.2	26	-160.2	22	11.9	31	51.0	10	-68.9	32	173.9
137	6850	15	-9.6	13	31.0	34	178.4	45	-125.3	30	22.6	32	103.8
138	6900	23	-129.1	7	58.1	28	46.7	27	171.4	17	-26.8	12	84.6
139	6950	9	30.7	20	67.5	29	-130.8	24	2.8	45	151.3	11	-71.9
140	7000	41	-30.3	36	118.2	38	-156.2	24	119.0	34	129.2	51	-55.4
141	7050	46	19.6	16	131.1	37	-163.3	24	115.2	23	-139.5	35	0.7
142	7100	68	169.2	46	-10.9	15	-52.6	20	-163.7	112	-10.4	93	176.7
143	7150	45	178.9	39	3.6	5	-92.0	56	-176.4	76	4.9	30	-166.1
144	7200	33	-9.3	61	-156.8	35	46.8	88	-65.5	34	-165.9	104	90.3

Current in all phases Steady State DC-link=250V, Hardware Setup:

Currents SteadyState Hardware 250V. DC -link 27 ohms and 40mH per phase							
		A		B		C	
H	F	Mag.	Angle	Mag.	Angle	Mag.	Angle
0	0	13.3	180.0	416.6	0.0	184.6	180.0
1	50	6700.3	97.3	6789.2	-22.5	6718.7	-143.4
2	100	246.2	-87.0	165.0	133.7	157.9	51.7
3	150	118.2	-82.8	92.8	137.3	96.2	59.6
4	200	74.0	-100.2	21.2	-148.3	91.3	68.5
5	250	110.5	-63.5	114.6	105.0	30.5	-155.1
6	300	82.7	-127.2	58.4	74.6	32.0	7.4
7	350	85.7	-150.6	79.5	64.8	49.5	-40.4
8	400	35.6	-75.2	15.5	-175.2	40.0	77.8
9	450	39.6	-94.2	11.7	134.2	29.6	89.6
10	500	14.7	-69.7	25.5	-167.0	25.2	28.7
11	550	13.7	-143.3	24.0	-148.7	39.8	28.6
12	600	37.7	-95.4	21.1	85.5	19.5	102.9
13	650	40.9	-99.3	20.5	104.1	20.6	77.2
14	700	28.6	-85.3	12.4	90.0	16.1	101.1
15	750	19.9	-107.9	8.5	19.5	18.1	92.3
16	800	34.8	-106.1	11.6	11.9	23.9	95.5
17	850	26.6	-102.9	10.8	56.1	21.7	91.3
18	900	4.7	-65.7	5.5	98.8	2.9	139.4
19	950	41.6	-91.3	28.9	135.1	34.9	36.9
20	1000	6.6	107.9	13.8	-20.3	13.9	-158.4
21	1050	9.3	-102.5	5.6	12.9	7.3	68.1
22	1100	12.1	-106.3	0.7	74.0	12.8	87.4
23	1150	17.0	-146.8	9.3	-62.2	23.0	45.9
24	1200	20.9	-69.1	29.6	104.7	10.3	-130.3
25	1250	8.6	-96.4	14.9	72.6	3.6	-32.7
26	1300	15.1	-10.0	10.7	-81.5	21.8	128.4
27	1350	9.5	-29.7	1.9	-51.0	11.2	113.3
28	1400	6.7	-72.8	2.8	-75.4	6.1	83.7
29	1450	16.2	-62.8	9.1	77.8	9.2	161.3
30	1500	3.0	-132.1	6.1	-166.9	7.1	20.8
31	1550	13.3	-19.0	8.1	-155.7	16.6	90.3
32	1600	2.2	129.5	3.4	59.6	4.4	-147.9
33	1650	6.6	-103.2	4.4	75.7	4.4	122.7
34	1700	9.9	-87.3	2.4	136.2	4.3	138.7
35	1750	9.4	-88.4	4.0	109.1	5.1	118.1
36	1800	5.4	-7.2	5.7	-118.8	5.6	42.6
37	1850	5.6	-70.4	6.3	75.8	6.2	125.7
38	1900	16.4	-73.9	6.7	115.6	5.4	84.3
39	1950	3.1	-69.8	6.7	166.6	6.1	101.8
40	2000	7.9	-48.7	3.9	-164.1	8.6	91.8
41	2050	4.0	-68.6	7.2	123.5	1.9	4.1
42	2100	10.5	-100.2	6.5	19.8	13.6	114.4
43	2150	12.0	-67.4	1.1	-52.2	9.0	108.6
44	2200	17.2	-80.3	9.5	145.8	13.7	60.9
45	2250	7.1	-77.8	0.7	39.1	1.2	65.7

Current in T1 Steady State DC-link=250V, Hardware Setup:

Currents SteadyState Hardware 250V. DC -link 27 ohms and 40mH per phase										
		A			T1			B1		
H	F	Mag.	Mag./Fun	Angle	Mag.	Mag./Fun	Angle		Mag./Fund	Angle
0	0	13.2	0.00195	0	64.6	0.01927	0	179.6	0.0534992	0
1	50	6759.1	1	-65.55	3351.1	1	113	3357.1	1	-63.9
2	100	202.3	0.02993	103	1763.7	0.5263	-8.066	1697.4	0.5056127	-1.539
3	150	111.2	0.01646	88.73	211.0	0.06297	-156	203.9	0.0607328	172.7
4	200	101.6	0.01504	90.21	261.2	0.07794	-119.3	183.7	0.0547238	-131.8
5	250	90.7	0.01341	153.5	128.8	0.03845	111.5	202.5	0.0603183	128.8
6	300	94.7	0.014	85.55	543.9	0.1623	-162.7	508.4	0.1514326	-171.9
7	350	83.7	0.01238	120	158.6	0.04732	2.019	140.2	0.0417666	35.64
8	400	33.7	0.00499	74.69	204.2	0.06094	66.11	235.7	0.070215	66.42
9	450	28.5	0.00422	81.25	62.3	0.01859	-12.23	67.3	0.0200417	14.11
10	500	45.8	0.00678	76.68	109.7	0.03272	-89.35	61.9	0.0184494	-78.84
11	550	52.6	0.00778	82.62	5.4	0.0016	2.95	50.2	0.0149474	72.4
12	600	12.1	0.00178	90.27	158.5	0.04729	73.11	174.2	0.0518899	74.73
13	650	21.2	0.00313	60.78	48.8	0.01457	-137.6	37.6	0.0112001	-154.3
14	700	16.7	0.00247	88.47	41.9	0.01249	-101.1	25.9	0.0077042	-108.7
15	750	12.9	0.00191	99.99	11.7	0.00349	-120.2	2.0	0.0005879	147.5
16	800	15.5	0.00229	10.68	29.8	0.0089	93.58	36.5	0.0108867	79.89
17	850	9.4	0.00139	111	36.1	0.01077	-29.92	33.9	0.0100948	-15.63
18	900	23.0	0.0034	104.2	35.3	0.01055	-78.89	7.7	0.0022796	-96.4
19	950	41.7	0.00617	51	9.9	0.00294	175	39.6	0.0117853	67.45
20	1000	19.6	0.0029	145.5	30.1	0.00899	25.9	23.0	0.0068494	65.13
21	1050	13.4	0.00199	108.5	9.2	0.00273	142.6	20.5	0.0060968	114.5
22	1100	11.5	0.0017	71.85	11.0	0.00328	-54.06	9.9	0.0029585	42.86
23	1150	23.6	0.00349	56.11	11.2	0.00334	117.9	28.5	0.0084851	83.93
24	1200	22.9	0.00338	129.1	13.2	0.00395	12.1	21.1	0.0062874	103.4
25	1250	21.3	0.00315	113.1	4.8	0.00142	-124.6	19.8	0.0059013	116.3
26	1300	5.6	0.00083	-75.66	25.9	0.00771	52.94	22.3	0.0066509	56.65
27	1350	10.4	0.00154	148.9	12.2	0.00365	-71.85	8.1	0.0024162	-83.93
28	1400	10.6	0.00156	85.08	10.7	0.00318	55.51	15.0	0.0044715	79.08
29	1450	8.1	0.0012	-163.3	10.7	0.00318	53.47	0.8	0.0002414	16.52
30	1500	20.0	0.00296	93.81	11.4	0.00341	41.1	32.8	0.0097595	72.81
31	1550	9.0	0.00133	79.39	11.0	0.00329	-167.7	12.9	0.0038507	127.8
32	1600	14.9	0.0022	113.7	10.4	0.00311	-25.08	7.2	0.0021525	52.67
33	1650	10.3	0.00152	109.7	7.2	0.00215	-147.2	9.3	0.0027715	136.4
34	1700	7.5	0.00111	92.03	3.2	0.00095	-147.2	5.0	0.0014761	113.8
35	1750	7.3	0.00108	108.2	11.7	0.00349	31.16	17.0	0.0050698	57.57
36	1800	11.1	0.00164	71.74	7.9	0.00235	-58.6	8.2	0.0024382	46.89
37	1850	8.5	0.00126	85.67	11.3	0.00336	14.34	15.9	0.004742	47.76
38	1900	10.7	0.00158	73.99	27.4	0.00816	136.8	30.2	0.0089861	117.7
39	1950	5.8	0.00085	115.2	2.6	0.00078	9.272	5.7	0.0016983	155.5
40	2000	4.4	0.00066	105.1	12.8	0.00382	-18.67	14.0	0.0041645	14.16
41	2050	10.4	0.00153	120.2	0.5	0.00016	109.9	10.1	0.0030227	132.4
42	2100	6.2	0.00092	-5.531	22.8	0.0068	173.1	17.8	0.0052983	164.4
43	2150	4.5	0.00067	89.59	29.9	0.00893	104.8	33.4	0.0099544	116.5
44	2200	17.5	0.00259	80.15	20.3	0.00606	-103.3	8.6	0.0025728	-81.7
45	2250	5.5	0.00082	126.8	8.5	0.00252	30.14	9.8	0.0029175	84.46

Current in T1 Steady State DC-link=50V, Hardware Setup:

Fourier Analysis of Current in T1 Steady State				
Harm	Freq	Mag.	Angle	Mag./fund Mag.
0	0	51.9	180.0	0.059
1	50	884.9	-140.2	1.000
2	100	248.2	-142.0	0.280
3	150	23.9	19.2	0.027
4	200	50.5	74.0	0.057
5	250	89.1	122.5	0.101
6	300	229.5	81.8	0.259
7	350	56.8	-132.9	0.064
8	400	91.0	160.1	0.103
9	450	35.2	-39.8	0.040
10	500	15.5	172.6	0.018
11	550	24.3	176.6	0.027
12	600	61.2	177.1	0.069
13	650	13.9	-43.9	0.016
14	700	15.8	-178.5	0.018
15	750	15.7	-17.7	0.018
16	800	1.6	20.5	0.002
17	850	16.1	-27.7	0.018
18	900	34.1	-70.5	0.039
19	950	21.1	-1.1	0.024
20	1000	13.5	-100.8	0.015
21	1050	15.5	-144.5	0.018
22	1100	18.2	-85.1	0.021
23	1150	8.8	-14.0	0.010
24	1200	21.2	163.6	0.024
25	1250	14.9	-154.7	0.017
26	1300	8.7	28.4	0.010
27	1350	10.1	74.9	0.011
28	1400	1.4	159.4	0.002
29	1450	13.0	8.0	0.015
30	1500	11.2	122.5	0.013
31	1550	1.7	51.0	0.002
32	1600	7.1	22.1	0.008
33	1650	9.6	27.8	0.011
34	1700	3.9	59.8	0.004
35	1750	6.0	30.5	0.007
36	1800	12.6	-36.3	0.014
37	1850	8.3	-18.5	0.009
38	1900	9.9	72.6	0.011
39	1950	10.7	-20.1	0.012
40	2000	10.9	-17.8	0.012
41	2050	8.7	-82.0	0.010
42	2100	2.3	-32.3	0.003
43	2150	10.8	-174.4	0.012
44	2200	14.9	-158.6	0.017
45	2250	5.3	-70.1	0.006
46	2300	2.3	159.9	0.003

Appendix 4 Fourier Analysis Fault Tolerant, Hardware Setup

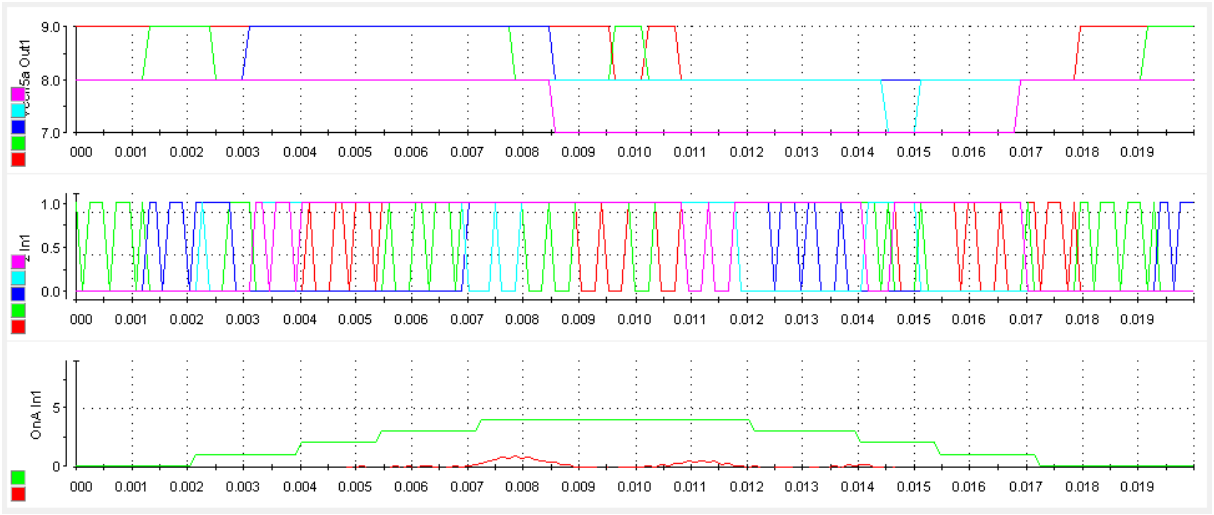
Current analysis:

Fault Tolerant State 100V. DC -link 27 ohms and 40mH per phase							
		A		B		C	
H	F	Mag.	Angle	Mag.	Angle	Mag.	Angle
0	0	102.0	0.0	46.6	0.0	26.2	180.0
1	50	2655.6	30.5	2558.9	-89.1	2635.8	152.6
2	100	58.6	-113.6	83.7	99.4	47.4	-33.6
3	150	30.9	-119.3	65.5	108.5	53.3	-45.0
4	200	54.4	-67.6	60.9	82.3	28.3	-166.9
5	250	36.7	-116.5	54.8	59.2	20.6	-116.7
6	300	8.3	-46.6	27.2	93.4	25.0	-86.7
7	350	15.1	137.5	29.9	37.2	31.8	-113.1
8	400	8.1	-136.2	18.8	67.2	16.4	-106.3
9	450	5.2	-48.8	13.2	149.2	5.1	-9.8
10	500	15.3	-77.9	22.7	94.9	9.3	-81.8
11	550	3.9	-26.5	8.0	103.0	11.5	-104.2
12	600	7.9	-18.8	9.5	126.3	7.1	-62.1
13	650	7.7	-98.6	14.4	59.4	7.3	-135.7
14	700	7.6	-75.1	8.6	118.3	4.0	48.3
15	750	8.2	-114.5	4.2	63.2	4.7	-81.6
16	800	8.3	-48.8	10.2	91.5	3.3	-135.5
17	850	2.2	91.7	5.4	153.3	4.2	-35.9
18	900	14.3	-13.3	2.8	-157.5	9.2	168.9
19	950	6.3	2.1	4.9	58.6	10.0	-177.5
20	1000	8.6	-128.6	14.3	102.6	5.0	-23.9
21	1050	6.4	-99.5	10.6	123.3	10.3	-28.0
22	1100	7.1	-100.4	12.6	97.3	7.7	-76.5
23	1150	4.6	18.8	8.2	151.2	6.8	-69.3
24	1200	10.9	-135.8	7.5	60.5	4.3	71.1
25	1250	9.4	-79.0	7.9	101.1	4.4	86.3
26	1300	5.5	-176.0	11.1	42.2	4.3	-88.9
27	1350	6.7	173.2	5.5	67.5	6.9	-58.3
28	1400	1.9	-120.1	5.4	85.4	6.8	-70.6
29	1450	3.9	-119.0	8.9	50.7	0.7	-157.5
30	1500	8.2	-63.9	5.6	90.5	3.9	175.3
31	1550	4.3	-109.7	10.5	88.5	4.2	-73.0
32	1600	5.4	-93.0	7.8	97.5	1.7	-53.1
33	1650	5.3	-118.8	4.7	102.7	3.0	-6.2
34	1700	4.7	-58.2	5.9	58.9	2.3	-117.1
35	1750	3.4	-77.3	4.6	120.5	5.4	-119.1
36	1800	6.4	-150.2	5.6	89.7	2.3	35.4
37	1850	5.6	-173.2	4.8	67.7	2.2	-22.7
38	1900	2.9	-43.5	4.5	134.7	3.7	-55.2
39	1950	3.5	-39.1	4.4	66.0	1.7	-6.4
40	2000	9.0	-88.1	5.3	93.0	1.3	24.8
41	2050	4.9	178.9	6.9	21.1	5.5	-44.6
42	2100	3.8	-106.4	5.3	106.2	1.5	160.0
43	2150	9.2	-116.7	7.1	72.2	2.9	93.2
44	2200	4.5	106.0	5.1	66.9	11.4	-71.7
45	2250	8.8	-81.4	6.1	84.5	2.9	151.4

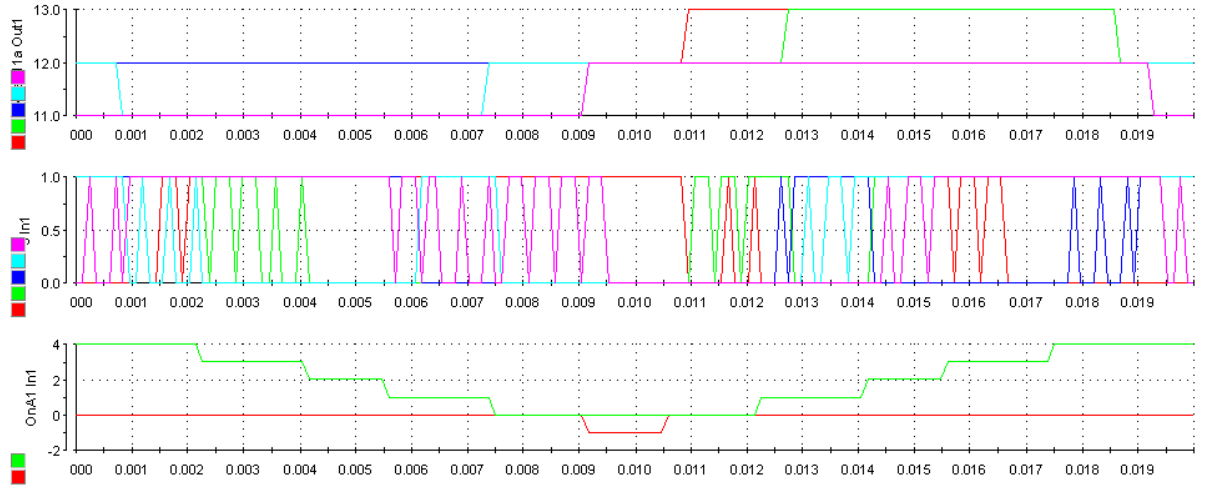
Appendix 5 Control Signals Results for Verification

To further verify the control signals, two more plots are provided. Plot a) is for the upper arm in phase A, and plot b) is for the lower arm in phase A.

a):

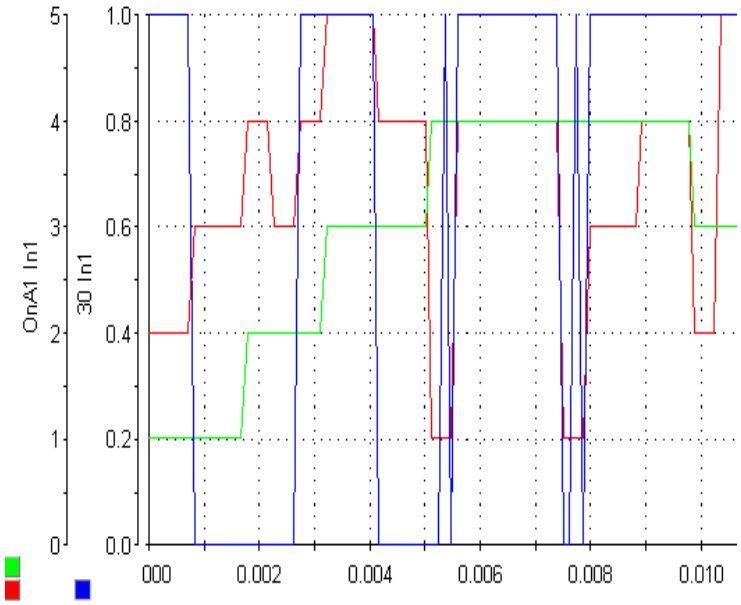


b):



The switching signal for SM 1 in B1 is the blue line, whilst the choice of PWM SM in this arm is shown in the red line. The green line shows the amount of SMs to be inserted in addition to the PWM SM. The blue PWM signal has a different y-axis scale to better show this signal. It can be seen that each time the red line is equal to 1, the blue signal oscillates according to the PWM signal. The rest of the time, it is either OFF or ON. This shows that the switching procedure described in 4.1.1.1 is followed.

Choice PWM SM (■),Amount of SMs Inserted (■) and the Switching signal for SM 1 (■), Lower Arm Phase A:

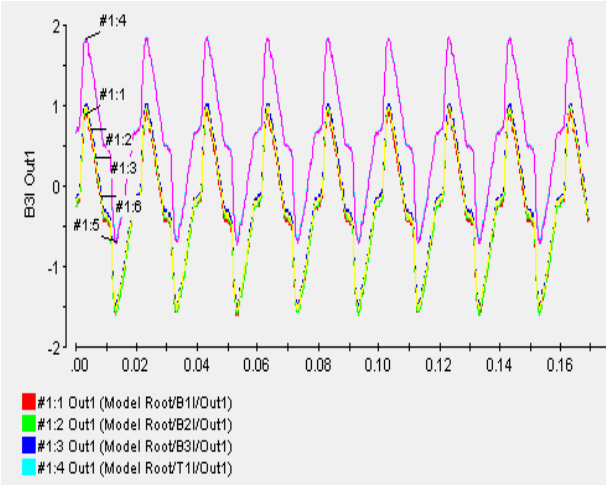

OnA1 In1
30 In1
5
4
3
2
1
0
1.0
0.8
0.6
0.4
0.2
0.0
000
0.002
0.004
0.006
0.008
0.010

Appendix 6 Arm Currents, LEM Modules, ControlDesk

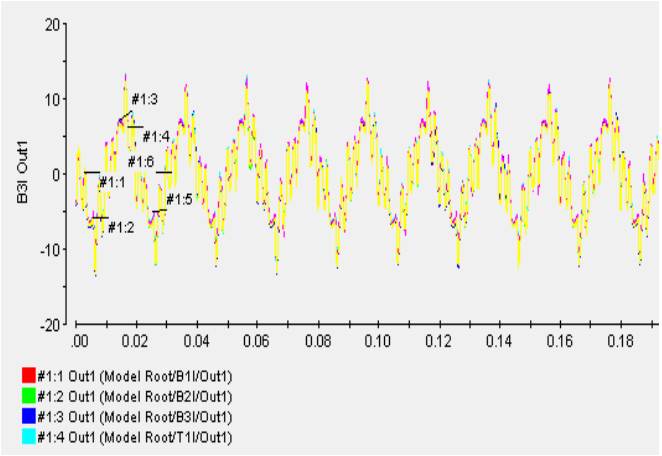
To investigate the current measurements, which are the only components that have not been tested separately; the measurements are taken with no voltage in the setup. The measurement circuit requires a voltage supply, when this supply is turned on the values changes. This supply voltage also closes the contactors T and B, in addition to the bypass of the charging resistor. There is a gain added in the Simulink model which is set to 100 in this case. The correct gain is 166 because the LEM modules used for these measurements are 50-p and the wire goes through each LEM module three times. The voltage input to dSPACE have been measured with a multimeter at 0.7V with the supply on, this corresponds well with the graph. The supply for the LEM modules are fed through a 230V. AC plug. It can be seen in the figures that the offset values vary with 50Hz, but since it is not sinusoidal, the signals could be filtered in Simulink for a better result.

One of the LEM modules is a 100-p which should have had six windings to match the 50-p with three windings rating. This module has seven windings, and it therefore has an amplitude higher than the rest.

Current Measurements with Supply Voltage OFF:



Current Measurements with supply voltage ON:



Appendix 7 Balancing Algorithm

The Balancing algorithm is implemented in Simulink like a MATLAB function. The extra if loop for the case with a fault in SM 1 in the upper arm of phase A is included but commented out. The xx_on signal consists of the number of modules for each arm that should be inserted. The pwm SM will add to that number. The pwm array that is an output of this code contains the number of the cell that should performe PWM for each arm. The indexes for this array is equal to the current and voltage arrays and matrices.:

```
function [pwm,V] = onoff(xx_on,vau,val,vbu,vbl,vcu,vcl,iarm)
%#codegen
%i=(iau,ibu,icu,ial,ibl,icl)
 %V=(vau';vbu';vcu';val';vbl';vcl']
%vau(1)=int8(0);In the hardware model it is necessary to set the value to
zero before the other capacitors are charged
V=int8(zeros(6,5));

pwm=int8(zeros(1,6))';

[~,Vsort]=(sort([vau';vbu';vcu';val';vbl';vcl'],2));

%counting to find the pwm cell, k=(au,al,bu,bl,cu,cl)
k=int8(zeros(1,6));
i=int8(0);
while i<5
    i=int8(i+1);
for j=1:6
    if iarm(j)>0
        Vsort(j,:)=fliplr(Vsort(j,:));
    end

        %%%Signals to phase a
     %fault in cell1:
%     %%the sorting will put the index 1 at place 1 or 5 depending on
%     %the current direction, to avoid switching of the faulty module
%     %this if loop is established

 %if iarm(1)>0 && i>1 || iarm(1)<0 && i<5    %this loop
 if xx_on(j)>0
V(j,Vsort(j,i))=int8(1);
xx_on(j)=int8(xx_on(j)-1);
 elseif k(j)==0 && xx_on(j)==0

     pwm(j)=int8(Vsort(j,i));

     k(j)=int8(1);
 end

% end


end
end
    end
```