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Interconnection of an Isolated Power System to an External Power Supply

- Dimensioning, modelling and control

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Preface

This master thesis concludes my five-year master degree in Energy and Environmental engineering. Throughout the work with this thesis, I have used much of what I have learned at my time at the Norwegian University of Science and Technology. I have also gained new and deeper understanding of the dynamics in power systems, converter control, faults and fault protection.

First, and foremost, I would like to thank my supervisor, Professor Lars Einar Norum at the Department of Electric Power Engineering at the Norwegian University of Science and Technology for guidance and advice throughout the semester. I would also like to thank my co-supervisor, Espen Haugan at Siemens, and Sverre Skaldeberg Gjelde at Siemens for help defining the task, and guidance throughout the semester.

Special thanks are given to Santiago Sanchez Acevedo at NTNU and Jon Are Suul at SINTEF for help with converter control related issues.

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Abstract

In this master thesis, a possible solution on how to connect a jack-up rig to an external supply was proposed. Using a conceptual layout of a typical jack-up rig power system as the basis, a suitable solution was proposed. The solution consists of a three winding transformer, and a frequency changer consisting of a twelve pulse rectifier and a voltage source converter. The frequency changer was needed because of the different frequencies on the supply and jack-up rig systems. In addition, filters, and a simple overcurrent protection relay were designed. After presenting the theoretical basis for the design of the components, a model was made in Matlab/Simulink to test and verify the solution.

It was assumed that the external supply was a stiff network, and the external supply was therefore modelled as a voltage source. The external supply supplies the jack-up rig through a sub-sea cable with voltage of 36 kV and frequency of 50 Hz. A simple RL equivalent was used to model this based on a suitable cable from Nexans. The twelve-pulse rectifier model was made using two premade six-phase rectifiers in Simulink connected in series. This to minimize DC link ripple. The DC link filter was dimensioned analytically with respect to allowed current and voltage ripple and the resulting values were inductance, L = 13.63 mH and, capacitance, C = 1.2 mF.

A two level voltage source converter was used to convert DC to AC at the desired 60 Hz frequency. The control system was based on proven methods using a cascaded control structure with an outer voltage control loop, and an inner current control loop. The control was performed in the d-q reference frame allowing the use of PI controllers. These were tuned using the pole placement technique.

The inverter output filter was tuned to attenuate the dominant inverter induced harmonics. A cut-off frequency of ω_o= 1257 [rad/s], with inductance, L = 6.3 mH, and capacitance, C = 100.36 µF proved to give good attenuation.

All steady state simulations proved successful with respect to harmonic distortion, voltage level and frequency. The largest load side THD was the current THD on the HV switchboard. This was 0.59 %. The supply line current THD at nominal load was 9.28 % due to the twelve pulse rectifiers and the lack of a filter.

During simulations of different load scenarios, step changes in load caused a maximum voltage dip of 20 V, and a current overshoot in one of the phases of about 1500 A. Using a linear ramp load instead, with a change in load power, $\frac{dP}{dt}$ = ± 6 MW/s, and reactive power change, $\frac{dQ}{dt}$ = ± 4 MVAr/s the supply followed perfectly, without any transients.

Fault simulations were done with a three-pole short circuit on different places on the jack-up AC side, and a bolted pole-to-pole short circuit of the DC link. None of the faults at the load islands caused any overcurrent in the interconnection. The largest being 159.2 kA at the inverter terminals. The initial peak fault currents during jack-up AC side fault simulations was caused by the inverter filter capacitors. A short circuit of the inverter switches proved critical. This yielded a peak fault current of 747 kA, and would destroy the inverter switches. The short

circuit on the DC link had a peak current of 23 kA, and would probably destroy the rectifier diodes. The overcurrent protection relays used proved successful in interrupting the fault currents, and selectivity was maintained.

Studying the results, it is apparent that the proposed solution works during normal operation, but that a multilevel converter should be used instead to minimize filter capacitors and thereby peak fault currents.

Sammendrag

I denne masteroppgaven ble en mulig løsning på hvordan en jack-up rig kan kobles til en ekstern kraftforsyning foreslått. Ved å ta utgangspunkt i hvordan et kraftsystem på en typisk jack-up rig ser ut, ble en passende løsning foreslått. Løsningen består av en tre-viklings transformator, og en frekvensomformer bestående av en tolv-puls likeretter og en vekselretter. Det var nødvending med en frekvensomformer grunnet ulik frekvens på den eksterne kilden, og jack-upen. I tillegg ble ett enkelt overstrøms relé, og filtre dimensjonert og designet.

Etter at det teoretiske grunnlaget for oppgaven ble presentert, ble en modell av den foreslåtte løsningen laget i Matlab/Simulink for å kunne teste og verifisere løsningen.

Det ble antatt at den eksterne forsyningen hadde ett stivt nett, og denne ble derfor modellert som en spenningskilde. Den eksterne forsyningen forsyner jack-upen gjennom en undervannskabel med et spenningsnivå på 36 kV, og frekvens 50 Hz. Kabelen ble modellert som en RL ekvivalent, basert på en passende kabel fra Nexans. En modell av en tolvpulslikeretter ble laget ved bruk av to ferdiglagde sekspulslikerettere koblet i serie. Tolv pulser ble brukt for å minimere rippel på DC skinnen. Filteret på DC skinnen ble dimensjonert analytisk med hensyn på tillatt strøm og spennings rippel. De resulterende verdiene var: induktans, L = 13.63 mH og kapasitans, C = 1.2 mF.

En to-nivå spenningskildeomformer ble benyttet for å konvertere DC til 60 Hz AC. Kontrollsystemet var basert på velutprøvde metoder, med en ytre spenningskontroll løkke, og en indre strømkontroll løkke. Kontrollen ble foretatt i et d-q referanse system slik at PI regulatorer kunne brukes. Regulatorene ble stilt inn ved bruk av pol plassering.

Utgangsfilteret på vekselretteren ble stilt inn for å fjerne de mest dominante harmoniske ordner fra vekselretteren. En knekkfrekvens på ω_o= 1257 [rad/s], med induktans L = 6.3 mH, og kapasitans, C = 100.36 µF gav god dempning.

Alle simuleringer der systemet var i stabil tilstand var suksessfulle med hensyn på harmonisk forvrengning, spenningsnivå og frekvens. Den største THD observert på lastsiden var i strømmen på høyspenningstavlen, med en THD = 0.59 %. I tilførsel kabelen var det en strøm THD = 9.28 %. Dette skyldes tolvpulslikeretteren samt mangelen av et filter.

I løpet av simuleringene med forskjellige lastscenarier førte en stegendring av lasten til en spenningsdypp på 20 V, og en overstrøm på rundt 1500 A. Under simularing av en lineær rampelast, med en endring i lasteffekt på $\frac{dP}{dt}$ = ± 6 MW/s, og endring i reaktiv lasteffekt på $\frac{dQ}{dt}$ = ± 4 MVAr/s, greide forsyningen å forsyne lasten tilfredstillende, og uten transienter.

Feilsimuleringer ble gjort med en trepolet kortslutning på forskjellige steder i jack-up riggens AC system, og en kortslutning av DC skinnene i frekvensomformeren. Ingen av feilene på lastøyene førte til noe overstrøm i sammenkoblingen. Den største feilstrømmen var på 159.2 kA ved en kortslutning på terminalene til vekselretteren. Den initiale strømtoppen ved feil på AC systemet skyldes filterkondensatorene på utgangen av vekselretteren. En kortslutning av vekselretterbryterene viste seg å være kritisk. Dette førte til en strømtopp på 747 kA, noe som

ville ødelagt bryterne. Kortslutningen på DC skinnen hadde en strømtopp på 23 kA, og ville sannsynligvis ødelagt diodene i likeretteren. Overstrømsvernene viste seg suksessfulle, og greide å bryte feilstrømmene. Selektivitet var også ivaretatt.

Ved å studere resultatene er det åpenbart at den foreslåtte løsningen fungerer som tiltenkt under normal drift. En fler-nivå omformer burde dog brukes for å minimere filterkondensatorene og dermed strømtopper ved feil.

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Nomenclature

Definition	Abbreviation
Low voltage	LV
Medium Voltage	MV
High Voltage	HV
Alternating Current	AC
Direct Current	DC
Insulated Gate Bipolar Transistor	IGBT
Metal Oxide Field Effect Transistor	MOSFET
Root Mean Square	RMS
Proportional Integral	PI
Per Unit	pu
Voltage Source Converter	VSC
Equation	Eq.
Cross-Linked Poly-Ethylene	XLPE
Phase Locked Loop	PLL
Total Harmonic Distortion	THD
Power factor	Pf
Pulse Width Modulation	PWM

1 Introduction

1.1 Motivation for Work

The focus on global warming and climate change in recent years, along with the global dependence on fossil fuel, has led to an increased focus on limiting emission associated with the Norwegian oil and gas industry. One of the most debated efforts in this context is the electrification of offshore units. This can either by done via a shore connection from land, or from an offshore power production unit. The possibility of an external supply is also advantageous because of the increased flexibility, reduced weight, reduced deck space usage and possible reduced cost. In either case, the offshore oil and gas units need a reliable, economical, and feasible way of interconnecting to the external power production units. This work tries to make one such solution.

1.2 Problem Description

This work studies how to interconnect a jack-up rig power system to an external power supply. A possible solution will be proposed. The solution has to be capable of supplying the entire platform, and perform equally or better than the existing power supply on the platform with respect to voltage and current distortion, power quality, and system behaviour during faults. The solution and a simplified jack-up rig power system are to be modelled in Matlab/Simulink using the SimPowerSystems extension.

After creating the model, the model is to be tested by running simulations with various load and fault scenarios. The purpose of the simulations are to test how the solution performs during both normal and extreme situations and to identify possible weaknesses with the solution.

Although this thesis studies the interconnection of an external power supply to a jack-up rig, the principles presented are applicable to many different types of offshore units, such as semi-submersibles; floating production, storage and offloading (FPSO) vessels; and drilling ships.

The system studied is not an actual system, but conceptual, and the goal of this work is therefore not to recreate the exact behaviour of a real system, but highlight the challenges related to creating and running a system on an external power supply.

1.3 Limitations of Work

- Inrush current protection, i.e. pre-magnetizing, pre-energizing and soft start circuits, are not studied. A real system would probably have such capabilities, and inrush currents during system start-up is therefore not studied in detail.
- The contribution and behaviour of the interconnection is studied solely, and it is therefore assumed that there is no jack-up rig side power production.
- Only the jack-up rig side of the interconnection is studied in detail.
- Only overcurrent protection is studied. This with the purpose of studying the behaviour and impact fault clearing has on system performance and stability.

- A discrete solver with variable step-size is used when simulating the system. This means that some transients may fail to be registered and that inaccuracies may occur in system control, performance and parameter measurements. In spite of this, the simulation results are considered valid for studying power flow, faults and tendencies. It will be pointed out in the relevant simulations where the simulation tool may be inaccurate, and what the consequences are.
- Many choices of design parameters depend on cost versus desired system performance. The choices made in this work seek to satisfy a balance between the two.

2 Theoretical Background

2.1 Jack-up Rigs

The jack-up rig, depicted in Figure 1, is the smallest class of offshore drilling platforms. As the name implies, the jack-up rig has legs attached to the buoyant hull that is used elevate, or jack, the rig up and above the sea thereby anchoring it. These self-elevating jack-ups are the most common offshore drilling unit [1]. Besides drilling, the mobile jack-up rigs are also used for maintenance of other offshore installations such as servicing fixed platforms or wind turbines. Based on experience, the weight of equipment on-board is approximately proportional to cost and should be kept at a minimum. Additionally, as jack-up rigs are relatively small and mobile, the deck space is limited.

Figure 1 – A jack-up rig

2.2 Jack-up Rig Loads

The jack-up rig load profile depend on the operational status. As the jack-up rig is drilling most of the time, and it is during drilling that the load demand are the greatest, this will be the dimensioning load profile. When drilling, a base load consisting of the drilling loads, hotel load, control system load and various other minor loads exists. The drilling loads consisting of the draw works, top drive, mud pumps and other auxiliary loads are mostly inverter fed, variable frequency induction motors. Based on experience, the total load is assumed to be 15 MW, with a power factor, $\cos(\varphi)$ = 0.9, so that the total nominal apparent power, $S \approx 16.6$ MVA.

Another load scenario is the “tripping” operation where the drill bit is replaced. The drill string is then raised one 30 m segment at a time until the whole string is up. The drill bit is replaced, and the drill string is then lowered in the same manner. This gives a highly dynamic load pattern that the power supply should be designed to accommodate.

Additionally, some jack-up rigs are installed with thrusters to assist in towing [2].

2.3 External Power Supply

The external power supply could be a shore connection connected through a HVAC or HVDC cable, it could be an offshore wind farm, or, as in this, a large production platform with gas turbines. The gas turbines on the production platform are rated at 25 MW, and the synchronous generators has a sub transient reactance of 18 %. Throughout this thesis, it is assumed the production platform has a power management system that maintains the supply voltage constant. This minimizes the jack-up side control complexity and equipment requirements, and thereby weight and cost. From the production platform a HVAC subsea cable, connected through transformers at both ends, supplies the jack-up rig.

2.4 Subsea Cable

The jack-up rig is connected to the external power supply by a subsea cable. For subsea medium voltage (MV) applications, one common alternative is a cross-linked poly-ethylene (XLPE) cable.

The modelling of a subsea cable can be performed with different levels of accuracy. According to [3], the length and voltage of the line determines how the line can be modelled with acceptable accuracy. For lines less than 80 km long, or if the voltage is not over 69 kV, the line capacitance can often be ignored without much error. The model then consist of a series impedance with a resistance and an inductance.

For lines above 80 km and below 250 km, a π-equivalent line model may be used [3]. For lines longer than 250 km, distributed parameters must be considered [3].

One challenge associated with the subsea cable are that harmonic currents injected into the cable may cause a parallel resonance due to the shunt capacitance of the subsea cable interacting with the inductance of the power system [4]. This will however not occur if the short line model is used.

2.5 Transformers

The system includes various transformers. The theoretical basis for modelling is described in the following.

2.5.1 Two Winding Transformer

The two winding transformer is used to connect low voltage loads to the main switchboard. The equivalent impedance circuit is illustrated in Figure 2.

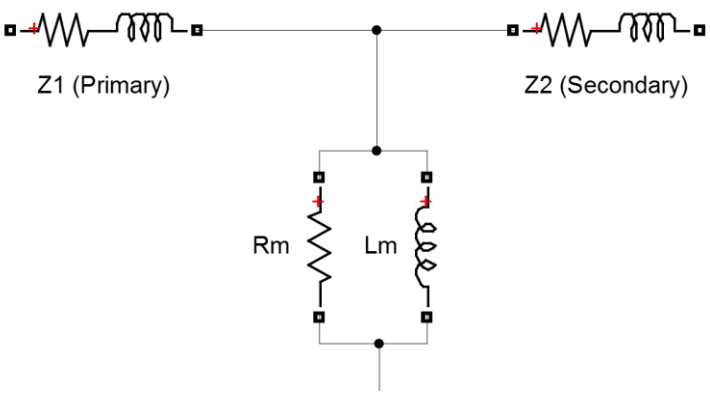


Figure 2 – Two winding transformer equivalent impedance circuit.

A simple approach to determine the winding resistances and inductances is assuming equal winding impedances in per unit. Voltage level conversion of the impedances is then unnecessary as this is handled implicitly in the per unit system [5]. Using a transformer also provides galvanic isolation, and as both loads and transformer secondary winding is isolated from ground, ground fault current loops are interrupted.

2.5.2 Three Winding Transformer

A twelve-pulse rectifier is used in the interconnection. When using a twelve-pulse rectifier, six input phases are needed. To create six phases, a three winding, Δ/Y/Δ connected transformer is used as input to the rectifiers. The delta connected tertiary winding provides a 30-degree voltage phase shift, thereby creating six output phases. According to [6], if all windings are connected to the grid, the fictitious per winding, per phase, equivalent impedances in linear conditions can be calculated by:

$$\bar{Z}_1 = \frac{1}{2}(\bar{z}_{12} + \bar{z}_{13} - \bar{z}_{23}) \quad \textit{Eq. 1}$$

$$\bar{Z}_2 = \frac{1}{2}(\bar{z}_{12} - \bar{z}_{13} + \bar{z}_{23}) \quad \textit{Eq. 2}$$

$$\bar{Z}_3 = \frac{1}{2}(-\bar{z}_{12} + \bar{z}_{13} + \bar{z}_{23}) \quad \textit{Eq. 3}$$

Where:

- $\bar{Z}_1, \bar{Z}_2, \bar{Z}_3$ are the primary, secondary and tertiary transformer impedances [Ω], respectively.
- $\bar{z}_{12}, \bar{z}_{13}, \bar{z}_{23}$ are the primary to secondary, primary to tertiary and secondary to tertiary transformer impedances [Ω], respectively.

The three winding transformer impedance equivalent circuit are depicted in Figure 3:

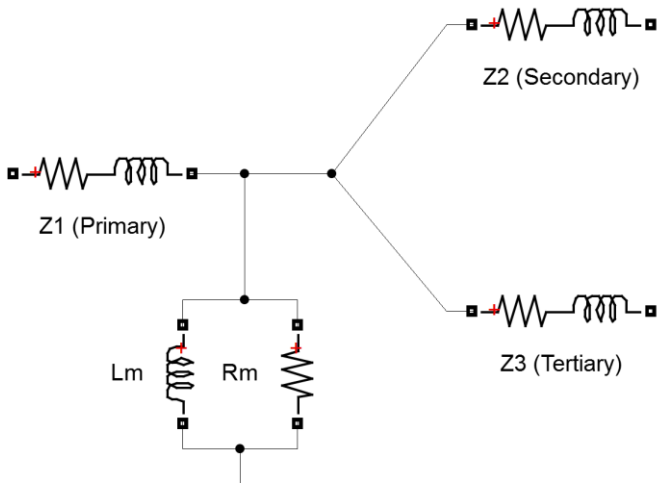


Figure 3 – Three winding transformer equivalent impedance circuit

A consequence of using this type of transformer is that with a delta-connected primary winding, excitation unbalances are avoided. The non-sinusoidal excitation currents can be taken from the supply system so that there is a complete ampere-turn balance [7]. Additionally, third harmonic currents (does not sum up to zero) and the multiples are trapped in the delta connection preventing third harmonic content reaching the supply, but causing heating of the transformer windings. In addition, a Y connected secondary winding provides access to a common neutral point if this is desired.

2.6 System Description

Traditionally, power systems on jack-up rigs have used alternating current (AC) on the main distribution, but direct current (DC) on the drilling load bus, with loads connected through inverters. These systems typically includes both high and low voltage sections. The system studied in this thesis are simplified and conceptual based on experience of how typical power systems on offshore rigs are designed. As the interconnection of the rig to an external supply are the focus of this thesis, the rest of the system are not discussed in detail. A simplified conceptual single line diagram of the system is illustrated in Figure 4:

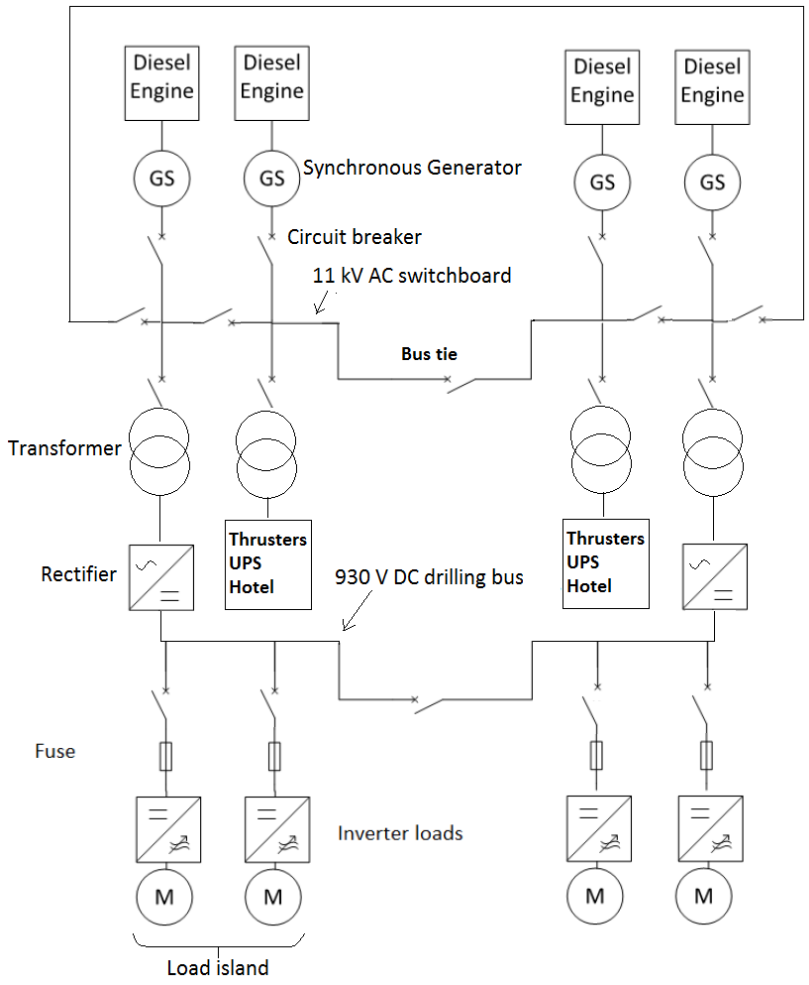


Figure 4 – Single line simplified conceptual diagram of jack-up rig AC power system

The simplified single line diagram depicts four generators, but the actual number of generators may differ. The generators are connected to an 11 kV AC switchboard through circuit breakers. Depending on the application and design of the system, the high voltage switchboard may be omitted by placing transformers at the power feeds. The switchboard is separated into segments of two diesel-generator sets pr. segment. These segments are called islands. The islands are interconnected through bus-ties that may be open or closed depending on the system state. From the main switchboard step-down transformers supplies power at various voltage levels to the various loads. The inverter drilling loads are connected to a DC bus to allow variable frequency operation. The DC bus islands are also separated by a bus tie. These are depicted at the bottom of Figure 4. Additionally, there is a conductor

connecting the endpoints of the high voltage switchboard. This may be connected to redirect power in case of a fault or maintenance.

2.7 Interconnecting an External Power Supply to the Jack-up Rig Power System

2.7.1 Interconnection Topology

The proposed interconnection layout simplified single line diagram is depicted in Figure 5:

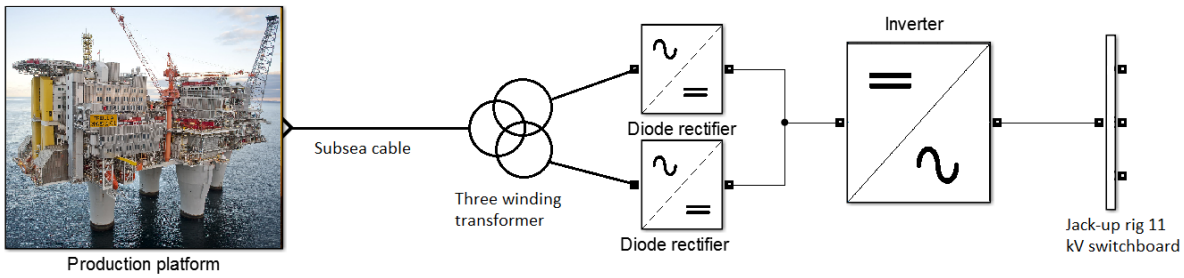


Figure 5 – Jack-up rig interconnection single line diagram

Because many of the jack-up rigs are designed to operate at 60 Hz, but needs to be able to be connected to a 50 Hz supply, a frequency changer is needed. A frequency changer adds flexibility if the jack-up rig is to operate worldwide.

To realize this the subsea cable from the production platform is feed into a three winding transformer. The three winding transformer steps down the high voltage from the subsea cable and creates six output phases. This is done to minimize DC link ripple in the frequency changer. Two full bridge diode rectifiers then rectify the voltage, before a voltage source converter (VSC) converts the DC to 60 Hz AC.

Redundancy is important in offshore installations. Therefore, a possible alternative to a single cable is to have another cable connected to yet another offshore unit and so on. By making a grid in this way, the power has two feeding points at each unit and a failure of one cable or interconnection will not lead to a blackout. An example of this kind of interconnection topology is the DNV “OPera” project [8].

Having a sole converter supplying the entire jack up rig load is also risky, as a failure of this will lead to a blackout unless the jack up rig has adequate local backup generators or UPS systems. Extra interconnecting converters with redundant power handling capabilities could then be considered.

As Figure 4 illustrates, the grid layout is radial, with distributed loads connected in parallel at the main switchboard separated into islands by bus ties. The interconnection to the external power supply should therefore have at least one feeder from the interconnection to each island.

2.7.2 Twelve Pulse Series Connected Rectifier

To improve the DC output voltage and current waveforms, a twelve-pulse diode rectifier is used. It consist of two three-phase full bridge diode rectifiers connected in series. The rectifier is supplied by the six output phases of the three winding transformer described in 2.5.2, thereby supplying twelve output pulses. A series connection is selected to avoid problems associated with paralleling of diodes.

2.7.3 DC Link Filter Inductor

A DC link filter inductor is used to reduce harmonics on the AC sides, and improve inverter operation. The inductance, *L*, as a function of transformer output line-to-line voltage, V_{LL} [V], supply frequency, ω [rad/s] and allowed current ripple, Δi_L [A], is calculated in Appendix G. The resulting equation is presented in Eq. 4:

$$L = \frac{0.00654972 V_{LL}}{\omega \Delta i_L} \ [H] \qquad \textit{Eq. 4}$$

2.7.4 DC Link Filter Capacitor

A filter capacitor is used to minimize voltage ripple. Because the inverter is controlled as a voltage source inverter, the capacitor should ensure a quite constant DC link voltage.

According to [9], the dc-link voltage variation is generally caused by front end and inverter power unbalance, and the filter capacitance, C, can be calculated as:

$$C = \frac{P_{max}}{(V_{do}\Delta V \pm \frac{1}{2}\Delta V^2) f_{sw}} \ [F] \qquad \textit{Eq. 5}$$

Where:

- P_{max} is the maximum(nominal) load power [MW]
- ΔV is the allowed voltage change [V]
- f_{sw} is the inverter switching frequency [Hz]

2.7.5 Inverter

2.7.5.1 Topology

A two-level VSC is used to convert DC to AC. The topology is depicted in Figure 6:

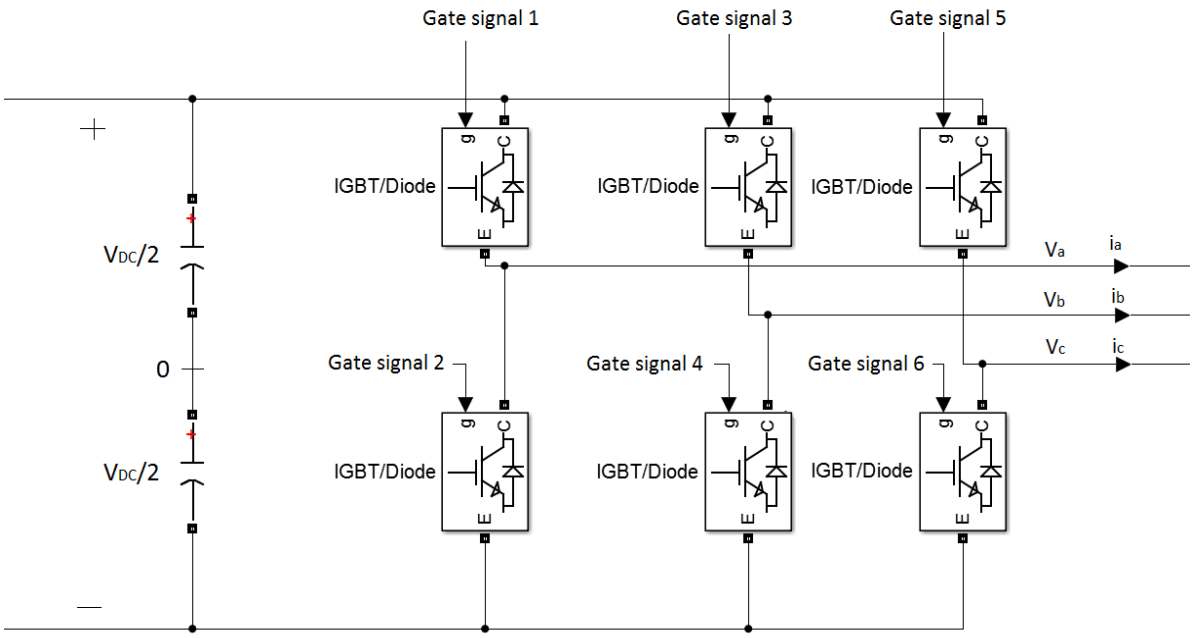


Figure 6 – Two level voltage source converter

The two level VSC consist of three half-bridge converters, one for each phase. It is called two-level VSC since each of its AC-side terminals can assume either of the voltage levels $-V_{DC}$ and V_{DC} [10]. The state of each switch is controlled by the gate signal, which in turn are determined by the control system. Depending on the application, more complex topologies, such as a three level "Neutral point clamped" or multilevel topologies can be used.

2.7.5.2 IGBT Valves

Insulated gate bipolar transistor (IGBT) technology has come a long way, and IGBTs with several kilo volts blocking voltage, and more than a kilo ampere of collector current are commercially available. However, for high power applications these IGBTs may not suffice. It is then possible to connect two or more IGBTs in parallel to increase the current handling capability [11]. A disadvantage of this is the possibility of uneven split in losses due to difference in IGBT characteristics. Similarly, to increase the voltage handling capability, several IGBTs can be connected in series [12]. This series connection is then called a valve. The most extreme example of this being IGBTs in HVDC applications, where hundreds of IGBTs may be connected in series to achieve the desired voltage level [13]. One challenge associated with this is that all the series connected IGBTs in one valve needs to be switched at the same time [10]. In addition, parallel resistors should be employed to enforce static voltage sharing, and RC snubber circuits should be employed to equalize voltage rate of rise [14].

For safety, [15] recommends that the maximum peak voltage the IGBT has to block, $V_{o,max}$, should not exceed 80 % of the IGBT rated voltage, V_{CES}, in an AC system. For n_{sd} series connected devices this yield:

$$\frac{V_{o,max}}{n_{sd}} \leq 0.8V_{CES} \qquad \textit{Eq. 6}$$

If one series connected IGBT fails, the inverter should still be able to function. This can be achieved by using press pack IGBTs. Using press pack IGBTs, one or more extra IGBTs can be installed in each valve for redundancy. If a press pack IGBT fails, it short circuits, and the other IGBTs are still useable [16], [17]. The faulty IGBT can then be replaced during the next maintenance of the inverter.

2.7.5.3 Pulse Width Modulation

To control the state of the IGBT switches the sinusoidal pulse width modulation (PWM) technique is employed. A sinusoidal reference voltage signal, $V_{control}$ [V], is compared to a triangular carrier signal, V_{tri} [V], as depicted in Figure 7. $V_{control}$ is supplied by the control system that controls the amplitude and frequency of this signal. The state of the switches in each inverter leg is then determined as follows: If $V_{control} > V_{tri}$, the upper switch of is on, else the lower switch is on. In this manner, an alternating output voltage in synthesized as the width and polarity of the resulting output rectangular pulses is varied.

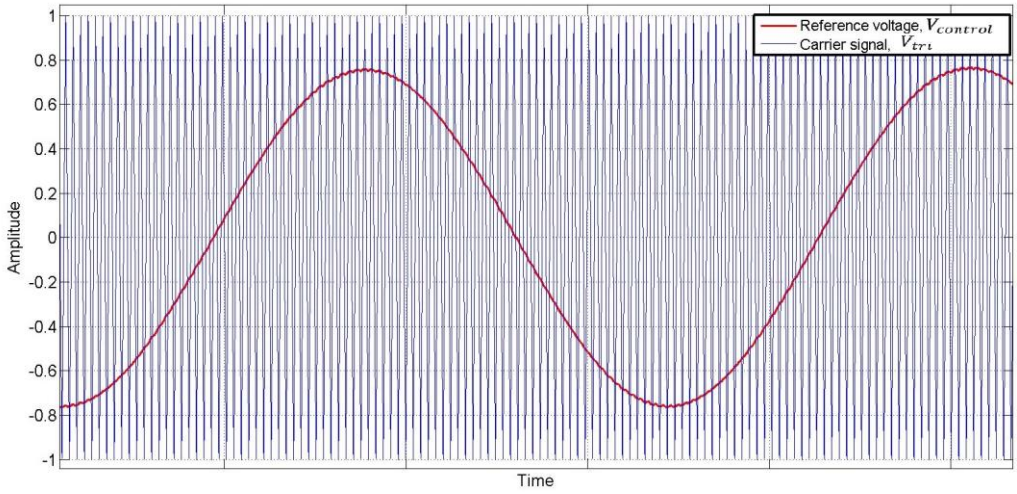


Figure 7 – Sinusoidal pulse width modulation.

Note that the amplitude may differ from the above figure.

2.7.5.4 DC Link Voltage

According to [18], the DC link voltage level has to satisfy:

$$(\hat{V}_{AN})_1 = m_a \frac{V_{DC}}{2} \qquad \textit{Eq. 7}$$

Where:

- $m_a = \frac{\hat{V}_{control}}{\hat{V}_{tri}}$, is the amplitude modulation ratio, i.e. the ratio between the peak of the control signal, $\hat{V}_{control}$, and the peak of the carrier signal, $\hat{V}_{tri}$.
- $(\hat{V}_{AN})_1$ is the peak value of the fundamental frequency component in one inverter leg

To operate in the linear region m_a is constrained to $0 < m_a \leq 1$. Operating in the linear region minimizes distortion of the output voltage [18].

2.7.5.5 Switching Frequency

The frequency modulation ratio, m_f, is defined as [18]:

$$m_f = \frac{f_s}{f_1} \qquad \textit{Eq. 8}$$

Where:

- f_s is the switching frequency [Hz]
- f_1 is the output voltage fundamental frequency [Hz]

According to [18], the choice of switching frequency depend on several factors. One the one hand, switching losses increases with increasing frequency, but on the other hand, filtering of higher frequency harmonics are easier. The switching also causes audible noise between 6 kHz and 20 kHz, so this interval should be avoided if noise is an issue. Additionally, using an integer value of m_f causes the carrier and control signal to be synchronous. This is called synchronous PWM, and by using synchronous PWM, undesirable sub-harmonics are avoided. Finally, m_f should also be an odd multiple of three. This result in odd symmetry and half-wave symmetry and the even harmonics are cancelled.

2.7.5.6 Inverter Control

As the VSC in the interconnection is considered the only power source, and the jack-up rig network is passive, the main purpose of the VSC is to maintain the grid voltage and frequency. If the network had other power supplies besides the external feed, e.g. diesel generators running, the external power supply would need synchronization with the jack-up power system. This could be achieved by using a phase locked loop (PLL), but as there are no jack-up side power generation in this model, the synchronization is omitted. If there were more than one power supply, another control strategy, such as controlling the output power, would be desirable [10], [19]. This allows the use of load sharing strategies and power management, which is necessary with multiple power sources acting in the same system. Examples of such strategies are the droop control method, and the master-slave control method.

A common strategy to control the inverter switching is by the use of the Park transform [10]. This transforms sinusoidal AC signals into DC signals and therefore allows control by PI controllers [10]. A “dq0 transform” block in Simulink is used to perform the transform. Some variations of the transform exist. As described in Appendix E, the transform can be made voltage magnitude invariant. This version of the transform is the same as used in the Simulink block [20] and is used in this work.

A proven and well-tested way of controlling a VSC is by using an in a cascaded control structure consisting of an outer voltage control loop and an inner current control loop. The purpose of the voltage control loop is to control the grid voltage by controlling output filter capacitor voltage, i.e. the line to neutral voltage magnitude, and to control output frequency. The purpose of the current control loop is to control the inverter output current. This is done by controlling the output filter inductor current. The reason for controlling the current in this

standalone mode is to protect the inverter IGBTs from overloading [21], [19]. A current limitation is then imposed on the current controller. A control scheme based on the control schemes presented in [10], [22], [23] and [24] are used. As a basis for design, instantaneous switching i.e. no blanking time, is assumed. The inverter output system overview is depicted in Figure 8:

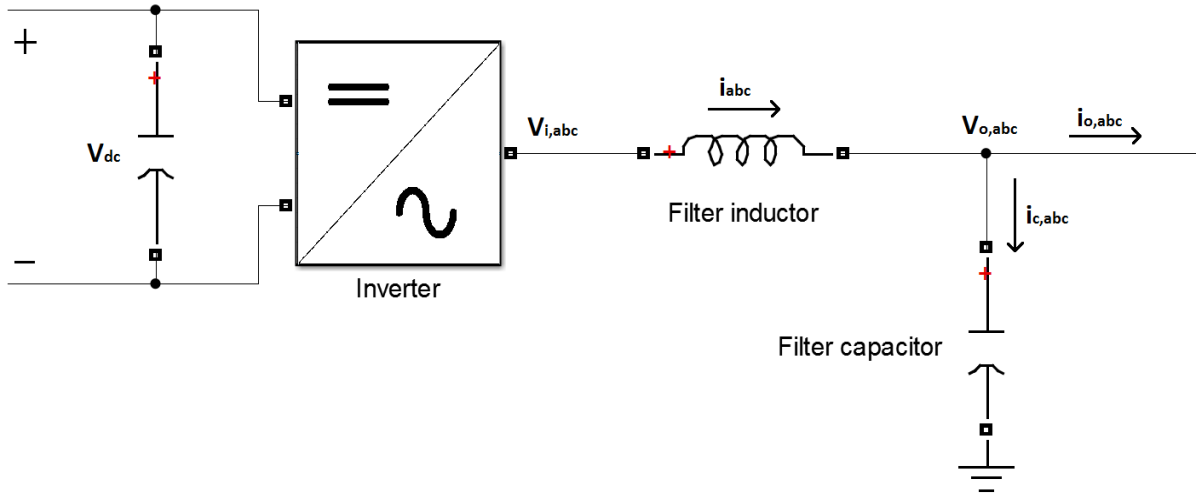


Figure 8 – Single line diagram of inverter and output filter

The basis for the control are derived:

The expressions for three balanced sinusoidal entities are:

$$f_a = \hat{f}\cos(\omega t + \theta_0) \qquad \textit{Eq. 9}$$

$$f_b = \hat{f}\cos(\omega t + \theta_0 - \frac{2\pi}{3}) \qquad \textit{Eq. 10}$$

$$f_c = \hat{f}\cos(\omega t + \theta_0 - \frac{4\pi}{3}) \qquad \textit{Eq. 11}$$

Where *f* represents voltages or currents, ωt is the angle [rad], and θ_0 is the initial angle [rad].

According to [10] , Eq. 9, Eq. 10 and Eq. 11 can be represented as a space vector by:

$$\vec{f}(t) = \frac{2}{3}\left[f_a(t)e^{j0} + f_b(t)e^{j\frac{2\pi}{3}} + f_c(t)e^{j\frac{4\pi}{3}}\right] \qquad \textit{Eq. 12}$$

This can be decomposed into a real and an imaginary component in a stationary $\alpha - \beta$ reference frame as:

$$\vec{f}(t) = f_\alpha(t) + jf_\beta(t) \qquad \textit{Eq. 13}$$

Which can be transformed onto a rotating *d-q* axis reference frame as:

$$\vec{f}(t) = (f_d(t) + jf_q(t))e^{j\theta(t)} \qquad \textit{Eq. 14}$$

Where $\theta(t)$ is the angle [rad] at time *t.*

The magnitude of $\vec{f}(t)$ is then:

$$|f| = \sqrt{f_d^2 + f_q^2} \qquad \textit{Eq. 15}$$

The generic filter capacitor current equation are:

$$i_C = C\frac{dv_o}{dt} = i - i_o \qquad \textit{Eq. 16}$$

In addition, neglecting inductor resistance, the generic inductor voltage equation are:

$$v_L = L\frac{di}{dt} = v_i - v_o \qquad \textit{Eq. 17}$$

Where:

- i_C is the capacitor current [A]
- v_o is the capacitor voltage [V]
- i is the inverter output current [A]
- i_o is the load current [A]
- v_L is the inductor voltage [V]
- v_i is the inverter terminal voltage [V]
- C is the filter capacitor capacitance [F]
- L is the filter inductor inductance [H]

All voltages are line to neutral and all currents are phase currents.

Representing Eq. 16 and Eq. 17 as space vectors:

$$C\frac{d\vec{v}_o}{dt} = \vec{\imath} - \vec{\imath}_o \qquad \textit{Eq. 18}$$

$$L\frac{d\vec{\imath}}{dt} = \vec{v}_i - \vec{v}_o \qquad \textit{Eq. 19}$$

Inserting Eq. 14 in Eq. 18 and Eq. 19, yields:

$$C\frac{d(v_{od} + jv_{oq})e^{j\theta(t)})}{dt} = (i_d + ji_q)e^{j\theta(t)} - (i_{od} + ji_{oq})e^{j\theta(t)} \qquad \textit{Eq. 20}$$

$$L\frac{d(i_d + ji_q)e^{j\theta(t)})}{dt} = (v_{id} + jv_{iq})e^{j\theta(t)} - (v_{od} + jv_{oq})e^{j\theta(t)} \qquad \textit{Eq. 21}$$

Carrying out the differentiations with $\frac{d\theta(t)}{dt} = \omega$ [rad/s], eliminating all the exponential terms and separating the real and imaginary components yield:

$$C\frac{dv_{od}}{dt} = C\omega v_{oq} + i_d - i_{od} \quad \textit{Eq. 22}$$

$$C\frac{dv_{oq}}{dt} = -C\omega v_{od} + i_q - i_{oq} \quad \textit{Eq. 23}$$

$$L\frac{di_d}{dt} = L\omega i_q + v_{id} - v_{od} \quad \textit{Eq. 24}$$

$$L\frac{di_q}{dt} = -L\omega i_d + v_{iq} - v_{oq} \quad \textit{Eq. 25}$$

The control variables are the inverter voltages and currents: i_d, i_q, v_{id} and v_{iq}, respectively. For convenience the inverter are controlled using a per unit system. The base values used are given in Appendix C. Expressing Eq. 22, Eq. 23, Eq. 24 and Eq. 25 in the Laplace domain, and dividing by the base values, i_{base} and v_{base}, the per unit expressions becomes:

$$\frac{sC_{pu}v_{od,pu}(s)}{\omega_{base}} = C_{pu}\omega_{pu}v_{oq,pu}(s) + i_{d,pu}(s) - i_{od,pu}(s) \quad \textit{Eq. 26}$$

$$\frac{sC_{pu}v_{oq,pu}(s)}{\omega_{base}} = -C_{pu}\omega_{pu}v_{od,pu}(s) + i_{q,pu}(s) - i_{oq,pu}(s) \quad \textit{Eq. 27}$$

$$\frac{sL_{pu}i_{d,pu}(s)}{\omega_{base}} = L_{pu}\omega_{pu}i_{q,pu}(s) + v_{id,pu}(s) - v_{od,pu}(s) \quad \textit{Eq. 28}$$

$$\frac{sL_{pu}i_{q,pu}(s)}{\omega_{base}} = -L_{pu}\omega_{pu}i_{d,pu}(s) + v_{iq,pu}(s) - v_{oq,pu}(s) \quad \textit{Eq. 29}$$

Where *s* is the Laplace operator.

As seen in Eq. 26, Eq. 27, Eq. 28 and Eq. 29, , the state variables v_{od}, v_{oq}, i_d and i_q is dependent on v_{oq}, v_{od}, i_q and i_d, respectively. Additionally, all state variables depend on the load. To mitigate this effect and allow independent control of the d and q axis components, feed-forward of the load and cross coupling terms are added to the control loops as illustrated in Figure 9. The feed forward terms are considered ideal, and are therefore eliminated from the above equations. Furthermore, by assuming a fast current control loop and neglecting inverter time delay, the current loop transfer functions can be approximated by a first order time constant, τ_{eq}, [10] so that:

$$i_{dq,pu}(s) \approx \frac{1}{1+\tau_{eq}s} * i_{dq,ref,pu}(s) \quad \textit{Eq. 30}$$

Inserting this in Eq. 26, Eq. 27 and rearranging, rearranging Eq. 28 and Eq. 29, and removing all feed forward terms, yield the following transfer functions:

$$\frac{v_{o,dq,pu}(s)}{i_{dq,ref,pu}(s)} \approx \frac{1}{1+\tau_{eq}s} * \frac{\omega_{base}}{sC_{pu}} \qquad \textit{Eq. 31}$$

And:

$$\frac{i_{dq,pu}(s)}{v_{i,dq,pu}(s)} \approx \frac{\omega_{base}}{sL_{pu}} \qquad \textit{Eq. 32}$$

Where:

- $i_{dq,ref,pu}(s)$ is the d or q axis output of the voltage PI controller, with the feed forward terms removed.
- $v_{i,dq,pu}(s)$ is the d or q axis output of the current PI controller, with the feed forward terms removed, i.e. the PWM modulating signals controlling the input to the system.

This means that $v_{o,dq,pu}(s)$ can by controlled by the output of the voltage PI controllers, $i_{dq,ref,pu}(s)$; and that $i_{dq,pu}(s)$ can be controlled by the output of the current PI controllers, $v_{i,dq,ref,pu}(s)$.

The corresponding control block diagram (with some additions) is depicted in Figure 9.

The voltage control loop produces the current references, and the current control loop produces the PWM voltage references i.e. the modulating d and q axis signals. These references are transformed from the d-q plane back to abc per unit quantities which are compared to a triangular carrier signal with amplitude 1 and frequency equal to the switching frequency as described in 2.7.5.3.

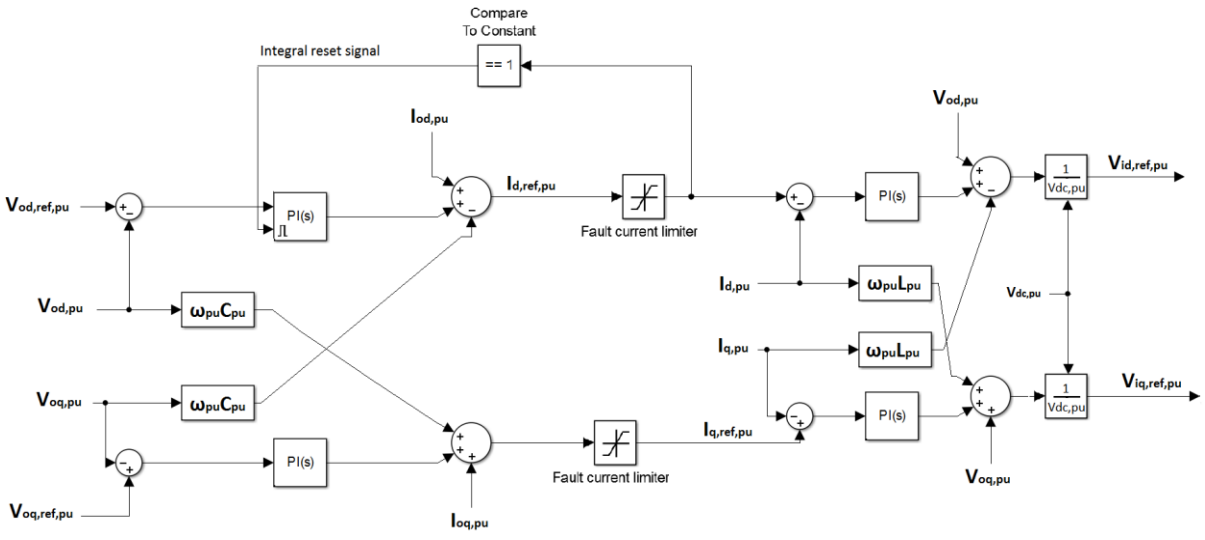


Figure 9 – Inverter control block diagram. All quantities in per unit.

A saturation block is added to the current references in the control system to protect the IGBTs from overcurrent and to limit fault currents. During a short circuit, the inverter will be unable to sustain the output voltage due to the saturation. This will lead to a windup of the integrator in the d-axis voltage PI controller. To avoid this, the integral is reset continuously while the current reference is saturated. This effectively makes the PI controller a P controller, and avoids large voltage offsets in the period after the fault is cleared.

As the DC voltage level is not perfectly stable, the voltage reference signals are divided by the measured DC voltage in per unit. The DC voltage base is chosen as the nominal DC voltage. By doing this the VSC controller is decoupled from the DC voltage level, which is done to make the controller more accurate.

2.7.5.7 Tuning of PI Controllers

The PI controllers are tuned using pole placement. The voltage control are the slowest and hence the poles are placed closest to the right half plane. The detailed tuning procedure of the controllers is included in Appendix D. The resulting proportional gain, K_p, and integral gain, K_i, values are presented in Table 1.

Controller	K_p	K_i
Voltage	0.3496	75.4877
Current	3.3781	7294

Table 1 – PI controller gains.

2.7.6 Inverter Output Low Pass LC Filter

A low pass LC filter is used on the inverter output to remove dominant load side harmonic components. The filter inductance, *L*, and capacitance, *C,* can be determined designing for minimum reactive power or system time constant, the cost function and total harmonic distortion (THD) [25]. On the one hand, to avoid voltage distortion, the filter capacitance should be maximized, and the inductance minimized when selecting the cut-off frequency. On the other hand, this means that the inverter has to supply more reactive power, thereby reducing the inverter active power capacity [25]. Here, the THD requirement is considered. The per phase filter diagram is depicted in Figure 8. The LC filter forms a voltage divider. Neglecting inductor resistance, this is described in the Laplace domain as:

$$v_o(s) = \frac{\frac{1}{sC}}{\frac{1}{sC} + sL} v_i(s) => \frac{v_o(s)}{v_i(s)} = h(s) = \frac{1}{s^2LC + 1} \quad \textit{Eq. 33}$$

The standard form of this equation is [26]:

$$h(s) = \frac{K}{\frac{s^2}{\omega_0^2} + 1} \quad \textit{Eq. 34}$$

Where:

- ω_o = The undamped resonance frequency [rad/s]
- K = Constant gain
- s = the Laplace operator

For this system, the resonant frequency, ω_o, equals the corner frequency [26]. However, choosing a corner frequency close to the fundamental frequency can boost the fundamental frequency component due to resonance. Therefore, the corner frequency should be several times larger than the fundamental frequency to avoid resonant voltages. Similarly, the corner frequency should be several times smaller than the switching frequency to provide good attenuation of the switching harmonics. After the corner frequency, because of the two integral terms, the asymptote drops with 40 dB/decade. Solving Eq. 33 and Eq. 34 for ω_o:

$$\omega_o = \frac{1}{\sqrt{LC}} \qquad \textit{Eq. 35}$$

The size of *L* are determined by the allowed current ripple. The inductor value are determined as described in [25], using:

$$L = \frac{1}{6}\frac{V_{DC}\delta}{\Delta I f_s} \qquad \textit{Eq. 36}$$

Where:

- L = Filter inductance [H]
- V_{DC} = DC link voltage [V]
- δ = Inverter duty cycle at maximum voltage output
- ΔI = Current ripple [A]
- f_s = Inverter switching frequency [Hz]

After this, the capacitance is determined using Eq. 35.

2.7.7 Faults

Faults at different locations in the jack-up rig AC system, and a bolted short circuit of the DC link is studied. The purpose is to study the reliability of the system feed by an external supply, the reliability of the interconnection, and identify critical faults. Therefore, only worst-case fault currents are studied. Additionally, the demands to fault protection has to be fulfilled. On the AC side, a three-pole short circuit of the phases, although not the most common fault, often yields the largest fault current [27]. As this is a symmetrical fault, it is unnecessary to use symmetrical components analysis while studying it. Additional AC side faults may be to-pole short circuit, or phase to ground faults. As the low voltage load side on jack-up rigs are isolated from ground, a single phase to ground fault will not cause a fault current because of the galvanic isolation provided by the transformer. A multiphase ground fault may however cause fault currents.

2.7.8 Fault Protection

To protect all loads and equipment against faults, and allow redirection of power, protection relays are installed at all interconnecting points. The protection layout is depicted in the simplified single line diagram in Figure 10, with only a few of the drilling loads included. Similar protection layout can be applied to all loads. In addition to the relay-controlled circuit breakers depicted, fuses could be considered as a backup at certain places. The relay protection can measure voltages, currents or impedance, and protect against overcurrent, over/under voltages.

The system topology is radially connected, so the nominal current in each branch is less than that of the inverter. In addition, there are multiple voltage levels in the system. This means that the tripping level of each relay has to be adjusted for this. The circuit breakers on the high voltage branches operates at the same voltage as the inverter, but only has to accommodate a portion of the current at nominal load and below. This allows the circuit breakers to be installed with a lower current handling capability and tripping level than the inverter current handling capability. The circuit breakers on the low voltage, load side of the transformers has to have a much higher nominal current than those on the high voltage side. The tripping level of these breakers then has to be below the corresponding inverter current handling capability on the high voltage side.

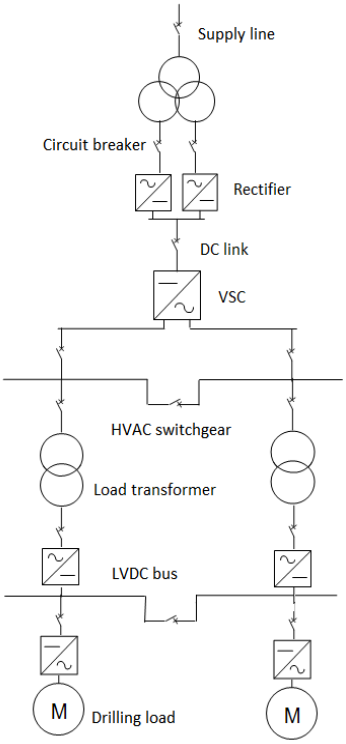


Figure 10 – Protection layout in simplified single line diagram

As an additional safety barrier, there are current limitations included in the inverter control system that limits the inverter current to rated current. Although the inverter output current is limited, the protection relay are still able to trip, because, as explained above, the system has a radial topology, and the inverter is therefor able to supply enough short circuit current to trip the relays. During a fault, other loads may experience a transient dip in power until the circuit breaker trips and steady state is restored.

In case of an inverter terminal fault, a separate fast acting detection system disconnects the inverter to protect the IGBTs. This is however, is a last resort, as disconnecting the VSC cuts all power to the jack-up.

Faults inside the frequency changer is also critical because, due to the large filter capacitors the initial currents are large and may destroy the frequency changer before any protection trips. Protection against faults on the DC link is also difficult, because the current does not have a natural zero crossing. Fault currents and arcs needs to be interrupted by other means. One solutions is to force the current to zero by employing parallel, pre-charged, capacitor that discharges opposing current into the arc hen the fault occurs [28]. Another solution is by employing fast acting IGBTs that open, and cuts the current. This is used in the intelligent load controller (ILC), a DC switch developed by Siemens.

There are also circuit breakers installed at the AC supply side of the rectifiers, cutting the supply line contribution to fault currents if necessary.

2.7.9 Selectivity

An important criterion when designing fault protection in a power system is to ensure selectivity. Selectivity means that only the fault protecting device closest to the fault trips, so that as much of the rest of the grid as possible still is operational [27]. In addition, if the fault protecting device closest to the fault fails to trip, the next series connected fault protecting device should trip, and so on. This is accomplished by letting the relay furthest away from the power supply should have the fastest tripping, and then increasing the time delay for each relay toward the supply.

It is important to protect the IGBTs in the VSC from overcurrent, so that the VSC still are able to supply power to the non-faulted part of the network after the fault. To accomplish this, all subsequent circuit breakers has to trip within the time dictated by the IGBT I^2t rating. This means that the circuit breakers detection time, movement time, and arc extinction time has to be smaller than the critical time before the IGBTs are destroyed.

2.8 Harmonics

When using non-linear elements in a circuit, such as power electronic converters, the voltage and current waveforms may become distorted with respect to a sinusoidal shape as illustrated in Figure 11:

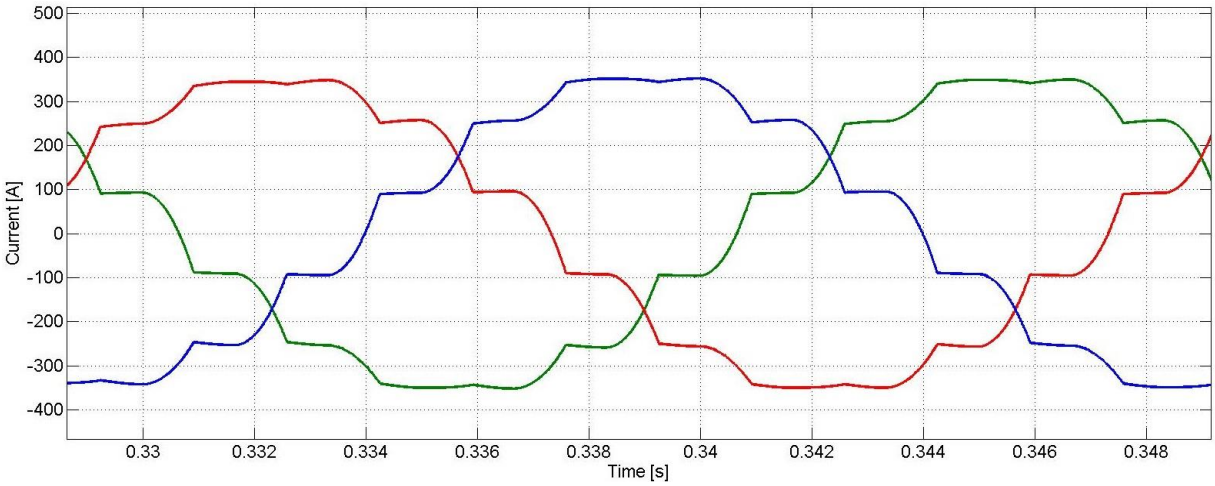


Figure 11 – Harmonics in the supply line currents of a twelve-pulse rectifier.

This distorted waveform can be described as the sum of many smaller sinusoidal waveforms at various frequencies. These waveforms are called harmonics. The frequency by which the distorted waveforms repeat are called the fundamental frequency [18], and all harmonic components are at integer multiples of this fundamental frequency [18]. The harmonics can be analysed by Fourier analysis [18]. An important design parameter when designing a power system is the total harmonic distortion (*THD*), which is defined as [18]:

$$\%THD_i = \sqrt{\sum_{h\neq 1}\left(\frac{I_{sh}}{I_{s1}}\right)^2} \quad \textit{Eq. 37}$$

Where the subscript i indicates the THD in current. I_{sh} is the line current h^{th} harmonic, and I_{s1} is the fundamental. Similarly, replacing the currents with voltages yield the voltage *THD*, $\%THD_v$ [18]. The power factor (PF) in the system depend on the THD_i. According to [18]:

$$PF = \frac{I_{s1}}{I_s} cos\phi_1 = \frac{cos\phi_1}{\sqrt{1 + {THD_i}^2}} \quad \textit{Eq. 38}$$

Where $cos\phi_1$is the same as the power factor in linear circuits, also called the displacement power factor (DPF) as it describes the displacement between the voltage and current.

As Eq. 38 illustrates, the power factor depend on the harmonics, and increasing harmonics reduces the PF and vice versa.

Harmonic sources in the presented system are the rectifiers and the inverter. The twelve pulse rectifiers draw current from the supply in pulses and creates harmonics of order $12k \pm 1$ at the source side [29]. The inverter synthesizes a sinusoidal output voltage with alternating DC pulses of different widths. There is therefore an inherent harmonic content in the output voltages and currents of the inverter. The transformers in the system may also cause harmonics if operated above rated power, voltage or frequency. This can cause the transformer to saturate and exhibit a nonlinear magnetizing current [29]. Transformer saturation is however not modelled in this work.

Using a delta connected transformer traps third harmonic currents, and these are not transferred to the wye (load) side [5]. This does however reduce the capacity of the transformer because of the circulating harmonic currents.

Based on IEC 61000-2-4, Det Norske Veritas (DNV) states "*the total voltage harmonic distortion shall not exceed 8 %. In addition no single order harmonic shall exceed 5 %.*" [30]. In addition, IEEE recommends that the total current harmonic distortion at nominal load should not exceed 5 % [31]. This will be used as the limits in this thesis.

3 System Modelling

All models are implemented in Matlab/Simulink with the SimPowerSystems toolbox.

3.1 External Power Supply Modelling

The external power supply is a 25 MW gas turbine connected to the jack-up rig via a subsea AC cable. It is assumed that the external supply has a robust power management system that manages to keep the supply line voltage constant regardless of the jack-up side load. The external power supply is therefore modelled as a 36 kV three-phase voltage source with a resistance and inductance. The resistance and inductance represent the subsea cable as explained in the next paragraph. The external generator has a sub-transient reactance, X_d'' = 18 %. As the gas turbine most likely operates at a lower voltage than 36 kV, this means that a transformer is needed on the supply side. The modelling of this is not studied in this thesis.

3.2 Subsea Cable Modelling

The supply-line voltage level is chosen to be 36 kV. With the nominal load, S = 16.6 [MVA], the nominal cable RMS line current is 266.2 A. Adding a 10 % safety margin, the cable should be able to carry 292.85 A. High voltage is chosen to limit currents, losses, and cable diameter. The cable parameters are based on a suitable cable from Nexans [32]. The datasheet is included in Appendix H. The RL parameters are summarized in Table 2:

Conductor AC resistance [Ω/km]	Inductance [mH/km]
0.26	0.4

Table 2 – Subsea cable data

As the distance between the supply unit and the jack-up rig is unknown, it is arbitrarily assumed 1 km, and hence the short line model described in 2.4 is used. The supply line frequency is 50 Hz.

3.3 Interconnection Topology

In this thesis, only one cable and one feeding point is considered in simulation models. The Simulink model of the interconnection and two load islands is depicted in Figure 12. The bus tie on the LVDC bus is open and therefore not included.

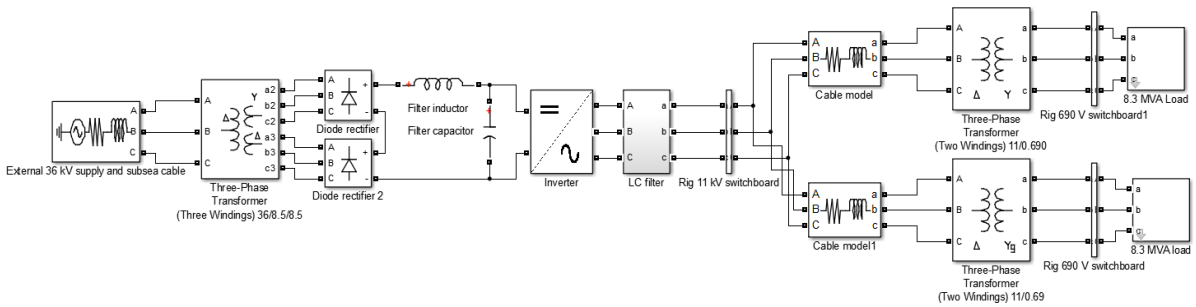


Figure 12 – Simulink model of interconnection topology and load model.

As Figure 12 illustrates, the sub-sea cable is connected to a three winding transformer that supplies a frequency changer. The frequency changer consist of a twelve-pulse rectifier, a DC link filter, a VSC, and an output filter. To study the effect of, and on, the low voltage loads, two

load islands with a two winding transformer and a load model is included. The modelling of all these components are described in the following.

3.4 Jack-up Rig Cables

As faults are studied in this work, approximate values of the HV side cable parameters are calculated. The load side LVAC cables are considered negligible because of the short distance, and because the fault are studied at the transformer terminals and above. The cable resistance are based on the "BATT cables, 11kV 3 core SWA PVC Cable BS6622" cable [33], and is set to R = 60 [μΩ/m] at 90^0 C. The length of the cables are assumed to be 30 m. The cable inductance is calculated in Appendix F, and is L = 0.327 [μH/m].

3.5 Three Winding Transformer Model

As this transformer would have to be custom made to the application, the transformer impedance values are unknown. Based on usual transformer impedance values, the values chosen that satisfy Eq. 1, Eq. 2 and Eq. 3 are summarized in Table 3.

Winding:	**Primary (Z1)**	**Secondary (Z2)**	**Tertiary (Z3)**	**Magnetizing**
Resistance [pu]:	0.005	0.001	0.001	300
Inductance [pu]:	0.035	0.035	0.035	200

Table 3 – Three winding transformer inductances and resistances.

The rated power of the transformer is 17 MVA, and the rated frequency is 50 Hz. The per unit values are based on the nominal power, frequency and winding voltage as in [34]. The primary/secondary/tertiary voltage ratios are: 36/8.5/8.5. These values are used in the pre-made "three winding transformer" model included in SimPowerSystems. Transformer saturation is not modelled.

3.6 Twelve Pulse Rectifier

Two full bridge diode rectifiers connected in series are used. The rectifiers are pre-made models in SimPowerSystems. Each rectifier are feed from the three winding transformer with a line-to-line RMS voltage of 8500 V to yield an approximate DC voltage of 23 kV (resistive losses and voltage drop due to current commutation excluded). As the average maximum currents through the diodes are about 660 A at nominal load, this is within commercially available diode ratings. The maximum steady state repetitive reverse blocking voltage over each diode is half the DC link voltage, i.e. 12.5 kV. As this is higher than commercially available diode ratings at the time of writing, multiple diodes in series are used. One of the highest rated diodes available at the time of writing is the "Infineon D 711N" rectifier diode with a maximum repetitive reverse voltage, $V_{RRM} = 6800\,V$, and an maximum average forward current, $I_{FAVM} = 790\,A$ [35], at 100° C. A part of the datasheet is included in Appendix H.

To accommodate the voltage, and as with the IGBTs in 2.7.5.2, include a 20 % safety margin, this means that at least three diodes are needed in series in each diode valve. In reality, the absolute maximum reverse voltage should be considered, but as limiting of inrush currents/soft start circuits not are studied in this thesis, the maximum voltages are unknown and 23 kV with at 20 % safety margin is assumed.

3.7 DC Link Filter Inductor Model

The maximum current ripple are set to 2 % of the nominal load current:

$$\Delta i_L = \frac{0.02 P_N}{V_{DC}} = \frac{0.02 * 15\ MW}{23\ kV} \approx 13\ A \qquad \textit{Eq. 39}$$

The filter inductance, with V_{LL} = 8500 V, using Eq. 4 and Eq. 39, becomes *L* = 13.63 mH. Actual simulations proved this to give a good accuracy, as depicted in Figure 13, where $\Delta i_L \approx 14\ A$.

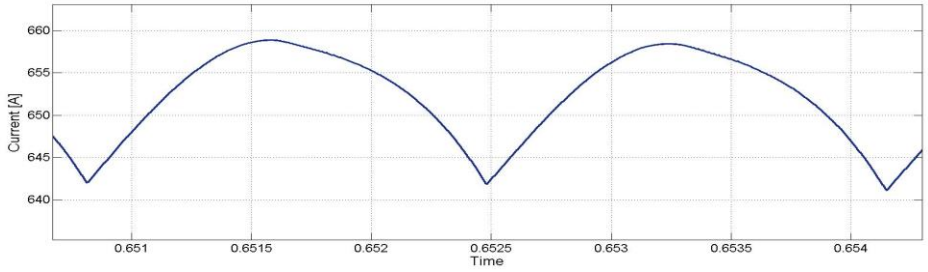


Figure 13 – 14 A current ripple on DC link

3.8 DC Link filter Capacitor Model

The allowed voltage ripple are set to $0.5\ \%$ of the average DC voltage, V_{do}, i.e. ΔV = 0.005*23000 V = 115 V.

Inserting the values in Eq. 5, with f_{sw} = 4860 Hz (from 2.7.5.5) yield a capacitance of *C* = 1.2 mF. Actual simulations yielded an acceptable ripple of 100 V as depicted in Figure 14.

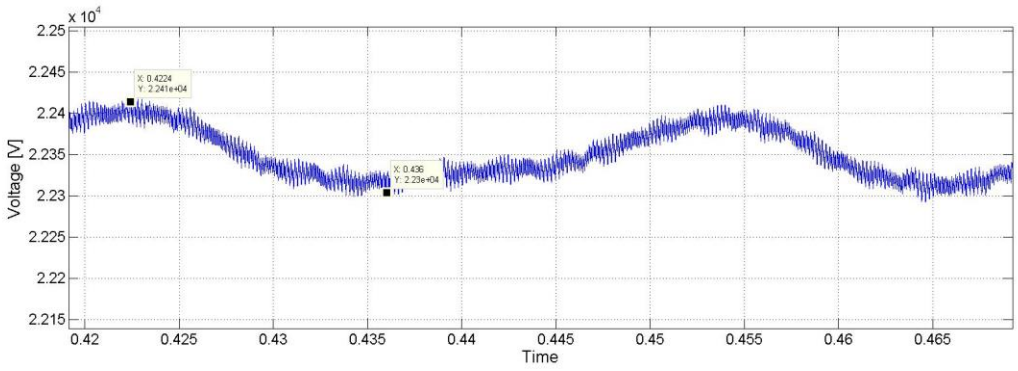


Figure 14 – DC link voltage ripple of about 100 V.

3.9 DC Link Voltage Level

Using Eq. 7, with $m_a = 1$ as a constraint, the required DC voltage is: V_{DC} ≥ 18 kV. The choice of voltage level depend on, among other things, desired system performance and cost. If the system connected has a large nominal load, and there are high transmission losses from the source supplying the DC link, the DC voltage will vary significantly with load. Changes in load and inrush currents may also cause transients in the DC voltage. Therefore, to ensure linear operation at all times, the no load DC voltage level should be higher than the minimum level so that it does not go below the minimum level during heavy load or transients. In this model, V_{DC} is chosen to be 23 kV to have good margin and allow linear operation even with

oscillations in the DC voltage. This means that m_a = 0.78 at nominal voltage with ideal components and no load.

3.10 Voltage Source Converter Model

In the frequency changer, a single two level voltage source inverter is supplying the entire load the control system presented in 2.7.5.6. Although multiple inverters may be considered for redundancy, implementing load sharing controllers and power management systems associated with multiple inverters in parallel are outside the scope of this thesis. The inverter uses IGBTs because of the higher current handling capability compared to metal oxide semiconductor field effect transistors (MOSFETS) [18]. The output fundamental frequency is, f_1 = 60 Hz. The modelling of the VSC components are described in the following.

3.10.1 IGBT Valves Simulink Model

One of the highest rated IGBTs commercially available at the time of writing is rated with a collector-emitter voltage, $V_{CES} = 1700\ V$ and nominal collector DC current, $I_{c,nom} = 2400\ A$ [36]. To accommodate the high voltage, several IGBTs are connected in series, together constituting an IGBT valve. The DC voltage is 23 kV, so using Eq. 6, the number of IGBTs in series needed are 23 kV / 0.8*1.7 kV = 16.9 ≈ 17. The Simulink model is illustrated in Figure 15:

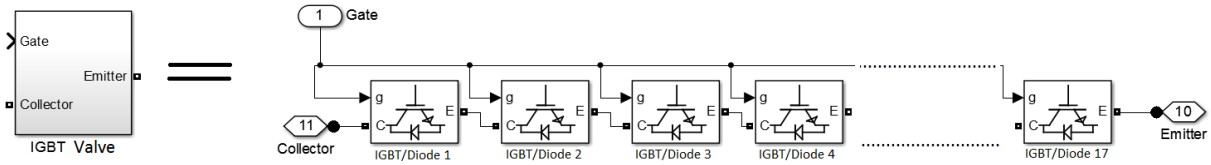


Figure 15 – Simulink model of IGBT valve consisting of seventeen IGBT/diodes. Not all IGBT/diode blocks are depicted.

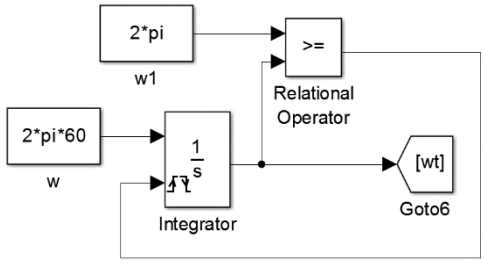
To reduce computational time, the forward voltage drop of the seventeen IGBTs are lumped into one equivalent switch. The IGBT switching characteristics are not the focus of this thesis, and as such, the premade Simulink IGBT/diode model is used. This model is linear, and only the forward voltage drop are of concern. It is assumed that all the IGBTs has equal characteristics, and that the switching is instantaneous. According to the datasheet included in Appendix H, the approximate forward voltage drop of each IGBT at a junction temperature of 25° C, and nominal collector current, is V_f = 1.8 V. The total equivalent resistance then becomes 17 mΩ.

3.10.2 Switching Frequency

The choice of switching frequency is based on the theory 2.7.5.5. As the choice of switching frequency depend on cost, among other things, and the calculation of the optimal frequency with respect to cost are not considered. A relatively high switching frequency is therefore chosen yielding good control and system performance. Satisfying the criteria presented in 2.7.5.5, m_f = 81 is chosen. Inserting this into Eq. 8, with f_1 = 60 Hz yields f_s = 4860 Hz.

3.10.3 Frequency Generator Simulink Model

To maintain the output grid frequency of 60 Hz, a frequency generator is used. In reality, this might be a crystal oscillator [19], but in this, it is modelled as depicted in Figure 16.



The frequency [rad/s] is a constant block, w. Integrating this with respect to time yield the angle [rad]. In addition, the integral is reset every 2π to limit the output from increasing indefinitely.

Figure 16 – Simulink model of frequency generator

3.10.4 Inverter Output LC filter

To limit the size of the inductor, $\Delta i_L = 100$ A is used as a basis for design. Using Eq. 36, assuming δ = 0.8, with V_{DC} = 23 kV, f_s = 4860 yield L = 6.3 mH.

After the inductance value is determined, the capacitance is determined using Eq. 35 [37]. The corner frequency is here chosen as ω_o= 400π to avoid interference with the fundamental and provide good attenuation of the frequency, yielding C = 100.36 [µF]. The frequency response of the voltage transfer function (Eq. 33) with these values is depicted in Figure 17:

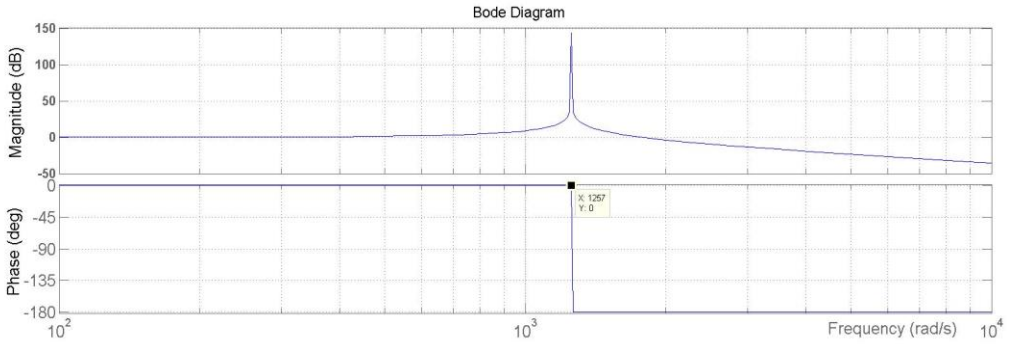


Figure 17 – Bode plot of output AC filter voltage-frequency response.

As the Bode polt illustrates, the corner frequency is at 400π = 1257 [rad/s], and the amplitude asymptote drops with 40 dB/decade after the corner frequency.

3.11 Two Winding Transformer

Similar values to the values used in the three winding transformer in section 3.5 are used. The values are summarized in Table 4:

Winding:	**Primary**	**Secondary**	**Magnetizing**
Resistance [pu]:	0.005	0.005	300
Inductance [pu]:	0.0035	0.0035	200

Table 4 – Two winding transformer per unit parameters

The “D1” connection type in Simulink is used, providing a thirty-degree phase shift.

3.12 Load

Based on experience, one way of modelling a drilling load is to consider the entire load as an RC load. The load model used is a static load model included in SimPowerSystems. To test the interconnections ability to accommodate brute load changes, step changes in load are modelled by using multiple static loads connected in parallel through switches. One such load model is depicted in Figure 18. A limitation of the pre-made static load model in Simulink is that it depend on the voltage level. Therefore, if the load voltage differs from the nominal voltage defined in the load model, the load will differ.

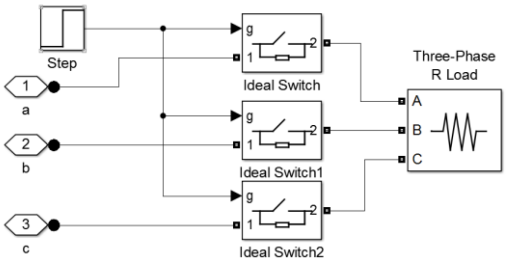


Figure 18 – Simulink static load model

As most drilling loads are motors that gradually increases or decreases the power demand, a dynamic load model included in Simulink is used to model this behaviour. The load is made of controlled current sources, which is controlled by applying a repeating signal of desired slope and magnitude. Because the dynamic load is made of current sources, it cannot be connected in series with an inductor. A parallel 1 MW resistive load is therefore used to overcome this issue. The model is depicted in Figure 19.

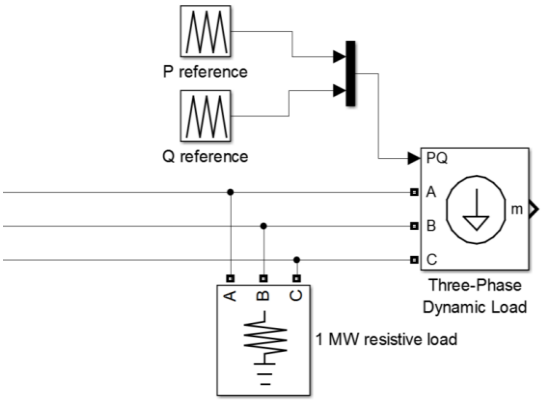


Figure 19 – Three phase dynamic Simulink load model

3.13 Fault Modelling

In this work, only a symmetrical three-phase short circuit fault is modelled on the AC side. In addition a bolted short circuit on the DC link is modelled. Based on experience, the fault resistance is set to 10 μΩ. This to create some energy dissipation. The three phase short circuit model created in Simulink is depicted in Figure 20. Similarly, the DC link fault is made by a switch short circuiting the DC link poles. Different fault locations are tested, and the bus tie switches are considered open prior to the faults. The fault locations studied are presented in Figure 21 and Figure 22, designated *F1, F2, F3, F4 and F5.*

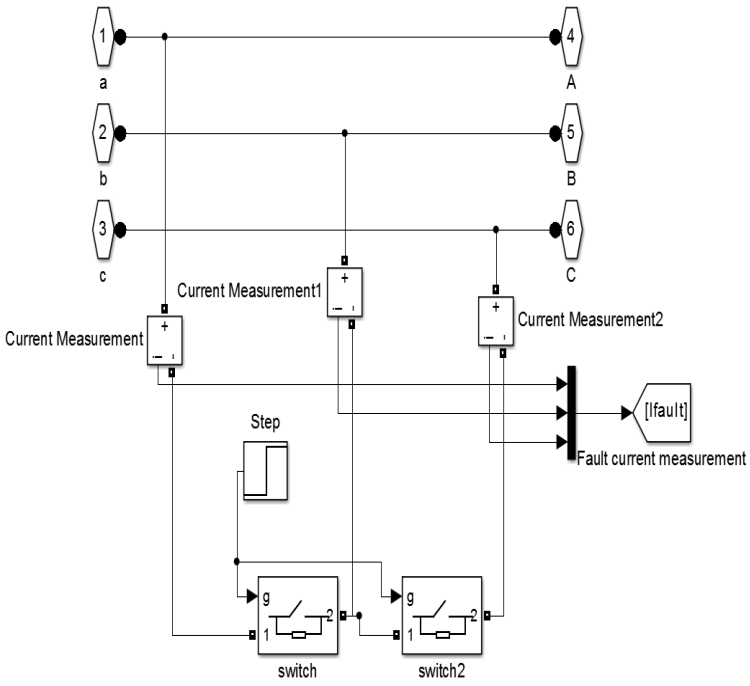


Figure 20 – Three-phase short circuit Simulink model.

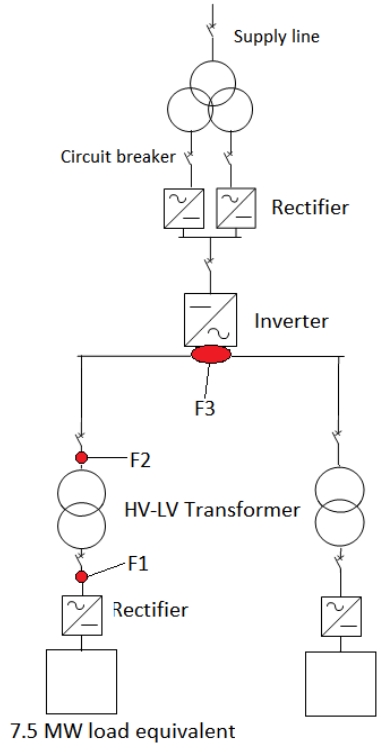


Figure 21 – Fault circuit with fault locations F1, F2 an F3 marked in red.

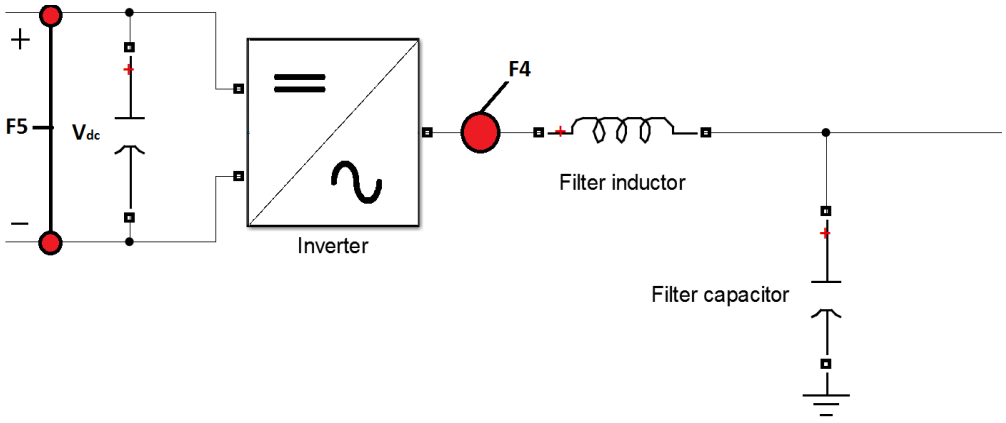


Figure 22 – Fault location F4 between inverter and inverter output filter and fault location F5 marked in red.

The faults are placed at different locations to study the impact that fault has on the supply, and to confirm that selectivity is maintained where protection is available. The simplified system has two equivalent loads, each representing a load island. As all drilling loads are connected through rectifiers, it is assumed that the rectifiers block all fault currents from the load and DC bus, and hence that all fault current is supplied from the interconnection and supply line. Therefore, when faults are simulated, the loads is purely resistive to eliminate the effect of load reactance.

3.14 Fault Current Protection Relay Model

To observe system behaviour during and after a fault with a protection relay tripping, a simplified relay is made. The relay model is only measuring current. The Simulink model of the relay is presented in Figure 23.

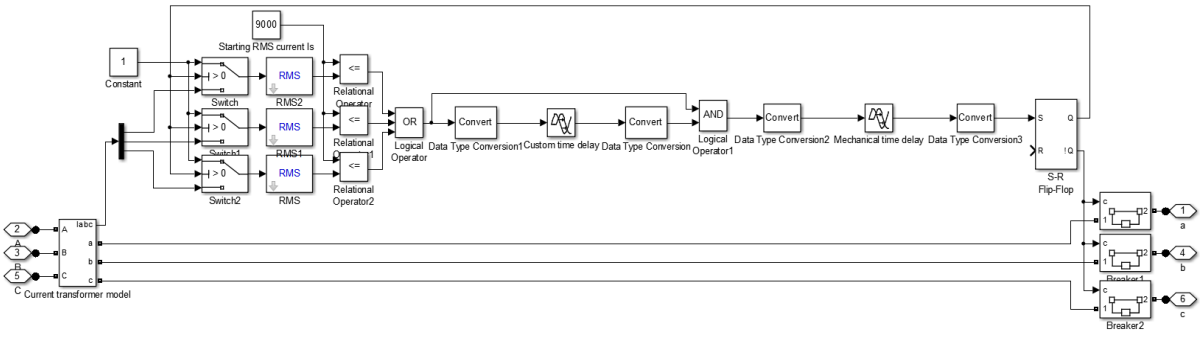


Figure 23 – Overcurrent protection relay Simulink model.

The phase currents are measured using a measurement block. In reality, this would be through a current transformer to limit currents in the electronic measurement system. The true RMS currents of each phase is then calculated in the "RMS" blocks. These values are then compared to the predefined relay starting RMS current. As described in [27], the predefined starting current is set to $2.4I_N$, where I_N [A] is the nominal load RMS current in the protected branch. If the measured currents exceed this value, a trip signal is sent through a time delay block. This time delay represents the user defined time delay. After the delay, the tripping signal is sent to the logical "AND" operator that checks if the fault still is present from the feed forward. If this is true, the tripping signal is sent to another time delay block representing the mechanical movement time of the circuit breaker. This is assumed 10 ms. After this, the tripping signal sets the "S-R Flip-Flip" block, and a signal is sent to the circuit breakers to open. The circuit breakers then opens instantaneously at the next current zero crossing in the respective phases. When the circuit breaker opens the RMS current becomes zero. As this halts simulation, switches that sets the RMS currents to one at the instant of tripping are used. Resetting of the relay is not modelled, as this would have the same effect on the system as a step in load, which is modelled in the load chapter (3.12).

3.15 Coordination of Protection

The overcurrent protection relays are installed at either sides of the load transformers and at the supply line. The inverter protection system and DC breaker is not modelled. The nominal branch current, tripping level and custom delay time of the circuit breakers is summarized in Table 5.

Location	Tripping RMS current [A]	Delay time [ms]
F1	9000	0
F2	1000	60
F5	2000	0

Table 5 – Relay tripping levels and delay times.

The relay at F2 has a delay. This is to ensure that during a fault at F1, the breaker at F1 trips first so that selectivity is maintained. Note that the supply line relay at F5 is set without any custom delay time. This is because the inverter limits the current to load side fault, and these faults will not cause the supply line relay to trip as long as the inverter is operational. Selectivity is therefore maintained. The F5 relay starting current is set to 2000 A, which is way more than $2.4I_N$. This is because of the large inrush currents at system start-up. If a lower tripping level is desired, an inrush current limitation solution is needed.

4 Results from Simulations in Matlab/Simulink

All models used are included in Appendix A, all model parameters are included in Appendix B. The power measurement block can be inaccurate for unbalanced or distorted sine signals. This causes ripple in the measured power. Power measurement may therefore have some inaccuracy. All RMS values are calculated using true RMS with a fundamental frequency of 60 Hz. Where applicable, the results are analysed on a per phase basis. Differences from phase to phase are brought up when relevant.

4.1 VSC Control System Verification

The inverter line-to-line voltage reference is changed from 11 kV to 7 kV after 0.3 s. The inverter frequency reference is changed from 60 Hz to 40 Hz after 0.4 s. The resulting line-to-line output voltage is depicted in Figure 24.

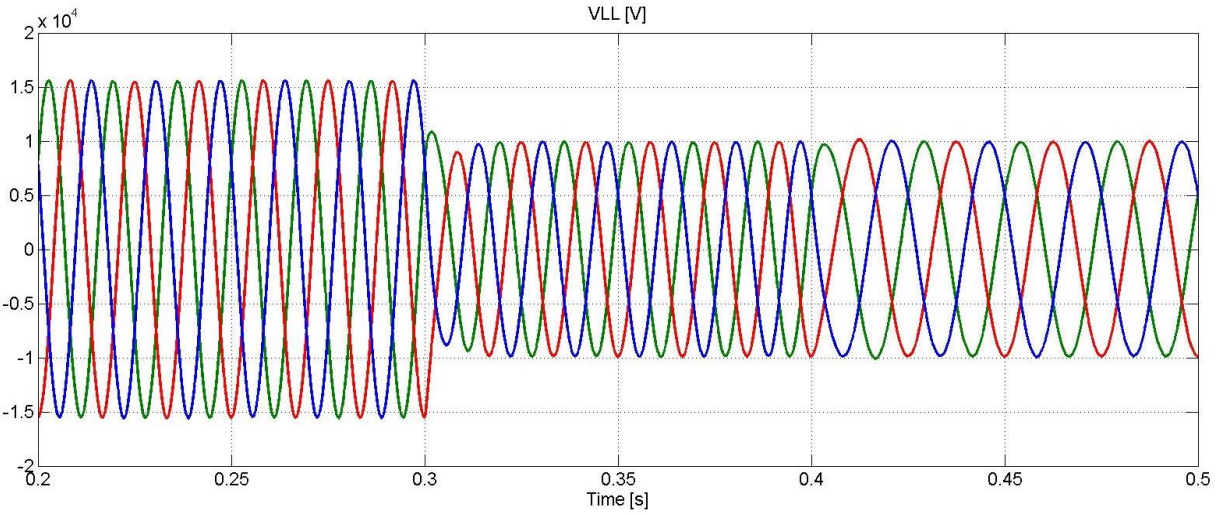


Figure 24 – Inverter control system test. Reference voltage changed from 11 kV to 7 kV at t=0.3 s. Reference frequency changed from 60 Hz to 40 Hz at t = 0.4 s.

The output voltage follows the voltage reference after 16 ms during which there is a 650 V dip in voltage. The frequency changes from 60 Hz to 40 Hz instantaneously.

4.2 Steady State System Verification

The system is run with nominal load, i.e. P = 15 MW, and Q = 7.2 MVAr (capacitive), connected. All harmonic content of the signals are analysed using the "fast Fourier transform" analysis in Simulink, and all harmonic magnitudes are relative to the magnitude of the fundamental component, and are designated *h.*

4.2.1 DC Link Voltage

The DC link voltage is presented in Figure 25.

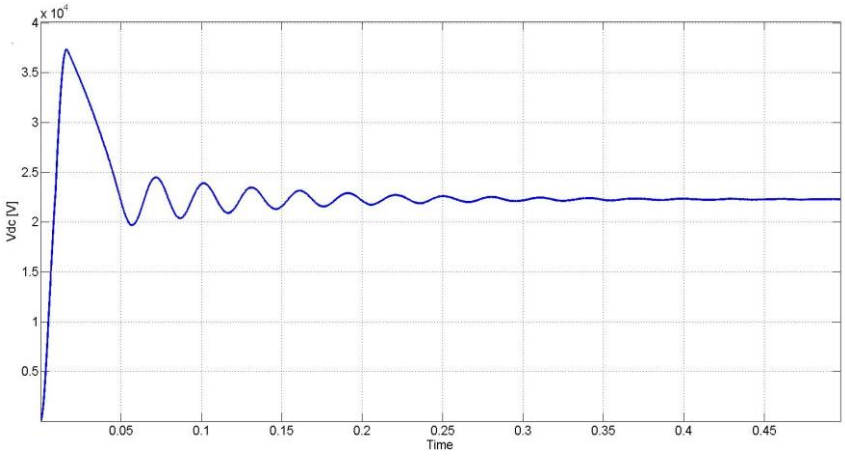


Figure 25 – DC voltage start up and steady state

At start-up, after the initial inrush currents, there are voltage oscillations with a peak of 37 kV, and a frequency of 30 Hz. The DC voltage reaches steady state after 0.45 s. The steady state voltage is 22.235 kV.

4.2.2 HV Switchboard Voltage

The high voltage switchboard line-to-line voltages are analysed. The resulting harmonic spectrum is depicted in Figure 26 along with the signal analysed.

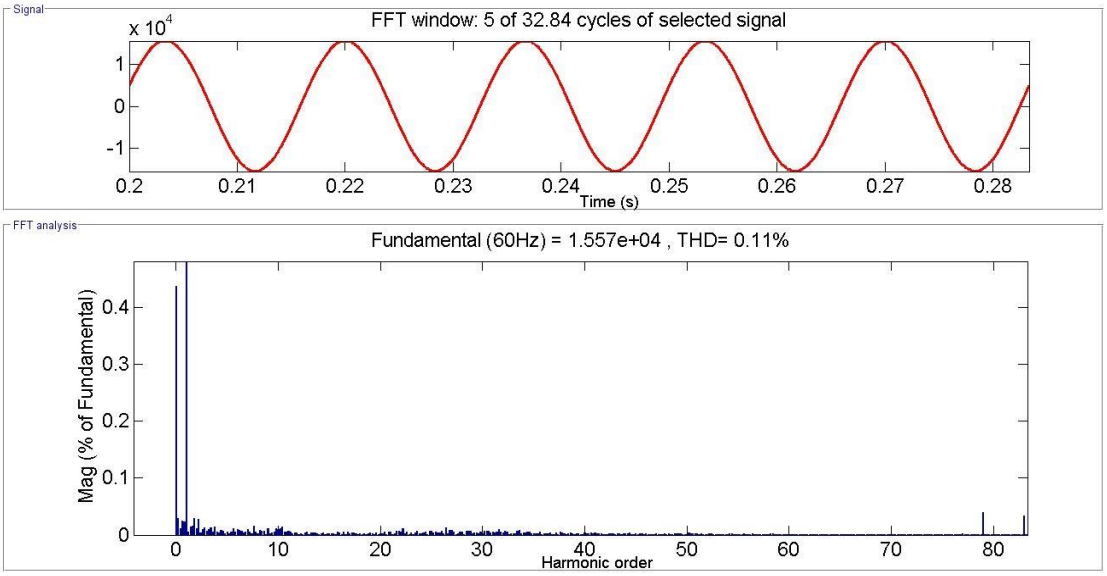


Figure 26 – Harmonic analysis of inverter output voltage.

The output voltage peak amplitude is 15570 V, i.e. 11.009 kV RMS. The total harmonic distortion (THD) is 0.11 %, and the largest harmonic orders around the fundamental frequency of 60 Hz, are h3, h5 and h7, each having a magnitude of 0.01 % of the fundamental. The switching frequency harmonic order is 81, i.e. 4860 Hz. There are two major odd harmonic sidebands around the switching frequency, h79 = 0.04 % and h83 = 0.03 %. The DC component is 0.44 %.

4.2.3 HV Switchboard Current

The filtered line currents in the HV switchboard is analysed. The output waveform and harmonic spectre is depicted in Figure 27.

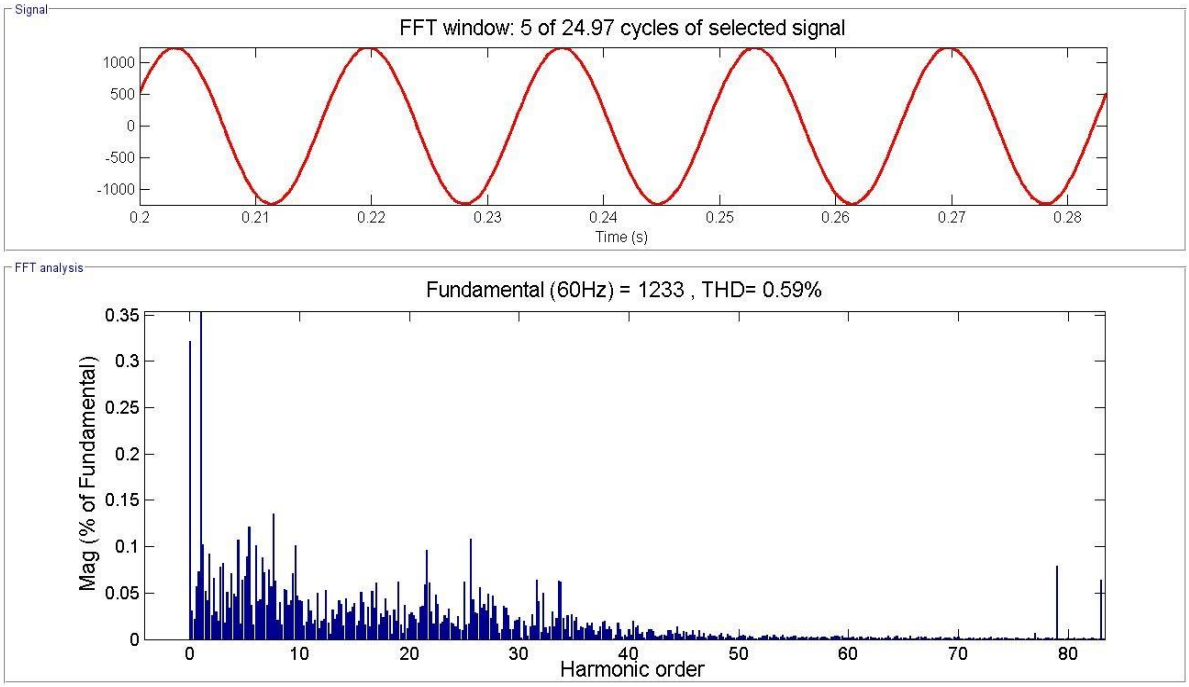


Figure 27 – Line current waveform and harmonic analysis of the inverter filtered output currents.

The current has a RMS value of 871.9 A. The dominant harmonic orders around the fundamental frequency is: h3 = 0.03 %; h9 = 0.06 %; h10 = 0.07; h11 = 0.04 % and h22 = 0.04%. In addition, there are two relatively major harmonic orders around the switching frequency, h79 = 0.07 % and h83 = 0.06 %. The harmonic spectre in the two other phases are of similar characteristics. The DC component is -3.972 A, and the DC components of the two other phases are 10.35 A, and -6.375 A. The sum of the DC currents are therefore zero.

4.2.4 Load Voltage

The load side voltages of the two winding transformer are analysed. The output waveform and harmonic spectre is depicted in Figure 28.

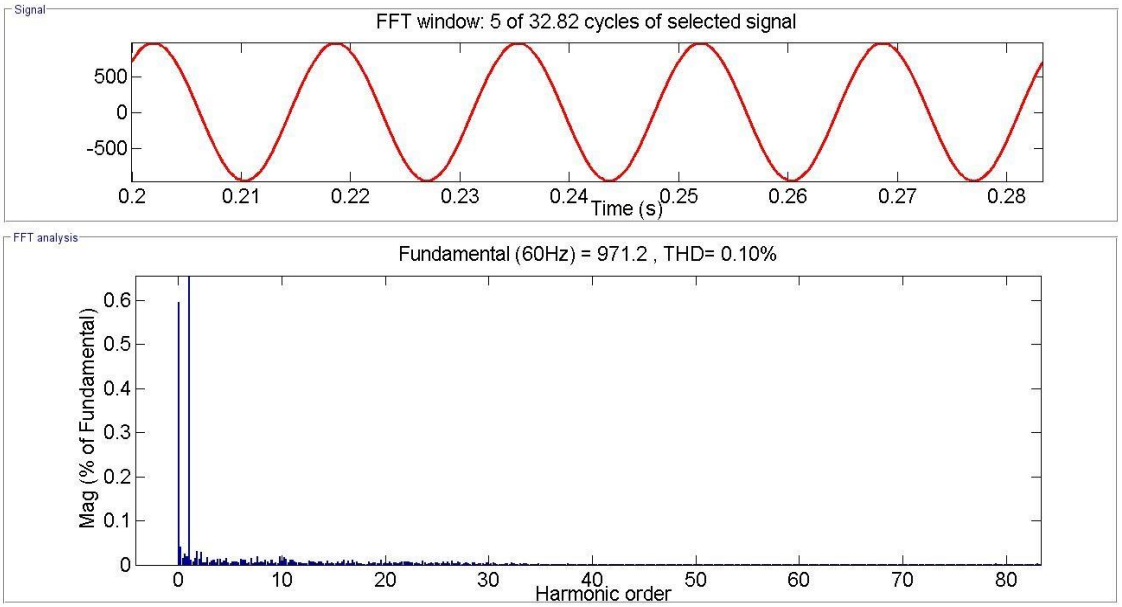


Figure 28 - Load side two winding transformer line-to-line voltage waveform and harmonic spectre.

The line-to-line voltages has an RMS value of 686.7 V. The THD is 0.1 %. The only harmonic orders slightly present are h2 = 0.01 %, and h4 = 0.01 %. The two other phases has similar characteristics.

4.2.5 Load Currents

The two winding transformer output line currents are analysed. The output waveform and harmonic spectre is depicted in Figure 29.

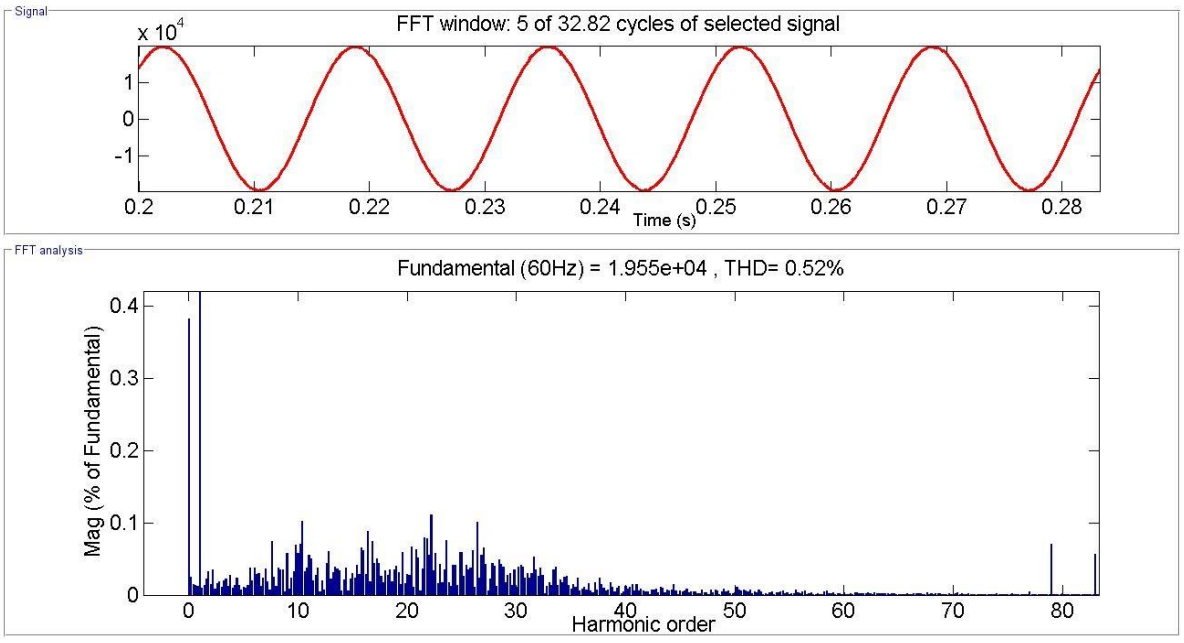


Figure 29 - Load side two winding transformer line current waveform and harmonic spectre.

The RMS magnitude of the current is 13.824 kA. The THD is 0.52 %. The DC component is 0.38 %. The dominant harmonic orders around the fundamental frequency are: h10 = 0.06 %; h11 = 0.06 %; h25 = 0.06 %; h26 = 0.06 %; h27 = 0.07 %. The dominant high order harmonics around the modulation frequency, $m_f = 81$, are: h79 = 0.07 % and h83 = 0.06 %. The two other phases has similar characteristics.

4.2.6 Subsea Cable Voltages

The sub-sea cable line-to-line voltages are analysed. The resulting waveform and harmonic spectrum is depicted in Figure 30.

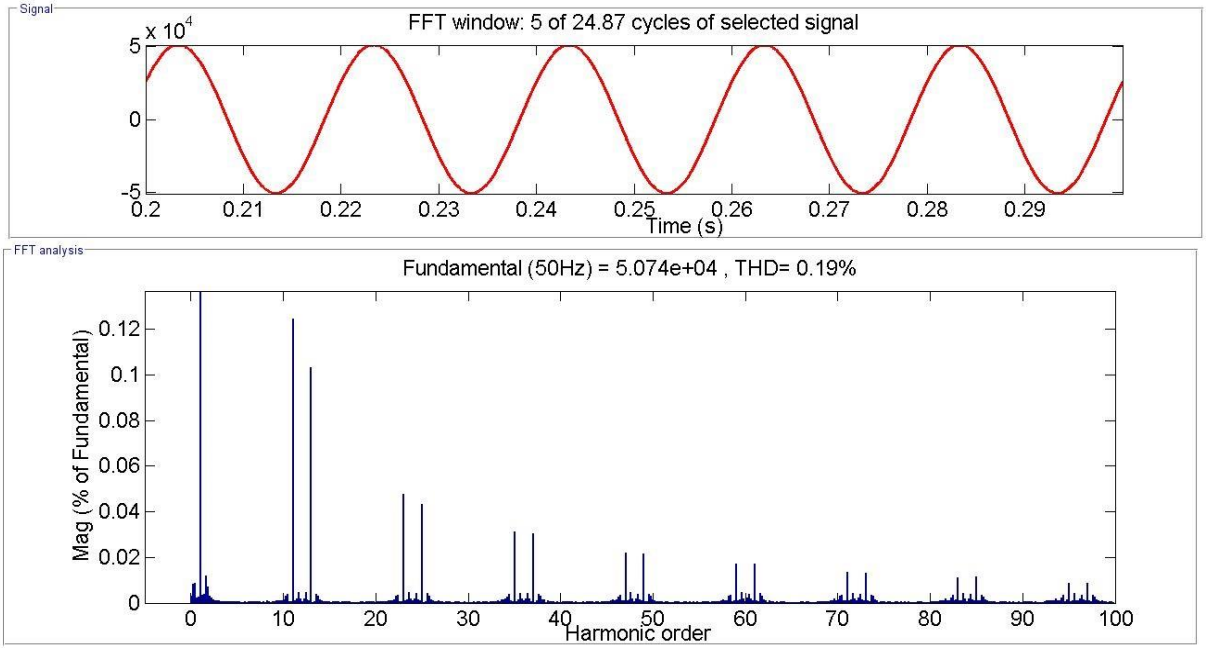


Figure 30 – Waveform and harmonic analysis of subsea cable line-to-line voltages.

The output voltage peak amplitude is 50740 V, i.e. 35.878 kV RMS. The THD is 0.16 %.The dominant harmonics are h11 = 0.097% and h13 = 0.08 %. The two other phases has similar characteristics.

4.2.7 Subsea Cable Currents

The sub-sea cable line currents are analysed. The resulting waveform and harmonic spectrum is depicted in Figure 31.

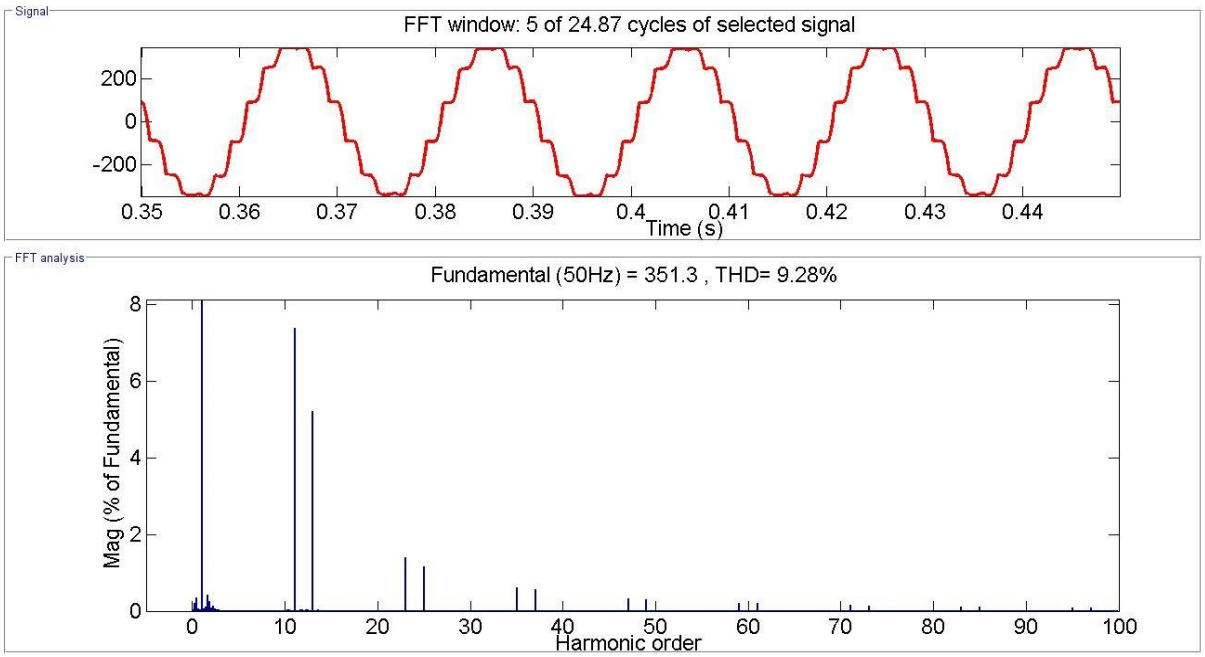


Figure 31 – Subsea line current waveform and harmonic spectrum.

The magnitude of the RMS line current is approximately 248 A. The THD is 9.28 %. The DC component is 0.16 %. The dominant harmonic orders are: h11 = 7.4 %; h13 = 5.21 %; h23 = 1.4 %; h25 = 1.17 %. The two other phases has similar characteristics.

4.3 Load Scenarios

4.3.1 Step Changes in Load

Step changes is load is simulated to test system stability and performance. The different loads at the various time intervals are summarized in Table 6. The load is increased from interval 1 to 2, and 2 to 3. This to study system performance at different load levels and system response to brute increases in load. Interval 3 corresponds to nominal system load. The load in interval 4 is 20 MVA, which is above rated power of the system, and is included to study system behaviour during overload. Interval 5 is included to study system performance to a decrease in load.

Interval #	Time interval [s]	Active power [MW]	Reactive power [MVAr]
1	0-0.2	5	-2.5
2	0.2-0.4	10	-5
3	0.4-0.6	15	-7.5
4	0.6-0.8	20	-10
5	0.8-0.9	10	-5

Table 6 – Load profiles and time intervals

The simulation results are presented in Figure 32.

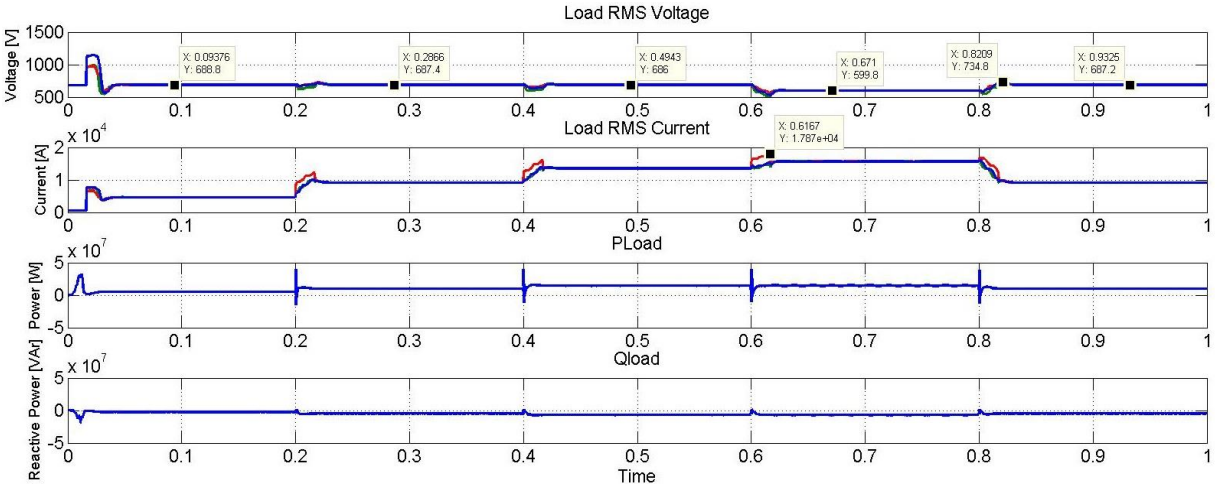


Figure 32 – Step changes in load

The steady state results are summarized in Table 7:

Interval #	Time [s]	$V_{RMS,load}$ $[V]$	$I_{RMS,load}$ $[A]$	P_{load} $[MW]$	Q_{load} $[MVAr]$
1	0-0.2	688.8	4619	4.957	-2.505
2	0.2-0.4	687.4	9125	9.709	-4.805
3	0.4-0.6	686	13510	14.4	-6.894
4	0.6-0.8	599.8	15600	14.99	-7.246
5	0.8-0.9	687.2	9125	9.584	-4.689

Table 7 – Simulation results during step-changes in load.

In addition, there are some current transients at the transitions, the largest being from interval two to three with a maximum RMS current of 16030 A, and from three to four with a maximum RMS current of 17870 A.

4.3.2 Ramp Load

A linear increase and decrease in load in one load island is simulated. The load extreme values is as summarized in Table 8 with linear transition between the extreme values.

Time [s]	Island load power [MW]	Island load reactive power[MVAr]
0	3	3
0.5	6	5
1	3	3

Table 8 – Load pattern during ramp loads

The resulting RMS voltage, RMS current, and power in the island is presented in Figure 33.

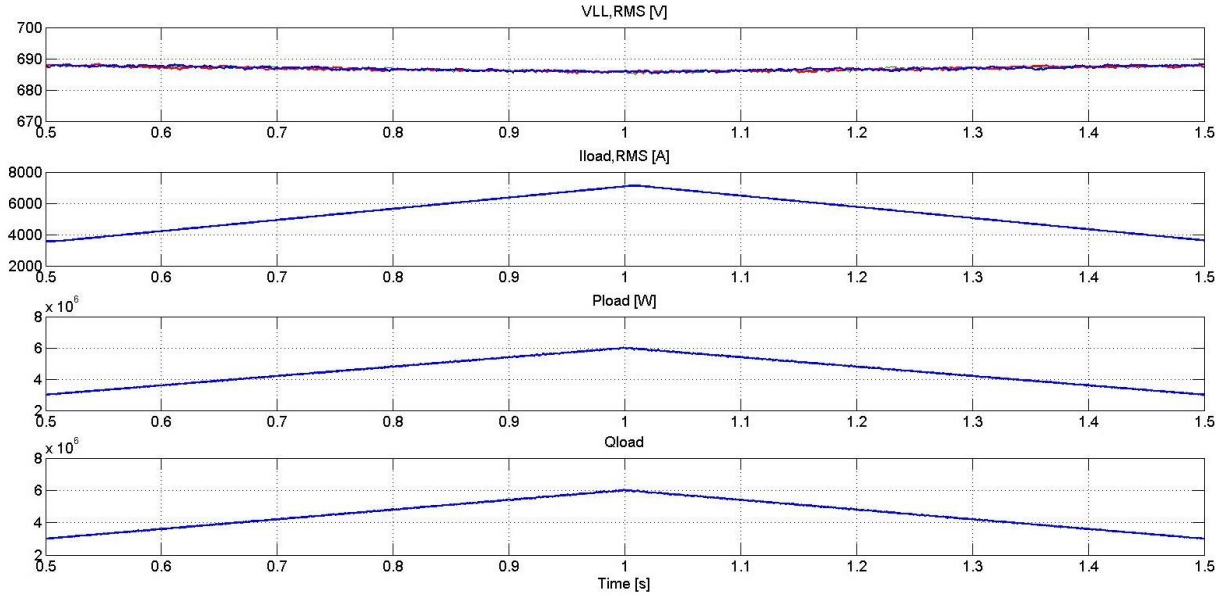


Figure 33 – RMS voltage, RMS current, active and reactive power, during dynamic ramp load.

The results are summarized in Table 9

Time [s]	RMS Voltage [V]	RMS current [A]	Active power [MW]	Reactive power [MVAr]
0.1	687.9	3558	3.003	3
0.5	686	7105	6.005	6
1	687.9	3632	3	3

Table 9 - RMS voltage, RMS current, active and reactive power, at extreme values during dynamic ramp load.

4.3.3 Sudden Loss of Load

A sudden loss of nominal load at t = 0.2 s is simulated. The results are presented in Figure 34.

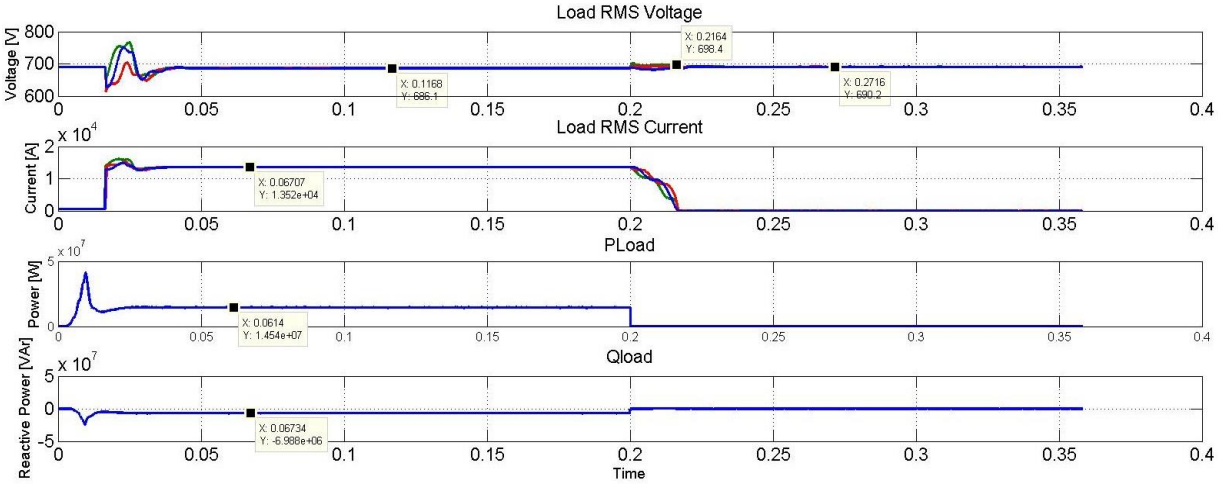


Figure 34 – Voltage, Current and Power graphs during sudden loss of nominal load

The load power before the load is disconnected is: P = 15 MW, Q = -7 MVAr. The steady state RMS voltage before disconnection is 686.1 V, the steady state RMS voltage after

disconnection is 690.2 V. During the disconnection, a transient peak RMS voltage of 698.4 V occurs.

4.4 Short Circuit Fault Simulations

Three pole short circuits are simulated at the places described in 3.13, designated, *F1, F2, F3 and F4.* In addition, a bolted short circuit on the frequency changer DC link, designated F5, is simulated. Both behaviour at the fault location and the propagation to the interconnection is studied and presented with graphs. In addition, if the fault causes overcurrent in the supply line, this is included.

The time intervals can differ from different figures. This is because the time intervals represented is chosen to give the best possible view, and to include some stationary behaviour before and after the fault event. In the graphs depicting IGBT/Diode measurements, both IGBT and diode are considered as a switch, and it is the switch current and voltage that is depicted. The positive current direction is from collector to emitter. Only one switch in the worst-case inverter leg is illustrated. The other switch in that converter leg will then have equal, but opposite, voltages and currents.

As the size of the fault current depend on both the time of the fault and inverter behaviour, the theoretically maximum fault current may be even larger than the simulation results. During all simulations, protection relays are installed at F1, F2 and F5 unless otherwise is specified. The times associated with the steady state values are the times in which the system attains steady state for the first time after the fault.

4.4.1 Fault on Location F1

A three-pole short circuit on the low voltage side of one of the two load islands is simulated. Because of the short fault clearing time, the fault never reaches steady state. The fault is therefore also simulated without protection installed for comparison. The fault occurs at t = 0.4 s. The load on each island is 7.5 MW, and the system is in steady state prior to the fault.

4.4.1.1 Without Overcurrent Protection Relay

The voltage, current and power at the fault location is presented in Figure 35.

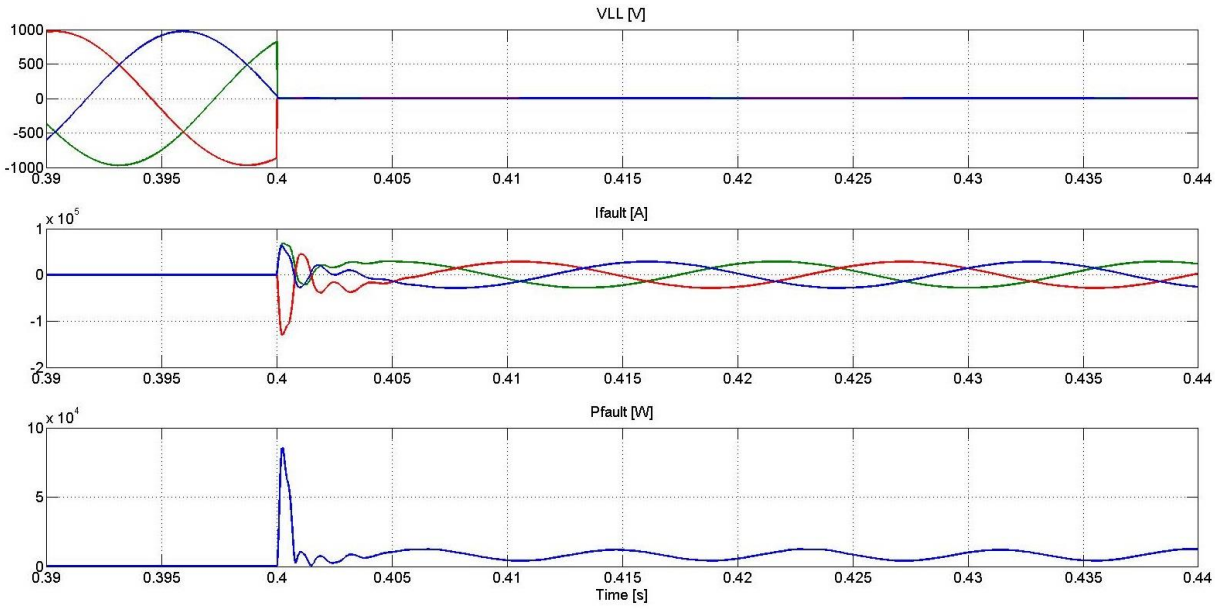


Figure 35 – Voltage, current and power at the fault location F1 during a three-pole short circuit.

The resulting values are summarized in Table 10

Quantity	Time [s]	Magnitude
$\hat{V}_{fault,ss}$	0.4	0.16 [V]
$\hat{I}_{fault}$	0.4002	130.9 [kA]
$\hat{I}_{fault,ss}$	0.405	28.21 [kA]
$\hat{P}_{fault}$	0.4002	85.85 [kW]
$\hat{P}_{fault,ss}$	0.405	12.2 [kW]

Table 10 – Peak parameters measured at fault location during fault at F1

Where:

- $\hat{V}_{fault,ss}$ is the peak steady state line-to-line fault voltage at the fault location [V]
- $\hat{I}_{fault}$ is the peak fault current at the fault location [A]
- $\hat{I}_{fault,ss}$ is the steady state fault current at the fault location [A]
- $\hat{P}_{fault}$ is the maximum fault power at the fault location [kW]
- $\hat{P}_{fault,ss}$ is the peak steady state fault power at the fault location [kW]

The inverter terminal voltage and current along with the switch IGBT/Diode voltage and current is presented in Figure 36.

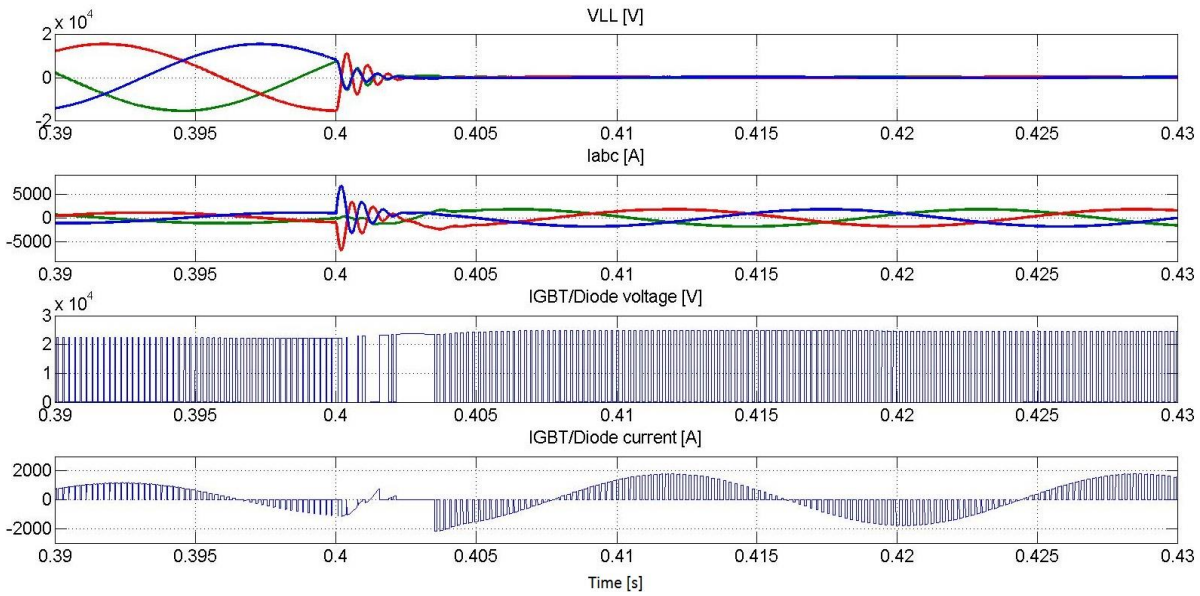


Figure 36 – Inverter terminal voltage and current, and switch voltage and current during fault.

The resulting values are summarized in Table 11.

Quantity	Time [s]	Magnitude
$\hat{V}_{LL,ss}$	0.405	294 [V]
$\hat{I}_{abc}$	0.4002	6.732 [kA]
$\hat{I}_{abc,ss}$	0.405	1.8 [kA]
$\hat{V}_{IGBT/Diode}$	0.407	24.9 [kV]
$\hat{I}_{IGBT/Diode}$	0.404	2 [kA]

Table 11 – Inverter output voltage and current, and switch voltage and current during a fault at F1.

Where:

- $\hat{V}_{LL,ss}$ is the peak line-to-line voltage at the HV switchboard [V]
- $\hat{I}_{abc}$ is the line currents at the HV switchboard [A]
- $\hat{I}_{abc,ss}$ is the peak steady state voltage at the HV switchboard [A]
- $\hat{V}_{IGBT/Diode}$ is the peak line-to-line voltage over the inverter switches [V]
- $\hat{I}_{IGBT/Diode}$ is the peak current through the inverter switches [A]

Finally, the DC voltage fault response is depicted in Figure 37.

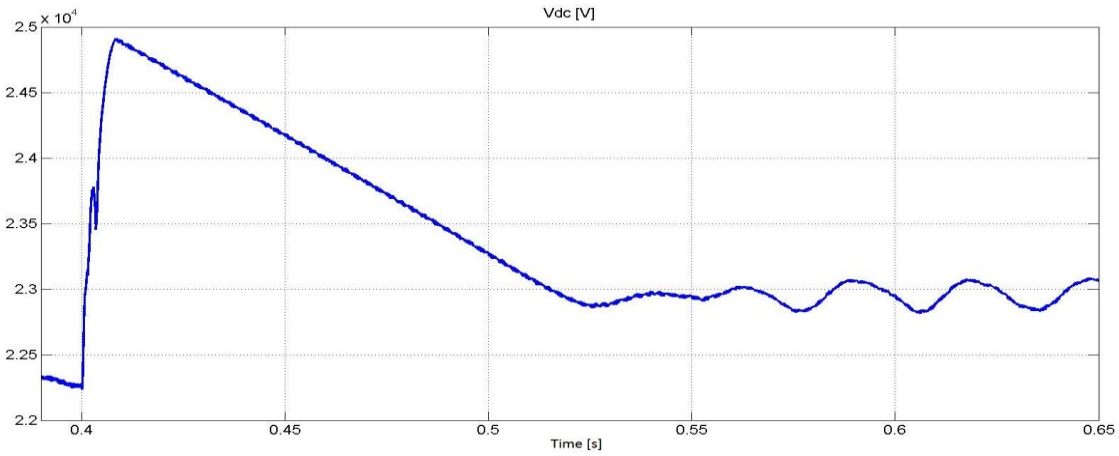


Figure 37 – DC voltage during AC side fault at F1.

The DC voltage peaks at 24.9 kV, and reaches steady state fault level at about 23 kV at t = 0.53 s.

4.4.1.2 With Overcurrent Protection Relay

The same fault is simulated with overcurrent protection relays installed. The fault still occurs at t = 0.4 s. As the initial fault behaviour already has been presented, only the behaviour during relay tripping is presented in the following. The resulting voltage, current and power at the fault location is presented in Figure 38.

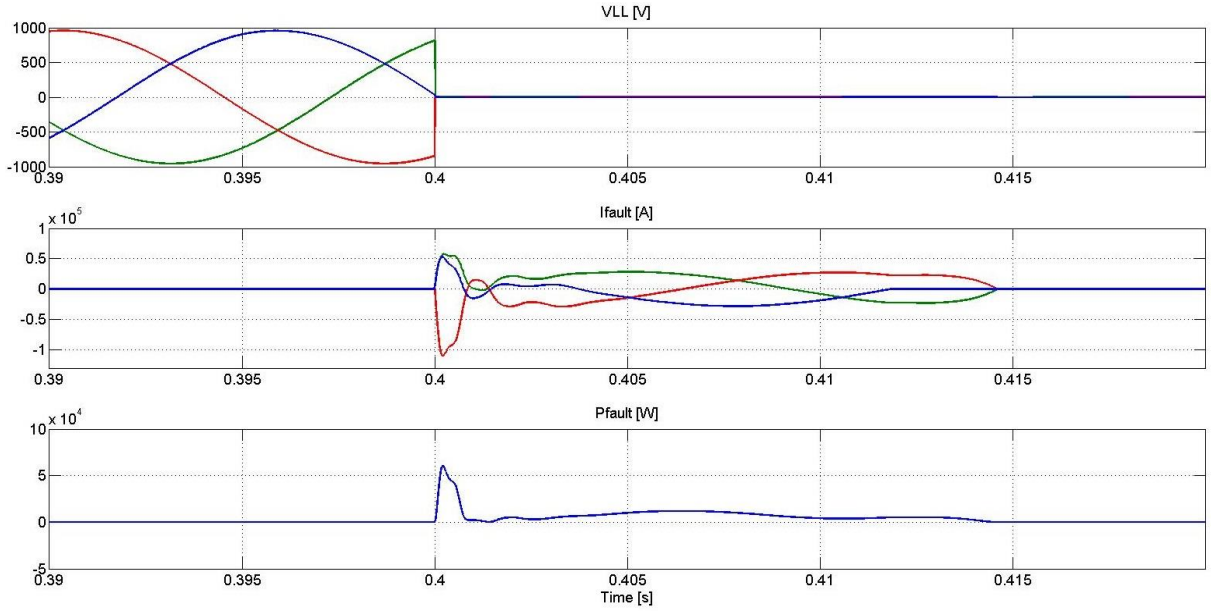


Figure 38 - Voltage, current and power at the fault location F1 during a three-pole short circuit with overcurrent protection relay installed.

After the fault detection time and the 10 ms mechanical time delay, the trip signal is sent to the circuit breaker to open. The first phase reaches zero a t = 0.4117 s. The second, and hence the third current becomes zero at t = 0.4145 s. At this time the fault voltage and power becomes zero.

The inverter terminal voltage and current along with the switch IGBT/Diode voltage and current is presented in Figure 39.

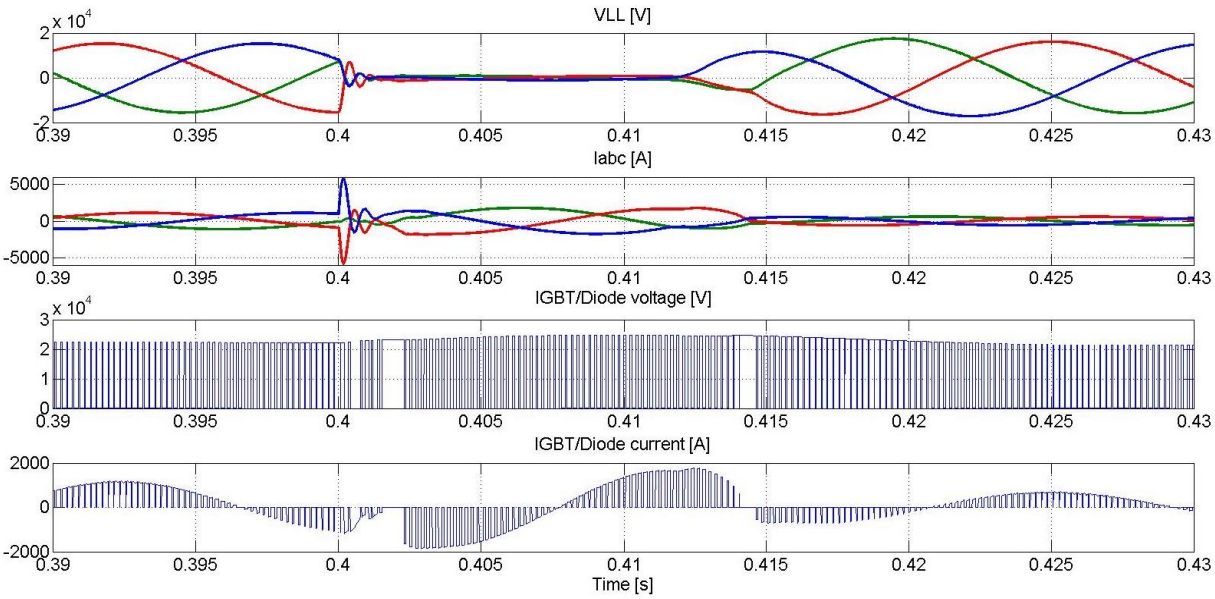


Figure 39 - Inverter terminal voltage and current, and IGBT/Diode voltage and current during fault with overcurrent relay tripping after 30 ms.

When the fault currents are cleared the-line-to line voltages resumes normal steady state conditions after about 7 ms, at t = 0.417 s. The total time from the fault occurs until normal voltage conditions are restored is then 17 ms. When the circuit breaker opens, the current through the switch changes direction from the IGBT to the diode.

The DC voltage during the fault is depicted in Figure 40.

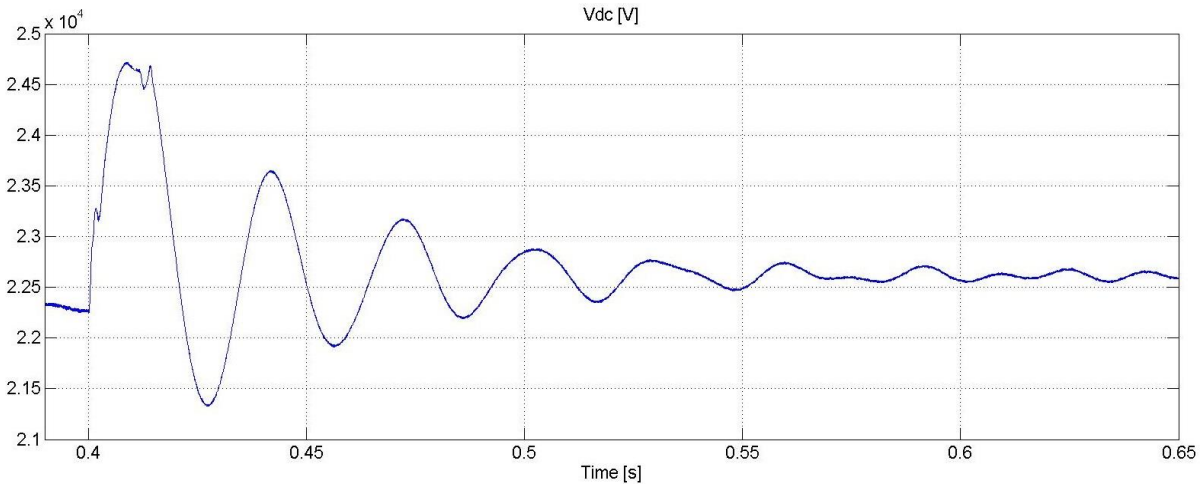


Figure 40 – DC voltage during fault at F1 with overcurrent relay tripping after 30 ms.

When the circuit breaker opens, the DC voltage declines rapidly, before oscillating. The DC voltage stabilizes at about t = 0.63 s.

4.4.2 Fault on Location F2

A three-pole short circuit at F2 is simulated. As the fault reaches steady state before the protection relay trips, simulations are done with protection relays installed. In addition, the

DC voltage is depicted for the same fault without protection relay installed. The voltage, current and power at the fault location is presented in Figure 41:

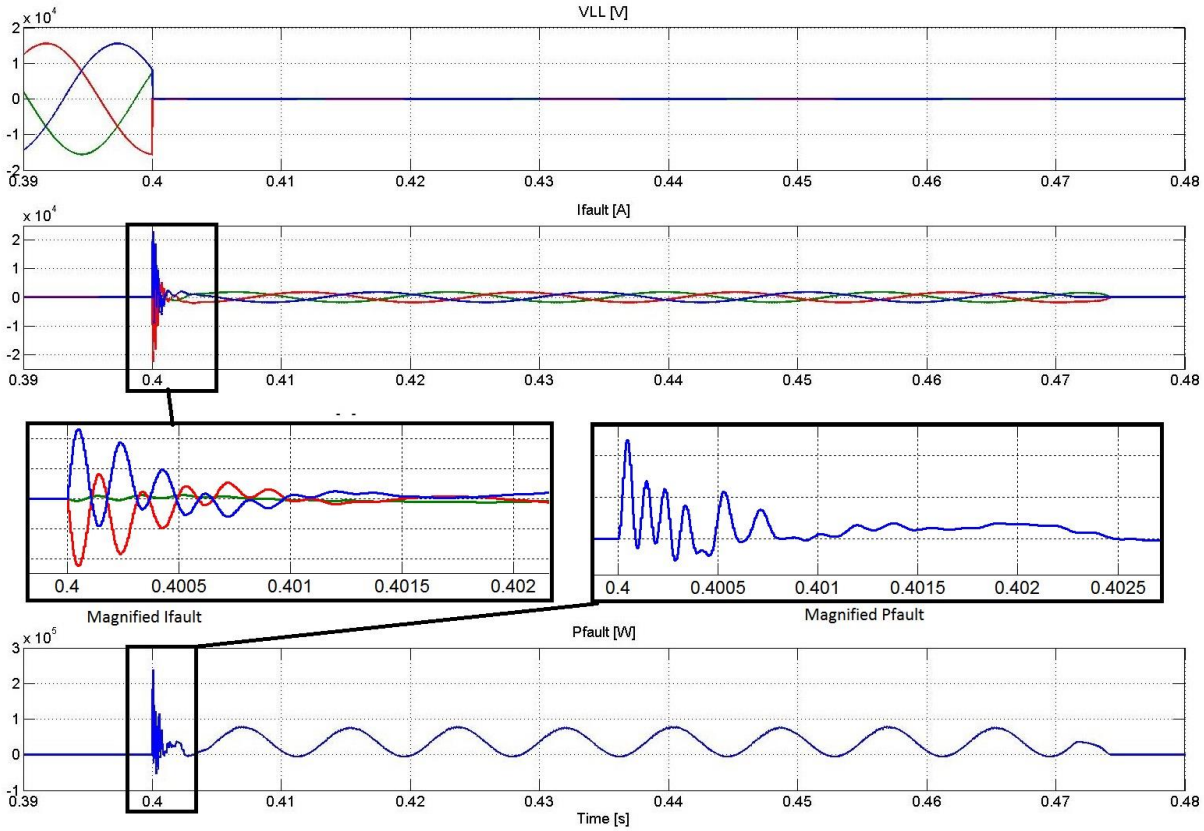


Figure 41 -Voltage, current and power at the fault location F2 during a three-pole short circuit with overcurrent protection relay tripping after 70 ms.

The resulting values are summarized in Table 12

Quantity	Time [s]	Magnitude
$\hat{V}_{fault,ss}$	0.4	0.44 [V]
$\hat{I}_{fault}$	0.4001	22.96 [kA]
$\hat{I}_{fault,ss}$	0.404	1.8 [kA]
$\hat{P}_{fault}$	0.4	237 [kW]
$\hat{P}_{fault,ss}$	0.404	73.4 [kW]

Table 12 - Peak voltage, current and power, measured at fault location during fault at F2.

After about 70 ms the relay trips. The first phase then becomes zero at t = 0.4715. The second phase reaches zero at t = 0.474, thereby extinguishing the final phase at the same time. The total fault clearing time is then 74 ms.

The voltage and current at the VSC terminals and the IGBT/Diode voltage and current is depicted in Figure 42:

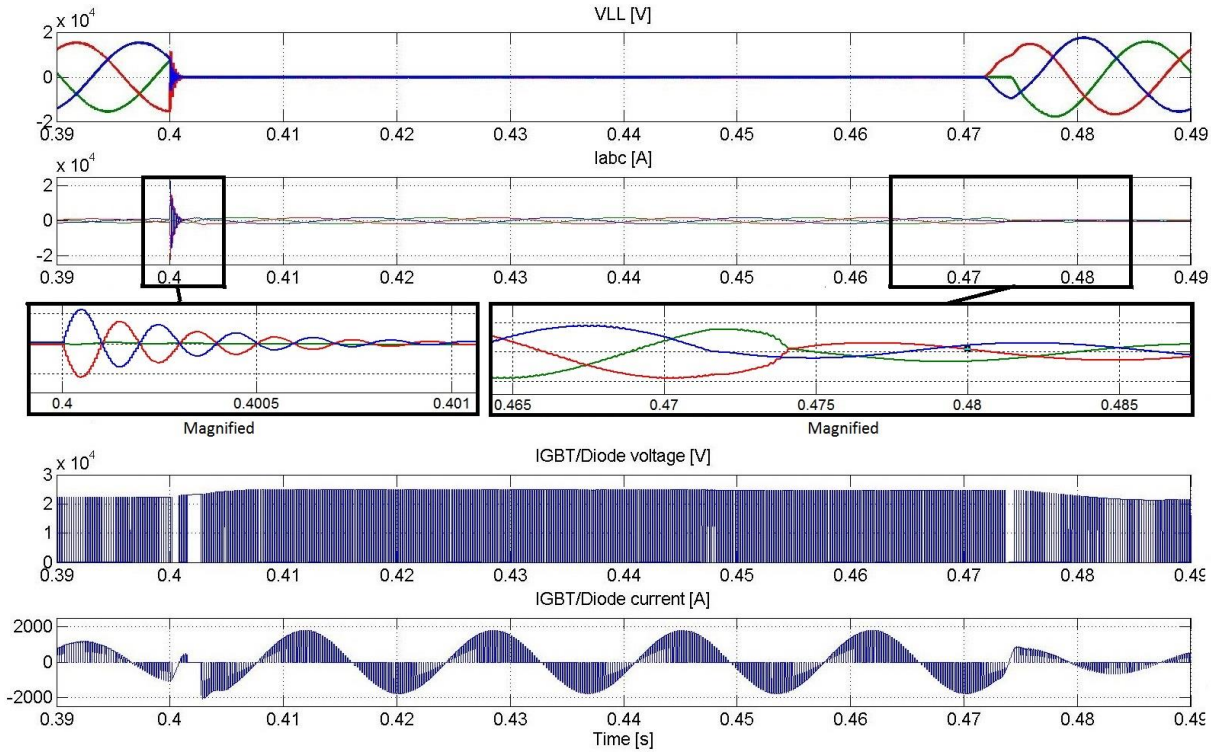


Figure 42 - Inverter terminal voltage and current, and IGBT/Diode voltage and current during fault at F2 with overcurrent relay installed.

The resulting values are summarized in Table 13

Quantity	Time [s]	Magnitude
$\hat{V}_{LL,ss}$	0.404	0.4 [V]
$\hat{I}_{abc}$	0.4001	22.3 [kA]
$\hat{I}_{abc,ss}$	0.406	1.8 [kA]
$\hat{V}_{IGBT/Diode}$	0.407	24.5 [kV]
$\hat{I}_{IGBT/Diode}$	0.403	2 [kA]

Table 13 – Peak voltage, current and power values at inverter terminals and IGBT/Diode switch peak voltage and current values.

The protection relay trips after about 70 ms, and the trip signal is sent to the circuit breakers. The voltage then resumes nominal level at approximately t = 0.487 s, and the currents then resume normal condition as the fault currents cross zero. The IGBT/Diode reverse voltage decreases back to nominal level.

The DC link voltage during the fault with protection relays installed is depicted in Figure 43.

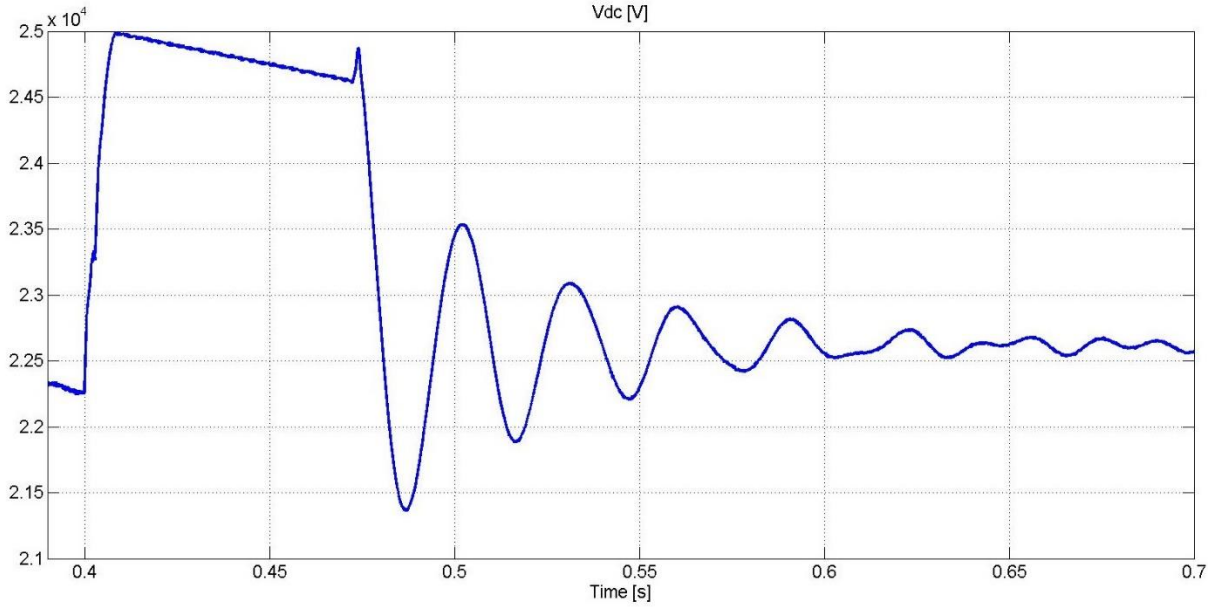


Figure 43 - DC voltage during fault at F2 with overcurrent relay tripping after 70 ms.

At t = 0.49 s. there is a slight increase in voltage to about 24.7 kV. After that, the voltage declines rapidly and starts oscillating. It reaches steady state at approximately t = 0.7 s.

The DC link voltage during the fault without protection relays installed is depicted in Figure 44.

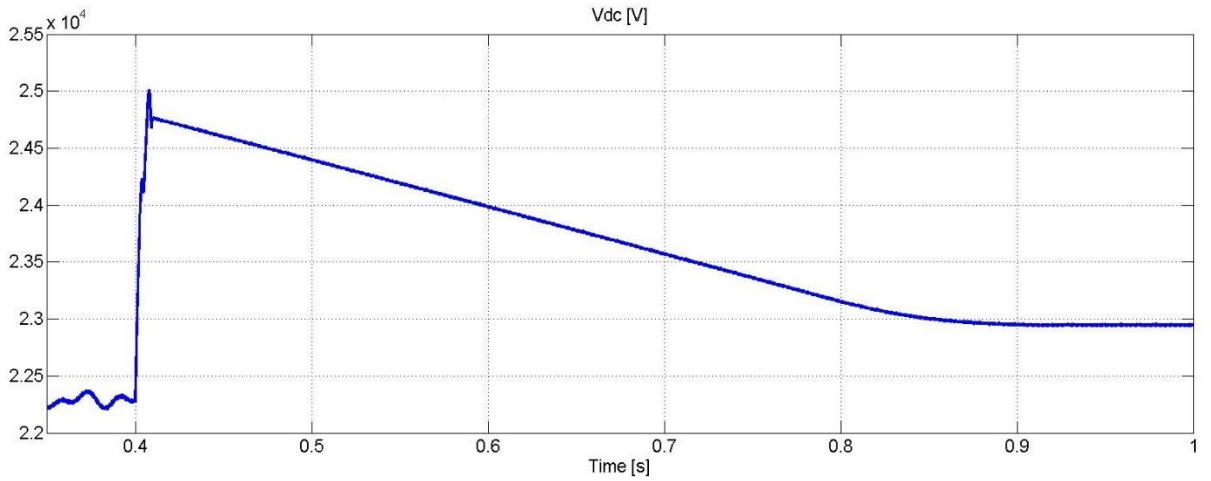


Figure 44 – DC voltage during fault at F2 without protection relays installed.

The DC voltage rapidly increases to a peak value of about 25 kV. After that, the voltage slowly declines and reaches a steady state fault value of 22.9 kV at t = 0.9 s.

4.4.3 Fault on Location F3

As the inverter itself is the protection for a fault at F3, and this is not modelled, only the short circuit characteristics without protection is simulated. The fault occurs at t = 0.4 s. The resulting voltage, current and power at the fault location is presented in Figure 45.

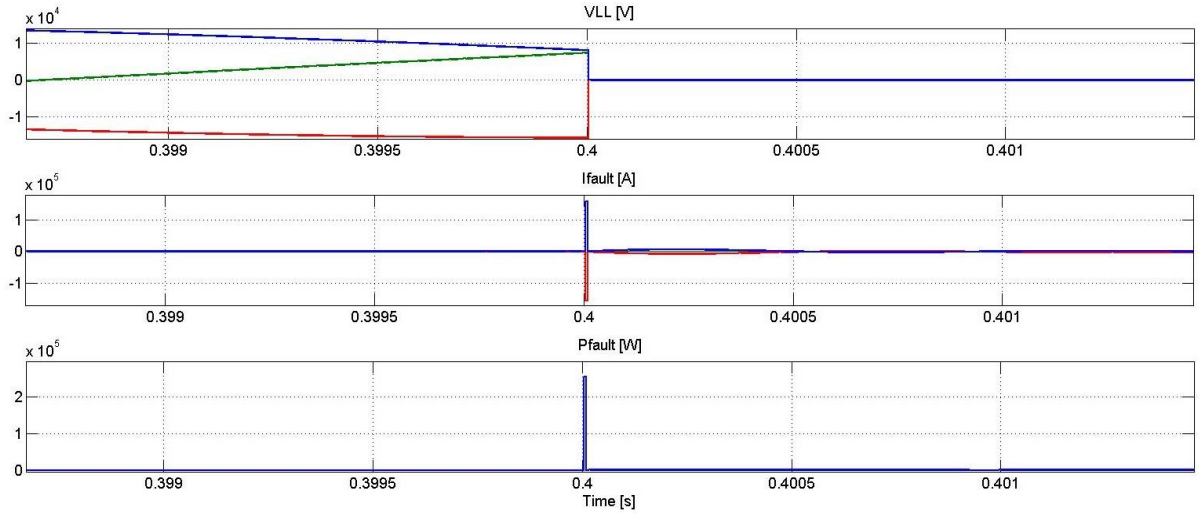


Figure 45 - Voltage, current and power at the fault location F3 during a three-pole short circuit.

The resulting values are summarized in Table 14.

Quantity	Time [s]	Magnitude
$\hat{V}_{fault,ss}$	0.4	0.005 [V]
$\hat{I}_{fault}$	0.4	159.2 [kA]
$\hat{I}_{fault,ss}$	0.4001	2 [kA]
$\hat{P}_{fault}$	0.402	253.6 [kW]
$\hat{P}_{fault,ss}$	0.402	28 [W]

Table 14 – Peak voltage, current and power measured at fault location during fault at F3.

The switch voltage and current is presented in Figure 46.

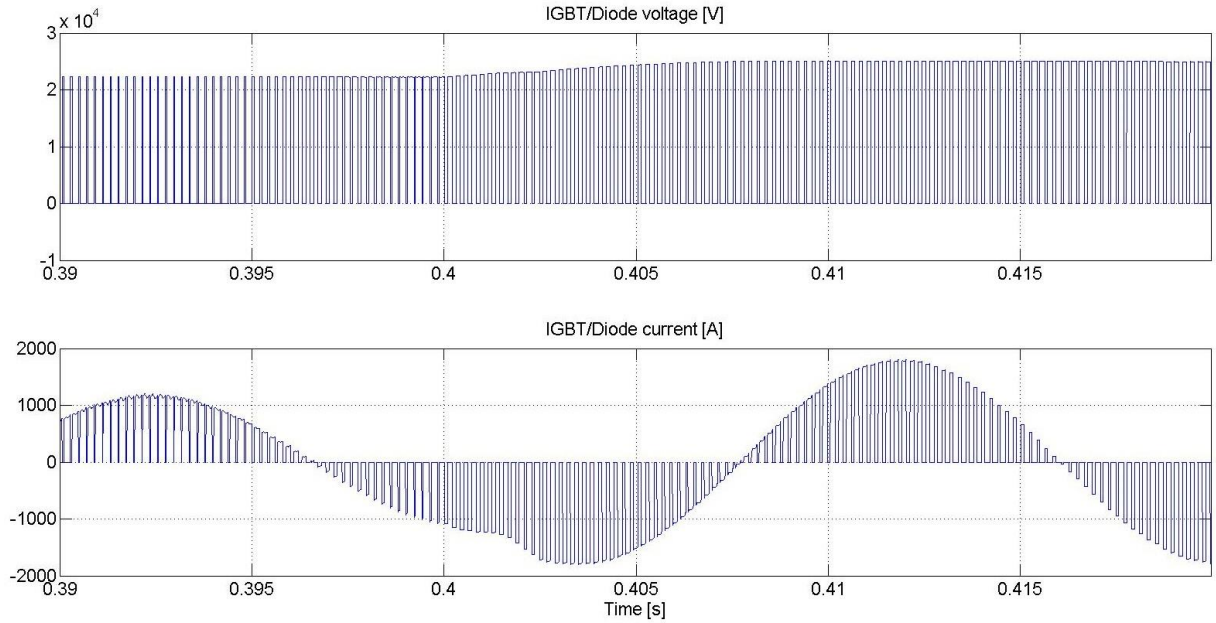


Figure 46 - IGBT/Diode switch voltage and current during fault at F3.

The switch blocking voltage increases to about 25 kV, and the current increases to a peak value of 1804 A.

The DC voltage during the fault is depicted in Figure 47.

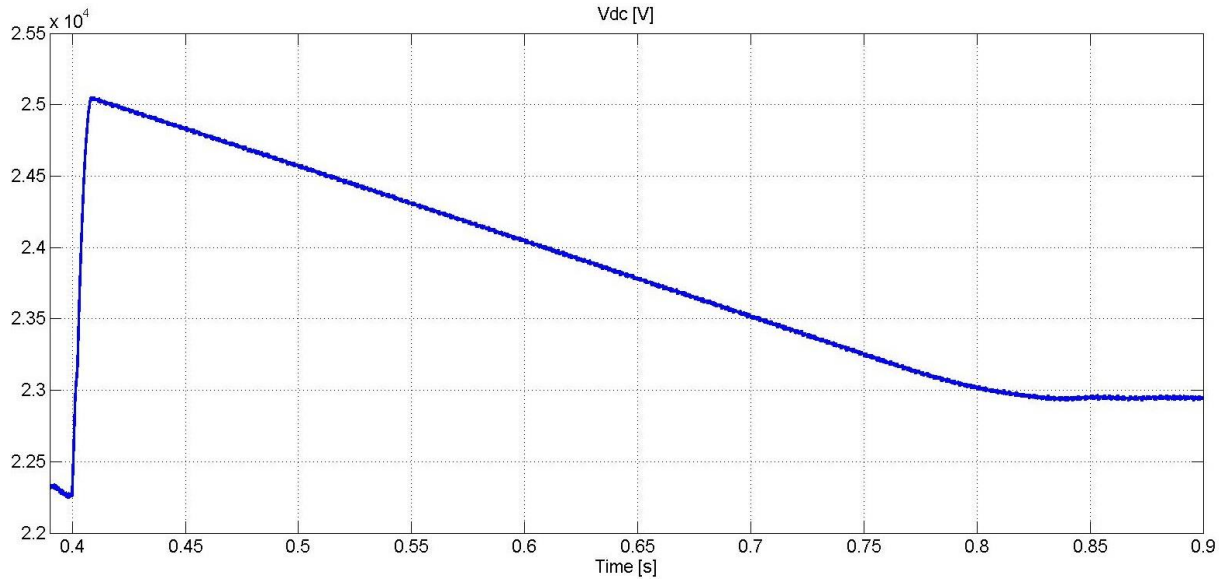


Figure 47 – DC voltage during fault at F3.

The DC voltage rapidly increases, and peaks at 25.1 kV. After that it sinks, until reaching a steady state voltage level of 22.59 kV at t = 0.95 s.

4.4.4 Fault on Location F4

The inverter switch voltage and current is depicted in Figure 48.

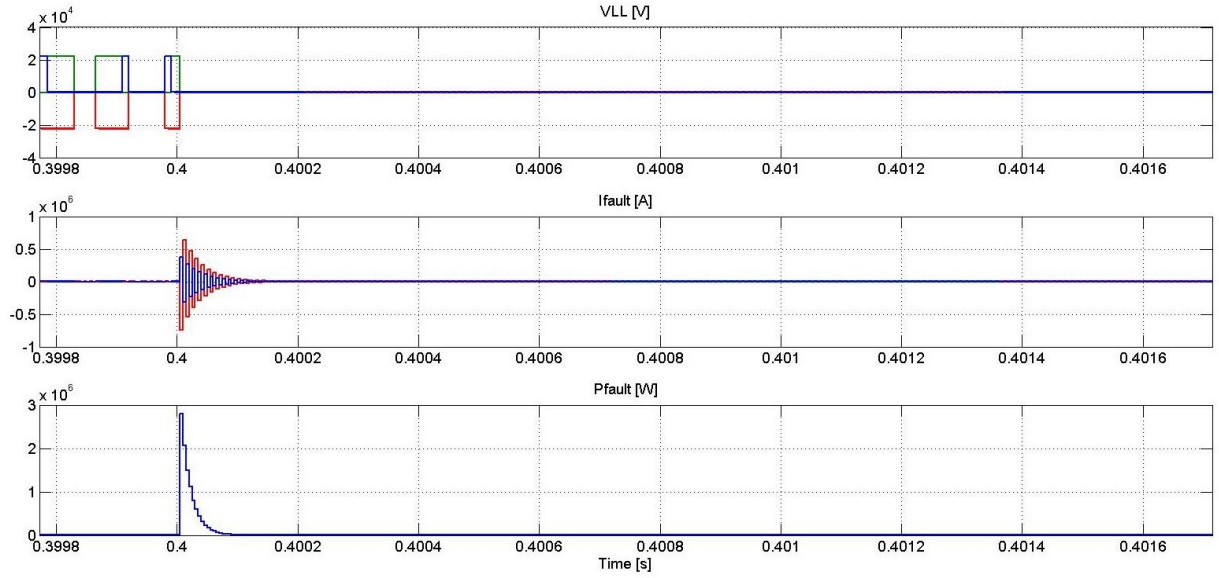


Figure 48 – Inverter switch voltage, fault current and fault power during fault at F4.

The resulting peak values are summarized in Table 15.

Quantity	Time [s]	Magnitude
$\hat{V}_{fault,ss}$	0.4	0.03 [V]
$\hat{I}_{fault}$	0.4	747 [kA]
$\hat{I}_{fault,ss}$	0.404	1.8 [kA]

$\hat{P}_{fault}$	0.4	2.79 [MW]
$\hat{P}_{fault,ss}$	0.4002	100 [W]

Table 15 Peak voltage, current and power values measured at fault location during fault at F4.

The switch voltage and current is depicted in Figure 49.

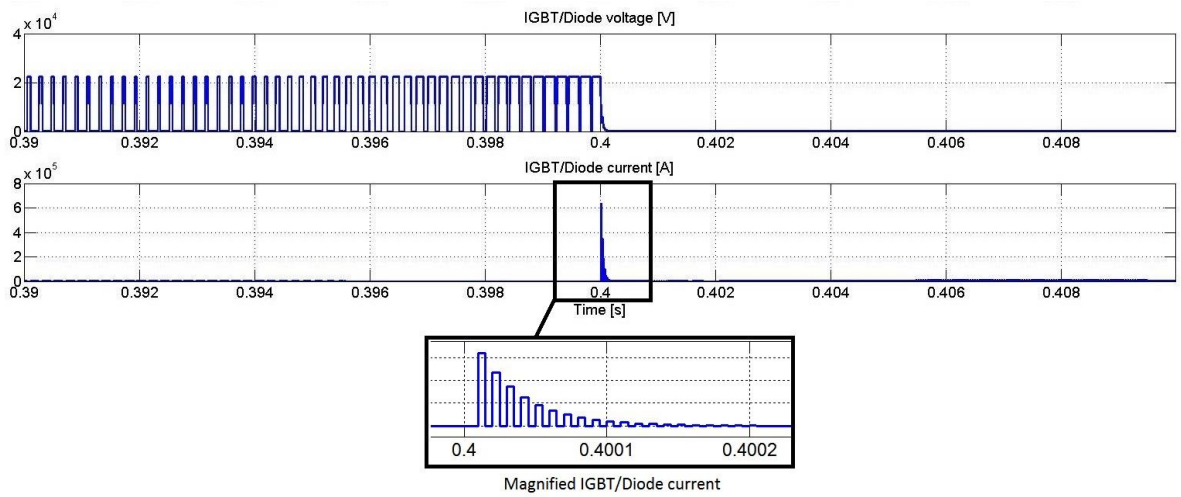


Figure 49 – IGBT/Diode voltage and current during fault at F4.

The peak voltage and current values are summarized in Table 16.

Quantity	Time [s]	Magnitude
$\hat{V}_{IGBT/Diode}$	0.4002	90 V
$\hat{I}_{IGBT/Diode}$	0.4	640 [kA]

Table 16 – IGBT/Diode switch peak voltage and current during fault at F4.

The DC voltage during the fault is depicted in Figure 50.

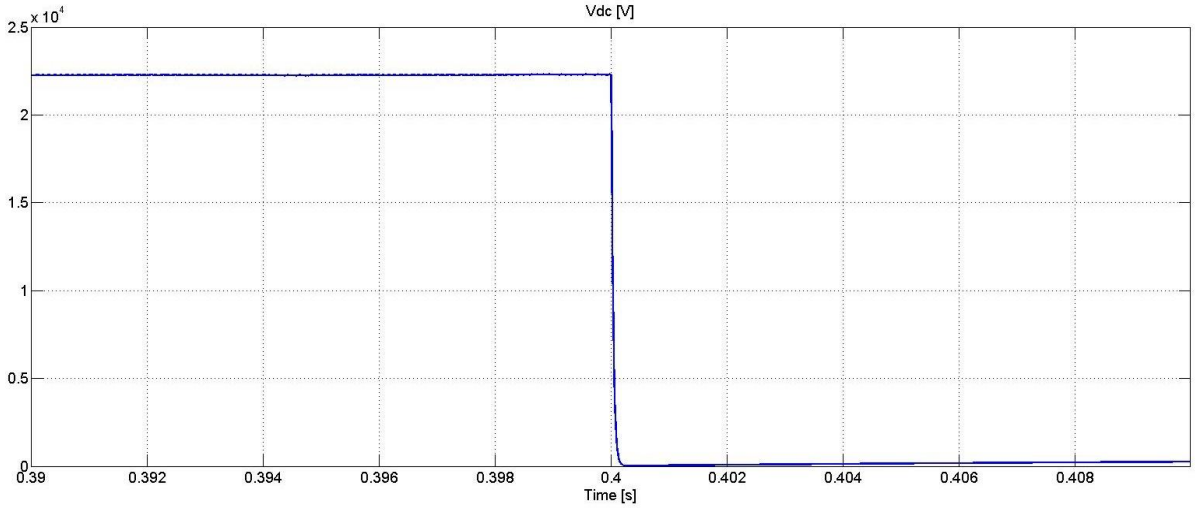


Figure 50 – DC voltage during fault at F4.

The DC voltage rapidly declines to 28 V, before slowly increasing.

4.4.5 Fault on Location F5

A bolted short circuit on the frequency changer DC link is simulated. A major supply line contribution to the fault current is expected in this fault, so the source generator sub transient reactance is included in this simulation. Hence, only the sub transient currents in the supply line are accurate, and simulations are done with the fast acting relay at F5 installed. The current and voltages are presented in Figure 51.

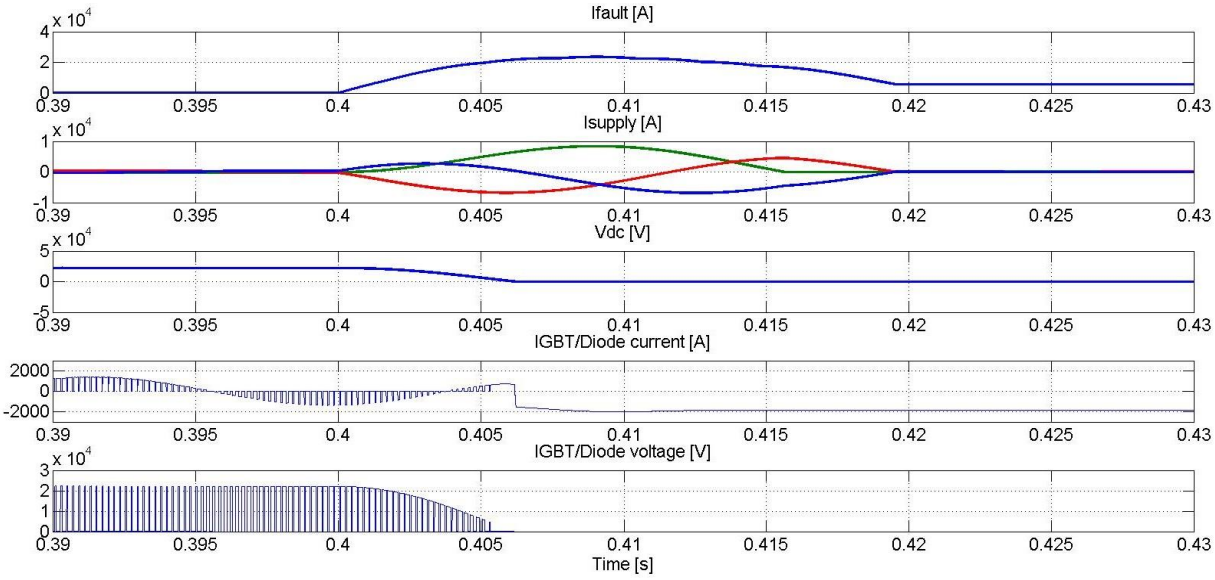


Figure 51 – Fault current, supply line current, DC voltage, and switch voltage and current during bolted short circuit at the DC link.

The DC voltage collapses to about 65 V at t = 0.4063. The diodes in the inverter starts conducting with a forward voltage of 28 V at t = 0.4063. The relay at F5 trips almost instantaneously, and the supply line current is cut at t = 0.419 s. After this, there is a slowly declining fault current flowing in the DC link with a magnitude of about 5.6 kA. In addition, the peak fault power is 5.5 kW.

The resulting peak current values are summarized in Table 17.

Quantity	Time [s]	Magnitude
$\hat{I}_{fault}$	0.409	23.51 [kA]
$\hat{I}_{supply}$	0.409	8.384 [kA]
$\hat{I}_{IGBT/Diode}$	0.409	1.956 [kA]

Table 17 – Peak fault current, supply line current and inverter switch current during a bolted fault at the DC link, F5.

4.4.6 Selectivity

Selectivity among the overcurrent protection relays at F1, F2 and F5 is maintained throughout the simulations with the values presented in 3.15.

5 Discussion of Results

5.1 Steady State Verification Simulations

The VSC control system proved to have a good response to changes in voltage or frequency references. At start up and during changes in load, there is oscillations on the DC link voltage. These oscillations are at 30 Hz, which is the same as the resonance frequency of the DC link LC filter. It could be possible to change the bandwidth of the filter to mitigate these oscillations. However, as the inverter control system is decoupled from the DC voltage, these oscillations are not affecting the inverter output voltages to any extent. The nominal load DC voltage is lower than the no load voltage due to transmission losses and voltage drop due to current commutation in the rectifiers.

In the harmonic analysis of system voltages and currents the THD of all jack-up rig side voltages and currents are within the limits mentioned in 2.8, the largest being the current THD at the HV switchboard with a THD of 0.59 %. Both current and voltage harmonics are centred on the fundamental and switching frequency. This is expected as the output LC filter has a corner frequency greater than the fundamental, but considerably smaller than the switching frequency. The harmonics around the fundamental are therefore not attenuated by the filter, while the large switching induced harmonics are attenuated with only the two relatively major odd sidebands present. The THD values on the load side of the load transformer is smaller than those at the HV switchboard. One reason for this might be the delta-wye connected load transformer trapping third harmonic currents, and multiples of it, in the delta winding.

The only major THD in the system is that of the supply line current with a THD of 9.28 %. This is because when the twelve-pulse rectifier commutates current at intervals with a frequency twelve times that of the line frequency, odd harmonic sidebands centred on this frequency and integer multiples of it are created. An input filter should probably be employed her to increase the power factor in the supply line.

The DC component in the inverter output may be due to the discrete solver used in simulations. As the output voltage is determined by the crossings of the control signal and the carrier signal, a discrete solver fails to detect the exact instant they cross. Hence a small DC component may occur. This effect is confirmed by testing different simulation step sizes and comparing. Although transformer saturation not is modelled in this thesis, a DC component in a real system could potentially cause the transformer to saturate, and should therefore be avoided. One solution is to increase the bandwidth of the inverter controller.

5.2 Load Scenarios

During step increases in load, the voltage dips briefly about 20 V for a short time, before settling at steady state. The steady state voltage decreases slightly with increased load. This is due to the transmission losses in the platform cable and load transformer. As the load model is voltage dependent, this causes the load to deviate from the intentional load power. The current in one of the phases exhibits some minor transient overshoot, but this is of no consequence to the interconnection or loads. The brutal load changes simulated are not realistic, as real loads are connected more gradually, but serves to test system and interconnection integrity. A more realistic, although quite brutal, change in load is presented

in the dynamic ramp load simulation. The voltage here is still slightly load dependent because of transmission losses, but the dynamic load is voltage independent. The load power consumption is therefore as expected. The current in this scenario has no transient overshoots, so the performance is satisfactory.

Finally, during a sudden loss of an entire island load, there is slight voltage transient from the steady state value of 686 V to 698.4 V. After the short transient, the voltage stabilizes at the steady state no-load voltage of 690.2 V. The current drops fast, only limited by the inductance in the circuit.

5.3 Fault Simulations

5.3.1 System Behaviour during Faults

When a fault occurs at the HV switchboard or at a load island, i.e. at F1, F2 or F3, the initial abrupt voltage decline of all phases causes the inverter output filter capacitors to discharge rapidly, thereby causing a high initial fault current. The largest fault current occurs in the phase with the most charged capacitor, i.e. the phase with the highest voltage at the time of the fault. During this initial period, the capacitors supplies most of fault current. As the d-axis current reference in the inverter control system is limited, the voltage controller will have a continuous error. The current controller will however follow the limited reference, which means that the switches in the inverter only conduct for short periods when the filter capacitors are supplying most of the current. The fault power is also limited due to the limitation of the current from the inverter and the resulting voltage drop. Once a fault occurs, the load power plummets, and the current controller holds the current at the limited value. As the inverter has inductors limiting the effect of transient currents on the output, the fast inverter control system manages to keep the switch currents within the limited value. The switches therefore seems to be adequately protected for faults on the load side of the output filter. None of these faults causes any overcurrent in the supply line due to the low fault power.

Another consideration is the rapid rise of the DC voltage when an AC side fault happens. This happens because when the inverter output power abruptly declines during a fault, the current in the DC link inductor declines rapidly, which in turn causes a rapid DC voltage rise. The rapid DC voltage rise causes the rectifier diodes to become reverse biased, cutting of the supply line. When the current in the DC link inductor reaches zero, the DC link capacitor starts discharging from this heightened voltage level, supplying the entire fault current. The fault current is very small seen from the DC side. This is because the AC side voltage is almost zero, while the DC side voltage is above 20 kV and stays high because of the limited energy dissipation in the system. When the capacitor reaches the nominal voltage level at about 23 kV, the rectifier and DC link inductor again starts to conduct a minor current supplied by the external platform. The slightly higher steady state DC voltage level during the fault is due to the reduced subsea cable, transformer and rectifier voltage drop because of the small steady state DC side and supply line current drawn by the fault.

When a fault happens at F4, the AC side filter inductances are shorted out, and there is no inductance between the fault and the DC link capacitor. This causes the DC link capacitor to discharge rapidly through the switches, without any current limitation. In addition, as the inverter controls the current in the filter inductors, the inverter control system will have no control over this part of the fault current. This causes a considerable current surge, which comes in addition to the energy from the AC filter capacitors.

The bolted short circuit on the frequency changer DC link, designated F5, causes the DC link voltage to drop to almost zero. The fault current then comprises of the current from the DC link capacitor discharging, in addition to a major contribution from the supply line through the forward biased rectifier diodes. Such a rapid discharge of the capacitor may cause the capacitor to fail, or even blow. Fast acting DC breakers should therefore be employed to limit this. Alternatively, the filter inductor could be increased to limit the supply line fault current contribution more.

5.3.2 System behaviour during fault clearing

Because the circuit breakers stop conducting at the current zero crossings, when the first phase reaches zero, the two remaining phases has a small voltage rise. When the second phase reaches zero, the current path is broken, and the fault is cleared. The exception is the fault at the DC link. After the supply line relay has cut the supply line current, there is still a considerable current flowing in the DC link through the inverter diodes. This would require a DC breaker to stop. The IGBT/Diode switch currents does however not exceed 2 kA. This is because the fault current is divided among the three inverter legs, so the current in each leg is one third of the fault current, assuming identical diodes. This should not cause any malfunction of the diodes.

Another phenomenon when the load side circuit breakers open, is that a phase shift occurs. This may cause the current in the switches to change direction. The phase shift when the fault is disconnected is due to the changed system impedance because of the circuit breakers opening.

After the faults at F1 or F2 is cleared, the non-faulted part of the system is restored. This causes the DC link capacitor to discharge quickly, which in turn causes transient oscillations because of resonance in the DC link LC filter. Faults at F3, F4 and F5 would cause the external power feed to be cut.

5.3.3 Comparison of results

The peak values at the different fault locations is summarized in

Fault location	$\hat{I}_{fault}\ [kA]$	$\hat{I}_{abc}\ [kA]$	$\hat{I}_{IGBT/Diode}\ [kA]$	$\hat{P}_{fault}\ [kW]$	$\hat{V}_{DC}\ [kV]$
F1	130.9	6.7	2	85.8	24.9
F2	22.96	22.3	2	237	24.7
F3	159.2	159.2	1.8	253.6	25
F4	747	-	640	2790	-
F5	23	-	2	5.5	-

Table 18 – Comparison of peak currents, power and DC voltage during faults at different locations

At F4 and F5 the DC voltage and HV switchboard currents are close to zero, and not included in the table.

The peak current during a fault at F1 is relatively large because of the load transformer, but has limited power due to the low voltage and impedances between the fault and the filter capacitors. The fault current during a fault at F2 is smaller than that of F1 and F3. This is because of the impedance between the source, i.e. the inverter filter capacitors, and the fault location. The inductance does however prolong the duration of the current surge. At F3 there is no inductance between the fault location and the filter capacitor, and hence the initial fault current is a very short, but large, spike. During a fault at F4, the current is considerably larger than at the other locations as explained in 5.3.1, and the fault at F4 is the only fault that causes overcurrent in the inverter switches. This would very likely cause a malfunction of the inverter, and cut the power feed to the jack-up rig. The fault at the DC link does not cause dangerous overcurrent in the inverter switches. It does however result in overcurrent from the supply line, which could cause malfunction of the rectifiers. In addition, it would cause the power to the jack-up to be cut.

It should be noted that on many jack-up rig power systems, the sub transient reactance of the synchronous generators are chosen deliberately to be high. This is to limit fault currents, so by using an external supply, the fault currents could be much higher than before.

6 Conclusion

This thesis describes the dimensioning and modelling of the interconnection of a jack-up rig to an external power supply in Matlab/Simulink. The simulation results presented proved the proposed solution to work as intended during stationary and variable load conditions.

The diesel engines traditionally supplying a jack-up, are slow, and are usually operated at low load to ensure redundant power availability. As the interconnection manages to follow variable loads instantly, depending of the stiffness and power management system on the external supply, this could mean increased overall efficiency on both platforms by coordinating power production to the loads on both platforms.

The harmonics generated by the power electronic equipment associated with the interconnection is largely supressed by the use of filters, and are within the requirements stated.

During fault simulations, critical faults, potentially causing blackout, was identified. Short circuit of the inverter switches, or a DC link pole-to-pole short circuit, would cause the external power supply to be disconnected causing blackout. The faults at F4 and F5 were the only faults that endangered the frequency changer components. Faults on load islands proved not to be critical to the interconnection. The peak fault currents was caused by the filter capacitances in the interconnection. To reduce the fault currents, a possible solution is to use a multilevel inverter instead of a two level. This would reduce the need for output filters, and thereby the peak fault currents.

If the proposed external supply were to be used as the sole supply of an existing unit, the existing overcurrent protection relays on that unit would most likely need changed, or recalibrated to the new fault currents.

7 Further Work

The model should be expanded to include a detailed model of the external power supply. By doing this, the interaction between the two systems could be studied in detail. Possible gains by redesigning the power management system on the supplying platform to include the load profile on the jack-up rig could then be studied. Furthermore, as the peak fault currents in the presented system largely was supplied by the inverter filter capacitors, a system using a multilevel inverter should be designed to minimize fault currents. A filter on the supply line could also be considered, and detailed load models could be considered to observe a more realistic load behaviour. Finally, a system with jack-up rig side generators connected should be designed. This with the purpose of studying the optimal load sharing between the local and external power supplies. This would also be interesting to study to identify possible improvements in redundancy, reliability and fault situations.

8 Bibliography

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Appendices

A. Simulink Models

Overview of Simulink Model

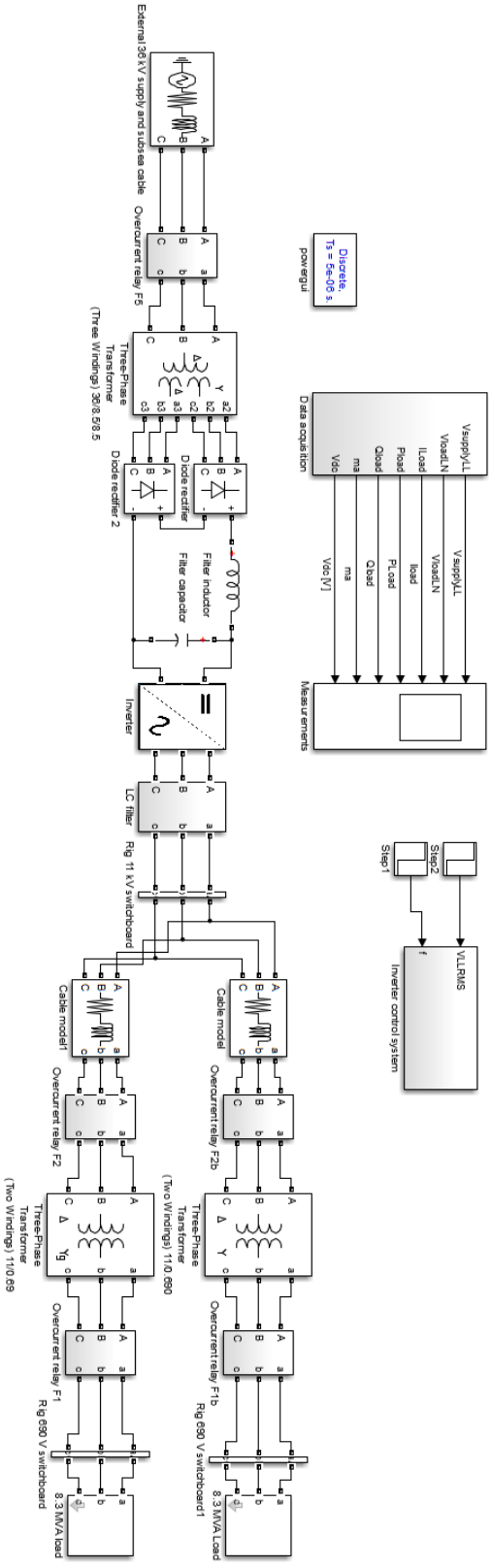

Figure 52 –System Simulink model overview

Inverter and Output Filter Simulink Model

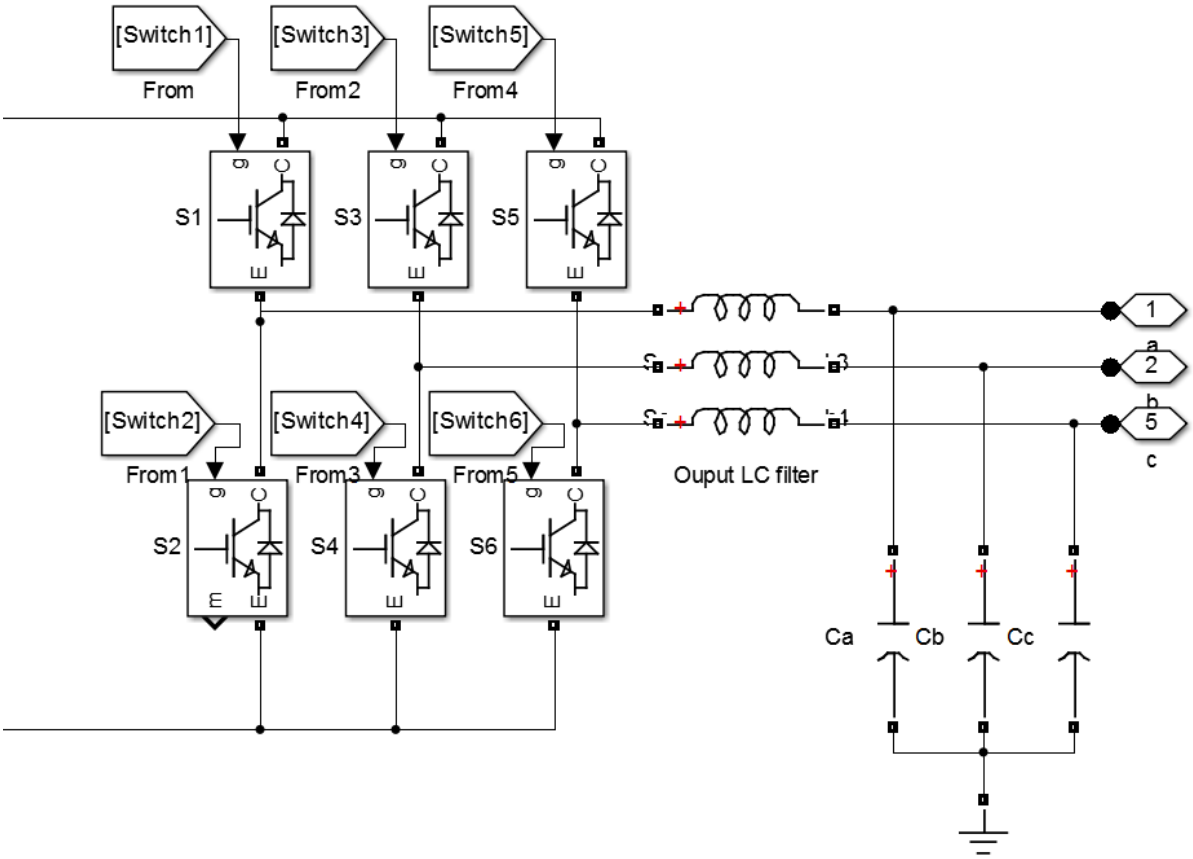

Figure 53 – Inverter and output filter Simulink model.

Simulink Model of Inverter control system

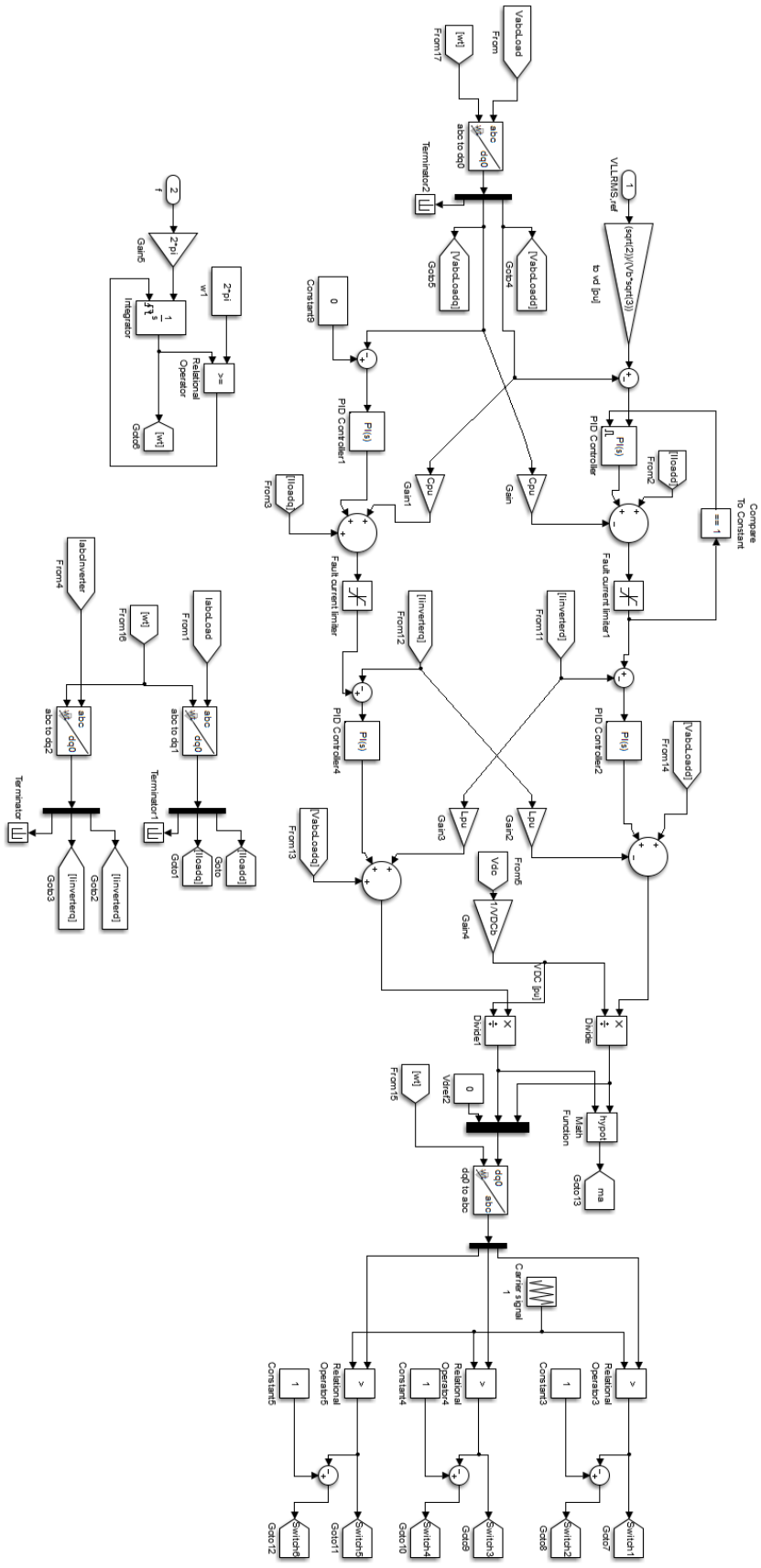

Figure 54 – Inverter control system Simulink model

Simulink model of Frequency generator

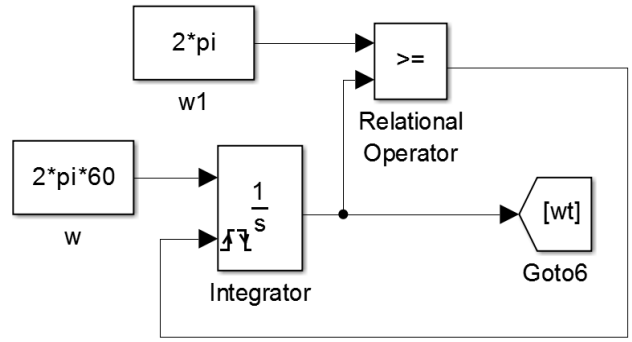

Figure 55 – Inverter frequency generator Simulink model

Simulink Model of Overcurrent Protection Relay

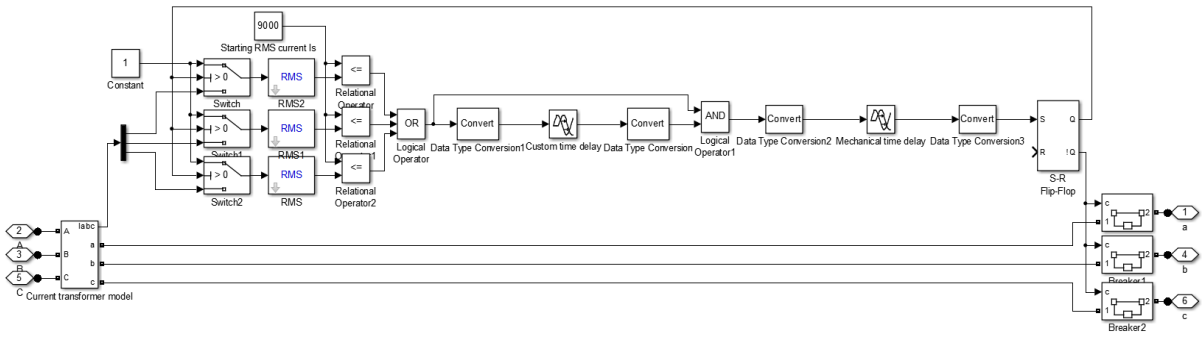

Figure 56 – Overcurrent protection relay Simulink model

B. Matlab Parameters Script

The values used in all components in simulations is defined in a Matlab script:

```
clear all

%System parameters
Vsource = 36000*(sqrt(2)/sqrt(3)); %Supply line nominal LN Peak voltage [V]
Pn = 15e6; %Nominal power [W]
Rcable = 0.26; %Subsea cable resistance [ohm]
Lcable = 0.4e-3; %Subsea cable inductance [H]
Ltopside = 9.81e-6; % Jack-up rig HV cable inductance
Rtopside = 30*60e-6; % Jack-up rig HV cable Ac resistance;
fsw = 4860; %Switching frequency [Hz]
Cdcfilter = Pn/((23e3*115+0.5*115*115)*fsw); %DC link filter capacitance
[F]
Ldcfilter = 13.63e-3; % DC link filter inductance [H]
Lacfilter = (23e3*0.8)/(6*100*fsw); %Inverter output filter inductance [H]
Cacfilter = 1/(((200*2*pi)^2)*Lacfilter); %Inverter output filter
capacitance [F]
wn = 2*pi*60; %nominal inverter output frequency [rad/s]
RIGBT = 17e-3; % IGBT onstate resistance [ohm]
D1 = 0; %Relay1 custom delay time [s]
D2 = 60e-3; %Relay2 custom delay time [s]
D5 = 0; % Relay 5 custom delay time [s]
Lsg = (((11e3)^2)/(25e6))*(1/(2*pi*50))*0.25; %External synchronous
generator subtransient inductance [H]

%Per unit base values:
Pb = Pn; % Base power = nominal power [W]
Vb = 11000*(sqrt(2)/sqrt(3)); % Base voltage [V]
Ib = (2*Pb)/(3*Vb); % Base current [A]
Zb = Vb/Ib; %Base impedance [ohm]
wb = wn; % Base frequency [rad/s]
Cb = 1/(Zb*wb); %Base capacitance [F]
Lb = Zb/wb; % Base inductance [H]
VDCb = 2.235e4; % DC link voltage base [V]

%Per unit values
Cpu = Cacfilter/Cb;
Lpu = Lacfilter/Lb;
wpu = wn/wb;

%Pi controller paramters [pu]

w0 = (2*pi*fsw)/10; %bandwith
rho = 1/sqrt(2); %damping factor

KpI = (2*w0*rho*Lpu)/wb; %Current controller proportional gain
KiI = KpI/((2*rho)/w0); %Current controller integral gain

%PI voltage controller parameters pu
w02=w0/10;

KpV = (2*w02*rho*Cpu)/wb; %Voltage controller proportional gain
KiV = KpV/((2*rho)/w02); %Voltage controller integral gain
```

C. Per Unit System

The per unit values are the actual values in SI units divided by the base values. The base values are summarized in Table 19:

Quantity	Expression and symbol	Description and unit
Power	$P_{base} = P_N$	System VA rating [W]
Voltage	$V_{base} = \hat{V}_{LN}$	Peak line to neutral voltage [V]
Current	$I_{base} = \frac{2P_{base}}{3V_{base}}$	Amplitude of nominal line current [A]
Impedance	$Z_{base} = \frac{V_{base}}{I_{base}}$	[Ω]
Frequency	$\omega_{base} = \omega_N = 2\pi f_N$	f_N is the load side grid nominal frequency [Hz]
Capacitance	$C_{base} = \frac{1}{Z_{base}\omega_{base}}$	[F]
Inductance	$L_{base} = \frac{Z_{base}}{\omega_{base}}$	[H]

Table 19 – Per unit system base values

D. Tuning of PI Controllers

The PI controllers are tuned by pole placement. The procedure used is largely based on the procedure presented in [38]. Using a cascaded control structure as in this thesis, the bandwidth of the inner current loop should be as large as possible without interfering with switching action [38]. The bandwidth of the current loop are therefore chosen to be an order of magnitude lower than the switching frequency. The voltage control loop should respond slower than the current control loop, and the bandwidth are chosen to be an order of magnitude smaller than that of the current control loop. Using Eq. 32 the d and q axis generic system transfer function becomes:

$$G_i(s) = \frac{i_{pu}(s)}{v_{i,pu}(s)} = \frac{\omega_{base}}{sL_{pu}} \qquad \textit{Eq. 40}$$

The generic transfer function of a PI controller can be expressed as:

$$G_{PI}(s) = K_{p,i}\left(\frac{T_{ii}s + 1}{T_{ii}s}\right) \qquad \textit{Eq. 41}$$

Where $K_{p,i}$ is the current loop PI controller proportional gain, and T_{ii} is the current loop integral time constant.

The system transfer function time constant is considered much larger than the inverter time constant which are usually approximated as: $\tau_{PWM} = \frac{1}{2f_{sw}}$. This is therefore neglected. The control loop block diagram then becomes:

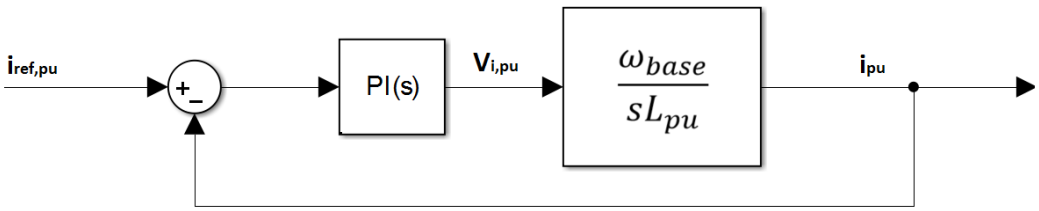

Figure 57 – Simplified control block diagram for the current loop.

The open loop transfer function becomes:

$$G_{OL}(s) = G_{PI}(s)G_i(s) = K_p\left(\frac{T_i s + 1}{T_i s}\right)\frac{\omega_{base}}{sL_{pu}} \qquad \textit{Eq. 42}$$

In addition, the closed loop transfer function becomes:

$$G_{CL}(s) = \frac{G_{OL}(s)}{1 + G_{OL}(s)} = \frac{K_p\left(\frac{T_i s + 1}{T_i s}\right)\frac{\omega_{base}}{sL_{pu}}}{1 + K_p\left(\frac{T_i s + 1}{T_i s}\right)\frac{\omega_{base}}{sL_{pu}}} \qquad \textit{Eq. 43}$$

$$= \frac{K_p\omega_{base}}{L_{pu}}\left(\frac{s + \frac{1}{T_i}}{s^2 + \frac{K_p\omega_{base}s}{L_{pu}} + \frac{K_p\omega_{base}}{L_{pu}T_i}}\right)$$

Assuming a second order system on the form [26], [38]:

$$G_{CL}(s) = \frac{\omega_0}{\beta}\frac{s + \beta\omega_0}{s^2 + 2\zeta\omega_0 s + \omega_0^2} \quad \textit{Eq. 44}$$

Finally, solving for the PI controller proportional gain and integral time constant yields:

$$K_{p,i} = 2\omega_0\zeta\frac{L_{pu}}{\omega_{base}} \quad \textit{Eq. 45}$$

$$T_{ii} = \frac{K_{p,i}\omega_{base}}{L_{pu}\omega_0^2} = \frac{2\zeta}{\omega_0} \quad \textit{Eq. 46}$$

Choosing the damping coefficient $\zeta = \frac{1}{\sqrt{2}}$ yields a good step response [38]. In addition, choosing the bandwidth ω_0 to be an order of magnitude lower than the switching frequency avoids interference with the switching action [38].

The voltage control loop are tuned the same way, based on Eq. 31. The current control loop time constant are considered negligible compared to that of the system. The damping coefficient are $\zeta = \frac{1}{\sqrt{2}}$. The voltage control loop has to be slower than the current control loop. The bandwidth of the voltage control loop is therefore chosen to be a magnitude of order less than that of the current control loop.

E. Park Transform

The inverter output voltages can be transformed onto a rotating reference frame by the relation [39]:

$$\begin{bmatrix} u_d \\ u_q \\ u_0 \end{bmatrix} = k * \begin{bmatrix} \cos(\theta) & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) \\ \sin(\theta) & \sin(\theta - \frac{2\pi}{3}) & \sin(\theta + \frac{2\pi}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} \quad \textit{Eq. 47}$$

Setting $k = \frac{2}{3}$, the inverse transform becomes:

$$\begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} = \begin{bmatrix} \cos(\theta) & -\sin(\theta) & 1 \\ \cos(\theta - \frac{2\pi}{3}) & -\sin(\theta - \frac{2\pi}{3}) & 1 \\ \cos(\theta + \frac{2\pi}{3}) & -\sin(\theta + \frac{2\pi}{3}) & 1 \end{bmatrix} \begin{bmatrix} u_d \\ u_q \\ u_0 \end{bmatrix} \quad \textit{Eq. 48}$$

Where:

- $\theta = \omega t + \delta_A$ [rad]
- $\delta_A =$ the initial phase shift of the voltage [rad]
- u_a, u_b, u_c is the a,b, and c phase voltages [V]
- u_d, u_q, u_0 is the direct, quadrature and zero component DC quantity voltages, respectively.

If the synchronous reference frame is aligned to rotate with the grid voltage, i.e. $\omega t = 2\pi f t$, with f = grid voltage frequency, and setting the phase displacement, $\delta_A = 0$, inserting the desired phase voltages yield:

$$\begin{bmatrix} u_d \\ u_q \\ u_0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos(\omega t) & \cos(\omega t - \frac{2\pi}{3}) & \cos(\omega t + \frac{2\pi}{3}) \\ \sin(\omega t) & \sin(\omega t - \frac{2\pi}{3}) & \sin(\omega t + \frac{2\pi}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} U_m \cos(\omega t) \\ U_m \cos(\omega t - \frac{2\pi}{3}) \\ U_m \cos(\omega t + \frac{2\pi}{3}) \end{bmatrix} \quad \textit{Eq. 49}$$

$$= \frac{2}{3} \begin{bmatrix} U_m \cos(\omega t)\cos(\omega t) + U_m \cos\left(\omega t - \frac{2\pi}{3}\right)\cos\left(\omega t - \frac{2\pi}{3}\right) + U_m \cos(\omega t + \frac{2\pi}{3})\cos(\omega t + \frac{2\pi}{3}) \\ U_m \cos(\omega t)\sin(\omega t) + U_m \cos\left(\omega t - \frac{2\pi}{3}\right)\sin\left(\omega t - \frac{2\pi}{3}\right) + U_m \cos(\omega t + \frac{2\pi}{3})\sin(\omega t + \frac{2\pi}{3}) \\ \frac{1}{2} U_m \cos(\omega t) + \frac{1}{2} U_m \cos\left(\omega t - \frac{2\pi}{3}\right) + \frac{1}{2} U_m \cos(\omega t + \frac{2\pi}{3}) \end{bmatrix}$$

Using the trigonometric identities:

$$\sin(a \pm b) = \sin(a)\cos(b) \pm \cos(a)\sin(b) \quad \textit{Eq. 50}$$

$$\cos(a \pm b) = \cos(a)\cos(b) \mp \sin(a)\sin(b) \quad \textit{Eq. 51}$$

This yield:

$$\begin{bmatrix} u_d \\ u_q \\ u_0 \end{bmatrix} = \frac{2}{3}\begin{bmatrix} \frac{3U_m}{2} \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} U_m \\ 0 \\ 0 \end{bmatrix} \quad \textit{Eq. 52}$$

So by using $k = \frac{2}{3}$ the transform is voltage invariant. By comparing the desired reference voltage, u_d^*, with the measured u_d, keeping u_q=u_0=0 and hence satisfying Eq. 52, using PI controllers, the output voltage magnitude are controlled. By using a PI controller to keep u_q= 0, the system phase and frequency is implicitly controlled as this is true only when the phase and frequency of the two reference systems are aligned.

F. Jack-up Cable Inductance

The conductors are assumed to be in a triangular configuration, placed in air, with no distance between the conductors. The conductors are assumed to be made of copper. The cross section is illustrated in Figure 58. d/2 is the conductor radius, assumed to be 8 mm based on usual cable dimensions. *r* is the cable radius, roughly assumed to be 16 mm. *D* is the distance between cable centres = *2r*.

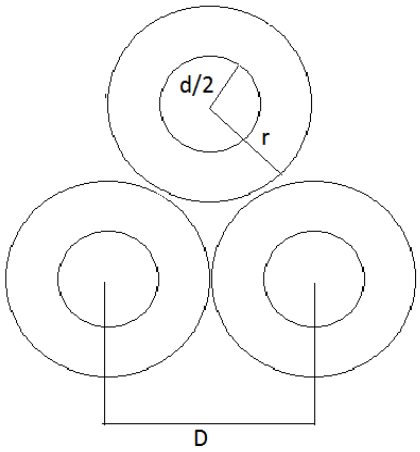

Figure 58 – Three-phase cable cross section

According to [3], assuming that the zero sequence currents are zero, the length of the conductors is much greater than the separation length, and that the conductors are massive, circular and of equal size, the pr. phase specific reactance can be calculated as:

$$X = \mu f ln\left(\frac{D}{0.39d}\right)\ [\Omega] \qquad \textit{Eq. 53}$$

Where:

- $\mu \approx \mu_0$, is the permeability in vacuum = $4\pi * 10^{-7}$ [A/m].
- *f* is the line frequency, here 60 Hz.
- *X* is the reactance = $2\pi fL$ $[\Omega]$

Inserting the values and solving Eq. 53 for *L* yield:

$$L = 0.327\ [\frac{\mu H}{m}]$$

Assuming 30 metres of cable between inverter output and load transformer yield $L = 9.81\ \mu H$.

G. Calculation of DC link Filter Inductor

The inductance for the DC link inductor is calculated. As a basis, ideal components and a stiff voltage source are assumed when calculating the inductance. Further tuning are later performed in Simulink.

Neglecting voltage drop due to current commutation, the output voltage of two ideal rectifiers in series with a $\frac{\pi}{6}$ [rad] phase displacement are:

$$V_d = \sqrt{2}V_{LL}\left(\cos(\omega t) + \cos\left(\omega t - \frac{\pi}{6}\right)\right) \{0 < \omega t < \frac{\pi}{6} \quad \textit{Eq. 54}$$

Where:

- V_{LL} is the AC side line-line RMS voltage [V] (secondary and tertiary transformer voltages)
- ω is the supply grid frequency = $2\pi f$ [rad/s], where f = 50 Hz.

The peak rectifier output voltage is:

$$V_{d,max} = \sqrt{2}V_{LL}\left(\cos\left(\frac{\pi}{12}\right) + \cos\left(-\frac{\pi}{12}\right)\right) = 2.73V_{LL} \quad \textit{Eq. 55}$$

Integrating the volt-second area of Eq. 54 and dividing by $\frac{\pi}{6}$ yeilds the average output voltage, V_{do}:

$$V_{do} = \frac{\sqrt{2}V_{LL}}{\frac{\pi}{6}}\int_0^{\frac{\pi}{6}}\left(\cos(\omega t) + \cos\left(\omega t - \frac{\pi}{6}\right)\right)d(\omega t) = \frac{6\sqrt{2}}{\pi}\,V_{LL} = 2.7V_{LL} \quad \textit{Eq. 56}$$

Temporarily assuming an infinite filter capacitor in parallel with the load, and a stiff voltage source, the inductor voltage $V_L(t)$ is:

$$V_L(t) = \sqrt{2}V_{LL}\left(\cos(\omega t) + \cos\left(\omega t - \frac{\pi}{6}\right)\right) - V_{do} \{0 < \omega t < \frac{\pi}{6} \quad \textit{Eq. 57}$$

In stationary conditions the inductor current starts rising when $V_L(t) > V_{do}$, and declines when $V_L(t) < V_{do}$. The first two points of intersection where $V_d = V_{do}$ are hence needed to find the current. Using Eq. 54 and Eq. 56:

$$\sqrt{2}V_{LL}\left(\cos(\omega t) + \cos\left(\omega t - \frac{\pi}{6}\right)\right) = 2.7V_{LL} \quad \textit{Eq. 58}$$

$$=> \cos(\omega t) + \cos\left(\omega t - \frac{\pi}{6}\right) = \frac{2.7}{\sqrt{2}} = 1.9092 \quad \textit{Eq. 59}$$

Expressing Eq. 59 in phasor notation with all angles expressed in [rad]:

$$1\angle 0 \; + 1\angle -\frac{\pi}{6} = 1.9092 \quad \textit{Eq. 60}$$

$$=> 1 + \cos\left(-\frac{\pi}{6}\right) + jsin(-\frac{\pi}{6}) = 1.9092 \quad \textit{Eq. 61}$$

$$=> 1.932\angle - 0.262 = 1.9092 \quad \textit{Eq. 62}$$

$$=> 1.932\cos(\omega t - 0.262) = 1.9092 \quad \textit{Eq. 63}$$

$$=> \omega t = \pm\, cos^{-1}\left(\frac{1.9092}{1.932}\right) + 0.262 \quad \textit{Eq. 64}$$

$$=> \omega t = 0.10822 \ \vee \ \omega t = \ 0.4158 \quad \textit{Eq. 65}$$

Using the chain rule, where ω is constant, the inductor voltage as a function of the inductor current, i_L [A], is:

$$V_L = L\frac{di_L}{d\mathrm{t}} = \frac{di_L}{d\mathrm{t}}\frac{d(\omega \mathrm{t})}{d(\omega \mathrm{t})} = L\omega\frac{di_L}{d\omega \mathrm{t}} \quad \textit{Eq. 66}$$

Solving for the current, integrating $\omega t = 0.10822$ to $\omega t = \ 0.4158$ and using Eq. 57:

$$\frac{V_{LL}}{L\omega}\int_{0.10822}^{0.4158}(\sqrt{2}\left(\cos(\omega t) + \cos\left(\omega t - \frac{\pi}{6}\right)\right) - 2.7)\, d(\omega t) = \Delta i_L \quad \textit{Eq. 67}$$

$$\frac{V_{LL}}{L\omega}0.00654972 = \Delta i_L \quad \textit{Eq. 68}$$

$$=> L = \frac{0.00654972 V_{LL}}{\omega \Delta i_L}\ [H] \quad \textit{Eq. 69}$$

H. Datasheets

Cable datasheet from Nexans

A2XS(FL)2Y>c<RAA 18/30(36) kV **Electrical Data**

1		2	3	4	5	6	7	8	9	
Nominal cross sectional area		Conductor resistance DC 20°C	Conductor resistance AC 90°C	Screen resistance 20°C	Capacitance	Inductance	Current rating	Losses	1s short circuit current after full load at 90°C conductor temperature	
conductor (mm^2)	screen (mm^2)	(Ω/km)	(Ω/km)	(Ω/km)	(µF/km)	(mH/km)	(A)	(W/m)	conductor (kA)	screen (kA)
70	16	0.443	0.57	1.15	0.16	0.45	200	70	6.8	3.3
95	16	0.320	0.41	1.15	0.17	0.43	237	72	9.2	3.3
120	16	0.253	0.32	1.15	0.19	0.41	269	74	11.7	3.3
150	25	0.206	0.26	0.73	0.20	0.40	299	76	14.5	5.1
185	25	0.164	0.21	0.73	0.21	0.39	337	78	17.8	5.1
240	25	0.125	0.16	0.73	0.22	0.37	388	81	23.1	5.1
300	25	0.100	0.13	0.73	0.25	0.36	432	82	28.9	5.1
400	35	0.0778	0.10	0.53	0.27	0.35	484	85	38.2	7.1
500	35	0.0605	0.080	0.53	0.30	0.33	544	89	47.7	7.1
630	35	0.0469	0.063	0.53	0.33	0.32	606	92	60.1	7.1

Diode datasheet from Infineon

Elektrische Eigenschaften / Electrical properties
Höchstzulässige Werte / Maximum rated values

Periodische Rückwärts-Spitzensperrspannung repetitive peak reverse voltages	T_{vj} = -40°C... $T_{vj\,max}$	V_{RRM}	5800 6000 6500 6800	V V
Periodische Rückwärts-Spitzensperrspannung repetitive peak reverse voltages	T_{vj} = 0°C... $T_{vj\,max}$	V_{RRM}	6000 6200 6700 7000	V V
Durchlaßstrom-Grenzeffektivwert maximum RMS on-state current		I_{FRMSM}	1670	A
Dauergrenzstrom average on-state current	T_C = 100 °C T_C = 60 °C	I_{FAVM}	790 1060	A A
Stoßstrom-Grenzwert surge current	T_{vj} = 25 °C, t_P = 10 ms T_{vj} = $T_{vj\,max}$, t_P = 10 ms	I_{FSM}	12500 10500	A A
Grenzlastintegral I²t-value	T_{vj} = 25 °C, t_P = 10 ms T_{vj} = $T_{vj\,max}$, t_P = 10 ms	I²t	780 550	10^3 A²s 10^3 A²s
Spitzensperrverlustleistung Surge reverse power dissipation	T_{vj} = 25 °C, t_P = 20 µs T_{vj} = $T_{vj\,max}$, t_P = 20 µs	P_{RSM}	80 90	10^3 W 10^3 W

IGBT datasheet from Infineon

A part of the datasheet for the IGBTs used. The complete datasheet is available online [36].

FZ2400R17HE4_B9

Package Name	A-IHMB190-2	**Totally lead-free**	no	**Halo-free**	no
ROHS	no	**Packing Size**	1	**Packing Type**	TRAYS
Configuration	Single switch	$I_{C(nom)}$ / $I_{F(nom)}$	2,400.0 A	**Technology**	IGBT4 - E4
V_{CEsat} (T_{vj}=25°C typ)	1.95 V	V_F (T_{vj}=25°C typ)	1.8 V	**Housing**	IHM B 190 mm