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Reactive Power Compensation and Active Filtering Capabilities of the Step-down AC Chopper

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Problem Definition

The aim of the study is to investigate the AC Chopper circuit, design a suitable control system, establish the system behavior in simulation and test the behavior on a laboratory prototype. The circuit will be connected to a 50Hz single phase grid. The final goal is to clarify if a possibility exists to use the AC Chopper as an active filter. To further specify the project goals, three goals were set:

1. During the initial investigation of the AC Chopper, some unexpected correlations were discovered concerning the open loop behavior. One task of the master project was to vary key device parameters to verify this newfound relation in simulation.

2. The capability of the AC Chopper to supply reactive power to a grid has been established in simulation. The device already has the traits of being less expensive and more efficient in reactive compensation than a STATCOM. It is interesting to see if the areas of use could be expanded to include active filtering. The student will map the active filtering capabilities of the AC Chopper using the predeveloped control system in dq-reference frame. Changes can be made to the control system if needed to achieve the necessary filtering capabilities.

3. Finally a prototype of the AC Chopper will be constructed to verify the results obtained in simulation. The prototype will work at a voltage of 400V with a rating of approximately 1kVAR.

The prototype ratings were later changed to simplify the prototype circuit and reduce the requirements of the component specifications.

Abstract

The Step-down AC Chopper (hereby referenced as "AC Chopper") has been presented in recent academic papers as a possible solution for reactive compensation. The goal of this project was to investigate and evaluate the topology to see if the praise could be justified. In addition, this project set a goal to take the research one step further by investigating if the uses of the AC Chopper could be expanded to include active filtering.

The ability of the AC Chopper converter to produce harmonic current was investigated. This was the first step in developing the AC Chopper's active filtering functionality. Theorems were developed and simulations were performed with both open and closed loop control. The results show that using the AC Chopper to produce harmonic current is very difficult if not impossible. This is due to intrinsic characteristics of the topology which leads to the converter producing multiple harmonics for a single control input frequency. Hence it was concluded that the AC Chopper is not fit for performing active filtering and that the results do not support continuing any further research on the AC Chopper's filtering capabilities.

A prototype of the converter was developed and built to compare the simulations against real observed behavior. The development process has been well documented in this thesis. Open loop control of the prototype was successfully implemented. The results show a good relation between the theory and the measured values. There are certain challenges connected to the realization of the AC Chopper, and the ways of dealing with these challenges have been described herein.

The topology was also compared to available technology to evaluate the competitiveness regarding reactive compensation at fundamental frequency. The AC Chopper was not found advantageous compared to the VSI, a modern available solution. The efficiency of the AC Chopper has been found to be slightly higher in simulation, but this has yet to be validated with tests on real prototypes. In addition to lacking the filtering capabilities, the AC Chopper has other disadvantages including expensive components and greater volume. Together the findings in this report suggests that the AC Chopper should be limited to use in single phase systems for reactive compensation at fundamental frequency in open loop control.

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List of Abbreviations

ACI   Atelier de fabrication de circuits imprimés - workshop at EPFL, Switzerland which produces PCBs

App   Appendix

BoomBox   Modular device developed for easier and faster control of power electronic devices

CCS   Code Composer Studio

dq-reference   Rotating reference frame using the Park Transform

EPFL   Ecole Poltytechnique Fédéral de Lausanne

Eq   Equation

FACTS   Flexible AC Transmission System

FAE   Fictive Axis Emulator

Fig   Figure

IDE   Integrated Development Environment

LEI   Laboratoire d'Électrionique Industrielle - laboratory at EPFL, Switzerland

PCB   Printed Circuit Board

PLL   Phase Locked Loop

PRBS   Pseudo Random Binary Sequence

PWM   Pulse Width Modulation

RMS   Root Mean Square

Sec	Section
SOGI	Second Order Generalized Integrator
STATCOM	Static Synchronous Compensator
SVC	Stativ VAR Compensators
UML	Unified Modeling Language
VSI	Voltage Source Inverter, also known as Voltage Source Converter

Chapter 1

Introduction

1.1 Background

In the modern grid there is a higher need for reactive power compensation. This demand is the result of a higher general power consumption and the introduction of new technology. New non linear loads add harmonics to the grid and raise the demand for reactive power[4]. Harmonics can also disturb the functionality or lifetime of existing grid connected devices, e.g. current ripple's effect on lifetime of electrolytic capacitors or the performance of older PLL technologies[6, 10]. The inductive losses connected with harmonics also lead to voltage drops which can strongly affect the performance of both the transmission lines and the connected loads. Thus measures are enforced to avoid or eliminate the presence of harmonics on the grid. Railway grids are typical weak grid systems which can experience large voltage fluctuations according to the load. In a railway grid there are also large inductive loads that contribute to the voltage fluctuations. These loads consists of long transmission lines and old train sets using thyristor technology[1, 13, 32].

Formerly, a rise in demand could only be countered by new investment in transmission lines and capacitor banks. But in this case, the new technology has given grid operators new solutions. Flexible AC Transmission System devices(FACTS) is technology used to condition transmission power transfer. By using such devices the need for new investments in transmission lines can be avoided [2, 31]. Reactive power compensation is a tool to help exploit the full potential of transmission lines without upgrading them. The compensation improves the power factor of the line which in turn maximizes the active power flow in the line[15]. The FACTS can also be used for local rapid control of voltage level and frequency so that the quality of the delivered power can be guaranteed. These new possibilities for real time control are known as smart grid functionality.

On the market today there exists several technologies for reactive power compensation. The cheapest and easiest solution is fixed capacitor banks. Such devices can help resolve

the voltage drops during high load. Capacitor banks have a fixed reactive power output, hence the output can not be varied and overvoltages can occur at low load situations. More flexible solutions are therefore needed. The most widely used solution is the Static VAR Compensator (SVC). These devices are based on thyristor technology and are therefore flexible and highly responsive solutions. The disadvantage of these devices is, as with all thyristor devices, that they produce a large quantity of low order harmonics. To avoid polluting the grid, large passive filters must be installed adding cost and complexity. Better performing solutions are available as the Static Synchronous Compensatos (STATCOM) based on the Voltage Source Inverter (VSI). The STATCOM is also able to filter out harmonics.

1.2   Brief Historic Overview of the AC Chopper

With the early research and fabrication of semi conductor devices, new solutions to old problems were developed. The mechanical variac was modernized with thyristors in anti-parallel. The new solution offered higher precision, more compact systems and digital control. In the 1970's the use of power transistors began to replace thyristors for the same variac circuit. Now the transistors could chop the input voltage with a frequency several times that of the grid. Concequently the voltage over the load could still be regulated without producing low order harmonics. This marks the the start of the AC Chopper[23].

The AC Chopper is AC/AC converter topology without an intermediary stage. The AC Chopper family consists of several topologies for solving a range of converter challenges. Different converter topologies may be able to elevate and/or lower the input voltage. One of these topologies is the step-down AC Chopper converter, also known as an AC Buck converter. This converter has been used for tasks including line conditioning, motor control, soft startup of induction motors and light dimmers[23, 8, 29]. In later times work has been done to eliminate harmonics in the voltage output of the AC Chopper, harmonics that could affect the functionality of the connected load[7, 17, 30].

One of the newer initiatives comes from the University of Toulouse which has been conducting research on a AC Chopper based static VAR compensator(SVC) for SNCF, the French National Railway Corporation[1, 26]. Through this work the AC Chopper is presented as a flexible compensation device with high efficiency, but it does not produce low order harmonics like classical SVCs. In simulation, the efficiency was found to be higher than for the VSI, hence the AC Chopper seemed to have an advantage over current technology.

The team at the University of Toulouse built and tested a prototype in the MVAR level. They designed a control system based on controlling the RMS value of the current. The prototype had a decent performance in supplying reactive power and showed an ability to filter out selected harmonics. Thus the AC chopper was acting as an active filter and was promising better efficiency than classic SVC devices and the VSI[21, 14].

1.3 Conclusions of the Preliminary Investigation of the AC Chopper

In the fall of 2012, a preliminary project was launched to understand the basic operation of the converter and start investigation into the possibilities of using the AC Chopper as an active filter. The work was based on much of the work done at the University of Toulouse[1, 26]. The two theses show that the AC Chopper could be used for reactive compensation and that there is a possibility to use it for some harmonic filtering. Further, they presented evidence for other advantages in favor of the AC Chopper over the standard VSI.

The hypothesis for the preliminary investigation was that using a control system based on PI regulators in a dq-reference could eliminate the harmonics. This is the same control system used for VSI solutions to perform active filtering. Modifications were made to make the control system fit to the AC Chopper topology and a control system based on a dq-reference was implemented and tested.

One requirement was that the controller produced a stable dc signal duty cycle for a grid voltage free of harmonics. A quasi-stable state was achieved for a situation where only the 50Hz current was controlled, the simplest of all operating conditions. The control system introduced a second order harmonic, making the control system performance worse than open loop. The performance was deemed unsatisfactory. Also, other tests in open loop regarding the correlation between inputs and outputs gave other results than expected, but the reason was not found.

The decision was taken to return to more elementary research of the AC Chopper. The dq control system was implemented with a condition that the AC Chopper model would work much in the same way as a VSI. But this condition was never tested or disputed. Therefore two goals were set for this project: to test the basic relations of the AC Chopper and documented the open loop behavior. With this information a new decision could be taken on how to use the AC Chopper in both closed loop fundamental current control and harmonic elimination. The last goal was to make a prototype to verify or refute the simulation results with observed data. Thus the problem to the current project was defined.

Chapter 2

AC Chopper Topology and Operating Principle

2.1 Circuit Layout

Figure 2.1.1 shows the full circuit layout of the Step-down AC Chopper. The step-down AC Chopper can be thought of as a Buck converter for AC voltages, only being able to lower the input voltage. The "Step-down AC Chopper" will just be referred to as "AC Chopper" throughout the report.

The AC source at the top represents the utility grid. The utility grid is connected to an input LC filter. The converter topology itself consists of four transistor switches $(T_1, T_{1c}, T_2, T_{2c})$ with four diodes connected in anti parallel $(D_1, D_{1c}, D_2, D_{2c})$. The device impedance is a passive element found at the converter output, which is an inductor and capacitor in series. How the impedance is used for reactive compensation purposes and the design process will be explained later in this section.

For a simpler discussion of the AC Chopper topology and a simplified simulation model, the topology showed in Fig. 2.1.2 is used. The input filter is removed and the grid becomes the direct input. for the converter. The amplitudes of the grid voltage and current are given by U_{IN} and I_{IN}. The voltage and current going through the device impedance are given by U_{OUT} and I_{OUT}. It is to be noted that with these definitions a positive I_{IN} with a positive U_{IN} the grid is supplying power even though the product of current and voltage is positive.

The incoming AC voltage is chopped by the switches, but the polarity of the voltage stays unchanged. Thus the applied voltage remains an AC voltage from the device impedance's point of view. The AC chopper is therefore an AC/AC device.
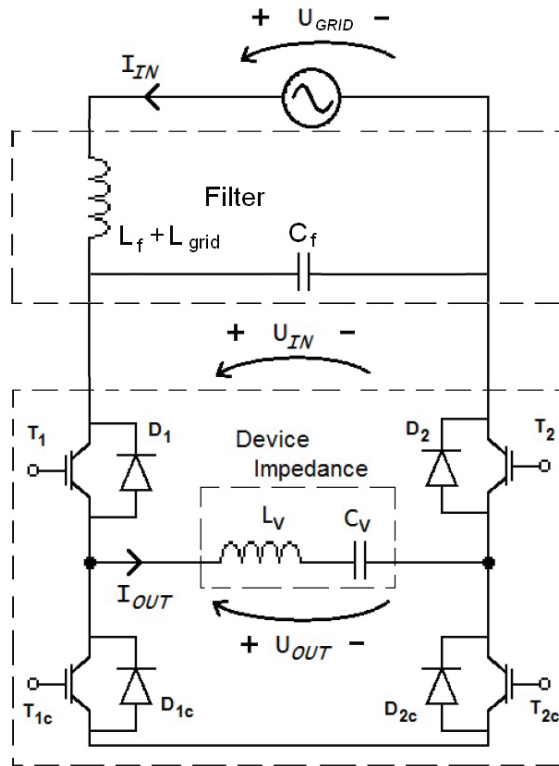
Figure 2.1.1: The full layout of the AC Chopper circuit with input filter for a single phase.

2.2   Switching Strategy

The device impedance is connected to an alternating voltage source, and the impedance experiences voltages and currents of positive and negative polarity. The commutation cells are designed to handle voltage and current flow in both directions, and the control system must also take this into account. The grid voltage must be measured and the switches are operated according to the polarity of the voltage. The control of the switches of the AC Chopper can be divided into two cycles according to the polarity of the grid voltage:

1. During the half of the period when the grid voltage has a positive polarity, the switches T_2 and T_{2c} are turned on to short circuit the right side of the circuit. Then T_1 and T_{1c} are treated like a switching cell to control the voltage over the load. When T_1 is switched off, the diode $D_{1c}+T_{2c}$ or $D_{2c}+T_{1c}$ constitute a free wheeling path and the current flows in the lower loop of the circuit (Figure 2.2.1a, 2.2.1b).

2. During the half of the period when the grid voltage has a negative polarity, the switches T_1 and T_{1c} are turned on to short circuit the left side of the circuit. Then
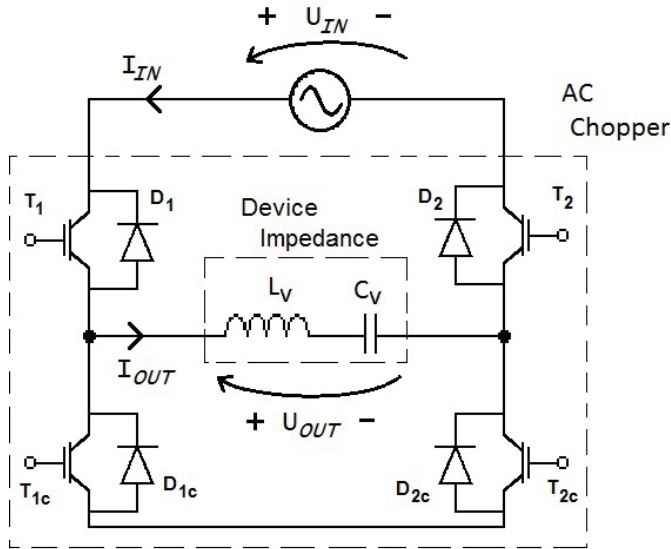
Figure 2.1.2: A simplified layout of the AC Chopper for a single phase. For all following discussion of the topology this model is used for simpler explenations.

T_2 is switched on and off to control the voltage over the load. When T_2 is switched off, the diode $D_{2c}+T_{1c}$ or $D_{1c}+T_{2c}$ constitute a free wheeling path and the current flows in the lower loop of the circuit (Figure 2.2.1c, 2.2.1d).
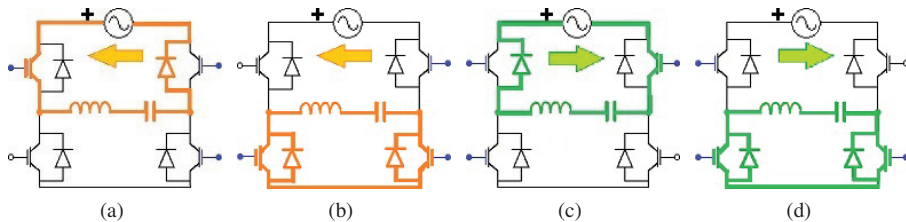
Figure 2.2.1: Current paths for the four different switch states according to positive (orange) or negative (green) polarity of the grid voltage.

This control regime is similar to that of the DC/DC Buck converter. If the varying input voltage over the device is disregarded and one looks at each of the isolated control cycles, the switching strategy is identical to that of the Buck converter: the input voltage is chopped over an impedance leading to reduced voltage and increased current when looking at the integrated values divided over the period (RMS values). As with the Buck converter, a duty cycle is used to express the relation between the input and the output from the converter. The duty cycle, α, has the range [0,1] and is defined as $\alpha = \frac{t_{ON}}{T_{sw}}$ where t_{ON} is the time the switch is turned on during the switching period T_{sw}. Here t_{ON}

represents both t_{ON,T_1} and t_{ON,T_2} for the two switches T_1 and T_2 within each of their respective control cycles.

Note that in practical applications the value of α_{max} will reside within [0.9, 0.95] in RMS value. This is related to challenges with zero crossing detection and safe operating margins, resulting in a maximum output value less than one at operation with duty cycle equal to one.

The PWM signal generation and gate signaling realizing the above switching setup is described in furter detail in App. A. The resulting correct open loop behavior is seen in Fig. 2.2.2. The simulation was done in Matlab Simulink with values equal to the nominal values for the prototype (400V RMS, 1kVAR).
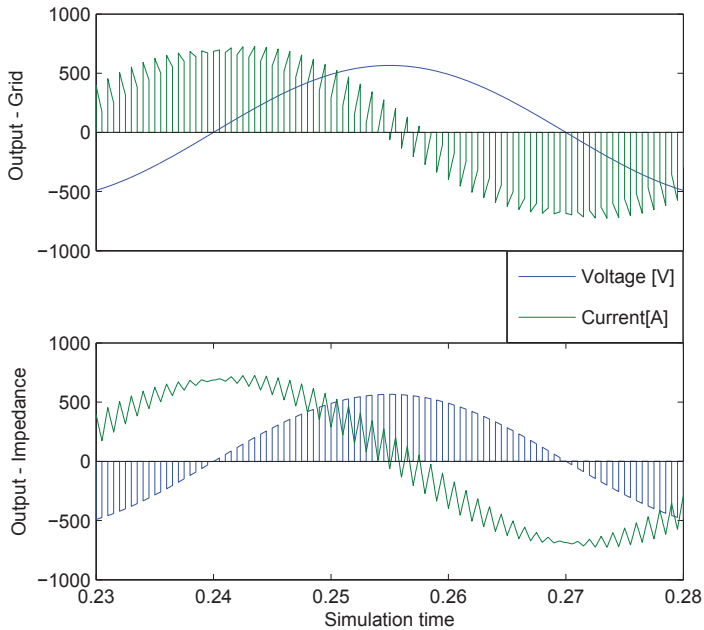
Figure 2.2.2: Form of input and output signals if the switching strategy is successfully implemented. The results are from a simulation with duty cycle set to 0.5. The component values were arbitrary. Grid-side voltage and current are shown in the top graph, while the applied voltage and current over the device impedance is seen in the bottom graph.

The input voltage is chopped over the device impedance according to the duty cycle. The results is an impedance voltage of the same frequency and phase shift, but with a modulated amplitude. For the currents the situation is swapped. The grid current appears like a chopped version of the impedance current. The chopped current is the reason for adding an input filter to the AC Chopper. The impedance current is a 50Hz current for which the phase shift is a result of the device impedance.

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2.3   Basic Relation

The similarity between the AC chopper and the Buck converter is not limited to their ability to lower an input voltage. In addition, the basic relations between the converter input and output are also identical as shown in Eq. 2.3.1. For the AC Chopper, the basic relation is only valid for the fundamental wave, which is 50Hz throughout this report.

$$U_{OUT} = U_{IN} \cdot D$$
$$I_{OUT} \cdot D = I_{IN} \tag{2.3.1}$$

In Eq. 2.3.1 the notation 'IN' indicates the current or the voltage on the grid side of the converter while the notation 'OUT' indicates the current or the voltage of the device impedance, as depicted in Fig. 2.1.2. The duty cycle is noted as D. Implementing the above described switching pattern and sending a duty cycle as input to the converter, the relation in Eq. 2.3.1 is realized. How to use this controllability is explored in the next section.

2.4   Operating Principle for Reactive Compensation

To decide how to control the AC Chopper for reactive compensation, a model for the power compensation possibilities of an AC Chopper was established. The starting point for this model is a capacitor bank. When the capacitor bank is coupled to the net, the reactive power supplied to net is described as follows (R $\simeq$ 0 $\Rightarrow$ Z = Q):

$$Q = \frac{U_{OUT}^2}{X} \tag{2.4.1}$$

where U_{OUT} is the voltage applied to the capacitor bank. The expression is developed further by expressing the reactance:

$$X = \frac{1}{\omega C_V} - \omega L_V = \frac{1 - \omega^2 L_V C_V}{\omega C_V} \tag{2.4.2}$$

$$Q = V_{OUT}^2 \frac{\omega C_V}{1 - \omega^2 L_V C_V} \tag{2.4.3}$$

The passive components C_V and L_V are chosen at the time of design, so Eq. (2.4.3) shows that if the reactive power is to be modulated then the voltage level must be changed. The basic relation of the AC Chopper for which the duty cycle is used to vary the output voltage amplitude(Eq. 2.3.1) is inserted in Eq. 2.4.3 and the final equation for reactive power output becomes:

$$Q = V_{IN}^2 D^2 \frac{\omega C_V}{1 - \omega^2 L_V C_V} \tag{2.4.4}$$

The Eq. 2.4.4 reveals the basic control principle for the AC Chopper. Assuming a constant grid voltage ($V_{IN} = constant$) and for a given set of component values, the device can vary its reactive power output by changing the duty cycle, α. Should the grid voltage change then the maximum power output would also change. This behavior is identical to SVC devices, while VSI output is less dependent on grid voltage. The maximum power output is shown in the power profile for the AC Chopper in Fig. 2.4.1.
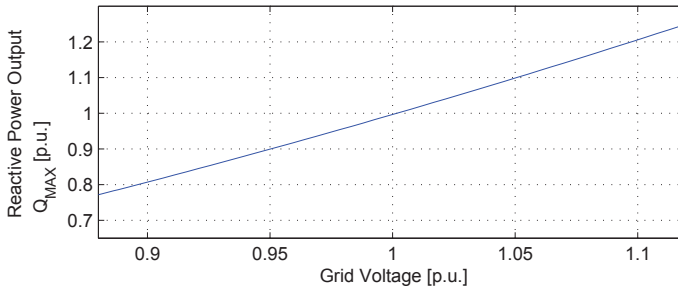
Figure 2.4.1: The maximum reactive power output of the AC Chopper as a function of grid voltage.

The figure shows that for a small decrease in grid voltage the maximum output decreases substantially. An example is a 5% voltage decrease leads to a approximately 10% loss in device output capability.

In times with large need for reactive power in the grid, the grid voltage level declines. A VSI would be able to supply reactive power close to its rated value. But for the AC Chopper the reactive power output decreases with grid voltage, hence the device rating is decreasing with the increasing demand. Compared to the VSI this property is a clear disadvantage, since the reactive power output decreases as the need increases.

Eq. 2.4.4 reveals that it is possible to control the reactive output of the AC Chopper by changing the duty cycle. But the duty cycle is squared which poses a challenge for the control system. The control system must compensate for this feature.

2.5 Active Filtering

The active filtering scenario is shown in Fig. 2.5.1. The generator and the transmission line is modeled as a AC voltage source and an inductance in series. A non-linear load and the filtering device are connected to the same node. The filtering device has been chosen to be the AC Chopper for the figure. The non-linear load consumes a current, i_{load},
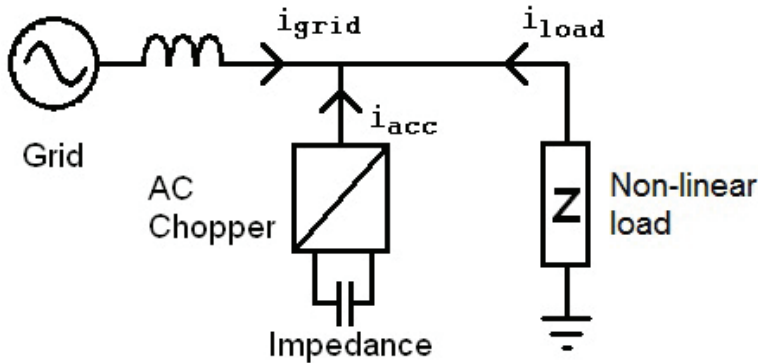
Figure 2.5.1: Active filtering concept. The harmonic current is measured and the opposite current is supplied from the filter. The result is that the merged currents negate each other and only the fundamental component of the grid current remains.

consisting of a fundamental component and a certain amount of harmonic components. The active filter measures the harmonic content of the current and outputs a current, i_{acc}, with the same content, but shifted 180°. Consequently i_{load} and i_acc merge and the harmonic content is eliminated. Thus the grid current is strictly fundamental. If the active filer also provides reactive power compensation then the reactive component could be compensated also and the grid current would be purely active.

From this scenario it is evident that the AC Chopper must be able to be operated as a controllable current source to achieve active filtering capabilities. The controllable current source could then provide harmonic currents for which each harmonic the amplitude and phase shift is controlled separately.

The relation used to model the AC Chopper was the basic relation . Since the basic relation for the AC Chopper, described by Eq. 2.3.1, was only thought to hold for 50Hz operation the closed loop current control was only done for the 50Hz component. Control of harmonic current was set outside the scope of the project until the model for harmonic current was confirmed.

Rather the possibilities for controlling the harmonic current would be investigated. The AC Chopper would be controlled in open loop and a appropriate control implementation would be made to facilitate the harmonic current production.

2.6 System Values For Simulations

The process of dimensioning of the device impedance and input filter is found in App. B. The values for the grid, device impedance, input filter and PWM unit are listed in Table 2.6.1. The original rating and nominal values mentioned in the problem definition were changed to accommodate a faster and simpler development of the prototype. The grid

Table 2.6.1: Grid, component and system values used in simulation

	Voltage	Current	Impedance	Frequency
Nominal values	50.0V RMS	2.4A RMS	20.8Ω	
Grid	50.0V RMS	-	-	50Hz
Grid [p.u.]	1.0	-	-	-
Device impedance	5mH	140μF	0.5$m\Omega$	190Hz
Device impedance [p.u]	2.40e-4	2.92e-3	2.40e-2	
Filter	2mH	47μF	-	519Hz
Filter [p.u.]	9.60e-5	9.79e-4	-	-
PWM	-	-	2000Hz	-

voltage was set to a maximum of 50V RMS and the nominal current was set to achieve approximately 100VAR reactive compensation. The PWM frequency was set to 2kHz unless specified otherwise.

2.7   Chapter Conclusion

In this chapter the AC Chopper has been introduced and explained through discussion about the circuit layout, switching strategy and basic relations. Based on these discussions, further work on finding a control scheme has been identified.

From the EMR method it was clear that to be able to control the grid current and the delivered reactive power, the fundamental impedance current must first be controlled. After the impedance current is controlled with a sufficient performance the work of controlling the grid current and the reactive power compensation can be continued. Hence the work done in closed loop control featured in Chapter 6 focused on controlling the fundamental impedance current.

As for the work concerning the active filtering possibilities of AC Chopper, a different approach was taken. It was unknown if the basic relation in Eq. 2.3.1 was valid for other frequencies than the fundamental. Since no reference to this issue was found in the literature, extensive testing in open loop was done to map the system behavior. This work is presented in Chapter 5.

In addition, the values for the circuit have been found and will be used in the simulations and later in designing the prototype. The values are noted in Table 2.6.1.

Chapter 3

Competing Technologies to the AC Chopper

When introducing a new product to an existing market, it is important to obtain an overview of the other competing solutions. The majority of this report concerns the technical aspects of the AC Chopper topology. As a developing technology it is important to compare it to the other available technologies to identify its strengths and weaknesses. Only then can the competitive benefits be identified. In this chapter the existing alternatives for reactive compensation are presented. The comparison with competing solutions is made in Chapter 10.

3.1 Voltage Source Inverter(VSI) and STATCOM

The Voltage Source Inverter(VSI), is the most modern of the widely used devices for reactive power compensation. It is also known as a Voltage Source Converter(VSC). The VSI is an AC/DC device in which the capacitor is coupled to the grid by a full bridge and an L-filter. The circuit is shown in Fig. 3.1.1.The capacitor voltage is a constant DC voltage, but because of switching transients the voltage will contain some ripple. The ripple can be minimized by increasing switching frequency or by increasing the capacitance. The VSI can produce any signal within the bandwidth of the converter and at maximum peak of the capacitor voltage. This makes the VSI very versatile. The topology is the same as for one half of back-to-back converters, a converter which is found in many applications today. Example of such application include electrical drives and power generation.
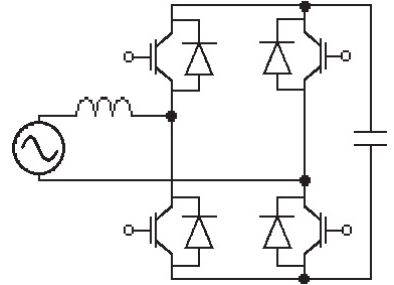
Figure 3.1.1: The circuit layout of the Voltage Source Inverter.

In reactive power compensation the VSI is known as a Static Synchronous Compensator(STATCOM). Due to the inherent characteristics of the VSI, the STATCOM can supply both inductive and capacitive power. The STATCOM should also be able to supply harmonic current if needed, as the VSI is used today in active filtering applications.

3.2 Matrix Converter

The matrix converter is an AC/AC converter without an intermediary stage like the AC Chopper. It is able to produce an output voltage with different amplitude and frequency to the input voltage[24]. The converter has several advantages as compared to the AC Chopper and a STATCOM. The matrix converter topology eliminates the need for a capacitor, hence the converter does not contain any storage elements. This improves reliability since an electrolytic capacitor is one of the less reliable components of a power converter. The lack of a storage unit also gives the converter an advantage of increased energy density.

Much of the research done on the matrix converter is directed towards three phase systems, envisioning areas of application such as voltage step-up or step-down for energy transmission, control of electrical machines (induction machine), etc. Nonetheless the matrix converter concept can also be used in a single phase arrangement[24]. Regarding reactive power compensation the matrix converter is not as flexible as the VSI. A characteristic of the control system of the matrix converter is that the amount of available reactive power is dependent on the amount of active power that is supplied e.g. lowering the active

power output of the converter lowers the possible reactive power output[15]. Research on how to improve the reactive power output of the matrix converter is ongoing[16]

3.3   Static VAR Compensator(SVC)

The SVC is an older device which was developed as a result of new possibilities using thyristor technology. It is widely in use today, and is still considered an option to the more modern solutions. An impedance designed to be either inductive or capacitive was connected to the grid by thyristor switches. The RMS voltage over the impedance was regulated by the firing angle of the thyristors. The reactive output was then made controllable as opposed to capacitor banks which only can be coupled to or decoupled from the grid. Because of the low forward voltage drop of the thyristors, this device is expected to have lower operating losses than the transistor based VSIs and the AC chopper [14]. The disadvantage of this technology is the high amount of low order harmonics it produces, leading to the need for relatively large passive filters installed in parallel to the SVC to avoid polluting the grid.
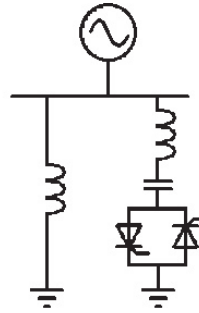
Figure 3.3.1: Layout of a Static VAR Compensator capable of supplying both inductive and capacitive power. The output power is controlled by setting the converter on the right to supply less or more reactive power than supplied by the connected inductor.

3.4   Chapter Conclusion

In this chapter the competing technologies for reactive power compensation have been presented. The three technologies(VSI, matrix converter and SVC) have strengths and weaknesses, but none of them are deemed victorious over the rest. When it comes to harmonic current generation, the VSI is the strongest opponent to the AC Chopper because of it's vast versatility. The matrix converter is still a young technology, so time and research will show if it is a contender alongside the VSI.

Chapter 4

Verification of the Basic Relation

4.1 Background

The first goal of the problem definitions is to check the basic realtion of the AC Chopper, which describes the relation between the input and output signals(Eq. 2.3.1). Tests done during the initial investigation in the fall of 2012 gave results indicating that the basic relation was not valid. Specifically the relation did not hold for tests done in simulation and the results were noted in RMS value. This led to a conflict between the simulation results and the known references for AC Chopper. The known references all support the basic relation found in Eq. 2.3.1, usually accompanied by the text "for RMS values". The new relation that was found in simulation between input and output values is noted in Eq. 4.1.2

$$V_{OUT} = V_{IN} \cdot \sqrt{\alpha} \tag{4.1.1}$$
$$I_{OUT} \cdot \sqrt{\alpha} = I_{IN} \tag{4.1.2}$$

If compared to Eq. 2.3.1 the only difference is that the correlation is the square root of the duty cycle (new relation) between converter input and output. An error in the calculation was ruled out as an explanation for the unexpected result since the method gave the correct result for the grid side voltage.

To investigate this phenomena, a series of simulations were conducted in open loop control. The hypothesis was that the recorded tendency was only a coincidence regarding the choice of system and component parameters. Thus a series of simulations were done where these parameters where isolated and changed. If the relation found earlier was only

per chance then these tests would certainly reveal that fact and the newly found relation could be refuted.

4.2   Component Variation

Simulations where done in PSIM with open loop control for the duty cycle equal to 0.3, 0.5, 0.7 and 0.9. For each experiment the grid and impedance's voltages and current were measured in both RMS and FFT. The following parameters were changed:

Experiment 1 The switching frequency was changed from 1kHz to 2kHz ($f_{sw} = 2000$Hz)

Experiment 2 The switching frequency was changed from 1kHz to 5kHz ($f_{sw} = 5000$Hz)

Experiment 3 The component sizes were set to $L_v = 0.1H$ and $C_v = 18\mu F$

Experiment 4 The grid frequency was changed from $16\frac{2}{3}Hz$ to 50Hz ($f_{net} = 50Hz$)

Experiment 5 The impedance resistance was changed from $1m\Omega$ to 1Ω ($R_v = 1\Omega$)

Experiment 6 The impedance resistance was changed from $1m\Omega$ to 0.5Ω ($R_v = 1\Omega$)

The new postulated relation of Eq. 4.1.2 was tested through these six experiments. The relation for the measured RMS values will be presented first. An apparent duty cycle was calculated based on the measured input and output RMS values. The apparent duty cycle was then subtracted from the expected duty cycle($\sqrt{\text{real duty cycle used in simulation}}$) and the difference was divided by the expected value. The result is the variance from the expected value in percentage. The results are shown in Fig. 4.2.1 and 4.2.2.
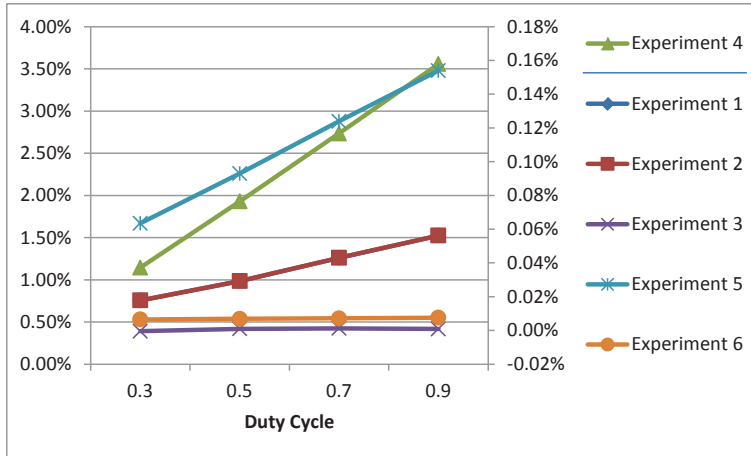
Figure 4.2.1: Variance from the expected relation between the input and output voltages of the converter. Experiment 4 follows the y-axis on the left, the rest follows the y-axis on the right.
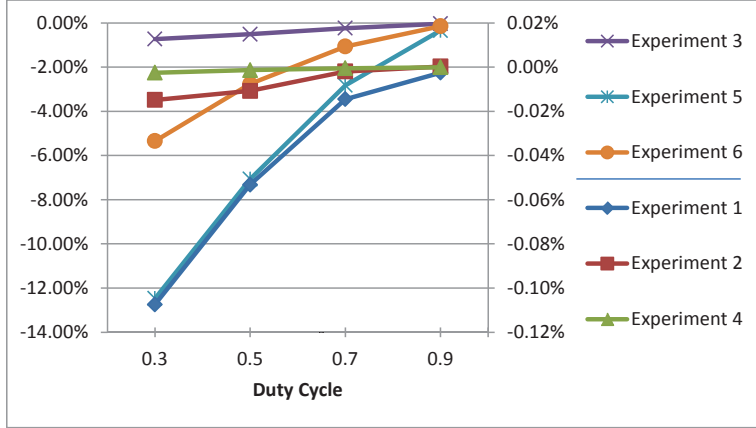
Figure 4.2.2: Variance from the expected relation between the input and output currents of the converter. Experiments 3,5 an 6 follow the y-axis on the left, the rest follows the y-axis on the right.

The results greatly support the new postulated relation, especially for the measured voltages where only experiment 4 differs slightly from the postulated relation. For the current the relation is less clear. The measurements using FFT are not presented in figure form, but is instead summed up in a single sentence: With very little variance the fundamental voltages and currents were found to correlate linearly with the duty cycle(less than 0.5%), i.e. Eq. 2.3.1 was found valid. One measurement supported the new relation while the other measurement refuted it. What was the correct answer? The answer is both. It is the calculation method that changes the result.

The definition of a RMS value is the following:

$$f_{RMS} = \sqrt{\frac{1}{T_2 - T_1} \int_{T_2}^{T_1} [f(t)]^2 dt}$$

If $f(t)$ is set to $a \cdot \sin(\omega t)$ the equation is evaluated to $\frac{a}{sqrt2}$, where a is the amplitude of the sine. But if $f(t)$ is set to a chopped signal then the result becomes:

$$f_{RMS} = \frac{a}{sqrt2} \cdot \sqrt{D} \quad\quad\quad (4.2.1)$$

where a is the amplitude of the sine and D is the duty cycle. The step by step solution is found in App. C. This relation is equal to the one that was measured in PSIM. So Eq. 2.3.1 is valid if the measurements are made in the frequency domain (or if using phasors). To calculate the RMS value then only the 50Hz signal measured by FFT is divided by the square root of two. This is the method that will be used throughout the report.

4.3   Chapter Conclusion

Former simulations revealed a conflict between simulation results and the basic relation found in the literature. The basic relation explains the relation between input and output values. It was therefore decided to perform more simulations to see if the results were valid for different AC Chopper parameter values. In this chapter the experiments and the results have been presented. The results were the same as for the original simulation and the conflict was not resolved.

A solution was found. The answer lied in the way the signal was calculated. Using the definition of the RMS value, the resulting relation between input and output becomes the square root of the duty cycle. If the signals are investigated in frequency domain then the relation from the literature is valid. For the rest of the report FFT will be used as the method of measuring RMS values.

Chapter 5

Open Loop Behavior with Time Varying Duty Cycle

In this chapter the possibilities for the AC Chopper to make harmonics are investigated. The second goal of the problem definition states that the open loop behavior should be mapped. This is done to better understand the behavior of the AC Chopper regarding harmonics. With the new information about open loop behavior, a qualified decision can be made about the best way to perform closed loop control.

The former dq control system will not be used. Instead two methods will be tested in controlling the harmonic output of the AC Chopper. The first method starts out with an already published method regarding harmonics of the AC Chopper[17]. This method is modified to fit the goals of this project. The second method takes a PWM method used for the VSI and applies it to the AC Chopper. The results are then analyzed and commented.

5.1 First Method for Varying the Duty Cycle: Inversing an Existing Method

A conference paper by a research group in China reveals a method for filtering out incoming voltage harmonics using the Step-down AC Chopper[17]. They have shown that the AC Chopper can eliminate incoming voltage harmonics from the grid, so that the output voltage of the converter contains only the fundamental voltage with modulated amplitude and switching noise which can easily be removed by a low-pass filter. An added advantage is the simplicity of the control system. Mathematically they obtain an expression for a duty cycle for which the output contains no low order voltage harmonics present at the grid side.

A suggestion for controlling the AC Chopper according to the goals in this report is to inverse this method. This means taking a harmonic free grid voltage and producing given harmonics on the output side. Before steps are taken to inverse and adapt the system for such a use, the original system is explained and reproduced here.

5.1.1 Eliminating Incoming Harmonics

In the scenario of the paper, the grid voltage is contaminated with harmonics which must not be passed on to voltage harmonic sensitive load. To overcome the challenge, a control system for eliminating the incoming low order harmonics is designed for the AC Chopper. In addition to solving the challenge, an added requirement is that the control system must be simple, i.e. avoid the use of harmonic frequency analyses. The solution consists of measuring two variables: the input voltage with harmonics and the fundamental component of the input current. The latter can be achieved by several known methods, e.g. a SOGI unit. From these two variables the duty cycle is calculated.

The input voltage with its harmonic content is defined as follows:

$$U_{main}(t) = u_1 \cos(\omega_0 t) + \sum_{k=2}^{\infty} v_k \cos(k\omega_0 t + \theta_k) \tag{5.1.1}$$

The duty cycle, $f_m(t)$ is defined as a sum of a static part D, and a variable part defined by the time-varying function $f_e(t)$.

$$f_m(t) = D + f_e(t) \tag{5.1.2}$$

The output voltage from the AC Chopper is defined as earlier with the basic relation of Eq. 2.3.1 and the input voltage is swapped for Eq. 5.1.1 above.

$$U_{out}(t) = f_m(t) \cdot U_{main} = D \cdot u_1 \cos(\omega_0 t) \tag{5.1.3}$$

were the left part of the equation is the desired output voltage containing only the fundamental voltage. If the two latter parts in Eq. 5.1.3 are rearranged using Eq. 5.1.1 and 5.1.2, the expression for the time varying duty cycle is found to be:

$$
\begin{aligned}
f_e(t) &= \frac{-D \cdot \sum_{k=2}^{\infty} v_k \cos(k\omega_0 t + \theta_k)}{U_{main}(t)} \\
&= \frac{-D \cdot [U_{main}(t) - v_1 \cos(\omega_0 t)]}{U_{main}(t)}
\end{aligned} \tag{5.1.4}
$$

A simulation was done to reproduce and validate the method. The simulation was done using Matlab Simulink. The input voltage with a 50Hz fundamental and 3rd, 5th and 7th
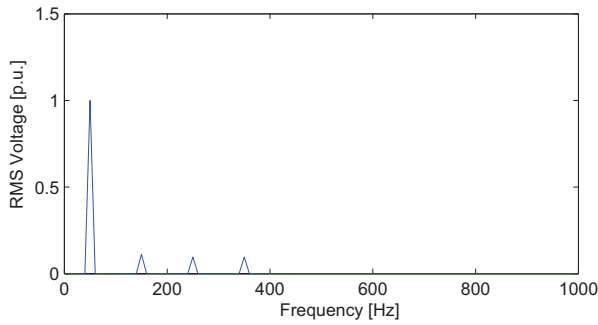
Figure 5.1.1: FFT of the input voltage to the AC Chopper for the harmonic filtering experiment containing harmonics of 3rd, 5th and 7th order.
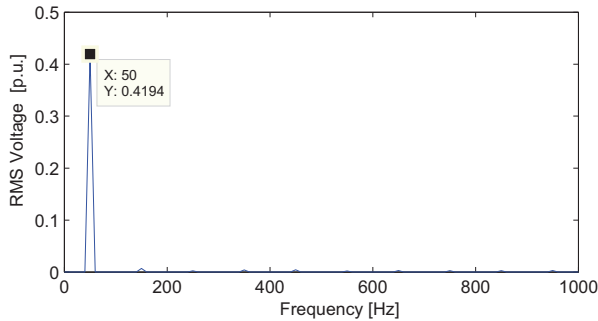
Figure 5.1.2: The output voltage of the AC Chopper for the harmonic filtering experiment where the harmonics have been filtered out.

harmonics are seen in Fig. 5.1.1. The nominal voltage is 311V. The value voltage peak of the three harmonics is 35, 30 and 30V respectfully. They are also phase shifted compared to the fundamental. The info regarding the fundamental component of the input voltage is feed directly to the controller and is perfect so there is no possibility for error. The static duty cycle was set to 0.42.

Figure 5.1.2 show the output voltage over the load, showing almost no trace of the former harmonics and the fundamental component. At the same time the fundamental is at the set point of the static duty cycle.

Figure 5.1.3 and 5.1.4 show the chopped voltage over the sensitive load and the calculated duty cycle. The duty cycle contains several harmonics and a non-linearity. The non-linearity originates from the way of calculating the duty cycle. U_{main} is sinusoidal in the denominator of the duty cycle calculation. When it approaches zero, large jumps as seen in Fig. 5.1.4 will occur.

The method found in literature appears to work as designed. The next step is to transform

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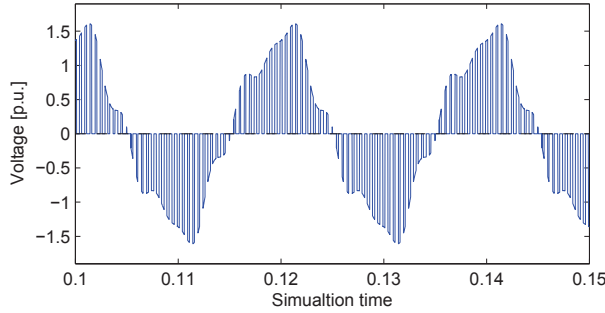
Figure 5.1.3: Realtime chopped voltage as seen by the load for the harmonic filtering experiment. The input voltage is clearly not the shape of a single sine.
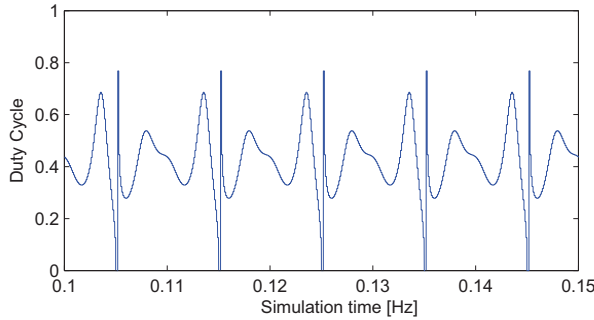
Figure 5.1.4: Realtime duty cycle to filter out the incoming harmonics for the harmonic filtering experiment.

the method to produce harmonics.

5.1.2 Making Harmonics

To turn the conecpt around from eliminating harmonics to making harmonics, the same mathematical reasoning was done. The only difference is that the desired output wass changed to contain harmonics.

The grid voltage is defined as previously given in Eq. 5.1.1, but for this scenario there are no input harmonics. The desired output voltage is set to

$$U_{out}(t) = D \cdot \hat{U} \sin(\omega_{net}t) + E \cdot \hat{U} \sin(n \cdot \omega_{net}t + \varphi) \qquad (5.1.5)$$

where n denotes the harmonic order.. The desired output contains a sine of the fundamental frequency with amplitude D and a harmonic voltage of the n'th order of amplitude E.

The desired output is set equal to the basic relation for the converter as in Eq. 5.1.3:

$$U_{out}(t) = f_m(t) \cdot U_{in} = [D + f_e(t)] \cdot \hat{U} \sin(\omega_{net} t)$$
$$= D \cdot \hat{U} \sin(\omega_{net} t) + E \cdot \hat{U} \sin(n \cdot \omega_{net} t + \varphi) \qquad (5.1.6)$$

Eq. 5.1.6 is then rearranged to express the time varying part of the duty cycle, $f_e(t)$:

$$f_e(t) = E \cdot \frac{\sin(n \cdot \omega_{net} t)}{\sin(\omega_{net} t)} \qquad (5.1.7)$$

To see whether the method works or not, several simulations were done in Matlab Simunlink. In each simulation a specific parameter of the duty cycle was isolated and varied (amplitude, frequency or phase shift). The static duty cycle was kept constant at $D = 0.5$. The input was a perfect sine of 50Hz and RMS value of 1.0. The results are shown in the following subsections.

Results of Varying the Harmonic Order, n

The simulation was run with n equal to 3, 5, 7 and 9. The resulting output voltage can be seen in Fig. 5.1.5 in the form of peaks in a frequency spectrum. The method is clearly able to make a harmonic at the selected frequency. But it is also clear that the method produced harmonics in both side bands of the desired frequency. Other smaller harmonics are also identified. For most of the cases the fundamental component stays constant at the set point of 0.5.

(a) $n = 3, f_{desiredharmonic} = 150Hz$

(b) $n = 5, f_{desiredharmonic} = 250Hz$

(c) $n = 7, f_{desiredharmonic} = 350Hz$

(d) $n = 9, f_{desiredharmonic} = 450Hz$
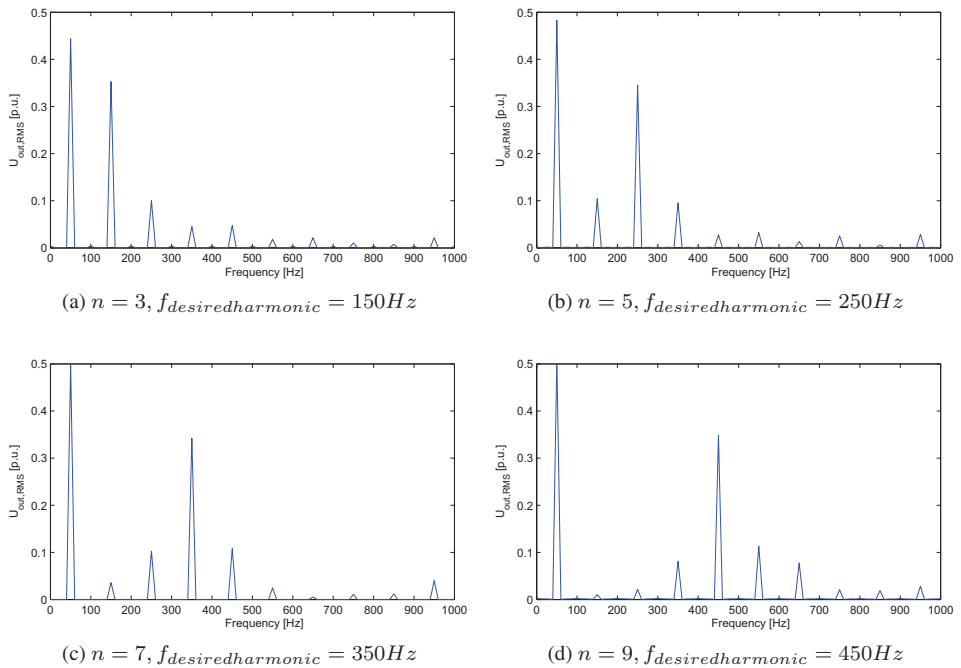
Figure 5.1.5: Frequency spectrum of the output voltage of the AC Chopper implemented with the inversed method for making harmonics. The frequency of the desired harmonic is varied.

Results of Varying the Amplitude, E

The simulation was run with E equal to 0.3, 0.5, 0.7 and 1.5. The frequency was set to 250Hz (5th harmonic). The resulting output voltage can be seen in Fig. 5.1.6 again in the frequency spectrum. For Fig. 5.1.6a the voltage peak of the desired peak seem to be of approximately same value as the set point (E = 0.3). For Fig. 5.1.6b, 5.1.6c and 5.1.6d the peak seems to increase each time, but the increase saturates for higher values of E. The sidebands seem to follow the trend, increasing in magnitude with increasing E. Other harmonics are also present elsewhere in the spectrum for all of the cases.

(a) $E = 0.3$

(b) $E = 0.5$

(c) $E = 0.7$

(d) $E = 1.5$
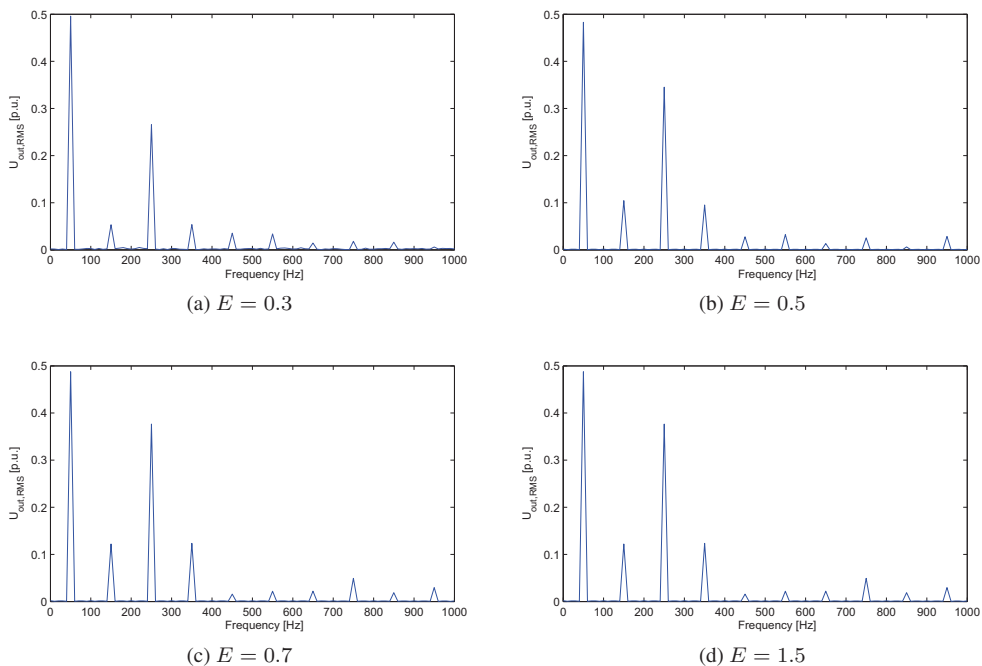
Figure 5.1.6: Frequency spectrum of the output voltage of the AC Chopper implemented with the inversed method for making harmonics. The amplitude of the desired harmonic is varied.

Results of Varying the Phase Shift, φ

The simulation was run with φ equal to 0.0, $\frac{\pi}{2}$, π and $\frac{3\pi}{2}$(0, 90°, 180° and 270°). The frequency was set to 250Hz (5th harmonic) and the amplitude was set to $E = 0.5$. The resulting output voltage can be seen in Fig. 5.1.7 in a rose plot, where the magnitude is the length of the vector and the phase shift is shown in degrees along the border of the circle. The fundamental voltage(in blue) follows the grid voltage and serves as a reference. The harmonic sidebands of the desired harmonic are almost 180° shifted from the desired harmonic.

From Fig. 5.1.7a it is seen that the desired harmonic has a less than 30° negative phase shift from the grid voltage. The other simulations show that the phase can be controlled. But the phase shift is not completely coherent with the set phase shift, φ. In Fig. 5.1.7b the phase shift seems to be larger than 90°, and in Fig. 5.1.7d the phase shift seems to be less than 270°. This could be small errors due to the FFT method, or it may also be a result of the implemented method for producing the duty cycle. This issue has not been addressed as the general tendencies are clear enough to conclude on the method's performance.

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(a) $\varphi = 0°$

(b) $\varphi = 90°$
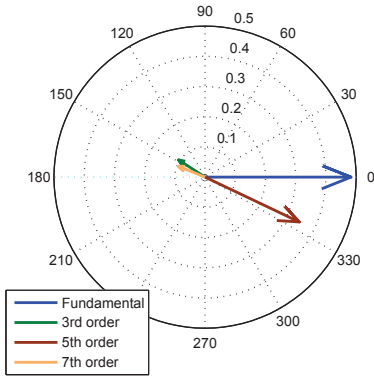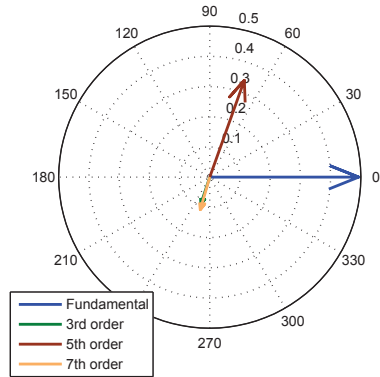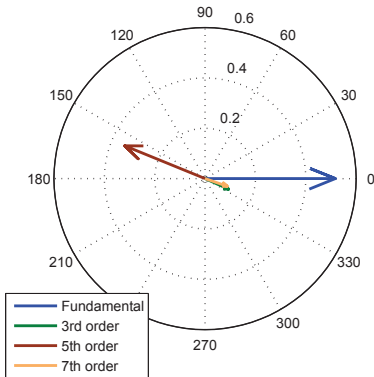
(c) $\varphi = 180°$
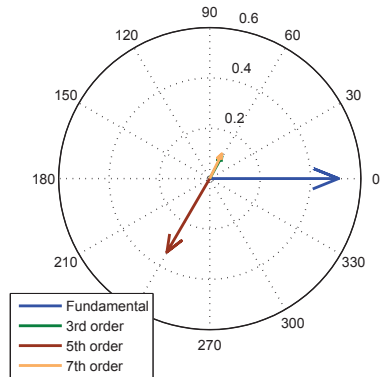
(d) $\varphi = 270°$

Figure 5.1.7: Phasor representation of the output voltages of the AC Chopper implemented with the inversed method for making harmonics. The phase shift of the desired harmonic is varied.

5.2 Second Method for Varying the Duty Cycle: Sinusoidal Duty Cycle

In the former section, harmonics were produced by inversing a method for harmonics elimination to produce harmonics. In the present section, the starting point will be on controlling the duty cycle directly. The goal is to identify the exact converter output when single frequencies are injected in the form of a duty cycle. The matter is investigated by looking at the basic equations found in Section 2. The relation is developed mathematically to see the result of injected sinusoidal duty cycle signals.
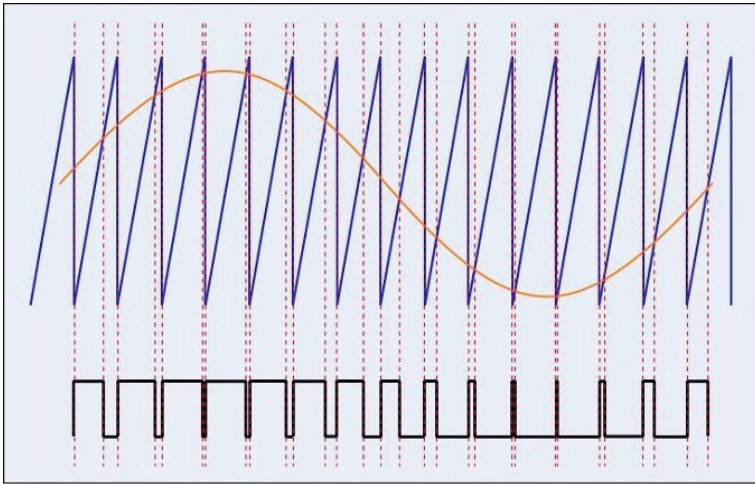
Figure 5.2.1: PWM modulation with a sinusoidal duty cycle. Image is taken from: http://maxembedded.files.wordpress.com .

The modulation is done in the same way as for inverters using VSI topology. A saw tooth or triangle wave is compared to a duty cycle, resulting in a PWM signal which turns a switching cell on or off. The concept is shown in Fig. 5.2.1. If the duty cycle is sinusoidal then the integral of the PWM signal will also be a sinusoidal, and so a sinusoidal output from the converter is produced.

5.2.1 Developing the Mathematical Expression

Before developing the mathematical expression for the output voltage, two definitions are presented. The grid voltage is defined as follows:

$$U_{in} = \hat{U} \sin(\omega_{net} t) \tag{5.2.1}$$

The grid voltage is used as a reference phasor, and so it has no phase shift ($\varphi = 0$). The duty cycle is defined as follows:

$$D = C_D \sin(\omega_D t + \varphi_D) + D_{static} \qquad (5.2.2)$$

where C_D is the amplitude, $\omega_D = 2\pi f_D$ is the angle speed and φ_D is the phase shift. The duty cycle consists of two parts. The first part is the static part which in not time dependent. The second part is sinusoidal and constitutes the part for which harmonics will be produced. The full expression for the duty cycle can be said to constitute of a sine wave and its bias. This is shown conceptually in Fig. 5.2.2a.
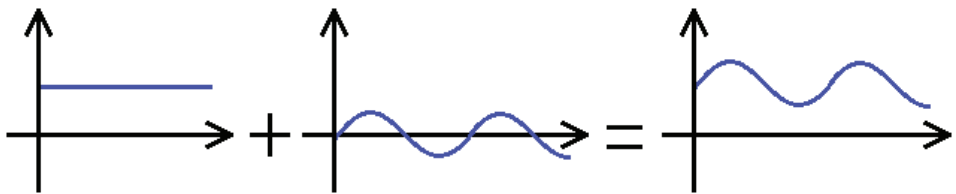
(a) The duty cycle is a superposition of two or more parts: the static part(bias) and the sinusoidal part. Several sines could be included in the signal (not depicted).
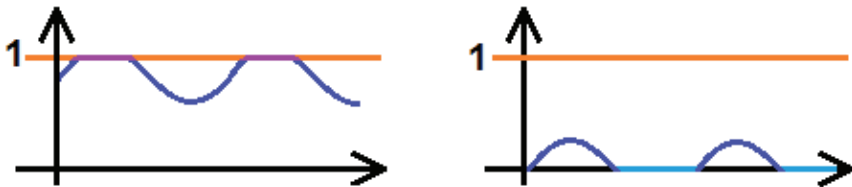
(b) Possible problems regarding the duty cycle. If sum of the static and the varying part of the duty cycle does not stay within the duty cycle limits of $[0, 1]$ then non-linearities will occur.

Figure 5.2.2: Concepts regarding the sinusoidal duty cycle when controlling the AC Chopper.

There is one consideration to take when making such a duty cycle. The sum of the different super imposed parts must still be within the limit of [0,1]. If not then the duty cycle signal will be saturated and non-linearities will occur. Two such scenarios are shown in Fig. 5.2.2. Here a lack of a static part or a large static part results in the sinusoidal part of the signal being saturated. If thinking in terms of Fourier Transform, this will result in adding harmonics of higher order. Therefore special attention must be made to stay within the duty cycle limits.

The mathematical expression of the output voltage of the AC Chopper is found by using the two definitions to developing the basic relation between input and output voltage of the converter, Eq. 2.3.1.

$$
\begin{aligned}
U_{out} &= U_{in}D \\
&= \hat{U}\sin(\omega_{net}t) \cdot [C_D\sin(\omega_D t + \varphi) + D_{static}] \\
&= \hat{U}\sin(\omega_{net}t) \cdot C_D\sin(\omega_D t + \varphi) + D_{static}\cdot\hat{U}\sin(\omega_{net}t) \\
&= \frac{\hat{U}\cdot C_D}{2}\left\{\cos[(\omega_{net}-\omega_D)t - \varphi] + \cos[(\omega_{net}+\omega_D)t + \varphi]\right\} \qquad (5.2.3) \\
&\quad + D_{static}\cdot\hat{U}\sin(\omega_{net}t)
\end{aligned}
$$

Equation 5.2.3 show that for a sinusoidal duty cycle (single frequency) then there will be produced two super imposed sinusoidal output voltages. The multiplication of two sines can be rewritten as the sum of two cosines. The angle speed of the two cosines will be the sum and the subtraction of the angle speeds of the two sines. If $\omega_{net}\neq\omega_D$ then the angle speed of each of the two cosines will be negative and positive, respectfully. Compared to the grid phasor, the two resulting voltages should be 90^0 shifted where each cosine is shifted in opposite directions due to the sign of the angle speed. Thus for any sinusoidal frequency duty cycle introduced to the AC Chopper, the harmonic order of the resulting voltages that will appear at the output will be of one order lower and on order higher compared to the original introduced duty cycle signal. As for the non-sinusoidal part of the duty cycle, designated D_{static}, Eq. 5.2.3 shows that the fundamental voltage stays unaffected by the sinusoidal part.

5.2.2 Simulation of Sinusoidal Duty Cycle and Frequency Response

In this section, results from simulation are presented. In the simulations different parameters of the duty cycle have been isolated and varied with the intention of showing the trends that confirm the mathematic expression found in the former subsection.

A setup was made in Matlab Simulink to investigate the open loop behavior. The model contains the AC Chopper circuit, modeled in PLECS. Further the switching system has been implemented as shown in App. A. The component and phasor values are given in p.u. as shown in Table 2.6.1. The simulations have been done in the time domain while a sampling unit stores values for FFT processing afterwards. The resulting output voltage will therefore be presented in frequency domain.

The different parameters to be varied are the angle speed of the sine signal, ω_D, the amplitude of the sine, C_D, the phase shift of the sine signal, φ, and the bias, D_{static}. The input voltage stays constant with a RMS value of 1.0 and frequency of 50Hz.

Results of Varying the Angle Speed of the Sine Signal, ω_D

For this experiment the frequency f_D was set to 200, 400, 500 and 600Hz. The duty cycle was set in the following way:

(a) $f_D = 4 \cdot f_{grid} = 200Hz$

(b) $f_D = 8 \cdot f_{grid} = 400Hz$

(c) $f_D = 10 \cdot f_{grid} = 500Hz$

(d) $f_D = 12 \cdot f_{grid} = 600Hz$
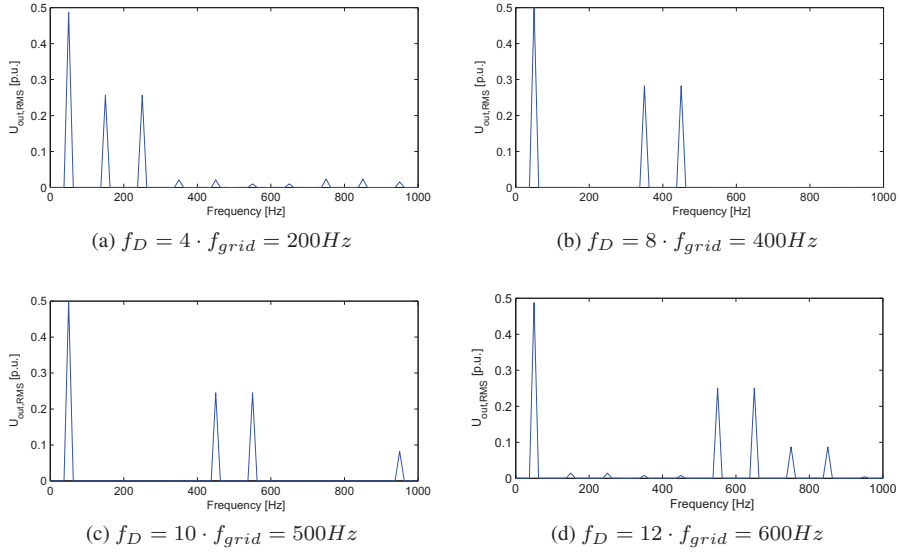
Figure 5.2.3: Output voltage of the AC Chopper for sinusoidal varying duty cycle where the frequency of the sine is varied.

$$D = 0.5 + 0.5 \cdot \sin(2 \cdot \pi \cdot f_D \cdot t + 0)$$

The results are shown in Fig. 5.2.3. The relation shown in Eq. 5.2.3, where a single sine in the duty cycle results in two voltage peaks of one order higher and one order lower than the duty cycle harmonic, e.g. Fig. 5.2.3a shows an output voltage at 150Hz and 250Hz for an input of 200Hz. The amplitude of the voltage seems uncorrelated to the part of the spectrum where the voltage harmonic is produced. The static duty cycle of 0.5 is seen at the 50Hz band, and this peak also seems mostly unaffected by the harmonic.

For Fig. 5.2.3c and Fig. 5.2.3d another set of peaks appears at the high end of the spectrum. The two extra peaks seem to have a lower frequency as the duty cycle frequency increases. These peaks could be an interaction with the switching speed or be a result of the FFT processing.

Results of Varying the Amplitude of the Sine Signal, C_D

For this experiment the amplitude C_D was set to 0.3, 0.5, 0.7 and 1.0. The duty cycle was set in the following way:

$$D = 0.5 + C_D \cdot \sin(2 \cdot \pi \cdot 300 \cdot t + 0)$$

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(a) $C_D = 0.3$

(b) $C_D = 0.5$

(c) $C_D = 0.7$

(d) $C_D = 1.0$
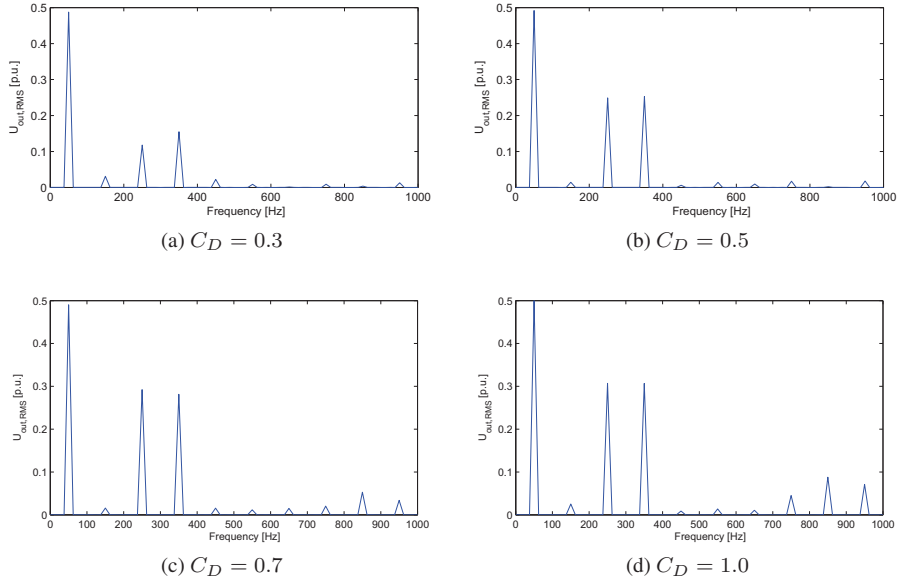
Figure 5.2.4: Output voltage of the AC Chopper for sinusoidal varying duty cycle where the amplitude of the sine was varied.

The results are shown in Fig. 5.2.4. This figures clearly shows the amplitude of the harmonics change with varying amplitude. The value seems to rise quickly(Fig. 5.2.4a and Fig. 5.2.4b), while for higher amplitudes the harmonic voltages seem to increase slightly at the cost of the introduction of higher order harmonics. This is in compliance with what was described and depicted in Fig. 5.2.2b regarding the duty cycle limitations. When the duty cycle saturates then higher order harmonics are produced.

The voltage values in Fig. 5.2.4a and Fig. 5.2.4b are approximately as expected according to Eq. 5.2.3. But for higher duty cycles the relation does not longer hold. This can be explained conceptually.

If using a VSI to produce a sinusoidal signal (either fundamental or harmonic), the limit of the amplitude of the produced signal is set by the DC bus voltage. The full voltage becomes the highest peak of the sinusoidal output voltage, and the RMS value becomes $\frac{1}{\sqrt{2}}$ of the DC bus voltage. What happens if the DC bus voltage varies sinusoidally?

In Fig. 5.2.5 a fundamental sine wave is shown in blue(with a mirror image) with amplitude equal to 1. If a harmonic sine wave of higher order is to be produced with this fundamental as input voltage, it might look something like the sine wave seen in green. Following the VSI concept of making a sine wave, the available bus voltage at any time is given by the fundamental in blue. It is seen that the possible amplitude of the harmonic varies with a frequency equal to the fundamental. If a DC bus voltage to make the har-

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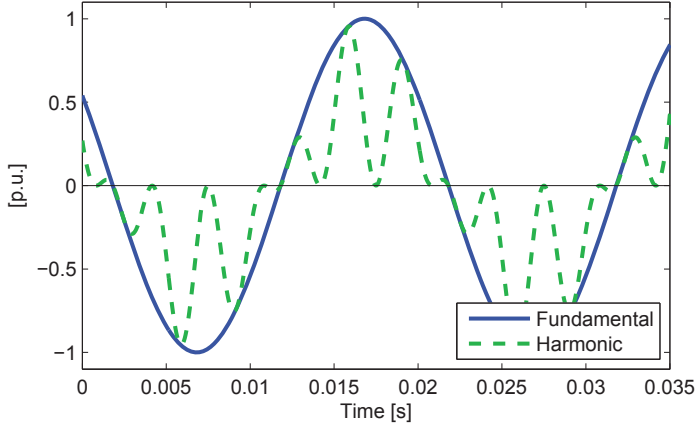
Figure 5.2.5: Concept regarding the physical limits of making harmonics with the AC Chopper.

monic was to be decided, a good approximation for the AC Chopper would be a virtual DC bus with the RMS value of the input voltage.

$$\hat{U}_{harmonic} = \frac{\hat{U}_{fundamental}}{\sqrt{2}} \tag{5.2.4}$$

and that the RMS value of the harmonic would be

$$U_{harmonic,RMS} = \frac{\hat{U}_{harmonic}}{\sqrt{2}} = \frac{\hat{U}_{fundamental,RMS}}{2} \tag{5.2.5}$$

in which the latter expression is similar to that of Eq. 5.2.3.

One could be quick to conclude that a higher static duty cycle gives a higher possible amplitude for the harmonics. But the phenomena regarding duty cycle saturation explained in Fig. 5.2.2b must still be respected. So an increasing D_{static} results in a smaller amplitude C_D in the relation $C_{D,max} = 1 - D_{static}$. However C_D is limited to a maximal value of 0.5 to remain within the duty cycle limit of [0,1](to avoid duty cycle saturation).

Thus, with the concept of the available bus voltage and known limits of the duty cycle, the maximum amplitude of harmonic voltages can be derived:

$$\begin{aligned}
\text{Max Amplitude of Harmonics} &= \text{Available fundamental} \cdot C_D \\
&= \hat{U}_{IN} \cdot D_{static} \cdot (1 - D_{static}) \\
&= \hat{U}_{IN}(D_{static} - D_{static}^2)
\end{aligned} \tag{5.2.6}$$

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which has it's maximum in $D_{static} = 0.5$. This consequently sets the operating point $C_D = 0.5$ for which the amplitude of the harmonics are the largest at one quarter of the input voltage.

Results of Varying the Bias of the Sine Signal, D_{static}

For this experiment the static duty cycle D_{static} was set to 0.0, 0.25, 0.5 and 1.0. The duty cycle was set in the following way:

$$D = D_{static} + 0.5 \cdot \sin(2 \cdot \pi \cdot 300 \cdot t + 0)$$

The results are shown in Fig. 5.2.6. Several interesting results are found in this experiment that confirm the former discussion regarding the duty cycle limitations.

Firstly, Fig. 5.2.6a shows that any harmonic cannot be made without the presence of a fundamental voltage. This is in compliance with formerly presented ideas in Fig. 5.2.2b regarding saturated duty cycles and in Fig. 5.2.5 regarding available bus voltage to produce an harmonic.

Secondly, the only case where there are almost no recognizable harmonics (expect the ones that are intentionally produced), is in Fig. 5.2.6c. This is due to the duty cycle not being saturated, as it is in all the other cases.

Lastly, as the static duty cycle increases above 0.5 the amplitude of the 5th and the 7th harmonic decreases in amplitude. This is in line with the argumentation in the former subsection, where the amplitude of the harmonic would be its maximum for $D_{static} = 0.5$ and $C_D = 0.5$.

(a) $D = 0.0$

(b) $D = 0.25$

(c) $D = 0.5$

(d) $D = 0.7$

(e) $D = 1.0$
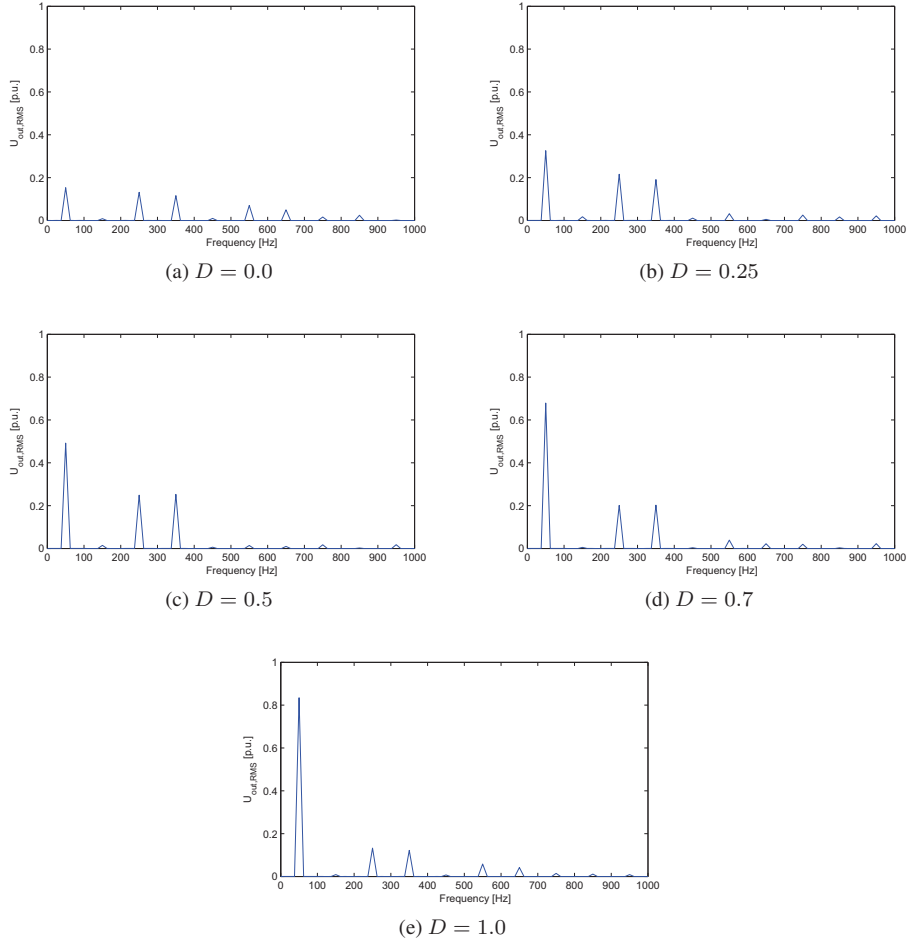
Figure 5.2.6: Output voltage of the AC Chopper for sinusoidal varying duty cycle where the static duty cycle of the sine is varied.

Results of Varying the Phase Shift of the Sine Signal, φ

For this experiment the phase shift φ was set to 0.0, $\frac{\pi}{2}$, π and $\frac{3\pi}{2}$ (0, 90°, 180° and 270°). The duty cycle was set in the following way:

$$D = 0.5 + 0.5 \cdot \sin(2 \cdot \pi \cdot 300 \cdot t + \varphi)$$

The results are shown in Fig. 5.2.7. This figure shows the phase shift of the 5th (250Hz) and the 7th (350Hz) order harmonics as related to the grid voltage. Fig. 5.2.7a show

a negative phase shift of 90°for the 7th order harmonic. This as expected for a cosine related to a sine. The 5th order on the other hand has a positive phase shift of 90°due to its negative angle speed. This is as expected from the discussion in Sec. 5.2.1.The other figures show that the phasors can be controlled to any phase shift that is desired.

(a) $\varphi = 0°$

(b) $\varphi = 90°$

(c) $\varphi = 180°$

(d) $\varphi = 270°$
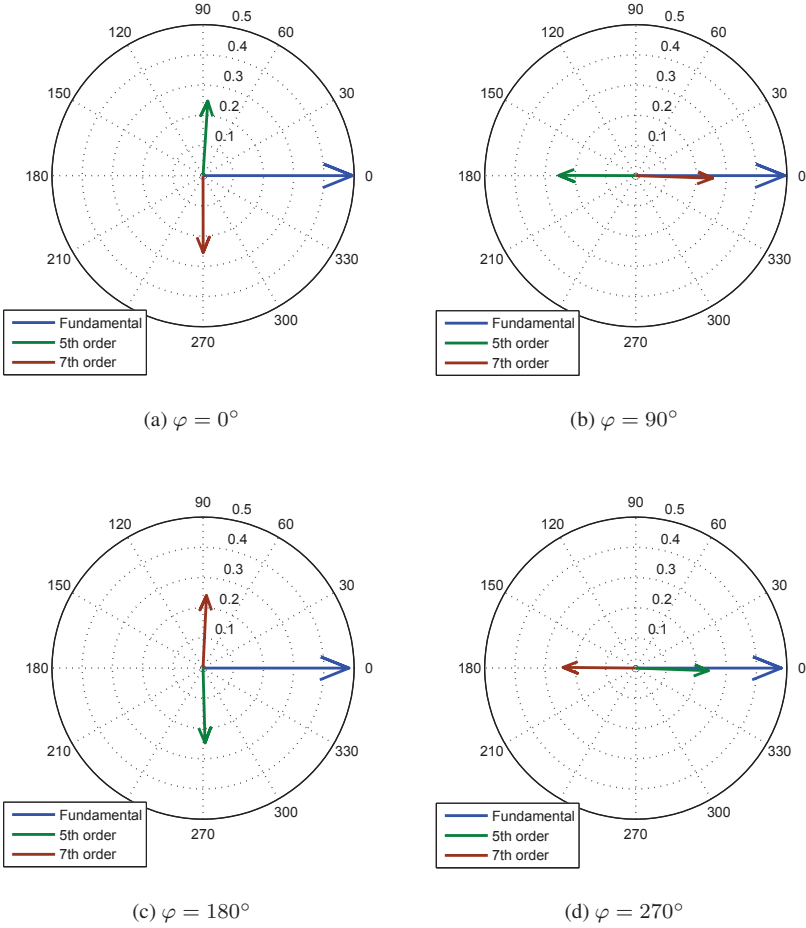
Figure 5.2.7: Output voltage of the AC Chopper for sinusoidal varying duty cycle where the frequency of the phase shift is varied.

5.2.3 Frequency Response of Impedance and Resulting Current

The results shown until now have only concerned the output voltage. This was purposely done because the voltage is less dependent on system values (except the input voltage). The current depends much on the impedance of the AC Chopper. Even if the current would be presented in p.u. the chosen resonance frequency of the device impedance would make a difference in the results. Thus less focus was put on presenting current results.

The dimensioning of the impedance for the 50Hz current is described in App. B. But this method does not take into consideration the frequency response of the higher order currents. It is up to the designer to chose a current profile that suits the needs for higher order harmonics. A methodology for such a design process is not covered in this report. However the frequency response for the circuit in question will be presented here, in form of a Bode plot.

Transforming $u = Ri + L\frac{di}{dt} + \frac{1}{C}\int i \qquad dt$ to LaPlacian space:

$$U = RI + sL + \frac{1}{sC}$$

and rearranging to obtain the relation between current and voltage:

$$\frac{I}{U} = \frac{1}{sL + R + \frac{1}{sC}} = \frac{\frac{s}{L}}{s^2 + s\frac{R}{L} + \frac{1}{LC}}$$
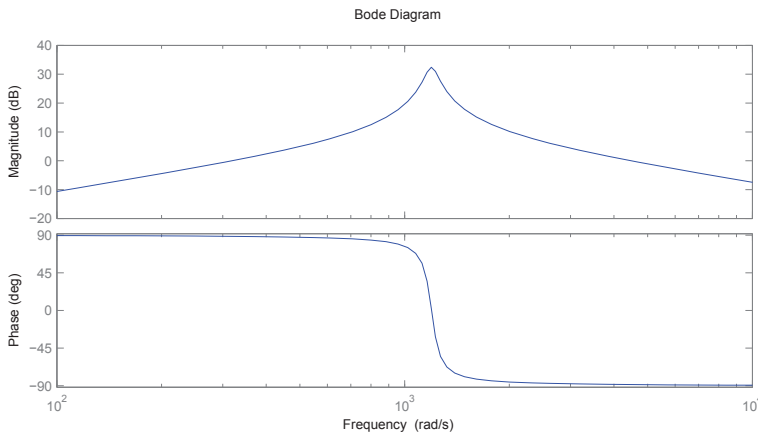
Figure 5.2.8: Bode plot for the impedance current for the simulations done using Matlab Simulink. Values are shown in p.u.

The bode diagram shown in Figure 5.2.8 is plotted using the component values in p.u. The resonance frequency is located at approximately 1190 rad/s (189.4Hz) which is close to the design goal as seen in Table 2.6.1.

5.2.4 Superposition of Multiple Sines to Produce Single Harmonics

The results of open loop testing shown in previous sections demonstrate that induced harmonics always comes in pairs when injecting sinusoidal duty cycles. As explained in Sec. 2.5 the goal is to operate the AC Chopper as a programmable current source, and so the control system must be able to control individual harmonics separately. The task now is to find a method for producing and controlling single current peaks.

The suggestion was to superimpose several sines and use this signal as duty cycle. The goal was to have sum of the sines that gave a single current peak. This could be achieved by having higher order sines to negate the harmonic of the lower order. The result would not be a single sine, but rather shifting two peaks from each other in the frequency domain.

FIRST SINE

Then sines could be injected into AC Chopper one after another. Following the first sine, each sine would negates the higher harmonic of the previous sine and add an even higher order harmonic. The thought is that a number of sines would be added until the highest non-negated harmonic would be in the far end of the frequency spectrum. The high order voltage harmonic would produce a negligable current (due to the frequency response of the impedance) or the harmonic would be in the bandwidth which is damped by the input filter.
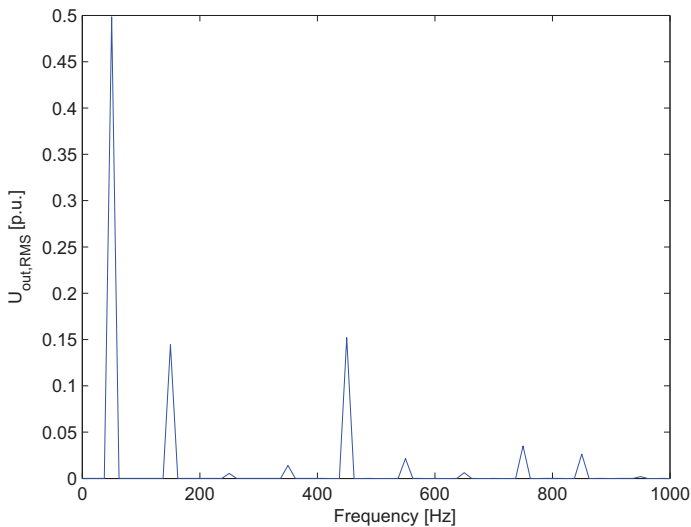
Figure 5.2.9: The frequency spectrum for the output voltage with a static duty cycle of 0.5 and $C_D = 0.3$. A superposition was made of multiple sines to move the second peak to higher frequency.

By replacing the single sine signal in the duty cycle by a multiple of sines, a single low order harmonic voltage can be produced.

$$D = \sum_{k=1}^{N} C_{D,k} \sin(\omega_{d,k} t + \varphi) + D_{static} \tag{5.2.7}$$

Results in Fig. 5.2.7 show that the two harmonics from one duty cycle frequency are shifted 180°from each other, so injected sines should have the same phase shift and a frequency of two orders higher. If we want to produce an harmonic with frequency ω and phase shift φ, then the injected duty cycle must be

$$D = \sum_{k=1}^{N} C_{D,k} \sin\{[\omega + (2 * k - 1)\omega_{net}]t + \varphi\} + D_{static} \tag{5.2.8}$$

where N denotes the number of sines to inject. In Fig. 5.2.9 sines with a frequency of 200, 300 and 400Hz have been injected. They all have the same phase shift and amplitude.
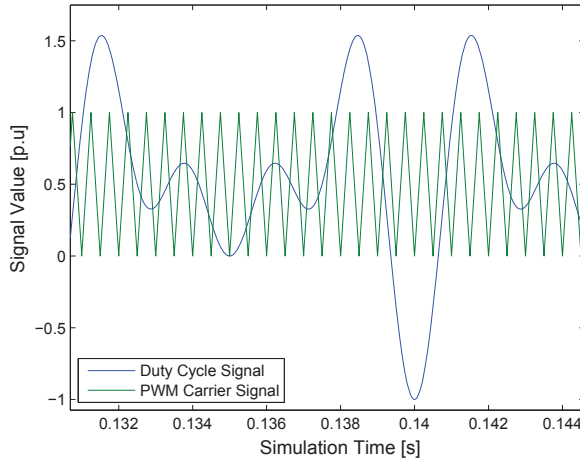
Figure 5.2.10: Realtime duty cycle and carrier signal for the superposition simulation. The duty cycle goes far outside the limit of [0,1].

Fig. 5.2.9 shows two clear voltage peaks six orders apart (150 and 450Hz). Thus the pair has been split up and the higher order peak is shifted to the right in the frequency spectrum. At the same time there exists several non-intended harmonics in the spectrum. Again the limitation related to saturation of the duty cycle is encountered. Fig. 5.2.10 shows a real time sample of the duty cycle and the triangle square. The duty cycle passes the limits of [0,1], and the voltage output does not become a correct projection of the duty cycle.

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Resulting Current when Superimposing Multiple Sines

Since the first voltage harmonic of the above experiment is close to the resonance frequency of the impedance, a new experiment was done. In this experiment the impedance current and the injected grid current was investigated. The duty cycle was set to $D_{static} = 0.5, C_D = 0.3$ with two sines with frequencies of 300 and 400Hz.
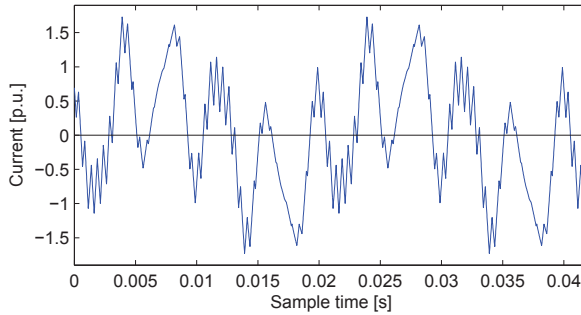
Figure 5.2.11: The realtime impedance current for the experiment with a variable duty cycle of multiple frequencies.
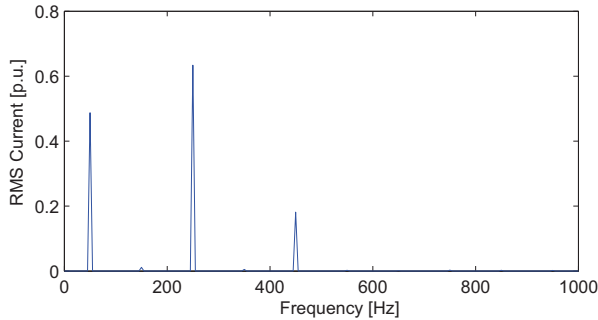
Figure 5.2.12: Frequency spectrum of the impedance current for the experiment with a variable duty cycle of multiple frequencies.

In Fig. 5.2.11 several frequencies can be identified. It is important to note that the maximum and minimum impedance current passes $\sqrt{2}$ and so the current passes its nominal value. Thus the impedance must be dimensioned for a current larger than the nominal value (maximum 50Hz current in stable state).

In Fig. 5.2.12 the current has three clear peaks at the expected frequencies. The large amplitude of the 250Hz current is due to the frequency response of the impedance as shown in the Bode plot in Fig. 5.2.8. The control system appears to work well. Even though the impedance voltage contains more harmonics than wanted the resulting current in the impedance shown in Fig. 5.2.12 is close to the desired input. The duty cycle

was modulated to make currents with frequencies of 50, 250 and 450Hz. The resulting impedance current contains exactly those currents. This could be seen as a sign that the control system is working and has potential to control the AC Chopper harmonics.
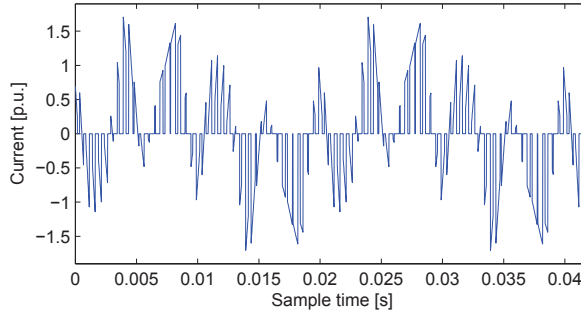
Figure 5.2.13: The realtime grid current for the experiment with a variable duty cycle of multiple frequencies.
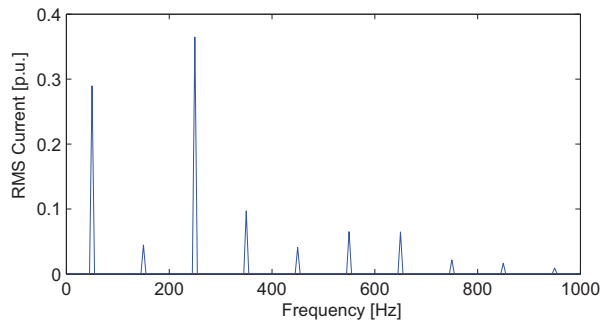
Figure 5.2.14: Frequency spectrum of injected grid current for the experiment with a variable duty cycle of multiple frequencies.

The chopped grid current is shown in Fig. 5.2.13 and the current in the frequency domain is shown in Fig. 5.2.14. The grid current reveals that the superimposing of sines is far from a good solution if the goal is to control the injected grid current. The frequency spectrum of the grid current contain more harmonics than intended, where some harmonics appear at low orders. Such harmonics which occur at lower orders are unwanted and impossible to filter out. The input filter was installed to filter out harmonics due to switching phenomena. These harmonics are found at high frequencies. If the input filter bandwidth was designed to include these low frequencies where the harmonics are occurring, the filter would also filter out the desired harmonics as well. Hence the method of superimposing sines to produce single harmonics is not a suitable control method.

5.3 Chapter Conclusion

In this chapter, the open loop behavior of the AC Chopper when using time varying duty cycles has been investigated. The first part presented a method for eliminating input harmonics found in the literature. The experiment has has successfully been reproduced in simulation. The simulation showed the effectiveness of the method. The next step was to inverse the method to make output harmonics instead.

The method was inversed and tested in simulation to document it's performance. Results shown in Fig. 5.1.5 show that the method is capable of making the an output voltage harmonic at the intended frequency. Additionally, the results show that the method also produces many other unintended harmonics, particularly in the sidebands of the intended harmonic. Other results show that the amplitude and the phase shift of the intended harmonic can be controlled, but the performance is very poor. The harmonic content was far too large for this method to be used to control the AC Chopper for active filtering. This method was therefore abandoned.

The second part focused on mapping of the open loop behavior by injecting a sinusoidally varying duty cycle. A mathematical expression was developed for the converter output voltage. Simulations were performed that confirm the mathematical expression. Individual parameters of the mathematical expression have been varied to identify trends. Limits and challenges were identified and explained through conceptual figures.

The mathematical investigation and the open loop testing show that the basic relation for the AC Chopper is also valid for harmonics. The model shows that a single frequency entering the control system of the AC Chopperwill result in two voltages on the converter output. Any intention to produce one single output harmonic will have to deal with this characteristic of the AC Chopper. Taking this characteristic into consideration the AC Chopper was manipulated using several superimposed sines in an attempt to produce a single current harmonic. The tests show that this system works for the impedance current. Unfortunately the injected grid current contains too many unintended low order harmonics. As such, controlling the AC Chopper as a current source for single currents seems far from possible.

The only remaining solution for the AC Chopper is to inject harmonics in pairs, e.g. trying to eliminate a 3rd harmonic current while also injecting a 5th order current uncontrolled. This 5th may partially eliminate an existing 5th harmonic present from the non-linear load or it may also be partially in phase and thus increase the amplitude.

Chapter 6

Closed Loop Control of Fundamental Current

One of the project goals was to implement a closed loop control for the 50 Hz impedance current. This goal was a continuation of the work that was started with the preliminary investigation. During this investigation a current control based on PI controllers in a dq-refrence frame was tried implemented. A control system was designed, however testing showed that it was set point dependent. Meaning one set point could give almost perfect steady state results while other set points would result in a standing 100Hz ripple on the output current. The conclusion was that the control system did not perform well due to using two control variables(d and q) to control one degree of freedom (amplitude).

A new approach was needed. The fundamental current in the impedance has only one degree of freedom, the amplitude. The two other characteristics of the impedance current, frequency and phase shift, are given. The current frequency is the same as the grid frequency and the phase shift is given by the device impedance. Therefore the new control system should only control the amplitude. The decision was made to use the RMS value of the current and implement a classic control scheme with PI or higher order controllers.

6.1 Choice and Implementation of a SOGI Unit

To implement a control system based on the RMS value of the current, a system for calculating the RMS value was needed. The definition of the RMS value is the following[33]

$$f_{RMS} = \sqrt{\frac{1}{T_2 - T_1} \int_{T_2}^{T_1} [f(t)]^2 dt}$$
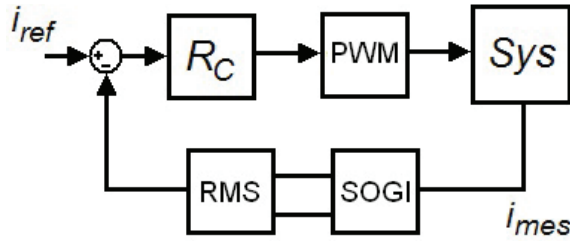
Figure 6.0.1: Scheme of the control system based on classic closed loop control with a transformation of the measured system variable.

Table 6.1.1: Paramters for the SOGI unit

Gain	Sampling Frequency	Omega
1.0	2000Hz	100π

The method above requires measurements to be done over the full period of the signal before the RMS value can be calculated. The measurement can be made more robus by gathering measures over several periods, at the cost of a slower dynamic performance. A large drawback of this method is its sensitivity to change in the signal angle speed. Such a change is not a problem in a simulation environment. In contrast this is likely to occur for the real implementation, since the grid voltage can vary slightly from the 50Hz. A better solution was sought after.

The RMS value can be found as long as a orthogonal phasor of the single phase value is produced. After the orthogonal phasor is created, the RMS value can be find by finding the magnitude of the $\alpha\beta$-vector or the dq-vector. Further the orthogonal phasor could be used in a PLL system to get the phase information of the grid voltage, which is valuable to the open loop control implementation later for the prototype.

One possibility was to use a Fictive Axis Emulator(FAE) developed at EPFL, Switzerland[27]. This system promises a much better dynamic performance than the standard transport delay. The described implementation is made for a system different to the AC Chopper. Using the FAE for the current project would necessitate modifying it, concequently this method was disregarded.

Second Order Generalized Integrator(SOGI) is another system for generating the orthogonal phasor of a single phase signal[32]. Many different methods were evaluated[6, 10, 9]. The choice of implementation would have to take into account the project's limited time, the available knowledge in the laboratory, relative ease of digital implementation(for the prototype) and adequate performance. A discrete SOGI was chosen with a z-approximation of the LaPlacian 's'[9].

From the source article two different approximation were tried implemented in Matlab Simulink: The triple integrator approximation and the trignometric approximation. The former method was predicted to be the most precise.
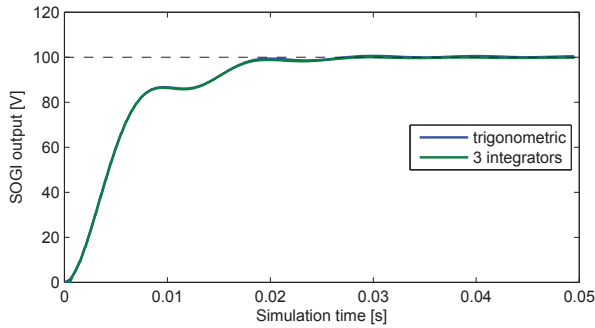
Figure 6.1.1: Step response of the two SOGI units to a 50Hz input voltage with an amplitude of 100V.

The values chosen for the SOGI module is listed in Table 6.1.1. The two methods were then tested in simulation with an input of a 100V 50Hz voltage signal. The RMS value of the voltage signal was found by calculating the magnitude of the voltage phasor and the orthogonal phasor produced by the SOGI. The performance of the two units are shown in Fig. 6.1.1 and Fig. 6.1.2.
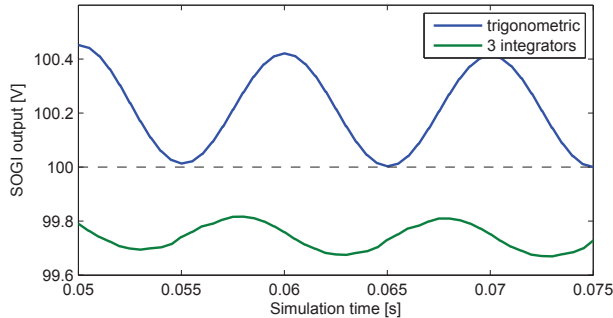
Figure 6.1.2: Close-up of the realtime SOGI output during steady state for a 50Hz input voltage with an amplitude of 100V.

Fig. 6.1.1 show the performance of the two methods to a step response. As seen in the figure, the step response and the static RMS error of about 0.2% are almost identical for the two methods. Fig. 6.1.2 show a close up on the two signals during steady state. A clear ripple is seen on the two signals. This 100Hz ripple is a characteristic of the calculation method. The observed difference between the two methods was the amplitude of the ripple, which is smaller for the triple integrator approximation. Seen how the AC Chopper reacts to sine input in the control loop in the former sections, the approximation producing less ripple was chosen i.e. the triple integrator approximation. The process continued to designing the current controller.

6.2 Designing a Controller

The method of designing the controller is based on two steps. The first step is to establish a valid frequency model of the system in question. The overall system was shown in Fig. 6.0.1. The impedance, containing a RLC element would easy to model in the frequency plane, on the other hand the transformation blocks posed a bigger challenge. Therefore a non parametric model was established by the use of a Pseudo Random Binary Sequence(PRBS). The second step was to design a controller based on the established system model and the desired controller performance. The Loop Shaping method was used to design the controller parameters[3]. These two steps are described in detailed in the following sections.

6.2.1 Non Parametric Model of the AC Chopper

The non parametric model was established with the use of PRBS. The system is treated as a black box with one input and one output. In this case the duty cycle input to the PWM unit is the input and the RMS impedance current is the output. The PRBS signal is used to excite the system, and both the input and the resulting output is stored. Then the results are processed to create the frequency model of the black box(the system). The details of this process is described in [3]. The result is shown in Fig. 6.2.1.
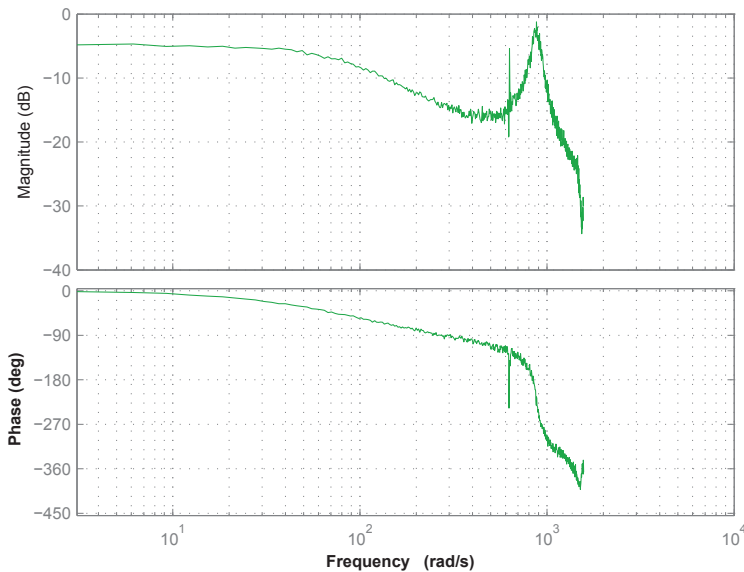
Figure 6.2.1: Bode diagram of the open loop system that was identified using PRBS. Magnitude is shown in p.u.

6.2.2 Design of Controller by Loop Shaping

Using the newly found model of the system the controller is designed based on the Loop Shaping method[3]. In short this method finds an optimized controller based on the designer's choice of the number of zero poles and the desired performance over the frequency specter. The resulting discrete controller is of the following form:

$$\mathbf{K}(z, \rho) = \frac{K_0 + K_1 z - 1 + K_2 z - 2 + ... K_n z - n}{1 - z^{-1}}$$

where $\rho = [K_0, K_1, K_2, .., K_n]$ and n is the number of parameters. This controller contains an integrator element to eliminate static error and n-1 zero poles. Fig. 6.2.2 shows the expected closed loop response with the designed controller.

The most stable controller was found by experimenting with the different design parameters. The general trend was that a slower controller gave less output ripple for the control variable (impedance current). This trend is contradictory to normal control practice, as a faster controller is able to react quicker to perturbations and control errors. In the case for the AC Chopper the situation was inversed. Thus a conservative and slow performance was desired. The desired performance was set to $w_b = \frac{1}{50}$, which is visible as a red line in Fig. 6.2.2. The controller frequency was also reduced to 500Hz. In this case a 5 parameter controller gave the best result.
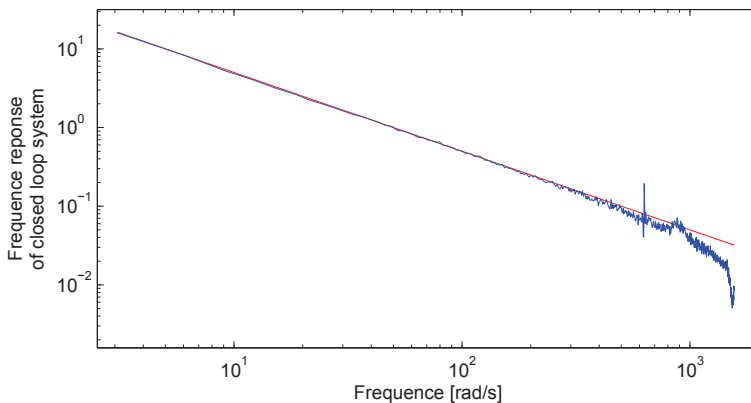
Figure 6.2.2: Bode diagram of the expected closed loop response using a 5 parameter controller.

6.3 Controller Performance

The simulation was done with Matlab Simulink. The set point for the RMS impedance current was set to 0.7. All values and components of the simulation were set according to the values found and noted in Table 2.6.1. All values are shown in p.u.
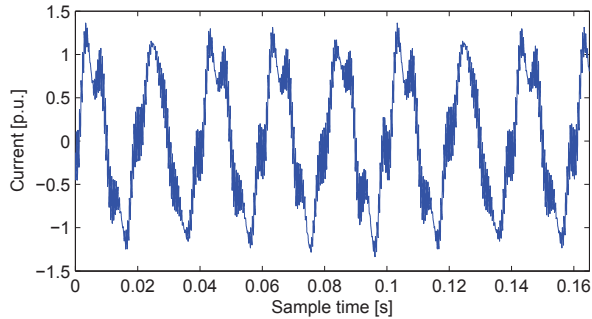
Figure 6.3.1: The realtime impedance current over the course of several periods. The 50Hz current is visible, but other harmonics are also present.
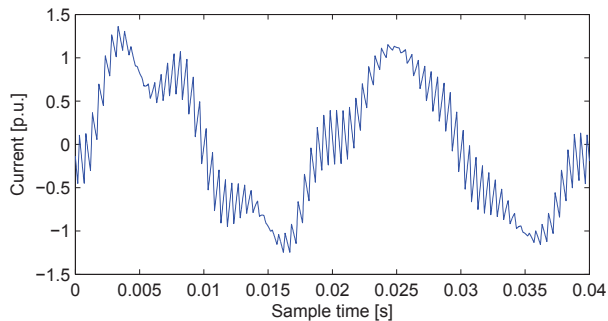
Figure 6.3.2: Close-up of the impedance current. The high frequency ripple is the switching ripple.

The measured impedance current is shown in Fig. 6.3.1 and a close up is seen in Fig. 6.3.2. The impedance current has a clear fundamental component of 50Hz. However other harmonics are clearly present. The calculated RMS of the current is shown in Fig. 6.3.4. The RMS current value was oscillating around the set point of 0.7 with ripples in the order of 8%. The steady state current contains a relatively high grade of ripples. Consequently the performance was deemed inadequate.
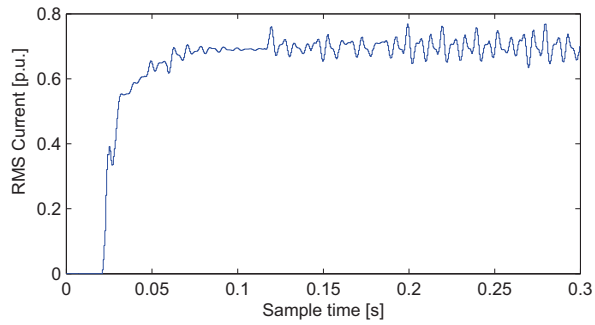
Figure 6.3.3: Step response showing the RMS impedance current of the closed loop system. The system responds fast, but the steady state is very oscillatory.
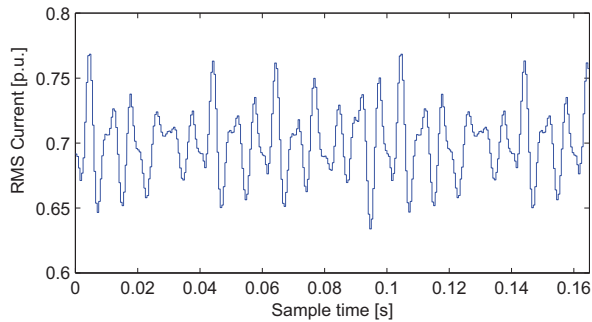
Figure 6.3.4: Close-up of the RMS value of the impedance current at steady state. Ripple amplitude reach up to 8%.

The duty cycle shown in Fig. 6.3.5 shows that the controller tried to correct the fault, but to no avail. In other similar control situations the solution would be to speed up the controller, but tests have shown that a faster controller creates more oscillations and ripple. The decision was made to further slow and dampen the control system in an attempt to achieve stable steady state current.
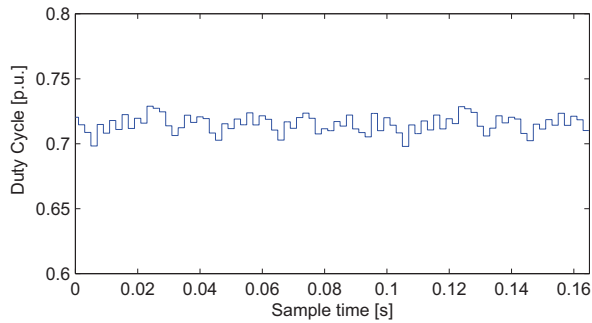
Figure 6.3.5: Close-up of the duty cycle from the controller for the same time window as for the former figure.

6.4 Second Attempt at Designing a Controller

A second controller was made because of the high ripple produced by the first controller. Since the trend had been that slower controllers gave less ripple the system was slowed down further. It seemed that even small ripples entering the control loop made a large influence on the output current. Therefore filters were added to the control system, which would both slow down the system and dampen harmonics. The second control system is shown in the block diagram in Fig. 6.4.2.

Two filters with a cut-off frequency of 10Hz were added. One filter was added to the output of the RMS transformation block. The other filter as added to the duty cycle output of the controller. This changed the system and a new non-parametric model and controller were made. The controller design parameters stayed unchanged. The system model and closed loop frequency response are shown in Fig. 6.4.1 and Fig. 6.4.3. Looking at the latter figure it was expected that this controller would have very little ripple, since all frequencies above a few Hz are damped.
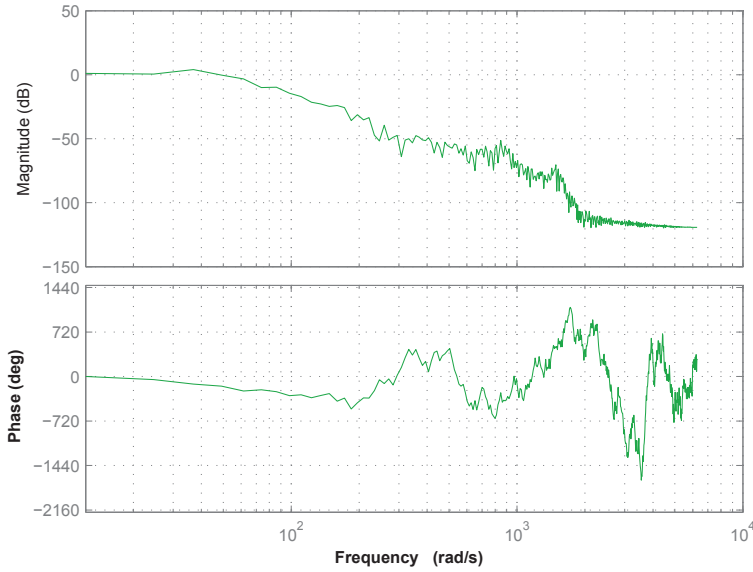
Figure 6.4.1: Bode diagram of the open loop system that was identified using PRBS. The added filters further dampen the system response even before the controller is added. Magnitude is shown in p.u.
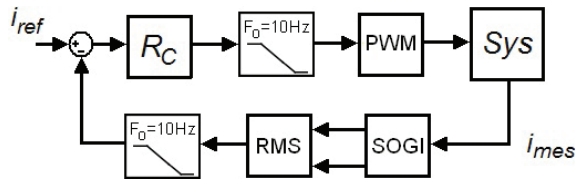
Figure 6.4.2: The new closed control loop scheme with heavy filtering.
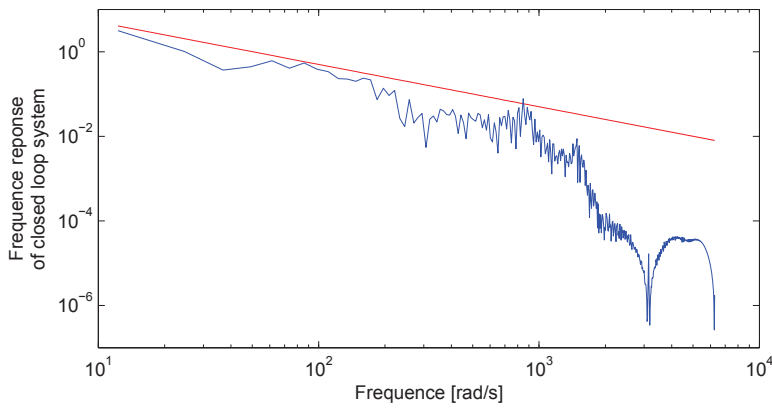
Figure 6.4.3: Bode diagram of the closed loop response using a 5 parameter controller and added filters.

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6.4.1   Performance of Second Controller

A second simulation was done to verify the performance of the second controller. The reference current was set to 0.7. The resulting impedance current is seen in Fig. 6.4.4 with a close up in Fig. 6.4.5. The figures show a real time current consisting almost exclusively of the 50Hz component. Compared to the performance of the first controller the current contains less harmonic content. Still some irregularities were observed.
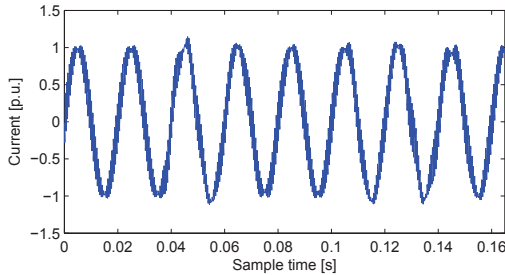
Figure 6.4.4: Realtime impedance current from closed loop control using the second controller. The fundamental component is dominant.
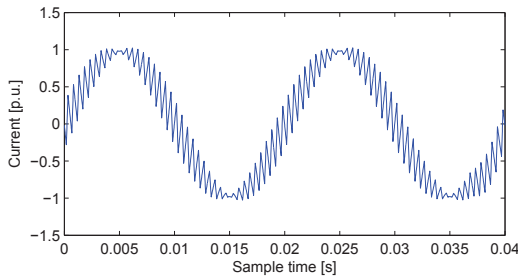
Figure 6.4.5: Close-up of the impedance current from closed loop control using the second controller. The high frequency ripple is the switching ripple.

Figure 6.4.6 shows the RMS current step response for the second controller. The transient period is long and oscillatory compared to that of the first controller. However the stable state is almost constant. A close-up on the RMS value of the impedance current is seen in Fig. 6.4.7. The duty cycle over the same time period is seen in Fig. 6.4.8. The RMS and duty cycle still show small oscillations. The RMS current contains longer periods of constant value. Though this value is below the set point, hence the controller increases the duty cycle slightly to correct the error. After some time the RMS measurement starts to increase. The increase overshoots the reference point. The controller then regulates the current back to a stable situation below the set point and the process is repeated.

Compared to the first controller, the ripple and oscillations are heavily reduced. Unfortunately the ripple is not removed completely. The dynamic response is also dramatically
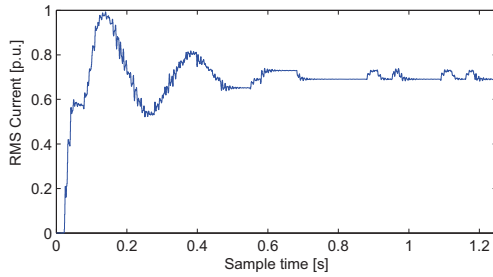
Figure 6.4.6: Step response showing the RMS impedance current of the closed loop system using the second controller. The response is slow and oscillatory during the transient period, while the steady state current is quite stable.
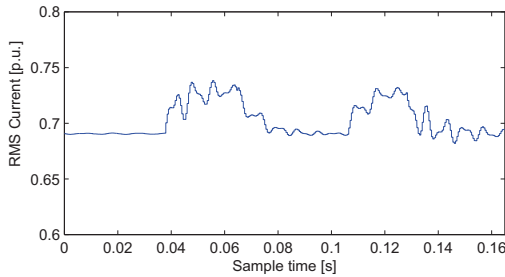
Figure 6.4.7: Close-up on the stable state RMS value of the impedance from closed loop control using the second controller. The current is stable for a longer period just below the set point of 0.7, followed by a new transient period. This behavior is then repeated.

reduced(Compare Fig. 6.3.3 and 6.4.6).

6.5 Chapter Conclusion

In this section an effort has been made to create a closed loop control system for the impedance current. Former experiments with control systems for the AC Chopper indicate that only the amplitude of the current should be controlled. The implemented system tries to control the RMS value of the current using a classical control scheme. The RMS value is calculated using a SOGI unit. The SOGI unit using a triple integrator approximation was implemented and tested. The controller was designed by acquiring a non parametric model of the system and then using loop shaping to design the controller parameters.

The first attempt at a controller resulted in a system able to follow the set point given by the user, but with relatively large ripples and added harmonics. This results was surprising
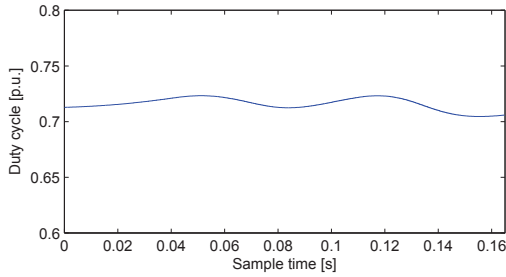
Figure 6.4.8: Close-up of the duty cycle form the closed loop control using the second controller.

because the expected closed loop behavior shows that all frequencies above some tens of Hz should be damped. Results being unsatisfactory a new attempt at making a control system was made. During experimentation with controller parameters the trend was clear: a slower controller gave less ripple. Thus filters were added to the control loop and the design process was redone.The second controller showed less ripple at the cost of slower dynamic response. Still there are some oscillations that remain undamped.

More filters could be added and the controller could be slowed down even further to dampen the last oscillation. Slowing the system in such a manner also slows down the dynamic response. The implementation made at the University of Toulouse also showed problems with output current ripple, so it seems the problem was not isolated to this project. But instead of adding filters or slowing the controller down further, it seems the control of the AC Chopper should rather be done in open loop for reactive compensation with the fundamental current. The open loop control has shown good correlation to the theoretical formulas, and a control system based on this approach might give adequate performance in a reactive compensation scenario.

At the time of writing of this report a new paper regarding the AC Chopper was recently published[34]. The paper uses a dq system to control the grid current. Results show that the system is able to produce a fundamental current without harmonics. This shows that using a controller based on the dq reference system might be an option to open loop control.

Chapter 7

Making an AC Chopper Prototype

The last of the project goals is to make an implementation of the AC Chopper and to to verify simulation results with live experiments. This chapter describes the design choices, the development process and the solutions that were implemented within this project as well as the encountered hardware limitations.

7.1 Prototype Design

7.1.1 Prototype Rating

As mentioned in the problem definition, the specifications of the prototype changed during the course of the project. The last specification that was realized is given in Table 7.1.1.

Table 7.1.1: Specifications of the AC Chopper lab prototype

Nominal voltage	Nominal capacitive power	Nominal current	Impedance resonance frequency	Filter resonance frequency
50V RMS	< 100VAR	2.4A RMS	200Hz	1000Hz

The control of the device MOSFETs were to be done with an external device. The external device, called "the BoomBox" is described next in Section 7.1.2. The BoomBox was developed by former and current PhD students at the same laboratory as where the prototype was realized (LEI, EPFL). Currently, Simon Delalay and Nicholas Cherix are responsible for the development.

The lower voltage and current ratings were chosen to avoid strict safety requirements and component complexity. For example, the tracks on the PCB could be closer and MOSFETs with lower blocking voltage could be used. This allowed an overall smaller and simplified prototype design process, while still keeping device ratings high enough to be able to show the behavior of the AC Chopper with reasonable precision.

The 50V RMS voltage rating allowed for use of plugs and contacts without upgraded isolation. With the lower voltage rating, the power and current rating were also downgraded. The power rating is of little importance when trying to show device behavior, and the current rating is of an order where most devices in the laboratory could be used for the experiments. The filter resonance frequency was increased to allow for the device to produce higher harmonics without exciting the filter itself.

The design process steps was done in the following order:

1. Ideal circuit components were added to the schematic and the correct pins were connected

2. A matching real component from an electronics manufacturer was selected, modeled in Altium and replaced the ideal component in the schematic

3. If the real component changed or created a need for other components, the design process was iterated from the first point

4. The components from the schematic were added to a PCB editor environment and the physical PCB layout was made

Particularities of each process step are described in the following subsections.

7.1.2 BoomBox

The BoomBox is a control platform intended for laboratory experiments with low-power laboratory prototypes[11]. It was developed at the LEI laboratory at EPFL, Switzerland. The function of the platform is to act as a intermediary stage between a computer and the prototype. The BoomBox is programmed in C or C++ and the program is transferred by USB to the internal storage of the BoomBox. The program has access to a series of modular hardware which provide input and output intended for prototype control, in particular power electronics. For example the BoomBox can easily be programmed to provide both electric and optical PWM signals and retrieve sensor values. During operation real time communication with the internal systems is possible from a computer through a serial port interface. With the BoomBox a faster development process for the prototype is achieved.

For this project the BoomBox was programmed in C. The BoomBox was used to generate optical PWM signals to control the AC Chopper transistors. With the installed voltage and current sensor on the PCB, open loop and closed loop control was planned with the aid of the BoomBox.
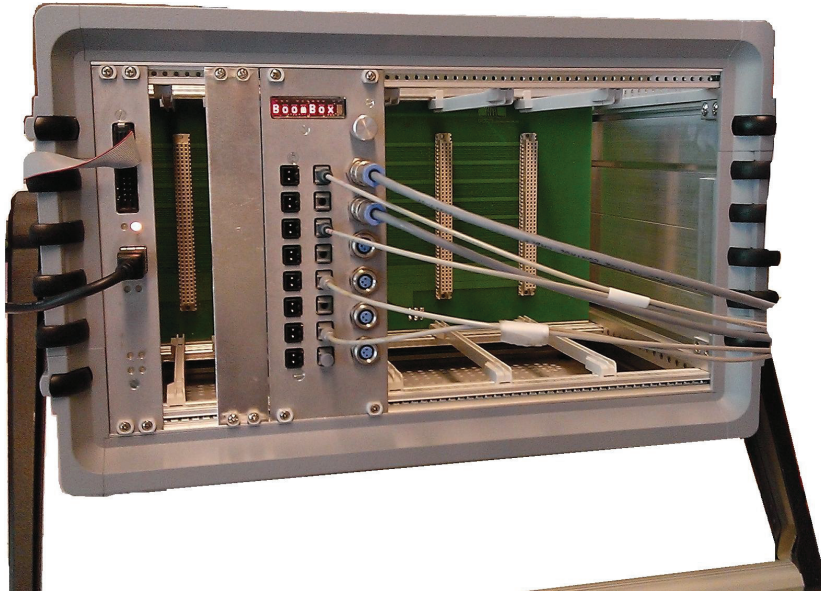
Figure 7.1.1: The physical appearance of the BoomBox. To the left the is motherboard with connected cables for external communication over USB and Serial. In the middle is a single MultiA daughterboard containing ports for sensor input and optic or electric output ports from PWM units.

7.1.3   Schematics

The schematics were designed using Altium software. The schematics are found in App. F and consist of two parts. The first schematic shows the overall circuit similar to the circiuit drawings i.e. Fig. 2.1.2. The second schematic shows a module that was connected to each transistor. This module contained the support systems for each MOSFET consisting of the power supply, optic receptor for the external gate signal and support logic.

The schematics differ from the concept figure on two points: Since the capacitors and inductors of the impedance and filter are of a relatively large physical size they were not implemented on to the PCB, and are therefore excluded from the schematics. Instead plugs are added to allow for external connection of the components. The second difference is the support systems for the gate signal of the MOSFETS. The gate signal was transfered from an external source in the form of an optic signal. This optical signal is received and controls a driver circuit which in turn controls the gate pin of the MOSFET. Due to the AC Chopper circuit behavior the support systems, for all four transistors need a floating power supply. This was achieved by adding a DC/DC converter with galvanic separation to each support cell.

7.1.4 Component Selection

The most influential selection criteria for components was the need to use the available component stock at the LEI laboratory. Only after the stock had been searched without success was a component sought externally and bought. A list of all the used components with manufacturer and part number can be found in App. E. In the table below, each component or group of components are listed with an added note. The note explains some background information regarding the component choice and tries to convey the aim behind each choice made during the process.

Impedance and filter capacitor	The AC Chopper impedance and the input filter will both operate at 50Hz AC, which eliminates cheap electrolytic capacitors as an option. Instead film capacitors were chosen. Since the number of choices are limited within this category the capacitance was the only criteria.
Impedance and filter inductor	The inductors were produced in the lab. Metglas cores were used(AMCC 40) which were wound with varnished copper wire. The wire had a diameter of 1.2mm, which should support a current of more than 5A RMS current. The varnished wire, as opposed to wire with plastic isolation, allows for higher winding density and thus reducing the size of the inductor.
MOSFET	There were two reasons for the choice of MOSFET. Firstly the breakdown voltage was more than double the expected voltage allowing for large overvoltages during prototype testing without destroying the component. Secondly there was an abundance of replacement MOSFETs available in case of component failure. The chosen MOSFET has a current rating far over the prototype rating and acceptable on-resistance.
Diode	External diodes were added since the MOSFET body diode was deemed too slow. Faster diodes were acquired with the same breakdown voltage rating as the MOSFET.
Optic Receptor	For the optic receptor the same brand as the transceiver found in the BoomBox was chosen. The chosen receptor as the inherent property that it inverses the input signal. Therefore, a high optic input at the BoomBox side results in a low electric signal at the receptor output. Thus an inverting element was needed between the receptor and the MOSFET driver enable pin.

Inverter	A small signal n-MOSFET was chosen to invert the signal. The inversion is done in a pull-up resistor setup[25]. In such a setup it is not the MOSFET itself that supplies the current to the enable port of the driver, the current rather comes directly from the 5v supply. The consequence is that the current and ohmic rating of the MOSFET can be greatly ignored.
Pull-up resistor	The maximum and the minimum values for the pull-up resistor were calculated to 10400Ω and 0.84Ω respectfully[18]. A 1000Ω 0.6W resistor was chosen.
Voltage supply for driver and logic circuit	15V was supplied to the drive circuit by the use of a 5 to 15V galvanic DC/DC converter. 5V were supplied to the converter externally. The converter was taken from the lab stock and was rated for 1W, which well exceeded the maximum consumption. A load resistor was added to the converter to guarantee an output voltage within $15V \pm 0.5V$. Also connected to the 15V rail of the converter was a linear 5V voltage regulator, which supplied the circuit logic.
Decoupling capacitors	Decoupling capacitors have been placed at the entry of all ICs with a capacitance according to the requirements found in the components' datasheets.
MOSFET driver	The driver circuit is designed to supply or drain charge from the MOSFET gate, in turn switching the transistor on and off. The higher the current rating of the driver the faster the charging of the gate capacitance which results in faster switching times. A driver capable of supplying a high charge current was chosen to allow for fast switching speed if needed. If slower switching was desired then higher ohmic gate resistances could be added.

Gate resistance	The quality of the track layout connecting the driver and the gate of the MOSFET decides the size of the stray inductance. The stray inductance and the gate capacitance form a LC circuit. When the driver changes state, this LC circuit is excited and a oscillation or "ringing" can occur. This ringing can be dampened by adjusting the resistance, at the cost of a slightly slower charging of the MOSFET gate capacitance. Estimating the stray inductance from the PCB design is complicated. To save time, the possibility of adding a gate resistance on the PCB was included. Small resistors starting from 1Ohm and increasing with 1Ohm steps where made available in stock and the tuning of the gate resistance was done by measurement. Because of a fault during this process a very large resistance of 133Ω was added, slowing down the MOSFET turn on and off processes. Since the slower performance was not critical to the circuit application, the larger gate resistances were kept.
Snubber circuit	An overvoltage snubber circuit was added to the circuit. An overvoltage snubber is designed to absorb the energy stored in the stray inductance during the switch off cycle and burn the energy off in a resistor during the turn on cycle. This limits the overvoltage on over the drain and source terminals of the MOSFET, and can be necessary in certain situations to stay within the breakdown voltage rating of the transistor. There are exact ways to calculate snubber values if the stray inductance is known. Measuring the stray inductance can be costly and complex, and so a different and simpler methods was applied[28]. In addition for an AC circuit, the MOSFET current and voltage change during the cycle, changing the performance of the snubber. The snubber was dimensioned for the nominal RMS values. The installed snubber consisted of a 1nF ceramic capacitor and 22Ω resistor.
Sensors	For the open loop and closed loop regulation the input voltage and the impedance current had to be measured. Appropriate sensors were chosen which would be compatible with the external device that would control the AC Chopper. These sensors were the standard choice at the LEI laboratory and were handed out.

7.1.5 PCB design

The design choices were limited externally by what the PCB manufacturer was able to produce. The PCB was produced at the ACI workshop at EPFL. The workshop's manufacturing methods imposed some specification limits. The board was produced using FR4-material and one copper layer on each side of the board, a varnish finish was added as top coating, drill holes could be done with a 0.1mm resolution, and the maximum card size was 320x230mm.

The PCB layout and 3D mechanical view was designed using Altium software. The 3D model was made to avoid space conflicts between components(e.g. the MOSFET heat sink in conflict with surrounding components). To achieve a good design, online guides were used, experienced colleagues were consulted and material from university courses were used[19]. Since this was a prototype several extra pin holes were added as test points, thus voltage levels on all points of common coupling could be easily be measured.

During the PCB design process, several points were given special attention:

- Minimizing stray inductance

For all components, the return track was placed as close to the connecting track as possible. Usually a ground plane was placed on the opposite side of the PCB. This also increases the immunity against EMI of the circuit, since smaller circuit loops results in a smaller area for incoming EM radiation[22].

- PCB track rules

Minimum clearance between tracks is a function of the voltage difference between the two tracks to avoid voltage breakdown[19]. Further, any track on the PCB must be wide enough to support the current passing through it. All tracks have higher clearance than necessary and where possible track width was maximized to decrease losses and assure low temperatures. In addition, the tracks on the PCB have no bends with an angle over 45°, which guarantees low and even temperatures.

- Ground plane

Ground planes were made to cover as much area on the back side of the PCB as possible. Such planes give shorter return tracks and thus supporting the first point. Also ground planes improve EMI immunity.

- Visual appearance

An effort was made to make a PCB design that is pleasing to the eye with clear structure and good order. A good design can increase the pride of the designer and increase the respect of colleagues. More importantly, it makes it easier to obtain an overview of the circuit and thus simplifies debugging and identifying faults.

The resulting PCB design is seen in Fig. 7.1.2. The figure shows the rendered 3D model of the design.
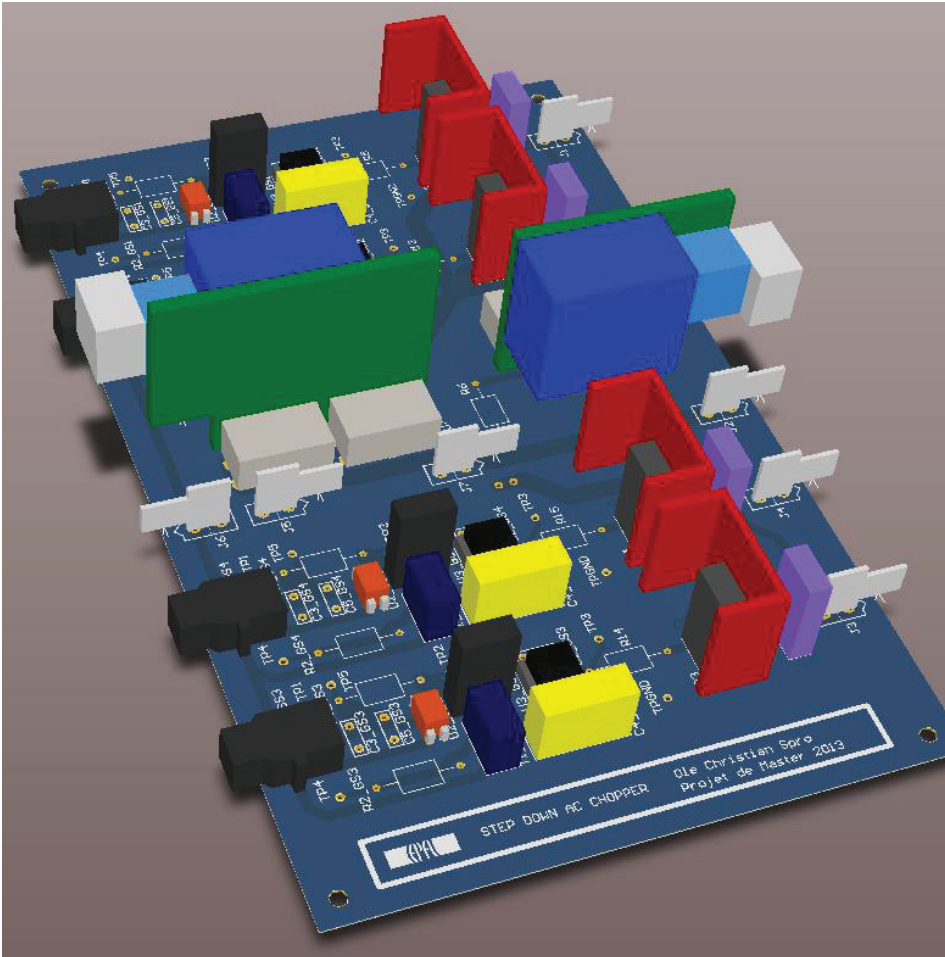
Figure 7.1.2: The finished PCB design as seen in Altium. The black squares on the left edge are the optical receptors. The large U-shaped red elements are the heat sinks on the MOSFETs. The smaller components between the receptors and the MOSFETs are the support circuitry. The violet components to the right of the heat sinks are the diodes. The large blue and green components are the two LEM sensors. Several LUG contacts are seen on the board, mainly on the right side of the PCB. These allow external connection with the input filter, the impedance and the external +5V source. The rendered model shows the top overlay in white. This was not present on the final PCB due to manufacturer limitations.

7.2 Finished PCB and Test Routines

The PCB was produced by the ACI workshop at EPFL and is seen in Fig. 7.2.1. The first step taken was to verify track integrity and drilled hole sizes. Then all components were soldered by hand to the PCB. After each soldering the solder integrity was verified with the use of a multimeter.
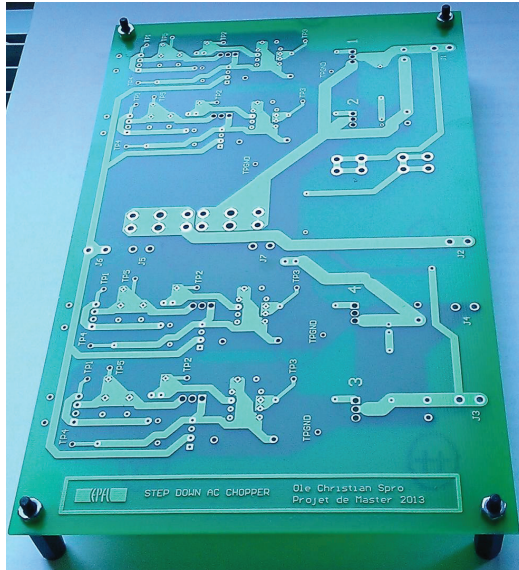
Figure 7.2.1: The PCB as received from the ACI workshop.

Two problems were discovered. In the pin layout in Altium for the driver chip, pins 5-8 were inverted compared to the data sheet. Since pin 6 and 7 are the same output, in practice only pin 5 and 8 were inverted. This problem was overcome by adding two more sockets in the one that was already soldered to the PCB. The two extra sockets were modified so that the formerly mentioned pins were inverted. The result is seen in Fig. 7.2.2. The second problem was that the screws for attaching the current LEM sensor to the PCB could not be unfastened once the rest of the components had been soldered to the PCB. The solution was to attach the sensor before soldering the conflicting components.
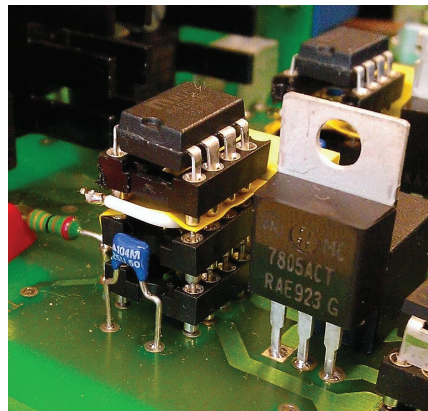
Figure 7.2.2: The solution to the pin problem.

The PCB with the soldered components are seen in Fig. 7.2.3 and in Fig. 7.2.4 the heat sinks and the cables have also been attached .
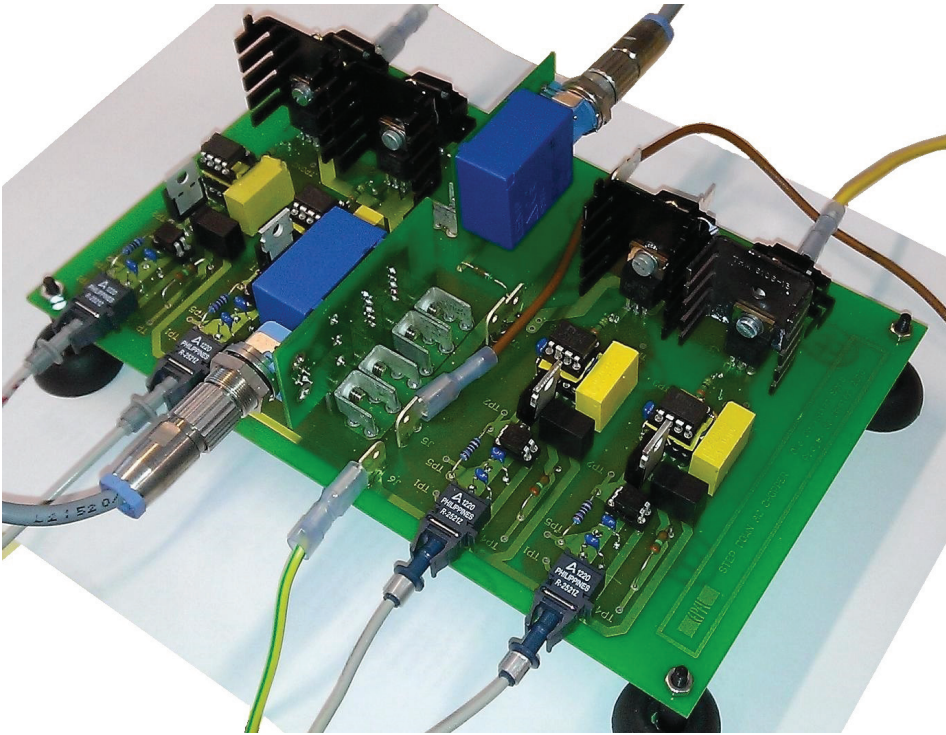
Figure 7.2.3: The converter module on the test bench with connected cables. At the bottom the four optic receptors are seen in dark grey with connected optic cables. The large blue components with the larger metallic contacts are the LEM modules to measure impedance current and input voltage. The +5V source for the driver circuit was supplied by an external source which is connected by the two LUG contacts at the bottom marked J5 and J6. The center LUG contact is for board debugging only. Contacts for the converter input and output are lined along the higher side of the PCB. The MOSFET and the diodes are seen with their heat sinks.
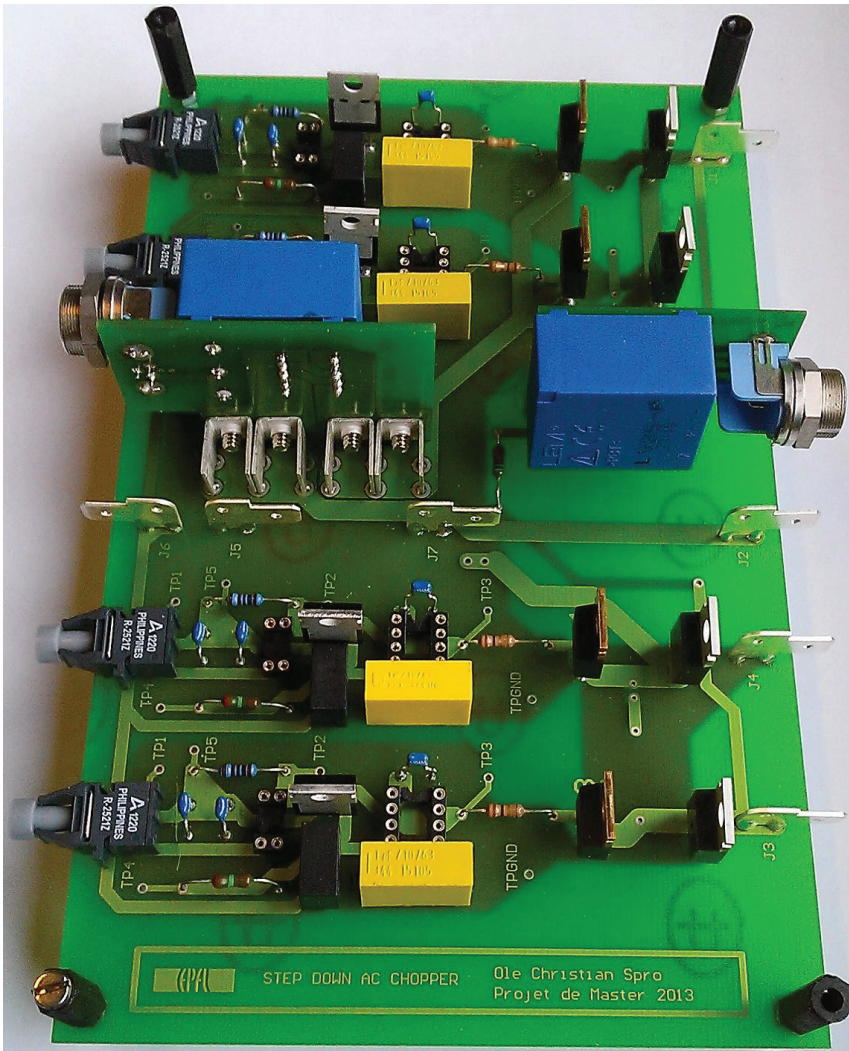
Figure 7.2.4: Overview of the PCB with the soldered components. The MOSFETs and the diodes are depicted without their heat sinks. The silk overlay layer seen in the figure of the designed PCB are not visible in the finished product since the manufacturer did not possess the equipment to do so. The bottom logo, test points and contact indicators are visible since they were added to the copper layer in the PCB design. The indicators makes it easier for the user to identify and operate the prototype.

7.2.1 Component Testing

After soldering was completed, all components were tested on the board to verify behavior and measure performance. Only the +5V was supplied to the circuit and the optic input would be manipulated. Then correct voltage levels on different test points were verified. Lastly the MOSFET and diodes were tested with low DC voltages. The test routine was made in advance and was therefore well structured. Tests were checked off the list as they were performed, as seen in Fig. 7.2.5.

Figure 7.2.5: Picture of the test sheet after tests had been done. The tests were planned to be executed in the right order and for all possible test parameters. As seen in the picture almost all tests were checked off green, confirming correct behavior. The four tests with orange crosses were found to have 0.1V above expected value, so they didn't comply with the expectation. Still, these components were passed since the overvoltage was relatively small.

Comparing Fig. 7.2.6 and 7.2.7 the effectiveness of the snubber becomes obvious. Especially for the turn-off cycle during which the snubber help dampen oscillation due to stray inductance. There is still a voltage overshoot at turn-off, but since the relative is size was so small it would not pose a problem for the circuit at full voltage. Thus the snubber circuit was kept at calculated values.

The MOSFET measurements were used later to set the PWM modulation dead time for
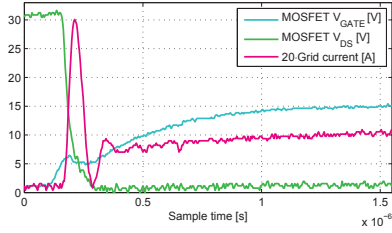
(a) MOSFET gate signal turn on
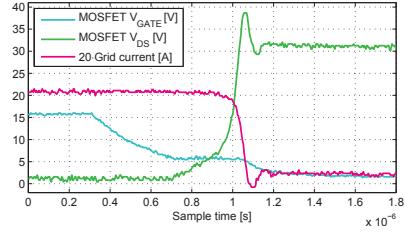
(b) MOSFET gate signal turn off

Figure 7.2.6: Testing of MOSFET turn-on and turn-off with an applied DC voltage of +30V and a 0.5A average current. The switching was made with the snubber circuit in place.
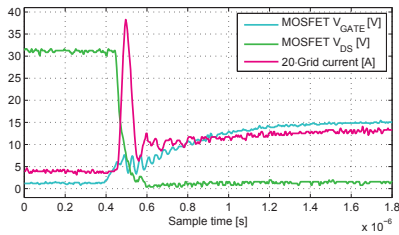
(a) MOSFET gate signal turn on
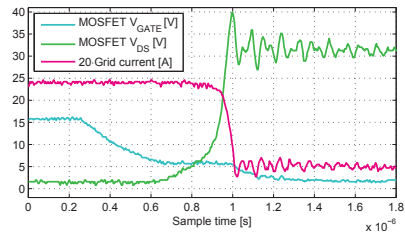
(b) MOSFET gate signal turn off

Figure 7.2.7: Testing of MOSFET turn-on and turn-off with an applied DC voltage of +30V and a 0.5A average current. The switching was made without the snubber circuit.

the switching cells. The turn-off speed of the MOSFET could have been shortened by adding a diode to the gate circuit. Both the turn-on and turn-off times could be improved by adding a lower gate resistance. The relative long inversion time could have been improved by using a more suitable MOSFET, but this performance was not critical for this project.

The passive components were also tested to verify their rated values. The results are shown in Table 7.2.2.

The inductances were measured by applying 50Hz current and measuring the voltage. With a resistance measurement using a multimeter, the inductance value was calculated along with realtive saturation over the measured current range. The capacitors were measured with an RLC meter. It was later discovered that there were some issues with the RLC meter that might have affected the precision of the measured values. Other phenomena observed later indicated that the capacitance values were in the measured area, hence the capacitors were not remeasured.

Table 7.2.1: Measured turn-on and turn-off times

Component	Turn-on delay	Turn-off delay
Receptor	10ns	50ns
Inverter	200ns	800ns
MOSFET	200ns	800ns

Table 7.2.2: Measured values of the passive elements of the prototype

	Rated value	Measured value	Relative saturation
Impedance capacitor # 1	$66\mu F$	$64.1\mu F$	
Impedance capacitor # 2	$66\mu F$	$63.0\mu F$	
Impedance inductor	$5.0mH$	$5.04mH$	7.0% (1A-6A)
Filter capacitor	$47\mu F$	$47.4\mu F$	
Filter inductor	$0.5mH$	$0.47mH$	0.5% (1A-6A)

The LEM modules installed on the PCB were calibrated. The details of the sensor circuit and processing by the BoomBox was found in the BoomBox manual[11]. A range of voltages were applied to the sensors. The applied value and the read-out in bits on the BoomBox were recorded. The results with tendency lines are shown in Fig. 7.2.8 and 7.2.9. The zero crossing point was decided with the voltage sensor being short circuited and the current sensor being in open circuit.

The setup for the LEM sensors are listed in Table 7.2.4.

Table 7.2.3: Estimated resonance frequencies for the impedance and the filter based on measured component values

	Resonance frequency
Impedance	199Hz
Filter	1066Hz
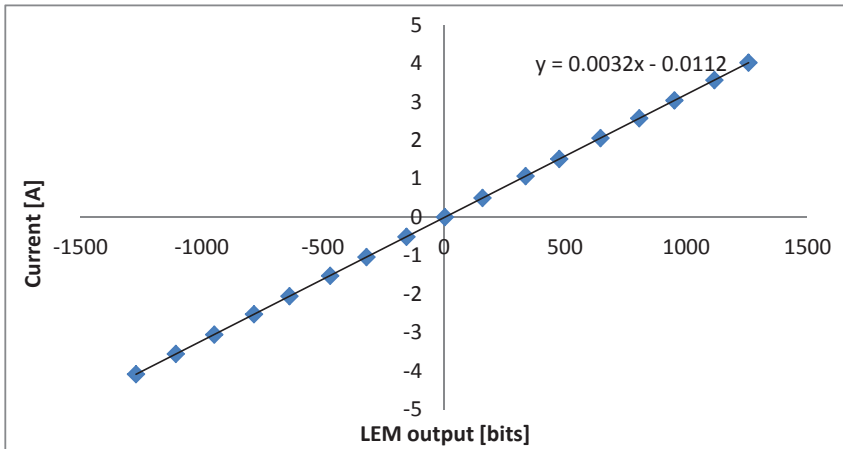
Figure 7.2.8: The results from the calibration process of the current sensor. The blue diamond points show the recorded values while the black line shows the calculated tendency line.

Table 7.2.4: Parameters for the current and the voltage sensors

	Hardware gain	Software gain	Software offset
Current sensor	2.5	0.0032	-0.0064
Voltage sensor	1.0	0.0561	0.0561
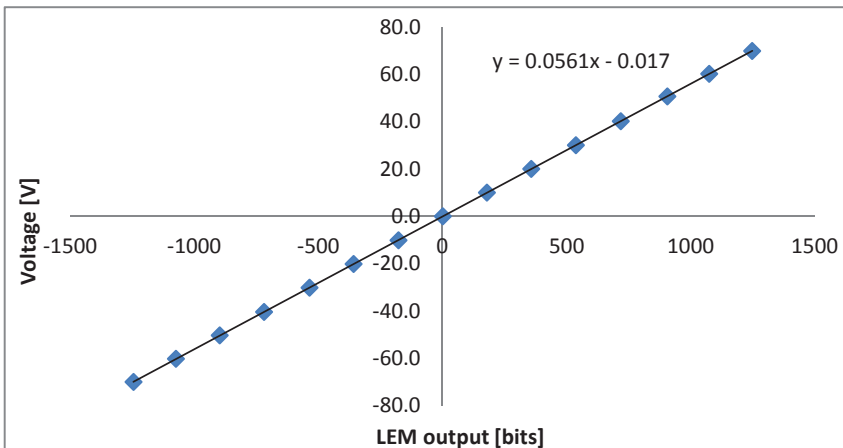
Figure 7.2.9: The resuts from the calibration process of the voltage sensor. The blue diamond points show the recorded values while the black line shows the calculated tendency line.

7.3   Software Development

In this section, the software development for the prototype will be discussed. This includes the software design process that was done before coding started as well as special phenomena that had to be taken into account when coding. Some results of the support systems that were coded to facilitate the open loop control will also be shown. The closed loop control was never implemented in the prototype for reasons that will be shown in a later chapter.

7.3.1   Software Design and UML 2.0

UML is standard for software model design based on best practices from the industry. The language is a graphical approach to building software systems that was developed during the early years of object oriented software development. Its quick and wide spread adoption is a demonstration of the effectiveness and the power in using this tool. The standard is controlled by an open consortium of companies called the Open Management Group[12]. The standard includes many different graphical notations with each their own set of rules and uses. The notations are used as early sketches of a system denoting structure, relations, order and more in a high level of abstraction. The UML sketches are said to be used as blueprints which the programmer later can implement.

In this project UML has been used for the software development of the program that was to run on the BoomBox platform, the program that controlled the AC Chopper. The UML notations that were used includes Use Cases and State Machine Diagrams. These diagrams are found in App. D. The Use Cases show the possible ways the different actors can interact with each other, and then the interaction are specified further in a separate document. The general scenarios and behavior of the system was then described. The State Machine diagrams show the behavior of the general state machine controlling the prototype program and the state machine controlling the switching setup.

7.3.2   Software Used in Development and Monitoring

To implement the features and monitor the BoomBox during operation two software packages were used.

The IDE that was used to code the program in C was Code Composer Studio(CCS). CCS came from Texas Instruments, which was also the producer of the chip that was controlling the BoomBox. Consequently, CCS could be used for program development, transfer of the compiled program to the BoomBox and provided monitoring features during experiments.

The open source program Tera Term was used. Tera Term has existed since 1994 and offers support for several communication standards for terminal environments. Tera Term supplied a simple terminal to communicate with the BoomBox over the serial port.

7.3.3   BoomBox Characteristics Influence on the Design

There were two characteristics of the BoomBox that had a large influence on the final software design.

1. BoomBox PWM shadow registers

When the function call is made to set the duty cycle of a PWM module, the duty cycle is sorted in a register on the BoomBox. This register, however, is not directly used by the BoomBox to control the output of the PWM module. Rather every time the BoomBox has finished a PWM period(one sawtooth of the PWM carrier signal), the value in the register containing the duty cycle value is transferred to a shadow register. This shadow register is involved in the setting the output of the PWM module at any time.

The consequence of this operation is that the duty cycle can only be changed at the end of a PWM period. For most situations this would be standard operation, and the user is blocked from oversampling by mistake. But for operating the AC Chopper this operation translates into a system of less performance.

In Section 2.2, the switching strategy was presented and the reason why the switching setup must be controlled to avoid short circuits was explained. When a polarity change for the grid voltage occurs then certain switches must be turned off to avoid short circuiting the grid. But since the duty cycle of the PWM modules are only updated every PWM period the switching must occur before the polarity change takes place. The exact calculation is done in Section 7.3.4. The results from the open loop testing will also show how the shadow register characteristic influence performance.

2. BoomBox stops all switching output on internal error

There are several ways for an error to occur on the BoomBox platform. A software error could be triggered if the user tries to do something that is illegal by the coding standards(e.g. division by zero). A hardware error could be triggered if the sensors connected to the BoomBox measure a current higher than the set limit. This type of error is a safety feature designed to protect both the BoomBox itself as well as the prototype.

In the case where an error is triggered, one of the first responses of the BoomBox is to shut down all PWM modules. This also is a safety feature to protect the prototype, and works perfectly for topologies with self opening free wheeling paths. For the AC Chopper to be set in free wheeling mode, two MOSFETs must be turned on (T_{1c} and T_{2c}). In the case of an error, the impedance current would have no path to follow, and huge overvoltages might occur and irreparable damage might be done to the prototype.

To overcome this unforeseen problem, a metal oxide varistor of suitable rating was added to the circuit. The varistor was placed over the impedance and would provide a path for the current in case of error, protecting the prototype circuit. The specifications of the varistor are presented in App. E.

7.3.4 Safe Switching

The program controlling the prototype must be able to guarantee safe switching arrangement to avoid overvoltages and short circuits. Two actions were taken to guarantee safe switching:

   1. Setting the correct dead time for each switching cell

In power electronic theory, the two switches in a switching cells are never allowed to be turned on at the same time[4]. And as seen in Table 7.2.1 the turn-on and the turn-off times for the MOSFETs are different. If the control signals to turn one MOSFET on and the other off are sent simultaneously then both switches will be turned on at the same time, and AC Chopper will be short circuited. To avoid such a situation a dead time must be set between the first switch being turned off and the second switch being turned on. A dead time of approximately 1200ns was set.

   2. Enter and exit free wheeling mode during polarity change
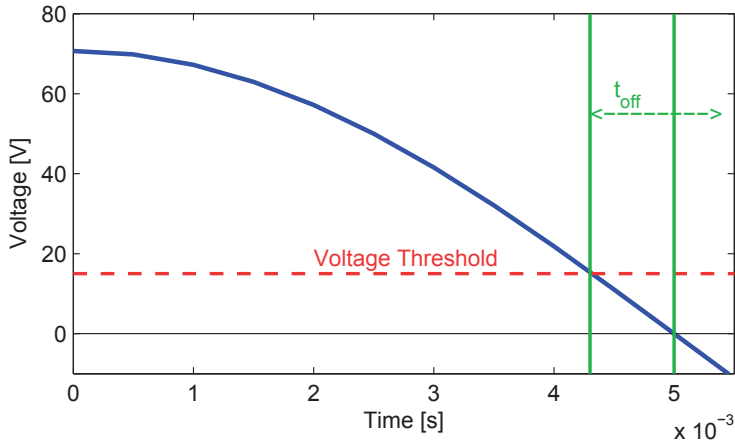
Figure 7.3.1: Concept of voltage threshold concerning the sensing of when to set the AC Chopper in and out of free wheeling mode.

As described in Section 7.3.3, there were challenges related to the switching around grid voltage polarity change. If the polarity of the grid voltage is reversed and the switches are not changed accordingly then the the AC Chopper constitutes a short-circuit.Therefore action was taken to avoid such a short-circuit. In this case, there were two possible setups: The impedance was connected to the grid or the impedance was set in free wheeling mode[1]. For this project the impedance was set in free wheeling mode.

When the grid voltage was measured to approach a zero crossing, the AC Chopper was set in free wheeling mode. When the grid voltage had passed the zero crossing, the switching was resumed with the appropriate switching setup. To detect the zero crossing, voltage thresholds were set up. The measured grid voltage was evaluated together with the voltage

Table 7.3.1: Performance of the SOGI and PLL modules

	Input Voltage (multimeter) [V RMS]	Estimated Voltage [V RMS]	Connected PLL Estimated ω
$SOGI_{3I}$	49.6	49.72 ± 0.21	$100\pi \pm 0.25$
$SOGI_{trig}$	49.6	51.75 ± 4.70	$100\pi \pm 4.5$
$DirectRMS$	50.3	50.79 ± 6.49	–

derivative to determine the voltage state(close to a zero passing or if already passed). The program behavior is described in the switching state machine diagram in App. D.

The threshold voltage was dependent on several factors: the resolution of the voltage sensor, sensor noise, the switching time delay, the update rate of the input voltage and the grid frequency. The time dependent factors where translated to voltage values as shown in Fig. 7.3.1. The threshold was calculated in the following way:

$$U_{threshold} = U_{resolution} + U_{noise} + \hat{U}_{grid}sin\langle 100\pi(T_s + t_{delay})\rangle$$

where T_s is the PWM period and constituted the largest factor of them all. As a result, the PWM frequency was directly going to influence the part during each grid period where the impedance was not connected to the grid.

7.3.5 Support Systems - SOGI and PLL

As described in former sections some support systems were needed to perform open and closed loop control. The SOGI system was implemented to calculate the RMS value of the impedance current. The PLL unit was added to shift to the phase of the duty cycle in open loop control. The grid voltage was used as reference. The two systems were implemented in the BoomBox program. The SOGI module was implemented as detailed in Section 6.1. The other SOGI alternatives were also implemented to show the performance difference. The results are shown in Table 7.3.1 and in Fig. 7.3.2 and 7.3.3. The implemented PLL unit was present in the BoomBox software library. It was paired with the SOGI modules to measure angle speed and phase of the grid voltage. The results are shown in Table 7.3.1 and Fig. 7.3.4.

7.4 Chapter Conclusion

In this chapter, the process of designing, building, programming and testing the prototype has been described. In an effort to comply with common standards regarding such a development process, design methods or commonly used guidelines have been utilized.
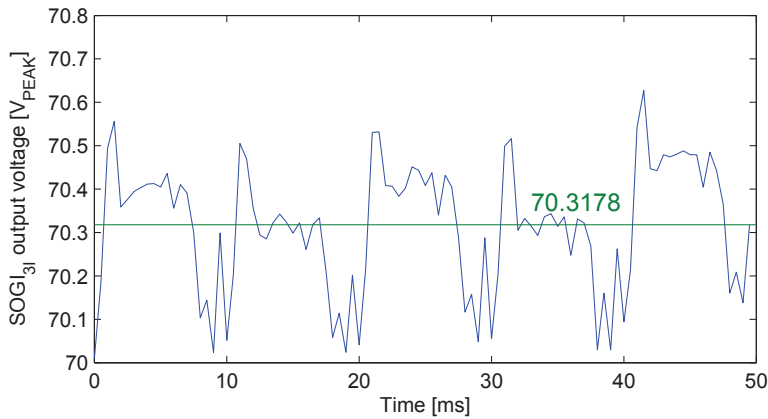
Figure 7.3.2: Real time RMS voltage output from the triple integrator method SOGI module in blue. The green line marks the average. The value in the graphs have not been divided by $\sqrt{2}$ which is why the values are higher than expected. The corrected RMS value is found in Table 7.3.1.

The choice of components were made to fulfill a prototype with a performance comparable to or better than the ratings that were set early in the project. The ratings are found in Table 7.1.1. The design of the PCB realizes the AC Chopper circuit and the support systems according to the schematic. Focus was set on creating a clean and structured design to simplify the testing and manufacturing job later on while maintaining safety standards with an extra margin.

The PCB was produced and the components were soldered to the board. A detailed and strict testing routine was kept during the whole process to avoid problems or mistakes in later parts of the process. The finished PCB was successfully made with all the planned functionality.

The prototype was controlled by a modular platform called "BoomBox" which has been developed at LEI, EPFL. The BoomBox provided possibilities in easy integration of sensors, PWM modulation and control systems. The program which controlled the prototype was made with the use of UML 2.0 and was coded in C, before it was loaded on the BoomBox. All systems functioned as expected. The next step was to start testing the open loop control with the real device.
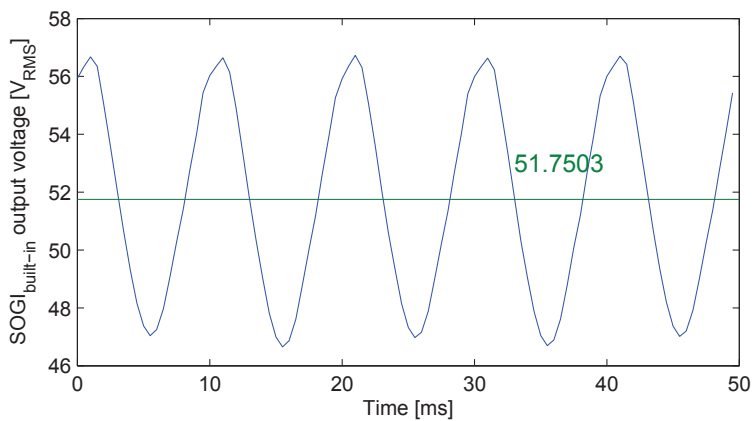
Figure 7.3.3: Real time RMS voltage output in blue from the SOGI module implementing the trigonometric method. The green line marks the average.
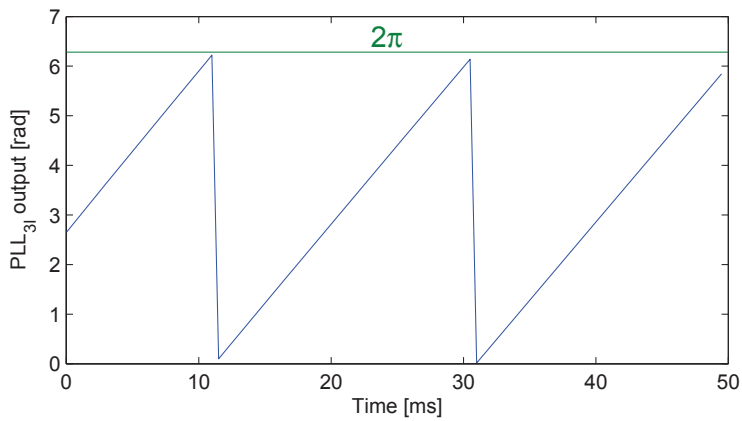
Figure 7.3.4: Phase output of the PLL using the SOGI triple integrator module. The PLL follows the phase of the input voltage well.

Chapter 8

Tuning the Performance of the AC Chopper Prototype

In the previous chapter the process of developing and testing the individual components was described. In this chapter the normal operation of the whole system will be tested. Initially the functions were tested with a resistive load. With a resistive load there is no stored energy in the system. Consequently there is less risk of component damage in case of faults. After the tests witha resistive load, the designed load impedance was added to the prototype and the the same tests were made. Problems were detected during testing. Some solutions partly solved the problems. Unfortunately for some of the cases there was no solution and the the general operation needed to be restricted.

The test setup was as follows:

- A variac was used to lower the 220V grid voltage to a maximum of 50V RMS. The variac had a 4A fuse allowing the prototype to run with a current higher than nominal.

- The designed filter was connected between the variac and the input of the converter.

- Either a resistive load or the impedance designed in earlier sections was connected to the converter output ports.

8.1   Testing with Resistive Load

A 22Ω load resistor was connected to the prototype. The applied grid voltage was slowly increased over a series of tests. The results with applied nominal voltage are presented here.
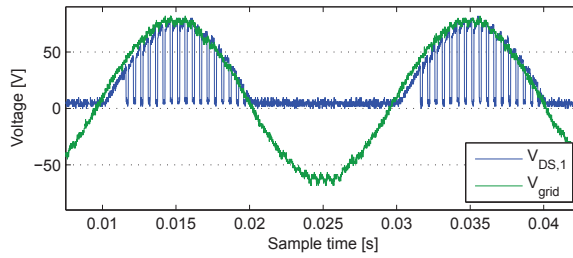
(a) Grid voltage and $V_{DS,1}$(voltage over MOSFET T_1).
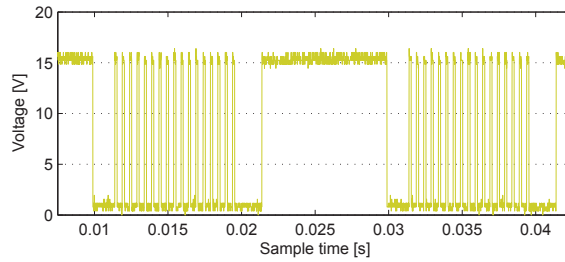
(b) Gate signal to MOSFET T_1.
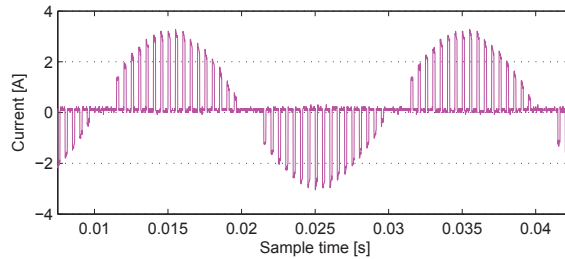
(c) Current through the resistive load.

Figure 8.1.1: Open loop control with fixed duty cycle set to 0.3 with a resistive load.

Figure 8.1.1 show the AC Chopper controlled in open loop with a fixed duty cycle of 0.3. In Fig. 8.1.1a the grid voltage of 50V RMS is shown in green and the voltage over MOSFET T_1 is shown in blue. Fig. 8.1.1b shows the gate signal to the same transistor. If the two figures are compared it shows how the positive grid voltage is blocked when the gate signal is low. The same was verified for MOSEFT T_2 during the negative voltage(not shown). The resulting current is seen in Fig. 8.1.1c.

During the negative grid voltage the MOSFET T_1 is turned on to short circuit on side of the AC Chopper circuit. As seen in Fig. 8.1.1a the voltage over the MOSFET remained zero during this period. What was more interesting was the period seen in Fig. 8.1.1b between the modulated area and the on area when the grid voltage is approaching the zero crossing. The switch remained off during this period. Hence the program successfully

sets the AC Chopper in free wheeling mode before the polarity change and resets the switching scheme after the crossing.

The length of the free wheeling period seemed to be too long from these results. The PWM signal generation seems to stop just before the zero crossing, on the other hand the free wheeling period stretch on for a long time after the zero crossing. This was because the program only tested the threshold voltage against the absolute value of the grid voltage. This was later changed to a more intelligent system that had different threshold voltages for the scenarios before and after the zero crossing. This system was described in earlier chapters and is also seen in the switching state machine diagram in App. D. Therefore, the remaining test results show tests done with a smaller free wheeling period.

The next step in testing was to apply a sinusoidally varying duty cycle. The same setup and control was used. The duty cycle was set to $0.2 + 0.2sin(2\pi \cdot 200 \cdot t)$.

Figure 8.1.2 show the AC Chopper controlled in open loop control with a sinusoidally varying duty cycle. In Fig. 8.1.2a the grid voltage of 50V RMS is shown in green and the voltage over MOSFET T_1 is shown in blue. The gate signal for the same MOSFET is shown in Fig. 8.1.2b. The resulting current is seen in Fig. 8.1.2c.

From the holes in the modulated area it is clear that the duty cycle is changing with time. The holes in the gate signal appeared at the same place for all periods. The duty cycle generation was therefore successfully synchronized with the grid voltage. The phase shifting of the sinusoidal part of the duty cycle also worked as planned(not shown). From the results it was concluded that the open loop control worked as planned. Therefore the testing with the designed impedance was commenced.
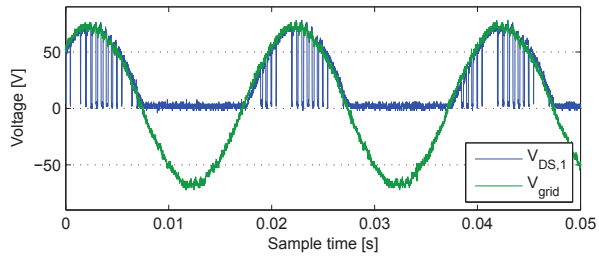
(a) Grid voltage and $V_{DS,1}$(voltage over MOSFET T_1).
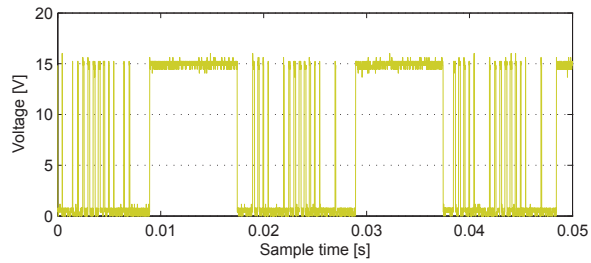
(b) Control signal to MOSFET T_1.
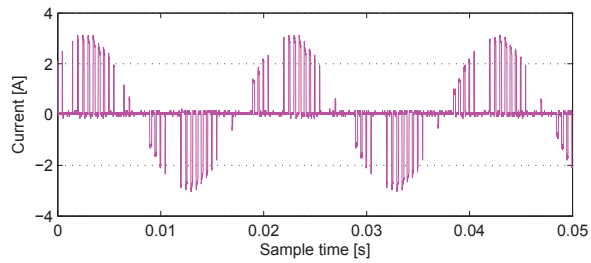
(c) Current through the resistive load.

Figure 8.1.2: Open loop control with a fixed duty cycle = 0.2 with a superimposed sinus of $0.2\sin(2\pi \cdot 200 \cdot t)$ with a resistive load.

8.2   Testing with the Designed Impedance

The time had come for testing with the designed impedance and to show if open loop control worked as desired for the planned operating conditions. The tests were done at low grid voltage values at first and slowly increased to full voltage. The tests done at approximately half of the nominal voltage are shown here. The test setup stayed unchanged.
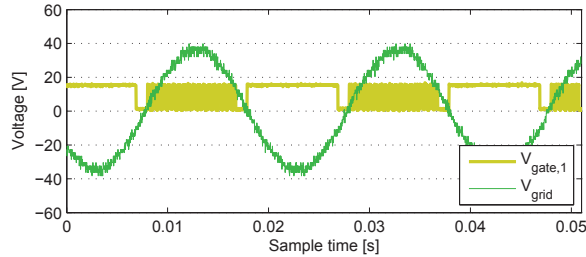
(a) Grid voltage and gate signal for the switch T_1.
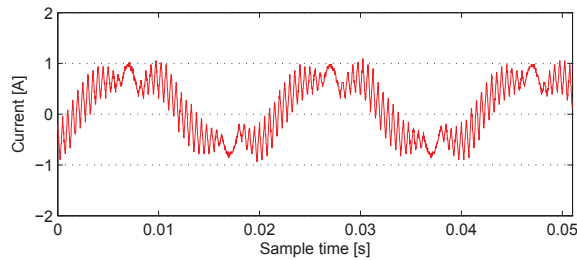
(b) The current running through the device impedance.

Figure 8.2.1: Perturbation of the impedance current during open loop control with the designed impedance for a fixed duty cycle = 0.5 . The grid voltage was measured to 25.6V RMS. The PWM frequency was set to 2kHz. The free wheeling period had been minimized, but still gave a perturbation to the impedance current.

Figure 8.2.1 show results from running the prototype at fixed duty cycle of 0.5. In Fig. 8.2.1a the grid voltage is shown in green and the gate signal for the MOSFET T_1 is shown in yellow. The resulting impedance current is seen in Fig. 8.2.1b.

A dominant 50Hz component of the current was identified from Fig. 8.2.1b. The current is clearly leading with almost 90°as was expected from the highly capacitive impedance. Superimposed on this fundamental current is the 2kHz switching ripple. The non-linearities appearing on the current during the grid voltage zero crossing and is the result of the free wheeling period. This was not foreseen in simulation, since the control system in simulation could change instantly according to the grid voltage polarity.

The duty cycle was increased to 0.9. The impedance current is shown in Fig.8.2.2. As with

Buck converters, the switching ripple for the AC Chopper is the largest for a duty cycle of 0.5. The ripple seen in Fig 8.2.2 had decreased compared to the test with $D = 0.5$ in Fig. 8.2.1b. The opposite seemed to be the case for the phenomena during the free wheeling period, which seemed to worsen with the higher duty cycle. In Fig. 8.2.2 the amplitude of the non-linearity at zero-crossing increased.
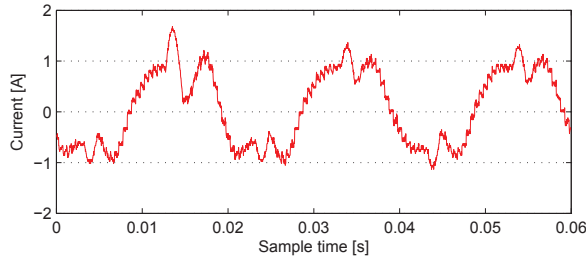
Figure 8.2.2: Perturbation of the impedance current during open loop control with the designed impedance for a fixed duty cycle of 0.9. With the higher duty cycle the fundamental component of the current became more distorted and the switching ripple decreased.

Another phenomena during testing that needed to be commented on was the noise. It was impossible to document the noise for this report, but the user of the AC Chopper could clearly identify the noise made by the device. Bystanders in the test environment also commented on the noise coming from the device. It noise came from the impedance inductor and was caused by the wire turns vibrating with the frequency of the current. The noise increased with increasing duty cycle.

The non-linear phenomena during the free wheeling period was a concern since it lead to current harmonics and it was unknown how it would affect closed loop control. Measures were tried implemented to decrease the length of the the free wheeling period. Without changing the hardware or reprogramming the hardware of the BoomBox, the only choice was to increase the switching frequency. As explained in Section 7.3.4 regarding safe switching, the PWM period was the single most important factor for the length of the free wheeling period. The frequency was increased to 6.9kHz, for which the program running on the BoomBox would still run without making changes.

Figure 8.2.3 show the gate signal for MOSFET T_1, the grid voltage and the resulting impedance current. The duty cycle was set to 0.5 so it could be directly comparable with Fig. 8.2.1. With the increased switching frequency both the switching ripple and the free wheeling period became smaller, and both these results were as expected. The increased switching frequency gave a better performance. The non-linearity decreased to significantly and the noise made by the prototype decreased drastically. Therefore the elevated PWM frequency was kept in further operation.
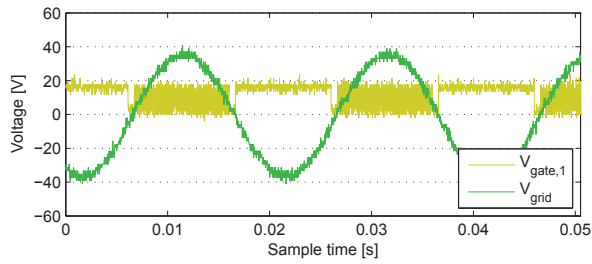
(a) Grid voltage and gate signal for the MOSFET T_1 with a PWM frequency of 6.9kHz.
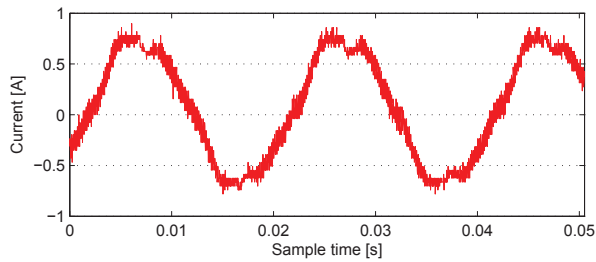
(b) The current running through the device impedance with a PWM frequency of 6.9kHz.

Figure 8.2.3: Dampening the perturbation of the impedance current by raising the PWM frequency. A fixed duty cycle of 0.5 was applied. The grid voltage was measured to 19.6V RMS. The PWM frequency was increased to 6.9kHz. With the increased frequency the free wheeling period was visibly smaller.

8.3 Commutation Problem at High Duty Cycle

During testing of the open loop behavior of the prototype another problem was discovered. This problem only occurred at duty cycles very close to or equal to 1.0 and is shown in Fig. 8.3.1.
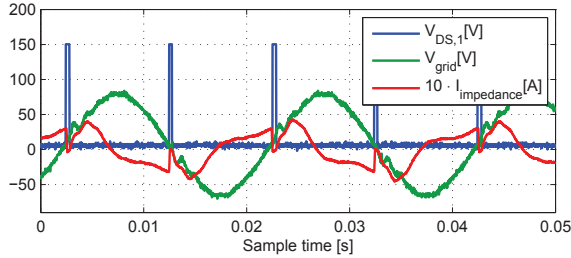
(a) Grid voltage, MOSFET voltage for MOSFET T_1 and the impedance current.
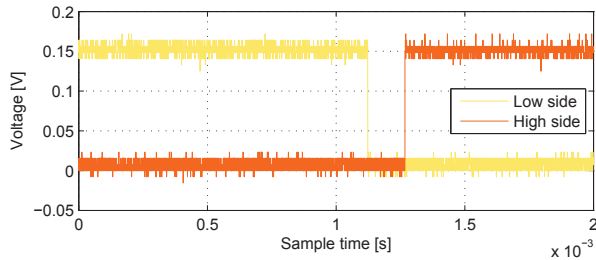
(b) The control output signals of the 4th PWM pair of the BoomBox (high side and low side) of which one controlled the switch T_{2c}.

Figure 8.3.1: Commutation problem for open loop control with a fixed duty cycle of 1.0. The grid voltage was measured to 50.5V RMS. The PWM frequency was set to 6.9kHz. A large voltage overshoot was observed for this duty cycle. The cause was within the BoomBox, as the free wheeling path was closed. The free wheeling path switches, e.g. switch T_{2c}, were turned off for exactly one PWM period(time between rise and fall is 144us, which is the same as 1/6.9kHz).

Every time the grid voltage did a zero crossing a huge voltage overshoot was registered over the T_1 MOSFET as seen in Fig. 8.3.1a. The amplitude of the overshoots were of the same height for each peak at approximately 150V. The reason for these overshoots was that all paths for the impedance current were closed. The overvoltage turned the varistor 'on' and the energy was burned off.

The cause of the blocking of the current paths were found to be within the BoomBox. To describe the fault a small technical explanation of the BoomBox must be presented. The BoomBox PWM modules come in pairs since to serve a transistor bridge(a common setup). From the PWM pair, one signal is sent to the high side transistor and one signal is sent to the low side transistor. Such a pair of transistors make up a switching cell where

both transistors being either on or off are illegal setups. So when one side is switched off the other side is switched on, only delayed from each other with a dead time set by the user. Both sides of a pair can be turned off if a specific command is explicitly called.

In Fig. 8.3.1b the output of the PWM pair supplying the MOSFET T_{2c} is shown. It shows that the signals for both high side and low side were shut off for a whole switching period, even though the command for this was not used in the program code. This phenomena only occurred when the AC Chopper duty cycle was set close or equal to 1.0. The fault seemed to come from the within BoomBox itself. The fault was not fixed due to time issues. Instead the duty cycle was limited to values below 0.9.

8.4   Filter Current

The filter was also investigated. The filter current was registered with the AC Chopper operating at no-load(duty cycle = 0). The result is shown in Fig. 8.4.1.
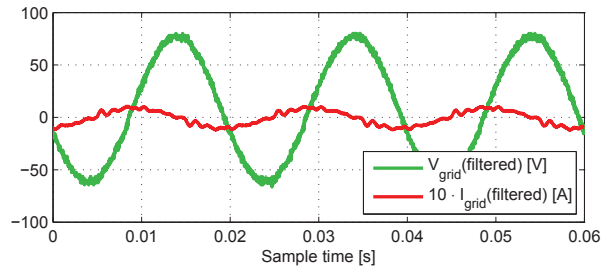
(a) Real time voltage and current for the input filter.
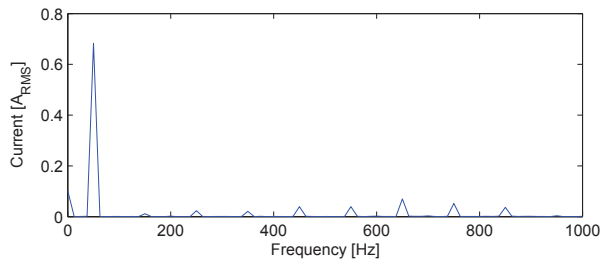
(b) FFT of the filter current. Some harmonic content was observed.

Figure 8.4.1: Input filter voltage and current at no-load condition. The current is the reactive current provided by the filter plus the small current going through the voltage sensor on the PCB.

The frequency spectrum of the filter current is shown in Fig. 8.4.1b. The fundamental current was measured to $0.683 A_{RMS}$. In addition several other harmonics are visible. It

is unknown if these harmonics are produced by the filter inductor, the variac or a combination of the two. The fundamental value must be deducted from later results to remove the filter as a perturbation for other experiments. Regarding the harmonics, the phase shift of the harmonics were not taken into account, so the amplitude cannot be subtracted directly from later results.

8.5   Chapter Conclusion

In this chapter the behavior of the complete prototype system was tested. In general the system worked as planned and the prototype works in open loop control. Unfortunately, the testing process revealed some unforeseen effects that had to be dealt with.

The free wheeling period was not included in simulations, hence the effect of this period on the open loop behavior was unexpected. To tackle this non-linearity the PWM frequency was increased. Consequently the effect was significantly reduced in the open loop behavior. In addition, the switching ripple was also decreased. Another problem that was discovered was an unknown fault within BoomBox which lead to unwanted behavior at high duty cycles. As a result the maximum applicable duty cycle for the prototype was limited to 0.9.

Lastly, the filter current at no-load condition was measured. The FFT result shows that some harmonic currents were produced. These harmonics must be taken into account for later results.

Chapter 9

Open Loop Control of the AC Chopper Prototype

In this chapter the measured performance of the prototype AC Chopper is presented. The test setup was unchanged from last chapter, except the grid voltage was set to nominal value at around 50V RMS. The PWM frequency was set to 6.9kHz.

Two tests are presented here. The first test shows the open loop control with a static duty cycle. The second test shows the open loop control with a sinusoidally varying duty cycle. The experiments were done with the same method as in Section 5.2 when a single sine wave was superimposed on a static duty cycle. For both tests the real time voltages and current of the input(filter) and the output(impedance) are shown. The results are also presented in frequency domain to facilitate the analysis of the harmonic content.

9.1 Test with Static Duty Cycle

For the static duty cycle test the duty cycle was set to 0.8. The results are shown in Fig. 9.1.1. The voltages and currents are highly regular with a frequency of 50Hz. The only identifiable irregularity is seen on both the currents after the grid voltage zero crossing. The small oscillation seen in Fig. 9.1.1a was measured to about 1000Hz, hence it originates from the filter. The non-linearity seen in the former chapter regarding the free wheeling period seemed to excite the resonance frequency of the input filter. As seen on the impedance side in Fig. 9.1.1b this grid side perturbation is carried over to the impedance side in the shape of a small oscillation on both the current and the voltage.
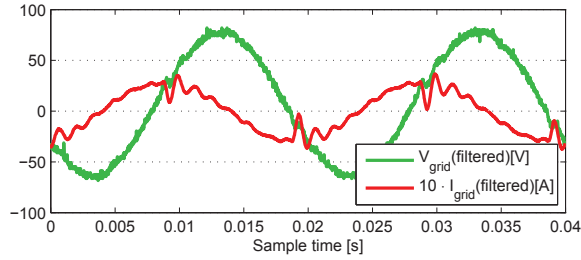
(a) Grid voltage and current.
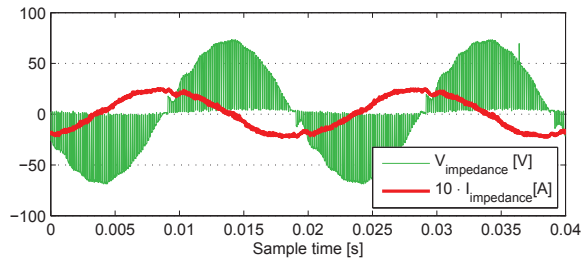
(b) Impedance voltage and current.

Figure 9.1.1: Results of the experiment with open loop control with a fixed duty cycle set to 0.8. The grid voltage was measured to 50.5V RMS. The PWM frequency was set to 6.9kHz. The results are very similar to the simulation results with open loop control.

The grid and impedance voltages are not shown in frequency domain as they appear strictly 50Hz in the real time figures. The FFT of the grid and the impedance currents are shown in Fig. 9.1.2. For both the grid and the impedance side the current is mostly consisting of the 50Hz fundamental. Correcting for the filter current, the amplitude of the currents correlated well with the basic relation (Eq. 2.3.1) for the AC Chopper. The small harmonic content on the impedance side seen in Fig. 9.1.2b is assumed to be produced by the impedance inductor due to physical properties of the component. The grid side current contains more harmonic content than the impedance side. Part of these harmonics are produced by the filter itself, however more lower order harmonics were observed than for the no-load test of the filter(Fig. 8.4.1).
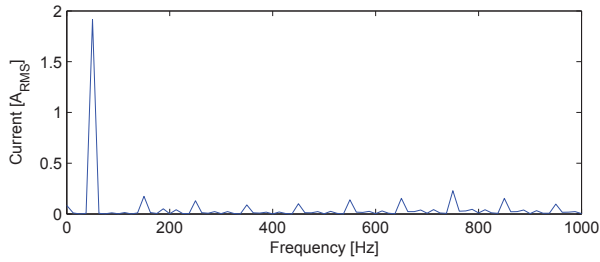
(a) FFT of the grid current.
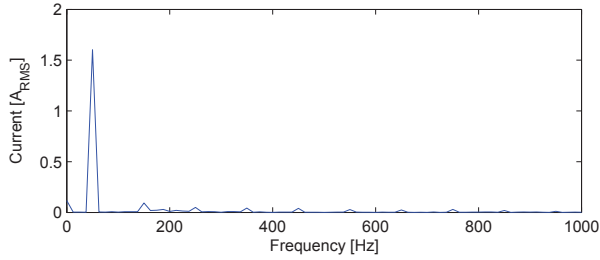
(b) FFt of the impedance current.

Figure 9.1.2: FFT of the results of the experiments with open loop control with a fixed duty cycle set to 0.8. The grid voltage was measured to 50.5V RMS. The PWM freq was set to 6.9kHz. The frequency spectrum shows that the fundamental component is dominant.

The harmonic content is undesired from an operator point of view. Nevertheless the test setup was not ruled out as a source of the harmonics, hence it is unknown if this characteristic is intrinsic to the converter. Components of higher quality mmight the resolve the harmonic issue.

As mentioned earlier in Sec. 6, a new paper regarding control of the AC Chopper was found at the time of writing of this report[34]. When looking at the results from their prototype testing, a small ripple can be seen on the current wave for each time the grid voltage changes polarity. This shows that this phenomena is not local to the prototype for the present project, but rather a behavior that must be addressed in all realizations of the AC Chopper.

9.2 Test with Variable Duty Cycle

In chapter 5.2 it was shown in simulation that harmonics could be made in pairs with the AC Chopper. Now the test would be reproduced on the prototype. The static duty cycle was set to 0.5. The frequency of the sinusoidal part of the duty cycle was set to 700Hz. This frequency was far from the resonance frequency of the impedance and at the same time a margin to the resonance frequency of the input filter was kept.
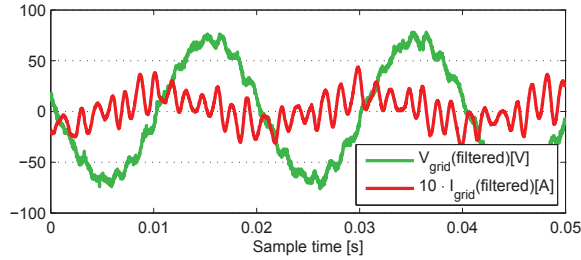
(a) Grid voltage and current.
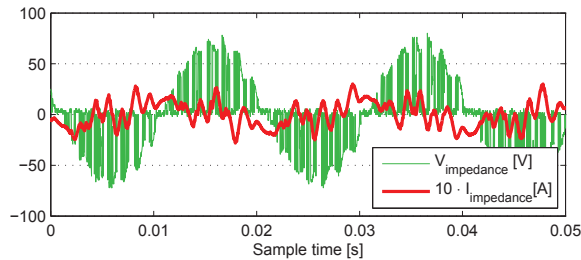
(b) Impedance voltage and current.

Figure 9.2.1: Results of the experiment with open loop control with a fixed duty cycle of 0.5 and a variable duty cycle of $0.5\sin(2\pi \cdot 700 \cdot t + 0)$. Grid voltage was measured to 50.0V RMS. The PWM frequency was set to 6.9kHz.

The real time voltages and currents are shown in Fig. 9.2.1. The FFT of these signals is found in Fig. 9.2.2. Figure 9.2.2a shows that the grid voltage consists dominantly of the 50Hz component. Some small harmonics are found around 650Hz. The voltage harmonic is a consequence of the harmonic current seen in Fig. 9.2.2b. Except for the 50Hz component, there are three relatively large current peaks at 550, 650 and 750Hz. The two last peaks were expected due to the duty cycle. However, the origin of the first peak remains a mystery. There is no resonance frequency or input signal that exist around the the 550Hz.

As seen in Fig. 9.2.2c the impedance voltage contains three voltage peaks . Two of the peaks are at 650 and 750Hz which is expected from duty cycle containing the 700Hz component. The peak at 550Hz probably originates from the 550Hz grid current. The

50Hz component is less than half of the 50Hz component of the grid, which is less than expected with a static duty cycle of 0.5. The voltage peaks seen at 650 and 750Hz produces impedance currents at the same frequencies. There are also a reasonable amount of lower order harmonic currents with peaks at 150, 250 and 350Hz. These low order harmonics are most probably a result of non-linearities of the impedance inductor e.g. magnetic saturation of the inductor core.

In simulation the focus was mainly on the results on the impedance side of the AC Chopper circuit, since it was the first step in closed loop control. In addition the linear relation between input, output and the duty cycle made the control system easy to implement. However, the results in Fig 9.2.2 turned the situation around. With a static duty cycle, the impedance current contained very little harmonic content. On the other hand, with a varying duty cycle several resonances outside the duty cycle scope were excited. Consequently, the closed loop would be very difficult to implement. Simulation has shown that the control system would produce small oscillations. On the other hand the results from the open loop control showed that a varying duty cycle would excite several resonances. It was therefore decided not to continue with closed loop control of the prototype as was planned. It was decided that open loop behavior needed to be improved before closed loop control could be handled.

9.3 Chapter Conclusion

In this chapter the results of the open loop control of the prototype have been presented.

The first test with static duty cycle shows that a stable state with few harmonics was achieved. The results correlate well with the theoretic relations. The only negative point was that the input filter resonance frequency was excited due to the free wheeling mode.

In the second test a sinusoidal duty cycle was feed to the prototype. The results differed in some ways from the expectations. The harmonics that were tried produced with the sinusoidal duty cycle were clearly visible on both the grid and the impedance side. Nevertheless, other non-trivial harmonics were also present, especially in the lower frequency domain on the impedance side. Some of these harmonics could not be accounted for. Even though the prototype was able to produce the desired peaks, the addition of other significant peaks arguments against the use the AC Chopper as an harmonic current source.

Consequently, the problems with the open loop behavior with a sinusoidal duty cycle led to a decision to not go on with closed loop control of the prototype.
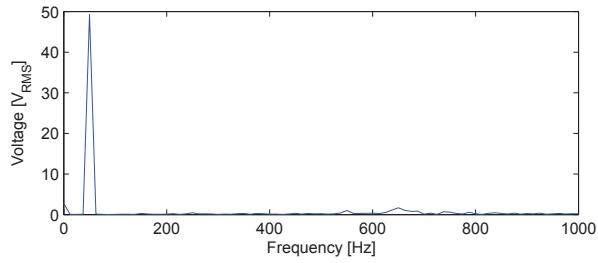
(a) FFT of the grid voltage.
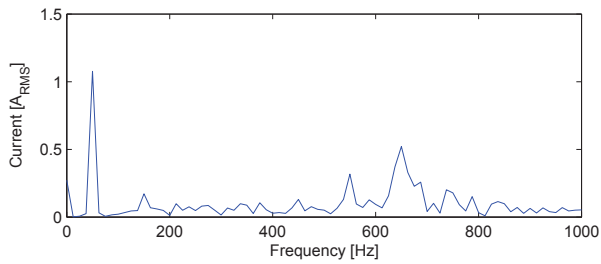
(b) FFT of the grid current.
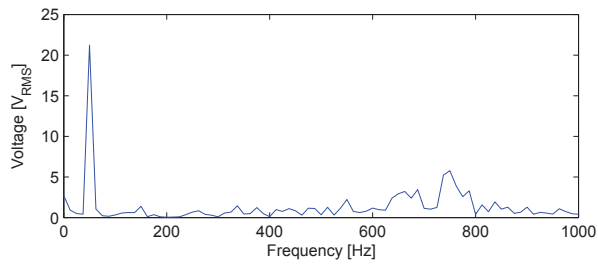
(c) FFT of the impedance voltage.
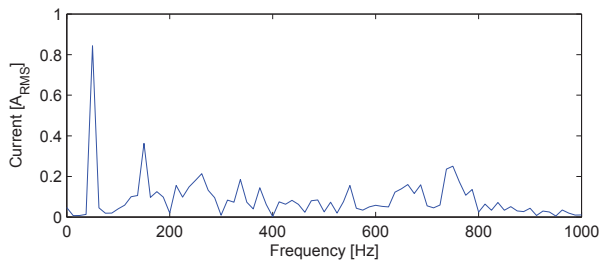
(d) FFT of the impedance current.

Figure 9.2.2: FFT of the tesults of the experiment with open loop control with a fixed duty cycle of 0.5 and a variable duty cycle of $0.5\sin(2\pi \cdot 700 \cdot t + 0)$. The grid voltage was measured to 50.0V RMS. The PWM frequency was set to 6.9kHz.

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Chapter 10

Final Remarks on the AC Chopper and Conclusion

Most of the report has been dedicated to technical aspects of the AC Chopper regarding the circuit behavior, designing of a suitable controller and the realization of a prototype. In this chapter, the strengths and weaknesses regarding the practical issues are discussed. These issues have not been found suitable to be included in earlier chapters and are therefore treated here in the final chapter. Following the discussion of these issues, the final conclusion for the current project is drawn.

10.1 Practical Sides of the AC Chopper

Early in the report the competing technologies were presented. For the AC Chopper to have a future, it must present some real advantages compared to the current or near-future technology. In this section, such advantages or the lack thereof will be discussed. The AC Chopper is compared to the VSI because this topology has been researched extensively and is widely used today. This is the technology to beat if the AC Chopper were to enter the market today. Four practical issues will be discussed: higher efficiency, consequences of component technology, multiple phases and resonance frequencies.

10.1.1 Higher Efficiency

It was mentioned in the introduction that the AC Chopper promises a better efficiency than the VSI solution. This is a statement taken from the work done at the University of Toulouse[14]. A simulation on reactive compensation and device losses was done for three converter topologies, from which the result of two of the topologies are presented in Table 10.1.1. The compared topologies are the AC Chopper and the VSI.

The two different topologies produce the same amount of reactive power with the same voltage and current. The carrier frequency for all cases is 4kHz, resulting in a 2kHz operation for each half-bridge of the VSIs and a 4kHz operation for the AC Chopper. The AC Chopper shows a slightly better efficiency than the VSI solutions. As the results show, the conduction losses are the same and the improved efficiency is due to the lower switching losses for the AC Chopper in spite of a higher switching frequency. There are two reasons for the improved efficiency. The first reason is the switching pattern of the AC Chopper, where only one switch is used in the modulation. The second reason is that the AC Chopper operates with soft switching since the input voltage varies, while the VSI switches with full voltage at times.

Table 10.1.1: Comparision of losses for 333kVAR reactive compensation [14]

	AC Chopper	VSI	Units
U_{conv}	500	500	V
I_{conv}	667	667	A
f_{sw}	4k	2k	Hz
$P_{conduction}$	2140	2140	W
$P_{switching}$	446	840	W
P_{total}	2.59	2.98	kW
$Q_{H-brdg.}$	333	333	kVAR
η	99.23	99.11	%

10.1.2   Consequences of Component Technology

In an article from the same team at the University of Toulouse, it is argued that the AC Chopper consist of less expensive passive components than the VSI[14]. The argument is based on the calculated stored energy in the passive components as a general indicator of price, with lower values being less expensive. The capacitance of the AC Chopper is considerably smaller than the VSI due to the nature of the two topologies(roughly one sixth). While this argument is considered to be true for elements of the same technology, it does not hold for passive elements of different technologies.

The capacitor of the AC Chopper device impedance is subjected to an AC voltage while the VSI capacitor works with DC voltages. The consequence for the AC Chopper is that electrolytic capacitors cannot be used. An option is film based capacitors, which compared to electrolytic capacitors, are several times more expensive and more voluminous for the same capacitance value. As for the volume difference an example is shown in Fig. 10.1.1. In this figure, the film capacitors used for the prototype are compared to a electrolytic capacitor of similar rating.

The film capacitors have a much higher voltage rating (1000 vs. 630VDC) and most probably a higher current rating which must be accounted for. Still the electrolytic ca-

Figure 10.1.1: Comparision of volume between electrolytic and film capacitors. Left: Electrolytic, 330μF, 630VDC. Right: Film, 2·66μF 1000VDC.

pacitor has double the capacitance value of the two film capacitors combined in parallel setup.

Consequently, even though the stored energy in the AC Chopper is reduced, the expected price and volume of the whole device is expected to be higher than for the VSI. At the same time, the AC Chopper is expected to be more reliable. Electrolytic caps are known as being the least reliable component in a power electronic device, and the capacitor life time has a certain correlation with the current ripple to which it is subjected. With a film capacitor the device life time is potentially longer. The question remains if the higher reliability and slightly higher efficiency make up for the elevated cost and increased device volume.

10.1.3   Multiple Phases

For the final price of a converter, the number of component plays has a certain influence. In this report only single phase topologies have been depicted and the topologies are similar in regards to the amount of semi-conductors and passive components. However, some attention should be made to the three phase setup as well, since most grid and high power applications concern three phase systems.

Where the VSI can share its DC capacitor for all three phases, the AC Chopper can not share its passive elements. Hence, the number of components are multiplied by three for a three phase system. In total that makes 12 transistors, 12 diodes, 3 input filters and 3 impedances (6 inductors and 6 capacitors) for the AC Chopper, compared to 6 transistors, 6 diodes, one input filter, one switching inductor and one DC capacitor for the VSI. The difference in the number of components is notable. It is therefore concluded that the AC Chopper is better used for single phase systems.

10.1.4 Two Resonance Frequencies

For all of the previously mentioned power converters it is common to add an input filter to minimize the injected harmonics to grid. For quick and stable control of such systems the control must be designed to dampen the resonance frequency of the input filter[20]. As for the AC Chopper there are two resonance frequencies present: the input filter and the device impedance. Another resonance frequency implies that the controller must be able to dampen two frequencies, thus increasing the complexity of the controller and the system in general.

10.2   Final Conclusion

The final conclusion will answer the problem definition posted at the start of the report based on the findings of the project that have been presented.

A reason for the results that dispute the basic relation has not been found. Rather a reasoning has been made to justify the validity of the original relation. But this point is of lesser importance, since the FFT results showed that the basic relation was valid for the fundamental wave. This implies that as long as it is the fundamental wave which is in question (RMS or peak value), the relation holds.

Extensive simulation was done in both open and closed loop control. The open loop behavior shows that for any single frequency signal in the duty cycle going to the AC Chopper, a voltage of at least two frequencies will be produced at the output. This intrinsic behavior originates from the AC Chopper having a sinusoidal input voltage. Hence, using the AC Chopper to produce a certain set of harmonics is very difficult or even impossible. If a task requires that harmonics are produced in pairs, then a possibility exists for using the AC Chopper as an active filter. For all other uses, the results of this report concludes that it is not to be encouraged.

The closed loop control of the impedance current was seen as a first step to controlling the injected grid current, with the desired end goal of creating reactive compensation device. The solution of controlling the RMS value of the impedance current did not give good results. Usually controllers give better results when the speed and bandwidth is increased. The results from simulation had the opposite trend than normal. The control system worked at its best when it was slowed down and filters were included to dampen the harmonics. The consequence was that the step response was slowed down while the ripple on the steady state current was almost eliminated. Still, it was concluded that the open loop control might be a better option, since the open loop results show a high precision between theoretic relation and measured relation between input and output values.

An improved closed loop control is shown in a recently published paper on the AC Chopper[34]. In the paper a control system based on dq-reference frame is suggested, simulated and implemented with good results. This indicates that a different control system than the one developed in this project may give better results.

In the present study, a prototype for the AC Chopper was developed and implemented. The design, programming and manufacturing process have been described in detail. Standard methods and commonly implemented guidelines were used. Despite certain technical challenges, the results demonstrate that the prototype was able to successfully reproduce open loop control. Unfortunately, the challenges imposed by the hardware led to certain limitations which restricted the testing possibilities. The challenges related to the physical implementation show that the real performance of the AC Chopper will be decreased compared to the performance that is obtained in simulation. This is common for most technical equipment, but it implies that the results in simulation must be better with a margin compared to other devices to be able to compete.

When the traits and possibilities of the AC Chopper are compared to that of the VSI, the VSI is deemed to be the better option. Even though the AC Chopper is expected to have a slightly higher efficiency, there are many other negative points related to the topology. Expensive components, more components needed for three phase systems and less controllability of the device output are three important issues that have to be countered by the elevated efficiency. As such the final conclusion of this report is that the AC Chopper is not suited for active filtering nor is it recommended for three phase systems.

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Appendix A

PWM Signal Generation

The PWM unit tranlates a duty cycle signal to the actual switching signals fed to the driver circuits for the induvidual switches. The PWM signal contains the switching pattern i.e. the information about whether a switch should be turned on or off at any given moment. A duty cycle is defined as the ratio between the time the converter is turned on and the switching period, $D = \frac{t_{on}}{T_{sw}}$.

The translation between these two signals is made with a carrier signal, u_c, and a comparator. The carrier signal is a triangular wave with a frequency equal to the switching frequency and an amplitude of $\hat{U}_c$. The triangular form of the carrier signal was used since it produces the lowest average latency [5]. The carrier signal is compared to the duty cycle signal and outputs a logic signal. The logic output signal has two possible states: logic high or logic low.

The two signals are compared with the logic expression $u_d > u_c$. If D is higher than the carrier signal u_c then the PWM block outputes a logic high. If D is lower than the carrier signal u_c then the PWM block outputs a logic low. The input signals and the resulting output voltage is shown in Fig. A.0.1.

A.0.1 Transistor Switching Signals

To implement the switching strategy from Section 2.2 a logic ciruit must be implemented. The control signals for each of the four switches are based on two input signals: the PWM signal described above and the input voltage polarity. The switching cell behaviour varies between T_1/T_{1c} and T_2/T_{2c} according to the polarity of the input voltage. A logic circuit must be designed that implements this behavior. The output states based on the input signals are summed up in Table A.0.1.

An optimal logic circuit to translate these states into the correct switching signals was designed. The logic circuit is portrayed in Fig. A.0.2.
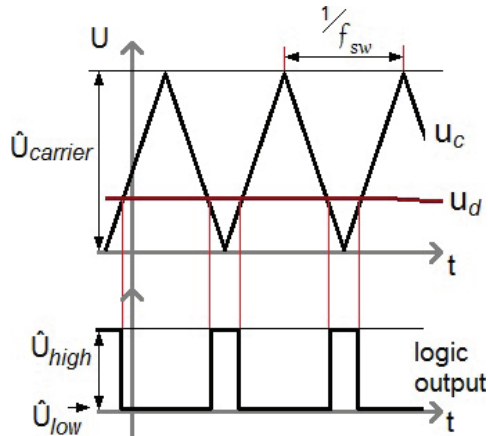
Figure A.0.1: PWM signal generation. The two input signals: the carrier signal and the duty cycle are shown on top. The resulting output signal is shown at the bottom half. The two possible output levels of the PWM block are logic high and logic low.

Table A.0.1: Switch states for the transistor switches(T_1, T_{1c}, T_2, T_{2c}) according to input voltage polarity and the PWM signal state. Logic low is noted as 0 while logic high is noted as 1. For the input voltage a state of 1 equals a positive voltage polarity and the state of 0 equals a negative voltage polarity.

		PWM	
		0	1
Polarity	0	1,1,0,1	1,1,1,0
	1	0,1,1,1	1,0,1,1

Fig. A.0.3 shows the successful regulating of the individual device switches according to the grid voltage polarity and the PWM signal. When the polarity signal goes high(t = [0.24 0.27]), the right side of the device is short circuited shown by T_2 and T_{2c} going to 1. During this period T_1 and T_{1c} are switched 'on' alternately. When the polarity signal goes low the process is mirrored between the left and the right side of the device.

Figure A.0.2: Logic circuit taking three input signals to produce the turn-on and turn-off signals for the four switching devices. Only NAND-gates were used.

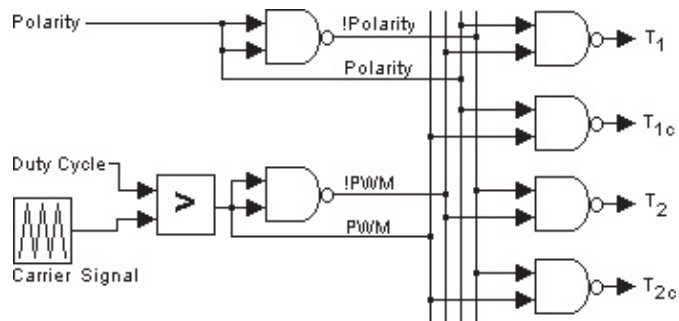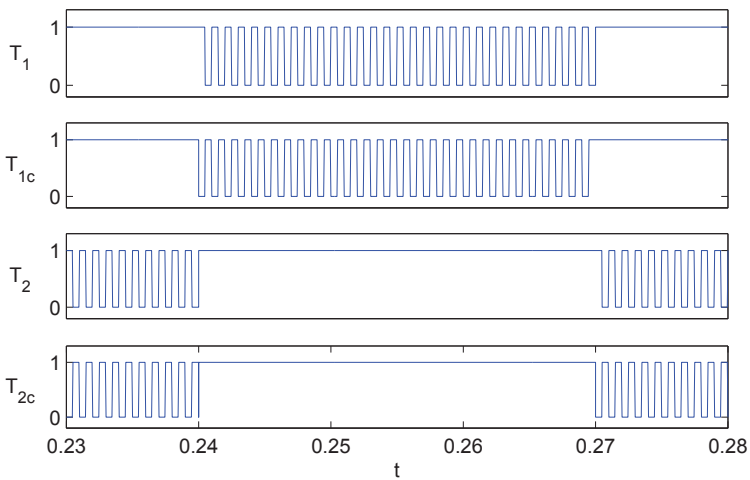Figure A.0.3: The control signals produced by the logic ciruit for a duty cycle of 0.5. Logic high is shown as 1 and logic low is shown as 0.

Appendix B

Dimensioning of the Passive Components of the AC Chopper

B.1 Device Impedance

In this section a method for selecting the right component values was taken from [1]. Two equations will be developed to select the size of L_V and C_V (seen in the circuit layout in Fig. 2.1.2).

The current ripple in the device inductor is chosen as a starting point. In freewheeling mode the device impedance is short circuited. If the resistive losses are ignored, then the voltage drop over the capacitor and the inductor are equal in value with opposite polarity. From this state the following equation can be derived [21]:

$$I_L = \frac{V_{C_V}(t)}{L}(1 - D)T_{sw} \tag{B.1.1}$$

where D is the duty cycle and T_{sw} is the switching period of the PWM unit. Further it can be shown that the maximum current ripple occurs at $D = 0.5$ and maximum input voltage. The final equation for maximum current ripple is acquired:

$$\Delta I_{OUT,max} = \frac{\sqrt{2}V_{IN}}{4L_V f_{sw}(1 - L_V C_V \omega_{net}^2)} \tag{B.1.2}$$

where V_{IN} is noted in RMS value and $f_{sw} = \frac{1}{T_{sw}}$.

As with the DC/DC Buck converter, the AC Chopper device impedance components experiences ripple effects as a result of the chopping process. The ripple effect is filtered by the input filter. However larger produced ripples necessitates a larger input filter, hence the ripple must be limited. If the current ripple rating is available at the time of the design this value can be entered into the equation. The current ripple can also be expressed as a ratio according to the maximum current of the system, noted as current ripple ratio, $K_{\Delta i}$, given in p.u [1]:

$$K_{\Delta i} = \frac{\Delta I_{LV,max}}{2\sqrt{2}I_{LV,max}} = \frac{V_{net}^2 \cdot D_{max}}{8L_S f_{SW} Q_{max}} \tag{B.1.3}$$

Another equation is needed to dimension the device impedance. For any LC circuit there exists a resonance frequency. The equation for this resonance frequency will be used here. The primary goal for the AC Chopper is to supply capacitive power to a utility grid and therefore it must be ensured that the combination of L_V and C_V in series results in a capacitive load at net frequency. In other words, the resonance frequency of the LC component must be higher than the net frequency.

$$\omega L_V - \frac{1}{\omega C_V} < 0 \implies \frac{1}{2\pi\sqrt{L_V C_V}} = f_R > f_{net} \tag{B.1.4}$$

where f_R denotes the resonance frequancy of the impedance. With Eq. (2.4.4), (B.1.2), (B.1.3), and (B.1.4) a method for dimensioning the components can be set up.

If the current ripple is defined directly, then Eq. (2.4.4) and (B.1.2) can be solved for L_V and C_V directly. To give a broader insight into possible combinations of component sizes and resulting current ripple, a graphical method is presented here.
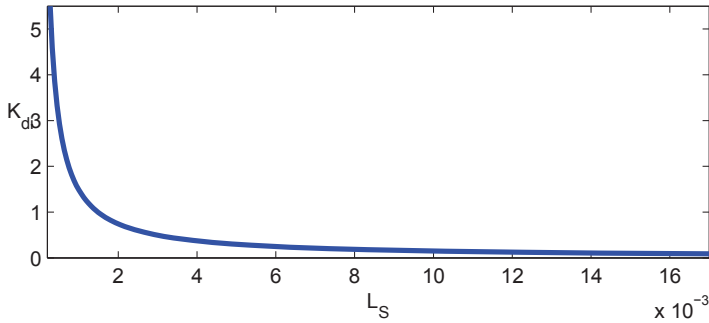

Figure B.1.1: Ration between the current ripple and maximum current as a function of inductor size.

Fig. B.1.1 shows the relation between the inductor size and the current ripple ratio as described by Eq. (B.1.3). The switching frequency was set to 2kHz. Fig. B.1.2 shows
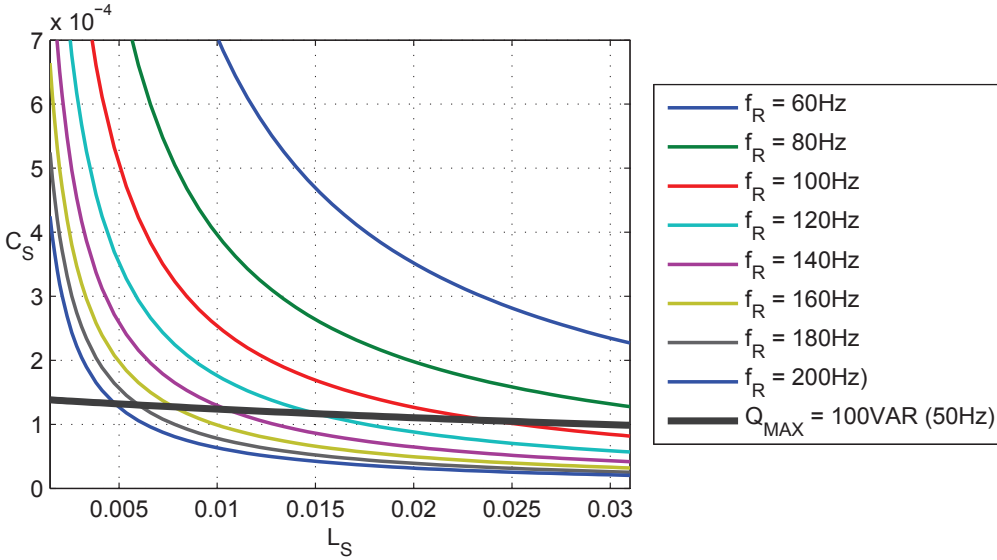
Figure B.1.2: Component size according to device impedance resonance frequency and maximum power output.

a multitude of graphs, where the thin graphs falling sharply represents component size combinations that result in a specific resonance frequency. The thick line indicates the maximum produced reactive power for a grid operating at 50Hz.

As seen in Fig. B.1.2 choosing a lower resonance frequency results in smaller component values resulting in a smaller devices. When comparing this result to Fig. B.1.1 it is apparent that choosing smaller component values leads to higher current ripple value. Thus, the final design will be a compromise between physical size and current ripple.

B.2 Input Filter

As seen in Fig. 2.2.2 the grid current appears severely chopped as a result of the converter operation. This was an unwanted effect as the chopped current represents harmonics which would be injected to the grid. Therefore an input filter was installed to filter out the switching harmonics. The dimensioning of the filter values was performed in the same manner as explained in [1]. The resonance frequency was set outside the controller bandwidth.

The filtered grid current is seen in Fig. B.2.1. The current no longer appears to be chopped. The current mostly consists of the fundamental component with a small ripple from the switching operation.
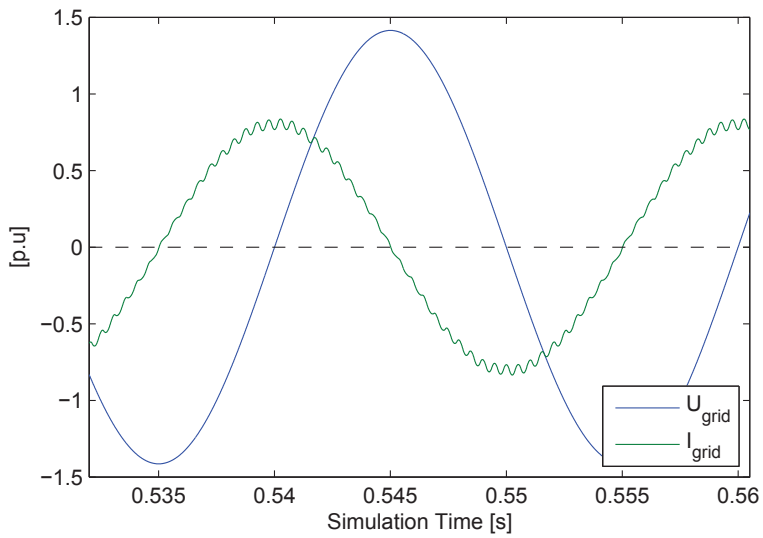
Figure B.2.1: The grid voltage and filtered grid current during an operation with duty cycle set to 0.5. The grid current is no longer chopped.

Appendix C

Analytic Calculation of the PWM-modulated Voltage RMS Value

T is the half period of the sine signal ($=\frac{1}{2f}$) and the angle speed ω equals $2 \cdot \pi f$. Two other definitions are also needed. T_s is the period of the PWM signal which is set to $T_\mathrm{s} = \frac{T}{n}$. This is done to simplify the calculation. Then duty cycle is defined as $D = \frac{t_\mathrm{on}}{T_\mathrm{s}}$ where t_on is the time the converter is turned on. Equally t_off is the time the converter is turned off. The definition of RMS value is the following:

$$f_{RMS} = \sqrt{\frac{1}{T_1 - T_2} \int_{T_2}^{T_1} f(t)^2 \, \mathrm{d}t} = \sqrt{\frac{1}{T} \int_0^T [f(t)]^2 \, \mathrm{d}t} \qquad \text{(C.0.1)}$$

For the time being we will focus on developing and solving the integral and then return to this expression. For a chopped signal the sine consist of periods where the full sine signal is applied or zero. The size of each of these periods is defined by t_on and t_off.

$$\int_0^T [f(t)]^2 \, \mathrm{d}t = \int_0^{t_\mathrm{on}} [f(t)]^2 \, \mathrm{d}t + \int_{t_\mathrm{on}}^{t_\mathrm{on}+t_\mathrm{off}} [f(t)]^2 \, \mathrm{d}t + \int_{T_\mathrm{s}}^{T_\mathrm{s}+t_\mathrm{on}} [f(t)]^2 \, \mathrm{d}t + \int_{T+t_\mathrm{on}}^{T+t_\mathrm{on}+t_\mathrm{off}} [f(t)]^2 \, \mathrm{d}t + ..$$

$$+ \int_{T_\mathrm{s}(n-1)}^{T_\mathrm{s}(n-1)+t_\mathrm{on}} [f(t)]^2 \, \mathrm{d}t + \int_{T_\mathrm{s}(n-1)+t_\mathrm{on}}^{T_\mathrm{s}(n-1)+t_\mathrm{on}+t_\mathrm{off}} [f(t)]^2 \, \mathrm{d}t \qquad \text{(C.0.2)}$$

During t_off the signal $f(t)$ is equal to 0. During t_on the signal $f(t)$ is equal to the input sine which is defined as

$$f(t) = a \cdot \sin(\omega t) \qquad (C.0.3)$$

The integral is cleaned up:

$$\int_0^T [f(t)]^2 \, dt = \int_0^{t_{on}} [a \cdot \sin(\omega t)]^2 \, dt + \int_{T_s}^{T_s+t_{on}} [a \cdot \sin(\omega t)]^2 \, dt + .. + \int_{T_s(n-1)}^{T_s(n-1)+t_{on}} [a \cdot \sin(\omega t)]^2 \, dt$$

$$= \int_0^{t_{on}} a^2 \cdot \sin^2(\omega t) \, dt + \int_{T_s}^{T_s+t_{on}} a^2 \cdot \sin^2(\omega t) \, dt + .. + \int_{T_s(n-1)}^{T_s(n-1)+t_{on}} a^2 \cdot \sin^2(\omega t) \, dt$$

$$(C.0.4)$$

The integral is solved

$$\int_0^T [f(t)]^2 \, dt = a^2 \left\{ \frac{t_{on}}{2} - \frac{1}{4\omega} \sin(2\omega t_{on}) - \frac{0}{2} + \frac{1}{4\omega} \sin(2\omega \cdot 0) \right.$$

$$+ \frac{T_s + t_{on}}{2} - \frac{1}{4\omega} \sin(2\omega[T_s + t_{on}]) - \frac{T_s}{2} + \frac{1}{4\omega} \sin(2\omega T_s)$$

$$+ \frac{2T_s + t_{on}}{2} - \frac{1}{4\omega} \sin(2\omega[2T_s + t_{on}]) - \frac{2T_s}{2} + \frac{1}{4\omega} \sin(2\omega 2T_s) + ...$$

$$+ \frac{(n-1)T_s + t_{on}}{2} - \frac{1}{4\omega} \sin(2\omega[(n-1)T_s + t_{on}]) - \frac{(n-1)T_s}{2} + \frac{1}{4\omega} \sin(2\omega[n-1]T_s)$$

$$= a^2 \sum_{k=0}^{n-1} \left\{ \frac{t_{on}}{2} - \frac{1}{4\omega} \sin(2\omega[kT_s + t_{on}]) + \frac{1}{4\omega} \sin(2\omega kT_s) \right\} \quad (C.0.5)$$

The induvidual sum of the two sine components inside the sum becomes zero. This is derived from that the integral of a sine over a full period equals zero. In Eq. C.0.5 the values of the sines are summed over a full period, so these expressions are evaluated to zero. This is shown graphically in Fig. C.0.1. If the result is inserted in the full expression for the RMS value the final result is achieved (using the definitions $T = nT_s$ and $t_{on} = D \cdot T_s$).

$$\text{RMS value} = \sqrt{\frac{1}{T} a^2 \sum_{k=0}^{n-1} \frac{t_{on}}{2}} = \sqrt{\frac{a^2}{T} \frac{n \cdot t_{on}}{2}} = \sqrt{\frac{a^2}{T} \frac{D \cdot T}{2}} = \frac{a}{\sqrt{2}} \cdot \sqrt{D} \quad (C.0.6)$$
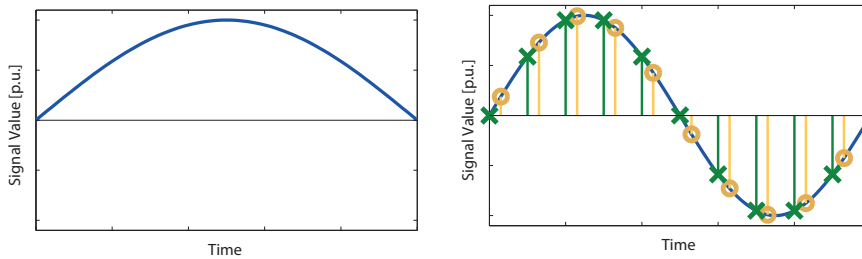
Figure C.0.1: Graphical explanation showing that the sum of each individual sine component becomes zero. The angle speed of the two sine components is the double of the speed of the input sine signal. To the left is the input sine and to the right is a sine of double speed for an example of n = 10 and d = 0.3. The y and x-axes are omitted to show that the effect holds for all values. The values of the two sine components are shown with makers(circle for the first component and crosses for the second component). Because of symmetry the sum of each component becomes zero, and the components are eliminated from the expression.

Appendix D

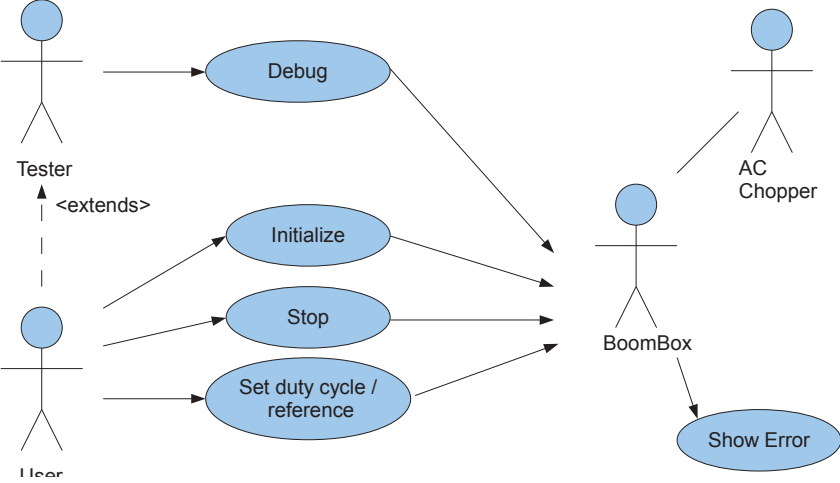# UML Diagrams

D.1 Use Cases

Figure D.1.1: Use Case diagram for the AC Chopper prototype.
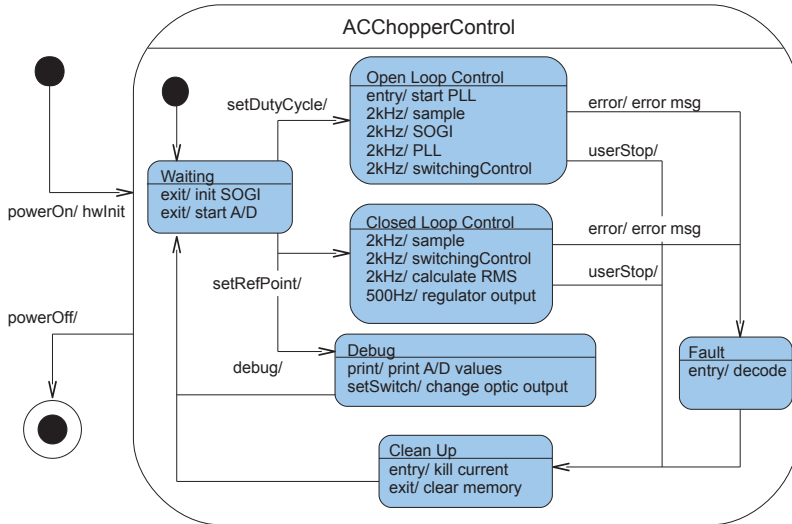
D.2 State Machine Diagrams

Figure D.2.1: State machine diagram describing the possible states and transitions of the prototype program running on the BoomBox.
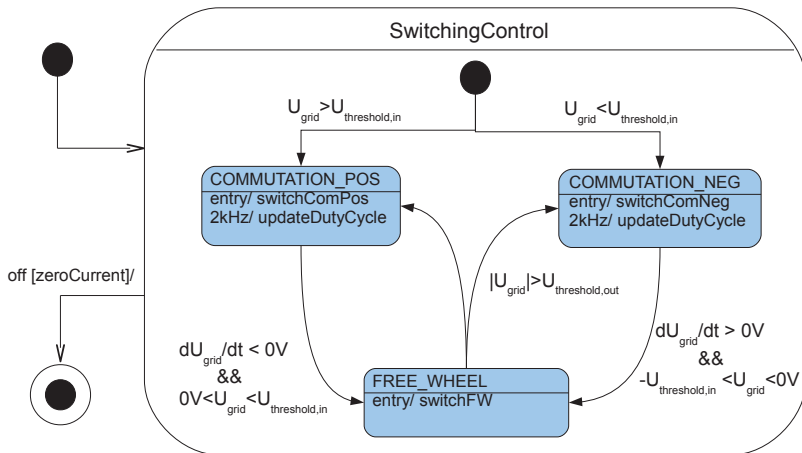

Figure D.2.2: State machine diagram showing the possible switching states and the transition variables.
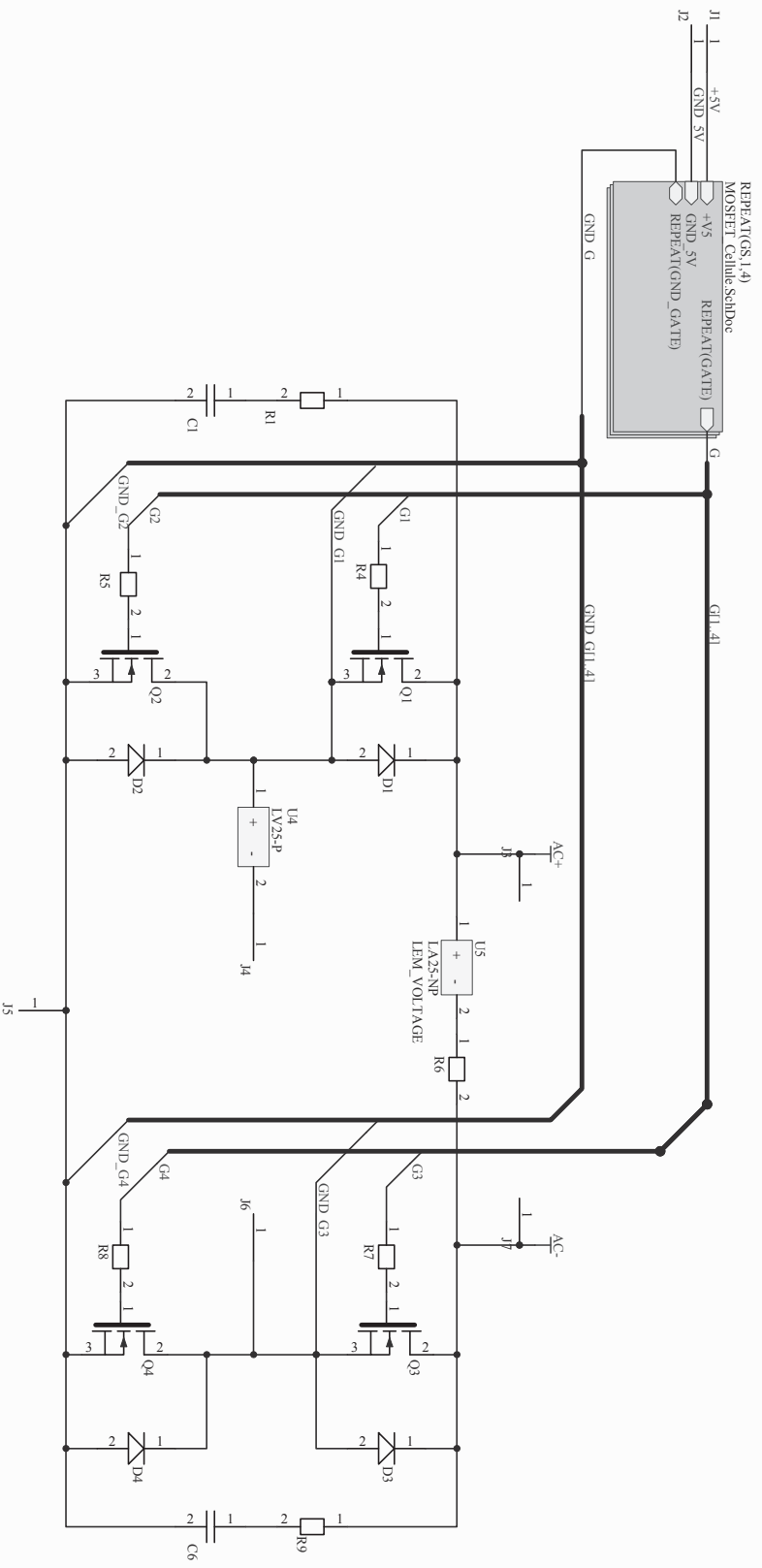
Appendix E

Component List

Table E.0.1: Complete list of components used for the AC Chopper prototype

Component Name	Main characteristic	Manufacturer	Part Number
Impedance capacitor	2 x 66uF	Cornell Dubilier Electronics	944U660K102AAM
Impedance inductor	5mH	Produced in the lab	Metglas, varnished 1.2mm wire
Filter capacitor	47uF	Cornell Dubilier Electronics	944U470K122AAM
Filter inductor	0.5mH	Produced in the lab	Metglas, varnished 1.2mm wire
Receptor	600nm	Avago Technologies Inc	HFBR-2521Z
Inverter MOSFET	–	Vishay Siliconix	IRLD014
Pull-up resistor	1000Ω	–	0.5W 5%
+15V voltage supply	+5V to +15V DC/DC galvanic seperation	Murata Power Solutions	NME0515DC
+5V voltage supply	+5V linear voltage regulator	–	LM7805
Main MOSFET	$V_{DSS} = 200V$, $I_D = 18A$	International Rectifier	IRF640N
Diodes	$V_R = 200V, I_F = 14A$, ultrafast	NXP Semiconductors	BYV79E
MOSFET driver	Low-side, 6A peak	Micrel, Inc.	MIC4420
Gate resistance	133Ω 0.5W 5%	–	–
Snubber	1nF ceramic + 22Ω	–	–

Component Name	Main characteristic	Manufacturer	Part Number
Decoupling capacitors	1nF or 0.1nF ceramic	–	–
Voltage sensor	10 .. 500V	LEM	LV 25-P
Current sensor	12A nominal	LEM	LA 25-NP
Varistor	130V RMS 9.5J	EPCOS	B72207S0131K101
External plug	–	–	LUG contact

Appendix F

Schematics

REPEAT(GS.1..4)
MOSFET_Cellule.SchDoc

J1 1 +5V
J2 1 GND_5V

+V5
GND_5V
REPEAT(GND_GATE)

REPEAT(GATE)

GND_G

GND_G1..4]

G[1..4]

C1   2 1   R1 2 1

GND_G2   G2

GND_G1   G1

R5 1
    2 1

R4 1
    2 1

Q2 3   2

Q1 3   2

D2 2 1

D1 2 1

U4
LV25-P
+
-
1
2

J4 1

J3 1 AC+

U5
LA25-NP
LEM_VOLTAGE
+
-
1
2

R6 1
    2

J5 1

GND_G4   G4

GND_G3   G3

R8 1
    2 1

R7 1
    2 1

J6 1

J7 1 AC-

Q4 3   2

Q3 3   2

D4 2 1

D3 2 1

C6   2 1   R9 2 1

Title

Size   Number   Revision
A4

Date: 18.07.2013
File: C:\Documents and Settings\..\ACCChopper Schematic.SchDoc   Sheet   of

Title

Size: A4 Number   Revision

Date: 18.07.2013
File: C:\Documents and Settings\..\MOSFET Gate Driver.SchDoc
Sheet of

+V5

GND_5V

T1 (T1_G81_)
NME0515SC
-VIN +VOUT
+VIN -VOUT

R2 (R2_G81_)

C2 (C2_G81_)

C4 (C4_G81_)

5V INTERN

Driver_EN

HFBR-2521Z
n.c.   n.c.
VO   RL
GND   VCC

U1 (U1_G81_)

C3 (C3_G81_)

T2 (T2_G81_)
COM
+15V
+5V

5V INTERN

74AHC1TG04
Gate   Drain
Source

U2 (U2_G81_)

GND

R3 (R3_G81_)

Driver_EN

C5 (C5_G81_)

MIC4429
VS   VS
IN   OUT
n.c.   GND
GND   VS

U3 (U3_G81_)

GND_GATE

GATE