NTNU

Norwegian University of
Science and Technology

Surface treatment of high performance multicrystalline silicon wafers

Gina Opstad Andersen

Chemical Engineering and Biotechnology
Submission date: June 2018
Supervisor: Gabriella Tranell, IMA

Norwegian University of Science and Technology
Department of Materials Science and Engineering

Preface

The work presented in this thesis has been carried out primarily at the Norwegian University of Science and Technology (NTNU) at the Department of Materials Science and Engineering. The thesis work took place during spring 2018, as a part of a research project organized by NTNU and SINTEF Industry, entitled Diamond sawing and surface treatment of high performance multicrystalline silicon wafers for high efficiency solar cell applications. Other partners in the project are Shanghai Aero Auto Electromechanical (HT-SAAE) and Shanghai Institute of Microsystem and Information Technology (SIMIT).

The aim of this thesis was to investigate possible optimization strategies to achieve high efficiency solar cells with advanced architecture. The experimental work in this thesis has been carried out at NTNU in Trondheim and HT-SAAE company in Shanghai.

Acknowledgements

This past semester has been a challenging and adventurous time for me, and I am very thankful for all the talented people that have helped and supported me during the process. I wish to express my sincere gratitude to my supervisor, Prof. Gabriella Tranell, for all guidance and support throughout the semester, and for making my stay in China possible. Further, I want to thank Dr. Song Zhang for welcoming me in the most fantastic way in Shanghai, both by offering great mentoring and support at HT-SAAE Co., and for introducing me to his family and colleagues.

Huge thanks to Birgitte S. Karlsen and Sergey Khromov for assisting and helping with characterization and preparation of the experiments. At last, I want to thank my family and friends for always being there, and especially my boyfriend for his kindness and support the past five years.

Trondheim, June 2018

Gina Opstad Andersen

Abstract

This master thesis investigates the properties of high performance multicrystalline silicon, and the production line of black multicrystalline silicon solar cells with PERC architecture. Possible solutions to achieve higher efficiency were explored, and different steps in the production route were examined.

Three steps of the production chain were in focus. Decreasing the polishing time by 70 seconds proved to enhance efficiency. Optimizing the emitter doping process by varying parameters in the deposition step, achieved a more uniform doping distribution across the wafers, and improved overall doping homogeneity by reducing standard deviation by 24%.

Further, the rear passivation step was investigated, and it was found that by increasing the thickness of the Al_2O_3-layer from 14 to 24 nm, efficiency was improved. The final experiments combined the best result in each of the other steps, and optimized parameters were implemented in the production chain for an overall optimization. A champion efficiency above 20% was achieved, which is 0.23% higher than average baseline efficiency for all PERC wafers investigated in this thesis.

Sammendrag

Dette mastergradsarbeidet undersøker egenskaper hos høyeffektiv multikrystallinsk silisium og produksjonskjeden til sorte multikrystallinske silisium solceller med PERC arkitektur. Mulige løsninger for å nå høyere virkningsgrad ble utforsket ved å undersøke ulike steg i produksjonsruten.

Tre steg i produksjonskjeden var i fokus. Ved å senke poleringstiden med 70 sekunder ble det observert en forbedring i virkningsgrad. Fosfordoping ble optimalisert ved å endre parametre i deponerings-trinnet. En mer uniform doping profil ble oppnådd, både på tvers av waferene og sammenlignet med de andre waferene. Totalt standardavvik ble redusert med 24%.

Videre ble baksidepassivering undersøkt, og eksperimentene viste at virkningsgrad ble forbedret ved å øke tykkelsen på Al_2O_3 -lag fra 14 til 24 nm. Avsluttende eksperimenter benyttet de parametrene som ga best resultater, og de ble implementert til en kombinert optimalisering. Det ble oppnådd en virkningsgrad på over 20%, hvilket er 0.23% høyere enn gjennomsnittlig virkningsgrad for alle PERC wafere som ble studert i dette mastergradsarbeidet.

Table of Contents

Abbreviations

ALD	=	atomic layer deposition
ARC	=	anti-reflection coating
BSF	=	back surface field
Cz-Si	=	Czochralski silicon
DS	=	directional solidification
DWS	=	diamond wire sawing
EHP	=	electron-hole pairs
FF	=	fill factor
FTIR	=	fourier-transform infrared spectroscopy
GB	=	grain boundaries
GDMS	=	glow discharge mass spectroscopy
HPMC-Si	=	high performance multicrystalline silicon
IQE	=	internal quantum efficiency
MACE	=	metal assisted chemical etching
mc-Si	=	multicrystalline silicon
mono-Si	=	monocrystalline silicon
MWSS	=	multi wire slurry sawing
PECVD	=	plasma enhanced chemical vapor deposition
PERC	=	passivated emitter rear cell
PV	=	photovoltaic

SD	=	standard deviation
sccm	=	standard cubic centimeter per minute (cm^3/min)
SEM	=	scanning electron microscopy
SRH	=	Shockley-Read-Hall
SRV	=	surface recombination velocity

1 Introduction

1.1 Background

Photovoltaic (PV) energy conversion is predicted to play a large part in the future power marked, and the interest in this technology is increasing worldwide. Our need for energy will continue to rise, as The United Nations predicts a world population growth of 7.6 billion today to 9.2 billion by 2040 [1]. The US Energy Information Administration presented in the International Energy Outlook 2017 that the world energy consumption from 2015 to 2040 is predicted to increase by 28% [2]. Solar energy is a reliable and sustainable power source. The sun emits energy corresponding to more than our whole energy demand if exploited to its full potential [3].

It is now becoming feasible and economically viable to cover a larger energy demand with solar energy almost all over the world [4]. Electricity from solar energy and onshore wind now provides the lowest power cost in more and more places around the world [5]. Thereby, the market and PV technology is evolving quickly, and there is a continuous urge to meet high quality and high efficiency with low cost. Crystalline silicon (c-Si) is

dominating the PV market and is produced through a directional solidification (DS) process. This process can either produce single crystals, known as monocrystalline silicon (mono-Si), or multicrystals. The low cost and reasonable quality of multicrystalline silicon (mc-Si) has become the mainstream in the PV industry and offers a high potential for efficient energy conversion [6].

As the wafer quality directly affects the energy conversion efficiency of solar cells, it is crucial to the cost of PV electricity. Today, high performance multicrystalline silicon (HPMC-Si) is entering the market. High efficiency is achieved by improving the ingot quality by reducing the number of dislocation clusters and defects [7]. It was the improvement of crystal growth technology, that led to the breakthrough of HPMC-Si solar cells. During growth of traditional mc-Si ingots, defects will generate throughout the material. The defects include randomly oriented grain boundaries (GB), dislocations, inclusions and oxides. These defects will serve as recombination centers for light-generated charge carriers, thus reduce the carrier lifetime and the solar cell performance. Higher efficiency is achieved due to the reduced amount of dislocation clusters. This beneficial effect is obtained by reducing the grain size and the density of symmetrical GB (twins), in combination with increased density of random angle GB [6].

Introducing diamond wire sawing (DWS) for mc-Si assures high productivity and reduces cost. Passivated emitter and rear cell's (PERC) are currently entering the industrial crystalline silicon solar cell market and is gradually

becoming the most cost-efficient choice for mass production of cells [8]. The ITRPV anticipates that the PERC technology will progressively take the largest market share in the years to come, as illustrated in Figure 1.1. PERC are expected to gain approximately 35% market share within the next few years.

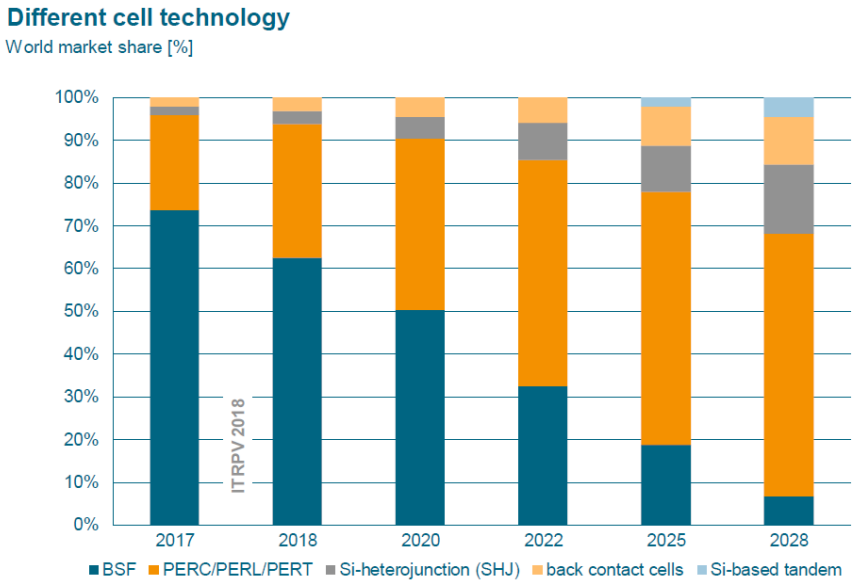


Figure 1.1: Forecasted market share of different solar cell technologies according to the ITRPV [9].

1.2 Research Definition and Motivation

The aim of this thesis was to investigate possible optimization strategies to achieve high efficiency solar cells with advanced architecture. The work included a characterization part, in order to investigate how properties of high performance silicon are improved compared to traditional casts. The cell technology that was in focus is the PERC architecture, and properties and cell performance parameters were investigated. Three steps of the production line of PERC were examined;

- Polishing step of texturization process
- Emitter doping
- Rear surface passivation

These are all important steps to assure a high efficiency cell. By optimizing the texturing process, it is possible to achieve a surface with a reduced number of surface states, hence higher efficiency can be achieved. The front surface should have low reflectance and regular morphology, and a well-passivated surface has to be achieved. An important loss mechanism for PERC is bulk recombination. A possible solution to overcome this is to improve the phosphorus diffusion gettering, which can be done by optimizing the emitter doping process. Finally, continuous improvement of the rear surface passivation is always relevant.

2 Theory

The following sections introduce relevant background and theory in order to interpret and investigate the experimental work and results in this thesis. There will be a focus on the production route of high performance mc-Si and PERC architecture. Important parameters in the production steps will be discussed, and performance limiting factors will be investigated in order to understand how enhanced efficiency can be achieved.

2.1 Traditional Solar Cell Technology

The efficiency of a solar cell is highly affected by the quality of the raw material, as well as the industrial production route and the final structure. Due to the reduction in prices the solar cell industry has experienced over the past few years, there is always an urge in the market to improve quality and efficiency without increasing the costs.

2.1.1 Output Parameters

The most common PV materials are made from semiconductors [10]. A semiconducting material is restricted by its bandgap, setting an upper limit

on the voltage, which can be observed in Equation 2.1, where E_g is the bandgap, V is the voltage and q is the elementary electric charge. The maximum voltage is thus correlated to the bandgap of the semiconducting material, if losses are neglected. The actual voltage achieved will usually be considerably less than this theoretical limit. While a larger bandgap would give rise to a higher voltage, it would simultaneously reduce the absorption and thus the current [11]. Through doping and material processing, a semiconductor can be tailor-made for optimal solar energy conversion. It is important for solar cell engineering to have an optimum energy bandgap, strong light absorption, efficient charge separation and charge transport, and the load resistance should be optimized [10]. Due to low cost and high quality, mc-Si is the main stream technology in today's solar cell production [6].

$$V = \frac{E_g}{q} \tag{2.1}$$

Solar cell performance is characterized by its output parameters derived from its I-V (current-voltage) characteristic, such as the energy conversion efficiency (η), open circuit voltage (V_{oc}), short circuit current (I_{sc}) and the fill factor (FF) [12]. When the voltage across the cell is zero, the current is I_{sc}, and when the current is zero, the output voltage is V_{oc}. The light-generated current, I_l, will be close to the short circuit current for a high quality solar cell. The I-V characteristic of a diode is given in the Shockley Equation 2.2, and relates the current, I_D and the voltage of a cell in zero illumination, k is the Boltzmann constant, T is temperature in degrees Kelvin and I_0 is the reverse saturation current. The overall current-voltage

characteristic of an ideal solar cell is then equal to the difference between the light generated current and the diode current, shown in Equation 2.3. I_0 is a measure of the leakage of minority carriers across the pn-junction in reverse bias and it is a material dependent, temperature sensitive parameter, related to the bandgap of the material [13].

$$I_D = I_0 \left[exp(\frac{qV}{kT} - 1) \right] \tag{2.2}$$

$$I = I_l - I_D \tag{2.3}$$

The FF is defined in Equation 2.4, where V_m and I_m, are the voltage and current respectively at which the solar cells delivers maximum power (P_{max}). Figure 2.1 shows the I-V characteristic of an ideal solar, representing the relevant parameters [14].The total solar cell energy conversion efficiency due to incident light (P_{in}) is determined by Equation 2.5.

$$FF = \frac{V_m I_m}{V_{oc} I_{sc}} \tag{2.4}$$

In real cells, the cell behaviour is degraded by the presence of series and shunt resistances. The series resistance arises from the resistance of the cell material to current flow, specially through the front surface to the contacts, and from resistive contacts [10]. Shunt resistance arises from leakage of current through the cell, around edges of the device and between contacts of different polarity. For an efficient cell R_s should be small and R_{sh} to be large, otherwise FF will be reduced.

$$\eta = FF \cdot \frac{V_{oc} I_{sc}}{P_{in}} = \frac{V_m I_m}{P_{in}} \tag{2.5}$$

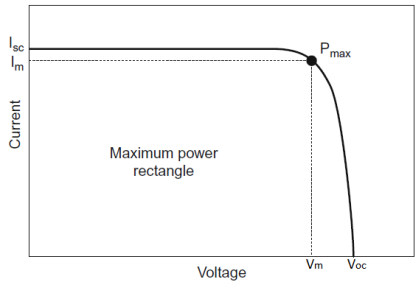


Figure 2.1: The I-V characteristic of an ideal solar cell [14].

2.1.2 Microstructures in Silicon for Solar Cells

Mc-Si has the greatest market share in the industry, as it is cheaper to produce compared to mono-Si. The efficiency of a solar cell is related to the lifetime of the charge carriers in the material. Long lifetime is required to obtain high efficiency, and is correlated to the recombination activities within the cell. A polycrystalline material will consist of microcrystallites, commonly called grains, which are arranged at random orientations. The boundaries between them are termed GB. Within the width of a grain, the material is crystalline, which is typically the order of one μm. Since the grains are large in quantum-mechanical terms, the band structure is essentially identical to that of the mono-Si [10]. However, the transport and recombination properties are strongly affected by the presence of the interfaces, meaning that the GBs inhibits the cell performance.

The performance of mc-Si solar cells is thus limited by impurities and crystal defects. Impurities are easily accumulated at crystal defects such as GBs and dislocations, forming recombination active defects in the material [15]. Silicon usually contains a large amount of impurities, such as metals, carbon and oxygen. The photogenerated charge carriers need to have long lifetime, so they can be collected and contribute to the electrical current. If the material is of low quality and have a lot of defects, the carrier lifetime will be shortened. Impurities and defects increases recombination velocity, as they give rise to allowed energy levels within the otherwise forbidden band gap [16].

The most important recombination processes in indirect semiconductors, such as silicon, are Shockely-Read Hall (SRH) recombinations traps in the bandgap [17]. The traps occur in crystals containing impurities and defects creating allowed energy levels, and these levels facilitate an efficient two-step recombination process through traps. The net recombination-generation rate will have its peak value if defect levels lie near the middle of the forbidden band gap.

GBs can be thought of as minority carrier sinks. To avoid significant loss in the performance of the solar cell, the lateral dimensions of the grains should be large compared to the minority carrier diffusion length in the material. Minority carrier diffusion length, L_n is given in Equation 2.6, where D_e is the diffusion constant and τ_n is the minority carrier lifetime, and describes the distance a carrier can diffuse before it is recombined [17]. Equation 2.6

is valid for p-type materials, where electrons are minority carriers.

$$L_n = \sqrt{D_e \tau_n} \tag{2.6}$$

Another important origin of recombination, is recombination at surfaces. The surface atoms will not have all the available bindings attached to other atoms, and thereby have so called dangling bonds. These bonds will be non-saturated and create a large density of defects within the bandgap [18]. The introduction of these allowed states within the forbidden band gap, will enhance the recombination rate. The recombination mechanism is the same as previously, surface states lying near midgap are the most effective recombination centers. Passivation of surfaces to reduce the surface recombination will be discussed in later sections.

Impurities in Silicon

Impurities and their impact on silicon solar cell performance have been investigated in several studies. Coletti *et al.* studied the impact of the transition metals iron, chromium, nickel, titanium and copper in an experimental study where each of the impurities where added to the feedstock, before growing p-type, directionally solidified, mc-Si ingots. It was found that impurities like iron, chromium and titanium cause a reduction in the diffusion length, while nickel affected the emitter recombination. Copper however, affected both the base-bulk recombination and the emitter recombination. The severity of the detrimental effects on performance is concentration dependent. Another study, that investigated the effect of aluminium impu-

rities in p-type mc-Si, found that the Al tolerance was much higher than expected. Al doped ingots showed weaker light induced degradation due to a preferential Al-O complex formation [19]. However, above threshold concentration, Al will have a negative impact on cell performance.

Oxygen, carbon and nitrogen are impurities that are present at very high levels in mc-Si, and they are introduced during crystallization [20]. Carbon is mainly introduced through the melt surface via carbon monoxide. Nitrogen originates from the crucible coating and oxygen from the silica crucible. Single oxygen atoms at interstitial sites in silicon are not electrically active. Carbon, on the other hand, will not influence carrier recombination if present at substitutional sites. However, if the solubility limit of carbon is exceeded, precipitates of SiC may form locally in the melt and in the crystal. The distribution of oxygen and carbon will vary in the ingot, and the segregation pattern differs for the two impurities. Like boron, carbon has a segregation coefficient (k_0) below 1, meaning that both impurities enriches towards the top of the ingot. The oxygen concentration will on the other hand increase downward, as k_0 for oxygen is above 1. Concentrations have also been found to be inhomogeneously distributed in radial direction. There is an increase in carbon concentration for the first $\frac{2}{3}$ of the solidified ingot towards the center line of the ingot, while for the last $\frac{1}{3}$ concentration remains almost constant. The radial oxygen distribution shows an opposite trend, it decreases towards the centerline for the first $\frac{2}{3}$ of the solidified ingot, while the last $\frac{1}{3}$ also here shows a constant concentration.

Stokkan *et al.* presented in May 2017 results from a national project about impurities in high performance mc-Si [21]. It was concluded that it is possible to achieve mc-Si with very high carrier lifetimes after phosphorus gettering and hydrogen passivation, if dislocation density and contamination levels are low. Acceptable impurity levels were summarized based on reviewing several investigations of contamination levels, also including the main sources during production: feedstock, crucible and coating. This is presented in Figure 2.2.

	feedstock SEMI I		feedstock SEMI II		coating		crucible		Ingot	
	ppbw	mg/270 kg	ppbw	mg/270 kg	ppmw	g/300 g	ppmw	g/80 kg	ppbw	colour scale
Al	0.5	0.1	10	2.6	10	0.003	500	40	19	100 %
Cr	3	0.7	13	3.6	2	0.0006	5	0.4	0.4	10 %
Cu	3	0.9	16	4.4	1	0.0003	0.2	0.02	1	1 %
Fe	3	0.8	14	3.8	10	0.003	20	1.6	5	0.1 %
Ni	3	0.8	15	4.0	1	0.0003	0.3	0.02	1	0.01 %
Ti	2	0.7	12	3.3	0.1	0.00003	100	8	1	0.001 %
Zn	3	0.9	17	4.5	1.5	0.0005	3	0.2	0.5	
Mo	5	1.3	24	6.6	0.1	0.00003	0.1	0.008	1	
Co					30	0.009	0.05	0.004	0.05	
Ca	5	1.3	24	6.4	5	0.002	50	4		
Na	3	0.7	14	3.7	5	0.002	50	4	10	
K	5	1.3	23	6.3	5	0.002	50	4	10	

Figure 2.2: Impurities in feedstock, crucibles coating and ingot. The concentration is given in the first column, and the content in an industrial crystallization system in the second. The colour scale compares the potential severity of different sources [21].

2.1.3 Traditional Production Route of Multicrystalline Silicon Solar Cells

The following section will describe the traditional production route for mc-Si. A simplified overview of the process from ingot to wafer is illustrated in Figure 2.3.

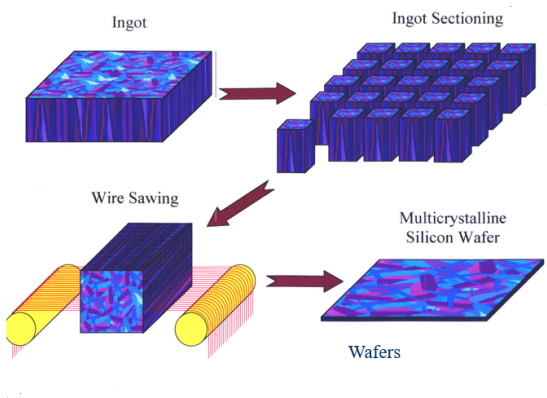


Figure 2.3: Overview of mc-Si production chain [22].

Many of the material properties are determined by the casting process, and the major casting method for producing mc-Si is DS. The most common method is Bridgeman, as it provides columnar growth and a planar front [23]. Mc-Si ingots made by DS are often pre-doped. The feedstock is charged, for example by doping with boron which is added together with the feedstock, prior to melting. Gallium as an alternative to conventional boron doping for p-type substrates has gained interest for the mc-Si market. Using Ga doping instead of boron, has been documented to suppress light-induced degradation of carrier lifetime in the literature [24, 25, 26].

Dhamrin *et al.* studied the quality and stability of Ga-doped mc-Si, and compared the results with boron doped wafers of ingots grown by the same solidifying conditions. Ga-doped materials have higher lifetimes, and solar cell characteristics were found to be very stable under illumination [26].

An important parameter in mc-Si casting is the crucible and its properties [27]. Crucibles are made of slip-cast silica, and they are lined with a Si_3N_4-based (silicon nitride) coating to prevent liquid silicon sticking to the walls and subsequent cracking of the ingot, as solidification and cooling induces strong stress. As most elements are more soluble in the liquid than in the silicon, impurities dissolved in the melt will segregate. Casting is thereby used as a purification method, as most impurities in silicon have low segregation coefficients(often less than 10^{-5}). When the melt solidifies from the buttom and up, the element concentration will increase with the ingots height according to Scheil's equation, given in Equation 2.7 [28]. The distribution coefficient of boron is close to 1($k_0 = 0.8$ [29]), which means that the doping profile will not vary as much with height in the ingot post solidification.

$$C_s^* = kC_0(1 - f_s)^{(k-1)} \tag{2.7}$$

Parameters defined as:

C_s^*: solid composition at the solid/liquid interface

k: equilibrium distribution coefficient

C_0: starting composition

f_s: fraction of solid

Heat will be removed from the bottom, inducing a crystal growth upwards, parallel to the solidification direction. After DS, the top of the ingot is highly contaminated due to segregation. This layer, called the carbide cut, have to be removed. Additionally, side-, top- and bottom-cuts are removed due to contamination from the crucible walls, coatings and from the carbide cut layer. After solidification, the ingot is sliced into wafers and etched to smooth the rough surfaces. For a long time, multi-wire sawing was the main slicing technique for both mono- and mc-Si in the PV industry [30]. However, as the the cost of solar cell processing and module fabrication have been vastly reduced over the past years, the sawing cost remains high, holding about 30% of the wafer production. During wafer cutting, about one third of silicon is lost into the cutting slurry as kerf [31]. These drawbacks of the traditional method has led the industry to seek new solutions. The establishment of DWS for mc-Si wafering is a promising way to govern the increasing demand on lower cost and higher efficiency. This will be discussed in more detail in section 2.2.2.

An overview of the next steps is given in Figure 2.4. After wafering saw damages are removed and surfaces is normally textured in order to enhance light absorption. The next part of the fabrication is to form the pn-junction of the wafers. If the substrate is p-type, the junction is prepared by high temperature diffusion of the n-type dopant, usually phosphorus, into the top surface. The generation rate of electron-hole pairs (EHP) is highest at the surface of the cell [16]. This requirement, combined with the fact that the

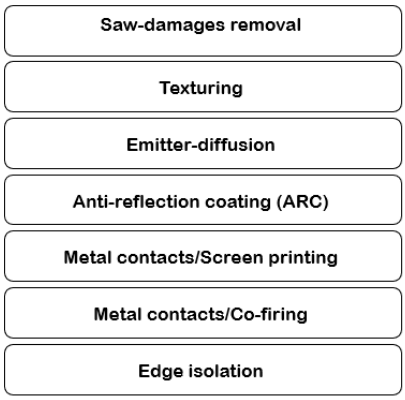


Figure 2.4: Overview of mc-Si production chain[22].

peak collection probability of generated minority carriers are at the depletion region and the region lying within a minority-carrier diffusion length of it, means that the junction should be as close to the surface as possible .

Another important aspect of the emitter doping is the contact resistance between Ag and n^+-Si contact [32]. The contact resistance is a function of several parameters, such as doping concentration, the type of semiconductor material and the metal work function. Of these, the doping concentration at the cells surface has the most critical impact. The sheet resistivity of this layer can be described by Equation 2.8. The sheet resisitivity is commonly described with unit ohms per square, deonted Ω/sq, which is dimensionally equal to an ohm, but it is exclusively used for sheet resistance. To achieve minimum sheet resistivity of this layer, high doping is required.

$$R_{sheet} = \frac{1}{q\mu_e N_D t} \tag{2.8}$$

Parameters defined as:

q: elementary electronic charge

μ_e: electron mobility

N_D: surface doping concentration

t: thickness of the emitter

However, the doping process is a trade off of many parameters. With high doping concentration, other undesirable effect are observed. There is an upper limit of electrically active phosphorus in silicon, and phosphorus in excess of this would be expected to be incorporated into phosphorus-rich precipitates [16]. In such regions, minority-carrier lifetime is greatly reduced and light-generated carriers have very little chance of being collected. Such phosphorus-rich precipitates near the surface are called dead layers. Another way dead layers may degrade cell performance is when the emitter thickness(x_p) is too wide [10]. If x_p exceeds the diffusion length of electrons, L_n, a part of the emitter becomes a dead layer which absorbs light without generating a photocurrent. This means that for optimal design it is preferred to have a thin, highly doped emitter and a thick, lightly doped base.

The dopant is deposited by exposure to nitrogen gas bearing phosphoryl chloride($POCl_3$) in high temperature [34]. The process is performed in a

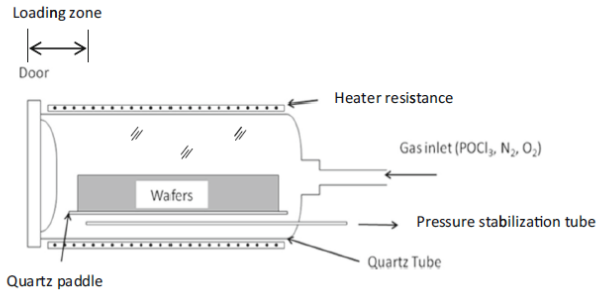


Figure 2.5: Schematic description of typical diffusion furnace [33].

diffusion tube furnace, illustrated in Figure 2.5. The diffusion process have two important steps, predeposition and drive-in. In the predeposition step, $POCl_3$ flow along with N_2 and O_2 through a tube, resulting in deposition of P_2O_5 on the silicon surface. In the drive-in step, the inflow of $POCl_3$ is switched off and diffusion proceeds from the layer deposited in the previous step. The main reaction during the pre-deposition step results is the formation of P_2O_5. After P_2O_5 is deposited on silicon, it is reduced with formation of SiO_2, according to the reaction:

$$2\,P_2O_5 + 5\,Si \longrightarrow 4\,P + 5\,SiO_2$$

This reaction results in formation of phosphosilicate glass (PSG), -xP_2O_5:ySiO_2, on the silicon surface. It is the PSG that provides the source of phosphorus atoms during the drive-in step. Diffusion process optimization aims to achieve uniform sheet resistance across each wafer and equal distribution of the wafers within one boat. Murukesan *et al.* performed a study of $POCl_3$ based diffusion optimization for the formation of homogeneous emitters in p-type c-Si solar cells [34]. The gas composition, exhaust rates and flat

zone temperature profile was varied aiming to achieve uniform sheet resistance. Trends in the results showed that by decreasing the opening area of the exhaust pipe, the suction velocity decreased and the standard deviation (SD) of the sheet resistance was reduced. Further, it was concluded that flow dynamics in the reactor tube plays a significant role in the uniformity of doping. Experiments showed that when a variation in temperature of $\sim 1^{o}$C across the 45 cm was achieved, sheet resistance SD was reduced to $\sim 6\ \Omega/sq$, while a variation of 17^{o}C resulted in a SD of R_{sheet} at 25 Ω/sq. An additional benefit from the emitter diffusion is removal of impurities through gettering. In gettering, the impurities are relocated to less critical sites, thus improving the performance of the cell [35].

The front surface of the wafer is further textured to reduce reflectivity, by depositing an anti-reflection coating (ARC). Traditional ARC is silicon nitride (SiN_y) or titanium oxide (TiO_2). Introducing a highly doped region near the back contact will increase I_{sc} and V_{oc}, and the effect is called a back surface field (BSF). This is a way to accomplish low effective recombination [16]. The most efficient technique to produce the BSF has been to screen print an aluminium-based paste onto the rear of the cell and alloy the aluminium into the silicon by a firing process. The last part of the cell fabrication is to add front and back metal contacts.

As emphasized earlier, the solar cell industry is facing a constant pressure to optimize their cell manufacturing processes, aiming higher efficiencies while not significantly increasing costs. Rahman *et al.* summarized four

different ways to improve c-Si solar cell efficiency [36]:

- Increased light trapping effect by improving surface structuring and texturization
- Redistributing the emitter profile profile on the front surface
- Upgrading or changing metallization processes to get thinner contacts with excellent electrical properties
- Optimizing the passivation layer on both surfaces to reduce the recombination losses

2.2 High Performance Multicrystalline Silicon Solar Cells

HPMC-Si is similar to mc-Si, but the quality is better. By controlling the growth front, the grain growth and the nucleation conditions, an ingot of higher quality is achieved. At the same time, the production cost is considerably lower than of mono-Si. This section will review and present some of the important steps when producing solar cells of high performance, and how this can be implemented to large scale production of industrial cells. Higher efficiency of silicon solar cells will have a positive impact through the entire value chain, meaning that the wafers not only achieve high efficiency, but also a narrow distribution in the performance.

2.2.1 Managing Crystal Growth

The Bridgeman method for DS is the most common method when producing mc-Si. The crystal growth will influence the final structure of the crystal, and is thus an important part of achieving a material with the optimal properties [23]. Well developed understanding and control of the growth mechanisms, the impurity distribution and defects are necessary. Silicon crystals have diamond structure, and a perfect crystal would have a periodic arrangement of atoms. However, deviation from the crystal symmetry occurs in all real crystals. These are called defects, and will affect the properties of the final crystal. The electrical properties of semiconductors can be greatly influenced by the occurrence of dislocations. Due

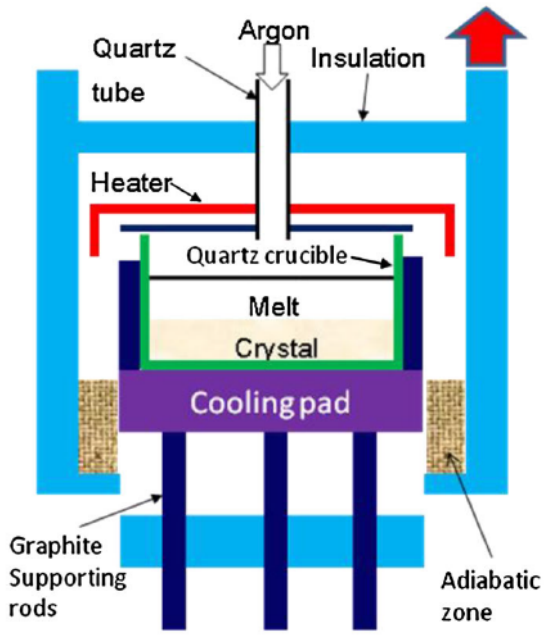


Figure 2.6: Schematic illustration of a directional solidification furnace [6].

to high impurity mobility on dislocations and pipe diffusion, clusters of impurities at dislocations can be observed, as impurities are attracted to dislocations. As growth technology advanced, the performance of the solar cells was improved and HPMC-Si entered the commercial marked. It has been established that it is possible to mitigate the multiplication of dislocations throughout the ingot by controlling nucleation and grain growth [6]. Improving lifetime and efficiency uniformity of whole ingots, means high production yield. An illustration of a DS furnace is given in Figure 2.6.

HPMC-Si is known for its lower average grain size and lower dislocation cluster density due to controlled grain-growth kinetics that render GB types

favorable to a low density of dislocation clusters [37]. It is believed that bigger grains are more vulnerable to the propagation of dislocations during growth, as less GBs are able to hinder it. However, as silicon expands when it is solidified, thermal stress during solidification is inevitable. In a study by Yang *et al.*, the key ideas for defect control were discussed [6]. A common practice of crystal growth in growing a good ingot, is to control the solidification front through the hot-zone design, meaning that crucible insulation is used to obtain a flat growth front. A similar, improved concept that has been used in the vertical Bridgeman crystal growth for years is to use the so called adiabatic zone, as shown in Figure 2.6.

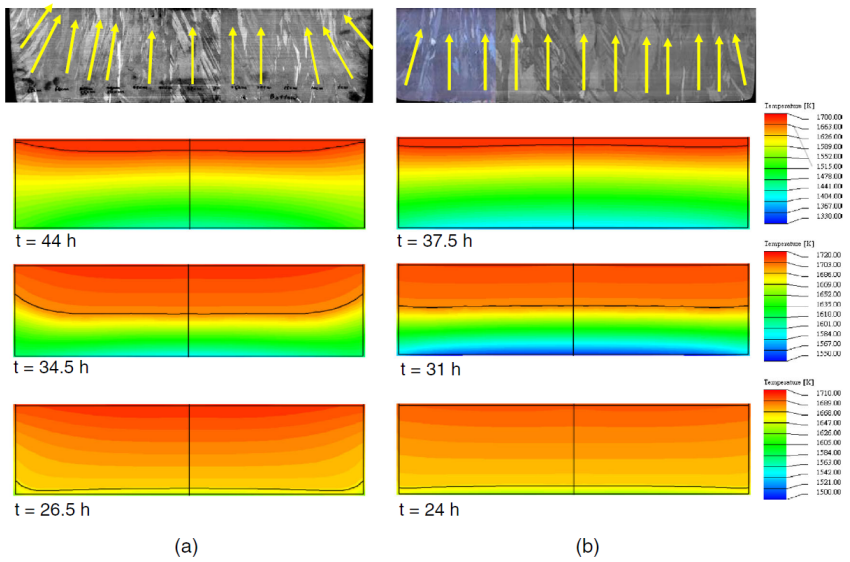


Figure 2.7: Simulated thermal fields and solidification front: (a) default hot zone and (b) improved hot zone; the cross sections of the ingots grown by the hot zones are shown at the top; the arrows indicate the direction of the heat flux [6].

Thermal fields can illustrate how the growth front varies with the different approaches. In the report, they simulated the fields using the software CRYSMAS as shown in Figure 2.7, which illustrates how the growth front was altered when using the default (without the adiabatic zone) and the improved (with the adiabatic zone) hot zones. It is possible to observe the interface changed from being very concave with the default hot zone, to a flat growth front for the whole period of crystal growth, as shown in Figure 2.7 (b). By achieving a flat growth front, thermal stress is reduced.

Lifetime mappings of the ingots showed that the grains grew inward near the crucible wall, indicating a concave growth front for the default hot zone. However, for the improved hot zone, the columnar grains grew vertically indicating that the growth front was flat. This reduced equiaxed grains near the top of the ingot, and efficiency was improved overall, compared to the default hot zone method. It was observed that lifetime dropped quickly with height as a result of multiplication of dislocations. Further investigations observed that ingots grown with small uniform grains generated at the beginning of solidification, gave the best uniformity, and a reduced amount dislocation clusters even close to the top of the ingot was observed. Wafers with small initial grains were thereby proved to produce solar cells with higher efficiency.

2.2.2 Wire Sawing Technology

After solidification, the ingot is sliced into wafers. Solar cell production has experienced a decrease in cost the past years, but the sawing costs remain

high and contributes to about 30% of the wafer production [38]. Today, the industry is moving away from the traditional multi-wire slurry sawing (MWSS) technique, and towards diamond sawing. The reason for this is that the DWS technology have the potential of two to three times higher productivity combined with possible kerf recycling [39].[1] Additionally, DWS eliminates the use of slurry, which is costly and causes environmental concern.

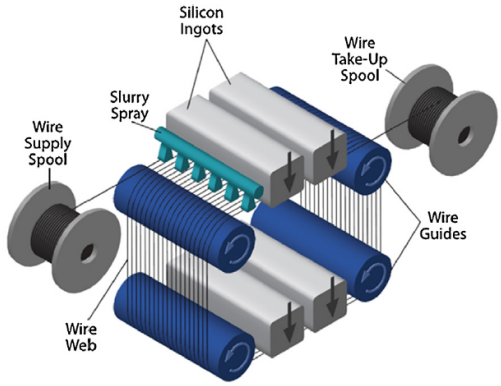


Figure 2.8: Schematic of multi-wire slurry sawing [39].

The principles of the MWSS are depicted in Figure 2.8. Multi-wire sawing was for long the main slicing technique, as the technology provides high throughput, small kerf loss, less restrictions on the size of the ingots and a good surface quality [30]. A single stainless steel wire is fed from a supply spool through a pulley and tension control unit to the wire guides. The silicon ingot is fed against the moving wire web and sliced into hundred of

[1] Kerf is the width of material that the process removes as it cuts through the plate.

wafers at the same time. Cutting of wafers can either be by wires moving in one direction or by osccillating wires. One direction wiring will allow higher wire speed, byt yields less planar surface. Cutting is achieved by an abrasive slurry, which is supplied through nozzles over the wire web and carried into the sawing channel by the wire. Silicon carbide(SiC) powder are the most commonly used abrasive, and the material is very expensive.

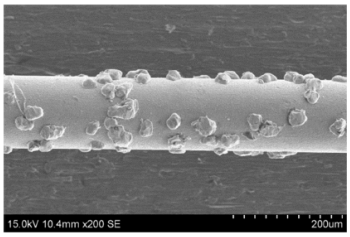


Figure 2.9: Scanning electron microscopy (SEM) image of diamond wire [39].

The diamond wafer sawing (DWS) is different from MWSS because instead of using SiC particles in the slurry as cutting agents, a stainless steel wire with diamonds implanted is used [39]. The diamond grits serves as fixed cutting points, illustrated in Figure 2.9. Diamond sawed wafers will have very different surface morphology than slurry sawn wafers, as illustrated in Figure 2.10. The introduction of this technique for mc-Si is challenging because the phase transformation, initiation and propagation of microcracks will vary with grain orientation. The resulting surface will consist of a damaged layer of variable thickness, which needs to be further treated to achieve high efficiency solar concepts. The two wafering processes have different material removal mechanisms, thus the resulting surfaces will have different properties. Schematics of the two cutting mechanisms is illustrated in

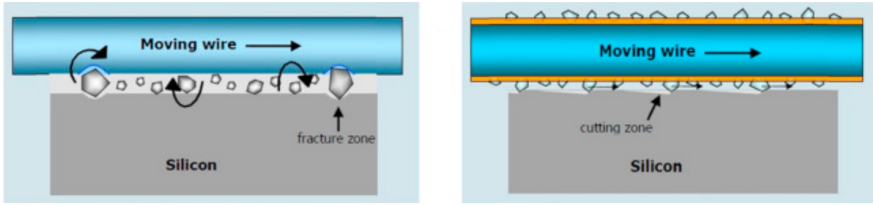


Figure 2.10: Schematics of the cutting mechanisms:slurry sawing to the left, diamond wire sawing to the right [39].

Figure 2.10. In slurry sawing, material is removed by interactions between SiC particles, wires and the Si surface. This process is referred to as three-body-wear. In DWS, the material removal process is referred to as two-body-wear. Material is removed as a result of direct interactions between Si substrate and the diamond grits. Because the sawing mechanisms for the two methods are fundamentally different, the resulting surface morphologies will be different too. Diamond sawed wafers show smooth cutting grooves, as can be observed to the right in Figure 2.11. The grooves indicate that silicon was removed by ductile mode of machining. Slurry cut wafer are covered with microcracks, illustrated to the left in Figure 2.11.

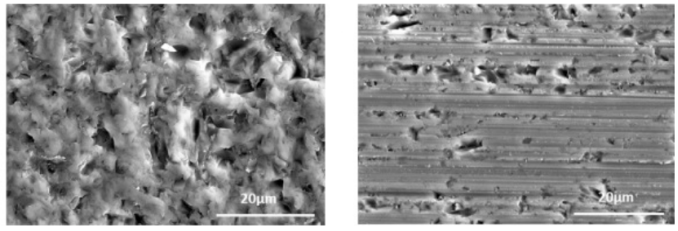


Figure 2.11: SEM of wafer surface morphology: slurry sawn wafer to the left, diamond wire sawn wafer to the right [39].

2.2.3 Surface Treatment

Texturing

The wafer cutting introduces a saw damage layer which has to be removed before entering the texturing process. When a wire saw is used, typically a layer of 10 - 20 μm has to be etched from both sides of the wafers [40]. A damage removal etch can be based on 20 - 30 wt.% aqueous solution of NaOH or KOH heated to 80-90 ^{o}C. The saw damage etch leaves the silicon surface shiny, and the high reflectivity will suppress the solar cell efficiency [41]. After saw damage removal (SRD), texturing of the Si wafers is performed. Surface texturation will reduce the reflection loss of sunlight on the surface, hence improve the optical properties of solar cells and increase the conversion efficiency.

It has been well established that nanoscale structures and the related porous layers around their walls have excellent light trapping properties [7, 42, 43]. Due to this, the reflectivity of mc-Si wafers can be vastly reduced by applying nanostructures on the surface of the wafers. Different methods to fabricate textured nanostructures include femtosecond laser etching, plasma immersion ion implementation etching, reactive-ion etching and metal assisted chemical etching (MACE) [41]. Among these methods, MACE has proved to be an effective fabrication technique for texturing large area Si wafers, due to its low cost and easy processing technique [44]. The nanostructured silicon surface produced with this technique is called black silicon (b-Si) and creates structures with needle- or pyramide like shape on the sur-

face of the silicon substrate. Surfaces with b-Si contains special properties such as large surface area, negligible reflectance and superhydrophobicity which provides interesting opportunities in various applications [35]. Branz *et al.* demonstrated in a study that the surface reflectance can be as low as 2% from 300 to 1000 nm for a nanoparticle-based etched silicon surface [43]. The use of black silicon can therefore vastly improve the light management of high performance silicon solar cells, but the surface needs further treatment as the texturing creates a surface that is challenging to passivate with high surface recombination. Enhanced light absorption will result in increased I_{sc}, which consequently improves the photoelectron conversion efficiency, η [45].

The etching process in MACE is a simple process which can be regulated by varying the concentration of the reactive elements in the solution, thus controlling the etching rate. An illustration of the process is given in Figure 2.12 [46]. The pore diameter at the bottom is equal to the size of the Ag particle, but the pores on the top is bigger than the Ag particle [47]. The penetration depth of the particles has been studied, and it has been found that pore depth increases linearly with etching time at a rate of ~ 0.4 μm/min [48]. For longer etching time it has also been shown that the pore openings will be larger and less clearly defined, which indicates a more progressive dissolution of the Si walls at the surface, forming a porous Si layer.

The chemical etching process can be explained by the following process, marked as step 1-4 in the figure:

1. Hydrogen peroxide (H_2O_2) works as an oxidizing agent and reduces the catalyst, eg. Ag-particles.

2. The reduction reaction generates holes, as the silver ions is digging into the Si substrate underneath the metal particle.

3. Ag^+ injects holes into the valence band of Si, and the Si surface is oxidised.The high hole concentration underneath the Ag particles will migrate to the sidewalls and the surface.

4. Hydrofluoric acid (HF) helps removal of the oxidized silicon.

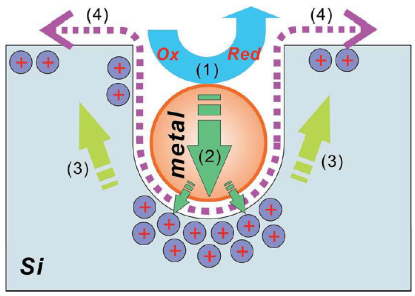


Figure 2.12: Schematic overview of the chemical etching process [46].

A challenge with textured surfaces is that it is hard to get a well passivated surface. As a result of the small diameter pores created by silver assisted etching, more of the silicon surface is left unpassivated because covering the structures on the surface with silicon nitride (SiN_y) is difficult[49]. This left the naked silicon surface as recombination centres of carriers. To

achieve better deposition of the SiN_y-layer, widening of the pore diameter became important. The mechanism is illustrated in Figure 2.13. Therefore, a tradeoff between optical gain and recombination loss must be considered to achieve high efficiency.

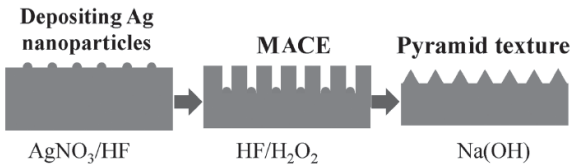


Figure 2.13: Schematic illustration of the three main steps preparing nanoscale pseudo-pyramid texture [50].

A good balance between the diameter of the etched pores and the surface reflectance must be achieved to obtain a solar cell with high efficiency. Using a post alkaline etching treatment has proven to produce pyramid-like texture which makes the structured surface obtain acceptable passivation quality [7, 50, 49]. The treatment will adjust the open area and height of the nanopores, in addition to removal of the porous layer. Figure 2.14 illustrate such a surface, where morphology of samples where examined in SEM and quasi pyramid texture was achieved by alkaline solution treatment. Yue *et al* concluded in a study that the combination of Ag-assisted etching combined with sodium hydroxide (NaOH) post-treatment produced a surface better suited for passivation, leading to an increase of efficiency of 0.65% though reflectance of the NaOH treated surface was increased from 2,03% to 5,45%.

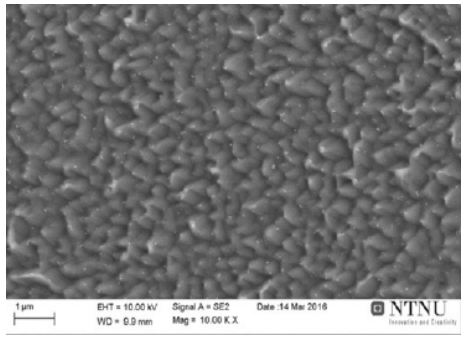


Figure 2.14: Smooth pyramide surface texture after alkaline treatment [7].

Passivation

The surface of c-Si represents the largest possible disorder in symmetry of the crystal lattice. Due to non-saturated bonds, a large density of defects (surface states) within the bandgap exists at the surface of the crystal [36]. As the solar cell industry are moving towards thinner silicon materials, effective passivation becomes even more crucial in order to avoid undesirable efficiency loss, as the relative importance of rear surface recombination increases. Additionally, certain requirements have to be met. It is important to make sure that the surface passivation is long-term stable (>20 years) and also that it is inert to degradation when exploited to the UV photons of sunlight if applied to the illuminated side of the cell surface.

In the surface recombination process, an electron form the conduction band recombines with a hole in the valence band via a defect level (surface state) within the bandgap. The process can be described mathematically by the Shockley-Read-Hall (SRH) theory, which relates the recombination rate and the properties of the surface states, for further theory on the subject

see [18]. The relationship shows that there are two fundamentally different technological possibilities to reduce the recombination rate at a surface: (i) the reduction of the density of surface states, and (ii) the reduction of the concentration of free electrons or holes at the surface. The two strategies are commonly referred to as chemical passivation and field effect passivation, respectively.

Chemical passivation is done by reducing the density of surface states, by saturating the dangling bonds [36]. This can be done by deposition or growth of an appropriate passivating film, introducing atomic hydrogen (H) or by a thin dielectric film. In field effect passivation, the electron or hole concentration at the surface is altered by electrostatic shielding of the charge carriers through the introduction of an electric field. This built in field can be formed by either implementation of a doping profile below the silicon surface or by field effect passivation due to electrical charges in an overlying insulator. The two passivation methods can be combined, eg. by introducing a SiO_2 film which greatly reduces the surface state density, and furthermore leads to field effect passivation due to fixed positive oxide charges. However, as the two surfaces of a solar cells possess different properties, different qualities in the passivation layer should be introduced. For the following section, passivation of a p-type solar cell is the main focus. Plasma enhanced chemical vapour deposition (PECVD) of SiN_y for front side passivation has achieved record low effective surface recombination velocity (SRV) [36]. SiN_y shows superior performance compared to other passivation techniques such as SiO_2 and TiO_2, and this can be at-

tained due to the following: (i) Field effect passivation provided by positive interface charges, (ii) Properties of capture cross sections of dominant defects, (iii) Adjustable refractive index as antireflection coating (ARC), and (iv) hydrogenated passivation of bulk defects.

For the rear side, aluminium oxide (Al_2O_3) has been established as the preferential passivation technology, due to the excellent passivation level provided. Its properties are fundamentally different from that of the other dielectric materials frequently used for the passivation, as they usually contain a fixed positive charge density, while Al_2O_3 contains a high density of fixed negative charges [51]. The high fixed negative charge density located at the Al_2O_3/Si interface provides very effective field effect passivation by shielding electrons from the interface. There has been a continuous development the past years to achieve cost-efficient processes, focusing on surface passivation, laser ablation and screen-printed Al local back surface field (LBSF). As a result of this, cells with PERC architecture have become a favorable choice for mass production of crystalline silicon solar cells [8, 52].

2.3 Advanced Cell Architecture

PERC technology has advanced over the years, and is currently entering the industrial c-Si solar cell marked. PERC is gradually becoming the most cost-efficient choice for mass production of cells, and offers a good approach to surpass the 20% cell efficiency level in mass production [52].

An overview of PERC structure is given in Figure 2.15. Although the transition to the PERC structure only requires that a few pieces of equipment is added to the standard production line, the improvement of efficiency is not an absolute [52]. Both the emitter and the rear of the cell have to be redesigned, because improving only one of them will not increase the cell efficiency as the recombination losses at the other device part will dominate. Further, if both emitter and rear surface is improved, recombination in the base region becomes important. This is due to boron-oxygen complex formation, which will suppress the FF in the cell. This means that PERC design requires a finetuning of influencing parameters that are not linearly interrelated.

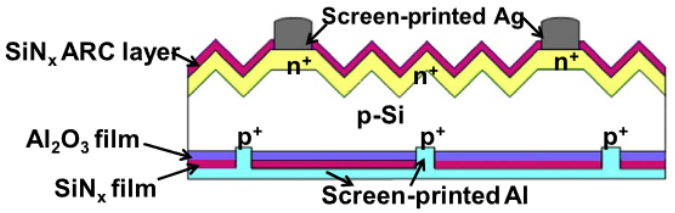


Figure 2.15: Schematic drawing of the industrial PERC cell structure [8].

The PERC design differs from the conventional full-area rear Al-alloyed BSF. As the recombination of the photo-generated charge carriers at the Al rear contact is only marginally suppressed and the Al layer only partly absorbs infrared light leading to poor light absorption, today's full areal Al-BSF industrial solar cells are limited to around 20% [53]. An important step towards industrialization of the PERC concept was to find a way

to obtain low cost and high throughput processes for the deposition of the rear passivation layer. SiN_y deposited by PECVD maintained as the most promising candidate for a long time, as this technology already was established as a successful front side passivation layer of phosphorus doped emitter in industrial solar cells. However, as the rear surface is p type, it was found that SiN_y passivation layers induce an inversion of the surface due to the positive fixed charges within the SiN_y layer. This effect was identified by Dauwe *et al.* in 2002, and was denoted parasitic shunting leading to an enhanced carrier recombination [54].

As discussed previously, AlO_x exhibits a high negative fixed charge density, thus avoiding any parasitic shunting on p-type Si surfaces, and was presented as a suitable option. Al_2O_3 passivation can achieve the lowest SRV on p-type Si due to excellent field effect passivation by the negative fixed charges (Q_f) and superior chemical passivation due to the low interface defect density (D_{it}) [8]. Among the techniques that exists to synthesize Al_2O_3, atomic layer deposition (ALD) is the preferential option due to advantages such as mono-layer growth control, pinhole-free coating, good step coverage and low substrate temperature. The Al_2O_3 film should have uniform thickness and obtain good electrical properties (Q_f and D_{it}) at the Al_2O_3/Si interface. The post anneal have been found to be a very important step to activate the passivation of the as-deposited Al_2O_3 film due to overall control of Q_f and D_{it}. Post anneal can activate the negative Q_f. Further, during the ALD process an interfacial SiO_x film will grow at the Al_2O_3/Si interface, and this continues to grow during post anneal. H from the Al_2O_3 bulk can also diffuse to the interface. It is the SiO_x layer and H

passivation that can be ascribed to the reduction of D_{iy}. The post anneal is important as it plays a crucial role for the overall control of Q_f and D_{it}, thus for achieving overall good passivation. An excessive thermal budget (too high temperature) in the process has been found to decrease the amount of already activated Q_f and a gradual decrease in D_{it} is observed [8, 55].

The PERC concept was further improved when introducing capping of the AlO_x layer with SiN_y. This makes the AlO_x/SiN_y layer stack resistant to Al pastes during firing and improves the optical reflectivity of the rear cell, thereby increasing the absorption of IR light in the solar cell due to improved light trapping [56]. For the industrial PERC, the most important function of SiN_y layer is to maximize protection of Al_2O_3 from the penetration and damage by the screenprinted Al-paste [8]. Furthermore, PECVD SiN_y process can help to activate the Al_2O_3 layer. In addition, the SiN_y film improves the firing stability of the Al_2O_3 film and the internal reflection of light compared to direct metallization of the Al_2O_3 layer, and provides H passivation for Si/Al_2O_3 interface and Si bulk. This can improve the open circuit voltage and to some degree the current output. The improved efficiency of PERC can be addressed to three main reasons: (i) electron recombination is significantly reduced, (ii) higher internal reflectivity is experienced, and (iii) more light is absorbed.

Huang *et al.* presented an experimental study on the most important material and cell parameters for industrial PERC solar cell and a discussed the roadmap to maximize efficiency for mass production of PERC [8]. It was

used Czochralski silicon (Cz-Si), p-type, boron-doped wafers in the experiments. The efficiency loss mechanisms based on some key characterization methods were analyzed and the recombination loss mechanisms were investigated through PC1D and PC2D simulations. The study concluded that the main loss mechanisms, combining efficiency loss mechanisms analysis and the recombination loss mechanisms analysis using simulations, for the current industrial PERC are:

- Relatively high front side recombination
- Series resistance from the cell front
- Not sufficiently efficient light trapping

By introducing the main limiting factors for PERC architecture it is possible to develop an optimization plan to improve performance. The front surface state, effects of the dead layer and bulk properties and the rear surface passivation is important limiting factors that should be investigated in order to achieve high efficiency. However, there is a need to further understand the η_{cell} loss mechanisms of the industrial PERC. Studies have shown that cells can reach well beyond 24%, within the current equipment that is in use in the standard production lines or with small structural changes. [52]. A roadmap for industrial PERC technology is summarized in Figure 2.16, and it shows that expected cell efficiency can approach $\sim$ 23% without cell structure change and 23,5-24% with the transfer to passivated emitter rear locally diffused (PERL) solar cell structure [8] .

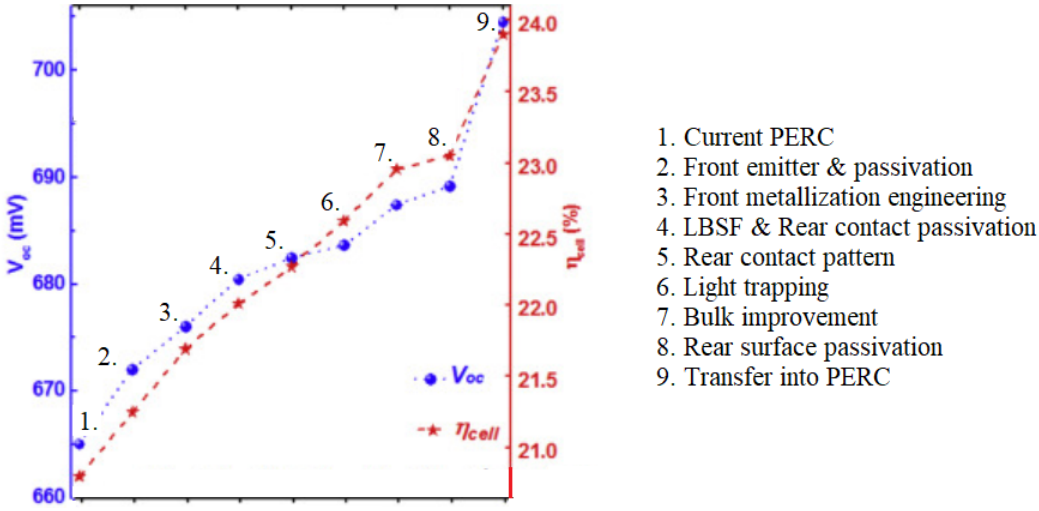


Figure 2.16: Roadmap for PERC technology to 24% [8].

Byungsul *et al.* suggested that key points for the improvements of PERC approaching the 24% limit, are by use of selective emitter, boron-added Al paste for the rear, wafers with high carrier lifetime, multi-wires instead of busbars, and narrow fingers with high aspect ratio [52].

3 | Materials and Methods

This chapter will give the experimental details related to all the results in this thesis. An overview and explanation of where the experiments are in the production chain will be presented.

The experiments were performed on diamond sawed wafers. The ingot is produced in Mongolia, before being sent to Shanghai for sawing. Sliced wafers are received at Shanghai Shenzhou New Energy Development Co., ready for processing. The wafers are the standard dimensions, 156*156 mm^2. Wafers used for PERC production are gallium doped, while traditional black mc-Si wafers are boron doped. A typical process flow of a PERC production line is given in Table 3.1.

After SDR, wafers are textured and then treated with NaOH solution, creating pyramid-like texture. Front emitter is then formed with $POCl_3$ diffusion. Edge isolation and rear side polishing is then performed by a wet chemical process using HNO_3-HF-H_2SO_4 solution. The rear polished surface will provide better light trapping and passivation opportunities. Then the rear side of the cell is passivated by ALD Al_2O_3. SiN_y coating is de-

Table 3.1: Overview of production line.

	Step
1.	Saw damage removal and texturing
2.	$POCl_3$ diffusion
3.	Wet chemical process of edge isolation and rear side polishing
4.	Rear Al_2O_3 + SiN_y coating
5.	Front PECVD SiN_y coating
6.	Laser ablation (rear contact pattern)
7.	Screen printing metallization
8.	RTP co-firing

posited by PECVD, capping the Al_2O_3-layer and surfaces are locally patterned using laser ablation. Finally, screen printing and co-firing is used for front and rear side metallization to form front Ag/n^+-Si- ohmic contact, Al-LBSF and rear local A/p^+-Si ohmic contact.

Before entering the industrial mass production line, the company treats the wafers with a multi-step texture process, the mechanisms are described in the section about MACE. The texture process includes the steps of alkaline polishing in KOH, silver coverage, digging of holes, enlarging of the etching pits and cleaning. All the process steps are performed in automatic tunnels illustrated in figure 3.1, and a list of all the steps is presented below:

1. Alkaline polish

2. Warm water isolation

3. DI water cleaning

4. Ag deposition

5. Hole digging

6. DI water cleaning

7. Ag degluing

8. DI water cleaning

9. HF treatment

10. DI water cleaning

12. Acid rinsing

13. DI water cleaning

14. Pre-hydration

15. Hot air drying

Figure 3.1: Two rows of texturing tunnels in the company's lab, printed with permission: HT-SAAE.

3.1 Characterization

Slabs from an ingot were cut in order to investigate the material properties. The ingot was boron doped. The cutting position of the ingot is given in Figure 3.2. Three heights were investigated for each position; top, middle and bottom. All the test samples were mechanically polished on both sides using waterproof silicon carbide P120, P240, P500, P1200, P2400 paper (FEPA system) and water with a DP-U3 Pedemax machine. The samples were polished further with Abrapol 20 machine and 9,3 and 1 μm paper. This procedure prepared the samples for characterization tests, by removing damage from cutting and assuring uniform surface.

Interstitial oxygen [O_i] and substitutional carbon[C_s] were measured at room temperature by Fourier transform infrared spectroscopy (FTIR) from Thermo Fisher Scientific. The FTIR polished samples were cut by a laser to 5*5 cm^2 dimension before polishing, and measurements were done at 5 sites of the samples, one in the middle and at each of the corners.

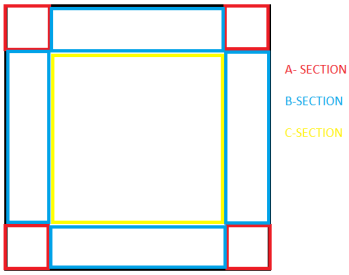


Figure 3.2: Positions in the ingot where the different slag samples were collected from.

Further, the metal impurity concentrations were investigated by glow discharge mass spectroscopy (GDMS). The isotopes that were measured was ^{27}Al, ^{48}Ti, ^{56}Fe and ^{63}Cu. The Astrum from Nu Instruments combines a glow discharge ion source with a high resolution mass spectrometer, and can be used to test high purity materials due to excellent detection limits.

3.2 Experimental Work

The process equipment that was used in the experiments is part of a large scale production at the Shanghai Shenzhou New Energy Development Company. The machines are automatic and experiment parameters were ad-

justed by programming. The experiments focused on three different parts of the PERC production line. When one step in the production line was investigated, the other steps were performed as the baseline production line, unless otherwise stated. Performance of the final cells was tested with HALM I-V tester system machines, which offers a detailed analysis and measuring method, making it possible to investigate the relevant cell parameters.

3.2.1 One-Sided Texturing

The difference in performance between one-sided and two-sided texturing of traditional black mc-Si cells and black mc-Si PERC was investigated in the first part. Cell parameters were measured and compared on one-sided textured surface, instead of the regular two-sided texturing. An illustration of single surface texture is presented in Figure 3.3. The texturing of only one side of the wafers was performed by arranging wafers in doublets, thus only the surface facing "out" was exposed. As observed in Figure 3.3, there is a slight darker area on the lower part of the rear side, meaning that there might occur some texturing due to leakage. This is, however, not detrimental and will be removed during further processing of the rear side.

3.2.2 Front Surface State

The second part aimed to investigate effects of different polishing times. Wafers were textured on both sides. The experiments were performed on wafers for both traditional black mc-Si and PERC solar cells. The baseline polishing time was 220s and the temperature was 80°C. The polish-

Figure 3.3: The single surface texture process, rear surface to left and front surface to the right.

ing was performed in a KOH-bath. The goal was to achieve smaller and shallower texture on nanoscale. Alternative polishing times that were investgated were; 100s , 150s and 300s. These experiments were performed on traditional black mc-Si wafers. The results were compared to the standard recipe, illustrated by the baseline measurements. After polishing, the wafers were subjected to the standard production line and cell parameters were measured. The optimization process was also performed on PERC solar cells, decreasing the polishing time from baseline 220s to 150s. The other time-points were discarded, as the 150s was the only time-point to achieve better results on the traditional cells.

3.2.3 Emitter Doping

The baseline experiment parameters are given in Table 3.2. Experiments were performed to improve the doping profile and additionally to reduce the variation of sheet resistance as a result of different positions in the tube furnace. $POCl_3$ vapor is carried into diffusion tube by inert nitrogen carrier gas. In all the performed experiments on emitter doping, the varied param-

eters were in the deposition step, see Table 3.2. The parameters that was changed is listed in Table 3.3.

Table 3.2: Baseline process parameters for emitter doping.

Procedure	T[^{o}C]	time[s]	N_2[sccm]	N_2-$POCl_3$[sccm]	O_2[sccm]
Pre-oxidation I	785	720	9000	0	0
Pre-oxidation II	785	300	6400	0	2600
Deposition	785	660	7870	830	300
Heat up	834	480	9000	0	0
Drive in	834	960	6400	0	2600
Gettering	810	660	30000	0	0

The first alternative to optimize the recipe was to increase deposition time from 11 minutes to 14 minutes. Additionally, inflow of nitrogen gas was increased from 7870 to 7900 sccm and inflow of nitrogen bearing $POCl_3$ gas was reduced from 830 to 800 scccm. The second batch of experiment wafers were exposed to an inflow of nitrogen of 7890 sccm and nitrogen bearing $POCl_3$ 810 sccm, and the deposition time was 12 minutes.

Table 3.3: Presentation of the parameters that was varied in the experiments compared to baseline.

	T[^{o}C]	time[s]	N_2[sccm]	N_2-$POCl_3$[sccm]	O_2[sccm]
Baseline	785	660	7870	830	300
1.opt	785	840	7900	800	300
2.opt	785	720	7890	810	300

To control and investigate how the phosphorus distribution varied in the furnace R_{sheet} was measured on wafers doped at different locations inside the

furnace. Additionally, the R_{sheet} measurements were performed on 5 different spots on the wafers to investigate the homogeneity of doping across the wafers. The positions are given in figure 3.4.

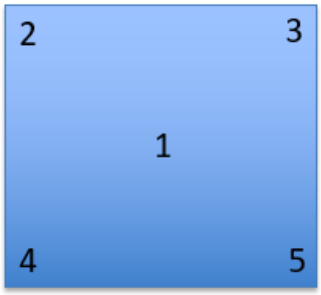


Figure 3.4: Position of the R_{sheet} measurements across each wafer.

3.2.4 Rear Surface Passivation

The cell rear side was passivated by ALD of Al_2O_3 and PECVD of SiN_y stacks.

The wafers in the experiments were separated into two batches, one group experienced longer annealing time and the other had an increased Al-oxide layer thickness. The varied process parameters are listed in Table 3.4.

In these experiments, the passivation layer was deposited by a trimethylaluminium (TMA)-based thermal ALD process, inducing an Al_xO_y layer. The post anneal process was implemented in a tube furnace. The baseline thickness of the alumina oxide layer was 14 nm. The baseline annealing time and temperature was 1800 seconds and 520°C.

Table 3.4: Overview of varied parameters in the rear passivation experiments.

	T [°C]	Layer thickness [nm]	Time [s]
Baseline process	520	14	1800
Increased layer thickness	520	24	1800
Increased annealing time	520	14	2100

3.2.5 Overall Optimization

As the former experiments have been focusing on different part of the production line, a combination of the different production steps is possible. The best achieved result in each of the steps was chosen and cells were produced with a combination of these steps. However, both sides were textured in this experiment even though one-sided texturing achieved better results. This is because one-sided texturing currently is too difficult to implement in a large scale mass production line. Overall, the combined optimization parameters were:

- Polishing time: 150s
- Recipe 2 for emitter doping:
    1. Time: 720s
    2. N_2 inflow: 7890 sccm
    3. N_2-$POCl_3$ inflow: 810 sccm
- Rear passivation layer thickness: 24 nm

4 | Results and Discussion

4.1 Characterization

4.1.1 FTIR

Results of FTIR measurements are given in Figure 4.1 - 4.3, illustrating the concentration of substitutional carbon and interstitial oxygen for the top-, middle- and bottom-cut, respectively. Averages of the five measurements are used for the plots. The graphs illustrate the difference in concentration of the two impurities with respect to site in the ingot at the same height. It is possible to observe that the radial distribution do not vary greatly at any of the heights, except for substitutional carbon at the top of the ingot. The C21 top carbon concentration is actually higher in the center than at the sides of the ingot, which would be more likely to be seen in the lower part of the ingot as discussed in section 2.1.2. SD of each of the five measurements performed on the samples is given in Table 4.1.

Average concentrations as a function of height are plotted for all the samples and are given in Figure 4.4. The observed trends differ to some degree

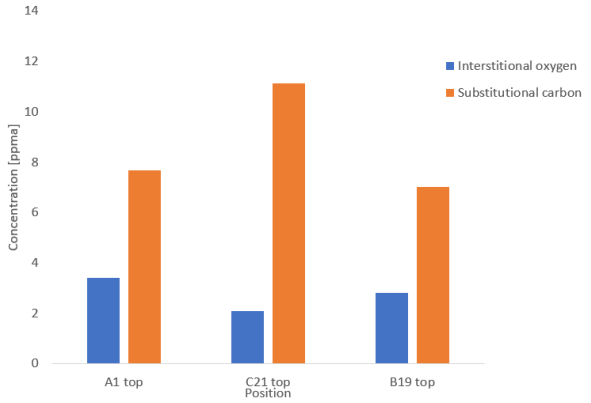


Figure 4.1: FTIR measurements of top cut.

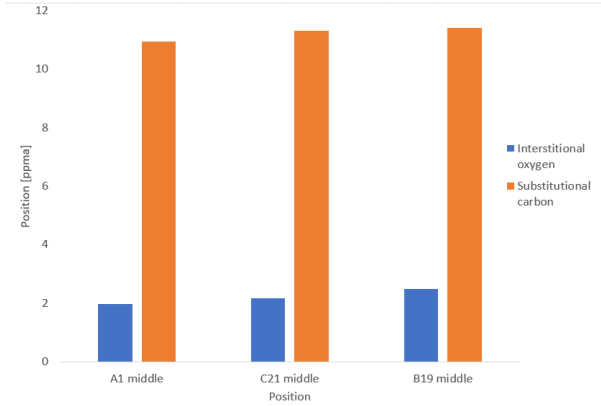


Figure 4.2: FTIR measurements of middle cut.

from what could be expected. It is observed an increasing concentration with height for carbon, and a decreasing concentration with height for oxygen, which matches well with the theory presented in previous chapters. However, the middle and top section do not show any consistent trend with respect to height, comparing the different samples. Many aspects may have an impact on how the distribution of impurities vary in the ingot, such as temperature profiles, shape and size of ingot and solidification front.

As discussed previously, interstitial oxygen and substitutional carbon do

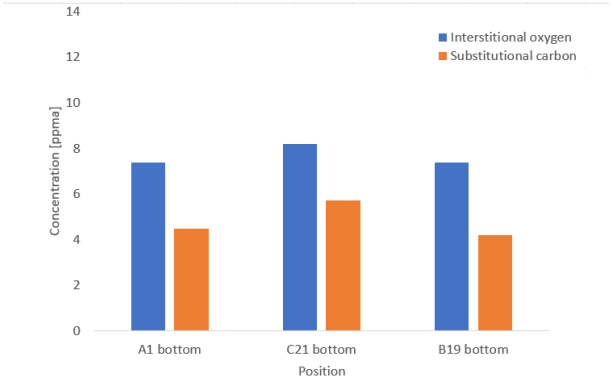
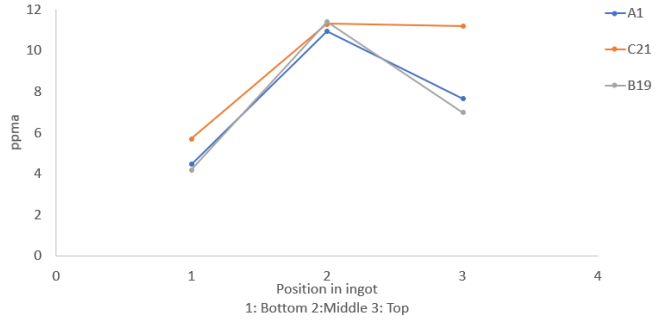


Figure 4.3: FTIR measurements of bottom cut.

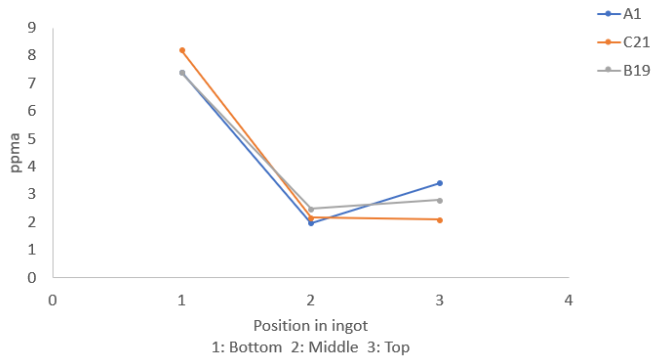
not have detrimental impact on cell performance. However, if concentrations exceed threshold limit/solubility limit in silicon oxygen can form detrimental complexes with eg. boron in the substrate, and bulk recombination may increase.

Table 4.1: Standard deviation for the concentration measurements of substitutional carbon and interstitial oxygen.

	SD oxygen[ppma]	SD carbon[ppma]
A1 bottom	0.24	0.14
A1 middle	0.05	0.14
A1 top	0.66	0.14
B19 bottom	0.38	0.05
B19 middle	0.29	0.22
B19 top	0.08	0.12
C21 bottom	0.02	0.22
C21 middle	0.07	0.24
C21 top	0.03	0.11



(a) Carbon concentration in samples.



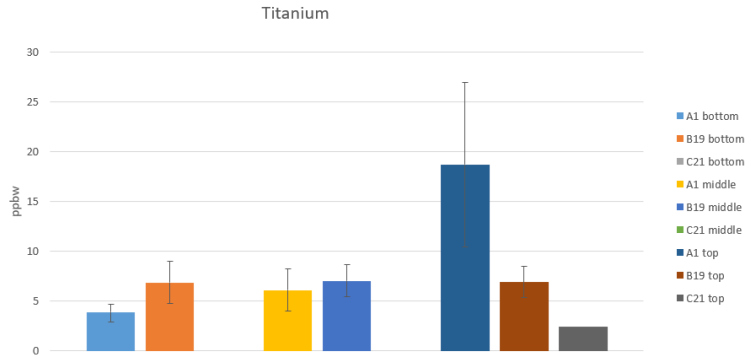
(b) Oxygen concentration in samples.

Figure 4.4: Concentration as a function of height in the ingot.

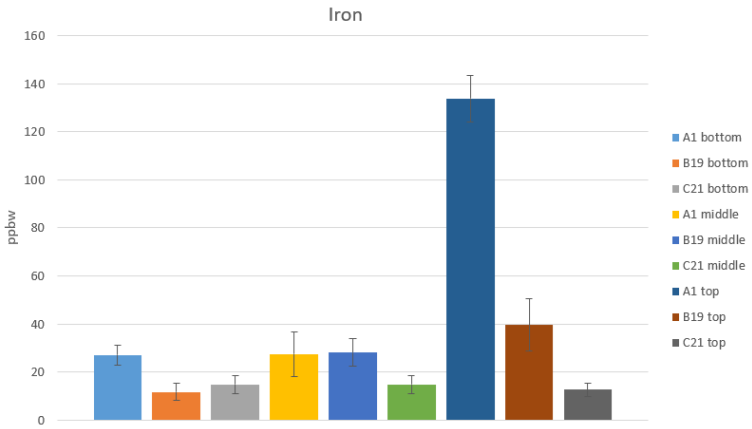
4.1.2 GDMS

The results of the GDMS measurements are presented in Figures 4.5 and 4.6, note the different scales of the y-axis in the diagrams. SD is included on top of the bars.

The concentrations are averages of the last 9-12 measurements after running the analysis for about two hours for each sample. Reviewing the values presented in Figure 2.2 and the acceptable levels of impurity concentration



(a) Titanium content in samples.

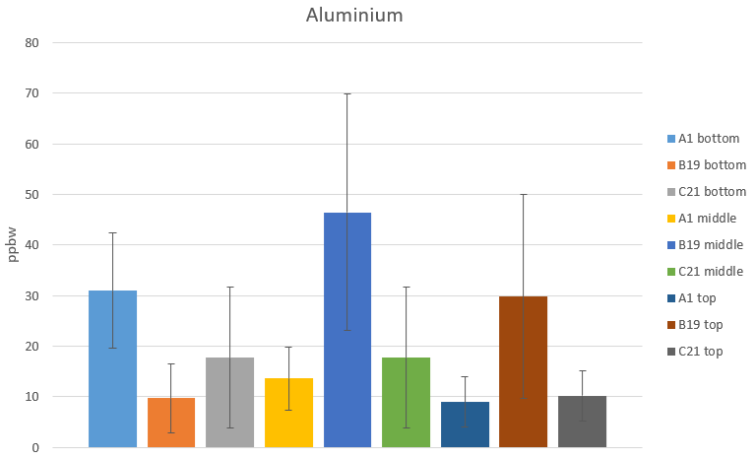


(b) Iron content in samples.

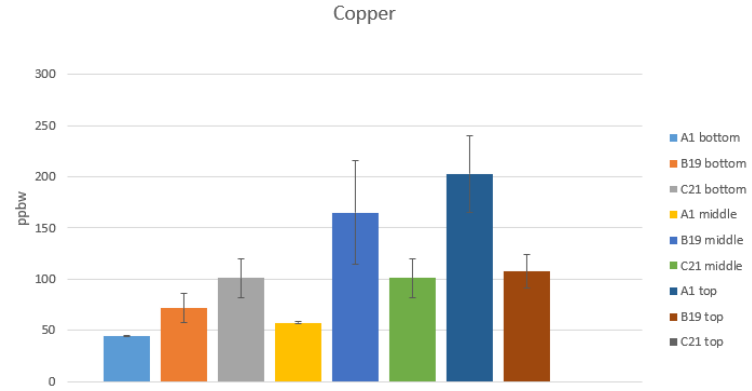
Figure 4.5

for high performance cells, the relevant impurities were as follows; Al: 19 ppbw, Cu: 1 ppbw, Fe: 5 ppbw, Ti:1 ppbw. This means that nearly all measurements do exceed the limit recommended for avoiding detrimental effect of solar cell performance. However, it can be observed in the graphs and the SD lines, some measurements do show a significant deviation compared to the other samples, meaning that these results may be misleading. Raw data for all measurements are presented in Appendix section A, showing

that in some of the measurements SD is very high, indicating that the high concentration measurements may not be valid.



(a) Aluminium content in samples.



(b) Copper content in samples.

Figure 4.6

Further, it was very difficult to stay within just one grain because the sputter crater was 8 mm in diameter and the grains in the samples were smaller. Thereby, comparing the measured concentrations to the values given in Fig-

ure 2.2, may give a wrong interpretation, as it was difficult to perform measurements without hitting GB, which serves as dislocation centres attracting impurities.

Based on the characterization it is difficult to say if further development of solidification process could enhance cell performance or not. Comparing recommended impurity concentration given in Figure 2.2, further development of the casting process to reduce introduction of impurities might be necessary. However, as GDMS results might be misguiding, this may not be the most critical aspect to focus on for improving efficiency. Assuming that Ga-doped wafers would possess similar properties as the B-doped ingot as they have the same casting method and thermal history, it might be more important to focus on the later process steps in the PERC production line to improve efficiency.

4.2 Experimental Results

4.2.1 One-Sided Texturing

The results of the one sided vs. two sided texturing of traditional black mc-Si and black mc-Si PERC is given in Table 4.2 and 4.3. All cell performance parameters presented in the tables in the upcoming sections are averages of the total amount of wafers that were included in the experiments, and the numbers of wafers are given in the tables.

Table 4.2: Performance parameters of traditional black mc-Si with BL (two-sided) and single-sided texturing.

	No.	V_{oc} [V]	I_{sc} [A]	FF [%]	η [%]	$R_s[\Omega]$	$R_{sh}[\Omega]$	$I_0[A]$
BL	47	0.63	9.04	79.00	18.53	0.002	214.70	0.38
SS	47	0.64	9.05	79.92	18.76	0.002	173.70	0.11

Table 4.3: Performance parameters of PERC with BL (two-sided) and single-sided texturing.

	No.	$V_{oc}[V]$	I_{sc}[A]	FF [%]	$\eta[\%]$	$R_s[\Omega]$	$R_{sh}[\Omega]$	I_0[A]
BL	46	0.65	9.40	79.48	19.65	0.002	314.50	0.26
SS	50	0.65	9.36	79.27	19.75	0.002	347.90	0.16

It can be observed that efficiency is improved with more than 0.1% in both cases when only one side is textured. As the rear surface is not textured, it is easier to manufacture a well-passivated rear surface for both cell architectures. Improved passivation of the rear of the cell is expected to improve V_{oc}, however, any profound variation is not observed. It can be observed in the tables that I_0 is decreasing for both architectures when only one side is textured, and a reduction in I_0 can be attributed to a reduction in recombination all over the cell, including surfaces. A reduction in I_0 would be expected to show an improved FF, which is the case for the traditional black mc-Si cell, but not the case for the PERC. By evaluation of the PERC performance parameters, it can be observed that actually no other parameter improves besides I_0 and R_{sh}, indicating that this is the reason for improved η. The SD of the PERC of the V_{oc}, I_{sc}, FF and η, is given in Figure 4.7. By inspection of the graphs, the PERC show a better performance compared to baseline with respect to the V_{oc}, which could not be observed in the aver-

age values in the tables. This can also be an explanation of the improved efficiency.

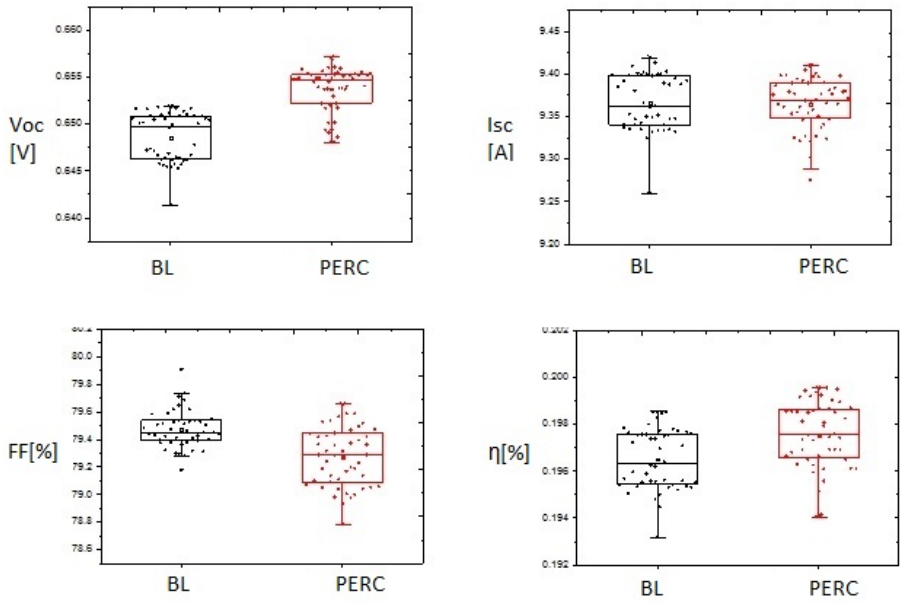


Figure 4.7: The standard deviation of V_{oc}, I_{sc}, FF and η of the PERC cells.

Front Surface State

Results for polish optimization for traditional black mc-Si cells are given in Table 4.4. Two parallels of 150 and 220 seconds polishing were performed, in addition to experiments with 100s and 300s polishing.

It is possible to observe that 150s polishing time showed the highest efficiency improvement both with respect to baseline time and the other times

Table 4.4: Overview of different parameters with varied polishing time for traditional black mc-Si.

Time[s]	No.	V_{oc}[V]	I_{sc}[A]	FF [%]	η [%]	$R_s[\Omega]$	$R_{sh}[\Omega]$	I_0[A]
220	189	0.64	9.07	80.20	18.86	0.002	104.20	0.16
300	181	0.64	9.06	80.30	18.83	0.001	101.50	0.14
150	188	0.64	9.10	80.22	**18.97**	0.002	100.40	0.16
220	193	0.63	9.09	80.46	18.85	0.001	100.70	0.15
150	186	0.64	9.13	80.32	**18.93**	0.002	101.90	0.15
100	182	0.63	9.11	80.25	18.86	0.002	83.20	0.20

investigated. Efficiency increased slightly for the 100s batch compared to baseline, while decreasing for the 300s. Both batches showed an efficiency above 18.9% for the 150s polishing, marked in bold in the table.

Polishing is important because if a uniform surface is achieved, this will improve the MACE with respect to homogeneity of the textured surface, and further achieving a well passivated surface with low enough reflectivity. The goal is to achieve smaller and shallower texture on nanoscale, meaning that pore depth is reduced and pore diameter is decreased.

It can be observed in Table 4.4, that η and I_{sc} are improved compared to baseline for the 150 seconds polishing. This indicates that changing the polishing time improved the surface morphology and made it easier to passivate, thus improving I_{sc} as a result of reduced surface recombination in the front of the cell. The enhanced polishing was also performed on the PERC, though only 150s were tested. The results are summarized in Table 4.5, showing a slight increase in η.

Table 4.5: Cell performance parameters for polishing experiments on cells with PERC architecture.

Time [s]	No.	$V_{oc}[V]$	I_{sc}[A]	FF [%]	$\eta[\%]$	$R_s[\Omega]$	$R_{sh}[\Omega]$	I_0[A]
220	203	0.65	9.36	79.35	19.77	0.002	236.67	0.15
150	376	0.65	9.36	79.54	19.82	0.002	215.82	0.19

4.2.2 Emitter Doping

The position of the wafers in the furnace will impact how they are doped, and sheet resistance measurements were taken from various positions in the furnace. The results of the measurements are given in Figure 4.8. A table of all values is presented in the Appendix, section 2. By comparing the R_{sheet} values measured at 5 different spots in one wafer, it is possible to investigate the doping homogeneity across the wafers.

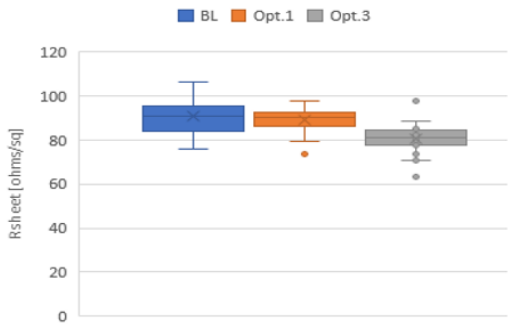


Figure 4.8: Summary of results of sheet resistance measurements.

The goal of the emitter doping experiments was to improve the diffusion process with respect to doping distribution and to reduce the effect of dead layers due to too high doping profiles. This effect can be observed and monitored by measuring the sheet resistance. Low sheet resistance will gener-

ally mean that a high doping concentration profile is achieved. However, if the doping concentration is too high, it might mean that dead layers also are present. A good doping profile means that you have a high amount of active phosphorus close to the surface, without inducing phosporus precipitates. Additionally, it is preferred to have a shallow pn-junction, as a too thick pn-junction will increase recombination. By evaluation of all measurements of R_{sheet}, which are presented in the Appendix, Table 5.1, the SD and averages of the baseline and the tests were calculated, presented in Table 4.6.

Table 4.6: Standard deviation and average of all R_{sheet} measurements of wafers in the boat.

	SD[Ω/sq]	Average [Ω/sq]
Baseline	7.55	90.84
1.opt	5.69	89.10
2.opt	6.71	80.67

If uniform phosphorous doping is achieved, the SD of sheet resistance will be reduced, meaning that all positions in furnace have achieved a uniform gas exposure and doping distribution. If deviations of sheet resistance can be reduced, this can contribute to overall better efficiency.

By investigation of the SD of the measurements across each wafer, it was observed that both new recipes improved the doping homogeneity in total. This is presented in Table 4.7. The positions are head, head middle, middle, middle tail and tail, and they describes the position of the wafer in the boat inside the furnace. It can be observed that the SD across each of the

wafers decreases for all positions except for the head position and middle-tail position for recipe 2.

Table 4.7: Average of all wafers in boat.

Position	BL [Ω/sq]	opt1 [Ω/sq]	opt2[Ω/sq]
H	5.78	8.18	8.60
HM	4.64	1.94	4.56
M	5.39	3.12	2.27
MT	6.38	5.56	7.70
T	8.21	4.65	6.98

The average of all measurements of the sheet resistance is 90.844 Ω/sq for BL, 89.096 Ω/sq for opt1 and 80.672 Ω/sq for opt2. As recipe 2 shows a lower resistance, it is a risk of having introduced phosphorus precipitates. Baseline and recipe 1 show similar average. SD for BL, opt1, opt2 are 7.554, 5.686 and 6.709, respectively. Of this, it is possible to conclude that both optimization recipes improved the doping distribution in the furnace.

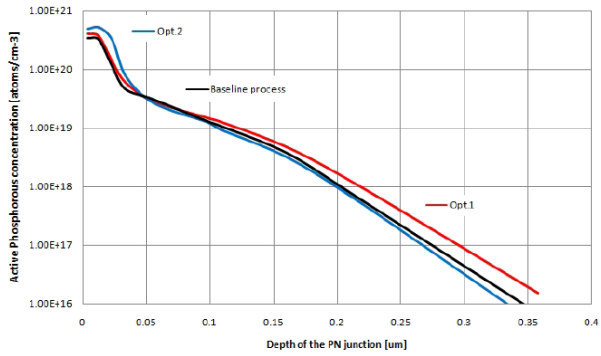


Figure 4.9: The Electrochemical Capacitance-Voltage (ECV) profiling.

In order to investigate the doping profile and the amount of active phosphorus in the wafer with respect to the position, an ECV profiling was performed. The results is presented in Figure 4.9. It can be observed from the figure that both optimization recipes show a higher concentration of active phosphorus in the region close to the surface. Recipe 2 achieved the shallowest pn-junction. Recipe 1 has a slightly thicker emitter region, which can be detrimental as recombination will increase and both I_{sc} and V_{oc} can be reduced.

Final cell performance parameters are given in Table 4.8. Compared to baseline (11 min deposition time), the deposition time of recipe 1 was 14 minutes and 12 minutes for recipe 2. The amount of inflow of nitrogen gas was increased in both cases, whereas the amount of $POCl_3$ was decreased in both cases. The tables illustrates that the FF and the η were increased for both optimization experiments. However, none of the other parameters improved particularly. In the literature, it has been stated flow dynamics plays a significant role in the uniformity of doping. The study by Murukesan *et al.* discussed in the theory chapter, found that by reducing the variation in temperature inside the furnace as exhaust rates was varied, SD of R_{sheet} was reduced. As it is observed a reduction in SD in the experiments performed in this thesis too, this might indicate that the parameters that were varied (inflow of gas and time) did improve temperature variation inside the parameters too. This was however not monitored.

Table 4.8: Cell performance parameters of emitter doping experiments.

Process	No.	V_{oc}[V]	I_{sc}[A]	FF [%]	η [%]	$R_s[\Omega]$	$R_{sh}[\Omega]$	I_0 [A]
BL	373	0.65	9.37	79.32	19.73	0.002	332.98	0.15
opt.1	372	0.66	9.35	79.54	19.83	0.002	255.97	0.15
opt.2	342	0.66	9.35	79.58	19.84	0.002	231.87	0.17

The V_{oc} did not vary greatly between baseline and optimized samples, while baseline I_{sc} was higher. As the sheet resistance was similar to baseline for opt.1, but lower for opt.2, which may be due to an increased amount of precipitates . However, as the V_{oc} did not show any profound variety from the baseline voltage, it can be concluded that the amount of phosphorus was still below the saturation solubility and that detrimental precipitation most likely did not occur. This is validated by the fact that recipe 2 achieved the champion η. FF is improved with both recipes and this is due to the higher doping levels, thus η. Further, as SD is reduced this would also contribute to the improved average η observed.

4.2.3 Rear Surface Passivation

The Al_2O_3 was deposited by ALD and baseline thickness is 14 nm. The baseline annealing time and temperature are 1800 seconds and 520°C, respectively. The results of the experiments are presented in Table 4.9.

The thickness and uniformity of the Al_2O_3 layer is important to achieve good passivation. However, if the layer is too thick, this would obstruct the SiN_y layer from introducing hydrogen passivation at the Al_2O_3/Si interface and Si bulk. Table 4.9 shows that the experiment with increased anneal-

Table 4.9: Cell performance parameters of passivation experiments.

	No.	V_{oc}[V]	I_{sc}[A]	FF%	$\eta[\%]$	$R_s[\Omega]$	$R_{sh}[\Omega]$
Baseline	89	0.65	9.37	79.57	19.75	0.002	219.4
Incr.annealing time	233	0.65	9.39	79.39	19.78	0.002	311.6
Incr.rear thin film	135	0.65	9.42	79.38	19.87	0.002	240.2

ing time did not improve cell efficiency. An excessive thermal budget have been reported to be detrimental for both Q_f and D_{it}, however, with respect to increased temperature. From the results presented here, it is observed that increasing annealing time do not show any great enhancement in efficiency either.

However, by investigating parameters for the increased Al_2O_3-layer thickness, I_{sc} improved and so did η. Improved passivation would reduce the number of recombined photo-generated charge carriers, and thus improve I_{sc} as observed. As enhanced passivation is observed, is can be concluded that the layer was not too thick and H passivation from the SiN_y layer did occur, in combination with good activation of Al_2O_3 leading to both chemical and field-effect passivation.

4.2.4 Overall Optimization

The results based on all of the other experiments were combined to investigate the total effect of the optimized steps in the production line. The results are presented in Table 4.10. It is possible to observe that the combination of the optimization recipes was successful, and a champion efficiency above 20% was achieved.

The η baseline in this experiment was higher than the average η for all baseline PERC measurements. A weighted average of efficiency of all PERC baseline used in this master is 19.78%, meaning that the overall optimized efficiency improved from the average baseline with > 0.2%.

Table 4.10: Cell performance parameters of overall opitmization.

	No.	V_{oc}[V]	I_{sc} [A]	FF[%]	η[%]	$R_s[\Omega]$	$R_{sh}[\Omega]$	I_0[A]
BL	400	0.65	9.42	79.30	19.89	0.00207	276.1	0.073
Comb.	400	0.66	9.42	79.40	20.01	0.00207	311.9	0.068

Internal quantum efficiency (IQE) of baseline and overall optimization is given in Figure 4.10. IQE is the ratio of the number of charge carriers collected by the solar cell to the number of photons of a given energy that shine on the solar cell from outside and are absorbed by the cell. It can be observed that the collection of carriers is higher for the optimized PERC in the region 900-1000 nm. This is consistent with the literature, as the introduction of Al_2O_3 has been found to improve the optical reflectivity at the rear of the cell, and thereby to increase the absorption due to improved

light-trapping, especially in the IR light region (700-1000 nm). The increased thickness of the Al_2O_3 may be the reason for this observation on the optimized PERC in comparison to the baseline PERC. This can further partly be the reason for the enhanced cell efficiency, in combination with improved passivation of surfaces and reduced recombination losses.

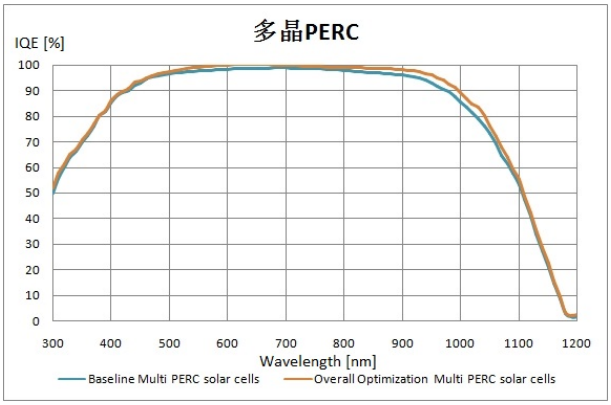


Figure 4.10: Internal quantum efficiency plotted for baseline and overall optimization.

5 | Conclusion

Properties of high performance multi-crytalline silicon and the production line of PERC architectured cells have been investigated, and an optimization route to achieve higher efficiency have been suggested. FTIR and GDMS characterization have been performed on as-cut slabs at 9 different sites in an ingot.

The effect of variation of polisihing time have been investigated at traditional black mc-Si and and mc-Si PERC's. Texturing of only one side, proved to increase more than 0.2% and 0.1% for traditional black mc-Si and black mc-Si PERC, respectively. Different recipes for the emitter doping step in production line was performed, aiming to achieve an improved doping profile and to enhance doping distribution with respect to the wafers position in the furnace and across each wafer. Sheet resistance measurements were performed to investigate the doping profiles.

The rear surface passivation was investigated, and the effect of increased annealing time and increased Al_2O_3- layer thickness was quantified. At last, based on the best results of each of suggested optimization steps, an

overall optimization was performed combining the enhanced steps.

- Reducing the polishing time from 220 to 150 seconds proved to increase average efficiency 0.08% in total, 0.1% for traditional black mc-Si and 0.05% for the PERC.
- Optimized emitter doping was achieved by increasing deposition time from 11 to 12 minutes, and N_2 inflow was increased from 7878 sccm to 7890 sccm, while N_2POCl_3 was reduced from 830 sccm to 810 sccm. 0.11% improvement in efficiency was observed.
- It was achieved a higher concentration of active phosphorus close to the front surface and SD of sheet resistance was reduced with 24%.
- Increasing the thickness of the Al_2O_3 thin film from 14 to 24 nm improved efficiency with 0.12%.
- Final optimization, combining the best results in each of the previous steps, the champion PERC efficiency was 20.01%, 0.23% higher than average BL efficiency of all PERC wafers measured (1111 wafers).

Further improvement of the PERC production line is necessary to reach the 24% limit. PERC design requires a finetuning of influencing parameters that are not linearly interrelated, thus it is a complicated matter to investigate. The results in this study is in agreement with the suggested roadmap (Figure 2.16), and improved efficiency was achieved by optimizing three of the suggested steps. Possible future work could further explore and optimize the steps that have been investigated in this thesis, in combination

with the other steps that are predicted to let current industrial PERC approach the 24% limit.

Bibliography

[1] Department of Economic and Social Affairs. World population prospects: The 2017 revision, 2017.

[2] US Energy Information Administration. International energy outlook 2017, 07 2017.

[3] Tomas Markvart. *Solar electricity 2.ed.* Wiley, Chichestern, 2000.

[4] Erlend Andenæs, Bjørn Petter Jelle, Kristin Ramlo, Tore Kolås, Josefine Selj, and Sean Erik Foss. The influence of snow and ice coverage on the energy generation from photovoltaic solar cells. *Solar Energy*, 159(Supplement C):318 – 328, 2018.

[5] International Energy Agency. Energy technology perspectives 2016.

[6] Y M Yang, A Yu, B Hsu, W C Hsu, A Yang, and C W Lan. Development of high-performance multicrystalline silicon for photovoltaic industry. *Progress in Photovoltaics*, 23(3):340–351, March 2015.

[7] Song Zhang, Fanying Meng, Rune Søndenå, Zhengxin Liu, and Gabriella Tranell. Investigation of nanoscale quasi pyramid texture for hit solar cells using n-type high performance multicrystalline silicon.

Energy Procedia, 124:321 – 330, 2017. 7th International Conference on Silicon Photovoltaics, SiliconPV 2017, 3-5 April 2017, Freiburg, Germany.

[8] Haibing Huang, Jun Lv, Yameng Bao, Rongwei Xuan, Shenghua Sun, Sami Sneck, Shuo Li, Chiara Modanese, Hele Savin, Aihua Wang, and Jianhua Zhao. 20.8efficiency loss mechanisms analysis and roadmap to 24 *Solar Energy Materials and Solar Cells*, 161:14–30, March 2017.

[9] International technology roadmap for photovoltaic results 2017, 03 2018.

[10] Jenny Nelson. *The physics of solar cells*. Imperial College Press, London, 2003.

[11] A. Niv, Z. R. Abrams, M. Gharghi, C. Gladden, and X. Zhang. Overcoming the bandgap limitation on solar cell materials. *Applied Physics Letters*, 100(8), February 2012.

[12] Maulid Mohamed Kivambe. Dislocations in multicrystalline silicon for solar cells : microstructure and sources, 2012.

[13] Priyanka Singh and N.M. Ravindra. Temperature dependence of solar cell performance—an analysis. *Solar Energy Materials and Solar Cells*, 101(Supplement C):36 – 45, 2012.

[14] Tom Markvart and Luis Castañer. Chapter ia-1 - principles of solar cell operation. In Augustin McEvoy, , Tom Markvart, , and Luis Cas-

tañer, editors, *Practical Handbook of Photovoltaics (Second Edition)*, pages 7 – 31. Academic Press, Boston, second edition edition, 2012.

[15] Marie S. Wiig, Krzysztof Adamczyk, Halvard Haug, Kai E. Ekstrøm, and Rune Søndenå. The effect of phosphorus diffusion gettering on recombination at grain boundaries in hpmc-silicon wafers. *Energy Procedia*, 92:886 – 895, 2016. Proceedings of the 6th International Conference on Crystalline Silicon Photovoltaics (SiliconPV 2016).

[16] Martin A Green. Solar cells : operating principles, technology and system applications, 1992.

[17] Karianne Austad. Characterization of electrical activity and lifetime in compensated multicrystalline silicon, 2011.

[18] Armin G Aberle. Surface passivation of crystalline silicon solar cells: a review. *Progress in Photovoltaics: Research and Applications*, 8(5):473–487, September 2000.

[19] T. Bartel, K. Lauer, M. Heuer, M. Kaes, M. Walerysiak, F. Gibaja, J. Lich, J. Bauer, and F. Kirscht. The effect of al and fe doping on solar cells made from compensated silicon. *Energy Procedia*, 27:45 – 52, 2012. Proceedings of the 2nd International Conference on Crystalline Silicon Photovoltaics SiliconPV 2012.

[20] M.P. Bellmann, E.A. Meese, and L. Arnberg. Impurity segregation in directional solidified multi-crystalline silicon. *Journal of Crystal Growth*, 312(21):3091–3095, 2010.

[21] Gaute Stokkan, Di Sabatino Marisa, Rune Sondena, Mari Juel, Antoine Autruffe, Krzysztof Adamczyk, Hanna Vaksvik Skarstad, Kai Erik Ekstrom, Marie Syre Wiig, Chang Chuan You, Halvard Haug, and Mohammed M'Hamdi. Impurity control in high performance multicrystalline silicon.(report). *physica status solidi a - applications and materials science*, 214(7), July 2017.

[22] Hydrogen technology, fuel cells and solar cells. tmt 4285. *Lecture*, February 2016.

[23] Birgit Ryningen. Formation and growth of crystal defects in directionally solidified multicrystalline silicon for solar cells, 2008.

[24] M Dhamrin, H Hashigami, and T Saitoh. Elimination of light-induced degradation with gallium-doped multicrystalline silicon wafers. *Progress In Photovoltaics*, 11(4):231–236, June 2003.

[25] M. Sheoran, A. Upadhyaya, and A. Rohatgi. A comparison of bulk lifetime, efficiency, and light-induced degradation in boron- and gallium-doped cast mc-si solar cells. *Electron Devices, IEEE Transactions on*, 53(11):2764–2772, November 2006.

[26] M. Dhamrin, H. Hashigami, T. Saitoh, I. Yamaga, T. Hirasawa, K. Fukui, K. Shirasawa, and H. Takahashi. Fabrication and evaluation of gallium-doped multicrystalline silicon wafers and solar cells - a promising material for future photovoltaics. volume 1, pages 931–934, Japan, 2003. IEEE.

[27] Francesca Ferrazza. Chapter ib-1 - crystalline silicon: Manufacture and properties. In Augustin McEvoy, , Tom Markvart, , and Luis Castañer, editors, *Practical Handbook of Photovoltaics (Second Edition)*, pages 79 – 97. Academic Press, Boston, second edition edition, 2012.

[28] Merete Tangstad. Chapter 6 - ferrosilicon and silicon technology. In Michael Gasik, editor, *Handbook of Ferroalloys*, pages 179 – 220. Butterworth-Heinemann, Oxford, 2013.

[29] Chandra P Khattak, David B Joyce, and Frederick Schmid. A simple process to remove boron from metallurgical grade silicon. *Solar Energy Materials and Solar Cells*, 74(1):77 – 89, 2002. PVSEC 12 Part I.

[30] H. J. Möller. Wafering of silicon crystals. *physica status solidi (a)*, 203(4):659–669, March 2006.

[31] Kazuaki Tomono, Seiji Miyamoto, Takuro Ogawa, Hirotoshi Furuya, Yuki Okamura, Makoto Yoshimoto, Ryuichi Komatsu, and Masaharu Nakayama. Recycling of kerf loss silicon derived from diamond-wire saw cutting process by chemical approach. *Separation and Purification Technology*, 120:304 – 309, 2013.

[32] Samir Ahmad, Cheow Leong, K. Sopian, and Saleem Zaidi. Role of firing temperature, sheet resistance, and contact area in contact formation on screen-printed metal contact of silicon solar cell. *Journal of Electronic Materials*, 47(3):2120–2134, March 2018.

[33] H. Ghembaza, A. Zerga, R. Saïm, and M. Pasquinelli. Optimization of phosphorus emitter formation from pocl 3 diffusion for p-type silicon solar cells processing. *Silicon*, 10(2):377–386, March 2018.

[34] Karthick Murukesan, Sandeep Kumbhar, A K Kapoor, A Dhaul, Saravanan S, Richard Pinto, and B M Arora. *POCl<inf>3</inf> diffusion process optimization for the formation of emitters in the crystalline silicon solar cells*. 2014 IEEE 40th Photovoltaic Specialists Conference (PVSC). IEEE, 2014.

[35] Toni Pasanen, Hannu Laine, Ville Vähänissi, Jonas Schön, and Hele Savin. Black silicon significantly enhances phosphorus diffusion gettering. *Sci Rep*, 8(1):1991–1991, December 2018.

[36] Mohammad Ziaur Rahman and Shahidul Islam Khan. Advances in surface passivation of c-si solar cells. *Materials for Renewable and Sustainable Energy*, 1(1):1, Oct 2012.

[37] G. Stokkan, Y. Hu, Ø. Mjøs, and M. Juel. Study of evolution of dislocation clusters in high performance multicrystalline silicon. *Solar Energy Materials and Solar Cells*, 130:679 – 685, 2014.

[38] H.J. Möller. Basic mechanisms and models of multi-wire sawing. 6:501 – 513, 07 2004.

[39] Hao Wu. Wire sawing technology: A state-of-the-art review. *Precision Engineering*, 43:1 – 9, 2016.

[40] Jozef Szlufcik, S. Sivoththaman, Johan F. Nijs, Robert P. Mertens, and Roger Van Overstraeten. Chapter ib-3 - low-cost industrial technolo-

gies for crystalline silicon solar cells1. In Augustin McEvoy, , Tom Markvart, , and Luis Castañer, editors, *Practical Handbook of Photovoltaics (Second Edition)*, pages 129 – 159. Academic Press, Boston, second edition edition, 2012.

[41] S. R. Chen, Z. C. Liang, and D. L. Wang. Nano silver-catalyzed chemical etching of polycrystalline silicon wafer for solar cell application. *AIP Advances*, 6(3):035320, 2016.

[42] Erik Garnett and Peidong Yang. Light trapping in silicon nanowire solar cells. *Nano Letters*, 10(3):1082–1087, March 2010.

[43] Howard M. Branz, Vernon E. Yost, Scott Ward, Kim M. Jones, Bobby To, and Paul Stradins. Nanostructured black silicon and the optical reflectance of graded-density surfaces. *Applied Physics Letters*, 94(23):231121, 2009.

[44] Zengchao Zhao, Ping Li, Yi Wei, Chunxi Lu, Xin Tan, and Aimin Liu. 17.3antireflection coating. *Solar Energy*, 110:714–719, December 2014.

[45] Fenqin Hu, Yun Sun, Jiawei Zha, Kexun Chen, Shuai Zou, Liang Fang, and Xiaodong Su. Pre-texturing multi-crystalline silicon wafer via a two-step alkali etching method to achieve efficient nanostructured solar cells. *Solar Energy Materials and Solar Cells*, 159:121–127, January 2017.

[46] Xiaogang Liu, Paul R. Coxon, Marius Peters, Bram Hoex, Jacqueline M. Cole, and Derek J. Fray. Black silicon: fabrication methods,

properties and solar energy applications. *Energy & Environmental Science*, 7(10):3223–3263, September 2014.

[47] Zp Huang, N Geyer, P Werner, J de Boor, and U Gosele. Metal-assisted chemical etching of silicon: A review. *Advanced Materials*, 23(2):285–308, January 2011.

[48] C. Chartier, S. Bastide, and C. Lévy-Clément. Metal-assisted chemical etching of silicon in hf–h 2o 2. *Electrochimica Acta*, 53(17):5509–5516, 2008.

[49] Zhihao Yue, Honglie Shen, Ye Jiang, Weilong Chen, Quntao Tang, Jiale Jin, Tian Pu, Jingwang Luo, Fanjian Kong, Chunbao Rui, and Jibo Cai. Large-scale black multi-crystalline silicon solar cell with conversion efficiency over 18 *Applied Physics A*, 116(2):683–688, August 2014.

[50] Xiaoya Ye, Shuai Zou, Kexun Chen, Jianjiang Li, Jie Huang, Fang Cao, Xusheng Wang, Lingjun Zhang, Xue-Feng Wang, Mingrong Shen, and Xiaodong Su. 18.45%-efficient multi-crystalline silicon solar cells with novel nanoscale pseudo-pyramid texture. *Advanced Functional Materials*, 24(42):6708–6716, November 2014.

[51] J. Schmidt, F. Werner, B. Veith, D. Zielke, S. Steingrube, P.P. Altermatt, S. Gatz, T. Dullweber, and R. Brendel. Advances in the surface passivation of silicon solar cells. *Energy Procedia*, 15:30 – 39, 2012. International Conference on Materials for Advanced Technologies 2011, Symposium O.

[52] Matthias Byungsul Min, Hannes Muller, Gerd Wagner, Rolf Fischer, Pietro P. Brendel, Holger Altermatt, and Holger Neuhaus. A roadmap toward 24% efficient perc solar cells in industrial mass production. *Photovoltaics, IEEE Journal of*, 7(6):1541–1550, November 2017.

[53] Thorsten Dullweber and Jan Schmidt. Industrial silicon solar cells applying the passivated emitter and rear cell (perc) concept, review. *Photovoltaics, IEEE Journal of*, 6(5):1366–1381, September 2016.

[54] Stefan Dauwe, Lutz Mittelstädt, Axel Metz, and Rudolf Hezel. Experimental evidence of parasitic shunting in silicon nitride rear surface passivated solar cells. *Progress in Photovoltaics: Research and Applications*, 10(4):271–278, June 2002.

[55] J. Benick, A. Richter, T.-T. A. Li, N. E. Grant, K. R. Mcintosh, Y. Ren, K. J. Weber, M. Hermle, and S. W. Glunz. Effect of a post-deposition anneal on al<inf>2</inf>o<inf>3</inf>/si interface properties. pages 000891–000896. IEEE Publishing, June 2010.

[56] Daniel Kray, Martin Hermle, and Stefan W. Glunz. Theory and experiments on the back side reflectance of silicon wafer solar cells. *Progress in Photovoltaics: Research and Applications*, 16(1):1–15, January 2008.

Appendix

5.1 Section A: GDMS Results

Rejected	Matrix	Sec isotope	Excluded	Not Acquired			
Element	**4998.raw**	**4999.raw**	**5000.raw**	**5001.raw**	**5002.raw**	**5003.raw**	**5004.raw**
Al27	14.702 ppb	26.541 ppb	54.994 ppb	31.680 ppb	46.810 ppb	34.470 ppb	30.899 ppb
Si28	100.00 %	100.00 %	100.00 %	100.00 %	100.00 %	100.00 %	100.00 %
Ti48	3.013 ppb	1.554 ppb	1.610 ppb	1.623 ppb	1.599 ppb	0.000 ppb	0.000 ppb
Fe56	14.410 ppb	11.891 ppb	18.480 ppb	9.315 ppb	18.351 ppb	9.009 ppb	18.171 ppb
Cu63	18.960 ppb	0.000 ppb	0.000 ppb	0.000 ppb	20.122 ppb	19.757 ppb	19.924 ppb
Element	**5005.raw**	**5006.raw**	**5007.raw**	**5008.raw**	**5009.raw**	**Average**	**Std Dev**
Al27	39.015 ppb	27.047 ppb	38.291 ppb	19.315 ppb	23.517 ppb	32.273 ppb	11.401 ppb
Si28	100.00 %	100.00 %	100.00 %	100.00 %	100.00 %	100.00 %	0.000 ppb
Ti48	0.000 ppb	3.167 ppb	3.139 ppb	1.583 ppb	3.213 ppb	2.278 ppb	0.813 ppb
Fe56	15.296 ppb	9.089 ppb	9.007 ppb	12.116 ppb	18.439 ppb	13.631 ppb	4.048 ppb
Cu63	0.000 ppb	19.932 ppb	0.000 ppb	19.927 ppb	0.000 ppb	19.770 ppb	0.413 ppb

Figure 5.1: A1 bottom

Rejected	Matrix	Sec isotope	Excluded	Not Acquired			
Element	**4896.raw**	**4897.raw**	**4898.raw**	**4899.raw**	**4900.raw**	**4901.raw**	**4902.raw**
Al27	19.903 ppb	19.466 ppb	9.804 ppb	9.465 ppb	9.849 ppb	9.766 ppb	4.838 ppb
Si28	100.00 %	100.00 %	100.00 %	100.00 %	100.00 %	100.00 %	100.00 %
Ti48	2.039 ppb	0.000 ppb	6.027 ppb	0.000 ppb	2.018 ppb	0.000 ppb	1.983 ppb
Fe56	0.000 ppb	3.816 ppb	7.687 ppb	18.553 ppb	19.306 ppb	15.315 ppb	18.965 ppb
Cu63	0.000 ppb	25.103 ppb	0.000 ppb	0.000 ppb	0.000 ppb	0.000 ppb	0.000 ppb
Element	**4903.raw**	**4904.raw**	**4905.raw**	**4906.raw**	**4907.raw**	**Average**	**Std Dev**
Al27	9.357 ppb	19.156 ppb	25.093 ppb	19.606 ppb	14.424 ppb	14.227 ppb	6.210 ppb
Si28	100.00 %	100.00 %	100.00 %	100.00 %	100.00 %	100.00 %	0.000 ppb
Ti48	5.753 ppb	0.000 ppb	0.000 ppb	0.000 ppb	0.000 ppb	3.564 ppb	2.126 ppb
Fe56	3.668 ppb	33.794 ppb	7.870 ppb	3.843 ppb	18.849 ppb	13.788 ppb	9.387 ppb
Cu63	0.000 ppb	0.000 ppb	25.889 ppb	0.000 ppb	0.000 ppb	25.496 ppb	0.555 ppb

Figure 5.2: A1 middle

Rejected	Matrix	Sec isotope	Excluded	Not Acquired		
Element	**5282.raw**	**5283.raw**	**5284.raw**	**5285.raw**	**5286.raw**	**5287.raw**
Al27	0.000 ppb	5.563 ppb	5.387 ppb	5.643 ppb	5.535 ppb	11.068 ppb
Si28	100.00 %	100.00 %	100.00 %	100.00 %	100.00 %	100.00 %
Ti48	23.560 ppb	22.801 ppb	17.662 ppb	2.313 ppb	0.000 ppb	9.073 ppb
Fe56	67.605 ppb	69.788 ppb	67.575 ppb	66.373 ppb	82.454 ppb	69.426 ppb
Cu63	148.259 ppb	57.392 ppb	111.145 ppb	58.223 ppb	85.653 ppb	85.642 ppb
Element	**5288.raw**	**5289.raw**	**5290.raw**	**5291.raw**	**Average**	**Std Dev**
Al27	16.730 ppb	17.262 ppb	5.674 ppb	11.516 ppb	9.375 ppb	4.957 ppb
Si28	100.00 %	100.00 %	100.00 %	100.00 %	100.00 %	0.000 ppb
Ti48	6.857 ppb	7.075 ppb	6.977 ppb	2.360 ppb	10.964 ppb	8.246 ppb
Fe56	69.960 ppb	54.141 ppb	48.935 ppb	76.747 ppb	67.300 ppb	9.708 ppb
Cu63	143.835 ppb	89.049 ppb	29.268 ppb	89.104 ppb	89.757 ppb	37.327 ppb

Figure 5.3: A1 top

Rejected	Matrix	Sec isotope	Excluded	Not Acquired		
Element	**5334.raw**	**5335.raw**	**5336.raw**	**5337.raw**	**5338.raw**	**5339.raw**
Al27	3.232 ppb	9.816 ppb	3.325 ppb	10.024 ppb	3.194 ppb	19.771 ppb
Si28	100.00 %	100.00 %	100.00 %	100.00 %	100.00 %	100.00 %
Ti48	7.948 ppb	2.682 ppb	4.089 ppb	2.739 ppb	0.000 ppb	2.701 ppb
Fe56	5.068 ppb	2.566 ppb	5.214 ppb	10.479 ppb	7.512 ppb	10.335 ppb
Cu63	16.671 ppb	33.758 ppb	51.458 ppb	17.236 ppb	0.000 ppb	33.997 ppb
Element	**5340.raw**	**5341.raw**	**5342.raw**	**5343.raw**	**Average**	**Std Dev**
Al27	3.338 ppb	19.674 ppb	16.172 ppb	12.939 ppb	10.149 ppb	6.804 ppb
Si28	100.00 %	100.00 %	100.00 %	100.00 %	100.00 %	0.000 ppb
Ti48	0.000 ppb	2.688 ppb	2.651 ppb	6.629 ppb	4.016 ppb	2.106 ppb
Fe56	2.617 ppb	10.284 ppb	2.536 ppb	2.536 ppb	5.915 ppb	3.466 ppb
Cu63	0.000 ppb	33.830 ppb	16.685 ppb	50.060 ppb	31.712 ppb	14.152 ppb

Figure 5.4: B19 bottom

Rejected	Matrix	Sec isotope	Excluded	Not Acquired			
Element	**5220.raw**	**5221.raw**	**5222.raw**	**5223.raw**	**5224.raw**	**5225.raw**	**5226.raw**
Al27	51.423 ppb	14.304 ppb	77.546 ppb	35.470 ppb	36.614 ppb	54.007 ppb	48.799 ppb
Si28	100.00 %	100.00 %	100.00 %	100.00 %	100.00 %	100.00 %	100.00 %
Ti48	6.022 ppb	0.000 ppb	0.000 ppb	5.815 ppb	3.001 ppb	0.000 ppb	0.000 ppb
Fe56	17.280 ppb	5.608 ppb	22.110 ppb	0.000 ppb	11.483 ppb	15.880 ppb	10.932 ppb
Cu63	0.000 ppb	0.000 ppb	0.000 ppb	0.000 ppb	0.000 ppb	0.000 ppb	0.000 ppb
Element	**5227.raw**	**5228.raw**	**5229.raw**	**5230.raw**	**5231.raw**	**Average**	**Std Dev**
Al27	69.928 ppb	85.015 ppb	7.250 ppb	57.710 ppb	42.213 ppb	48.357 ppb	23.318 ppb
Si28	100.00 %	100.00 %	100.00 %	100.00 %	100.00 %	100.00 %	0.000 ppb
Ti48	0.000 ppb	2.904 ppb	0.000 ppb	0.000 ppb	2.884 ppb	4.125 ppb	1.639 ppb
Fe56	21.932 ppb	5.555 ppb	11.369 ppb	16.968 ppb	16.549 ppb	14.151 ppb	5.678 ppb
Cu63	0.000 ppb	0.000 ppb	0.000 ppb	37.212 ppb	108.878 ppb	73.045 ppb	50.676 ppb

Figure 5.5: B19 middle

Rejected	Matrix	Sec isotope	Excluded	Not Acquired			
Element	**5118.raw**	**5119.raw**	**5120.raw**	**5121.raw**	**5122.raw**	**5123.raw**	**5124.raw**
Al27	55.072 ppb	48.252 ppb	7.675 ppb	55.099 ppb	56.156 ppb	31.896 ppb	23.358 ppb
Si28	100.00 %	100.00 %	100.00 %	100.00 %	100.00 %	100.00 %	100.00 %
Ti48	0.000 ppb	0.000 ppb	0.000 ppb	3.226 ppb	3.288 ppb	3.268 ppb	0.000 ppb
Fe56	37.012 ppb	25.223 ppb	24.071 ppb	12.344 ppb	12.580 ppb	0.000 ppb	30.524 ppb
Cu63	40.584 ppb	0.000 ppb	0.000 ppb	81.209 ppb	41.383 ppb	0.000 ppb	0.000 ppb
Element	**5125.raw**	**5126.raw**	**5127.raw**	**5128.raw**	**5129.raw**	**Average**	**Std Dev**
Al27	7.821 ppb	16.176 ppb	7.817 ppb	47.293 ppb	15.913 ppb	31.044 ppb	20.184 ppb
Si28	100.00 %	100.00 %	100.00 %	100.00 %	100.00 %	100.00 %	0.000 ppb
Ti48	6.412 ppb	0.000 ppb	0.000 ppb	0.000 ppb	0.000 ppb	4.049 ppb	1.576 ppb
Fe56	0.000 ppb	25.367 ppb	6.129 ppb	0.000 ppb	6.238 ppb	19.943 ppb	11.001 ppb
Cu63	0.000 ppb	0.000 ppb	40.326 ppb	40.661 ppb	41.043 ppb	47.534 ppb	16.501 ppb

Figure 5.6: B19 top

Rejected	Matrix	Sec isotope	Excluded	Not Acquired			
Element	**3812.raw**	**3813.raw**	**3814.raw**	**3815.raw**	**3816.raw**	**3817.raw**	
Al27	51.291 ppb	19.674 ppb	0.000 ppb	6.243 ppb	12.510 ppb	0.000 ppb	
Si28	100.00 %	100.00 %	100.00 %	100.00 %	100.00 %	100.00 %	
Ti48	0.000 ppb	0.000 ppb	0.000 ppb	0.000 ppb	0.000 ppb	0.000 ppb	
Fe56	5.027 ppb	0.000 ppb	4.942 ppb	9.790 ppb	4.905 ppb	14.586 ppb	
Cu63	66.146 ppb	33.830 ppb	0.000 ppb	0.000 ppb	0.000 ppb	0.000 ppb	
Element	**3818.raw**	**3819.raw**	**3820.raw**	**3821.raw**	**3822.raw**	**Average**	**Std Dev**
Al27	0.000 ppb	12.785 ppb	19.143 ppb	13.088 ppb	13.190 ppb	18.490 ppb	13.904 ppb
Si28	100.00 %	100.00 %	100.00 %	100.00 %	100.00 %	100.00 %	0.000 ppb
Ti48	0.000 ppb	0.000 ppb	0.000 ppb	0.000 ppb	0.000 ppb		0.000 ppb
Fe56	0.000 ppb	10.024 ppb	0.000 ppb	5.131 ppb	5.171 ppb	7.447 ppb	3.630 ppb
Cu63	0.000 ppb	0.000 ppb	0.000 ppb	0.000 ppb	34.021 ppb	44.666 ppb	18.603 ppb

Figure 5.7: C21 bottom

Rejected	Matrix	Sec isotope	Excluded	Not Acquired			
Element	**3812.raw**	**3813.raw**	**3814.raw**	**3815.raw**	**3816.raw**	**3817.raw**	
Al27	51.291 ppb	19.674 ppb	0.000 ppb	6.243 ppb	12.510 ppb	0.000 ppb	
Si28	100.00 %	100.00 %	100.00 %	100.00 %	100.00 %	100.00 %	
Ti48	0.000 ppb	0.000 ppb	0.000 ppb	0.000 ppb	0.000 ppb	0.000 ppb	
Fe56	5.027 ppb	0.000 ppb	4.942 ppb	9.790 ppb	4.905 ppb	14.586 ppb	
Cu63	66.146 ppb	33.830 ppb	0.000 ppb	0.000 ppb	0.000 ppb	0.000 ppb	
Element	**3818.raw**	**3819.raw**	**3820.raw**	**3821.raw**	**3822.raw**	**Average**	**Std Dev**
Al27	0.000 ppb	12.785 ppb	19.143 ppb	13.088 ppb	13.190 ppb	18.490 ppb	13.904 ppb
Si28	100.00 %	100.00 %	100.00 %	100.00 %	100.00 %	100.00 %	0.000 ppb
Ti48	0.000 ppb	0.000 ppb	0.000 ppb	0.000 ppb	0.000 ppb		0.000 ppb
Fe56	0.000 ppb	10.024 ppb	0.000 ppb	5.131 ppb	5.171 ppb	7.447 ppb	3.630 ppb
Cu63	0.000 ppb	0.000 ppb	0.000 ppb	0.000 ppb	34.021 ppb	44.666 ppb	18.603 ppb

Figure 5.8: C21 middle

Rejected	Matrix	Sec isotope	Excluded	Not Acquired		
Element	**3711.raw**	**3712.raw**	**3713.raw**	**3714.raw**	**3715.raw**	**3716.raw**
Al27	14.462 ppb	7.062 ppb	10.461 ppb	14.207 ppb	7.200 ppb	10.248 ppb
Si28	100.00 %	100.00 %	100.00 %	100.00 %	100.00 %	100.00 %
Ti48	0.000 ppb	0.000 ppb	1.429 ppb	0.000 ppb	0.000 ppb	0.000 ppb
Fe56	5.670 ppb	11.074 ppb	5.468 ppb	0.000 ppb	5.645 ppb	8.035 ppb
Cu63	0.000 ppb	0.000 ppb	0.000 ppb	0.000 ppb	0.000 ppb	0.000 ppb
Element	**3717.raw**	**3718.raw**	**3719.raw**	**3720.raw**	**Average**	**Std Dev**
Al27	3.615 ppb	21.236 ppb	6.883 ppb	11.012 ppb	10.639 ppb	5.034 ppb
Si28	100.00 %	100.00 %	100.00 %	100.00 %	100.00 %	0.000 ppb
Ti48	0.000 ppb	0.000 ppb	0.000 ppb	0.000 ppb	1.429 ppb	
Fe56	5.670 ppb	2.775 ppb	0.000 ppb	0.000 ppb	6.334 ppb	2.586 ppb
Cu63	0.000 ppb	0.000 ppb	0.000 ppb	0.000 ppb		0.000 ppb

Figure 5.9: C21 top

5.2 Section B: Sheet Resistance Measurements

Table 5.1: Sheet resistance measurements on wafers at different positions in the furnace.

	Pos.	C1	C2	C3	C4	C5	Av.
BL	H	92.1	84	84.3	83.1	75.8	83.9
BL	HM	94.5	89.4	87.8	92.1	82.3	89.2
BL	M	95.1	97.9	91.6	83.9	89.4	91.6
BL	MT	103.7	106.4	90.1	96.4	98.9	99.1
BL	T	102.7	90.7	83.5	82.4	93.0	90.5
opt1	H	94.5	90.1	79.6	85.0	73.9	84.6
opt1	HM	95.0	93.2	92.5	92.5	89.6	92.6
opt1	M	92.6	90.4	87.9	90.3	84.4	89.1
opt1	MT	82.7	92.1	79.3	88.3	91.3	86.7
opt1	T	96.9	90.7	87.0	89.9	97.7	92.4
opt2	H	86.8	79.2	80.1	78.5	63.4	77.6
opt2	HM	77.4	81.3	73.8	81.0	70.8	76.9
opt2	M	82.4	83.6	79.6	79.8	78.0	80.7
opt2	MT	97.9	83.7	77.4	81.7	85.1	85.2
opt2	T	84.5	85.9	70.9	85.3	88.7	83.1

C1 is the center of the wafers, while C2-C5 represents each of the corners. The wafers in the furnace are named H-Head, HM-Head Middle, M-Middle, MT-Middle Tail, and T-Tail, and represent the different sites in the boat. All numbers in the table are given in the unit Ω/sq.