Muhammad Jafar

Transformer-Less Series Compensation of Line-Commutated Converters for Integration of Offshore Wind Power

Thesis for the degree of Philosophiae Doctor

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Norwegian University of Science and Technology
Faculty of Information Technology, Mathematics
and Electrical Engineering
Department of Electric Power Engineering

NTNU – Trondheim
Norwegian University of
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Muhammad Jafar

Abstract

Wind energy is gradually becoming a major contributor to the overall energy production, especially in the developed world. This is because of the ever- increasing concerns about long-term availability of conventional fuels, global warming, and energy security. Wind power production is gradually moving offshore because of scarcity of onshore sites (particularly in Europe), environmentalists' concerns over noise and visual pollution, and better wind conditions out in the open sea. Offshore wind farms are generally located close to the shore currently in shallow waters. However, more power demand from wind will eventually put more and more wind farms farther out in the deep sea. This would require floating turbine and grid-integration platforms.

This is where High Voltage Direct Current (HVDC) interconnection between the offshore power plant and the onshore grid would become more attractive than the AC option. The power to be transmitted, if in excess of a certain amount, would necessitate either multiple Voltage Sourced Converter based HVDC (VSC HVDC) links or a single Line Commutated Converter based HVDC (LCC HVDC) link. The latter could be a cheaper option.

LCC HVDC is and will remain the preferred choice for point-to-point transmission of bulk power in the foreseeable future due to it being a proven technology in use for more than half a century, its lower losses, and high power and voltage capability. There remain inherent issues of black-start, high content of lower-order harmonics, and high fundamental-frequency reactive-power consumption. The reactive power and harmonics are traditionally compensated-for by shunt-connected passive filters, which take up a lot of area and make the LCC HVDC terminal size large and expensive. In a deep-sea offshore perspective, this would increase the cost of the floating platform.

This work has explored the possibilities of improvement in transformer-less series compensation of LCC HVDC so as to reduce the size of the converter terminal. The behaviour of the capacitor commutated converter based HVDC (CCC HVDC) was first compared to the conventional system. Later on, the Gate Commutated Series Capacitor (GCSC) was analysed for its potential in the reduction of the converter terminal size.

The work ultimately culminated in the proposal of a new compensator termed the Series Pulsed Voltage Compensator (SPVC), which is a transformer-less series-connected compensator employing full bridges. The compensator reduces the reactive-power consumption of the HVDC terminal in addition to compensating for the reactive-power consumption of the heavy leakage reactances of the converter transformers. It also reduces the lower-order current harmonics. The compensator demonstrates the capability to follow the changes in reactive-power reference at any given active-power

flow, a functionality which would eliminate the switching requirements employed in the conventional shunt compensation technique. Experiments on a small-scale laboratory setup have validated the simulation results.

The functionalities mentioned above have been achieved using very small capacitors in the SPVC. This indicates a potentially significant reduction in the need for shunt-connected capacitor banks and large passive-filter inductors with associated switchgear for reactive and harmonic compensation. This would result in a sizeable reduction in the size of the LCC HVDC terminal.

The simulation and modelling of an active shunt-connected reactive/harmonic compensator based on the relatively recent Conservative Power Theory is also presented in the appendix A. In addition, a few suggestions for improving the dynamic behaviour of the HVDC control loops are presented in appendix B.

Contents

1 Introduction

This chapter briefly discusses the global energy consumption and generation and the growing role of wind power in the energy mix. In addition, high voltage direct current transmission is introduced as one of the possible solutions for offshore wind-power integration. The major contributions of this research are also outlined.

The global energy consumption is increasing gradually with the increase in world population and elevated living standards as a result of development. Consumption of electrical energy is also increasing. In the recent past, the concerns over environment [1-4], depletion of fossil fuel reserves [5-7], and energy security [8, 9] have led to development and deployment of renewable energy sources [10-12]. In what follows, we will discuss these issues one by one.

1.1 Trends in Global Energy Supply and Consumption

The energy consumption of the world has almost doubled from 4.674 Mtoe (Million tons of oil equivalent) in 1973 to 8,353 Mtoe in 2009 [13]. The percentages of different forms in which energy was being consumed as in 1973 and 2009 are depicted in Fig. 1–1 and Fig. 1–2 respectively [13]. As can be seen, the use of energy in the form of electricity has almost doubled from 9.4% to 17.3%. It should be noted that the energy consumption has also doubled. Therefore, the penetration of electricity as a form of consumption of energy has almost quadrupled. However, looking at Fig. 1–3 and Fig. 1–4 [13], we observe that the collective share of coal, oil, and natural gas in the production of electricity has decreased by 10% from nearly 75% to almost 65%.

The details in [13] reveal that major forms of fossil fuel consumption is in the transport sector. The share of renewable energy sources can be significantly enhanced if the use of electric power is extended to mobile applications. If reliable, long-life, low-cost, compact, and sustainable energy storage technologies are made available, only then can the penetration of electric power to transport applications be realized. This will be the time when the dream of effectively mitigating global warming can be realistically achieved. Nonetheless, the conversion of current electric power sources to renewable will itself be a huge achievement as well as inevitable [14-17].

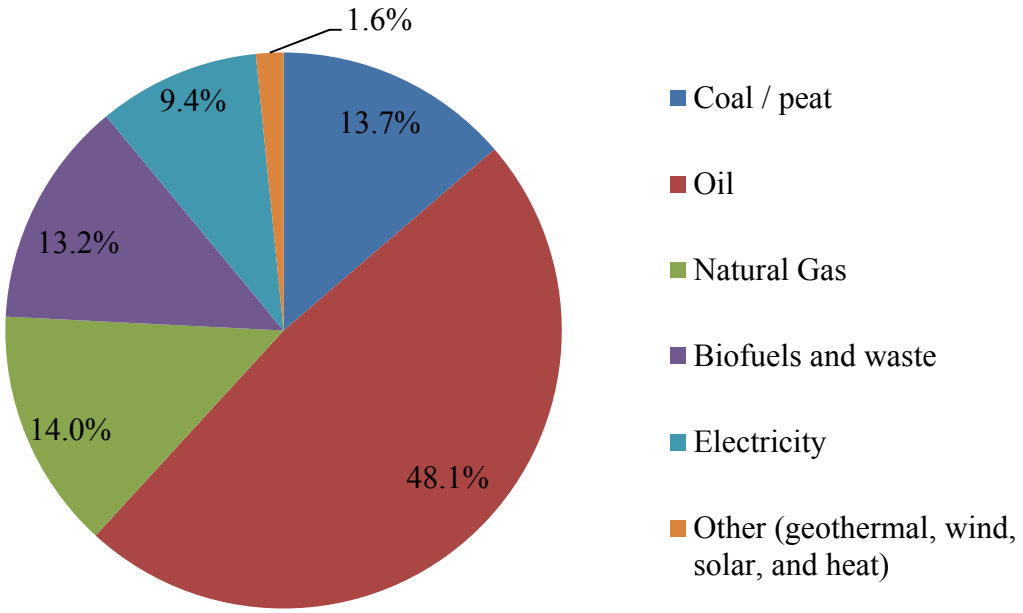

Fig. 1–1. Breakdown of the sources of energy of the world as in 1973.

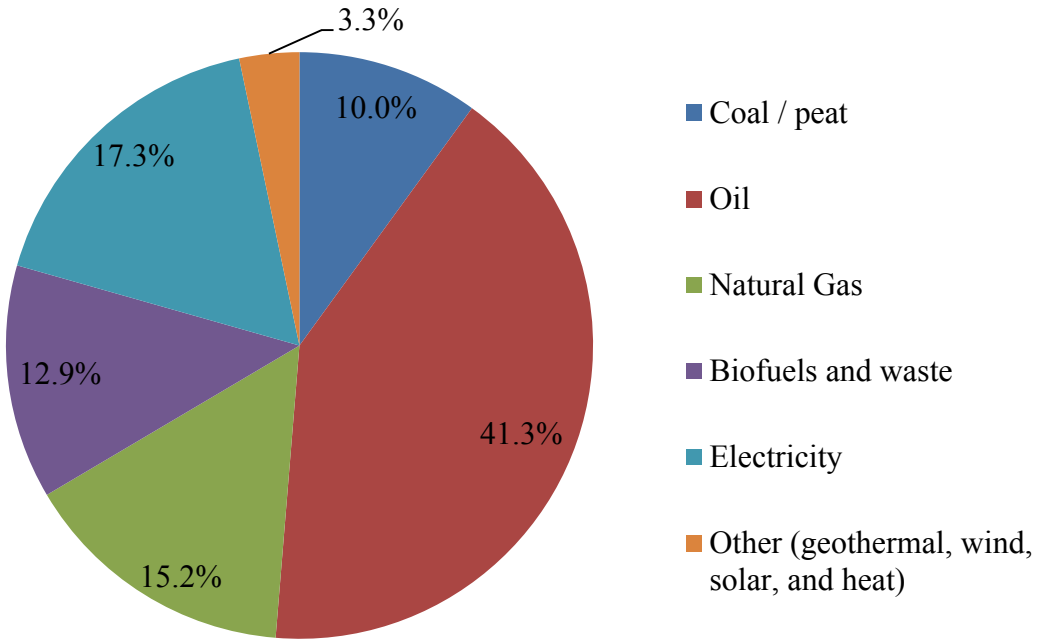

Fig. 1–2. Breakdown of the sources of energy of the world as in 2009.

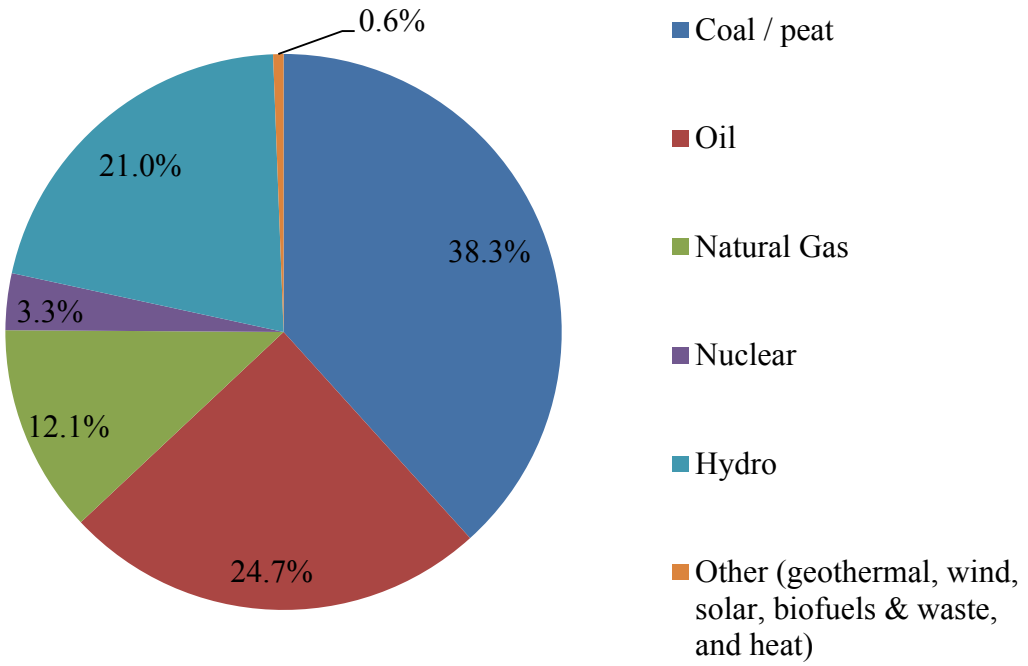

Fig. 1–3. Primary sources for electricity generation as in 1973.

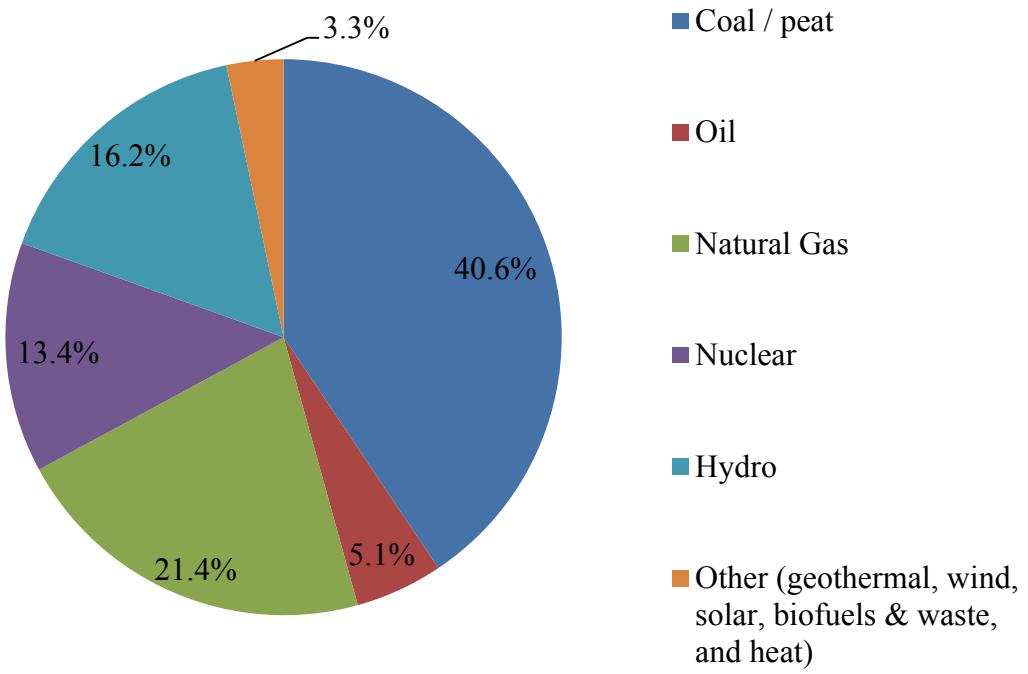

Fig. 1–4. Primary sources for electricity generation as in 2009.

1.2 Wind Power

Wind power [18-20] has seen enormous growth in the past couple of decades [21, 22]. The scarcity of land in Europe and opposition to visual and noise pollution [23, 24] are forcing the planners and developers offshore [25]; the additional advantage being better

wind conditions. The researchers and planners envisage a European super-grid that would integrate the renewable resources much more efficiently and increase their penetration into the energy mix [26]. The technology of all the components required in such a system is growing rapidly [27-30].

1.3 Deep-Sea Offshore Wind Power

Currently, the offshore wind plants are located in shallow waters close to the coast [31, 32]. The implications are solid foundations for turbine & grid-integration platforms and AC connection to the onshore grid. The distance to shore is going to increase in the future [33]. This will result into the following:

- The water depths will be too much to economically build structures with solid foundations extending from water level to the ocean floor, forcing the construction of floating structures for turbines and grid-integration equipment [33].
- The distances to shore will make High Voltage Direct Current (HVDC) transmission [34-38] attractive, technically and economically [39]. Subsea-cable based AC transmission requires intermediate reactive power compensation and also suffers from stability issues. The stability problem limits the maximum transmission distance. In addition, for a given voltage-insulation level, HVDC technology can transmit more power than its AC counterpart.
- The increased distance will also mean exposure of the equipment to tougher weather conditions. The reliability of equipment will be of utmost importance as the climatic conditions might not permit servicing and repair for major part of a year.
- The reliability constraints and the cost of the floating platform demand the grid-integration equipment be optimally compact.

1.4 Electrical Layout of Wind Power Plants

The only layout employed currently is the generators connected in parallel to the grid. However, there have been numerous architectures put forward by the researchers [40-44].

1.5 HVDC Technologies

HVDC is considered to be the driver for renewable energy integration [45, 46]. There are two types of HVDC technologies in commercial use nowadays.

1.5.1 Line-Commutated Converter based HVDC (LCC HVDC)

This is the classic HVDC technology [38], in use for over five decades. In the beginning, it employed mercury-arc valves which were later replaced by thyristors as solid-state power electronics matured. The topology maintains a constant current on the DC side that is switched between the three phases on the AC side based on the state of the commutating line voltages; a fact that has given this topology its name. The major benefits of the topology are listed below:

- The voltage and power levels achieved by this topology are unmatched.
- The technology is very mature and highly-reliable devices ensure trouble-free operation.
- Losses are very low.

The main disadvantages are:

- The DC -link current is made constant by the use of large inductors. This flat-current profile appears in the AC line current, which has trapezoidal shape implying the presence of significant low-order harmonics. The propagation of these harmonics in the AC system distorts the terminal voltage at the HVDC-terminal AC bus and may also excite resonances leading to AC-system instability. This effect is more pronounced in weaker systems. The classical method for blocking the propagation of these harmonics into the AC system is through the use of passive filters which are bulky and wasteful.
- The commutation of current from one phase to the other lags the respective phase voltages by design. The incoming thyristor is fired after a specific delay after the crossover of the concerned commutating voltage known as the firing-delay angle, commonly denoted by α in literature. This leads to large reactive power consumption even with small values of α. To complicate matters further, the leakage reactance of the transformer connecting the AC grid to the AC/DC converter has to be high to reduce the rate-of-change-of-voltage burden on the thyristors and to reduce the harmonic content. This leakage inductance, therefore, consumes more reactive power. Conventional reactive power compensation is done by the passive filters mentioned above (as their behaviour is capacitive at fundamental frequency) and additional shunt capacitor banks. This leads to a larger footprint of LCC HVDC converter terminal.
- LCC HVDC does not have the capability of black start. The presence of commutating voltages is essential in the inverter mode of operation making this topology handicapped for interconnection of islanded systems without any generation. There are a few suggestions for black start [47, 48], however, the author is unaware of any commercial deployment of any of these.
- LCC HVDC uses Mineral Insulated (MI) cable which is more costly when compared to the cable used in the recently-developed alternative HVDC technology that will be discussed in the succeeding section. This is because of the requirement of reversal of polarity for situations such as power reversal and for DC-fault clearance.

- The control is generally complicated & slow, and requires communication between the rectifier and inverter terminals.
- The inverter terminal is especially susceptible to commutation failures [36]. As evident from the name, these are events when the outgoing phase does not commutate out of conduction at the end of its conduction period; which result in short-circuit of the DC link when the complimentary thyristor in the same phase leg commutates into conduction. Consequently the DC-link voltage and transmitted power is reduced to zero. The recovery time from these events is rather large.
- Multi-terminal operation is complicated.

There have been numerous suggestions to eliminate or alleviate some of the problems associated with LCC HVDC transmission [49], and this work is also an attempt to tackle a few of these.

1.5.2 Self-Commutated (Voltage-Sourced) Converter based HVDC (VSC HVDC)

A relatively recent development, VSC HVDC utilizes self-commutated converters [50] to maintain a constant voltage on its DC link [38, 51-55]. This voltage is then connected and disconnected several times in a single power cycle to synthesize an AC voltage which is connected to the AC grid through a coupling inductor. The phase and magnitude difference of the synthesized voltage to the grid voltage is controlled in the classical AC-generator-infinite-bus-interaction method [36] to achieve active- and reactive-power control. Advantages of the system are as under:

- This topology can control the reactive power independently of the active power hence large shunt capacitors are not required. The topology has the capability to generate or absorb reactive power on demand like a conventional AC generating station.
- The high switching frequency implies that low-order harmonics are eliminated. The switching-frequency harmonic components can be filtered out using very small passive filters. This together with the reactive-power-generation capability leads to a smaller physical footprint of the converter terminal.
- The control action is very fast compared to LCC HVDC.
- Multi-terminal operation is simple.

The disadvantages are listed below:

- The voltage and power ratings of VSC HVDC have not yet reached the levels available in LCC HVDC. For grid integration of large offshore wind power plants, more than one HVDC connections may be required driving the costs upwards.
- Multiple switching operations in a single cycle lead to higher power losses in the converter bridges leading to lower efficiencies [56], although these are coming down as the technology matures with other topologies coming in like the modular multilevel converter based HVDC (MMC HVDC) [57].

- There is a little-known problem of non-integral harmonics that can be generated by VSC HVDC based on Pulse-Width Modulation (PWM) [58]. These can cause low-frequency oscillations in the system.

1.6 Reactive and Harmonic Compensation Techniques for LCC HVDC – State of the Art

1.6.1 Shunt Passive Filters and Capacitor Banks

This is the classic compensation arrangement for LCC HVDC [35, 59]. Inductors and capacitors are connected at the primary side of the converter transformers to provide fundamental-frequency reactive and harmonic compensation. These form a significant portion of a converter terminal (50%-60% of the total area). Secondly, their reactive power output is a function of the voltage and not the load current. Therefore, capacitors have to be switched in and out of the circuit to meet the reactive-power requirement. This also implies that significantly larger capacitance would be required if the grid connection to the HVDC terminal is at a lower voltage.

The layout of a typical LCC HVDC terminal is shown in Fig. 1–5. A calculation of distribution of area covered by the thyristor valve hall, the various filters, and the shunt capacitors based on [59] is given in TABLE 1–1. As can be seen, the basis for the percentage calculation is the sum of the areas of the concerned equipment only. The important thing to note here is that the filters and capacitor banks take up more than 80%. A substantial reduction in the filtering and reactive-power requirements can bring about a drastic reduction in the size of the terminal.

1.6.2 Fixed Series Capacitors

This is a relatively recent development [60-63] commonly employed at the inverter terminal of an HVDC link. This type of LCC HVDC is commonly referred to as Capacitor Commutated Converter based HVDC (CCC HVDC). Fixed series capacitors are connected between the secondary windings of the converter transformers and the thyristor bridges. The series capacitors are not sized to supply the entire reactive-power demand of the system. Rather, these are used in conjunction with the conventional shunt filters. Their effect is the reduction in capacitance requirement in the shunt filters. Secondly, the reactive-power flow through the converter transformers is reduced, due to which, there is a saving in their size. Also, the reactive-power contribution by the series capacitors varies with variation in active-power flow. This reduces the number of switching operations in the shunt filters.

The disadvantage is the degradation in current harmonics making the requirement on the shunt filters tougher. Secondly, the variation in the reactive-power output is not sufficient to neutralize the reactive-power demand of the system, which would again require switching in the shunt filters. Finally, due to stored energy in the series capacitors, the stability of the system is influenced negatively.

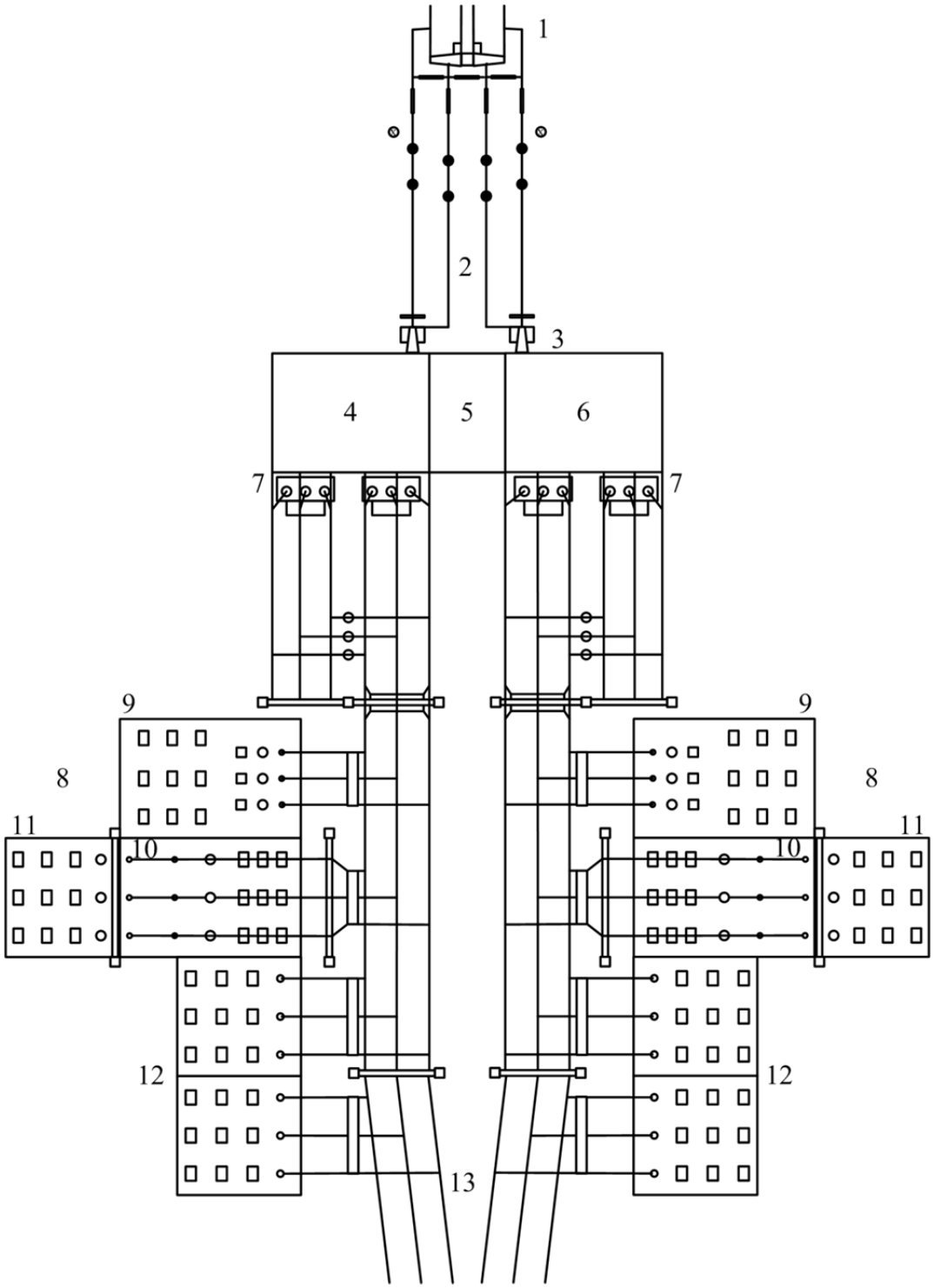

Fig. 1–5. Station layout of 1000 MW bipolar HVDC terminal. 1, DC and electrode lines: 2, DC switchyard; 3, DC smoothing reactors; 4, valve hall, pole 1; 5, service building with control room; 6, valve hall, pole 2; 7, converter transformers; 8, AC harmonic filters; 9, high-pass filter; 10, 11th harmonic filter; 11, 13th harmonic filter; 12, shunt capacitance; 13, AC switchyard [59].

TABLE 1–1
% Area Distribution in an LCC HVDC Terminal

Equipment	% Area
Thyristor valve hall	18
High-pass filter	20
11^{th} harmonic filter	21
13^{th} harmonic filter	13
Shunt capacitors	28
Total	100

1.7 Proposed Alternative Solutions

Over the years, numerous solutions based on power-electronic converters have been proposed in literature for several purposes in the AC-transmission domain. The technology is generally referred to as the Flexible AC Transmission System (FACTS) technology [64-67]. These can be broadly categorized into shunt-connected, series-connected, and hybrid compensators.

1.7.1 Shunt-Connected Active Compensators

This type of compensators were first introduced as Static VAR Compensators (SVC) [68] which generally comprised of line-commutated switches. These transformed into Static Synchronous Compensators (STATCOM) [69-73]. One of the instances where a combination of a STATCOM and LCC HVDC has been proposed in [74].

1.7.2 Series-Connected Active Compensators

Series compensation of transmission lines started with the use of fixed series capacitors [75, 76]. This concept expanded into several thyristor-controlled topologies, which would make the series device behave as a controlled capacitor/inductor [64, 77-83]. The Static Synchronous Series Compensator (SSSC) [77] is different from other topologies in the sense that it injects a voltage through an injection transformer, whereas the others are transformer-less topologies.

The benefit of the transformer-less topologies is their compactness due to the absence of the transformer. Secondly, these do not employ high-frequency switching leading to lower switching losses. A benefit of that is the elimination of switching-harmonic filters. These, therefore, are potential solutions of the reactive-power-compensation problem in LCC HVDC. However, very little has been reported in literature for this application like in [63].

1.7.3 Hybrid Compensators

There are suggestions for combined series and shunt compensators referred to as Unified Power Flow Controllers (UPFC) in the power systems and Unified Power Quality Conditioners (UPQC) in active power filtering [84]. However, these invariably use transformers for series and shunt injections leading to larger area requirements.

1.7.4 Reactive Power Control with Wind Turbine Converters

The proposals discussed above offer local solutions at the AC/DC conversion terminal. In addition to these, there are several proposals [30] for alternative wind-farm grid architectures, one of which is to integrate the offshore wind farm output using an LCC HVDC link [85], where the offshore rectifier terminal is based on diodes only. The proposed solution necessitates the use of wind turbines with permanent-magnet generators connected to the offshore grid through full-scale converters. The authors have employed distributed control of the wind-turbine converters to achieve control of active power and offshore-grid frequency. The reactive power and harmonic compensation of the rectifier terminal is carried out by the use of shunt passive filters and capacitors connected at the rectifier AC bus. The values of the capacitors and inductors are not reported in this paper. Neither have the voltage levels in the offshore grid been provided.

The same authors have presented the same case with reduced shunt filter and capacitor banks for reactive/harmonic compensation at the rectifier bus in [86]. The shunt passive filters have been removed completely and the shunt capacitors remain the same as in [85]. The claim is that the reactive power is supplied by the wind-turbine converters in addition to the provision of active-power and frequency control described in [85]. The wind farm is modelled with 5 aggregated wind turbines of different active-power ratings adding up to 1000 MW. In the author's view, the distributed control of reactive power had the following negative effects:

- Oscillations were introduced in the grid frequency with amplitude of 2 Hz.
- The wind-turbine converters required larger apparent-power ratings by a factor of almost 6.5%.
- An increase in voltage harmonics at the HVDC converter terminal was observed, for example, the amplitude of the 11^{th} harmonic with the original filter and capacitor bank was almost 0.005 pu at rated power, whereas it jumped to 0.025 with the reduced filter and capacitor bank. This is indicative of poor harmonic-current filtering by the proposed scheme.
- The total harmonic distortion of the voltage at the filter bus jumped to over 3.5% with reduced filters from approximately 0.75% in the benchmark case.
- The total harmonic distortion in the offshore-grid current increased from 0.3% to over 1.1%.
- The losses in the offshore grid increased by over 6%. This is to be noted that many impedances have been neglected for simplifying the simulation model in both the papers. These loss figures could go up further when a more detailed model is simulated.

Nonetheless, the availability of full-scale converters in the wind turbines equipped with permanent-magnet generators offers the possibility of active-power and offshore-grid-frequency control and permits the use of diode converters in the HVDC rectifier terminal. This would lead to slightly-reduced capacitor banks and shunt filters at the HVDC conversion terminal, as the additional reactive-power consumption due to firing-delay angle of the thyristors would be eliminated.

1.8 Scope of Work

The work carried out during the course of this research focused on LCC HVDC. The basis for preference over High Voltage AC (HVAC) transmission was the large transmission distance involved requiring expensive intermediate compensation. VSC HVDC was discounted due to the fact that multiple HVDC terminals and cables would be required to carry a huge amount of power that would potentially be available. Secondly there is a wealth of growing knowledge about VSC HVDC technologies because there is a lot of research and development being done in this area.

The major obstacles in using LCC HVDC for this purpose are mentioned in section 1.5.1. The offshore HVDC terminal will act as a rectifier so the problem of commutation failures is not significant. Large direct-driven wind turbines with permanent-magnet generators seem likely to be the preferred choice in the near future [87, 88]. These machines do not require external power supply for start-up; therefore, the issue of black start will likely become insignificant.

The focus of this work was thus to reduce the physical footprint of the offshore rectifier terminal by suggesting ways to compensate for the fundamental-frequency reactive power and lower-order harmonics with a minimum amount of equipment. As a lot of work has been (and is still being) done in shunt compensation for such systems [64, 69], this work has suggested ways to solve the problem with series-connected compensators.

1.9 Main Contributions

The major contributions of this work are listed below:

1. The performance of the series capacitor commutated converter based HVDC (CCC HVDC) has been compared with the conventional shunt-compensated LCC HVDC.
2. The gate-commutated series capacitor (GCSC) has been employed for controlled series compensation of LCC HVDC terminal; something that has not been attempted with GCSC before. It has been shown that the GCSC can use very small capacitors as compared to CCC HVDC and follow the reactive-power reference at all loads. However, the deterioration in the harmonic behaviour hinted towards the weakness of this solution.
3. A transformer-less series-connected compensator, named the Series Pulsed Voltage Compensator (SPVC), has been proposed and developed gradually. It

employs very small capacitors (60 μF DC capacitance with a maximum voltage of 150 kV) as compared to the total capacitance (273 μF AC capacitance to be rated for 345 kV AC line-to-line) employed in the conventional shunt-connected passive filter and capacitor banks or the CCC-HVDC arrangement [89-94].

4. Ultimately, two control strategies for the same physical-compensator setup have been developed and simulated. The first of these two strategies involves instrumentation of SPVC variables [93], and the second does not need any measurements of the compensator variables to achieve the desired control objectives [94].
5. One of the control strategies has been experimentally verified [94].
6. It has been shown that the proposed compensator can follow a reactive-power reference with changing active power, and also alleviates the harmonic problem instead of deteriorating it, as observed with the CCC and GCSC.
7. The Conservative Power Theory (CPT) has been employed for reactive and harmonic compensation of LCC HVDC [95].
8. In addition, a few suggestions have also been made to improve the control of the conventional LCC HVDC setup by modifying the control loops at the rectifier and inverter terminals [96, 97].

1.10 List of Publications

The research work carried out has resulted into numerous publications in renowned peer-reviewed conferences and journals. A journal paper is under review at the time of this writing.

1.10.1 Journal Papers

- M. Jafar and M. Molinas, "A Transformer-less Series Reactive/Harmonic Compensator for Line-Commutated HVDC for Grid Integration of Offshore Wind Power," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 6, pp. 2410-2419, 2013. Reference [93]
- M. Jafar and M. Molinas, "Transformer-less series reactive/harmonic compensation of line-commutated HVDC for offshore wind power integration" *submitted to IEEE Transactions on Power Delivery*. Reference [94]

1.10.2 Peer-Reviewed Conference Papers

- M. Jafar and M. Molinas, "Effects and Mitigation of Commutation Failures in Line-Commutated HVDC Transmission System," in *IEEE International Symposium on Industrial Electronics ISIE2009*, Seoul, South Korea, 2009, pp. 81-85. Reference [96]
- M. Jafar and M. Molinas, "Ride-Through Enhancement of Line-Commutated HVDC Link for Large Offshore Wind Parks," *in 35th Annual Conference of*

the IEEE Industrial Electronics Society, Porto, Portugal, 2009, pp. 779-784. Reference [97]

- M. Jafar and M. Molinas, "Improvement in reactive power consumption of line commutated HVDC converters for integration of offshore wind-power," in *8th international workshop on large-scale integration of wind power into power systems as well as on transmission networks for offshore wind power plants*, 14 -15 October, 2009, Bremen, Germany, 2009, pp. 619-623. Reference [89]
- M. Jafar and M. Molinas, "Forced commutation through series voltage injection for reactive power reduction of line commutated HVDC converter terminal," *in 2010 International Power Electronics Conference (IPEC)*, Sapporo, Japan, 2010, pp. 1788-1793. Reference [90]
- M. Jafar and M. Molinas, "A Series Injection Strategy for Reactive Power Compensation of Line Commutated HVDC for Offshore Wind Power," in *IEEE international symposium on industrial electronics, ISIE2010*, Bari, Italy, 4-7 July, 2010, pp. 2339-2344. Reference [91]
- M. Jafar, M. Molinas, and P. Tenti, "Application of conservative power theory for active power filtering of line-commutated HVDC for offshore wind power," in *2011 IEEE PowerTech,* Trondheim, 2011, pp. 1-8. Reference [95]
- M. Jafar and M. Molinas, "Transformer-less Series Voltage Injection for Reactive Power Compensation of Line-Commutated HVDC," in *15th International Power Electronics and Motion Control Conference and Exposition EPE-PEMC 2012, ECCE Europe*, Novi Sad, Serbia, 2012, pp. 15-1-15-5. Reference [92]

1.11 Layout of the Thesis

The behaviour of the conventional shunt-compensated LCC HVDC system is presented in chapter 2 with the help of detailed simulations. Next, the CCC HVDC system is described in detail in chapter 3. Chapter 4 introduces the gate-commutated series capacitor (GCSC) as an alternative for series compensation of LCC HVDC. The next chapter describes the operating principle, control, and simulation results for the main contribution of this research work, i.e. the SPVC. An alternative control of the SPVC is developed, simulated, and experimentally verified in chapter 6.

The details of a shunt active-power filter (SAPF), based on CPT for active-power filtering of the HVDC link with the SPVC are given in appendix A. At the end, the proposals for improving the control of the conventional LCC HVDC system are presented briefly in Appendix B.

2 The Conventional LCC HVDC Behaviour

The behaviour of the conventional shunt-compensated line-commutated HVDC system is discussed in this chapter. The reactive power and the harmonic behaviour were the variables in focus. Benchmarks have been identified for other compensation topologies.

The behaviour of the conventional LCC HVDC will be discussed in this chapter. The reader is referred to [34, 35, 59] for theoretical details. The reactive and harmonic behaviour will be discussed in order to keep the discussion brief. CIGRÉ (Conseil international des grands réseaux électriques, English: International council on large electric systems) benchmark for HVDC studies [98] provides a good foundation for this work. The proposed and other series compensators will also be implemented to the same in the later chapters, in order to provide a fair comparison between all of them. The simulation platform used in this and later chapters is MATLAB®/Simulink® using the components from different libraries including the SimPowerSystems® library.

2.1 Simulation Setup

2.1.1 Schematic Arrangement

The schematic arrangement of the rectifier terminal of a single-pole 12-pulse LCC HVDC is depicted in Fig. 2–1. Z_g is the source impedance and Z_f is the impedance of the shunt passive filter and capacitor bank as employed in a conventional system. The circuit arrangements of the 6-pulse thyristor bridge, Z_g, and Z_f are depicted in Fig. 2–2, Fig. 2–3, and Fig. 2–4 respectively.

The parameter values with reference to Fig. 2–1, Fig. 2–2, Fig. 2–3, and Fig. 2–4, are taken from [98] and are listed in TABLE 2–1. The parameters values for Z_g and Z_f are given on a per-phase basis. It should be noted that the total capacitance in the shunt passive filter and capacitor bank is 90.99 μF. This implies a total of 273 μF in three phases. It should be noted that this value depends upon the grid-side voltage which in this case is 345 kV line-to-line. In case of a lower voltage on the grid side, the required capacitance would be larger to fulfil the requirement of reactive power according to:

$$Q = \omega C V_{rms}^2 \tag{2.1}$$

where, Q is the three-phase reactive power, ω is the angular frequency in radians/s, C is the capacitance per phase, and V is the line-to-line voltage at the point of connection of the capacitors. It can be seen that to supply the same amount of reactive power at a lower voltage, the capacitance has to be increased.

The two converter transformers are each 3-phase, 50 Hz, 603.73 MVA, 345/213.4557 kV. One of these transformers is wye-wye (*YY*) connected whereas the other is connected in wye-delta (*YD*), with the *D*-connected winding connected to the thyristor converter. The leakage inductance of both the transformers is 0.18 pu with the transformer ratings used to calculate the base impedance. The converter-side line voltages on the *YD* transformer lag the primary voltages by 30°.

2.1.2 Control Loops

The rectifier terminal is responsible for controlling power flow in LCC HVDC whereas the inverter terminal establishes the voltage on the DC link. This leads to the simplified control loop for control of power flow in Fig. 2–5. The mean value of the DC -link current (I_d) is compared with the reference (I_{dR}) and fed to a proportional-integral controller (*PI*). The output of the *PI* controller is the firing delay angle (α) which is limited by a saturation component.

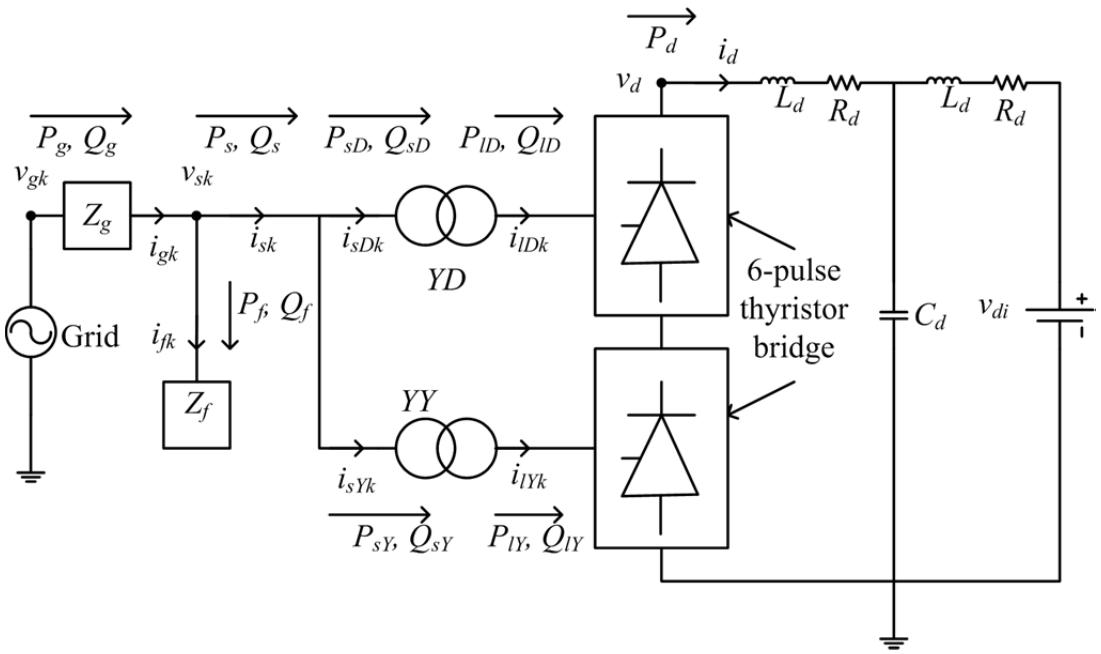

Fig. 2–1. Schematic diagram of the 12-pulse arrangement used in the simulation setup.

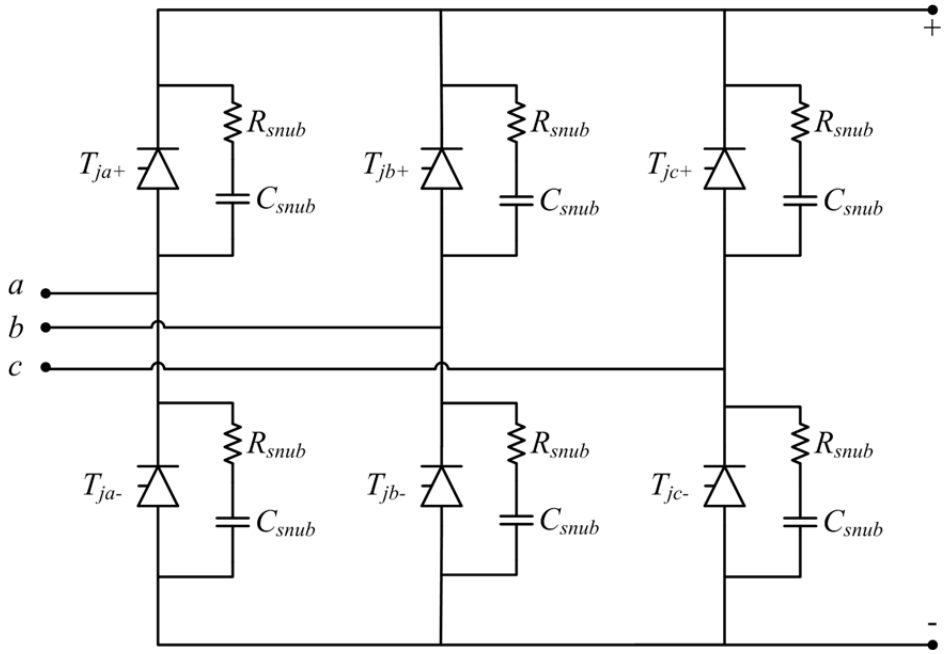

Fig. 2–2. Schematic arrangement of the 6-pulse thyristor bridge in Fig. 2–1.

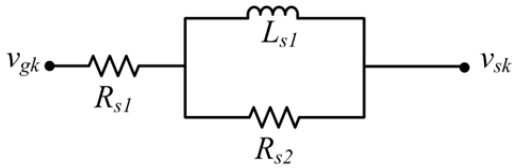

Fig. 2–3. Composition of Z_g in Fig. 2–1.

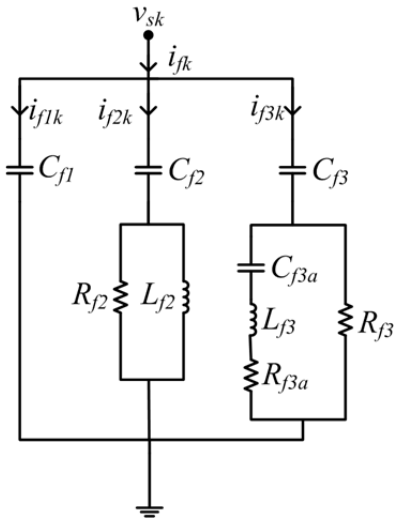

Fig. 2–4. Composition of Z_f in Fig. 2–1.

TABLE 2–1
Parameter Values for Simulation Setup

Parameter	Symbol	Value	Unit
DC reactor inductance	L_d	0.5968	H
DC line resistance	R_d	2.5	Ω
DC line capacitance	C_d	26	μF
Grid impedance	Z_g		Ω
	R_{s1}	3.737	Ω
	R_{s2}	2160.633	Ω
	L_{s1}	0.151	H
Shunt filter impedance	Z_f		Ω
	C_{f1}	3.342	μF
	C_{f2}	6.685	μF
	R_{f2}	83.32	Ω
	L_{f2}	0.0136	H
	C_{f3}	6.685	μF
	R_{f3}	261.87	Ω
	C_{f3a}	74.28	μF
	R_{f3a}	29.76	Ω
	L_{f3}	0.1364	H

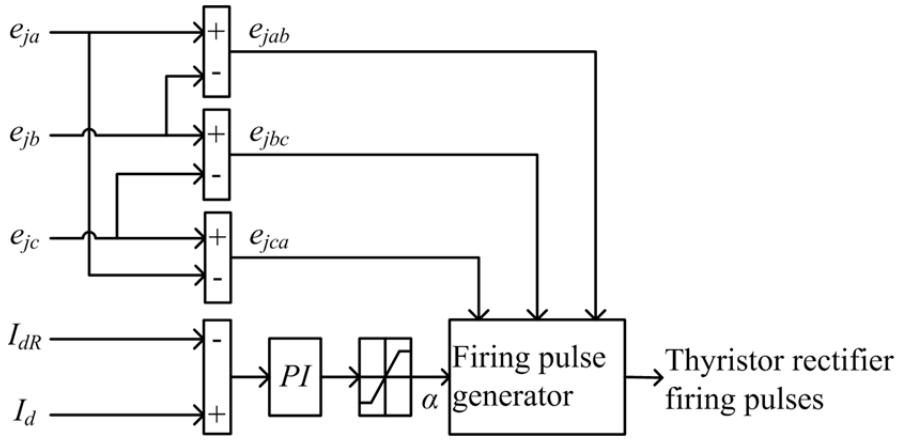

Fig. 2–5. Active power control loop for rectifier terminal of LCC HVDC.

The reference voltages for the firing-pulse generator (e_{ja}, e_{jb}, and e_{jc}) are the voltages behind the leakage reactances on the secondary side of the converter transformers. The subscript "*j*" denotes the concerned converter transformer and can either be "*D*" (for *D* secondary) or "*Y*" (for *Y* secondary). During commutation in LCC HVDC, the AC current in the incoming phase is 0 and that in the outgoing phase is essentially constant equal in magnitude to the DC -link current. Therefore, there is no reactive drop in either of the phases that are about to commutate and, consequently, these voltages appear across the converter terminals and are referred to as commutating voltages.

It can be observed from Fig. 2–5 that a decrease in the reference power and thereby reference current (I_{dR}) would increase the value of α. An increased value of α produces a larger phase displacement between respective phase voltages and currents meaning increased reactive-power consumption. To avoid this excessive reactive-power consumption, converter transformers are equipped with On-Load Tap Changers (OLTC), which decrease or increase the AC voltage to keep α at a constant steady-state value (normally 15°).

The transformer with OLTC for time-domain analysis is not available in the simulation software used. To emulate the function of OLTC, another control loop has been designed and is depicted in Fig. 2–6.

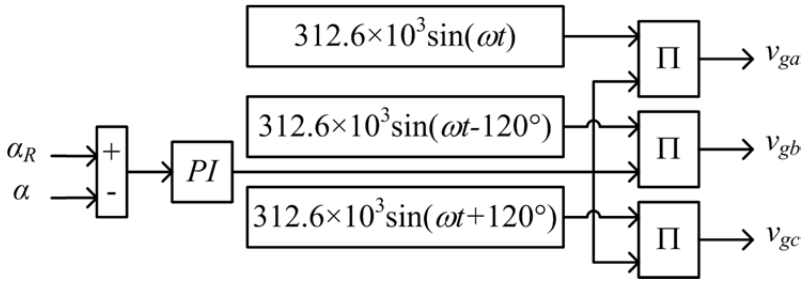

Fig. 2–6. AC voltage control loop to keep α at a reference value given by α_R.

2.2 The Commutation Process

The basic commutation circuit for commutation of positive current from phase *c* to *a* is shown in Fig. 2–7. The equation of the loop taking the zero crossing of the commutating voltage as the reference would be:

$$e_{jac} = -e_{jca} = \sqrt{2}E_{lj}\sin(\omega t) = 2L_{tr}\frac{di_{comm}}{dt} \tag{2.2}$$

Where, E_{lj} is the rms value of the commutating voltage, ω is the electrical frequency in radians per second, L_{tr} is the leakage reactance per phase of the converter transformer, and i_{comm} is the commutating current in the commutation loop.

It has to be noted that the rate of change of current is directly proportional to e_{ja} and inversely proportional to L_{tr}. This means that the overlap angle u is influenced by these two parameters.

Rearranging (2.2), we get:

$$\frac{E_{lj}}{\sqrt{2}\omega L_{tr}}\int_{\alpha}^{\omega t}\sin(\omega t)d\omega t = \int_{0}^{i_{comm}} di_{comm} \tag{2.3}$$

where, α is the firing delay angle. Solving (2.3) for i_{comm}:

$$i_{comm} = \frac{E_{lj}}{\sqrt{2}\omega L_{tr}}[\cos(\alpha) - \cos(\omega t)] \tag{2.4}$$

This equation holds true during commutation. The commutation takes a certain time during which both the incoming and outgoing phases conduct current. After the completion of commutation, i_{comm} becomes equal to I_d. Putting this condition into (2.4), we get:

$$I_d = \frac{E_j}{\sqrt{2}\omega L_{tr}}[\cos(\alpha) - \cos(\alpha + u)] \tag{2.5}$$

where, u is the overlap angle or commutation angle. Solving (2.5) for u:

$$u = \cos^{-1}\left[\cos(\alpha) - \frac{I_d\sqrt{2}\omega L_{tr}}{E_j}\right] - \alpha \tag{2.6}$$

The overlap angle depends in a complex manner on the commutation reactance, the direct current and the commutating voltage. In general, it is higher for higher DC-side current and higher commutation inductance. It is, however, inversely proportional to the commutating voltage.

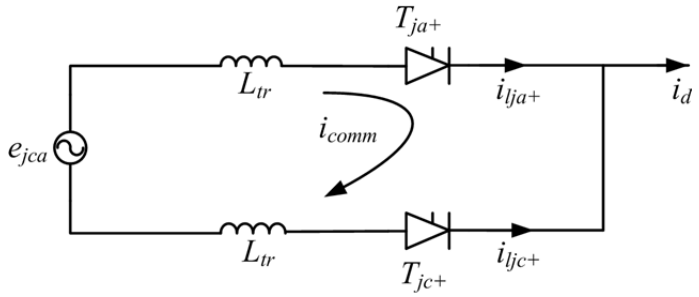

Fig. 2–7. Commutation circuit for transfer of current from phase *c* to *a* in the upper bridge arms.

The DC-link voltage is linked to the AC side voltage through the equation:

$$V_{dj} = (\frac{3}{\sqrt{2}\pi})E_{lj}[\cos(\alpha) + \cos(\alpha + u)] \tag{2.7}$$

where, V_{dj} is the mean DC voltage from the bridge in j branch. The use of (2.5) in (2.7) provides a more convenient relationship that does not involve u (not measurable directly).

$$V_{dj} = (\frac{3}{\sqrt{2}\pi})E_{lj}\cos(\alpha) - \frac{3\omega L_{tr}}{\pi} I_d \tag{2.8}$$

This means that higher commutation reactance and DC-side current affect the mean DC-link voltage negatively. This is obviously due to reduced voltage during prolonged commutation.

The relationship between fundamental frequency AC- and DC-side currents is given by:

$$I_{1lj} = I_d\sqrt{6}/\pi \tag{2.9}$$

where, I_{1lj} is the fundamental component of the AC current.

The expression for instantaneous current in terms of the DC-link current is given by:

$$i_{lj} = \frac{I_d[\cos(\alpha) - \cos(\omega t)]}{\cos(\alpha) - \cos(\alpha + u)} \text{ for } \alpha < \omega t < \alpha + u \tag{2.10}$$

When the valve is commutating out, the current becomes:

$$i_{lj} = I_d - \frac{I_d[\cos(\alpha) - \cos(\omega t)]}{\cos(\alpha) - \cos(\alpha + u)} \text{ for } \alpha + \frac{2\pi}{3} < \omega t < \alpha + \frac{2\pi}{3} + u \tag{2.11}$$

For periods not involving commutation, the AC- and DC-side currents are equal:

$$i_{lj} = I_d \text{ for } \alpha + u < \omega t < \alpha + \frac{2\pi}{3} \tag{2.12}$$

Similar equations can be written for the negative half-cycle of the current and combining all of these, we get the fundamental component of the AC current as:

$$I_{lj} = \frac{\sqrt{6}}{\pi} I_d \frac{\sqrt{\{[\cos(2\alpha) - \cos 2(\alpha + u)]^2 + [2u + \sin(2\alpha) - \sin 2(\alpha + u)]^2\}}}{4[\cos(\alpha) - \cos(\alpha + u)]} \tag{2.13}$$

The Fourier representation of i_{sY} neglecting commutation overlap is:

$$i_{sY} = \frac{2\sqrt{3}}{\pi}[\cos(\omega t) - \frac{1}{5}\cos(5\omega t) + \frac{1}{7}\cos(7\omega t) - \frac{1}{11}\cos(11\omega t) + ...] \tag{2.14}$$

It is evident that harmonics of the order $6n\pm1$ (where n is a positive integer) are present in a 6-pulse bridge converter. Similarly for the D branch, i_{sD} can be expanded into a Fourier series as:

$$i_{sD} = \frac{2\sqrt{3}}{\pi}[\cos(\omega t) + \frac{1}{5}\cos(5\omega t) - \frac{1}{7}\cos(7\omega t) - \frac{1}{11}\cos(11\omega t) + ...] \tag{2.15}$$

The two series in (2.14) and (2.15) are identical with the exception of the second and the third term inside the square brackets. These cancel out and we obtain a higher pulse number where harmonics are of the order of $12n\pm1$. This shifts the lowest harmonic in the AC current from the 5th to the 11th thereby reducing the size of the filtering components.

It has to be emphasized that the harmonic contents provided above are calculated without the consideration of the overlap angle. A harmonic reduction factor for calculation of specific harmonic magnitudes is given below:

$$\frac{i_h}{i_{h0}} = \frac{\sqrt{H^2 + K^2 - 2HK\cos(2\alpha + u)}}{\cos(\alpha) - \cos(\alpha + u)} \tag{2.16}$$

where, i_h is the harmonic current, i_{h0} is the harmonic current with no overlap, h is the harmonic order, $H = [\sin(h+1)u/2]/(h+1)$, and $K = [\sin(h-1)u/2]/(h-1)$

In conventional shunt-compensated HVDC systems the normal operating values of α and u are 15° and 20° respectively. The magnitude of the 11th and the 13th harmonics are therefore between 30% and 40% of the predicted values without consideration of the commutation overlap.

Under ideal conditions, the active power into each thyristor bridge from the AC side is equal to the DC-side power; and is given by:

$$P_{lj} = \sqrt{3} E_{lj} I_{1lj} \cos\varphi = V_{dj} I_d \tag{2.17}$$

where, P_{lj} is the active power in the branch j, φ is the power factor angle. Rearranging (2.17), we get:

$$\cos\varphi = \frac{V_{dj} I_d}{\sqrt{3} E_{lj} I_{lj}} \tag{2.18}$$

Putting (2.7) and (2.9) into (2.18):

$$\cos(\varphi) = \frac{1}{2}[\cos(\alpha) + \cos(\alpha + u)] \tag{2.19}$$

For a negligible overlap angle, the power factor angle and the firing delay angle are the same. This is however not achieved in practice and the higher the overlap angle, the lower would be the power factor angle.

The reactive power is given by:

$$Q_{lj} = \sqrt{3} E_{lj} I_{lj} \sin\varphi \tag{2.20}$$

In addition, the reactive power consumed by the converter transformer is:

$$Q_{trj} = 3 I_{lj}^2 \omega L_{tr} \tag{2.21}$$

The total reactive power consumption seen by the primary side of each converter transformer is:

$$Q_{sj} = Q_{lj} + Q_{trj} \tag{2.22}$$

Finally, the reactive power seen by the filter bus (that has to be neutralized by the shunt compensator) is:

$$Q_s = Q_{sD} + Q_{sY} \tag{2.23}$$

The dependence of the reactive power on the load current is evident from (2.20) to (2.23). This is why shunt capacitors in the filter banks have to be switched in and out of the circuit according to the reactive-power demand.

2.3 Simulation Results

Results of simulation where the active-power reference changes from 1 pu to 0.5 pu will be discussed in this section. Time- and frequency-domain behaviour of different system variables will be discussed with the help of various plots.

2.3.1 Active and Reactive Powers

The active/reactive-power picture is presented in Fig. 2–8. The simulations start with P_{sR} (reference active power) at 1 pu, which is stepped down to 0.5 pu at 3 s. Fig. 2–8 (a) depicts the transition of P_s at 3 s. As can be seen, Q_s drops down as well. This reduction is attributable to reduction in Q_{sD} and Q_{sY} (Q_s is the sum of Q_{sD} and Q_{sY}) as depicted in Fig. 2–8 (b) and (c) respectively. The reactive powers consumed by thyristor bridges due to the firing-delay angle are Q_{lD} and Q_{lY} and are depicted in Fig. 2–8 (b) and (c) respectively. The difference between the primary and the secondary reactive powers is the reactive-power consumption in the leakage reactance of the converter transformers. This also drops down due to a decrease in current flowing through the transformers.

Finally, Q_f and Q_g are plotted in Fig. 2–8 (d). With 1-pu active power, Q_g is just under 0 whereas Q_f is a little more than Q_s in magnitude. That means that the filter and capacitor arrangement is supplying the entire reactive-power demand of the converter terminal and an excess amount is also being exported to the AC grid for voltage support.

After the transition at 3 s, Q_f drops slightly because of the change in grid voltage under the influence of the algorithm presented in Fig. 2–6. However change in Q_s is much more than the change in Q_f. The excess reactive power is, therefore, exported to the AC grid and a significant change in Q_g can be observed in Fig. 2–8 (d). This abrupt change is not suitable for the AC-grid operation and this is the reason for switched capacitors in shunt compensation to adjust to the demand of the load. Of course, these switching arrangements add to the size, cost, and complexity of the system.

2.3.2 Control-Loop Operation

The satisfactory operation and effects of the control loops depicted in Fig. 2–5 and Fig. 2–6 are presented in Fig. 2–9 (a) and (b) respectively. Before the transition at 3 s, the values of α and V_{sa} are steady at their respective values. As soon as the active-power reference goes down, the algorithm in Fig. 2–5 increases the value of α. The algorithm in Fig. 2–6 detects this deviation from reference and accordingly adjusts the instantaneous voltage. The effect is a reduction in AC voltage and α returns to its reference value.

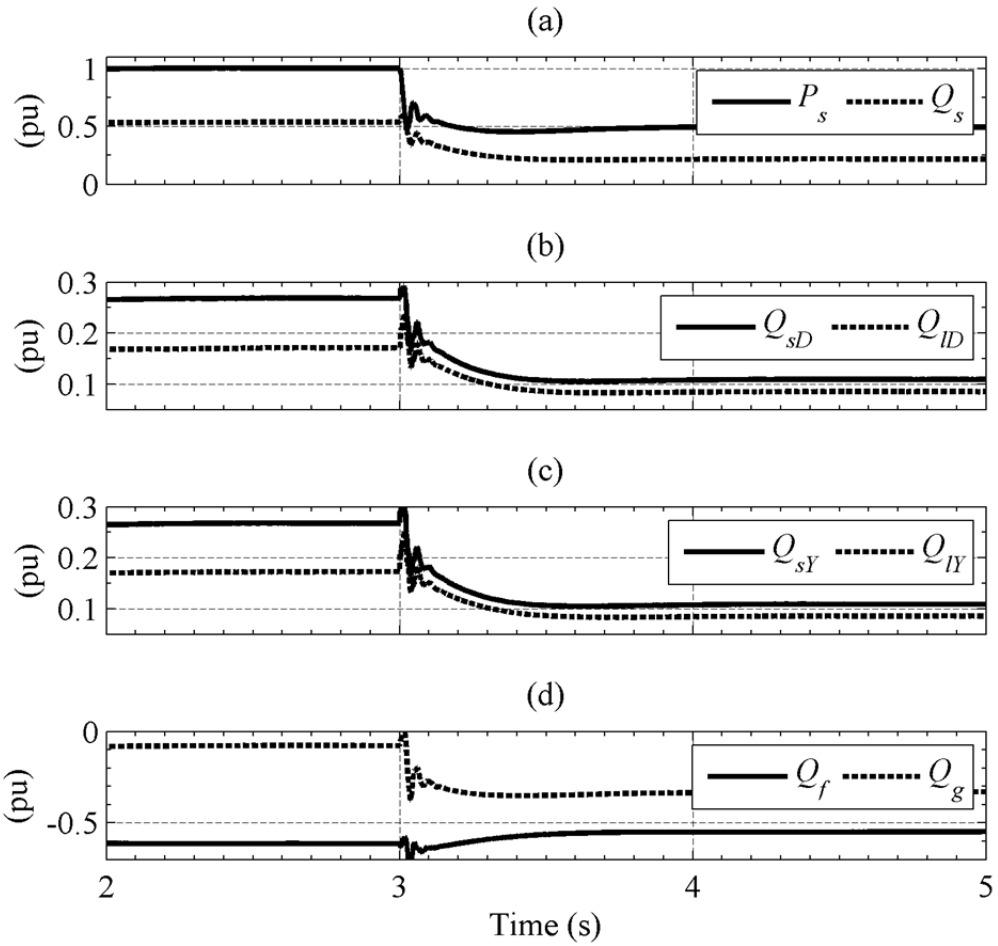

Fig. 2–8. Active and reactive powers in pu on a base value of 1000 MVA (a) total into the converter transformers, (b) in the *D* branch, (c) in the *Y* branch, and (d) at the filter bus.

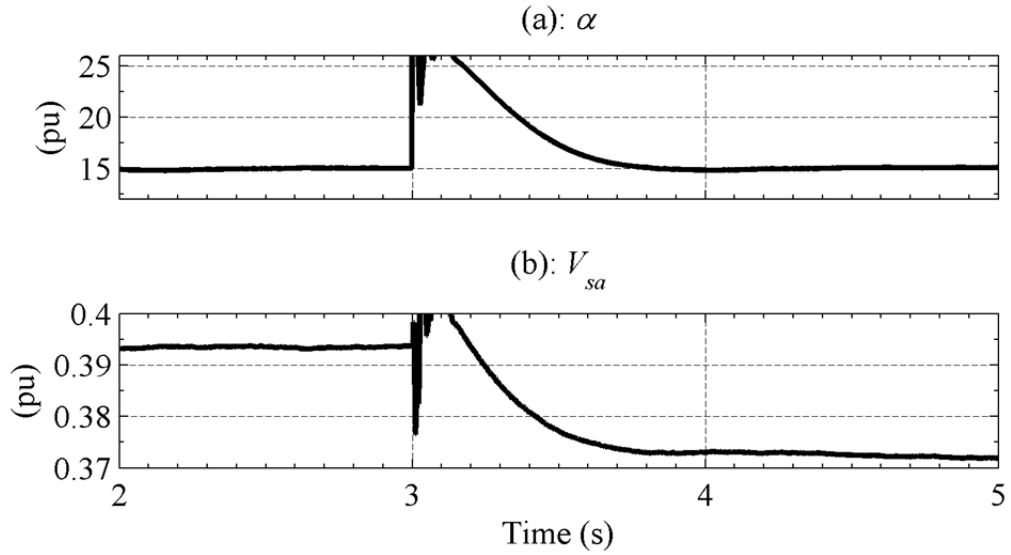

Fig. 2–9. Plots of (a) α and (b) rms value of phase a voltage on filter bus on a base of 500 kV.

2.3.3 Instantaneous Currents and Voltages

The instantaneous converter-side currents for both the D and Y bridges are presented in Fig. 2–10 (a) and (b) respectively. The appropriate thyristor in the incoming phase is triggered after a delay equal to α and the current commutates. This has to be noted that e_{Dca} going negative means that phase a has become positive with respect to phase c, therefore, positive current should start to flow in phase a at this instant. It is also worth observing that the commutating voltage on the Y secondary leads that on the D secondary by 30° and hence the currents also have a phase difference of 30°.

The same currents at 0.5-pu active power have been plotted in Fig. 2–11. It can be seen here that the currents commutate quickly as compared to the full-power case. The reason is the reduced amount of energy stored in the leakage reactance in the outgoing phase during commutation.

The primary-side currents into the YD transformer, YY transformer, their sum, into the shunt filter, and the grid current are depicted in Fig. 2–12 (a), (b), (c), (d), and (e) respectively. v_{sa} has also been plotted to get a view of the phase displacement between phase currents and voltage. The primary-side current into the YD transformer exhibits a different wave-shape from that into the YY transformer. This is because of the transformer connection. The harmonic content of both these currents is similar; however, there is a relative phase displacement in the individual harmonics. The sum of these two current contains lesser harmonics as the 5^{th} and 7^{th} in i_{sDa} and i_{sYa} cancel out making the 11^{th} and 13^{th} as the lowest harmonics in i_{sa}. Fig. 2–12 (d) depicts the current flowing into the shunt passive filter. As can be seen, it is composed of a fundamental and a harmonic part. The fundamental component is for fundamental-frequency reactive-power compensation and the harmonic part is for compensation of harmonics in i_{sa}. The dominant harmonics here are the 11^{th} and the 13^{th} as demanded by the wave-

shape of i_{sa}. As a consequence of shunt-filter action, the grid current is a fundamental wave almost in phase with the supply voltage as depicted in Fig. 2–12 (e).

The pattern of AC currents in the primary side of the system is depicted in Fig. 2–13 for 0.5-pu power reference. The general pattern is the same but the distortion in i_{sa} and i_{fa} (Fig. 2–13 (c) and (d)) is more pronounced as compared to the full-load case.

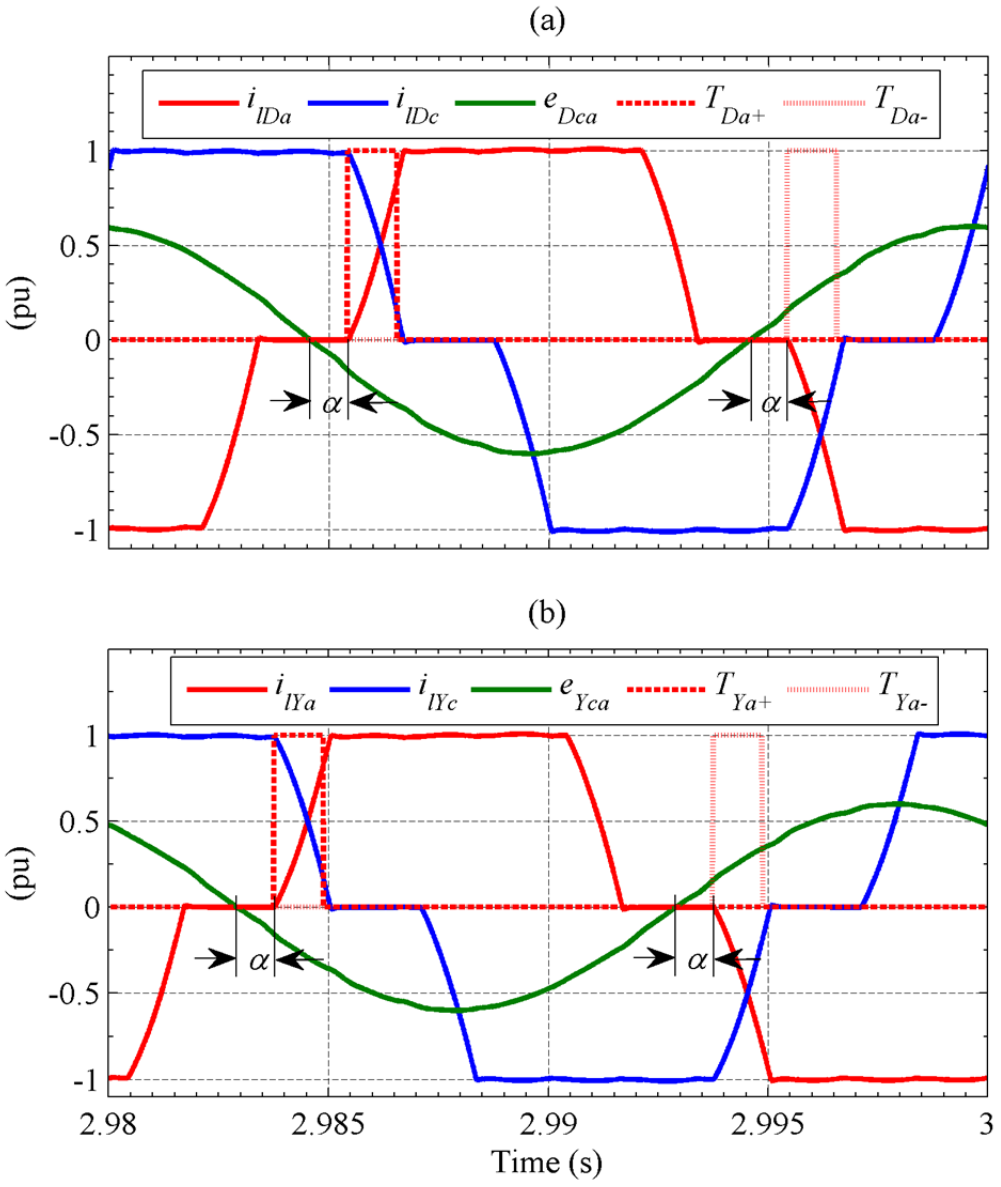

Fig. 2–10. Commutation of current from phase *c* to *a* in the thyristor bridge connected to (a) *D* secondary, and (b) *Y* secondary. Current base is 2 kA and voltage base is 500 kV.

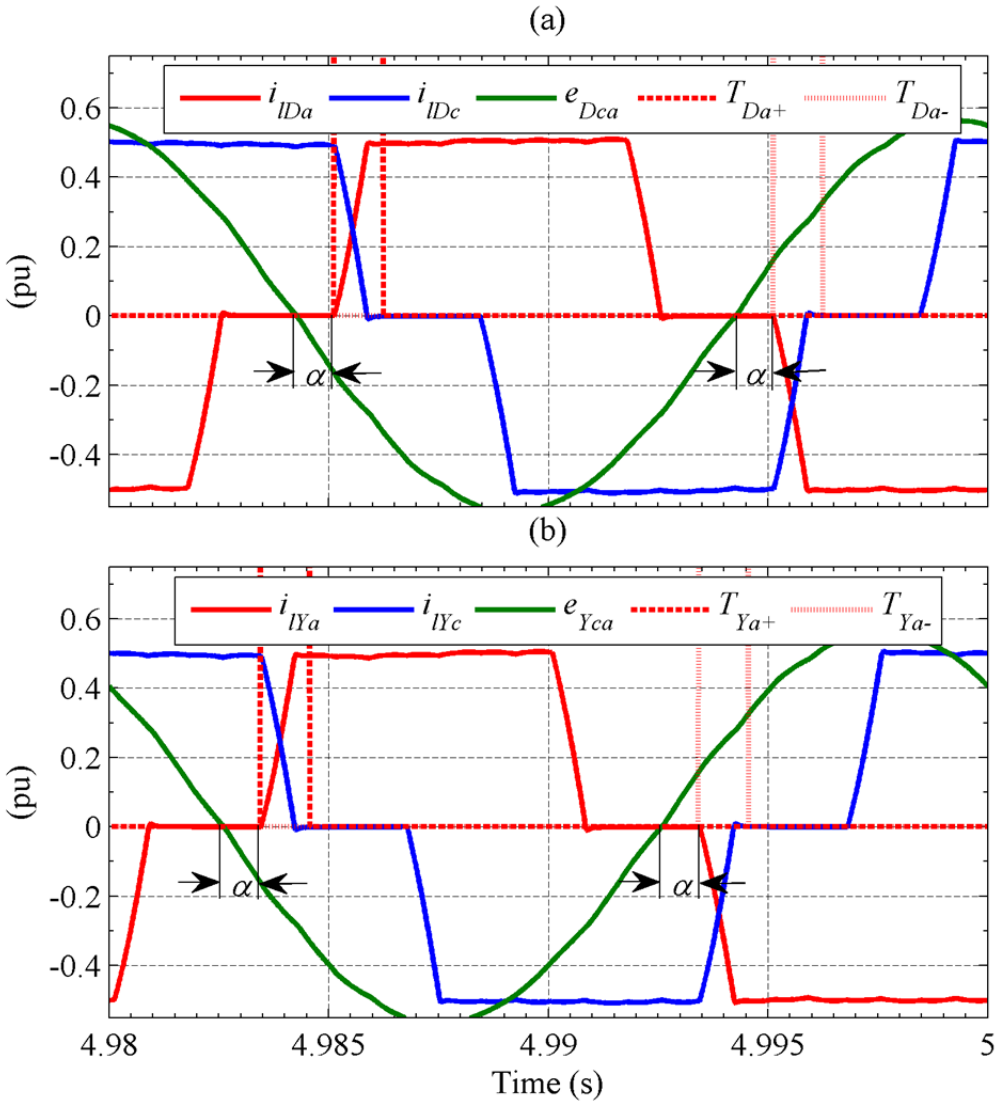

Fig. 2–11. Commutation of current at 0.5 pu active power from phase *c* to *a* in the thyristor bridge connected to (a) *D* secondary, and (b) *Y* secondary. Current base is 2 kA and voltage base is 500 kV.

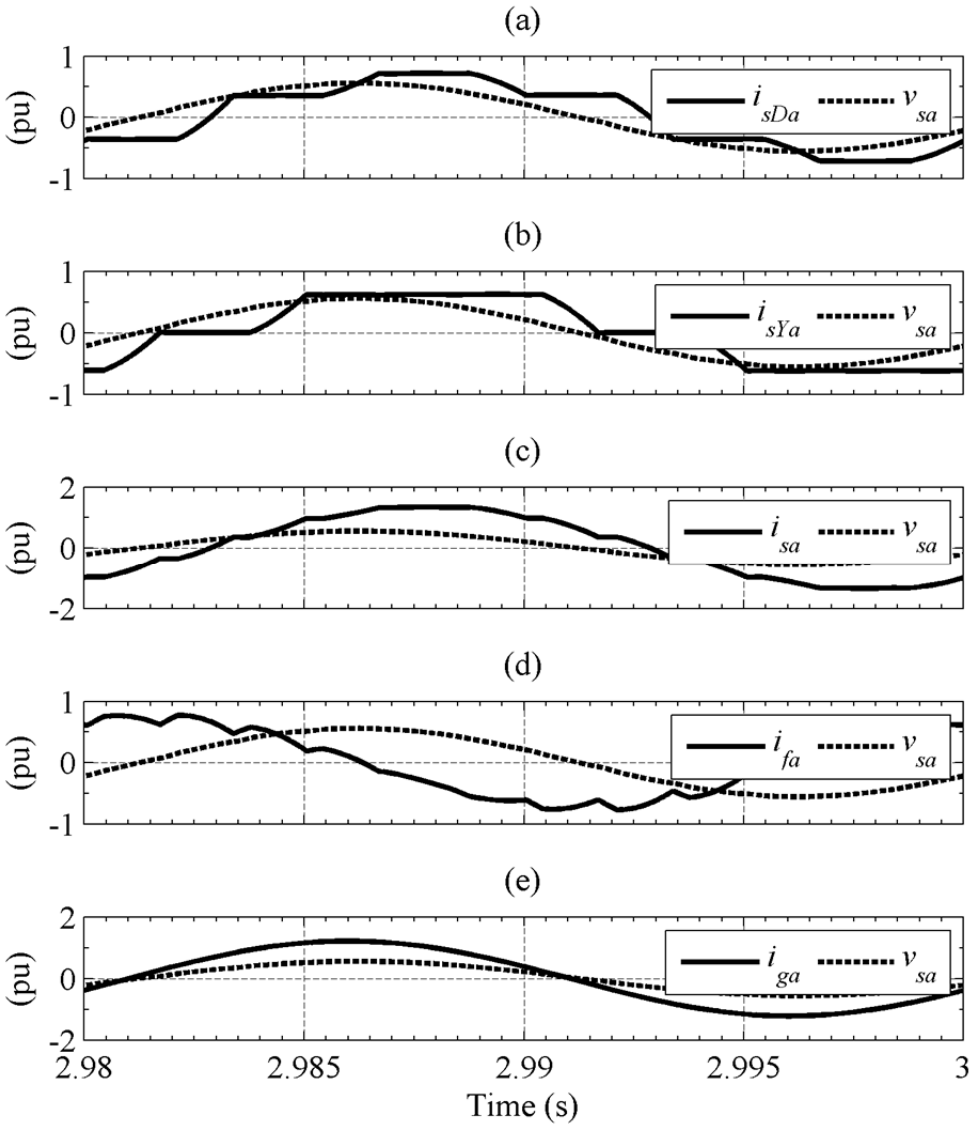

Fig. 2–12. phase *a* current at 1-pu load (a) into *YD* transformer primary, (b) into *YY* transformer primary, (c) the sum of converter transformer currents, (d) into the filter, and (e) being supplied by the grid.

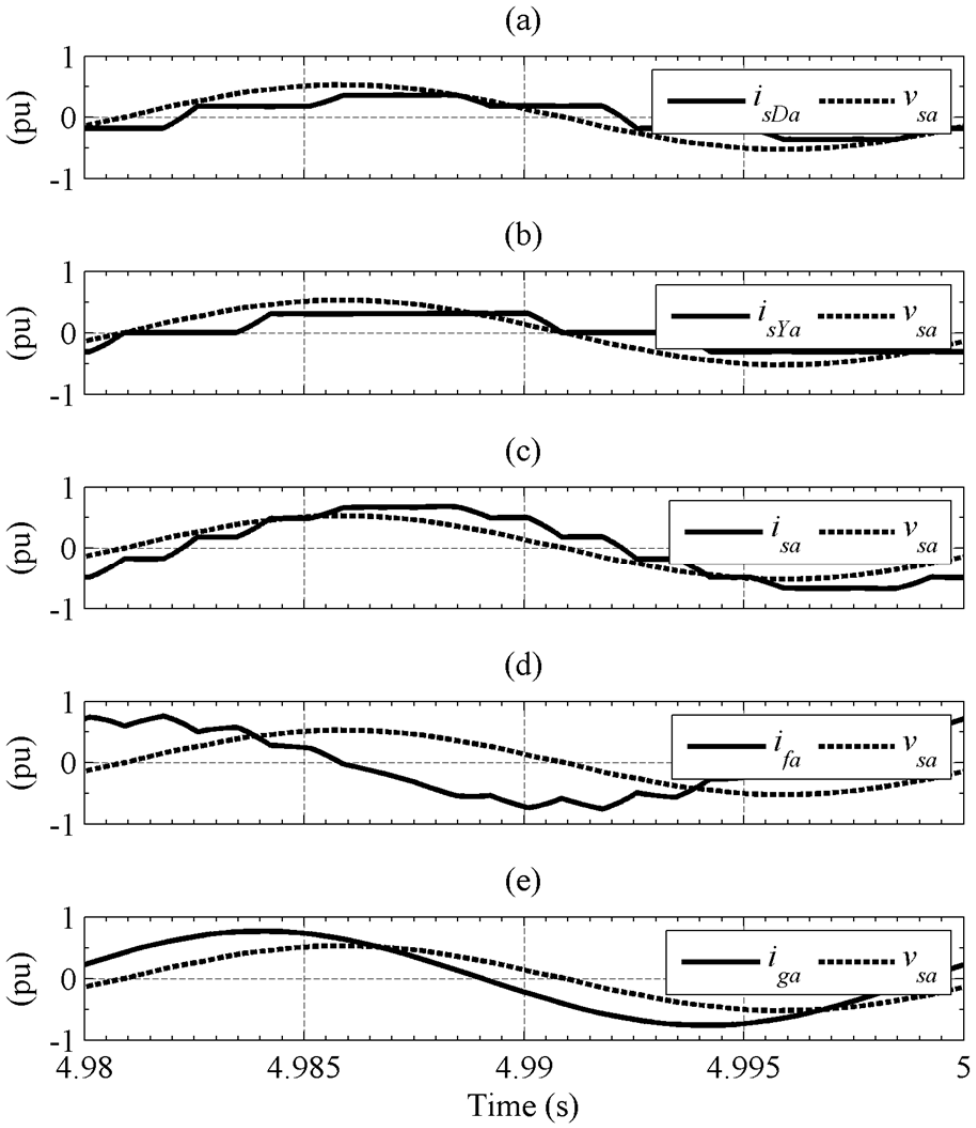

Fig. 2–13. phase *a* current at 0.5-pu active power (a) into *YD* transformer primary, (b) into *YY* transformer primary, (c) the sum of converter transformer currents, (d) into the filter, and (e) being supplied by the grid.

The instantaneous voltages appearing across one thyristor in one cycle in each converter bridge are plotted in Fig. 2–14. The plotted values will act as reference for other compensation techniques to be discussed later. The voltage is predominantly negative with a small positive portion depending upon the value of α. The phase difference in the blocking voltage is due to the displacement in the firing instants of the two converter bridges. For 0.5-pu active-power flow, the same voltage waveforms are given in Fig. 2–14 (b). As can be seen the reduction in voltage stress with reduction in active-power flow is insignificant.

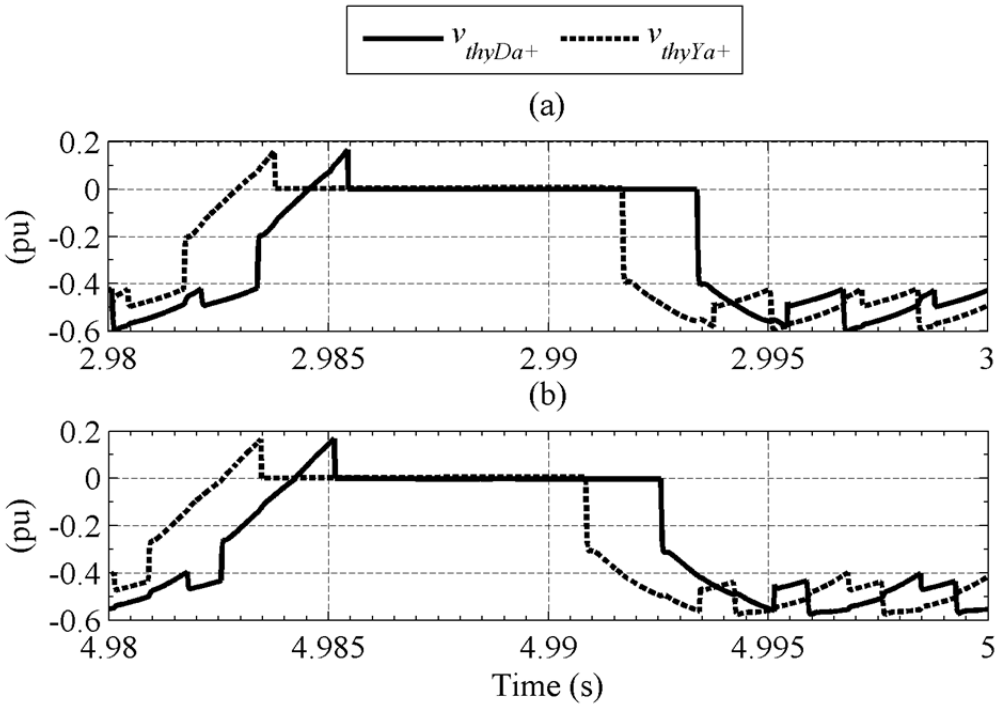

Fig. 2–14. Instantaneous voltage appearing across the thyristors with their anodes connected to phase *a* with active power equal to (a) 1 pu and (b) 0.5 pu.

2.3.4 Current Harmonics

The harmonic spectra of i_{lDa} and i_{sDa} are shown in Fig. 2–15 (a) and (b) respectively for rated-power flow. Predictably, the dominant harmonics are the 5th, 7th, 11th, 13th, 17th, 19th and so forth. The lower the harmonic number, the bigger the passive components required to filter these out. Harmonic spectra for the same currents at 0.5-pu active power are given in Fig. 2–16. A comparison between Fig. 2–15 and Fig. 2–16 reveals that the THD figures go up as the power goes down. The dominant-harmonic magnitudes do not decrease linearly with the decrease in active power.

THD figures and major harmonics for these two cases are given in TABLE 2–2. This is the first of a series of tables that will be generated in this and the succeeding chapter for i_{lDa}, i_{sDa}, i_{lYa}, i_{sYa}, and i_{sa}. These tables would provide instant comparison for all the series-compensation topologies discussed in this work. It can be seen in TABLE 2–2 that the amplitudes of significant harmonics do not drop linearly with active-power flow; therefore, we observe an increased THD value for lower active power.

Similarly, the harmonic spectra of i_{lYa} and i_{sYa} with P_s = 1 pu are presented in Fig. 2–17 (a) and (b) respectively. These are quite similar to the ones in the *D* branch. The harmonic spectra of the same currents at half power (presented in Fig. 2–18) have increased THD figures as in the case of *D*-branch currents. The important data extracted from the *Y*-branch harmonic spectra are tabulated in TABLE 2–3.

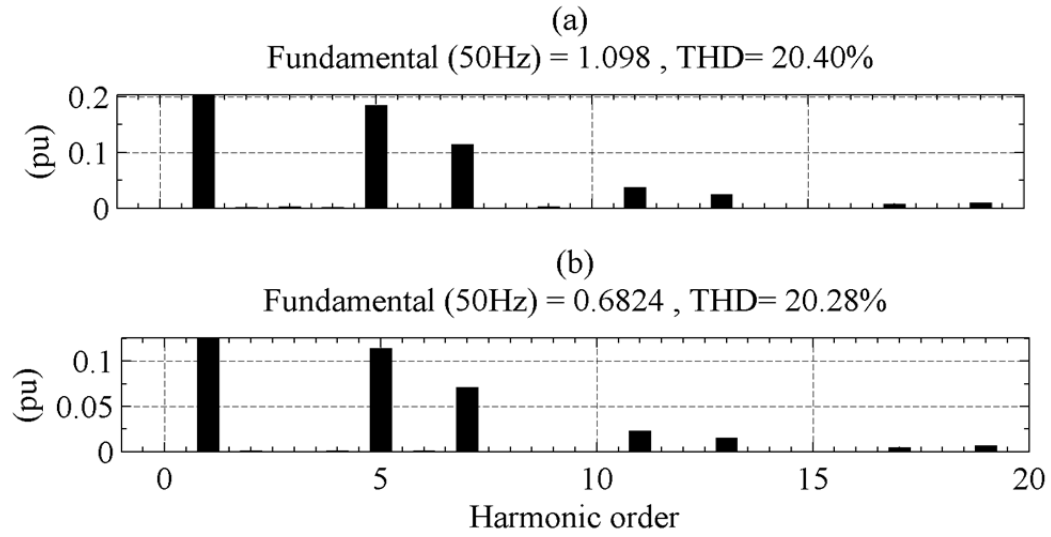

Fig. 2–15. Harmonic spectra at 1-pu active power (a) i_{lDa}, and (b) i_{sDa}.

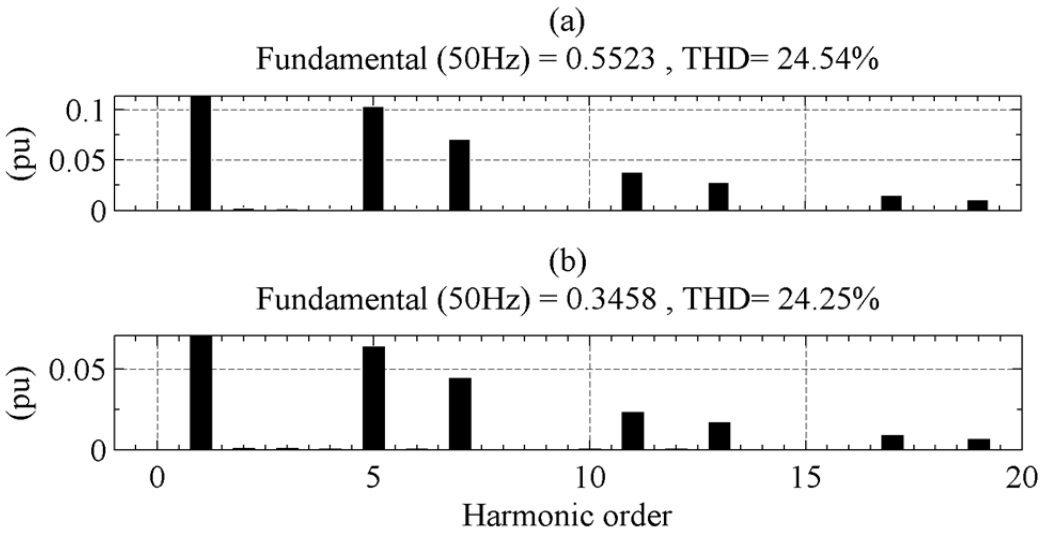

Fig. 2–16. Harmonic spectra at 0.5-pu active power (a) i_{lDa}, and (b) i_{sDa}.

TABLE 2–2
Important Harmonic Figures in The D Branch

	P_s (pu)	Parameter	Value
i_{lDa}	1	THD (%)	20.40
		5^{th} (pu)	0.1855
		7^{th} (pu)	0.1151
		11^{th} (pu)	0.0377
		13^{th} (pu)	0.0246
	0.5	THD (%)	24.54
		5^{th} (pu)	0.1035
		7^{th} (pu)	0.0710
		11^{th} (pu)	0.0379
		13^{th} (pu)	0.0276
i_{sDa}	1	THD (%)	20.28
		5^{th} (pu)	0.1147
		7^{th} (pu)	0.0712
		11^{th} (pu)	0.0230
		13^{th} (pu)	0.0151
	0.5	THD (%)	24.25
		5^{th} (pu)	0.0640
		7^{th} (pu)	0.0442
		11^{th} (pu)	0.0231
		13^{th} (pu)	0.0171

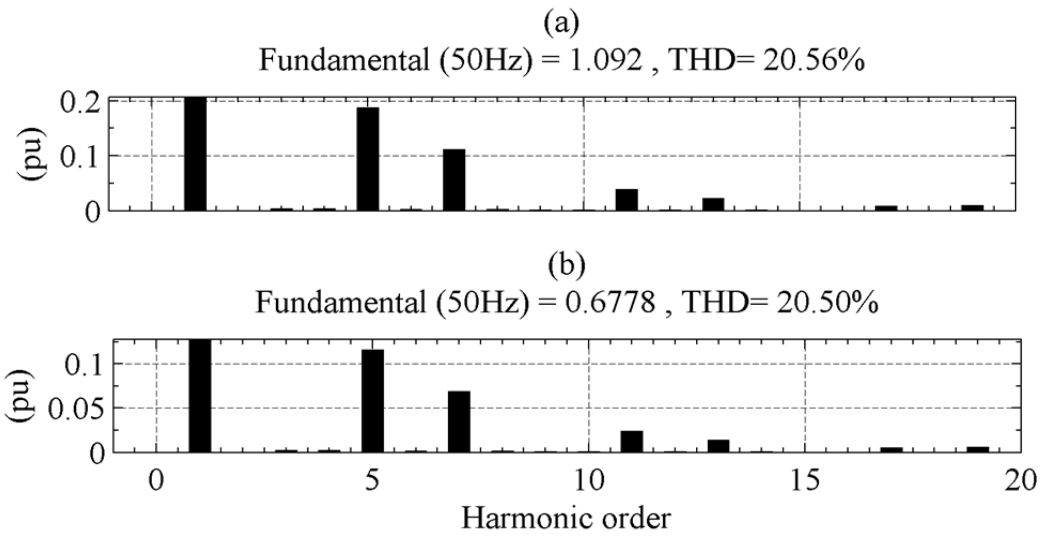

Fig. 2–17. Harmonic spectra at 1-pu active power (a) i_{lYa}, and (b) i_{sYa}

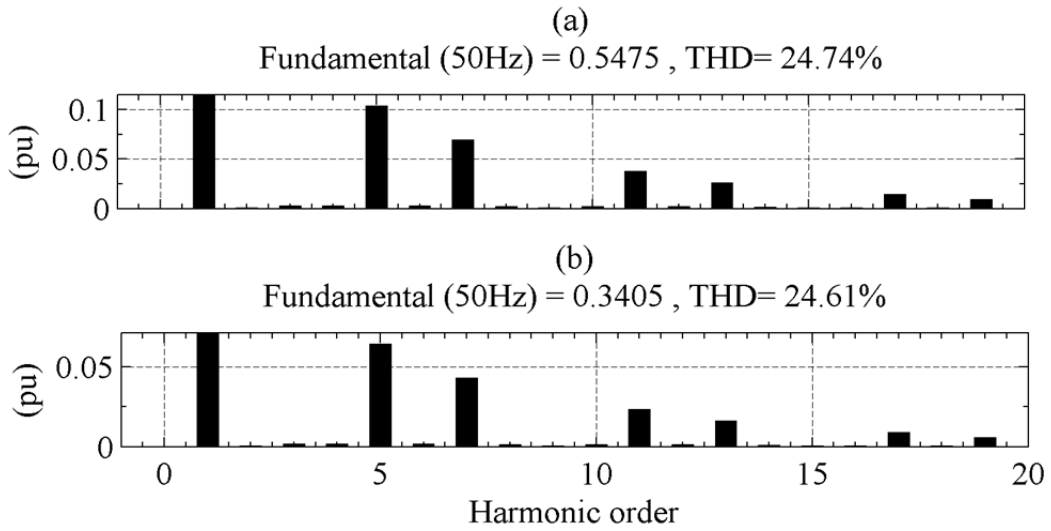

Fig. 2–18. Harmonic spectra at 0.5-pu active power (a) i_{lYa}, and (b) i_{sYa}.

TABLE 2–3
Important Harmonic Figures in The *Y* Branch

	P_s (pu)	Parameter	Value
i_{lYa}	1	THD (%)	20.56
		5^{th} (pu)	0.1882
		7^{th} (pu)	0.1117
		11^{th} (pu)	0.0388
		13^{th} (pu)	0.0229
	0.5	THD (%)	24.74
		5^{th} (pu)	0.1043
		7^{th} (pu)	0.0697
		11^{th} (pu)	0.0382
		13^{th} (pu)	0.0264
i_{sYa}	1	THD (%)	20.50
		5^{th} (pu)	0.1164
		7^{th} (pu)	0.0691
		11^{th} (pu)	0.0240
		13^{th} (pu)	0.0142
	0.5	THD (%)	24.61
		5^{th} (pu)	0.0646
		7^{th} (pu)	0.0431
		11^{th} (pu)	0.0237
		13^{th} (pu)	0.0164

Finally, the harmonic spectra of i_{sa}, i_{fa} and i_{ga} are given in Fig. 2–19 (a), (b), and (c) respectively. The same are repeated for 0.5-pu P_s in Fig. 2–20. The dominant harmonics in i_{sa} (Fig. 2–19 (a)) are now 11^{th} and 13^{th} instead of the 5^{th} and the 7^{th} in the

individual-transformer currents. This is why a 12-pulse arrangement is preferred over the 6-pulse HVDC scheme. The filter current i_{fa}, mainly consists of a large fundamental portion and 11th and 13th harmonic terms (Fig. 2–19 (b)). The fundamental portion is for fundamental-frequency reactive-power compensation whereas the harmonic terms are cancelling the harmonics drawn by the converter arrangement. As a consequence of the filter action, the grid current i_{ga} is now almost sinusoidal with a THD of less than 0.5%. The peak of the fundamental component in i_{ga} is much smaller than that in i_{sa}. The reason is the fundamental frequency quadrature current which is supplied by the shunt passive filter. The peak of the fundamental component being supplied by the filter is around 0.734 pu which is quite high which asks for a large arrangement with bulky capacitors and inductors capable of handling these currents at the grid voltages.

Important harmonic characteristics for i_{sa} are given in TABLE 2–4. The significant figures are the magnitudes of the 11th and the 13th harmonics. These are the lowest harmonics for which tuned filters are installed and take up a lot of space. In addition, high-pass filters are installed to filter out higher-order harmonic contents. In the case of 0.5-pu P_s, i_{fa} is performing its harmonic-compensation duty satisfactorily. However, the fundamental component does not drop in proportion to the active power. The same effect was observed in Fig. 2–8 (d), where the filter appeared to be unable to control its reactive-power output and the excess reactive power was observed to be absorbed by the grid.

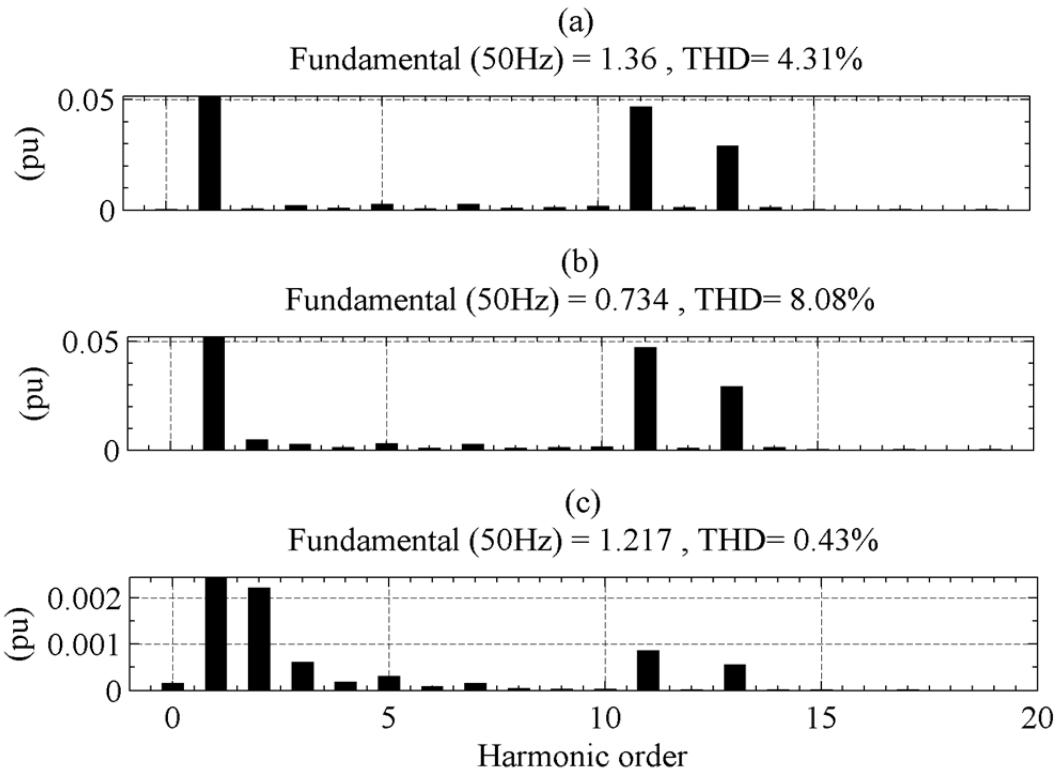

Fig. 2–19. Frequency spectra at 1-pu active power (a) i_{sa}, (b) i_{fa}, and (c) i_{ga}

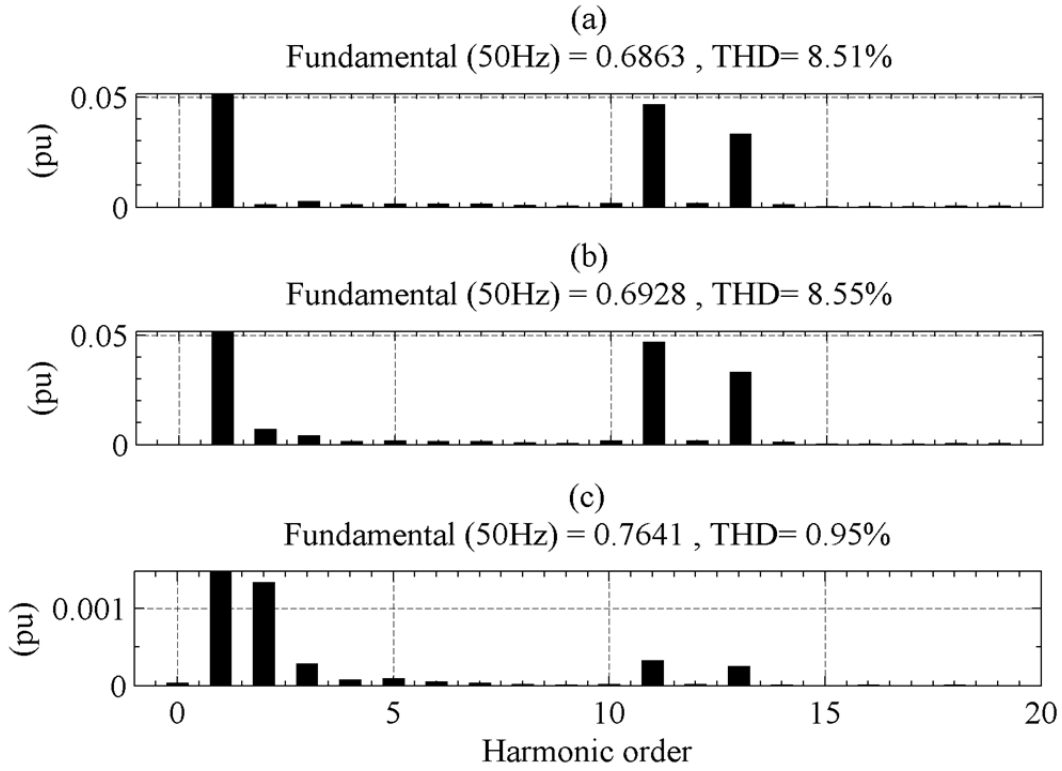

Fig. 2–20. Frequency spectra at 0.5-pu active power (a) i_{sa}, and (b) i_{fa}, and (c) i_{ga}..

TABLE 2–4
Important Harmonic Figures in the Combined Terminal Current

	P_s (pu)	Parameter	Value
i_{sa}	1	THD (%)	4.31
		5^{th} (pu)	0.0027
		7^{th} (pu)	0.0027
		11^{th} (pu)	0.0470
		13^{th} (pu)	0.0293
	0.5	THD (%)	8.51
		5^{th} (pu)	0.0017
		7^{th} (pu)	0.0015
		11^{th} (pu)	0.0468
		13^{th} (pu)	0.0334

2.3.5 Instantaneous Power

The instantaneous powers at different points in the system are depicted in Fig. 2–21. The DC -link instantaneous power shows the characteristic 12-pulse behaviour (Fig. 2–21 (a)) which consists of 6-pulse power pattern of the two thyristor bridges (Fig. 2–21 (b)) displaced in such a fashion that they create a 12-pulse pattern. The leakage

reactance of the converter transformers changes the instantaneous-power waveforms into the primary windings as shown in Fig. 2–21 (c) and their sum is again a 12-pulse pattern, though it is much smoother than that on the DC link. The shunt passive filter instantaneous power (Fig. 2–21 (d)) has the same wave-shape as p_s but is inverted. These two add up to make p_g which has a much smoother wave-shape with very small oscillatory component as depicted in Fig. 2–21 (e). It can be seen that the current harmonics have a direct impact on power oscillations. The smaller these harmonics, the smaller will be the power oscillations. These power oscillations should be minimized to avoid the excitation of resonances in the AC grid.

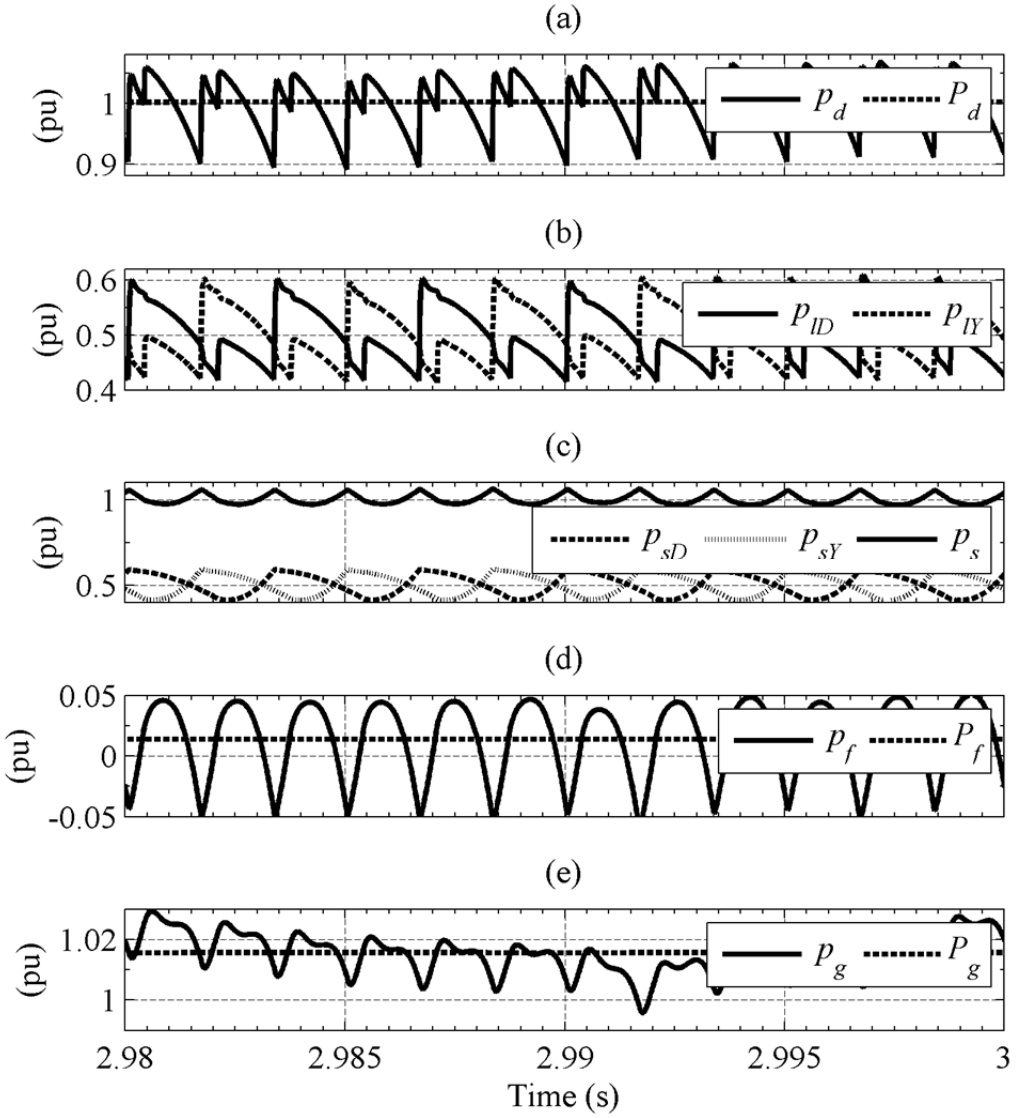

Fig. 2–21. Instantaneous power behaviour at (a) the DC link, (b) the thyristor bridge terminals, (c) converter-transformer primary windings, (d) shunt passive filter, and (e) the grid.

The active power transferred on the DC link is reduced by reducing the current order keeping the DC-link voltage the same. The instantaneous powers at different

points in the system are plotted again for reduced active power in Fig. 2–22. As the currents in the system go down, the reactive energy stored in the leakage reactance of the converter transformers also goes down. Secondly, the reactive-power consumption of the converter bridges also falls. The former has an effect on the duration of commutation due to which the currents commutate faster than in the case of rated power. This faster transition leads to proportionally-higher harmonic content in the system currents. The converter-side currents are depicted in Fig. 2–11 and confirm that the commutation does indeed occur much faster. The consequence of this is reflected on the primary side as depicted in Fig. 2–13.

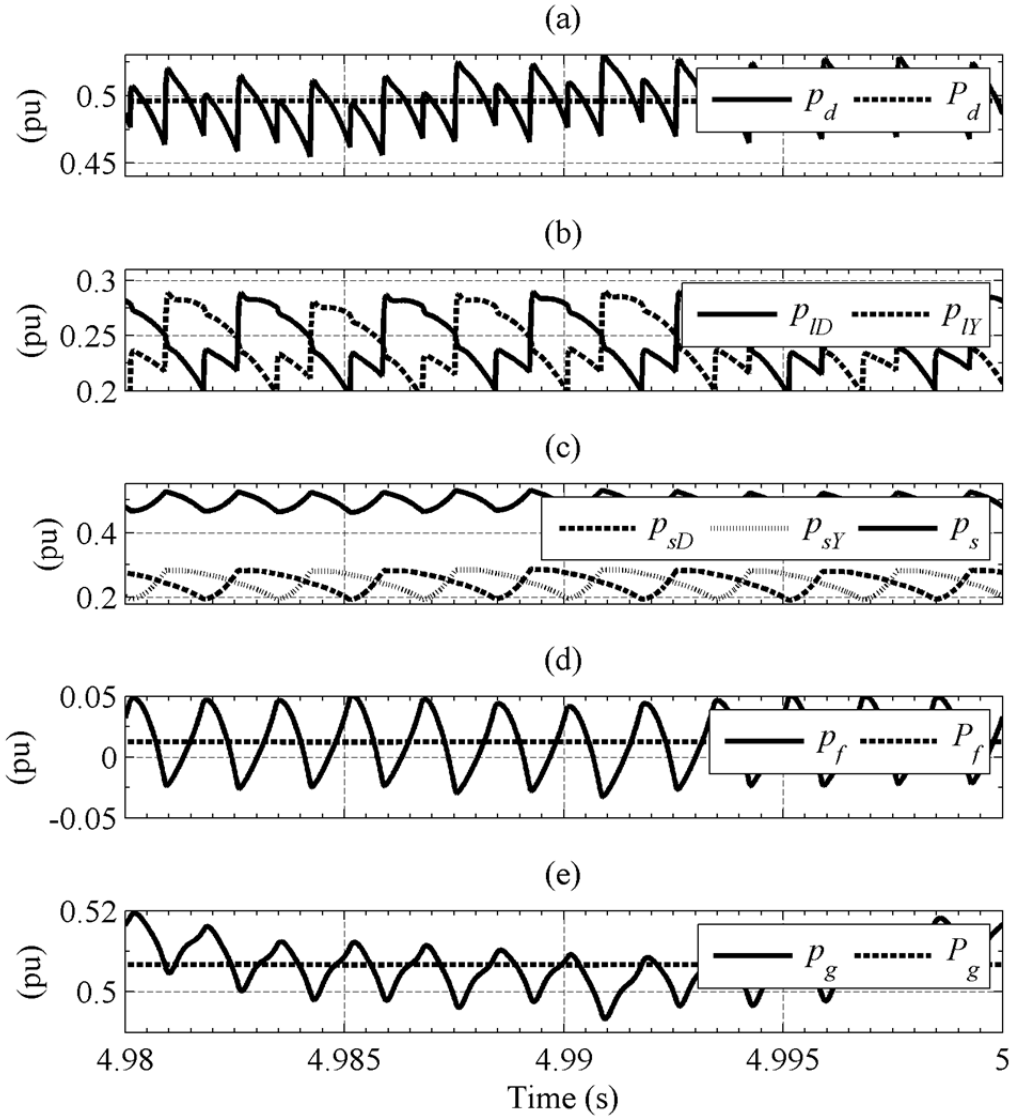

Fig. 2–22. Instantaneous power behaviour for 0.5-pu active power at (a) the DC link, (b) the thyristor bridge terminals, (c) converter-transformer primary windings, (d) shunt passive filter, and (e) the grid.

2.4 Conclusion

The behaviour of the rectifier terminal of LCC HVDC has been presented in this chapter. The schematic arrangements have been discussed and simulation results presented for changing active power reference.

It has been seen that the reactive power consumption of the link is composed of the reactive power consumed by the AC/DC conversion process of the thyristor bridges and that consumed by the leakage reactance of the converter transformers. Both these components of reactive power change with change in the active power.

The shunt passive filter arrangement has to compensate for the reactive power as well as the harmonics in the current. The reactive power compensation is necessary for stable AC grid operation whereas the harmonic compensation is required to avoid detrimental resonances in the AC grid, improve voltage quality at the filter bus, and reduce mechanical oscillation in the generating sources.

The fundamental-frequency component of the filter current is quite large as compared to the harmonic content it is supplying. This leads us to believe that the harmonics can be compensated with smaller filters if the shunt compensator is relieved of the duty of fundamental-reactive compensation. This is what is achieved with the use of CCC HVDC.

3 The Series-Capacitor Commutated Converter based HVDC

The series-capacitor commutated converter based HVDC is introduced in this chapter. Simulation results with special regards to the reactive-power and harmonic behaviour of the topology have been presented. In addition, the variables of interest have been compared with the conventional shunt-compensated HVDC.

The behaviour of the series-Capacitor Commutated Converter based HVDC (CCC HVDC) will be discussed in this chapter. This topology owes its name to the series capacitors which are connected in series between the secondary of the converter transformers and the thyristor bridges in each phase and in each branch.

3.1 Simulation Setup

3.1.1 Schematic Arrangement

The schematic of CCC HVDC for these simulations is depicted in Fig. 3–1. It is similar to the shunt compensated system discussed in the preceding chapter, except the inclusion of six series capacitors, one in each phase, in between the converter transformer secondary and the thyristor bridge. The subscript '*k*' signifies the phase in which the capacitor is connected. The series capacitor value in each phase is 85 μF for the simulations presented in this chapter. The value has been chosen so as to compensate for the full reactive-power demand of the HVDC terminal at rated power flow. The rest of the details are the same as presented in Fig. 2–2, Fig. 2–3 , and Fig. 2–4.

3.1.2 Control Loops

The control loop presented in Fig. 2–6 has been used as it was, however, the control loop for firing the thyristors has to be modified to accommodate the inclusion of the voltages injected by the series capacitors. Therefore, the modified form of the control loop in Fig. 2–5 is presented in Fig. 3–2. The voltages e'_{jab}, e'_{jbc}, and e'_{jca} act as commutating voltages now, for generation of firing pulses for the thyristor bridges.

It is important to note that v_{compjk} (the voltage injected by the series capacitors in the respective branch and phase) is dependent upon the current which in turn depends upon the active-power command. The change in DC-link power order will, therefore, affect the voltage injected by series capacitors and also force a change in the instant of firing with respect to the voltages behind the leakage reactance. This will be explained further in the results section.

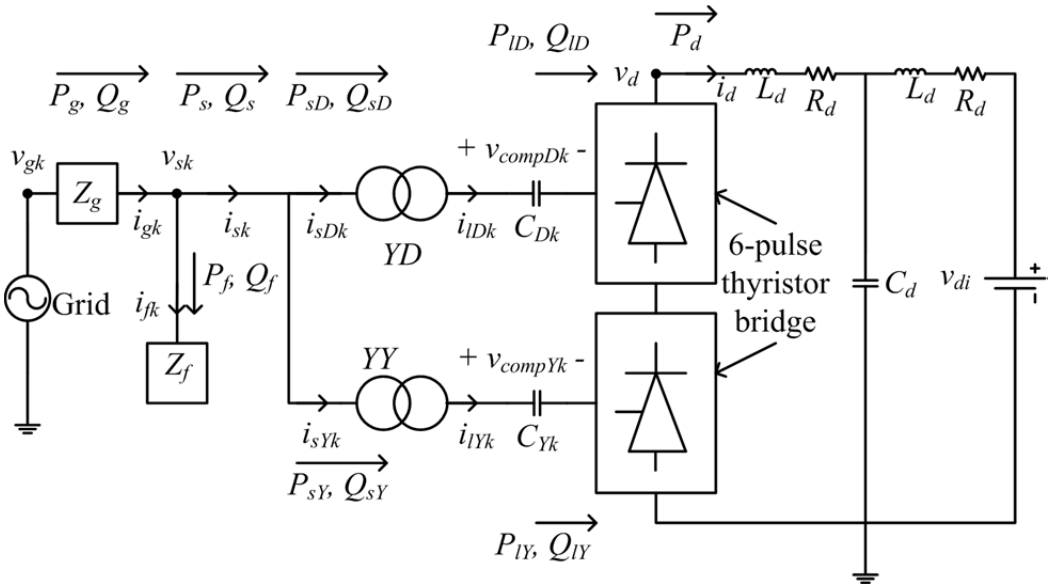

Fig. 3–1. Schematic diagram of the simulation setup for CCC HVDC.

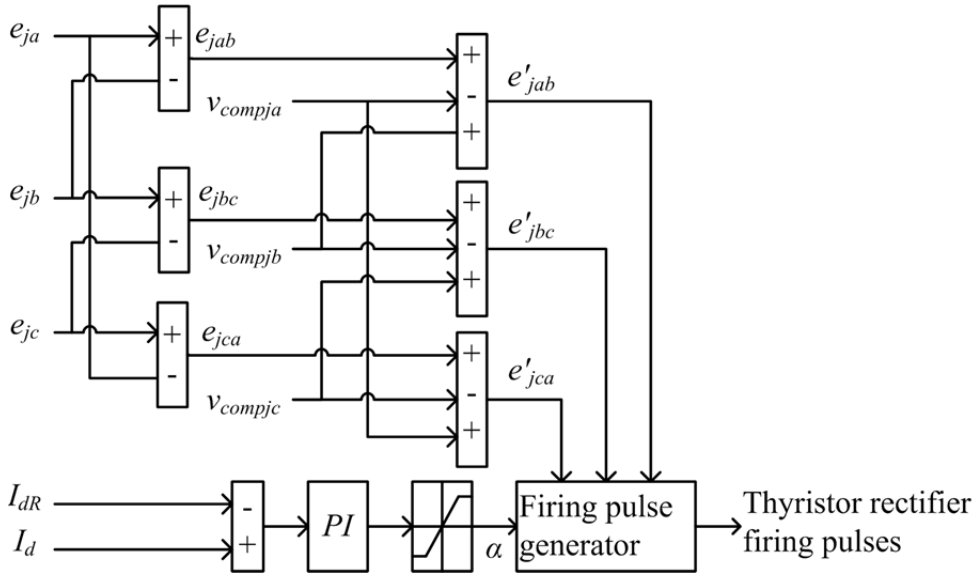

Fig. 3–2. Active-power control loop for CCC HVDC.

3.2 The Commutation Process

The eventual commutation circuit is shown in Fig. 3–3. It obviously has two capacitors in series with the leakage reactance of the converter transformers indicating and effective reduction in the commutation reactance. The equation of commutation circuit becomes:

$$e_{jac} = \sqrt{2}E_j \sin(\omega t) = 2L_{tr}\frac{di_{comm}}{dt} - \frac{1}{C_{ja}}\int i_{comm}dt + \frac{1}{C_{jc}}\int i_{comm}dt + v_{C_{ja}(0-)} + v_{C_{jc}(0-)} \tag{3.1}$$

The initial voltages on the series capacitors depend upon the history of current flow through the respective phases. In brief, just before the start of commutation of current to phase *a*, the initial voltage on the capacitor in phase *a* would contain an assisting polarity to the commutation voltage. This would be attained during the negative current flow through phase *a*. At the same time, the current flowing in phase *c* would be charging the capacitor in phase *c* in a polarity which would oppose the phase-*c* voltage. Both these voltage would add up to assist e_{jac}, such that the voltage at the thyristor terminals would cross at an angle (λ) before the crossover of e_{jac}. The reader is referred to [60, 62] for details.

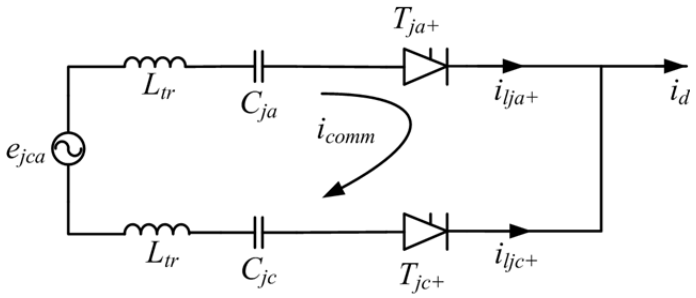

Fig. 3–3. Commutation circuit for CCC HVDC.

Referring to (2.6), the commutation angle *u* would be reduced as the capacitive reactance tends to reduce the overall reactance in the path of current. This reduced value of u would influence the presence of harmonics as seen in (2.16). The active power is given by:

$$P_{lj} = \sqrt{3}E'_{lj}I_{lj}\cos(\varphi) \tag{3.2}$$

The reactive power contribution of the series capacitors is:

$$Q_{compj} = 3I_{lj}^2 / \omega C_j \tag{3.3}$$

The measurements are carried in such a manner that the passive sign convention is applicable for the series capacitors. The reactive-power contribution would thus appear to be negative in the simulation results. The smaller the value of the series capacitors, the higher would be the reactive power supplied by these. Simultaneously, smaller capacitors would mean higher capacitive reactance leading to higher voltages injected by these. Secondly, the reactive-power contribution depends upon the current. Therefore, if the reactive power is sufficient at a specific current level, it would be far less than required at lower currents. The injected voltages at these currents would also be very small leading to smaller values of λ. The total reactive power as seen by the primary side is:

$$Q_{sj} = Q_{lj} + Q_{trj} - Q_{compj} \tag{3.4}$$

The variable nature of Q_{compj} means that Q_{sj} can be zero at a specific load; however, it would be non-zero at other loads.

3.3 Simulation Results

The simulations start with an active-power reference of 1 pu as in section 2.2. The series capacitors (bypassed at the start of the simulation) are switched in at 3 s. The active-power reference changes to 0.5 pu at 5 s.

3.3.1 Active and Reactive Powers

The active and reactive powers at different points in the system are presented in Fig. 3–4. With reference to Fig. 3–4 (a), P_s and Q_s start at their steady-state values before the series capacitors are switched in. As the power reference does not change, P_s stays at 1 pu after the capacitors are switched in. However, Q_s is reduced to 0 pu. At 5 s, P_s is reduced to 0.5 pu following the power command. But this change is accompanied by an increase in Q_s. This increase can be explained by the plots in Fig. 3–4 (b) and (c). At 1-pu active-power flow, the reactive power supplied by the series capacitors is sufficient to compensate for the reactive power consumed by the converter terminal and that consumed by the leakage reactance of the converter transformers. Therefore, Q_{sD} and Q_{sY} drop to 0 pu as seen in Fig. 3–4 (b) and (c) respectively, in the period between 3 s and 5 s. When P_s is reduced to 0.5 pu at 5 s, Q_{compD} and Q_{compY} are reduced in magnitude proportional to the square of the current. Therefore Q_{sD} and Q_{sY} do not remain 0 pu any longer. This has to be noted also that Q_{sD} and Q_{sY} values do not change after the addition of series compensation at 3 s.

The reactive powers of the filter and the grid are plotted in Fig. 3–4 (d). Before the introduction of series capacitors into the system, Q_f is compensating for Q_s. As the capacitors are switched in, the entire amount of filter reactive power is exported to the

grid, as Q_s is equal to 0. Due to the change in Q_s at 5 s, Q_g no longer remains equal to Q_f, as a part of Q_f is utilized in compensating for Q_s.

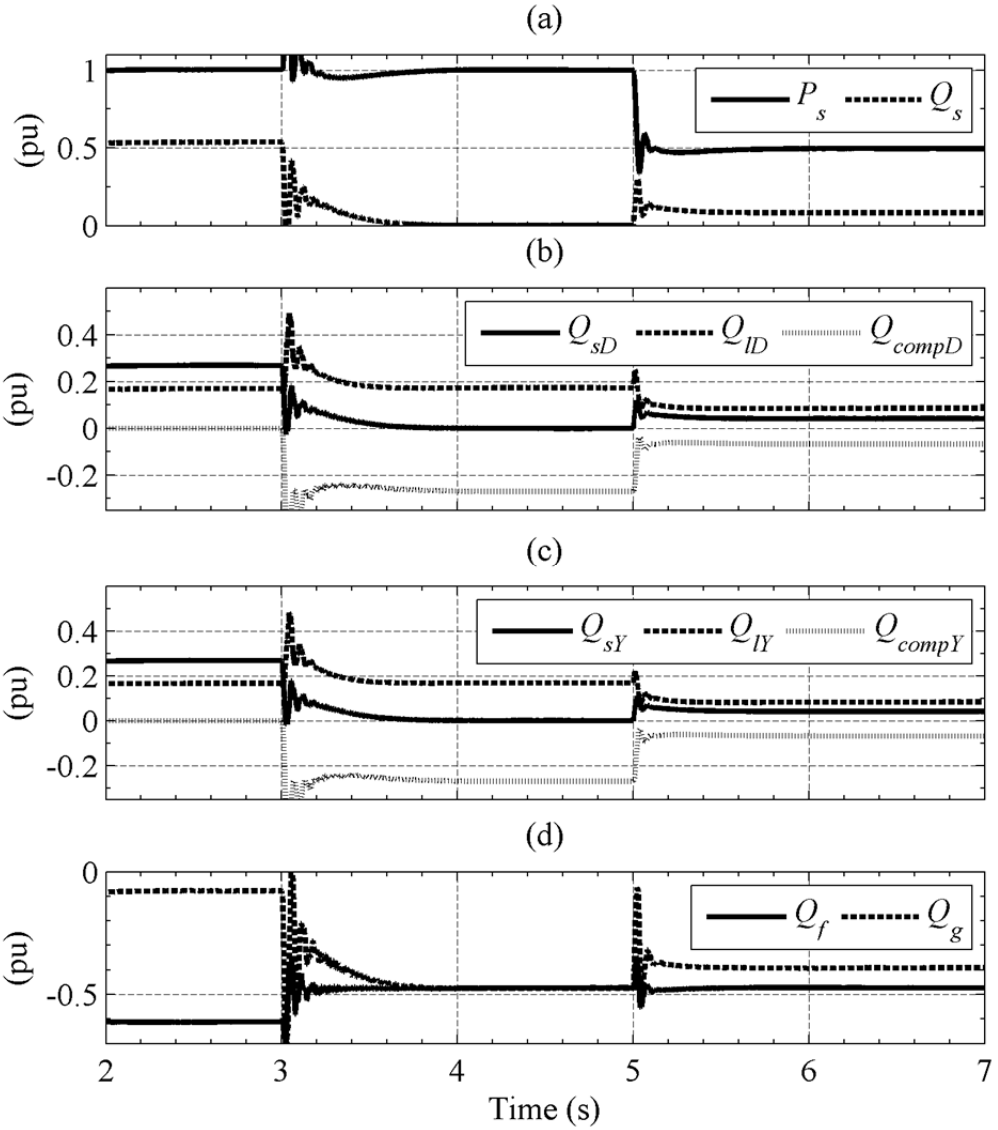

Fig. 3–4. Active and reactive powers for CCC HVDC.

3.3.2 Control Loop Operation

The behaviour of control loop depicted in Fig. 2–6 in conjunction with the control loop in Fig. 3–2 for keeping α at a constant value is presented in Fig. 3–5. The inclusion of series capacitors at 3 s eliminates the reactive-power flow into the converter transformers and hence reduces the voltage required to transmit the same amount of active power. The transition of P_s from 1 pu to 0.5 pu at 5 s does not influence V_{sa} significantly. The reason is a non-zero Q_s flowing into the converter transformers and voltage support is required to achieve 0.5-pu P_s with non-zero Q_s.

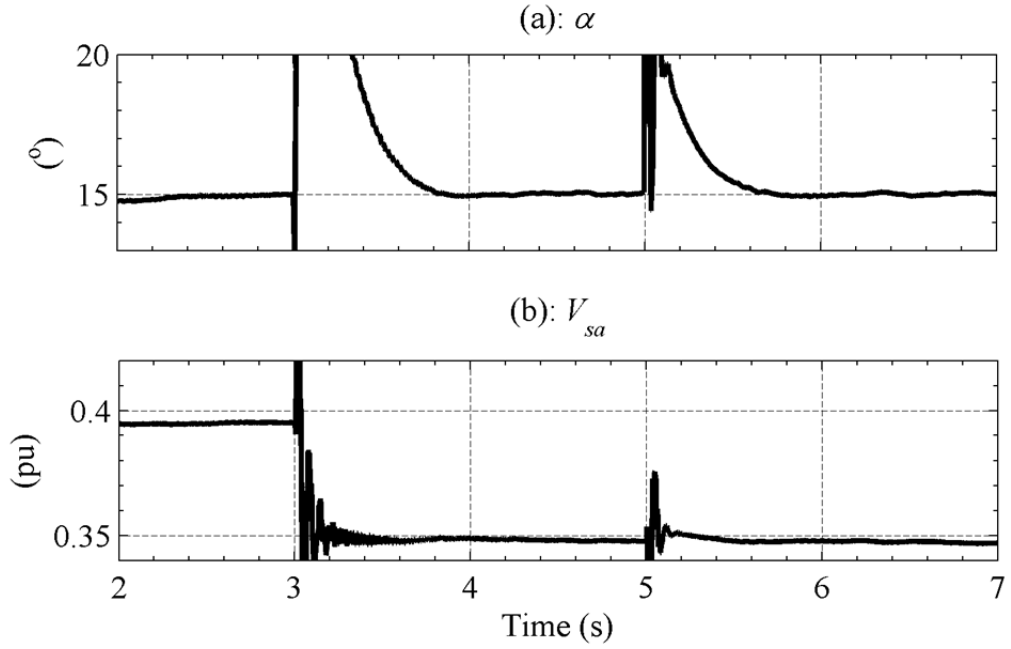

Fig. 3–5. Plots of (a) α and (b) rms value of phase-*a* voltage on the filter bus with a base voltage of 500 kV.

3.3.3 Instantaneous Currents and Voltages

To understand the effect of series capacitors, the capacitor voltage in phase *a* without compensation, with compensation at full load, and with compensation at 0.5-pu load are presented in Fig. 3–6 (a), (b), and (c) respectively. When the series capacitors are bypassed, no currents flow through them and therefore the voltages are zero (Fig. 3–6 (a)). Similar voltage patterns occur in the other phases with respect to the currents flowing through them. Due to these series voltages, the commutation voltages for thyristor firing in AC/DC converter bridges were modified in Fig. 3–2. The new commutations voltages for commutation between phase *c* and *a* for all the conditions are shown in Fig. 3–7. Without series compensation, e_{jca} crosses zero at the crossing point of the respective phase voltages (Fig. 3–7 (a)). With series compensation at full load, the crossover of commutation voltage occurs much before the phase-voltage crossover and hence the thyristor in the incoming phase can be fired earlier as compared to the case without series compensation (Fig. 3–7 (b)). In the case of partial load, the delay between the commutation-voltage crossover and the respective voltage-crossover is reduced (Fig. 3–7 (c)). This is due to the reduced capacitor voltages caused by a reduction in current flowing through them.

The commutation process for the *D* branch for all the three cases is depicted in Fig. 3–8. These commutations are similar, except in the duration of commutation which appears to reduce (Fig. 3–8 (b)) when capacitors are in the circuit. It reduces further when the active power reference goes down to 0.5 pu (Fig. 3–8 (d)). This alteration in the current wave-shape is an indication of changed harmonic composition which will be discussed in the next section. The commutation of current happens in a similar fashion in the *Y* branch which has not been shown here to keep the discussion short.

The currents on the primary side of the converter transformers at 1-pu active-power flow are depicted in Fig. 3–9. Due to modified commutating voltages, the currents commutate earlier in comparison with the uncompensated case and therefore the primary-side currents into the individual converter transformers are in phase with the respective phase voltages (Fig. 3–9 (a) and (b)). Their sum is i_{sa} which is also in phase with v_{sa} as can be seen in Fig. 3–9 (c). As the shunt-passive-filter arrangement has been unchanged from the uncompensated system, it injects its reactive and harmonic component without any control (Fig. 3–9 (d)) and therefore i_{ga} leads v_{sa} (Fig. 3–9 (e)) implying reactive-power export into the grid.

The same currents and voltages are plotted in Fig. 3–10 for 0.5-pu active power. As can be seen in Fig. 3–10 (a) and (b), i_{sDa} and i_{sYa} now lag v_{sa}. This implies insufficient reactive-power compensation by the series capacitors which results in i_{sa} lagging v_{sa} (Fig. 3–10 (c)).

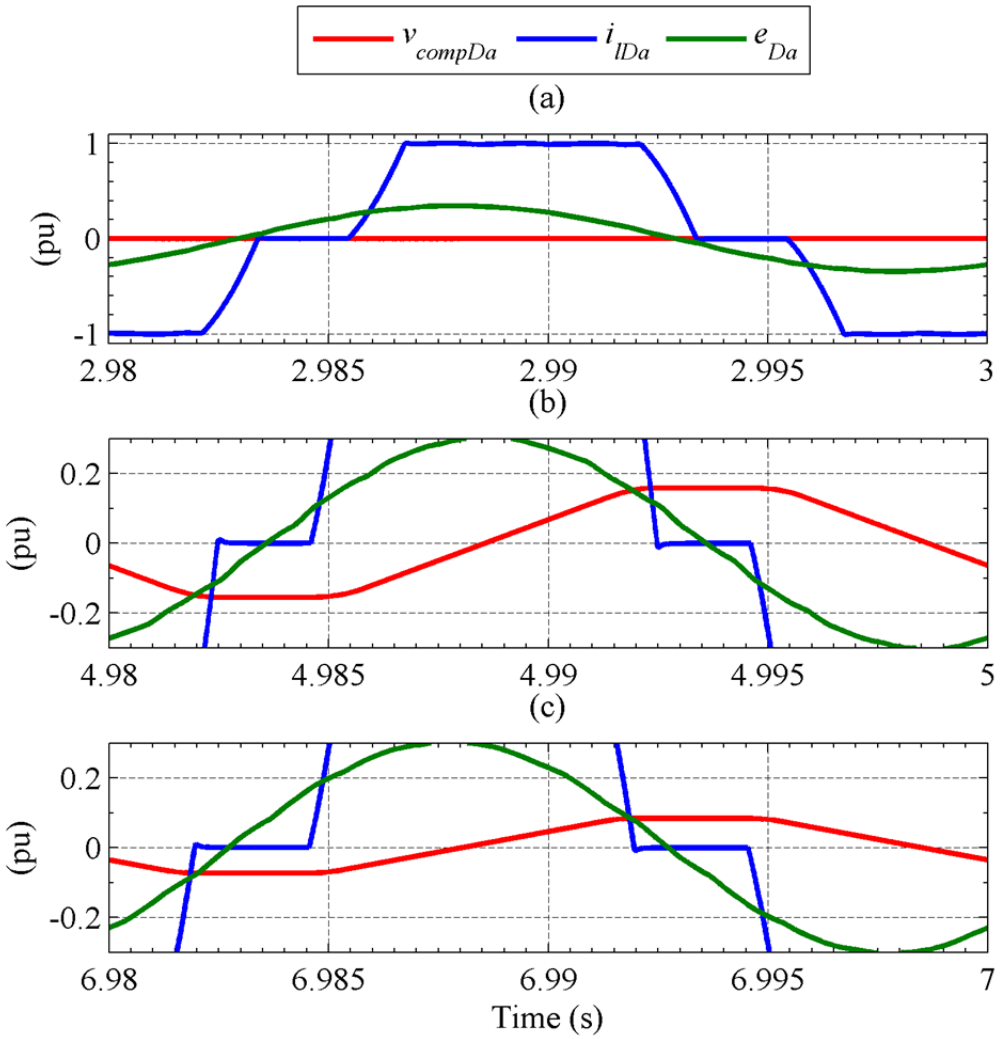

Fig. 3–6. Plots of compensator voltage, load current, and voltage behind the transformer reactance (a) without series compensation (b) at full load with series compensation, and (c) at 0.5-pu load with series compensation.

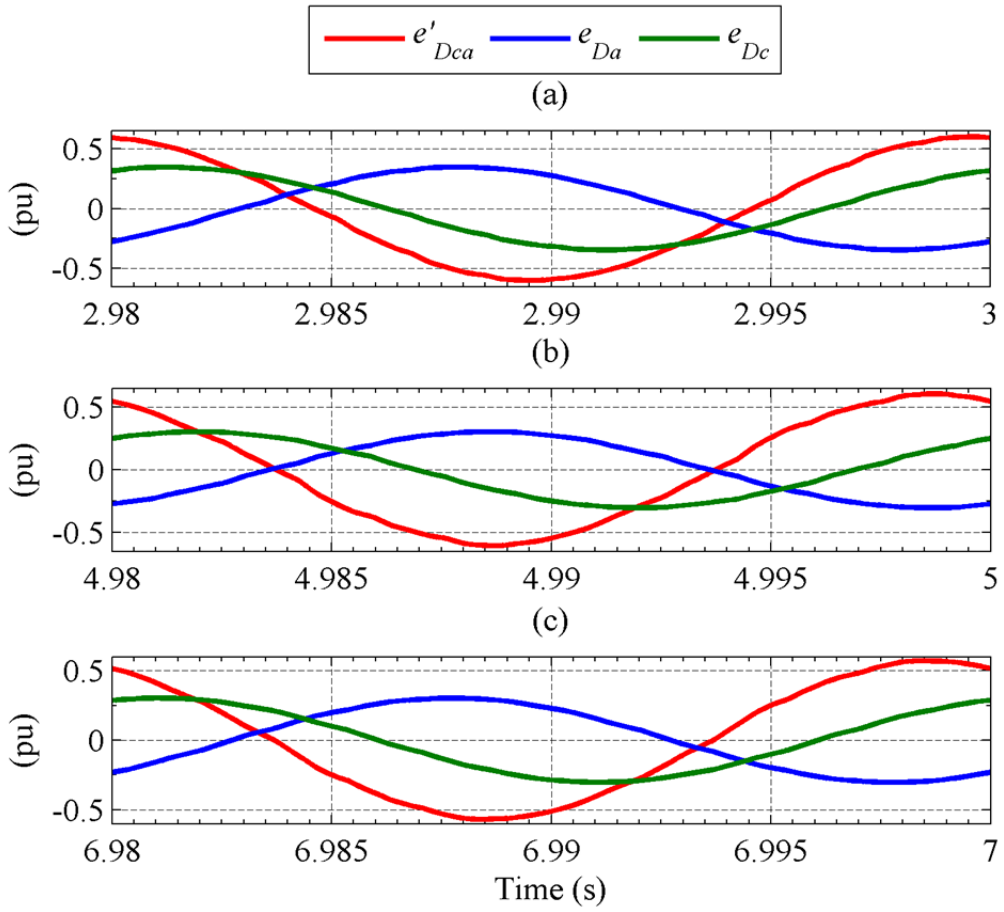

Fig. 3–7. Commutation voltage (a) without series compensation, (b) with series compensation at full load, and (c) with series compensation at 0.5-pu load.

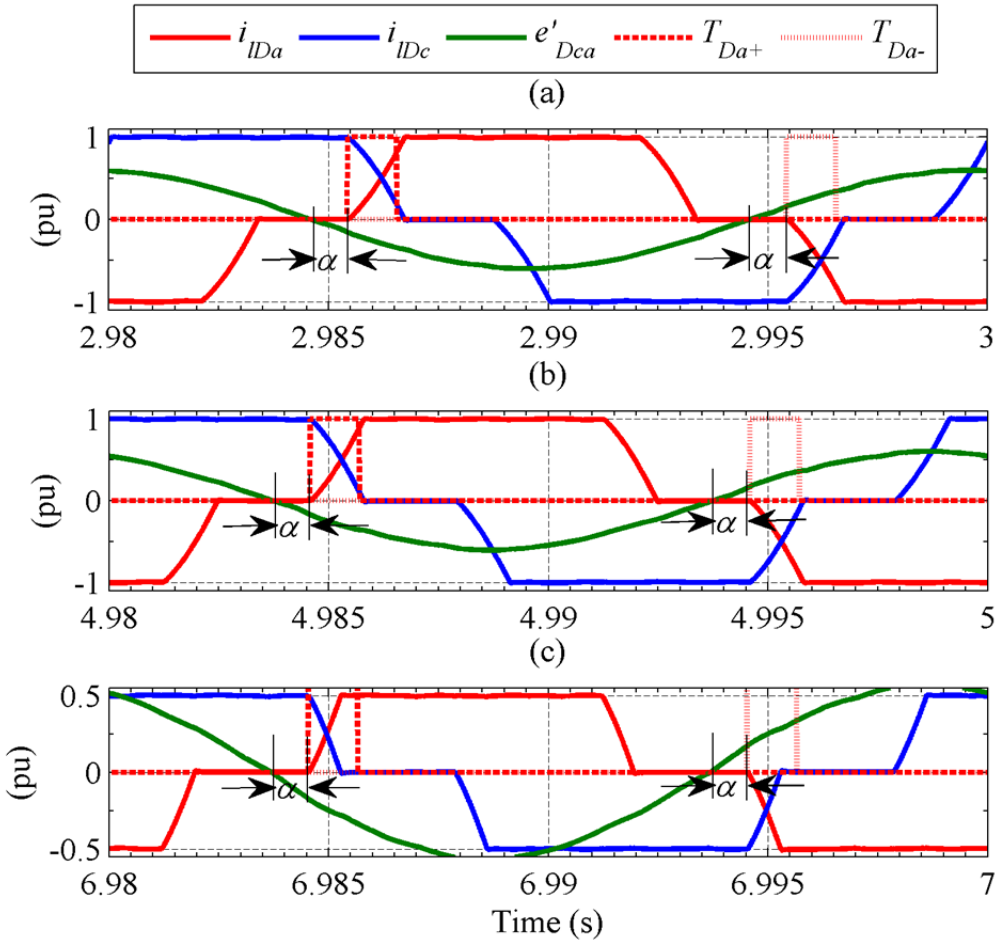

Fig. 3–8. Current commutation from phase *c* to *a* (a) without series compensation, (b) with series compensation at full load, and (c) with series compensation at 0.5-pu load.

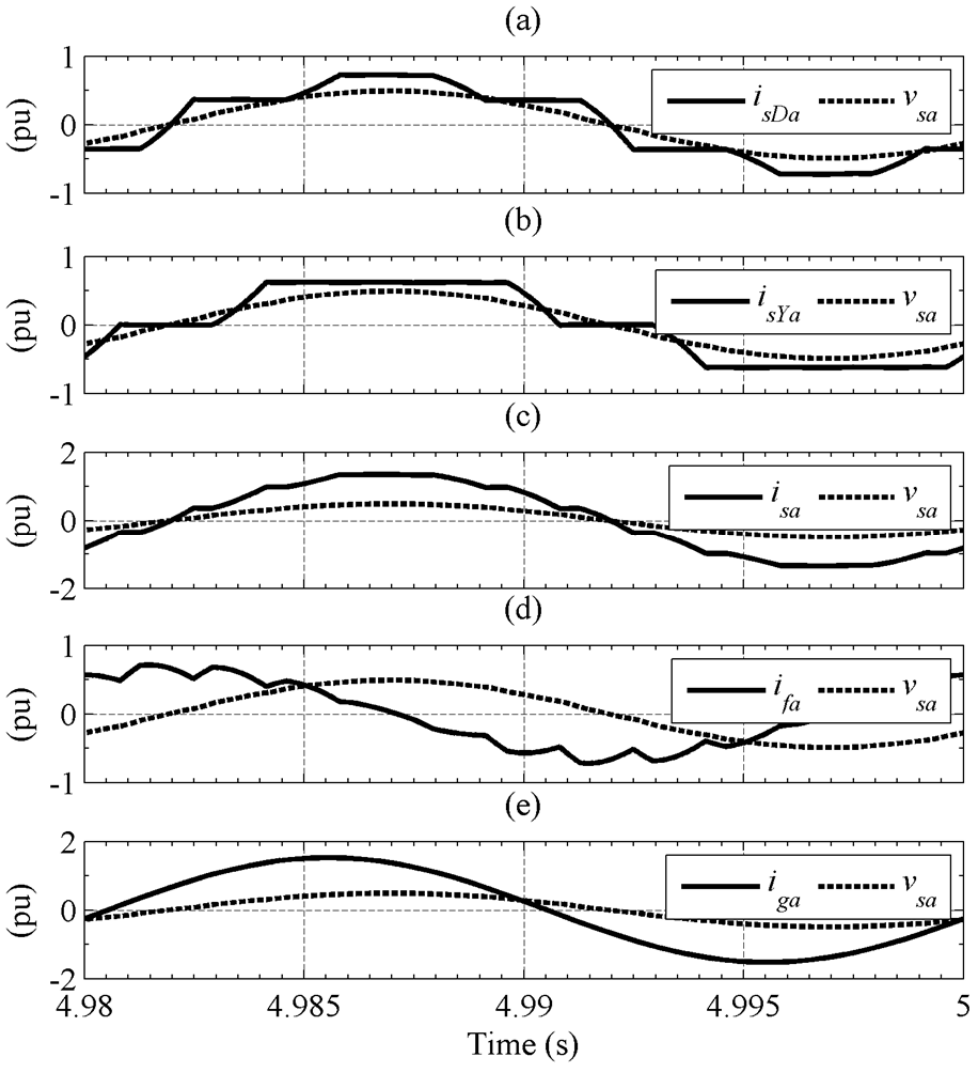

Fig. 3–9. Instantaneous currents and voltage in phase *a* on the primary side of the converter transformers at 1-pu active-power flow.

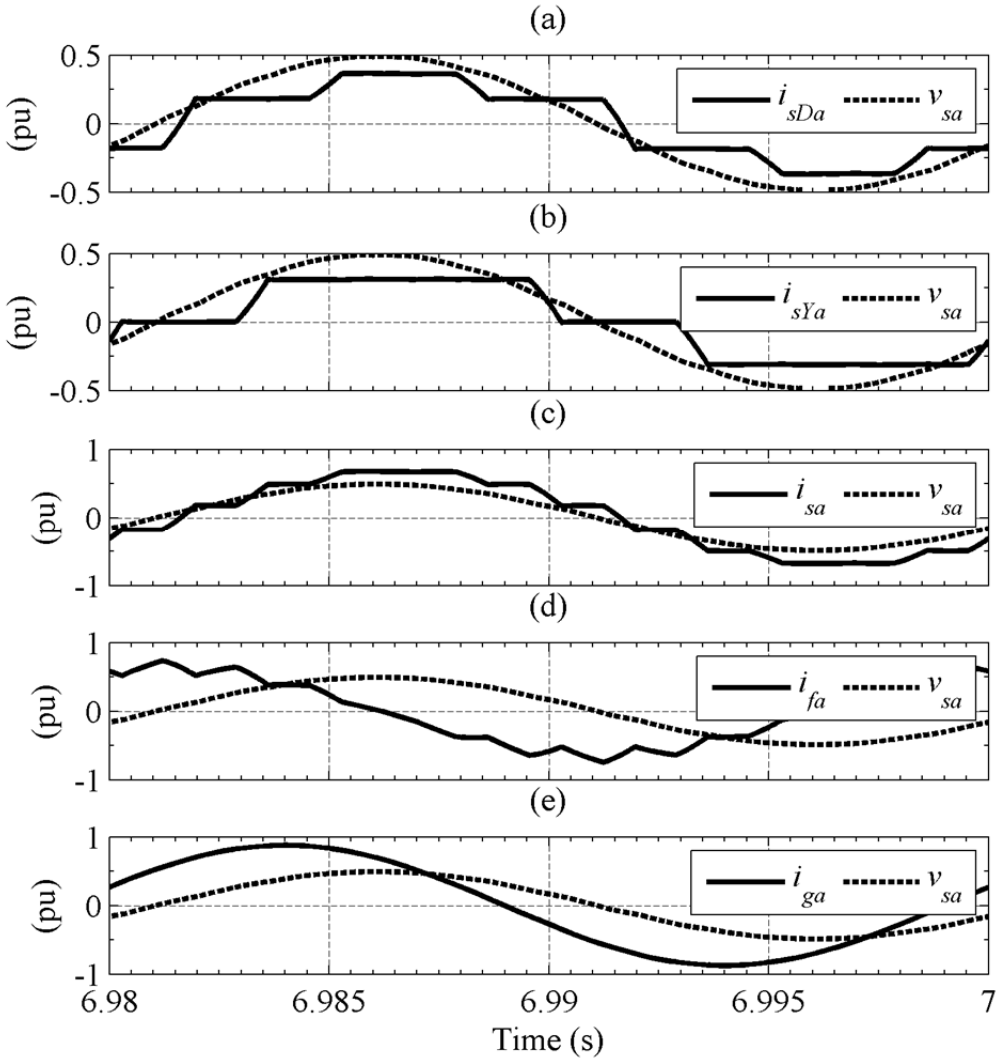

Fig. 3–10. Instantaneous currents and voltage in phase *a* on the primary side of the converter transformers at 0.5-pu active-power flow.

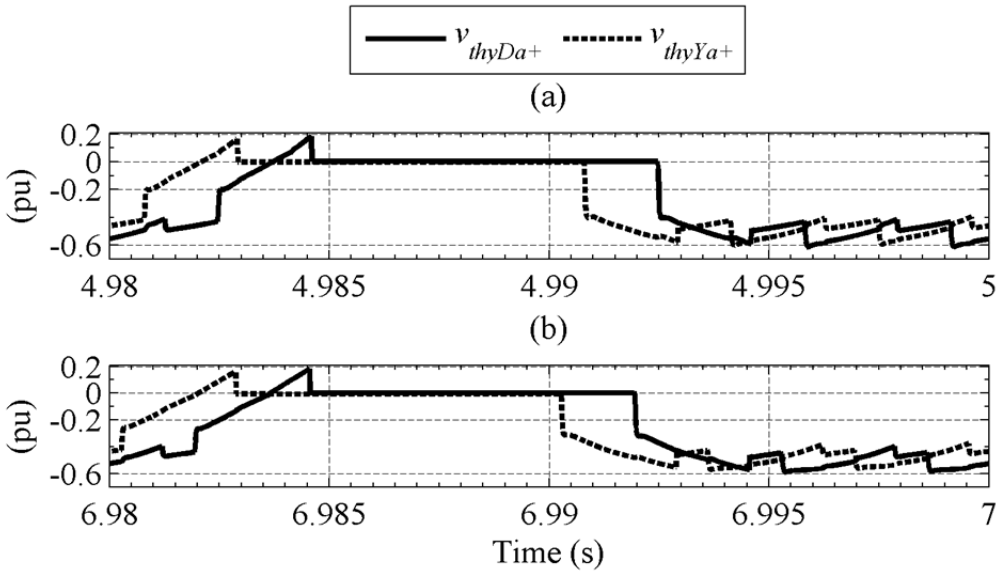

Fig. 3–11. Instantaneous voltage appearing across the thyristors with their anodes connected to phase *a* with active power equal to (a) 1 pu and (b) 0.5 pu.

The instantaneous device voltages appearing across the two thyristors with their anodes connected to phase *a* of the bridge in the *D* and *Y* branches are depicted in Fig. 3–11. These are similar to the ones presented in Fig. 2–14.

3.3.4 Current Harmonics

The harmonics in i_{lDa} and i_{sDa} are presented in Fig. 3–12 and Fig. 3–13 for 1-pu and 0.5-pu active-power flow respectively. A comparison of Fig. 3–12 and Fig. 2–15 reveals that the harmonic content in CCC HVDC is higher because of the reduced commutation time in this topology. Similar behaviour is observed at 0.5-pu active-power flow when Fig. 3–13 and Fig. 2–16 are compared. However, the difference between the two is smaller when compared to the case of 1-pu active-power flow. The reason being the reduced effect of the series capacitors as the injected voltage is directly proportional to the current.

The important harmonic characteristics of the *D*-branch currents are tabulated in TABLE 3–1. The acronym SPF refers to Shunt Passive Filter. The data in this column comes from chapter 2, where there was no series compensation and the conventional shunt arrangement was used for reactive-power compensation. The acronym CCC is used for CCC HVDC topology. The THD values for the currents flowing in the primary and the secondary windings of the converter transformer in the *D* branch at full and half power are higher than the shunt compensation topology. These numbers are significant as the converter transformer has to be designed to sustain the harmonic stress. It is observed that the CCC-HVDC topology contributes negatively to the harmonic behaviour and, thus, complicates converter-transformer design.

Similar observations can be made for i_{lYa} and i_{sYa} whose harmonic spectra for 1-pu and 0.5-pu active-power flow are given in Fig. 3–14 and Fig. 3–15 respectively.

The important harmonic numbers in the *Y*-branch currents are given in TABLE 3–2. It also exhibits deterioration in harmonic numbers similar to what was noted in the case of *D*-branch.

The harmonic spectra of i_{sa}, i_{fa}, and i_{ga} at 1-pu active power are shown in Fig. 3–16 (a), (b), and (c) respectively. A comparison of i_{sa} with series-capacitor compensation with that in the uncompensated case, plotted in Fig. 2–19 (a), shows that the harmonic content is somewhat higher in the compensated case. The shunt passive filter is able to supply the necessary amount of harmonic content to prevent the harmonics from spreading into the AC grid as can be seen in Fig. 3–16 (b) and (c). The harmonic content in i_{sa}, i_{fa}, and i_{ga} given in Fig. 3–17 (a), (b), and (c) (at 0.5-pu active power) reveal that the THD figures increase with lower active power and the grid current contains more distortion than in the full-load case. TABLE 3–3 lists the important harmonic numbers in i_{sa} for CCC-HVDC topology. The magnitudes of the 11^{th} and the 13^{th} harmonics are much higher than those with SPF. The shunt filter, therefore, has to be designed for larger currents and would take up more space.

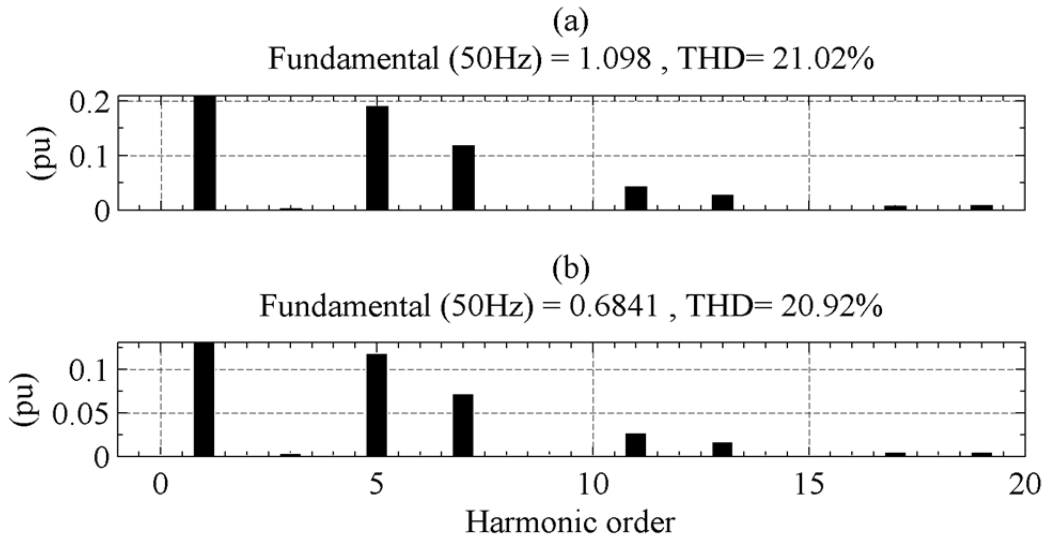

Fig. 3–12. Harmonic spectra at 1-pu active power (a) i_{lDa} and (b) i_{sDa}.

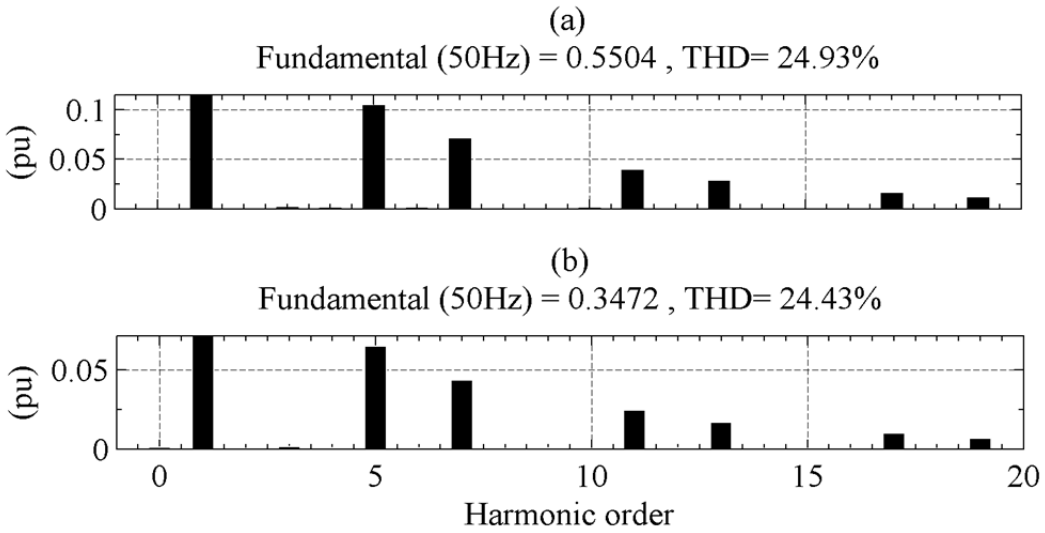

Fig. 3–13. Harmonic spectra at 0.5-pu active power (a) i_{lDa} and (b) i_{sDa}.

TABLE 3–1
Important Harmonic Figures in The *D* Branch

	P_s (pu)	Parameter	Value	
			SPF	CCC
i_{lDa}	1	THD (%)	20.40	21.02
		5^{th} (pu)	0.1855	0.1905
		7^{th} (pu)	0.1151	0.1180
		11^{th} (pu)	0.0377	0.0430
		13^{th} (pu)	0.0246	0.0275
	0.5	THD (%)	24.54	24.93
		5^{th} (pu)	0.1035	0.1048
		7^{th} (pu)	0.0710	0.0710
		11^{th} (pu)	0.0379	0.0393
		13^{th} (pu)	0.0276	0.0279
i_{sDa}	1	THD (%)	20.28	20.92
		5^{th} (pu)	0.1147	0.1189
		7^{th} (pu)	0.0712	0.0718
		11^{th} (pu)	0.0230	0.0272
		13^{th} (pu)	0.0151	0.0166
	0.5	THD (%)	24.25	24.43
		5^{th} (pu)	0.0640	0.0650
		7^{th} (pu)	0.0442	0.0435
		11^{th} (pu)	0.0231	0.0246
		13^{th} (pu)	0.0171	0.0170

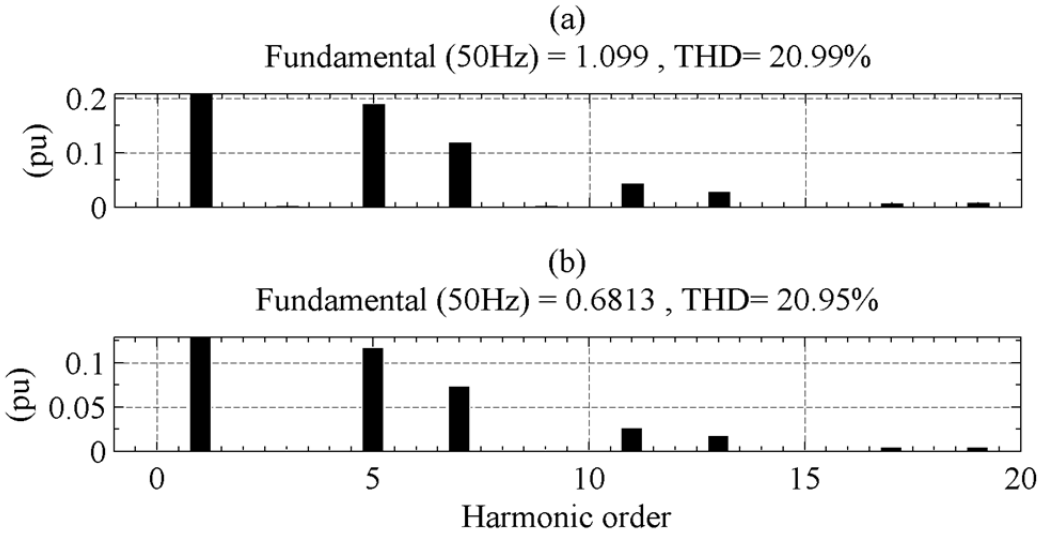

Fig. 3–14. Harmonic spectra at 1-pu active power (a) i_{lYa} and (b) i_{sYa}.

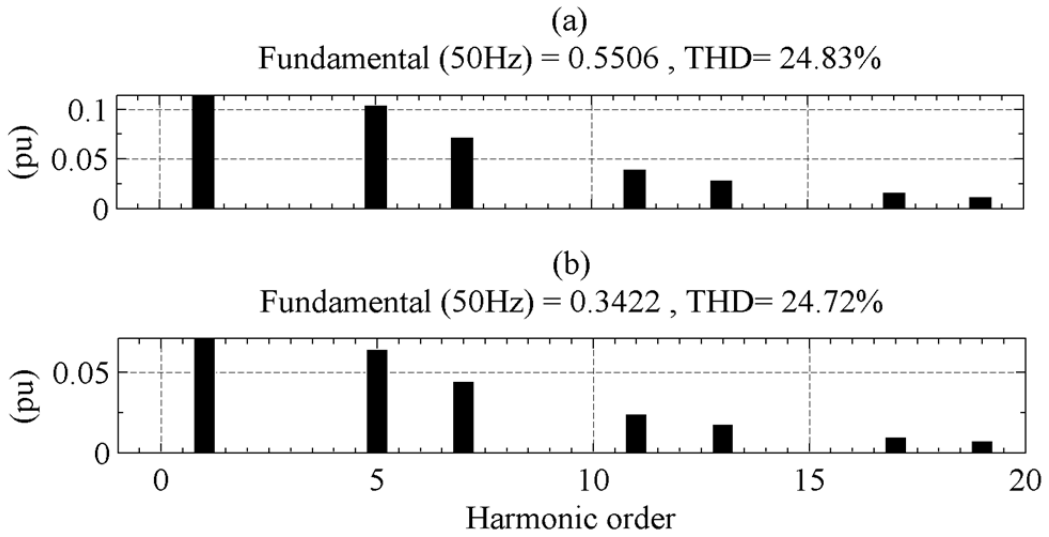

Fig. 3–15. Harmoinc spectra at 0.5-pu active power (a) i_{lYa} and (b) i_{sYa}.

TABLE 3–2
Important Harmonic Figures in The *Y* Branch

	P_s (pu)	Parameter	Value	
			SPF	CCC
i_{lYa}	1	THD (%)	20.56	20.99
		5^{th} (pu)	0.1882	0.1898
		7^{th} (pu)	0.1117	0.1188
		11^{th} (pu)	0.0388	0.0432
		13^{th} (pu)	0.0229	0.0282
	0.5	THD (%)	24.74	24.83
		5^{th} (pu)	0.1043	0.1038
		7^{th} (pu)	0.0697	0.0715
		11^{th} (pu)	0.0382	0.0391
		13^{th} (pu)	0.0264	0.0284
i_{sYa}	1	THD (%)	20.50	20.95
		5^{th} (pu)	0.1164	0.1174
		7^{th} (pu)	0.0691	0.0735
		11^{th} (pu)	0.0240	0.0267
		13^{th} (pu)	0.0142	0.0174
	0.5	THD (%)	24.61	24.72
		5^{th} (pu)	0.0646	0.0642
		7^{th} (pu)	0.0431	0.0442
		11^{th} (pu)	0.0237	0.0242
		13^{th} (pu)	0.0164	0.0175

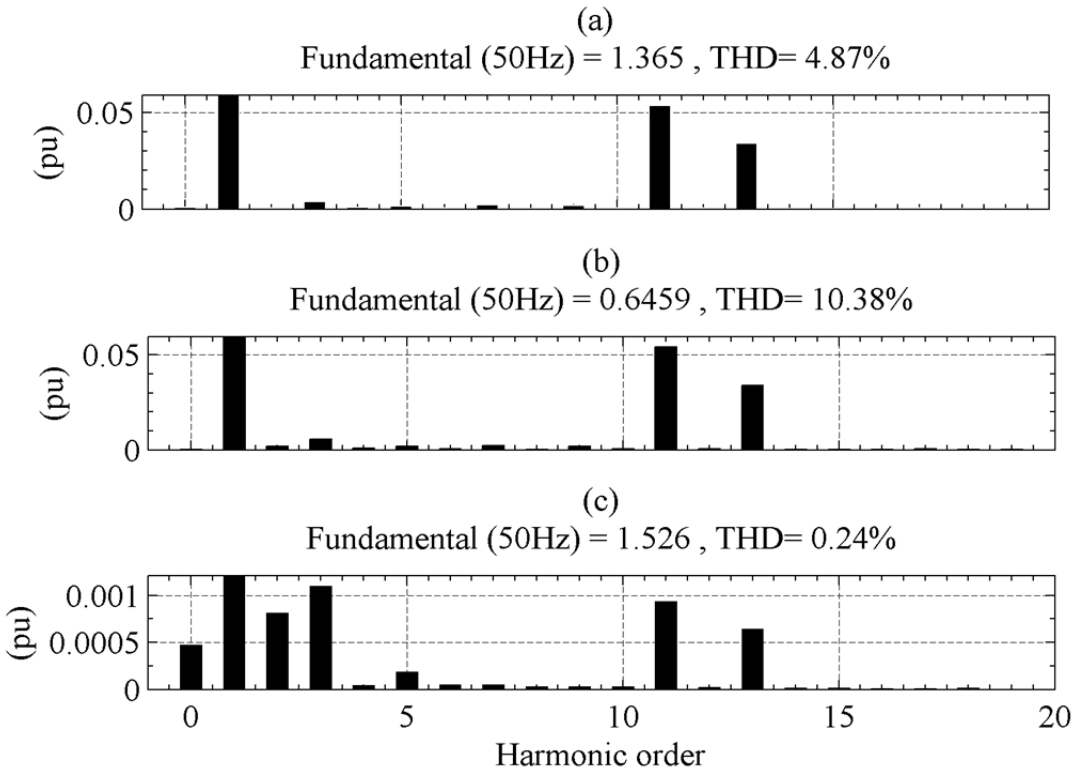

Fig. 3–16. Harmonic spectra at 1-pu active power (a) i_{sa}, (b) i_{fa}, and (c) i_{ga}.

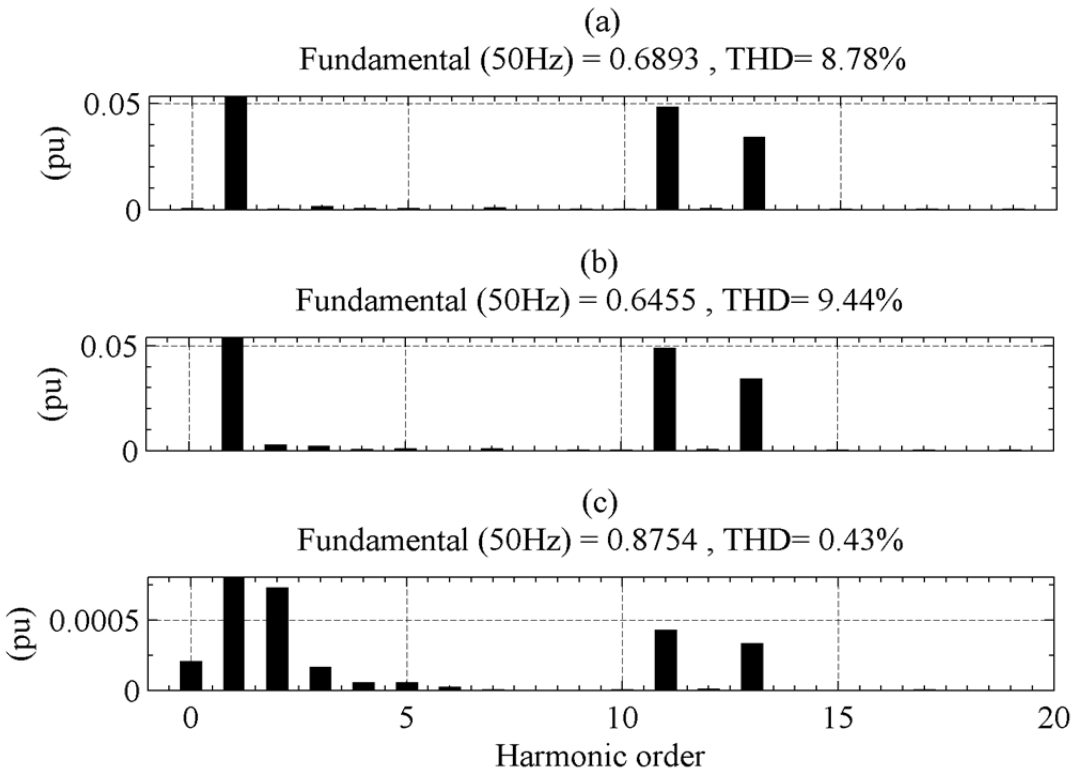

Fig. 3–17. Harmonic spectra at 0.5 pu active power (a) i_{sa}, (b) i_{fa}, and (c) i_{ga}.

TABLE 3–3
Important Harmonic Figures in the Combined Terminal Current

	P_s (pu)	Parameter	Value	
			SPF	CCC
i_{sa}	1	THD (%)	4.31	4.87
		5^{th} (pu)	0.0027	0.0015
		7^{th} (pu)	0.0027	0.0021
		11^{th} (pu)	0.0470	0.0539
		13^{th} (pu)	0.0293	0.0340
	0.5	THD (%)	8.51	8.78
		5^{th} (pu)	0.0017	0.0008
		7^{th} (pu)	0.0015	0.0010
		11^{th} (pu)	0.0468	0.0487
		13^{th} (pu)	0.0334	0.0345

3.3.5 Instantaneous Power

The instantaneous powers at different points in the system for CCC HVDC are plotted in Fig. 3–18. Panel (a) and (b) in this case are the same as those in Fig. 2–21 (a) and (b). However, due to the inclusion of the series capacitors, the waveforms of p_{sD}, p_{sY}, and p_s shown in Fig. 3–18 (c) differ from those in Fig. 2–21 (c). The oscillations in these powers have reduced even though the harmonics in i_{sD} and i_{sY} are somewhat higher in CCC HVDC than in conventional HVDC as can be seen from comparison of Fig. 3–12(b) and Fig. 3–14(b) with Fig. 2–15 (b) and Fig. 2–17 (b). This is a verification of the fact that the oscillation amplitudes in instantaneous power are not always proportional to the harmonic currents in the system. The same plots are regenerated in Fig. 3–19, when the active-power flow is reduced to 0.5 pu. Similar arguments hold true as in the case of 1 pu active-power flow.

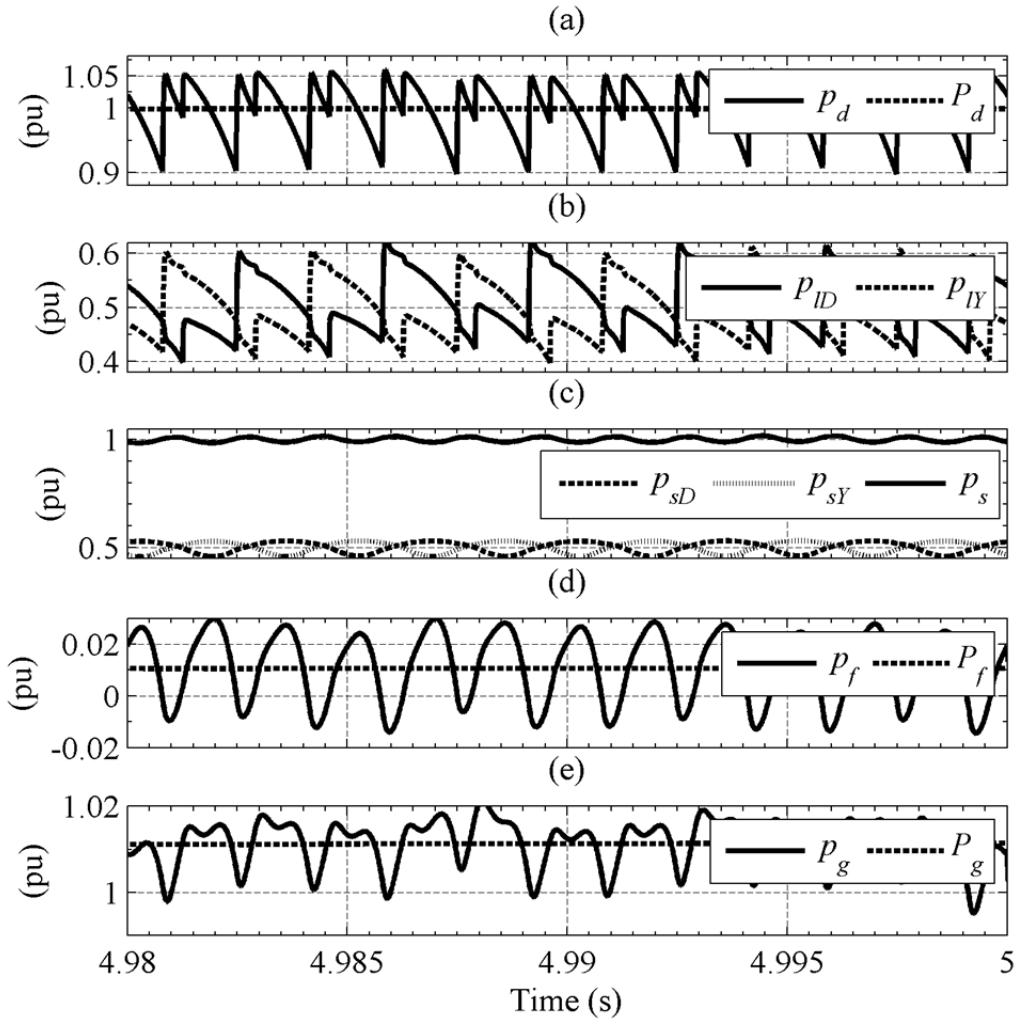

Fig. 3–18. Instantaneous powers at 1-pu active power.

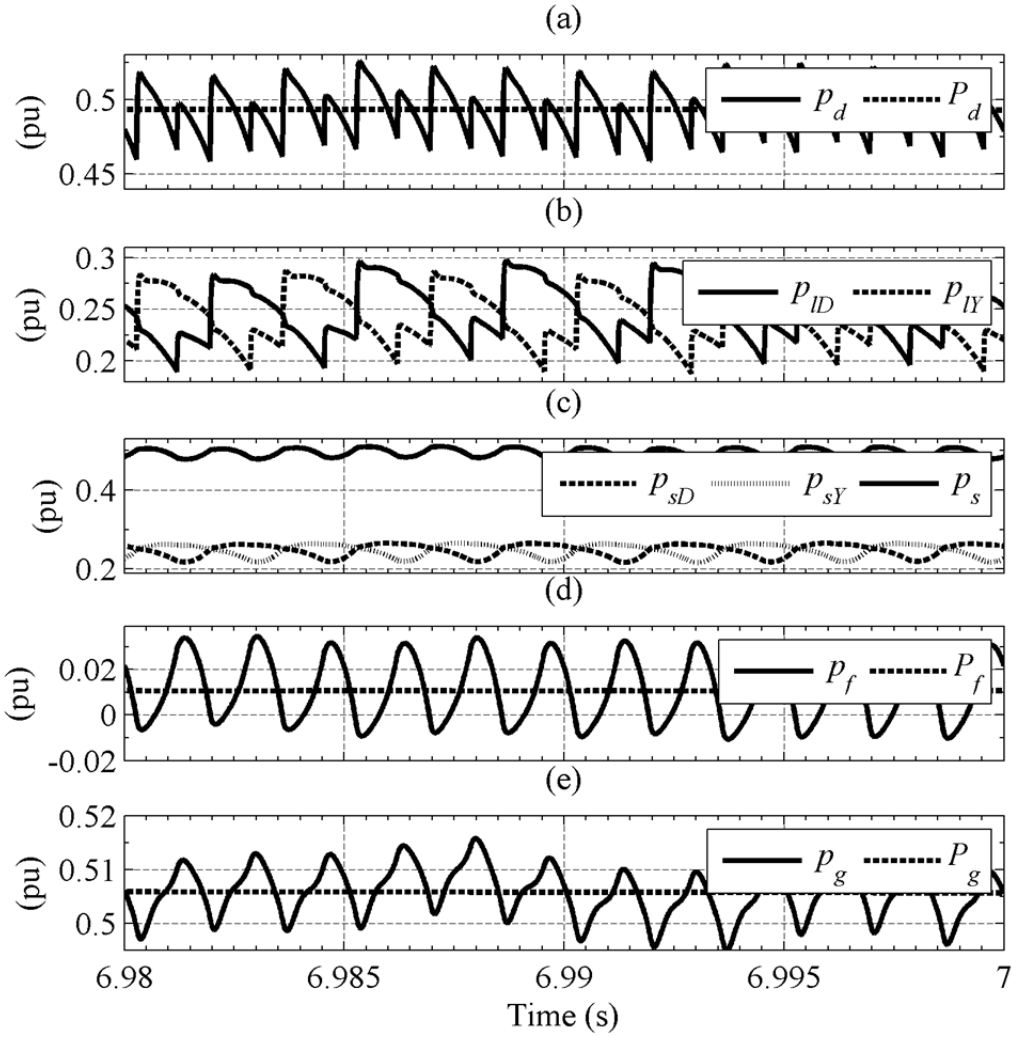

Fig. 3–19. Instantaneous powers at 0.5-pu active power.

3.4 Conclusion

Simulations for CCC HVDC systems have been presented in this chapter. It has been found that the total series capacitance required for full reactive compensation is 510 μF, which is much higher than the capacitor requirement in the combined reactive and harmonic scheme connected in shunt in the conventional system (273 μF). This is why the series capacitors in commercial CCC HVDC projects are sized for partial reactive compensation with the rest of reactive compensation provided by the shunt-filter and capacitors which act as reactive-power sources at fundamental frequency.

The main benefit of the scheme is the reduction/elimination of reactive-power flow through the converter transformers allowing a reduction in their MVA rating and, therefore, reduction in their size.

The reactive-power contribution of CCC HVDC varies with load which is beneficial because it reduces switching as opposed to the conventional arrangement. But

it was seen that the variability in the reactive-power output does not follow the variation in reactive-power demand and thus some switching is inevitable.

It has been observed that the harmonic content in the AC currents increase with the introduction of series capacitors. As with the case of conventional HVDC, at reduced active-power flow, the THD figures in the AC currents go up.

Series capacitors, being series devices, need fast protection schemes to avoid damage due to excessive fault currents. In addition, they also need common-mode voltage insulation for both terminals.

4 The Gate Commutated Series Capacitor Compensated HVDC

This chapter presents a series-compensator specifically designed for line-commutated HVDC based on the gate-commutated series capacitor. Simulation results showing the capability of the compensator to provide full reactive-power control with changing active power is demonstrated. The harmonic behaviour is compared with the state-of-the-art topologies.

It was observed in chapter 3 that CCC HVDC needs large capacitors to compensate for the entire reactive-power demand of the terminal. In this chapter, an alternative compensator for use in the same location as that of the fixed series capacitors is proposed. This is known as the Gate-Commutated Series Capacitor [78, 79, 99], which has not been employed for this application before. The major difference is the remarkable reduction in the size of the required capacitors. The total series capacitance used with GCSC is 60 μF as against 510 μF in the CCC HVDC case.

4.1 Construction of GCSC

The GCSC is a compensation arrangement with a capacitor connected in parallel with a pair of antiparallel-connected Gate-Turnoff Thyristors (GTO) in each phase. The control of the voltage across the capacitor is achieved by turning on the GTOs when the voltage across the capacitor is zero. This bypass duration can be controlled by controlling the duration of gate pulses to the GTOs. This way, the GCSC injects variable series voltages in the positive and negative half-cycles of the current. The construction of one leg of a GCSC is shown in Fig. 4–1.

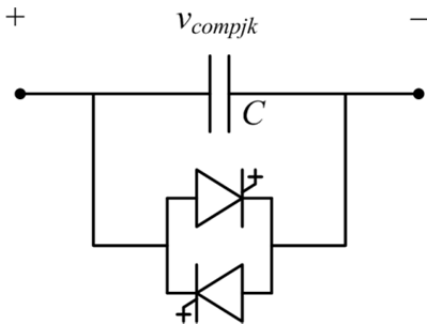

Fig. 4–1. Schematic arrangement of the GCSC.

4.2 Proposed Arrangement with the GCSC

The proposed compensation arrangement is the same as in Fig. 3–1. However, the fixed series capacitors would be replaced with the compensator in Fig. 4–1.

4.3 Switching Strategy with the GCSC

The concerned pair of thyristors will be switched on using the algorithm given in Fig. 4–2. If the phase of the concerned current is between 0 and the bypass duration angle (θ_{compjR}), and the compensator voltage hits 0, a flip-flop will be set. The flip-flop would be reset, once the condition above is no longer satisfied. The same would happen in the negative half-cycle of the current when the current phase should fall between π and $\theta_{compR} + \pi$ to set the second flip-flop. The output of the two flip-flops is ORed to produce the gate pulse (G_{jk}). This pulse would be provided to both the GTOs in a specific phase leg.

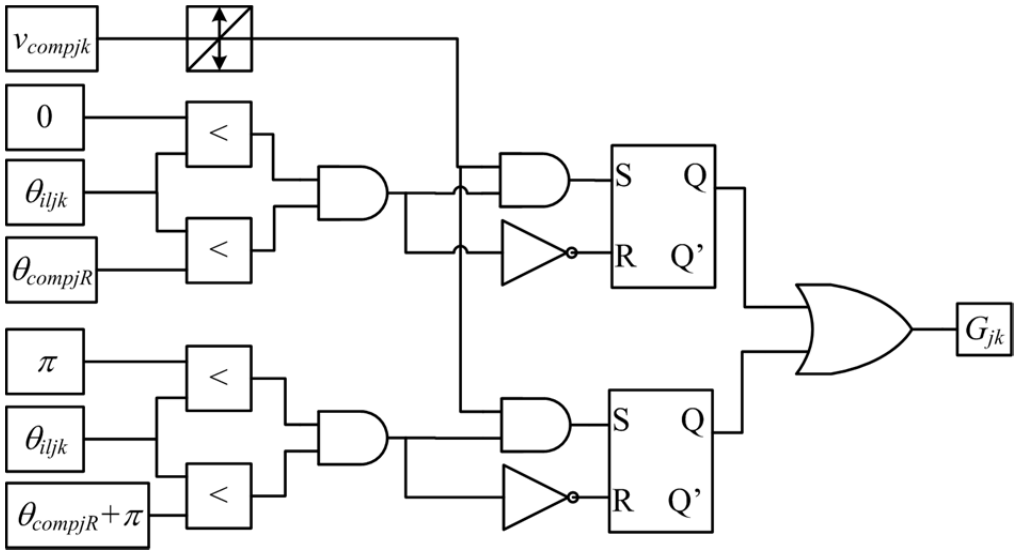

Fig. 4–2. Algorithm for Generation of Gate pulse for the GCSC in branch *j* and phase *k*.

It should be noted that the phase-angle information of all the currents can be collected by the phase information of just one of the currents and the rest can be computed by the controller. It has to be said that this algorithm can be designed in a manner in which separate gate pulses can be provided to the two GTOs in antiparallel, based on the direction of current. This could be helpful in reducing the switching losses.

4.4 The Commutation Process

The commutation circuit is shown in Fig. 4–3. It is similar to the CCC HVDC circuit except the fact that the series capacitance is not fixed and is a function of the blocking angle γ_{compj}. If the blocking duration is large, the capacitor is not in the circuit for a

longer time and the effective injected voltage is small; leading to an effect of a lower reactance and higher capacitance. On the contrary, if the blocking duration becomes smaller and tends to zero, the capacitor is connected for a longer time and its original smaller value is exposed more and more to the circuit. At smaller γ_{compj} values, the GCSC is able to inject higher voltages for lower currents. The discussion and equations (given in (3.1) to (3.4) for CCC HVDC) hold true for GCSC as well. The difference is the controllability of the series capacitance which is responsible for effective reactive-power control. For a thorough treatment, the reader is referred to [100].

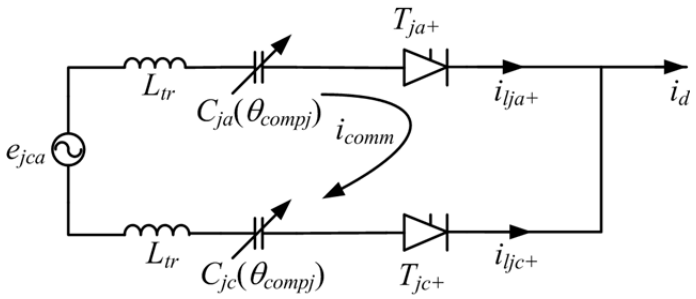

Fig. 4–3. Commutation circuit for GCSC HVDC.

4.5 Simulation Setup

The setup for simulations is the same as in the preceding chapters. The control loops used for the generation of firing pulses for the main AC/DC converter (Fig. 3–2) and for keeping α constant (Fig. 2–6) are used. However, the generation of θ_{compjR} had to be added for use in the control algorithm in Fig. 4–2.

The need is to control the reactive-power flow as directed by a reference command. Therefore, a control loop is required which should compare a reference value for reactive power into the converter terminal to the actual flow in order to control the magnitude and instant of voltage injected by the GCSC. The output of this control loop should, therefore, be θ_{compjR}. The control loop is depicted in Fig. 4–4. The reference reactive power that should flow into the two converter transformers is divided by 2 and subtracted from the actual reactive-power flow into each transformer. The error signals are processed by *PI* controllers and the outputs form the reference bypass durations for the GCSC compensators in the *D* and *Y* branches.

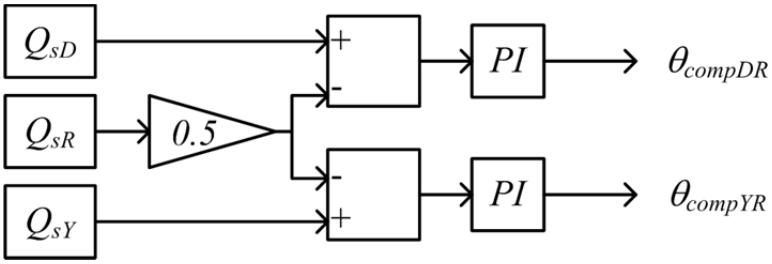

Fig. 4–4. Control loop for generation of θ_{compjR}.

4.5.1 Case I: Changing Active-Power and Constant Reactive-Power Reference

The simulation starts with P_s = 1 pu, Q_{sR} = 0 pu, and the GCSC bypassed. The GCSC is connected at 3 s and the behaviour of the system is observed. P_s is stepped down to 0.5 pu at 5 s and the simulation runs for another 2 s allowing time for the system to settle to steady-state again.

4.5.2 Case II: Constant Active-Power and Changing Reactive-Power Reference

P_s is held at 1 pu throughout this case. Q_{sR} is set to 0 pu at the beginning and the GCSC is connected at 3 s. Q_{sR} is set to 0.3 pu at 5 s and the simulation runs for another 2 seconds to allow the system to settle to steady-state.

4.6 Simulation Results for Case I

4.6.1 Active and Reactive Powers

The active and reactive powers at different points in the system are plotted in Fig. 4–5. As the GCSC is connected (at 3 s), Q_s drops to 0 pu (panel (a)). Q_f , generated by the shunt filter is exported to the grid as can be observed in the trace for Q_g. The reason is that Q_{compD} (panel (b)) and Q_{compY} (panel (c)) act in such a manner such that Q_{sD} and Q_{sY} are both neutralized. As P_s goes down to 0.5 pu at 5 s, the compensator adjusts itself to keep Q_{sD} and Q_{sY} at 0 pu, so that Q_s, remains at 0 pu. The difference with the CCC-HVDC topology is that the GCSC arrangement fully compensates for the reactive power even when the active-power flow is changing; whereas the former did not as can be seen in Fig. 3–4.

4.6.2 Control Loop operation

The outputs of the control loops in Fig. 3–2, Fig. 2–6, and Fig. 4–4 are shown in Fig. 4–6 (a), (b), and (c) respectively. The active-power control loop and the AC-voltage control loop act satisfactorily to keep α constant (panel (a) and (b)). The behaviour of the control loop in Fig. 4–4 is interesting to analyse. The value of θ_{compjR} is around 2.14 radians when P_s = 1 pu. As P_s is reduced to 0.5 pu at 5 s, the value of θ_{compjR} goes down to allow more time for the capacitors to conduct and build up their voltage to a level which would allow full reactive-power compensation.

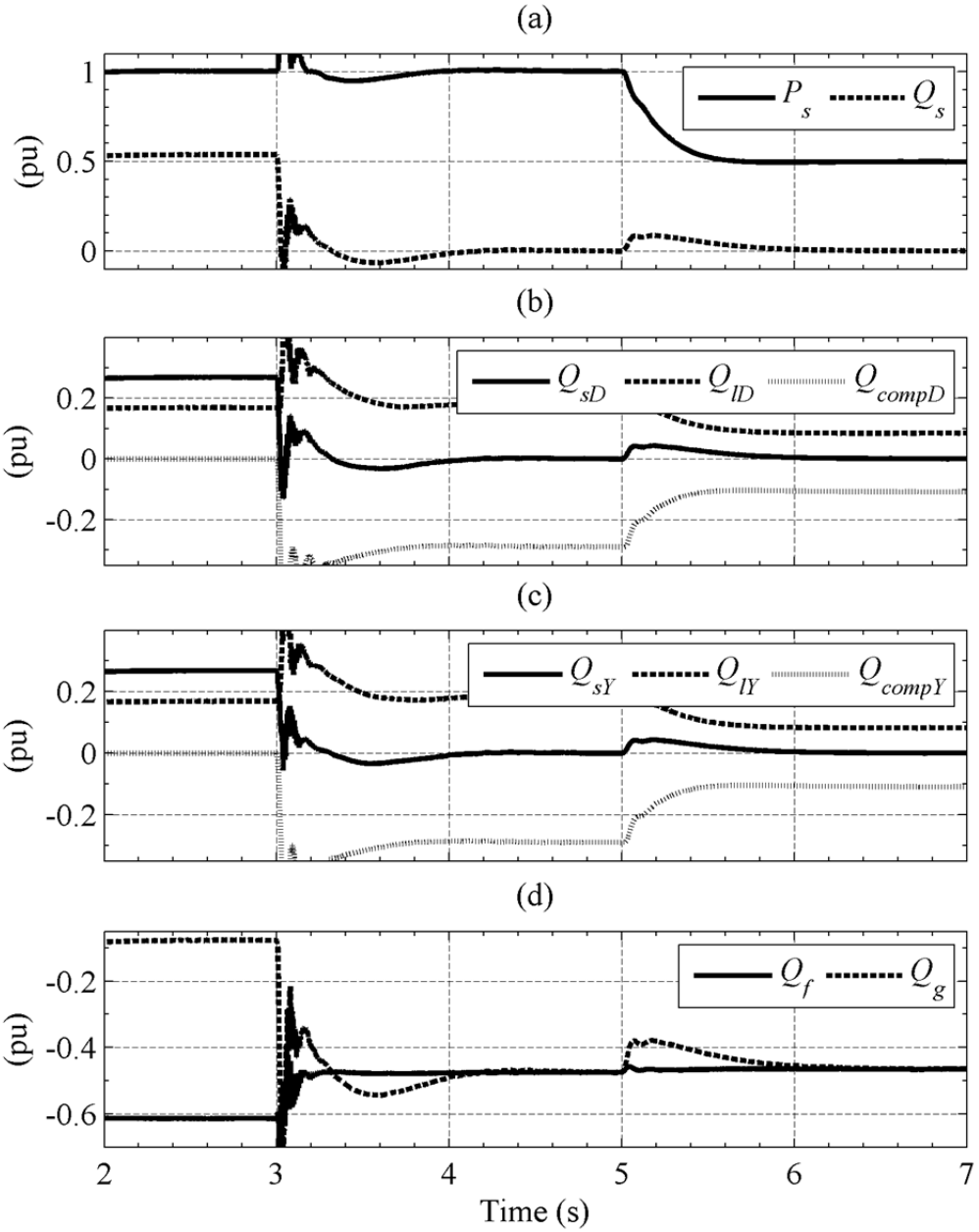

Fig. 4–5. Active and reactive powers for case I.

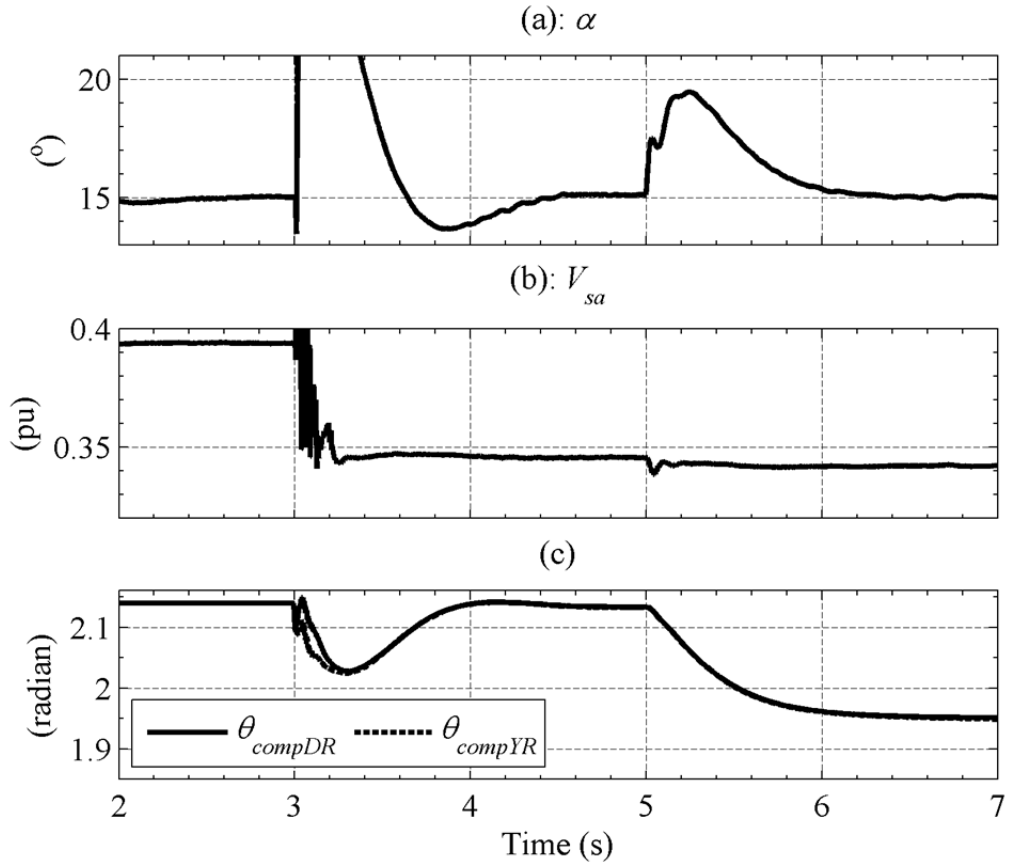

Fig. 4–6. Operation of the control loops for case I.

4.6.3 Instantaneous Currents and Voltages

The instantaneous currents and voltages on the converter side in the *D* branch are shown in Fig. 4–7. The current commutations for phase *c* to phase *a* along with the voltages of interest are plotted only. Similar plots can be made for the rest of the commutations from phase *a* to *b* and from phase *b* to *c*. The currents and voltages follow the same pattern with the compensator bypassed as in the preceding chapters (panel (a)). The important observations to make are the rates of change of currents during commutations, and the instantaneous value of the commutation voltage available at the instant of firing of the incoming thyristor.

When the GCSC is connected and P_s = 1 pu, the voltages injected by the compensator in the incoming phase are at their peak. As the injected voltages hit zero in the positive or negative half-cycle of the current, the thyristors in the respective GCSC are fired to bypass the capacitor. This delays the charging of the capacitor in the opposite polarity until the thyristors are switched off again to let the current flow through the GCSC capacitor to charge it with the opposite polarity.

Secondly, the converter terminal voltages cross earlier under the influence of the voltage already available on the GCSC in the incoming phase (phase *a* in this case), and also because of the increasing voltage on the GCSC in the outgoing phase (phase *c*

in this case). This can be observed in panel (b) where the rate of change of v_{lDlca} is higher than that in the uncompensated case. Due to this, commutation occurs at a higher voltage with the GCSC than without it. This influences the commutation angle u in such a way that it is reduced. This is evident from the elevated rates of change of currents in panel (b), which implies the existence of higher harmonic content. This behaviour is similar to CCC HVDC as discussed in chapter 3. It will be seen later that the harmonic performance is even worse with the GCSC as compared to CCC HVDC.

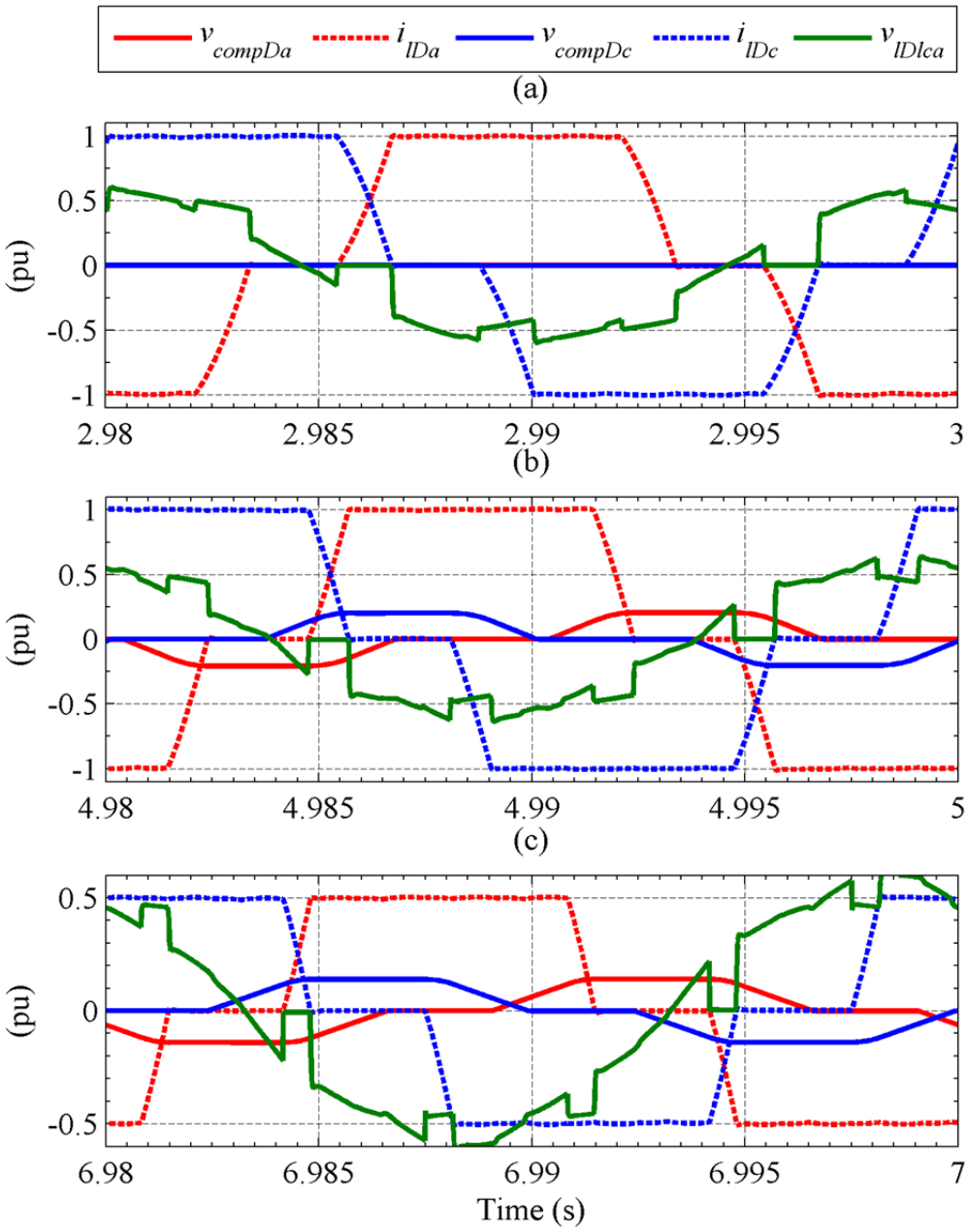

Fig. 4–7. Instantaneous converter-side currents and voltages in the *D* branch for case I.

Another important observation to be made is the waveform of the injected voltages, which are essentially the voltages across the GCSC capacitor when it is not

blocked. These voltages are AC in nature and, therefore the capacitors have to be non-polarized leading to larger-volume capacitors; similar to the conventional shunt arrangement.

The peak-to-peak voltage injected by the GCSC is over 0.4 pu for P_s = 1 pu (Fig. 4–7 (b)). When P_s is stepped down to 0.5 pu, the slope of the commutating voltage at reversal is higher and hence, the rate of change of current is also larger. This is similar to the case of the uncompensated system discussed in chapter 2, however, the commutation angle is even shorter. This means that the GCSC is behaving as a variable capacitor in this system. The downside of this behaviour is increased harmonic content in the AC system and consequently, higher demands on the harmonic filters. The benefit is the total capacitance employed (60 μF), far less than what was used in chapter 3 (510 μF).

The grid side currents for P_s = 1 pu are plotted in Fig. 4–8. The fundamental components of the currents in panels (a), (b), and (c) are in phase with the phase voltage. The harmonic content in i_{sa} (panel (c)) is higher than that in the conventional system and with the CCC-HVDC topology. The shunt filter current in panel (d) shows a high harmonic content.

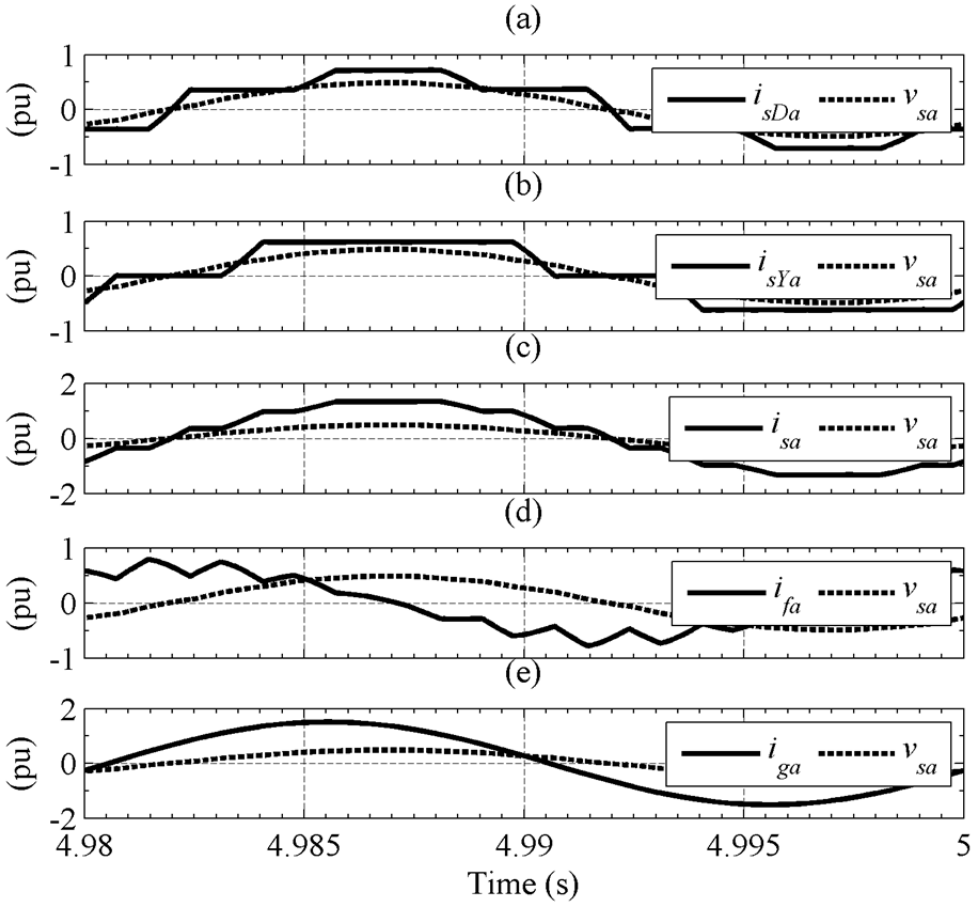

Fig. 4–8. Instantaneous currents and voltages in phase *a* on the grid side with P_s = 1 pu.

The same currents are plotted in Fig. 4–9 for P_s = 0.5 pu. These plots show that the GCSC is performing satisfactorily for full reactive-power compensation. The zero phase difference between i_{sa} and v_{sa} (panel (c)) is a proof of the fact.

The voltages which the GCSC switches have to block are the same which are injected by it (Fig. 4–7 (b) and (c) respectively for P_s = 1 pu and P_s = 0.5 pu). The voltages appearing across single thyristors in the main AC/DC conversion bridges are shown in Fig. 4–10 and are quite similar to those observed with the topologies discussed in the preceding chapters in terms of peak voltage appearing across the thyristor. The rate of change of voltage is, however, larger as compared to the conventional shunt-compensated arrangement.

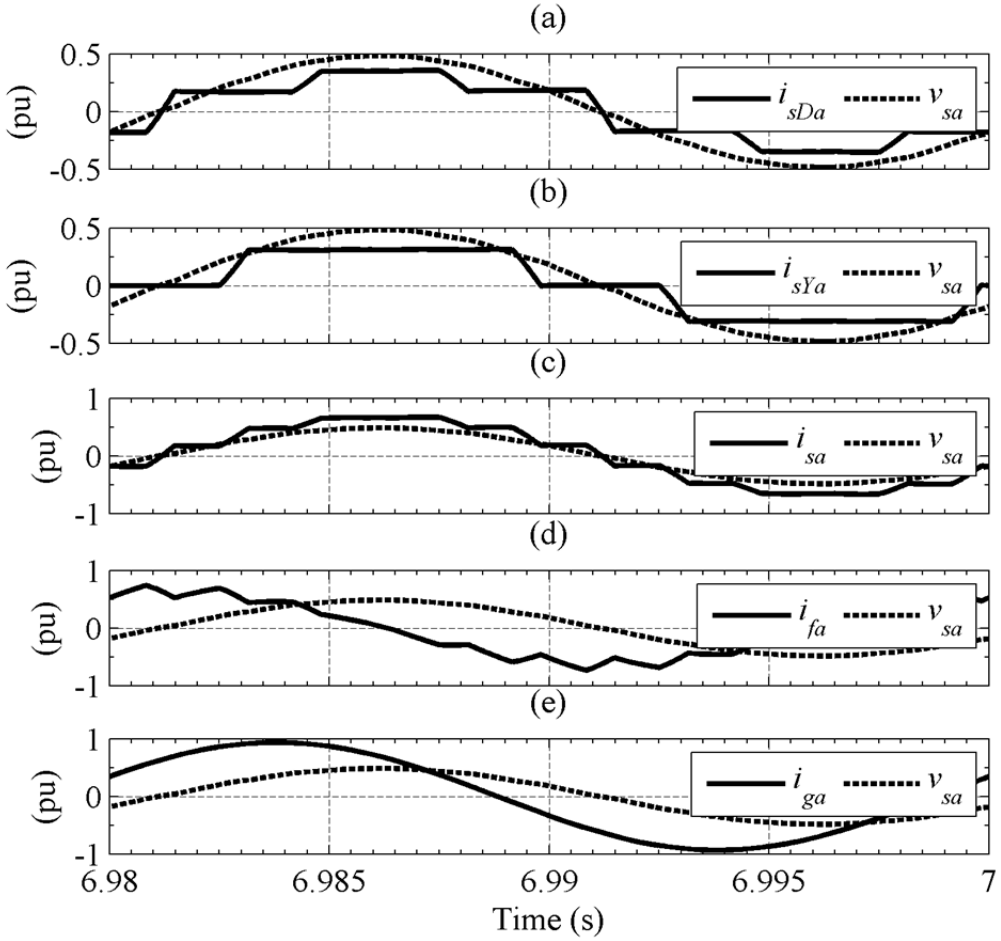

Fig. 4–9. Instantaneous currents and voltages in phase *a* on the grid side with P_s = 0.5 pu.

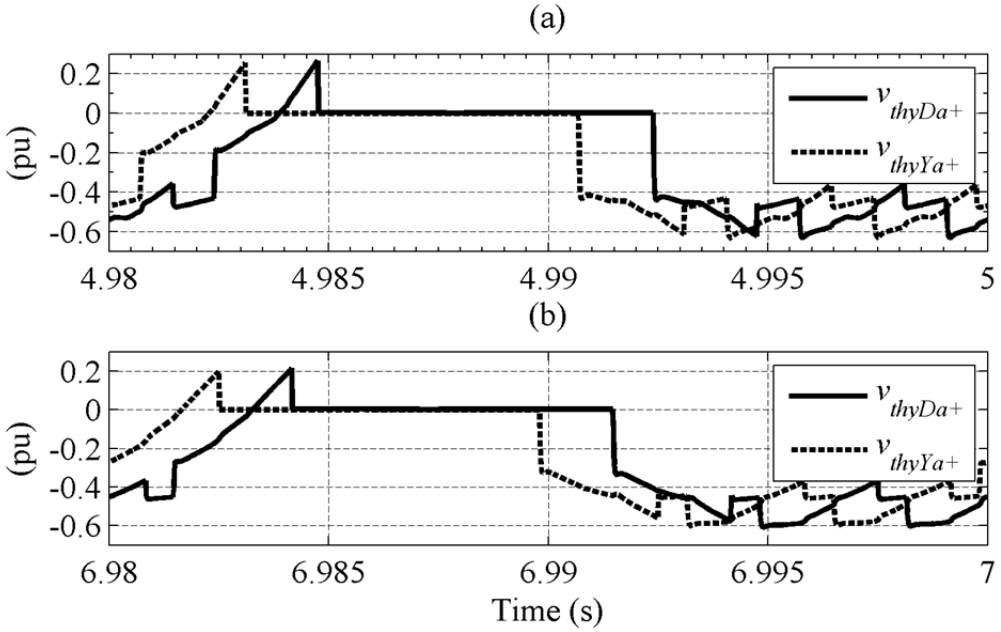

Fig. 4–10. Instantaneous voltages appearing across one thyristor in the main AC/DC conversion bridge when (a) P_s = 1 pu, and (a) P_s = 0.5 pu.

4.6.4 Current Harmonics

The harmonic spectra of i_{lDa} and i_{sDa} are given in Fig. 4–11 (a) and (b) respectively. Comparison with the similar case in the uncompensated system in Fig. 2–15 shows that the current THD has increased by 2% on both sides of the converter transformers. The current harmonics for P_s = 0.5 pu are given in Fig. 4–12. The THD figures are higher than the conventional shunt-compensated system reported in Fig. 2–16. They are also slightly higher than the corresponding figures for CCC HVDC (Fig. 3–13).

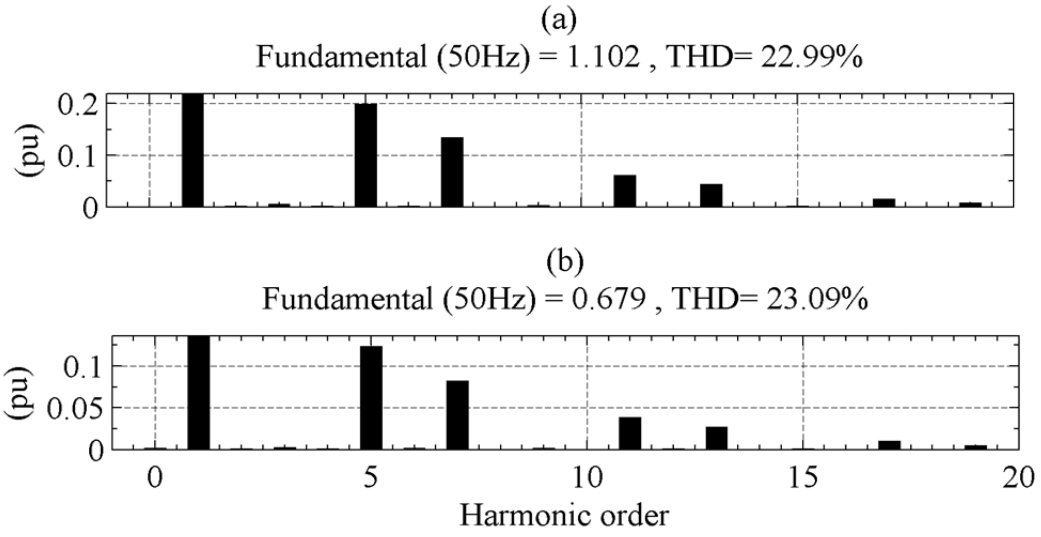

Fig. 4–11. Harmonic spectra for case I with P_s = 1 pu. (a) i_{lDa}, and (b) i_{sDa}.

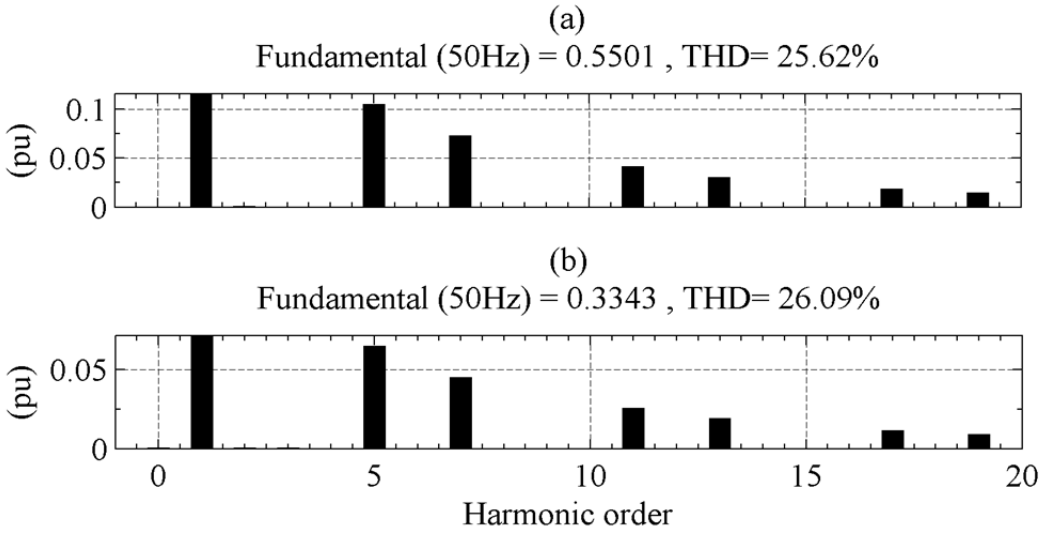

Fig. 4–12. Harmonic spectra for case I with P_s = 0.5 pu. (a) i_{lDa}, and (b) i_{sDa}.

The harmonic analyses of the *Y*-branch current (i_{lYa} and i_{sYa}) for P_s = 1 pu and P_s = 0.5 pu are presented in Fig. 4–13 and Fig. 4–14 respectively. These exhibit a harmonic pattern similar to what has been seen in the *D*-branch currents.

The harmonic contents of the currents i_{sa}, i_{fa}, and i_{ga} are depicted in Fig. 4–15 (a), (b), and (c) respectively. For comparison with other cases, THD in i_{sa} is 4.31% in Fig. 2–19 (conventional shunt), and 4.87% in Fig. 3–16 (CCC HVDC). Therefore, some of the advantage gained with the GCSC approach is offset by a larger-harmonic content to contend with. Similar observations can be made for the case with P_s = 0.5 pu, the harmonic for which are given in Fig. 4–16. The THD in i_{sa} increases as in similar situations in the preceding chapters and the shunt filter has to inject higher amount of harmonics to neutralize the same.

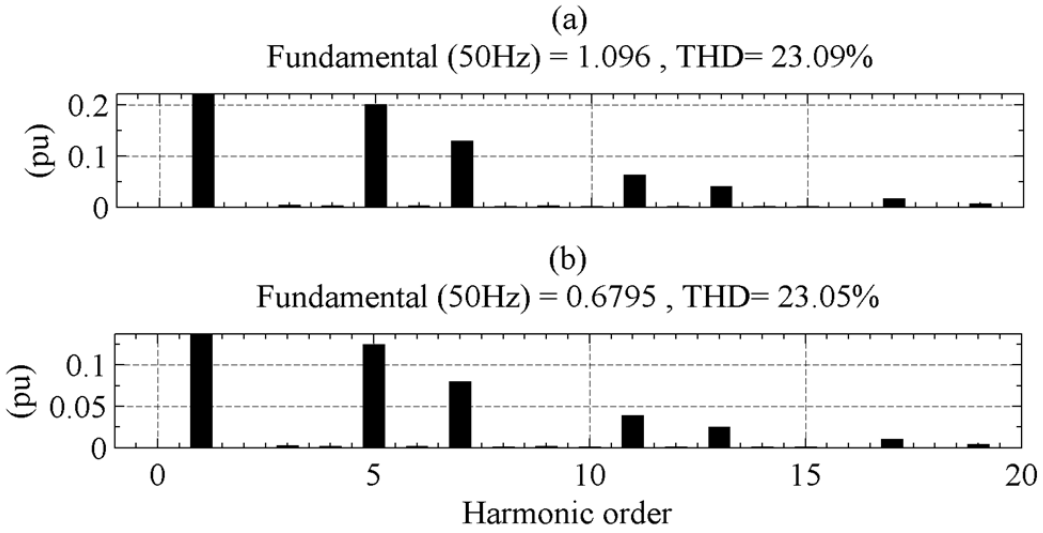

Fig. 4–13. Harmonic spectra for case I with P_s = 1 pu. (a) i_{lYa}, and (b) i_{sYa}.

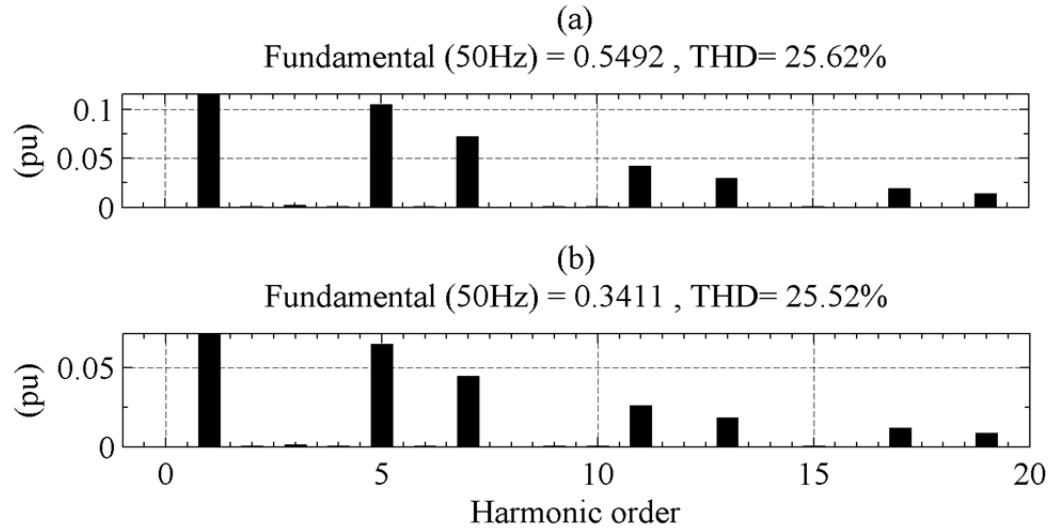

Fig. 4–14. Harmonic spectra for case I with P_s = 0.5 pu. (a) i_{lYa}, and (b) i_{sYa}.

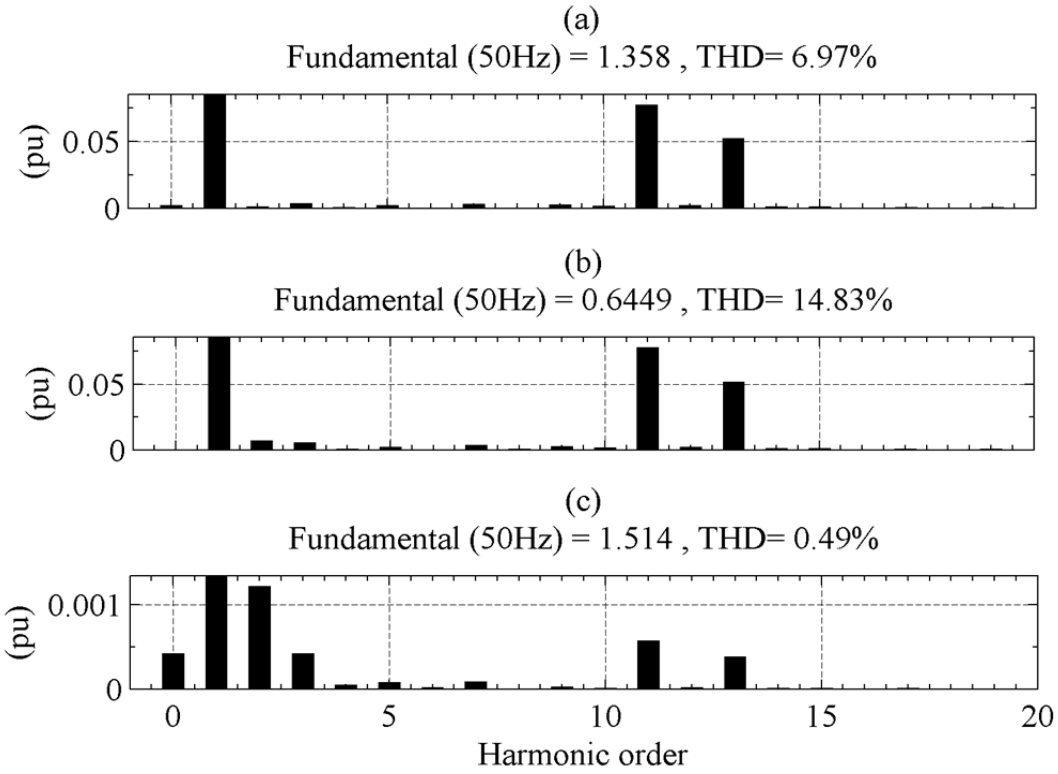

Fig. 4–15. Harmonic spectra for case I with P_s = 1 pu. (a) i_{sa}, (b) i_{fa}, and (b) i_{ga}.

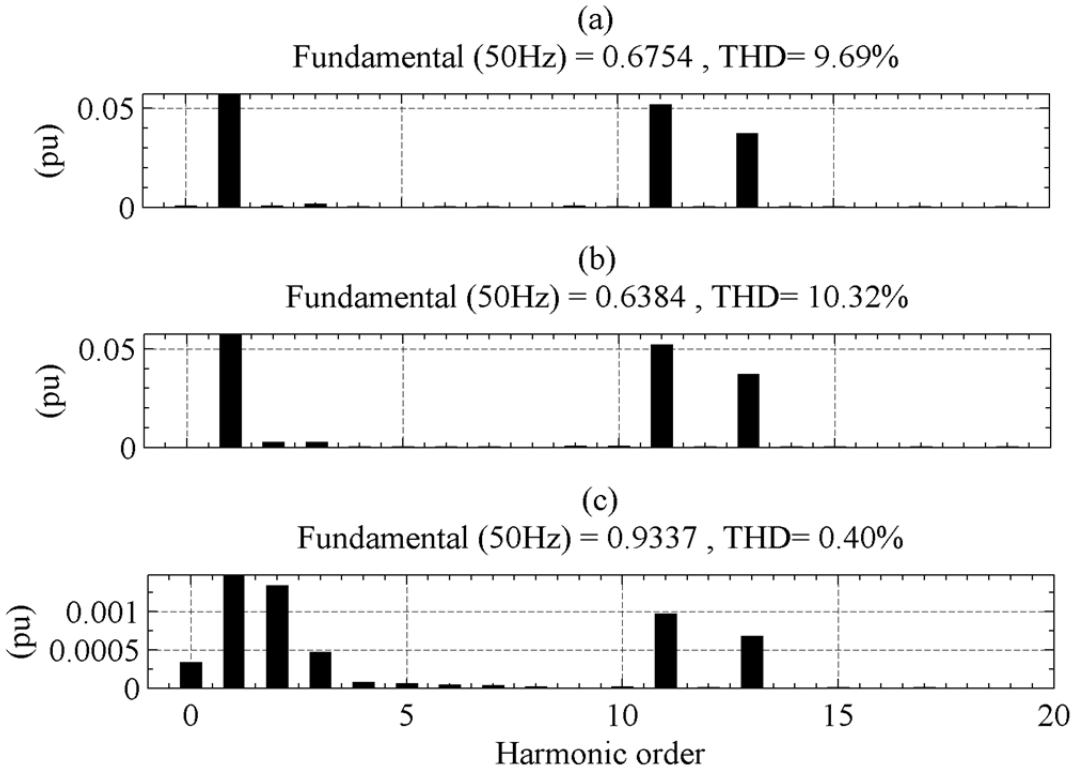

Fig. 4–16. Frequency spectra for case I with *Ps* = 0.5 pu. (a) i_{sa}, (b) i_{fa}, and (b) i_{ga}.

4.6.5 Instantaneous Powers

The instantaneous powers at different points in the system with P_s = 1 pu are depicted in Fig. 4–17. In comparison with the conventional shunt-compensated LCC HVDC (Fig. 2–21), the instantaneous DC-link power has smaller oscillation amplitude. However, the oscillations on the AC side are much higher, indicative of higher harmonic content in the currents. The instantaneous power picture of the system with P_s = 0.5 pu is shown in Fig. 4–18 and one can observe even higher oscillation magnitudes than with the 1-pu active-power case.

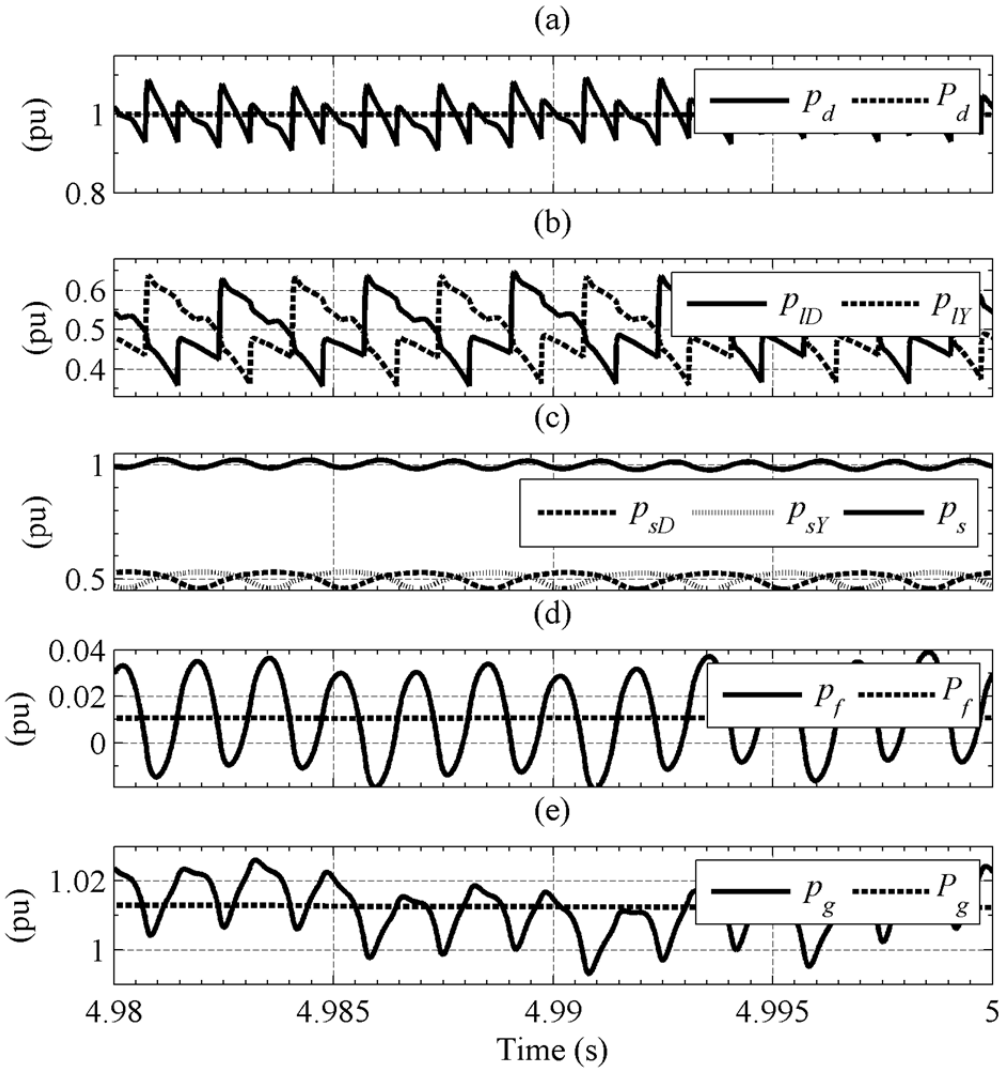

Fig. 4–17. Instantaneous powers at different locations in the system for case I with P_s = 1 pu.

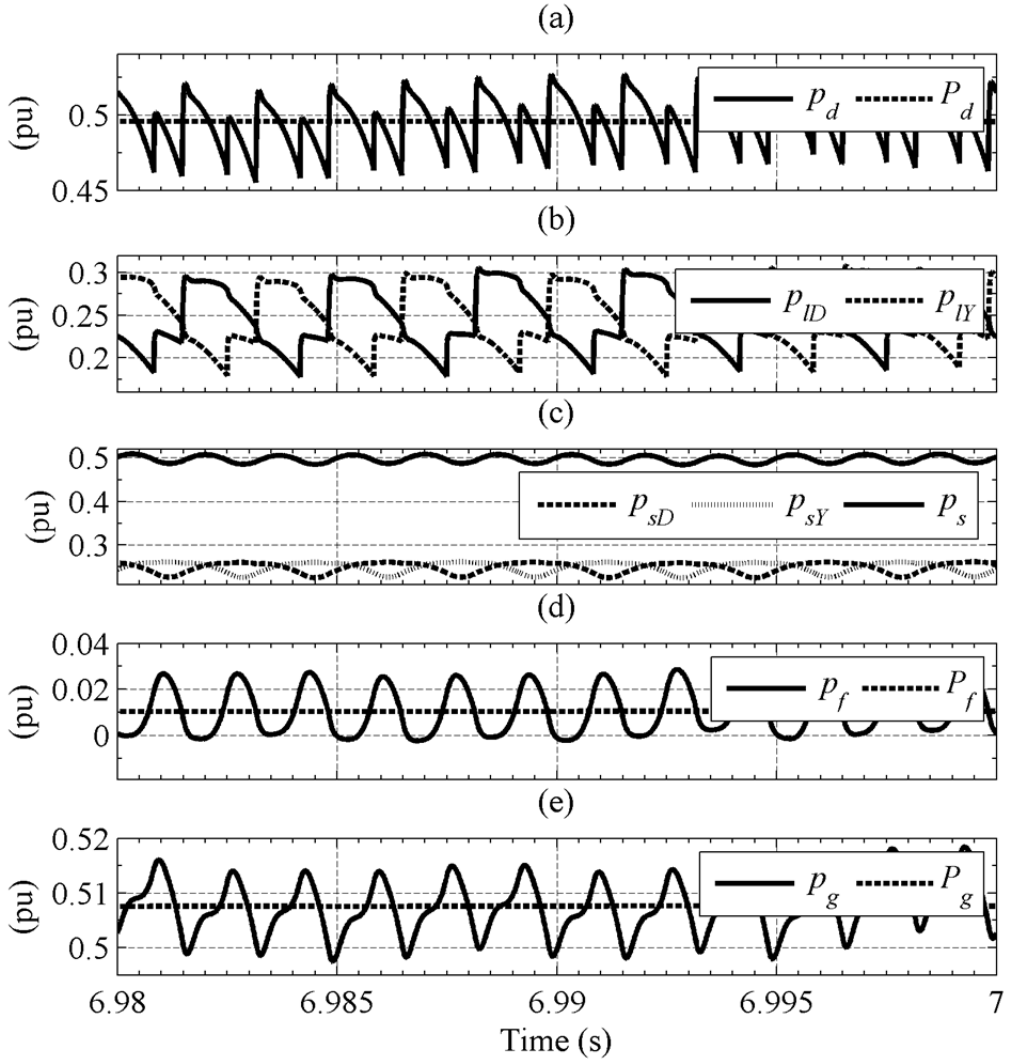

Fig. 4–18. Instantaneous powers at different locations in the system for case I with P_s = 0.5 pu.

4.7 Simulation Results for Case II

4.7.1 Active and Reactive Powers

The active and reactive powers at different locations in the system are plotted in Fig. 4–19. Before the GCSC is connected, the reactive-power demand is entirely compensated by the shunt passive filter. The transition to full reactive-power compensation by the GCSC is explained in the preceding section and does not need to be repeated here. At the transition of Q_{sR} to 0.3 pu from 0 pu at 5 s, the GCSC adjusts its output so that Q_{sD} and Q_{sY} both end up at 0.15 pu and, therefore, Q_s settles to 0.3 pu. More of the reactive power supplied by the shunt passive filter is now used up in to compensate for the non-zero Q_s. This is where the GCSC compensator shows superior performance as compared to CCC HVDC scheme.

4.7.2 Control Loop Operation

The operation of the control loops in this case is depicted in Fig. 4–20. At the transition to Q_{sR} = 0.3 pu at 5 s, the blocking duration for the GCSC switches increases so that the GCSC capacitor has to conduct the current for shorter period of time in a half-cycle. This results into a smaller voltage across the capacitors leading to partial reactive-power compensation by the GCSC.

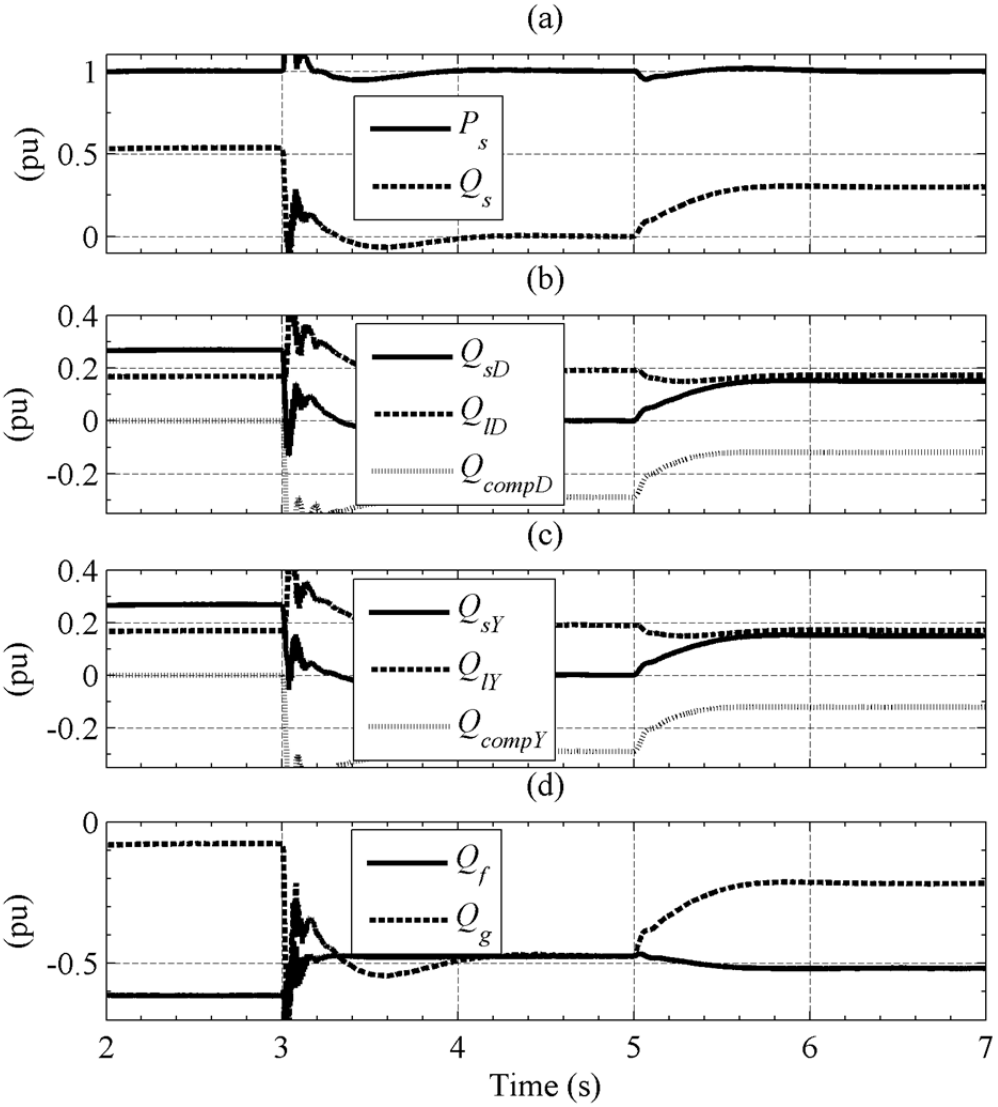

Fig. 4–19. Active and reactive powers for case II.

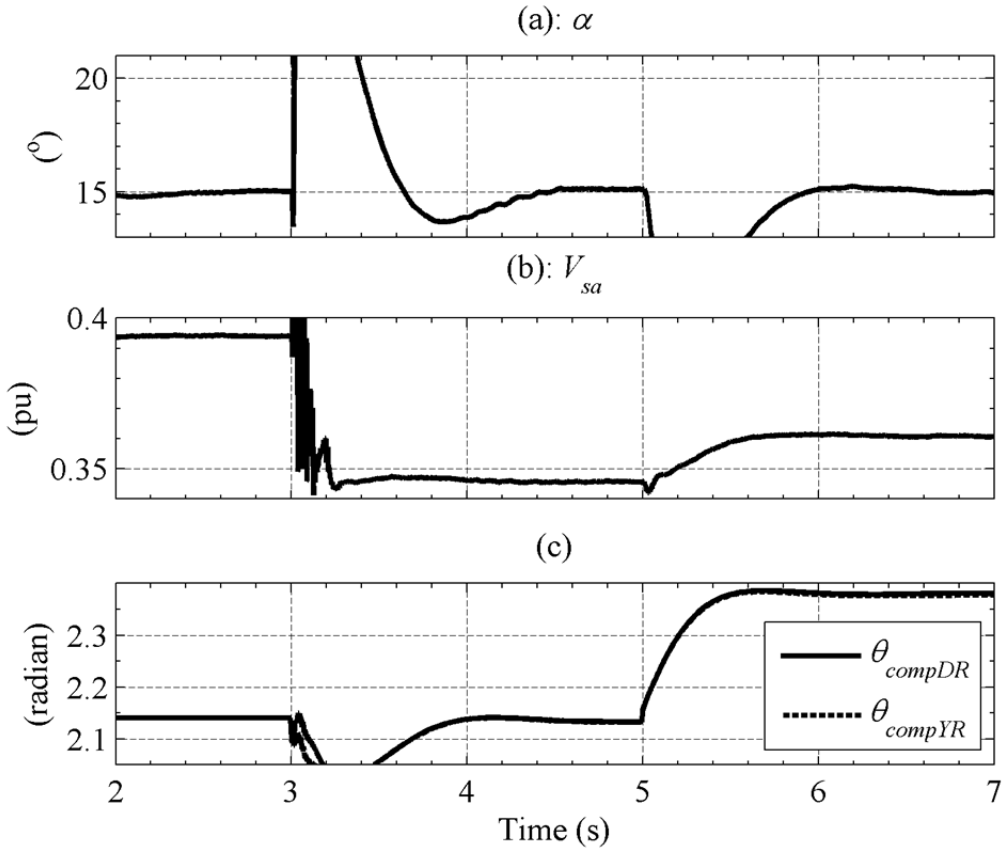

Fig. 4–20. Operation of the control loops for case II.

4.7.3 Instantaneous Currents and Voltages

The period with full compensation for P_s = 1 pu has been discussed in section 4.6.3. Here, we will discuss only the period with partial reactive-power compensation being provided by the GCSC. The instantaneous currents and voltages on the converter side for this period are plotted in Fig. 4–21. The currents and voltages involving the commutation of current from phase *c* to phase *a* in the positive and negative half-cycles in the *D* branch are plotted as a representative case. It can be seen that the injected-voltage magnitudes (v_{compDa} and v_{compDc}) have decreased because of the longer bypass period. For comparison, the reader is referred to Fig. 4–7 (b) for the period with full compensation. A consequence of this reduction in injected voltage is the comparatively smaller rate of change of current. A reduction in harmonic content is, therefore, predicted. This is because the GCSC is now behaving as a larger capacitor with lower reactance. This lower reactance cancels a smaller part of the inductive reactance in the path of currents.

The grid side currents and voltages in phase *a* are shown in Fig. 4–22. These plots are for the period with partial compensation only, as the interval with P_s = 1 pu and Q_{sR} = 0 pu has been discussed already in section 4.6.3. There is a distinct phase difference between the phase voltage and the current in panels (a), (b), and (c); which indicates the partial reactive-power compensation by the GCSC.

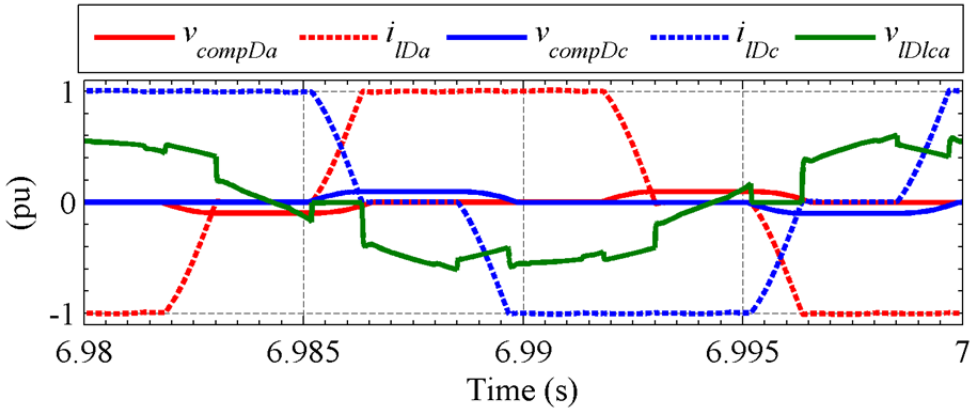

Fig. 4–21. Instantaneous converter-side currents and voltages in the *D* branch for case II for the interval with partial compensation.

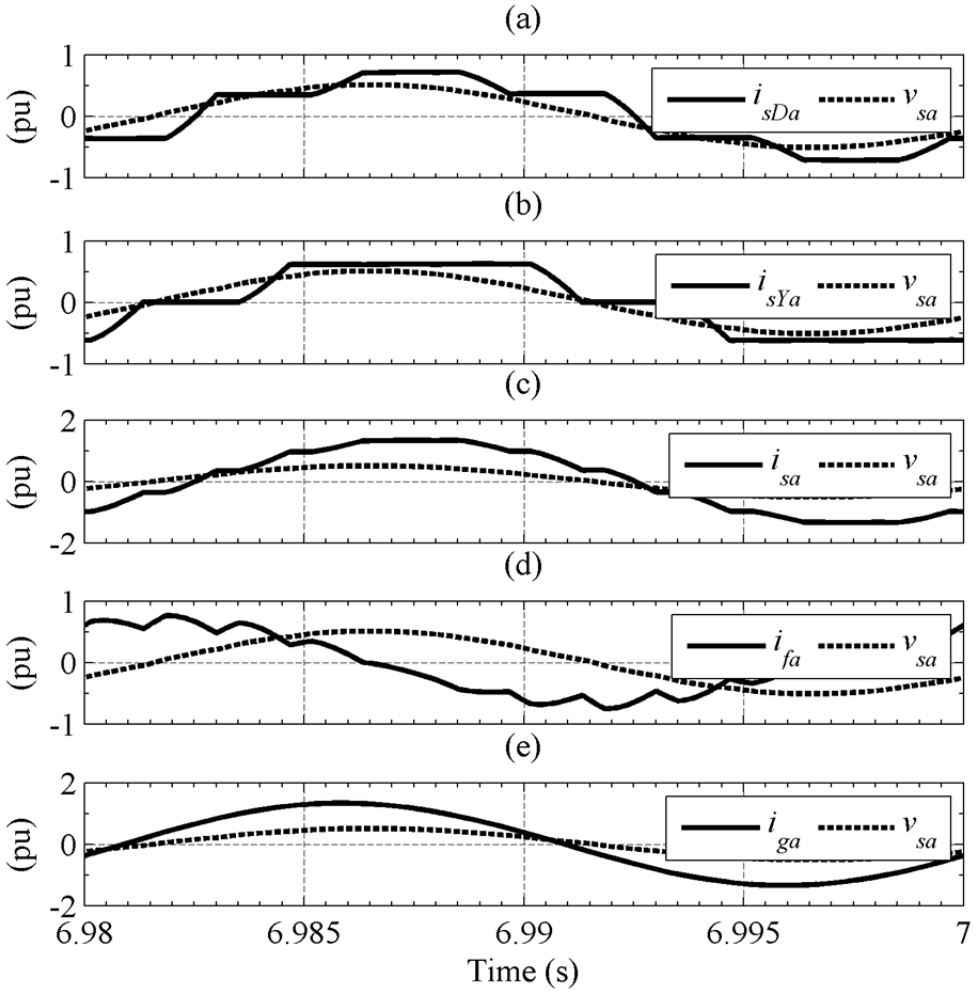

Fig. 4–22. Instantaneous currents and voltages in phase *a* on the grid side with Q_{sR} = 0.3 pu.

The voltages that have to be sustained by the GCSC switches in the period with partial compensation are the same which are injected by the GCSC and can be observed in Fig. 4–21. The voltages appearing across thyristors in the main AC/DC converter bridge when Q_{sR} = 0.3 pu are shown plotted in Fig. 4–23. Predictably, these are not very different from the case with Q_{sR} = 1 pu as observed in Fig. 4–10 (a).

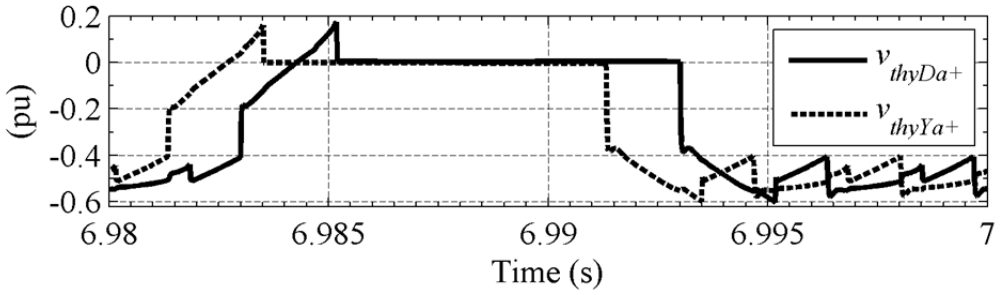

Fig. 4–23. Instantaneous voltages appearing across one thyristor in the main AC/DC conversion bridge with Q_{sR} = 0.3 pu.

4.7.4 Current Harmonics

The harmonic spectra for the *D*-branch currents on the converter and grid sides are plotted in Fig. 4–24 (a) and (b) respectively. The THD values are lower than the corresponding figures seen in Fig. 4–11, as predicted in the preceding section. Similar pattern is seen in the *Y* branch, the harmonic spectra for which are given in Fig. 4–25. The harmonic spectra for the remaining currents in the system, i.e. i_{sa}, i_{fa}, and i_{ga}, are shown in Fig. 4–26. The THD in i_{sa} (panel (a)) is lower when compared to the corresponding figure for case I (6.94% in Fig. 4–15 (a)). The grid current (panel (c)) is almost harmonic-free after the harmonics have been taken care of by the shunt passive filter.

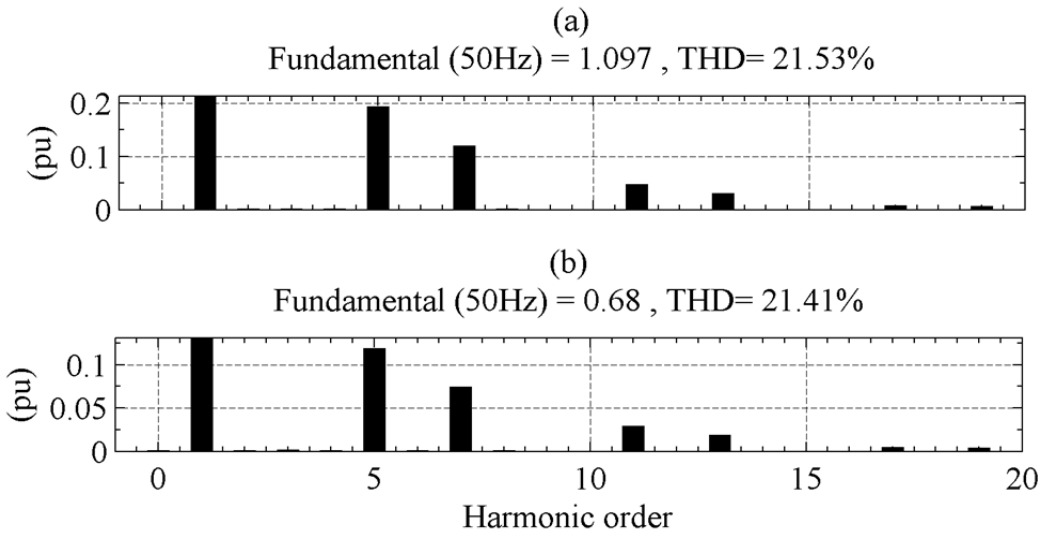

Fig. 4–24. Harmonic spectra for case II with Q_{sR} = 0.3 pu. (a) i_{lDa}, and (b) i_{sDa}.

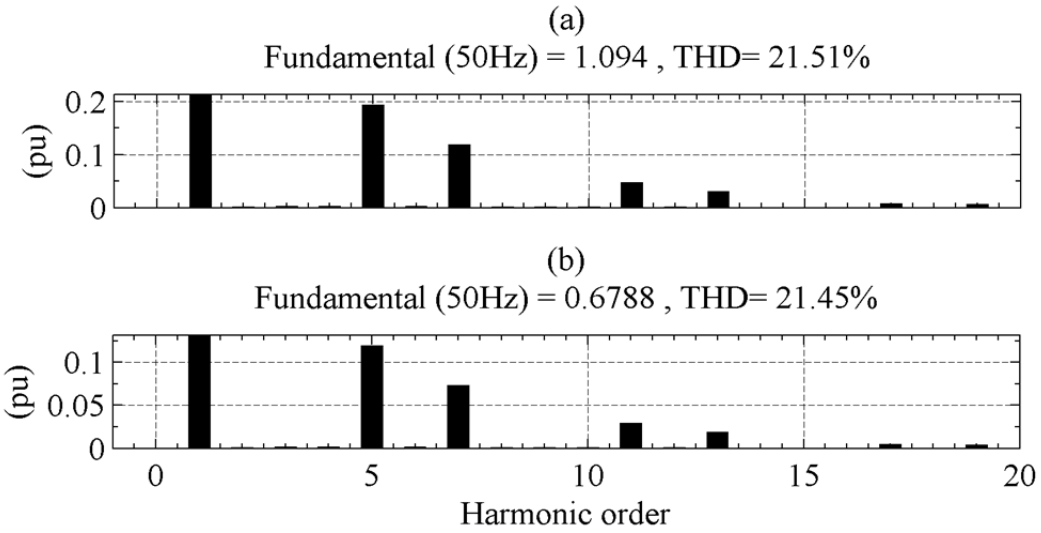

Fig. 4–25. Harmonic spectra for case II with Q_{sR} = 0.3 pu. (a) i_{lYa}, and (b) i_{sYa}.

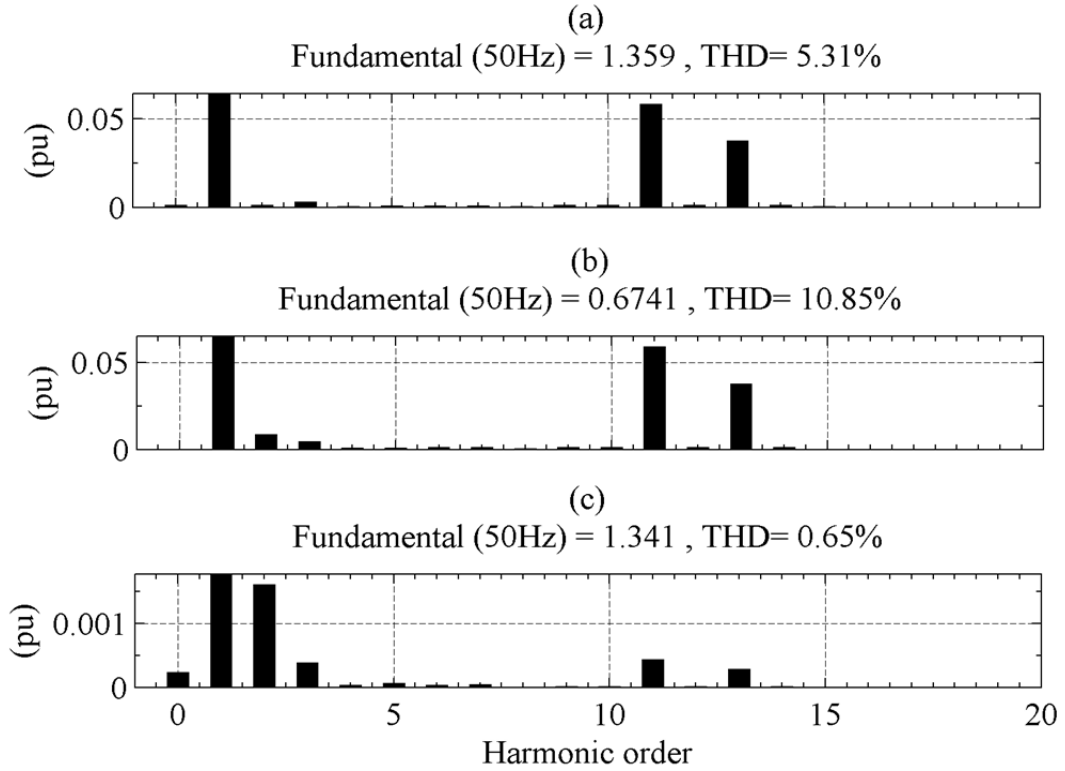

Fig. 4–26. Harmonic spectra for case II with Q_{sR} = 0.3 pu. (a) i_{sa}, (b) i_{fa}, and (b) i_{ga}.

4.7.5 Instantaneous Powers

The instantaneous-power picture for the period with partial compensation is presented in Fig. 4–27. There is a marked difference in the oscillation amplitudes of p_{lD} and p_{lY} (panel (b)) when compared to those with full compensation (Fig. 4–17 (b)). Similarly, p_s (seen plotted in panel (c)) has a lower oscillatory component than that in Fig. 4–17 (c).

The instantaneous power of the shunt filter (panel (d)) is identical to what is seen in Fig. 4–17 (d). The grid power p_g (panel (e)) exhibits slightly higher oscillatory content when compared to case I, however, it is insignificant.

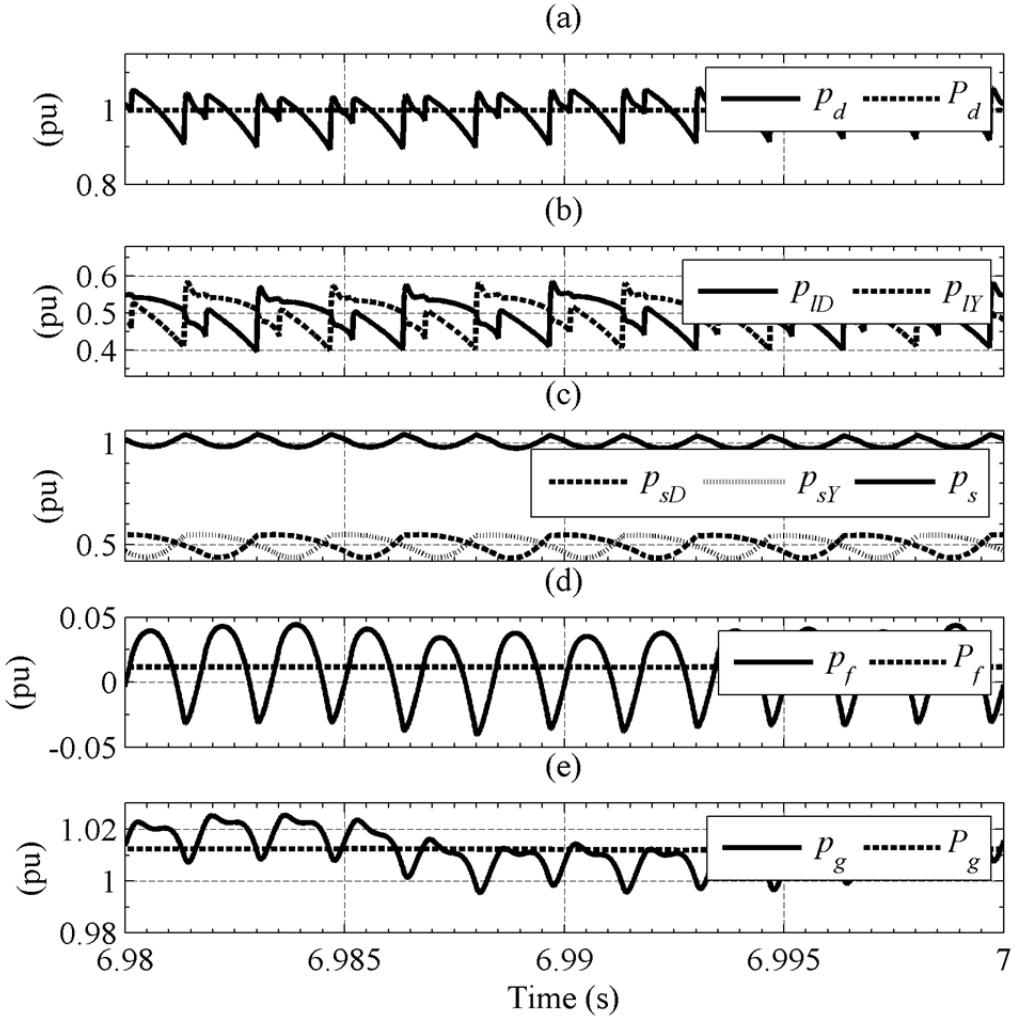

Fig. 4–27. Instantaneous powers at different locations in the system for case II with Q_{sR} = 0.3 pu.

4.8 Comparison of Harmonic Figures

The important harmonic numbers for the *D* branch are presented in TABLE 4–1. A new set of measurements has been added to the format of the table in comparison with the preceding chapters. The term "1 par." in the column with the header P_s refers to the case where the active-power flow is 1 pu and partial compensation is being done by the compensator. This set of measurements was not included in similar tables in chapter 2 and 3, because the conventional shunt-compensated HVDC did not have any series-compensation capability. Moreover, the CCC-HVDC topology discussed in chapter 3 did not have the capability to perform partial compensation at full load. The entries for

the GCSC that are listed in line with the SPF and CCC approach are for the cases in which full reactive compensation is being performed by the GCSC.

TABLE 4–1
Important Harmonic Figures in The *D* Branch

	P_s (pu)	Parameter	Value SPF	CCC	GCSC
i_{lDa}	1	THD (%)	20.40	21.02	22.99
		5^{th} (pu)	0.1855	0.1905	0.1995
		7^{th} (pu)	0.1151	0.1180	0.1341
		11^{th} (pu)	0.0377	0.0430	0.0612
		13^{th} (pu)	0.0246	0.0275	0.0440
	0.5	THD (%)	24.54	24.93	25.62
		5^{th} (pu)	0.1035	0.1048	0.1054
		7^{th} (pu)	0.0710	0.0710	0.0731
		11^{th} (pu)	0.0379	0.0393	0.0418
		13^{th} (pu)	0.0276	0.0279	0.0307
	1 par.	THD (%)	-	-	21.53
		5^{th} (pu)	-	-	0.1940
		7^{th} (pu)	-	-	0.1201
		11^{th} (pu)	-	-	0.0480
		13^{th} (pu)	-	-	0.0312
i_{sDa}	1	THD (%)	20.28	20.92	23.09
		5^{th} (pu)	0.1147	0.1189	0.1239
		7^{th} (pu)	0.0712	0.0718	0.0824
		11^{th} (pu)	0.0230	0.0272	0.0384
		13^{th} (pu)	0.0151	0.0166	0.0268
	0.5	THD (%)	24.25	24.43	26.09
		5^{th} (pu)	0.0640	0.0650	0.0652
		7^{th} (pu)	0.0442	0.0435	0.0453
		11^{th} (pu)	0.0231	0.0246	0.0258
		13^{th} (pu)	0.0171	0.0170	0.0191
	1 par.	THD (%)	-	-	21.41
		5^{th} (pu)	-	-	0.1194
		7^{th} (pu)	-	-	0.0745
		11^{th} (pu)	-	-	0.0293
		13^{th} (pu)	-	-	0.0193

The THDs of the currents flowing in the primary and the secondary windings of the converter transformer in the *D* branch are higher than those in the topologies discussed in the preceding chapters. The same holds true for the significant harmonic magnitudes. It implies that the converter-transformer design would be further complicated in comparison with the conventional and the CCC-HVDC topologies. When the GCSC is partially compensating for the reactive power, the difference in the

THDs of i_{lDa} and i_{sDa} with those with the SPF and CCC approaches is reduced. This leads to the inference that a practical implementation of the GCSC compensation should follow the same lines as those with the CCC HVDC, i.e. partial reactive compensation to be provided by the series compensator and the rest with the shunt filter, in order to avoid complications in the design of the converter transformers and the shunt filters.

Important harmonic figures for the currents flowing in the primary and the secondary windings of the converter transformer in the *Y* branch are given in TABLE 4–2. These show a similar pattern to what was observed in the case of *D* branch, i.e. elevated THD figures and higher magnitudes of significant harmonics for full and half power than those with the SPF and CCC approaches.

TABLE 4–2
Important Harmonic Figures in The *Y* Branch

	P_s (pu)	Parameter	Value SPF	CCC	GCSC
i_{lYa}	1	THD (%)	20.56	20.99	23.09
		5^{th} (pu)	0.1882	0.1898	0.2023
		7^{th} (pu)	0.1117	0.1188	0.1296
		11^{th} (pu)	0.0388	0.0432	0.0634
		13^{th} (pu)	0.0229	0.0282	0.0409
	0.5	THD (%)	24.74	24.83	25.62
		5^{th} (pu)	0.1043	0.1038	0.1056
		7^{th} (pu)	0.0697	0.0715	0.0725
		11^{th} (pu)	0.0382	0.0391	0.0424
		13^{th} (pu)	0.0264	0.0284	0.0298
	1 par.	THD (%)	-	-	21.51
		5^{th} (pu)	-	-	0.1940
		7^{th} (pu)	-	-	0.1191
		11^{th} (pu)	-	-	0.0475
		13^{th} (pu)	-	-	0.0302
i_{sYa}	1	THD (%)	20.50	20.95	23.05
		5^{th} (pu)	0.1164	0.1174	0.1252
		7^{th} (pu)	0.0691	0.0735	0.0802
		11^{th} (pu)	0.0240	0.0267	0.0392
		13^{th} (pu)	0.0142	0.0174	0.0253
	0.5	THD (%)	24.61	24.72	25.52
		5^{th} (pu)	0.0646	0.0642	0.0653
		7^{th} (pu)	0.0431	0.0442	0.0448
		11^{th} (pu)	0.0237	0.0242	0.0263
		13^{th} (pu)	0.0164	0.0175	0.0184
	1 par.	THD (%)	-	-	21.45
		5^{th} (pu)	-	-	0.1200
		7^{th} (pu)	-	-	0.0737
		11^{th} (pu)	-	-	0.0294
		13^{th} (pu)	-	-	0.0187

In the end, the harmonic characteristics of i_{sa} in comparison with those with the SPF and CCC approaches are shown in TABLE 4–3. The THD at rated condition is higher than that with the CCC approach and it is much higher when compared to the SPF approach. In contrast, the difference in THDs at 0.5-pu power flow is not as high as with the full-load case, even though it is still higher than the THDs with the other two approaches. When the GCSC is partially compensating for the reactive power, the THD in i_{sa} is reduced but is still higher than that with the SPF and CCC topologies. The magnitudes of the 11^{th} and the 13^{th} harmonic are still very high as compared to the other two topologies.

TABLE 4–3
Important Harmonic Figures in the Combined Terminal Current

	P_s (pu)	Parameter	Value		
			SPF	CCC	GCSC
i_{sa}	1	THD (%)	4.31	4.87	6.97
		5^{th} (pu)	0.0027	0.0015	0.0021
		7^{th} (pu)	0.0027	0.0021	0.0030
		11^{th} (pu)	0.0470	0.0539	0.0776
		13^{th} (pu)	0.0293	0.0340	0.0522
	0.5	THD (%)	8.51	8.78	9.69
		5^{th} (pu)	0.0017	0.0008	0.0003
		7^{th} (pu)	0.0015	0.0010	0.0006
		11^{th} (pu)	0.0468	0.0487	0.0520
		13^{th} (pu)	0.0334	0.0345	0.0375
	1 par.	THD (%)	-	-	5.31
		5^{th} (pu)	-	-	0.0009
		7^{th} (pu)	-	-	0.0009
		11^{th} (pu)	-	-	0.0587
		13^{th} (pu)	-	-	0.0379

This leads us to conclude that the GCSC topology would complicate the converter-transformer and shunt-filter designs. The shunt filter would have to be much larger than that with the CCC-HVDC approach, even though the capacitance requirement in the series compensator would be negligible compared to that in CCC HVDC.

4.9 Conclusion

The Gate Commutated Series Capacitor (GCSC) has been used in this chapter to provide series reactive-power compensation of Line-Commutated Converter based HVDC (LCC HVDC) rectifier terminal. It was shown that very small capacitors could be used as compared to Capacitor-Commutated Converter based HVDC (CCC HVDC) with the use of power-electronics technology. It was also demonstrated that the GCSC-based series compensation would follow a given reactive-power reference independent

of the active-power command; something, which is not possible with the CCC HVDC topology.

It was observed that the harmonic behaviour of the link worsened with the GCSC approach. This implies increased size and weight of shunt harmonic-compensation equipment. The harmonic behaviour was even worse than the, conventional shunt-compensated and CCC HVDC topologies. In addition, all the negative criticism of the CCC HVDC topology is equally applicable to GCSC approach.

5 The Series Pulsed Voltage Compensator

The major contribution of this work is introduced here. The construction and control of the proposed compensator is discussed in detail. The simulation results with regards to reactive/harmonic compensation capability of the proposed compensator have been presented in addition to the comparisons with the previously discussed topologies.

The details of the proposed compensator will be discussed in this chapter. The motivation of this proposal is the fact that series compensation is now being extensively used in Flexible AC Transmission Systems (FACTS) technology [64]. Fixed series capacitors have been used to improve the stability and increase the power-transmission capacity of AC-transmission lines [75]. Thyristor-controlled series compensators (TCSC) can achieve variable series compensation of transmission lines [83]. The use of the gate-commutated series compensator (GCSC) [78, 79] was demonstrated in the preceding chapter and it was observed that the harmonic behaviour of the link worsened and needed even larger shunt filters to compensate for the harmonics and the advantage achieved by reduction in series capacitance would be mostly (if not completely) offset by larger shunt filter. Magnetic energy recovery switch (MERS) [101, 102] is another series compensator employing single-phase bridge circuits in series in each phase to act as variable capacitors. Several successful experiments have been reported for various applications from low to medium power and voltages.

All of the above-mentioned compensators are transformer-less topologies, their main difference with the static synchronous series compensator (SSSC) [77], which uses an injection transformer and switching-harmonic filters on the converter side to inject a purely-sinusoidal voltage in quadrature with the line current. The complication and cost involved with SSSC have, therefore, rendered it an economically unattractive option.

Transformer-less compensators with the exception of fixed-series capacitors have the disadvantage that they inject non-sinusoidal voltages into the system. These can, therefore, distort the voltage beyond their point of connection. This can be detrimental as unnecessary resonances can be caused by these harmonics in a transmission line. If used at the terminal point of a line - for example, at a consumer's point of connection - sensitive loads can fail leading to further problems. Fixed series capacitors also inject non-sinusoidal voltage into LCC HVDC terminals owing to the AC-current wave-shape in such systems. However, this is not detrimental as the resulting voltage is applied to the thyristor bridges.

It has to be noted that series compensators with self-commutating switches have not been used to compensate for reactive power in LCC HVDC systems. There are a few papers that suggest the use of GCSC in a superconducting-magnetic-energy-storage application employing thyristor bridges [100].

The aim, here, was to propose a series compensator that could reduce the size of the series capacitors required to fully compensate for reactive power as well as not aggravate (if not improve) the harmonic problem as seen by the use of fixed-series capacitors and the GCSC. The problem can be simply seen as one of reduction in the commutation reactance because of the partial cancellation of transformer leakage reactance with the capacitor reactance.

The instantaneous voltages across the series capacitors in CCC HVDC depend on the current waveform. This means that the capacitor should be large enough to avoid an overvoltage due to integration of current.

If there was a controlled voltage injection scheme that could stop the capacitor from uncontrolled charging, small capacitors could be used as the main purpose of the capacitor in this context is to change the commutating voltage with respect to the grid voltage for forcing early commutation. In addition, there should be an arrangement to recharge the capacitor for use in subsequent commutations. In the case of the GCSC, the magnitude of injected voltage is controllable, but the topology has to allow charging of the outgoing-phase capacitor for use in the next commutation. This is what causes the harmonic situation to worsen.

These objectives can only be achieved by the use of self-commutating switches in conjunction with capacitors. A single-phase bridge in each phase can serve the purposes of controlled voltage injection and recharging the capacitors as and when desired.

5.1 Proposed Arrangement

The schematic of the system with the proposed compensators is shown in Fig. 5–1. This is the same arrangement as used in chapters 2, 3, and 4, with the exception of the series compensator which replaces the series capacitors of Fig. 3–1. The schematic for the full bridge in each phase is given in Fig. 5–2. As will be explained in the succeeding pages, the compensator injects voltage pulses to achieve reactive/harmonic compensation. We propose the name **Series Pulsed Voltage Compensator (SPVC)** for the arrangement.

This compensator is a single-phase bridge consisting of IGBTs employing a DC capacitor on its DC link. The size of the capacitor used in simulations is 10 μF. It should be noted that the total capacitance in all the six lines connecting the converter-transformer secondary windings to the thyristor bridges will then be 60 μF. For comparison, the total capacitance in the conventional shunt passive filter arrangement is 273 μF, whereas the total series capacitance in CCC HVDC system, presented in chapter 3 is 510 μF. The total capacitance required in the GCSC arrangement discussed

in chapter 4 is also 60 μF. In addition, all of these topologies employ AC capacitors in contrast to the DC capacitors used in the SPVC.

The reference polarity in Fig. 5–1 and Fig. 5–2 is chosen so that the reactive power of the compensator is negative when it is supplying and positive when it is absorbing reactive power. The same holds true for the instantaneous power. As will be explained later, the polarity of the voltage across the capacitor is fixed with the positive bus indicated in Fig. 5–2.

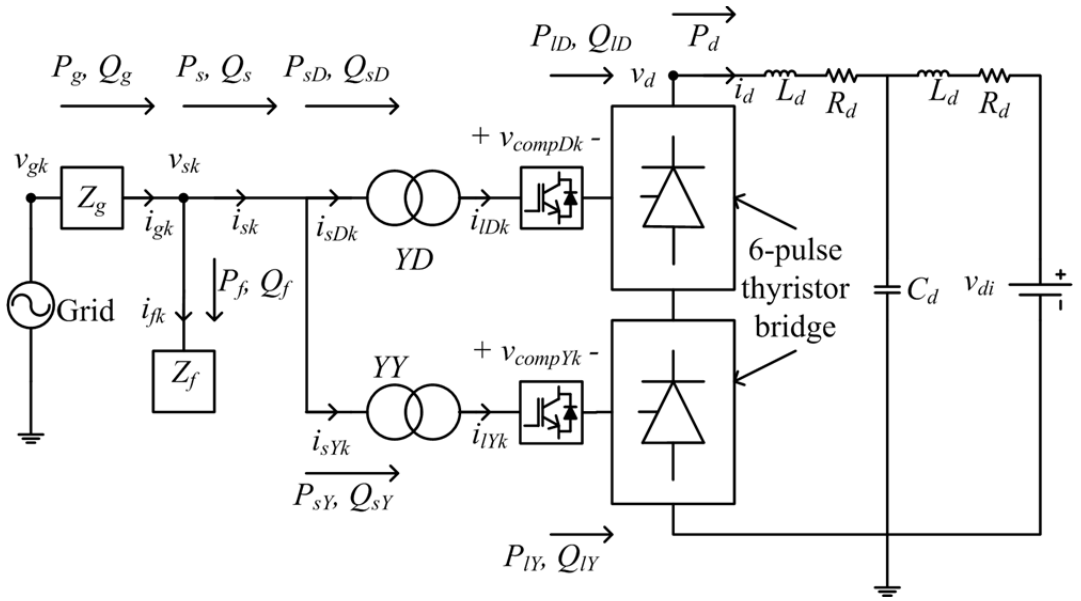

Fig. 5–1. Schematic arrangement of the HVDC conversion system with the proposed compensator. The series compensators are connected in series in each phase.

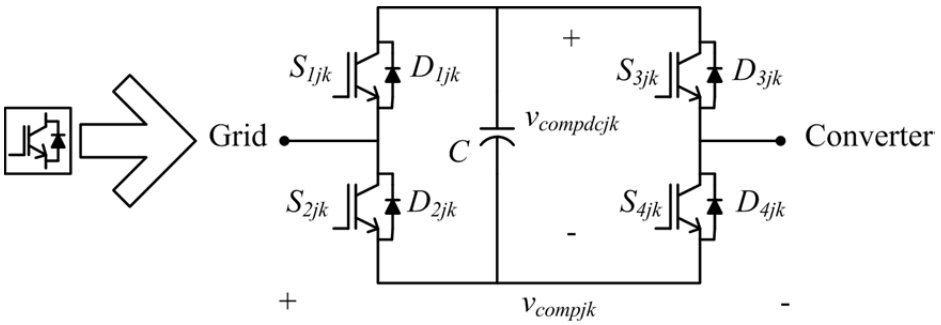

Fig. 5–2. Schematic arrangement of the series compensator in Fig. 5–1.

5.2 Switching Scheme of the SPVC

With reference to Fig. 5–2, the voltage across the capacitor is denoted as $v_{compdcjk}$, where j is either D or Y, indicative of the branch concerned; and k is the either a, b, or c, denoting the phase. The same subscripts appear along the IGBT and diode numbers.

The main consideration here is that an assisting-polarity voltage should be injected into the incoming phase, which would force the converter terminal voltage to cross over before the actual commutating-voltage crossover. The measurement of phase angle and the eventual firing of the thyristor in the incoming phase can now be done from the crossover of the altered commutating voltage. This is similar to CCC HVDC as shown in Fig. 3–2; the difference being the injection of series voltages uncontrollably into the outgoing and incoming phases by CCC HVDC. The fixed capacitor in the outgoing phase absorbs energy and has to be made large enough to keep the voltage on the capacitor as low as possible.

In controlled series injection, only the assisting-polarity voltage is injected into the incoming phase, which discharges the capacitor bringing its voltage down. The opposing-polarity voltage is injected when charging the capacitor and can be discontinued as the desired voltage magnitude is achieved. This would help reduce the size of the capacitors required in such an arrangement.

There are, therefore, three requirements on a compensator in each phase:

1. Inject an assisting-polarity voltage in the incoming phase to force early commutation. This assisting polarity is different for current commutation in the positive and negative half-cycles of the current. No opposing-polarity voltage would be injected in the outgoing phase.
2. Inject an opposing-polarity voltage in the phase to which the current commutated in step 1 to recharge the capacitor. This would provide the voltage needed to be injected again when the phase would undergo commutation again to take up the current in the opposite half-cycle.
3. Bypass the capacitor in the compensator during all other times.

As a result of the above objectives, the SPVC injects short-duration voltage pulses. As will be presented later, the SPVC does not employ high-frequency switching like SSSC, and, hence, does not have the drawback of high switching-frequency losses. Secondly certain switching actions in the compensation process occur at zero voltage and some at zero current making the loss minimal.

5.2.1 Switch Modulation for Current Commutation

Based on the discussion above, the algorithm for charging is presented in Fig. 5–3. The algorithm shown is for commutation of current from phase *c* to *a* in the positive and negative half cycles in panels (a) and (b) respectively. The switch-modulation algorithms for commutations from phase *a* to *b* and from phase *b* to *c* will be similar with the input variables taken from the respective line voltages, SPVC DC-link voltages, and the line currents.

Referring to Fig. 5–3 (a), the induced line voltage behind the leakage reactance is e_{jca}. When this crosses into its negative half-cycle, phase *a* becomes more positive than phase *c*, the positive current flowing in phase *c* should commutate to phase *a*. So a voltage injected into phase *a* opposing e_{jca} will force early crossover of converter

terminal voltage. This can be achieved by switching S_{2ja}, and S_{3ja} of the compensator in phase *a*. This injected voltage v_{compja} will have an opposite polarity to that of the reference polarity chosen in Fig. 5–1 and Fig. 5–2.

The timing of the injection is as soon as e_{jca} goes below $v_{compdcja}$ (the voltage available on the DC-link capacitor in the compensator connected in phase *a*). A set-reset flip-flop would be set, which would drive the gate signals of the concerned switches high, turning them on. The gate signals would be reset once e_{jca} would become higher in magnitude than $v_{compdcjR}$ (the reference DC-link voltage on the capacitor in the series compensators in the *j* branch). The second condition for resetting is that the current in the incoming phase should attain at least 90% of the reference current. The algorithm for commutation of current from phase *c* to *a* in the negative half-cycle is similar in nature with a few differences as can be seen in Fig. 5–3 (b). This is because the algebraic sign on e_{jca} and i_{lja} reverse whereas $v_{compdcja}$ and $v_{compdcjR}$ retain their positive sign.

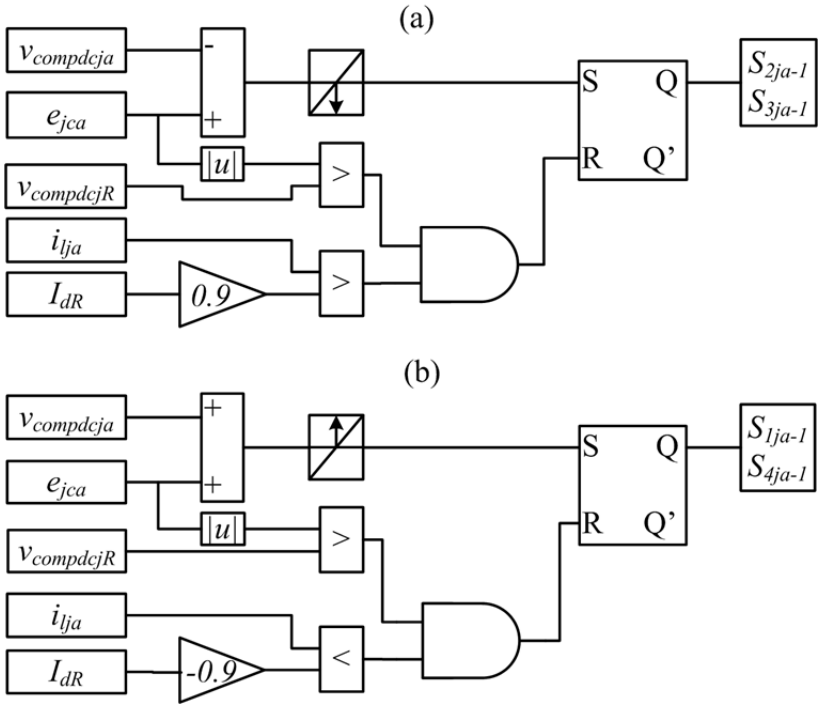

Fig. 5–3. Algorithm for switch modulation for assisting commutation from phase *c* to *a* in the (a) positive half cycle, and (b) in the negative half cycle.

The polarities of the compensator-injected voltages and the current paths during the positive and negative half-cycle are depicted in Fig. 5–4 (a) and (b) respectively. The polarity of the injected voltage and the direction of the current indicate that the compensator will discharge the DC-link capacitor of the compensator. Of course, this discharge will only occur once the current starts to flow after the firing of the concerned thyristor in the thyristor bridge. This will happen after a lapse equal to α from the switching of the compensator IGBTs.

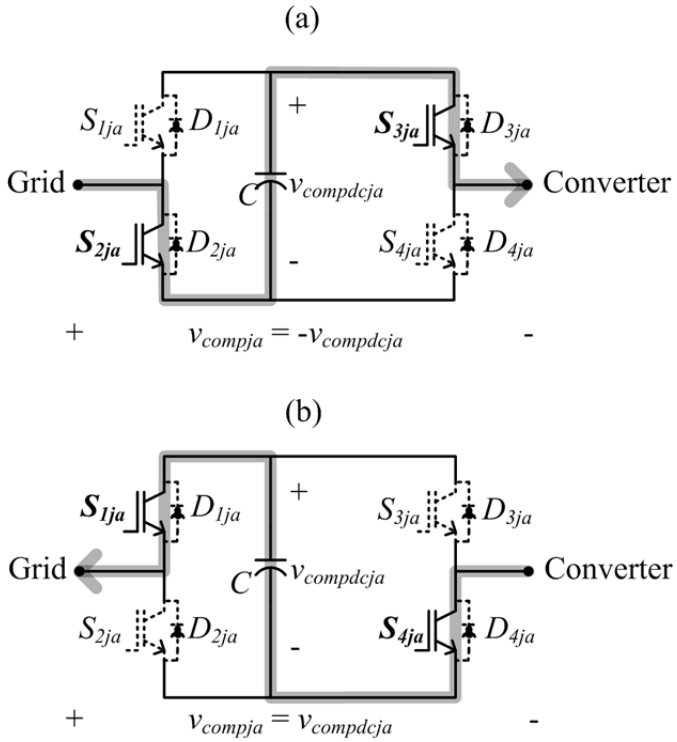

Fig. 5–4. Current flow and injected voltage during commutation in (a) the positive half-cycle, and (b) the negative half-cycle. Current is represented by the thick grey line with the arrow-head indicating the direction.

A major difference between CCC HVDC (also the GCSC) and the SPVC is that an assisting-polarity voltage is injected into the incoming phase only, and no opposing-polarity voltage is injected into the outgoing phase. The reason is that the assisting-polarity voltage will always drain the DC link of the compensator bringing the voltage on the capacitor down. On the other hand, an opposing-polarity voltage injected into the outgoing phase would make the compensator DC link absorb energy, thereby increasing the DC-link voltage. The smaller the capacitor on the DC link, the higher will be the voltage. This would drive up the weight and size of the DC-link capacitors as well as the required insulation.

5.2.2 Switch Modulation for Compensator Recharging

Once the commutation is complete, the compensator DC-link capacitor has to be recharged for the next commutation. This recharging has to be done after commutations in the positive and negative half-cycles, both. The algorithm for recharging the compensator DC-link capacitors is presented in Fig. 5–5. The basic condition is that the charging switch combination should be turned on only when the discharge switch combination has been reset. The charging switch combination should then be kept on as long as $v_{compdcja}$ is smaller than $v_{compdcjR}$ (the reference DC-link voltage). The other condition is that the current in the phase in which the compensator is connected should have increased beyond a specific percentage of the reference load current. In this case, it has been fixed at 50%. However, this algorithm will not be activated until the algorithm

in Fig. 5–3 is deactivated, and that requires the current to build up beyond 90% of the reference value.

The current direction and the voltage polarity for the SPVC during the positive and negative half-cycle are shown in Fig. 5–6 (a) and (b) respectively. It can be observed that the switch combination used for discharging in positive half-cycle is being used to charge the capacitor in the negative half-cycle and vice versa. Another point worth noticing here is the current conduction path. Even though an IGBT is switched on in the charging mode, the current flows through the antiparallel diode and not the IGBT. Therefore, an alternative algorithm for DC-link recharging is to simply turn off all the IGBTs when the output of the AND gates in Fig. 5–5 go high.

5.2.3 Switch Modulation for Compensator Bypass

The SPVC should be bypassed when it is neither discharging (i.e. during commutation) nor charging. This can be achieved by a simple algorithm consisting of a NOR gate with the inputs taken from the outputs in Fig. 5–3 and Fig. 5–5. The bypass algorithm is shown in Fig. 5–7 with the corresponding conduction paths in Fig. 5–8. The dotted switch combination in Fig. 5–7 is an alternative if the positive DC bus of the series compensator is to be used as the bypass path as shown in Fig. 5–8.

It can be observed that one IGBT and diode will form the conduction path for bypass in one direction and the alternate IGBT and diode would form the bypass path in the reverse direction. Therefore, another algorithm could be to switch on just one suitable IGBT in one direction of current and the alternative IGBT could be switched on for reverse flow. This could further reduce the switching losses. As an example, with reference to Fig. 5–8 (a), S_{2ja} could be switched on for positive current and S_{4ja} could be switched on for negative current. Similar approach can be used when using the positive DC bus as the bypass path.

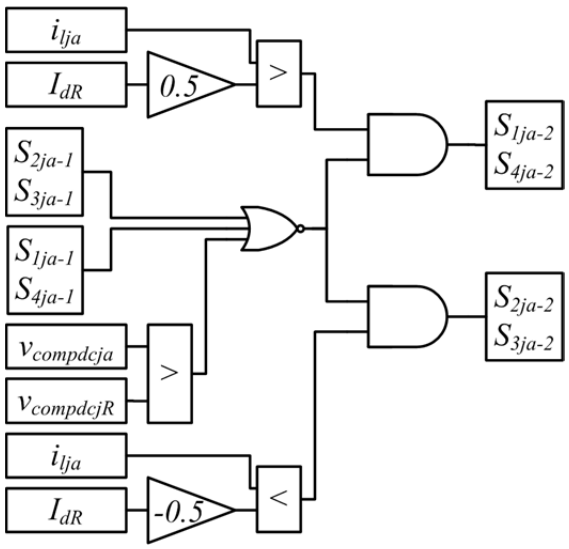

Fig. 5–5. Algorithm for switch modulation for recharging the DC-link capacitor of the SPVC in the positive and negative half-cycles.

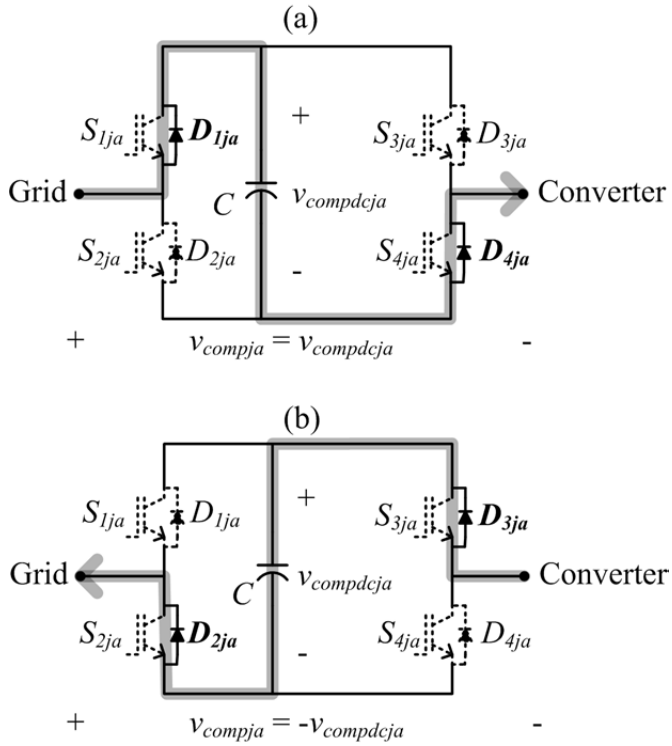

Fig. 5–6. Current flow and injected voltage during recharge in (a) the positive half-cycle, and (b) the negative half-cycle.

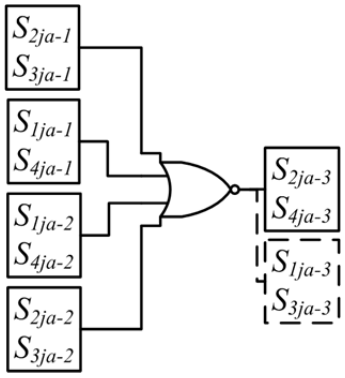

Fig. 5–7. Algorithm for switch modulation for bypassing the SPVC in the positive and negative half-cycles.

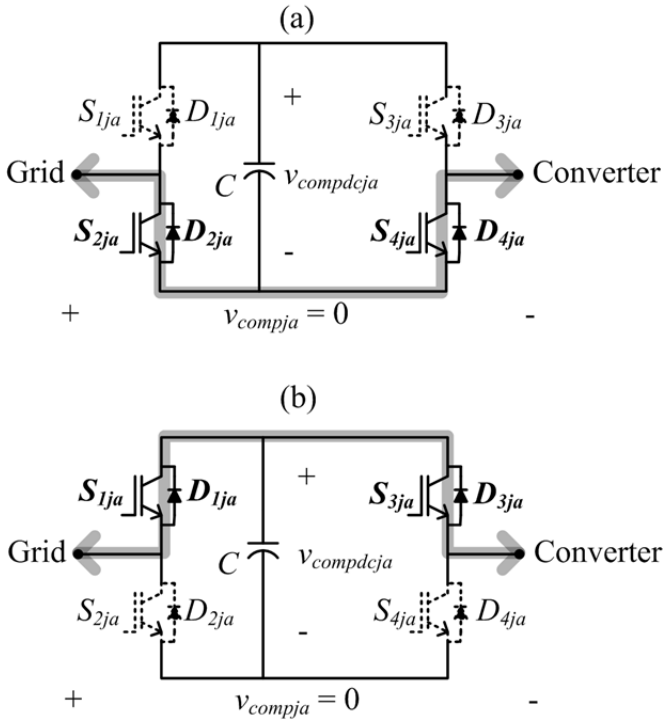

Fig. 5–8. Current flow and injected voltage during bypass when (a) negative DC bus is chosen as the bypass path, and (b) positive DC bus is chosen as the bypass path.

5.3 The Commutation Process

The commutation circuit with the SPVC is shown in Fig. 5–9. The difference from CCC and GCSC topologies is that the series voltage is only injected into the incoming phase. The polarity indicated is the reference polarity and not the actual polarity during the current commutation in the positive half-cycle. In fact, the voltage polarity is opposite to the one that is shown here when positive current is to commutate from phase *c* to phase *a*. The equation of the commutation circuit becomes:

$$e_{jac} = 2L_{tr}\frac{di_{comm}}{dt} + v_{compja} \tag{5.1}$$

This is so because, the SPVC leg in the outgoing phase does not inject any voltage. This injected voltage forces an early crossover and the thyristor is fired after an interval determined by α. As soon as the thyristor is fired, the magnitude of the injected voltage drops depending upon the current that starts to flow in phase *a*. The voltage after the start of commutation is given by:

$$v_{compja} = v_{compja(0-)} - \frac{1}{C_{compja}}\int i_{lja}dt \tag{5.2}$$

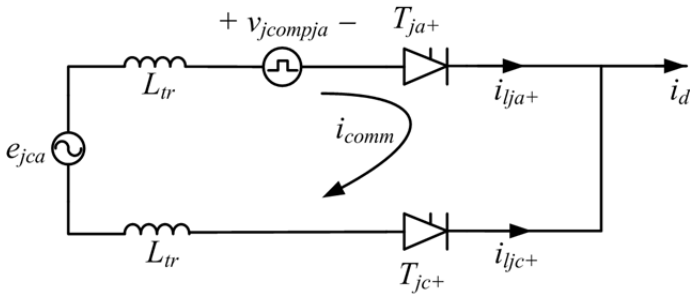

Fig. 5–9. Commutation circuit for SPVC HVDC.

This voltage does not drop below zero due to reasons discussed in section 5.2. This is where SPVC is different from CCC and GCSC topologies. In CCC, the capacitor continues to conduct and charges to a specific voltage for commutation in the negative half-cycle before it is commutated out of the circuit in the positive half-cycle. The magnitude of the voltage depends upon the current flowing in the phase and the value of the capacitor. With the GCSC, the capacitor discharges cooperatively during commutation and the bypass is turned on as the capacitor voltage hits zero. But the bypass is deactivated when the phase is about to commutate out of the circuit during positive half cycle for the capacitor to charge for commutation in the negative half-cycle. There is more freedom available in the GCSC approach than the CCC topology. The voltage on the capacitor depends upon the current, the value of the capacitor and the duration of bypass. However, once the bypass is deactivated, it cannot be reactivated again unless the capacitor voltage hits zero. In SPVC, bypass can be activated at any time. The additional degree of freedom is that the SPVC can charge or discharge as per the control methodology.

After the completion of commutation, the SPVC in phase *a* has to recharge for the next commutation (i.e. during the negative half-cycle). The switching combination employed charges the SPVC capacitor during this phase according to:

$$v_{compja} = \frac{1}{C_{compja}} \int i_{lja} dt \tag{5.3}$$

The rest of the equations for active and reactive power hold as discussed in the preceding chapters; the exception being the reactive power. In CCC and GCSC approaches, the voltage injected by the series compensator has a significant fundamental-frequency component that leads the current by 90°. This influences the phase of the voltage at the thyristor terminal. The phase of the current is also influenced due to series compensation. The reactive power consumed by the thyristor terminal depends upon the relative phase between the phase-shifted voltage and current waveforms. In SPVC, the voltage is injected in pulses for charge and recharge and there are four voltage injections in a single-cycle; two each for discharge and recharge in each half-cycle. The principal frequency of the injected voltage is therefore double the fundamental frequency. The fundamental component is thus very small and therefore, the influence on the phase of fundamental voltage at the thyristor terminal is negligible.

However, the current phase is significantly influenced by earlier commutation. Therefore, the thyristor terminal consumes far less reactive power with the SPVC than without it. This is an effect that would be observed in the simulation results repeatedly. Additionally, the reactive power supplied by the SPVC would also be much smaller due to the smaller fundamental-frequency voltage injected by it.

5.4 Simulation Setup

Based on the discussion in sections 5.1 and 5.2, simulations were carried out as in chapters 2, 3, and 4. The control loops of Fig. 2–6 and Fig. 3–2 for constant-α and active-power control respectively have been used the way they were in chapter 2 and 3.

As will be demonstrated in the simulation results, the SPVC has the capability to regulate the reactive-power intake from the rectifier-side AC grid (like the GCSC topology discussed in the preceding chapter), a control loop is required, as with the GCSC, which should compare a reference value for reactive power from the grid and compare it with the actual value to control the magnitude and instant of voltage injected by the SPVC. The output of this control loop is therefore $v_{compdcjR}$. The control loop is depicted in Fig. 5–10. The reference reactive power that should flow into the two converter transformers is divided by 2 and subtracted from the actual reactive flow into each transformer. The error signals are processed by *PI* controllers and the outputs form the reference voltage on the DC-link capacitors of the SPVCs in the *D* and *Y* branches. As the two branches have identical active- and reactive-power consumption, the output reference voltages would also be identical (except in transient stages). Two cases have been simulated to demonstrate the adequateness of the compensator and its control loops and algorithms.

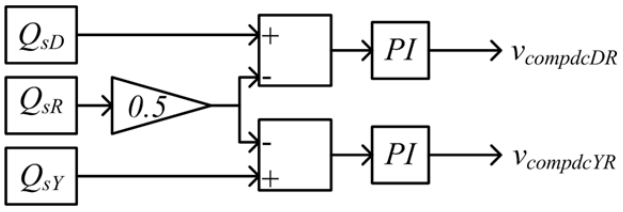

Fig. 5–10. Reactive-power control loop for the SPVC.

5.4.1 Case I: Changing Active-Power and Constant Reactive-Power Reference

The simulations start with 1-pu active power without series compensation. The SPVC is connected at 3 s. The active power is brought down to 0.5 pu at 5 s. Q_{sR} is kept at 0 pu throughout. This means that the SPVC has to eliminate reactive-power flow from the AC grid into the converter transformers.

5.4.2 Case II: Constant Active-Power and Changing Reactive-Power Reference

The ability of the SPVC to let a controlled quantity of reactive power from the AC grid into the converter transformers is demonstrated in this case like case II in the preceding chapter with the GCSC as the series compensator. The simulations start with active power fixed at 1 pu. The reactive power reference is set to 0 pu initially. The SPVC is connected at 3 s. Thereafter, Q_{sR} is changed to 0.3 pu at 5 s, implying a controlled flow of reactive power from the AC grid.

5.5 Simulation Results for Case I

5.5.1 Active and Reactive Powers

The active and reactive powers at different points in the system are plotted in Fig. 5–11. P_s and Q_s are plotted in panel (a). Q_s is at just above 0.5 pu before the SPVC is connected at 3 s. Q_s is brought down to 0 pu by the action of the SPVC.

The components of Q_s in the D and Y branches are plotted in Fig. 5–11 (b) and (c) respectively, along with the respective SPVC reactive power and the thyristor bridge consumption. The interesting thing to note here is that Q_{lD} and Q_{lY} values are reduced even when the active power is not reduced. This is in contrast with what was observed with CCC and GCSC compensation, where the reactive-power consumption of the thyristor bridges did not change with the addition of the series compensation. Due to this reduction in Q_{lD} and Q_{lY}, Q_{compD} and Q_{compY} values (under 0.2 pu) are less than those of Q_{sD} and Q_{sY} before compensation (almost 0.3 pu). Q_{sD} and Q_{sY} are brought down to 0 pu with the injection of lower reactive power by the SPVC.

The satisfactory action of the SPVC can also be observed after the change in active power at 5 s. Q_s remains zero, so do Q_{sD} and Q_{sY}. The SPVC changes its voltage injection again to adjust Q_{compD} and Q_{compY} to eliminate reactive-power flow into the converter transformers. This is in contrast with the plots in Fig. 3–4 for CCC HVDC, where the series capacitors are unable to fully compensate for the reactive-power demand of the system. The reactive power supplied by the shunt passive filter is exported to the grid as the converter terminal itself does not need any reactive power from it, as seen in Fig. 5–11 (d).

A comparison with the GCSC compensator shows that the values of Q_{lD} and Q_{lY} with the SPVC (Fig. 5–11 (b) and (c)) came down; whereas they did not with the GCSC. As a result, Q_{compD} and Q_{compY} have smaller magnitudes with the SPVC than with the GCSC. The same holds true for the interval between 5 and 7 s.

5.5.2 Control Loop Operation

The behaviour of the control loops depicted in Fig. 2–6, Fig. 3–2, and Fig. 5–10 is plotted in Fig. 5–12. At the start of series compensation at 3 s, the voltage profile

on the converter terminal improves resulting into an increased DC-link current which increases active-power flow on the AC side. The active-power control algorithm of Fig. 3–2 attempts to increase α but the constant-α control algorithm in Fig. 2–6 observes this deviation and reduces the input AC voltage. These values settle and go through a transition again when the active-power reference is reduced to 0.5 pu at 5 s. The interesting thing to note here is the variation in V_{sa}, the rms value of the phase voltage at converter-transformer primary (Fig. 5–12 (b)). It is clearly observable that V_{sa}, for the same amount of active-power flow, without the SPVC (before 3 s) is much higher than that with the SPVC (between 3 and 5 s). This means a lower voltage and insulation rating is required for the converter transformer and allied equipment. At the same time, the reactive power control loop in Fig. 5–10 observes the error between the reference reactive power and the actual and adjusts the reference voltage on the SPVC DC-link capacitor to a value of 0.3 pu at full load. After the reduction in active power at 5 s, the reactive-power demand is lowered, forcing control loop to lower $v_{compdcjR}$.

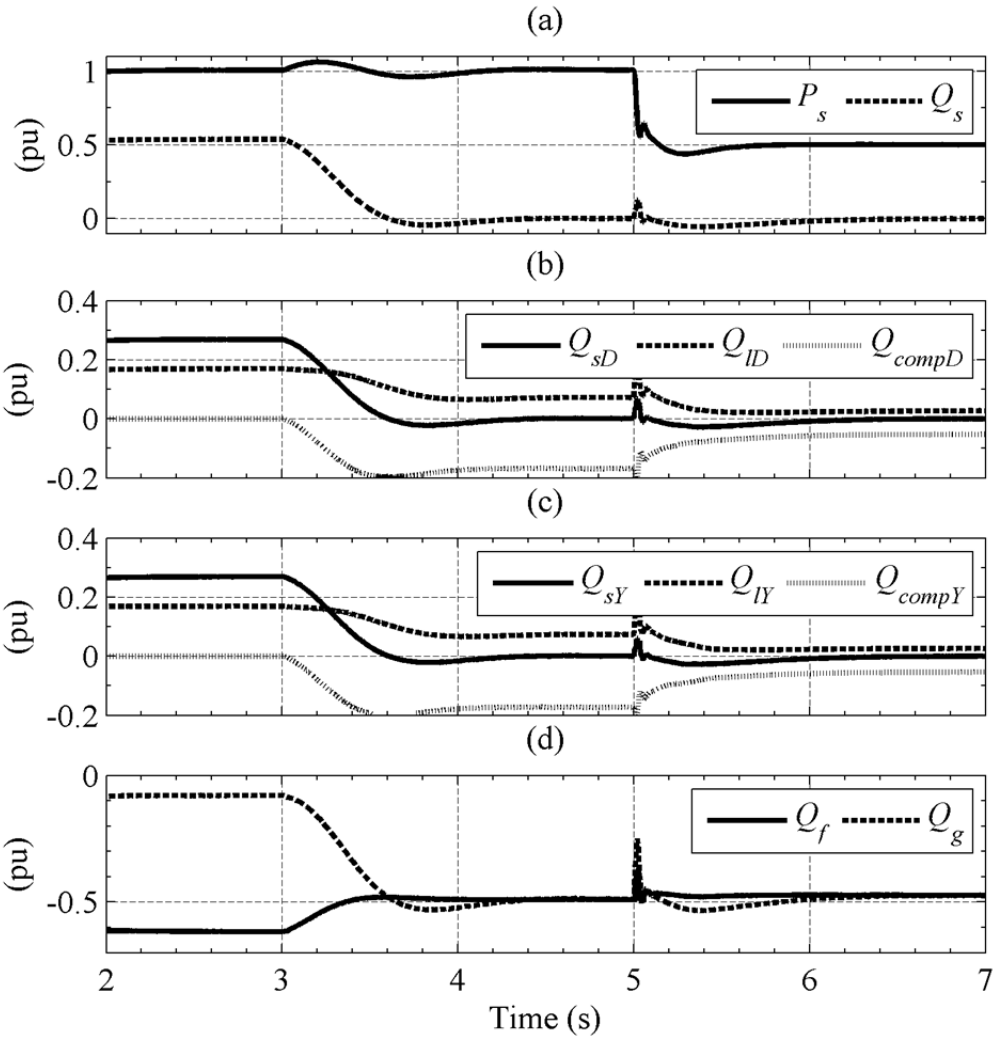

Fig. 5–11. Active and reactive powers at different points in the system.

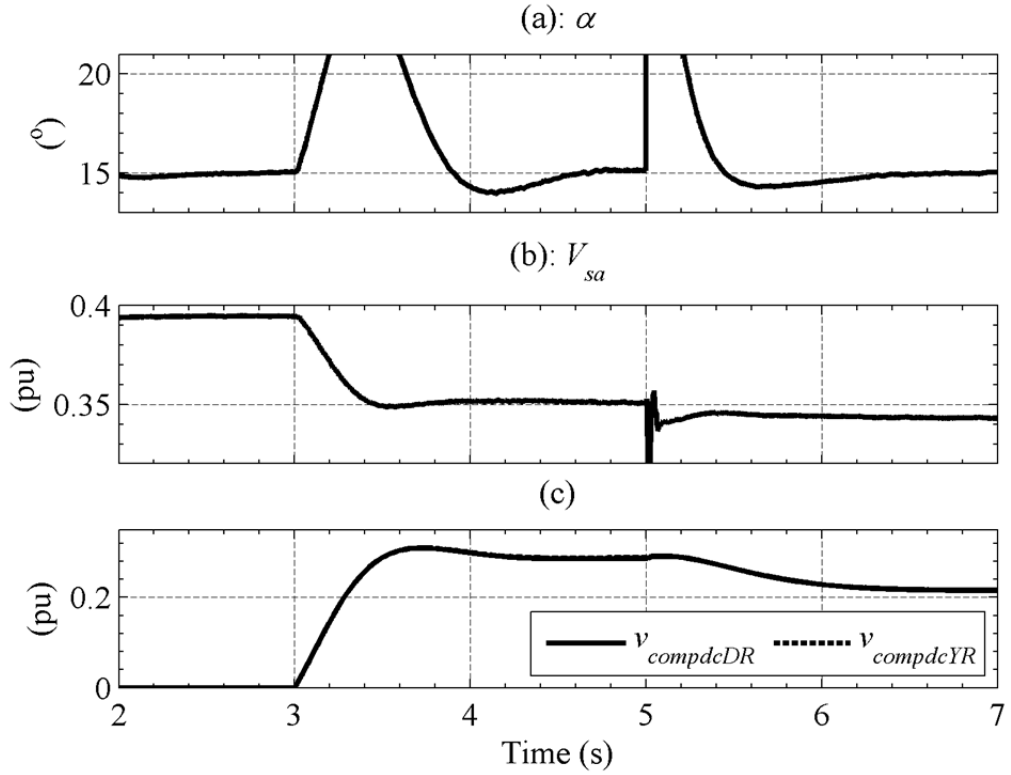

Fig. 5–12. Behaviour of control loops (a) α, (b) rms value of the phase *a* voltage on the converter transformer primary side, and (c) reference voltage on the series-compensator DC-link capacitor.

5.5.3 Instantaneous Currents and Voltages

The voltage injected by the compensator, load current, and phase voltage behind the transformer leakage reactance for phase *a* in the *D* branch are plotted in Fig. 5–13. Without compensation (Fig. 5–13 (a)), there is a distinct phase difference between the voltage and current which is responsible for the reactive-power consumption. It is due to the fact that the thyristor is fired after a delay equal to α after the phase *a* voltage becomes higher than the phase *c* voltage (not shown here).

When the SPVC is connected and the load is drawing 1 pu power, an assisting-polarity voltage is injected into phase *a* which forces the commutating voltage crossover at an earlier instant, and even a lag of α after this artificial crossover does not make the converter terminal consume reactive power. As can be seen in Fig. 5–13 (b), during commutation, the injected voltages decreases and finally goes to zero as the DC-link capacitor is discharged of its stored energy. To recharge this capacitor, the SPVC switches to the algorithm of Fig. 5–5, and an opposing-polarity voltage is injected which increases as the capacitor charges. When the DC-link voltage is equal to the reference determined by the control loop in Fig. 5–10, the compensator switches to bypass mode in accordance with the algorithm in Fig. 5–7.

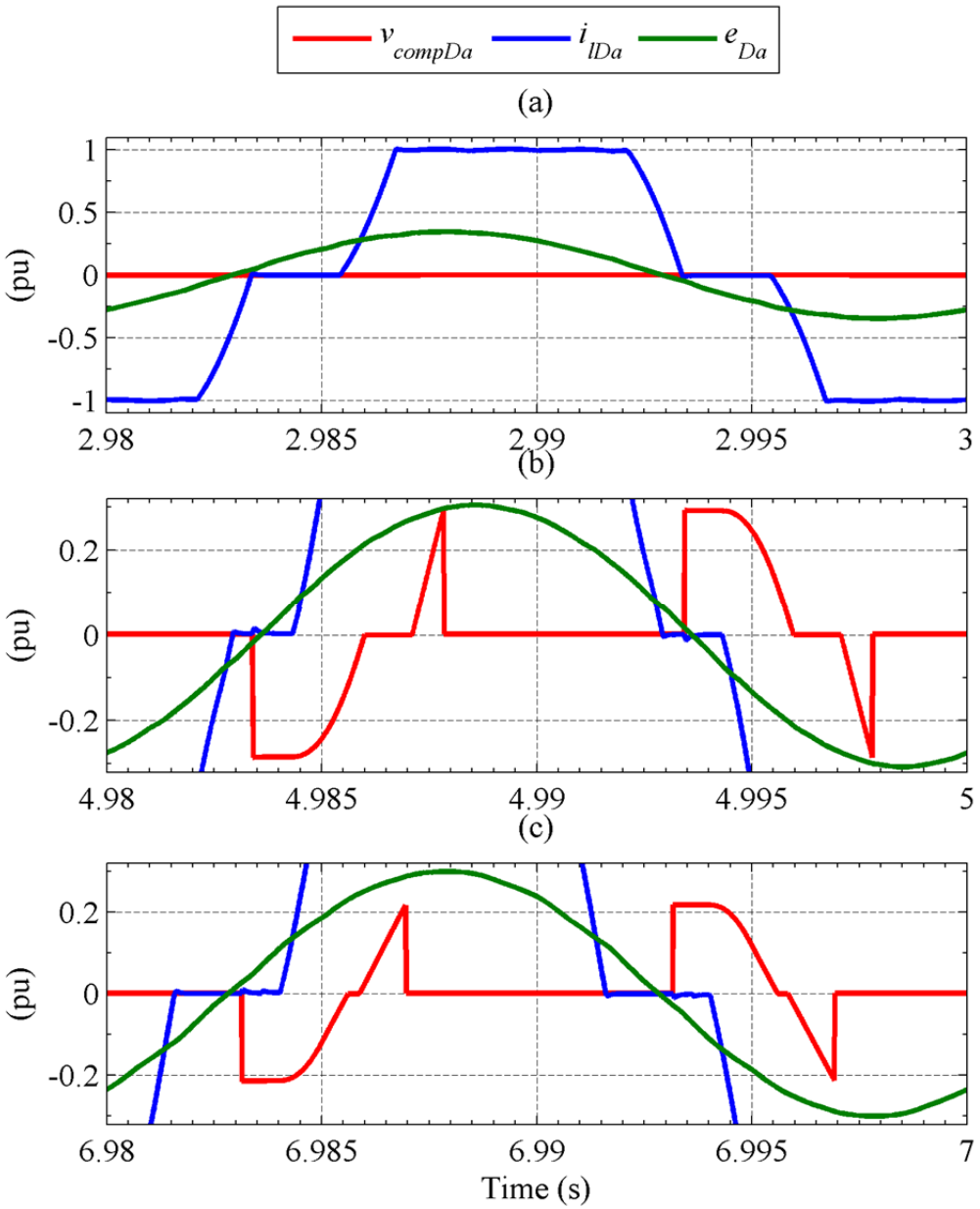

Fig. 5–13. Single-cycle plots of selected variables on the converter side (a) without series compensation at full load, (b) with series compensation at full load, and (c) with series compensation at 0.5-pu load.

The peak of the voltage injected by the series capacitor for full load is almost ±0.3 pu. When compared to the CCC HVDC case, the voltage injected by each capacitor is of the order of ±0.18 pu (0.36 pu peak to peak). This is logical because in CCC HVDC, capacitors in the outgoing and incoming phase contribute to the commutating voltage. The disadvantage of that approach is an effective reduction in commutation reactance leading to worse harmonic characteristics. However, as will be demonstrated later, the DC-link capacitor on the proposed compensator has a unipolar voltage with the peak given by the peaks of the positive and negative voltages injected by the SPVC (0.3 pu in this case).

The behaviour of the system and the SPVC at half power is depicted in Fig. 5–13 (c). The voltage injected by the SPVC is reduced now as the reference tracking the reactive power flow into the converter transformers detects that a lower voltage would be sufficient to eliminate reactive power. This reduction is controlled in contrast to the uncontrolled reduction in injected voltage by the fixed capacitors in CCC HVDC (Fig. 3–6 (c)) which led to a non-zero reactive-power flow into the converter transformers (Fig. 3–4).

The commutating voltage e'_{ca} without SPVC, with SPVC at full load, and with SPVC at partial load is depicted in Fig. 5–14 (a), (b), and (c) respectively. Without the SPVC (panel (a)), the commutating voltage crosses over at the natural crossover of the phase voltages. However, with series injection (panel (b)), it crosses over before the natural crossover and the thyristor is then fired bases on the angle measurement from this crossover, hence the reduced reactive-power consumption due to artificial commutation. With reduced load (panel (c)), the point of injection and consequently the point of artificial crossover moves closer to the natural crossover point as explained before.

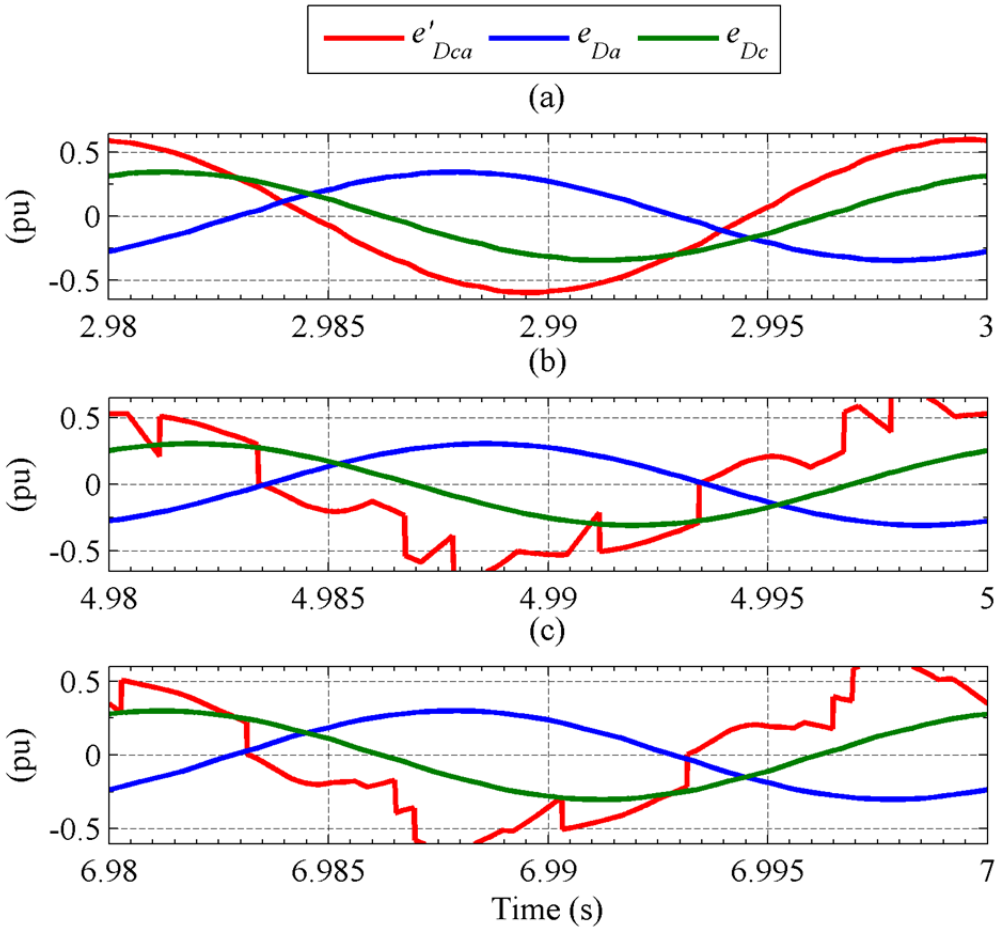

Fig. 5–14. Commutating voltage between phase *c* and *a* in the *D* branch (a) without SPVC, (b) with SPVC at full load, and (c) with SPVC at 0.5-pu load.

When the commutating voltage in the proposed compensator is compared to that in CCC HVDC (Fig. 3–7), it is observed that the former is more distorted than the latter. However, the phase of the fundamental does not change in contrast to the CCC-HVDC case. This is the reason for the apparent reduction in reactive-power consumption by the thyristor bridges.

The commutation of current is presented in more detail in Fig. 5–15. The situation without series compensation has been explained before. The effect of pulsed-voltage injection can be seen in Fig. 5–15 (b) and (c) for full and half power respectively. In the uncompensated case, the commutating voltage increases as a sine function in favour of the incoming phase during commutation (Fig. 5–15 (a)). In the series-compensated case of Fig. 5–15 (b), the commutating voltage almost levels out as soon as the incoming-phase thyristor is fired. This is because of the drop in the SPVC-injected voltage (caused by the discharge of the SPVC DC-link capacitor). This makes the commutation interval longer and is responsible for reduced harmonic content in the summed-up current on the primary side of the converter transformers. This will be discussed in detail later.

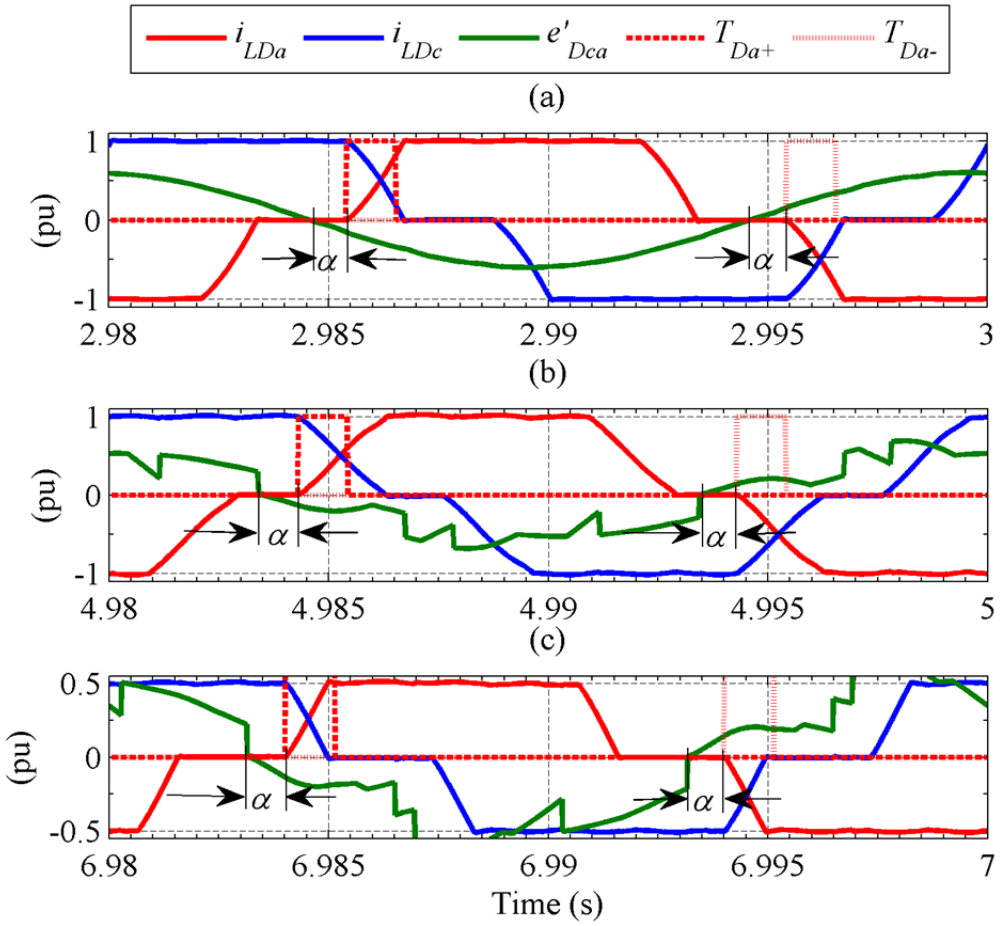

Fig. 5–15. Current commutation from phase *c* to *a* in the *D* branch (a) without SPVC, (b) with SPVC at full load, and (c) with SPVC at 0.5-pu load.

When the load is reduced, the commutation interval appears to be reduced as well, as seen in Fig. 5–15 (c). Even though, the commutating voltage levels out, the stored energy in the leakage reactance of the converter transformer is exchanged quickly between the phases resulting into reduced commutation interval and worse harmonic characteristics. However, this commutation interval is still longer than those in the uncompensated case as seen in Fig. 2–11 and CCC HVDC case presented in Fig. 3–8.

The grid-side currents for the case with full compensation at full load in the *D* branch primary, *Y* branch primary, total into the two converter transformers, the filter current, and the grid current are plotted in Fig. 5–16 (a), (b), (c), (d), and (e) respectively. Refer to Fig. 2–12 and Fig. 3–9 for comparison with the conventional shunt compensator and full compensation with CCC HVDC. The phase difference between the primary phase voltage and the line current is almost zero. Therefore, the entire terminal appears to be reactive-power neutral to the filter bus. The system can afford smaller converter transformers as there is no need to over-size the transformer for additional reactive-power flow and additional insulation for higher voltages required for that flow. The current i_{sa} appears to have lesser harmonic content than the uncompensated and CCC HVDC case. This is also backed by the waveform of i_{fa} which has a relatively smaller harmonic content on top of a large fundamental frequency component.

The same plots are repeated in Fig. 5–17 for 0.5-pu load. The current and voltage in the respective phase are in phase and thus no reactive power is flowing into the converter transformers. This was not achieved using CCC HVDC as has been observed in Fig. 3–10.

Clearly, the harmonic content has increased in proportion to the fundamental when compared to the full-load case. This however is better than the uncompensated case as well as the partial-compensation case with the CCC and GCSC compensators. The filter supplies the harmonic demand and the grid current is free of harmonics.

The instantaneous voltage appearing across the thyristors in the main AC/DC conversion bridges in the *D* and *Y* branch are plotted in Fig. 5–18 (a) and (b) respectively. Comparison with the GCSC, CCC, and the conventional shunt-compensated cases reveals that the voltage stress on the thyristor does not increase. The harmonic content in the voltage however increases.

The voltages appearing across single switches in the SPVC for full and 0.5-pu active power are plotted in Fig. 5–19 (a) and (b) respectively. This blocking voltage forms the basis for voltage rating for the proposed compensators. It can be seen that maximum voltage appears across these switches at full load and with full compensation. This voltage is of the order of 0.3 pu.

The SPVC injects voltages of both polarities, but the SPVC DC-link voltage does not change polarity; which is contrary to what happened with the fixed series capacitors and the GCSC. The SPVC would, therefore, work with polarized capacitors, which are compact as compared to non-polarized capacitors.

The SPVC-injected voltages in Fig. 5–13 (b) are 0.6 pu peak-to-peak. This is because, in the SPVC design, the voltage which contributes to the reversal of commutating voltage is injected into the incoming phase only; whereas, in the case of the GCSC, both the incoming- and outgoing-phase GCSCs contributed to it. However, the peak voltage on the SPVC DC-link capacitor is 0.3 pu, whereas the peak-to-peak voltage on the GCSC is 0.4 pu. This implies that the SPVC, in addition to the use of polarized capacitors, would use capacitors with lower peak-voltage ratings.

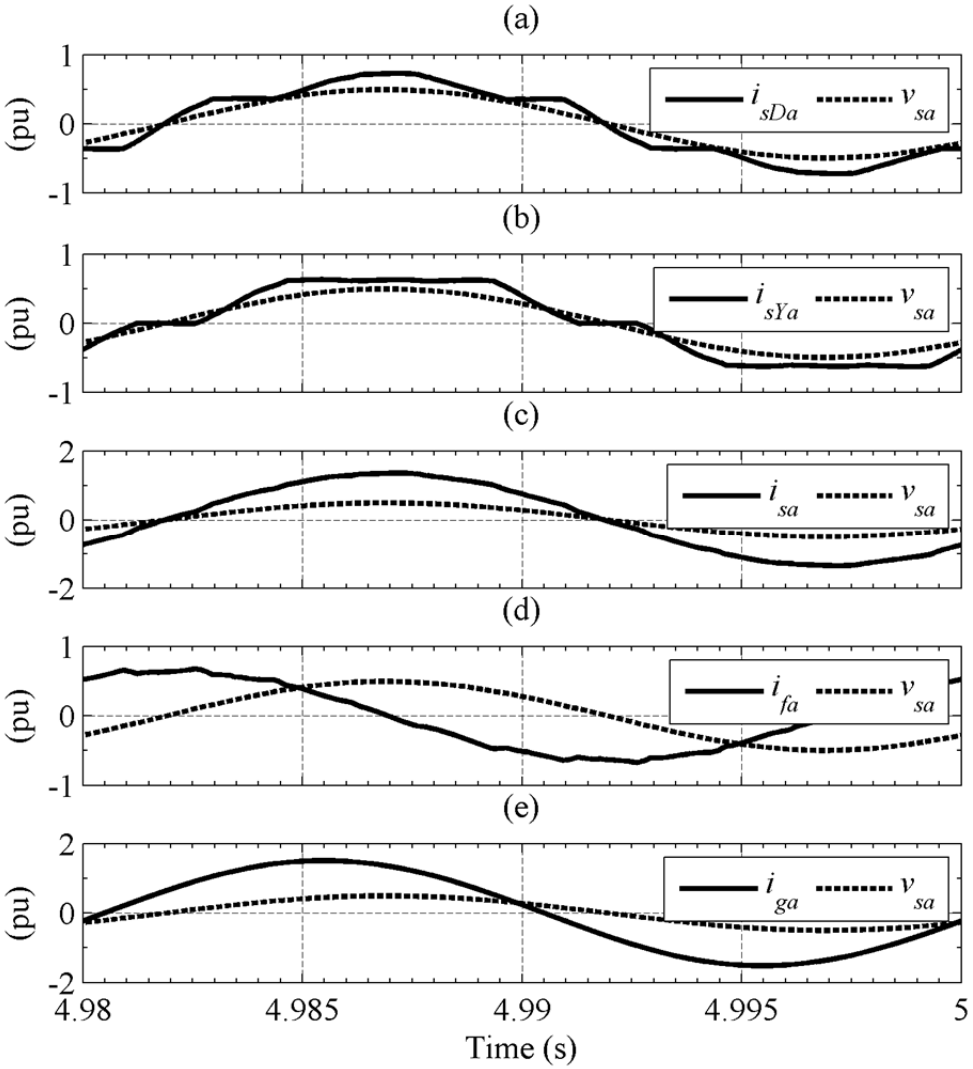

Fig. 5–16. Grid side current for phase *a* with full compensation at full load.

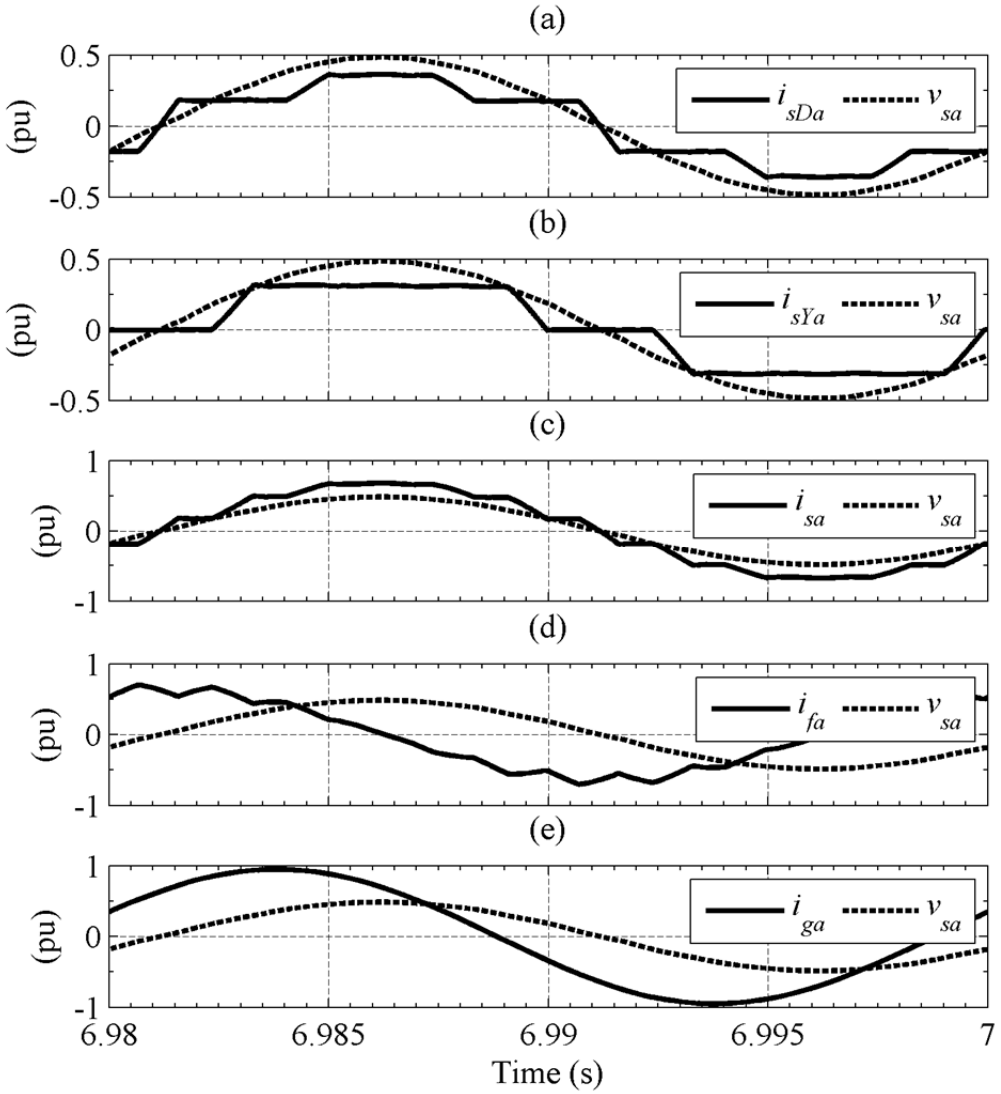

Fig. 5–17. Grid side current for phase *a* with full compensation at 0.5-pu load.

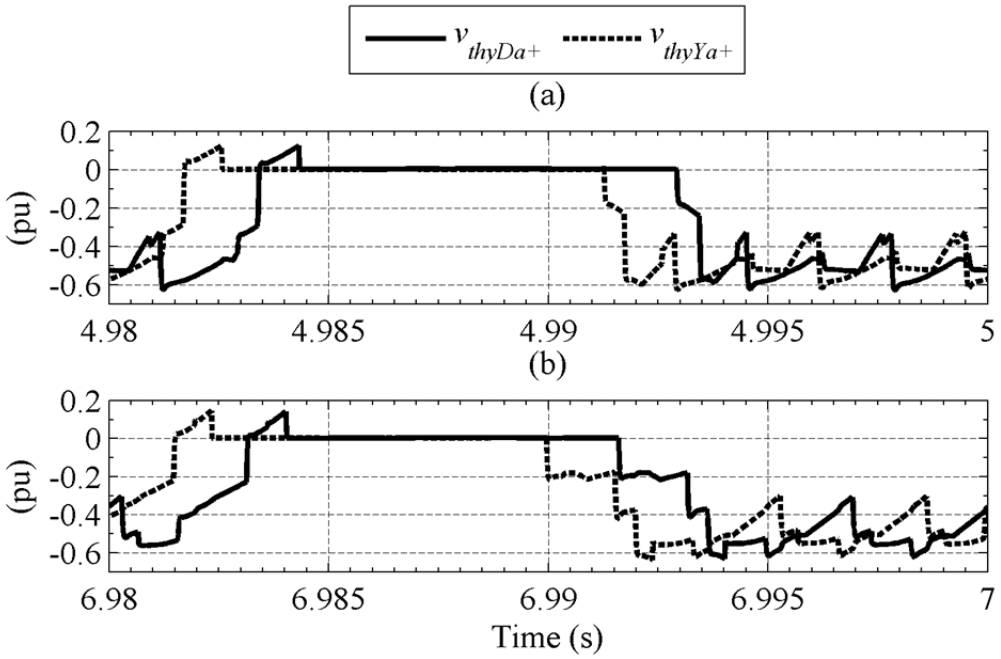

Fig. 5–18. Voltage appearing across one thyristors in the *D* and *Y* branches for (a) full load, and (b) 0.5-pu load.

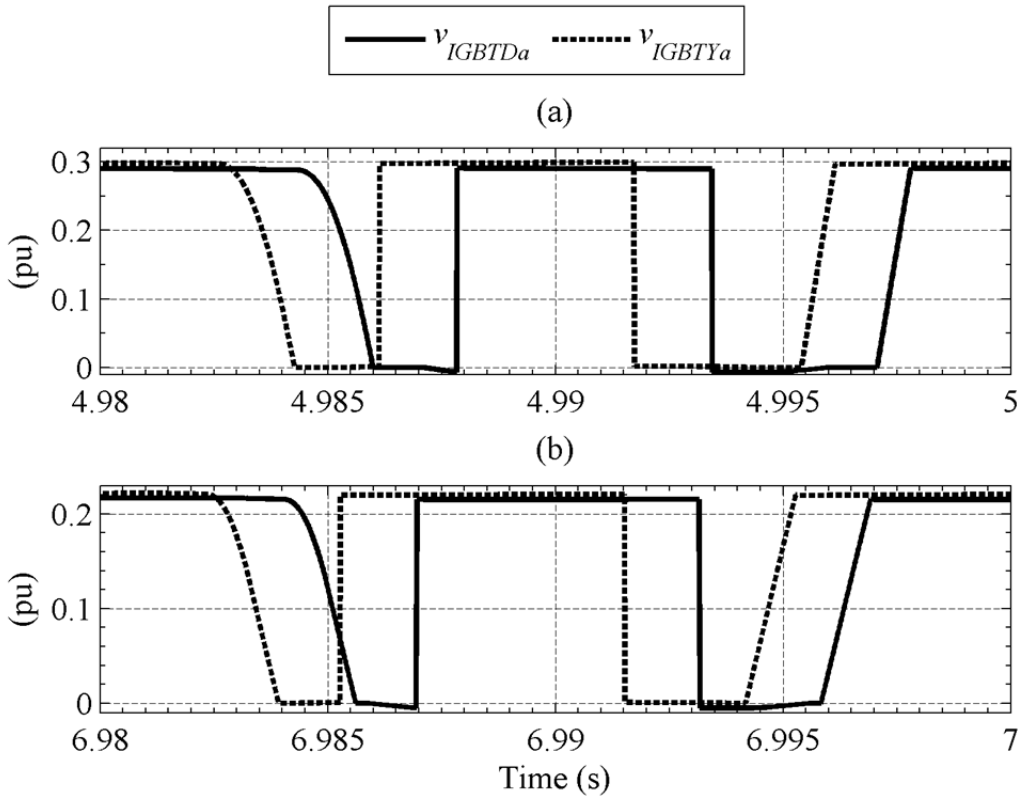

Fig. 5–19. Voltage appearing across one IGBT in the *D* and *Y* branches for (a) full load, and (b) 0.5-pu load.

5.5.4 Current Harmonics

The harmonic spectra for i_{lDa} and i_{sDa} at 1-pu active-power flow are plotted in Fig. 5–20 (a) and (b) respectively. A comparison with the conventional shunt compensated HVDC, CCC HVDC, and the GCSC shows that the THD value has gone down by more than 5% from the minimum value in those cases. Similarly, the harmonic content is smaller for 0.5-pu active-power flow in i_{lDa} and i_{sDa} (plotted in Fig. 5–21 (a) and (b) respectively) as compared to all the topologies discussed in the preceding chapters.

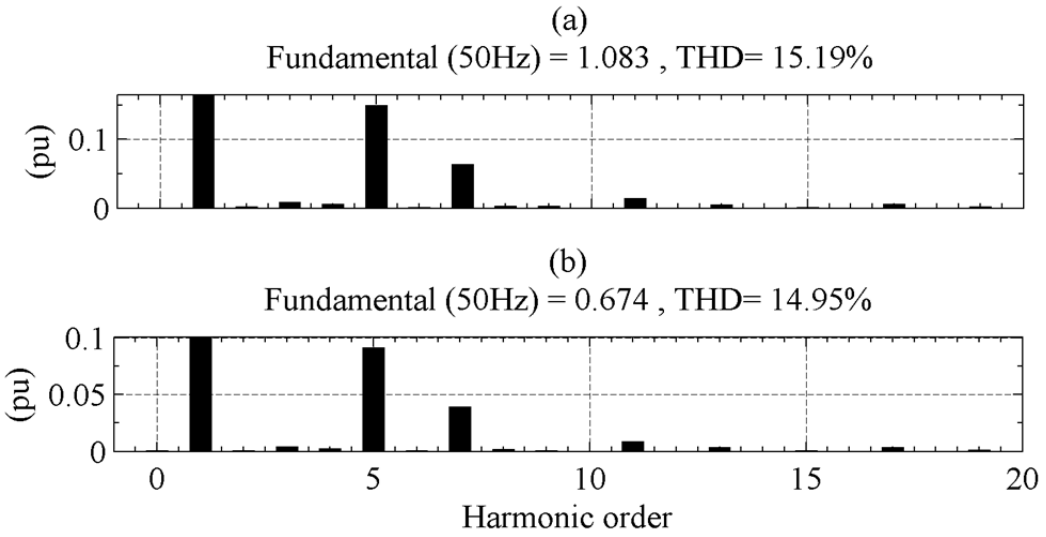

Fig. 5–20. Harmonic spectra for 1-pu power flow (a) i_{lDa} (b) i_{sDa}.

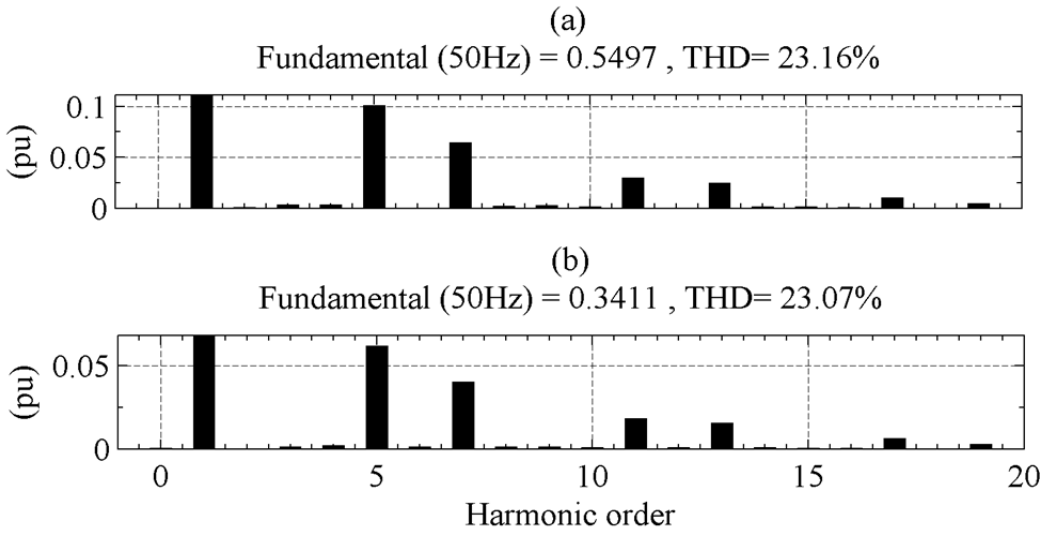

Fig. 5–21. Harmonic spectra for 0.5-pu power flow (a) i_{lDa} (b) i_{sDa}.

Even though, the THD value has gone up to 23% from 15% in the rated-power case with the SPVC, it is still lower than half-power THDs in the case of conventional shunt, CCC, and GCSC cases. Similar comparisons can be made about i_{lYa} and i_{sYa} for

rated- and half-power cases, the harmonic spectra for which are plotted in Fig. 5–22 and Fig. 5–23 respectively.

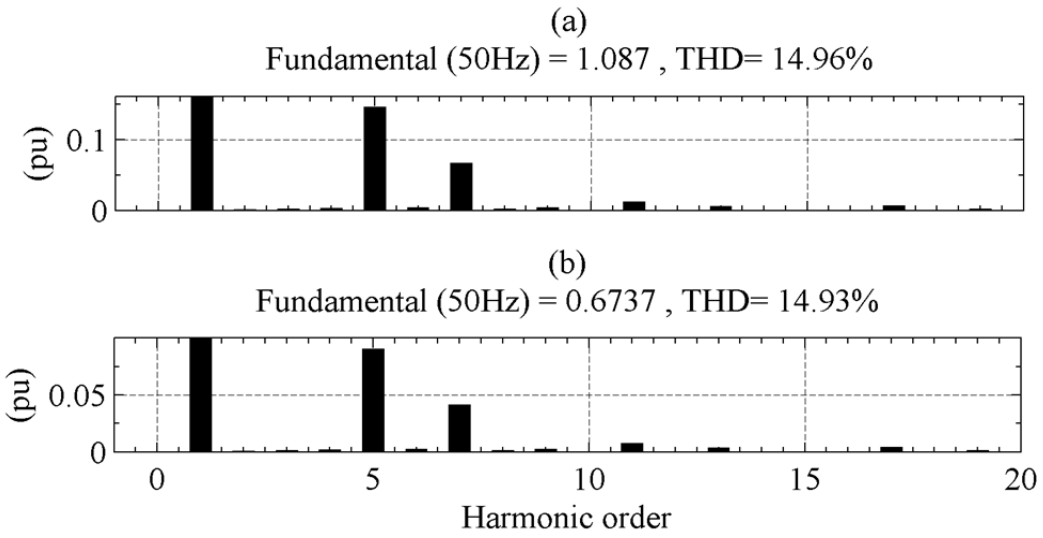

Fig. 5–22. Harmonic spectra for 1-pu power flow (a) i_{lYa} (b) i_{sYa}.

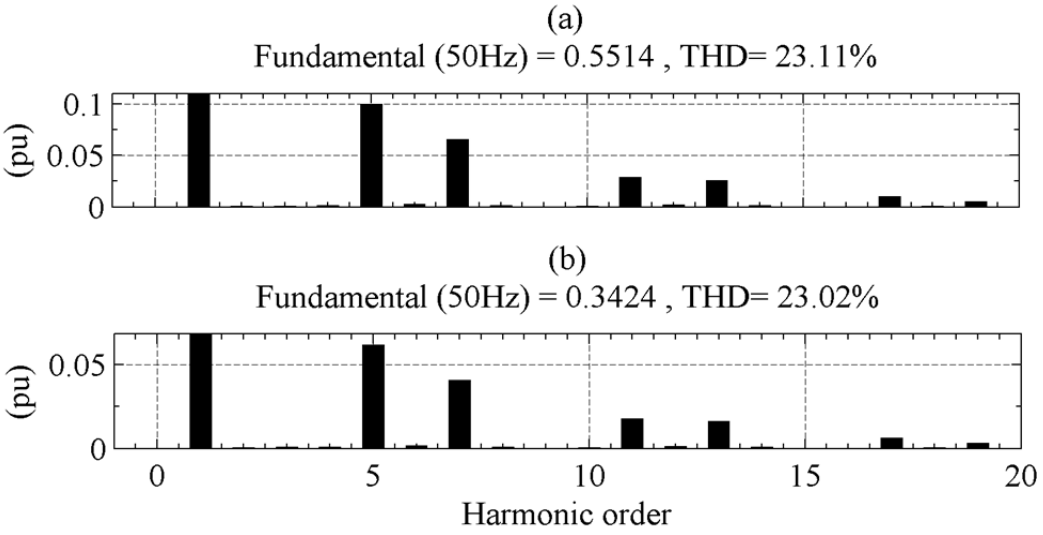

Fig. 5–23. Harmonic spectra for 0.5 pu power flow (a) i_{lYa} (b) i_{sYa}.

The harmonic spectra of aggregated line current, the filter current, and the grid current in phase *a* are given in Fig. 5–24 (a), (b), and (c) respectively. The THD for i_{sa} is 1.64%, well below that in the case of the shunt-compensated, CCC, and the GCSC. The magnitudes of the 11^{th} and the 13^{th} harmonics are smaller when compared to the same in the other topologies. This results into a smaller current requirement at the specific harmonic frequency requiring smaller tuned filters. The harmonic spectra for i_{sa}, i_{fa}, and i_{ga} at 0.5-pu load are presented in Fig. 5–25 (a), (b), and (c) respectively. Again, the THD is smaller than the other topologies. The consequence is a smaller current requirement on the shunt filter requiring smaller components and lower losses.

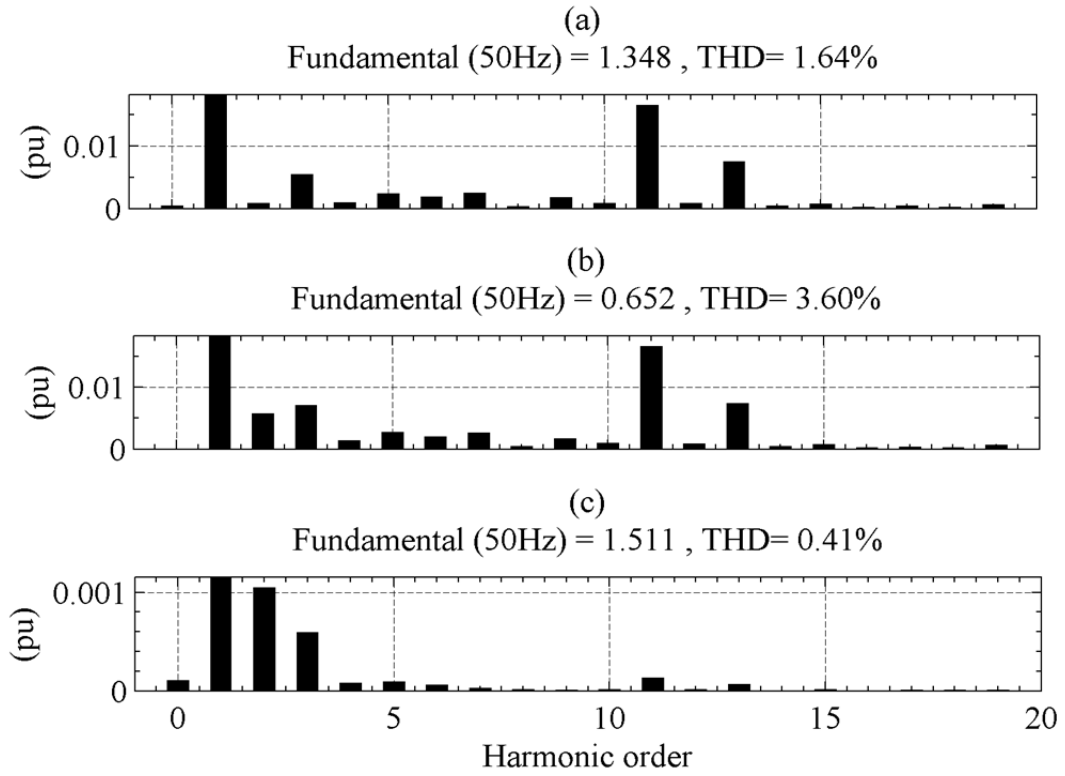

Fig. 5–24. Harmonic spectra for 1-pu power flow (a) i_{sa}, (b) i_{fa}., and (c) i_{ga}.

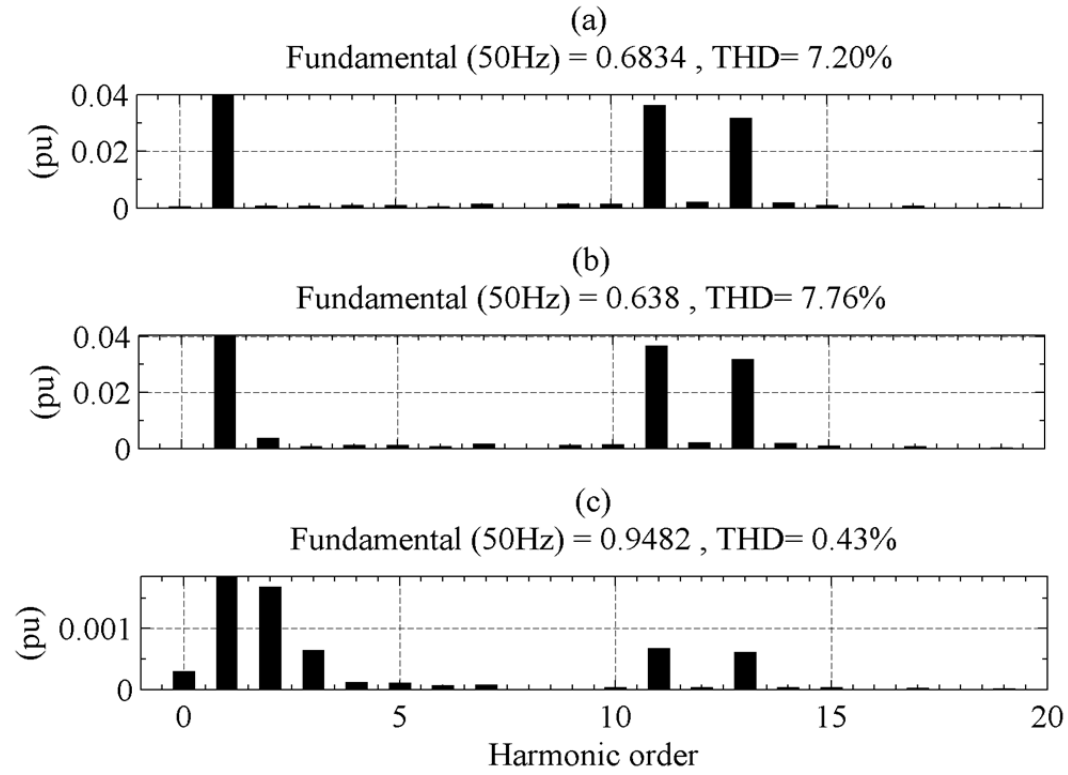

Fig. 5–25. Harmonic spectra for 0.5-pu power flow (a) i_{sa}, (b) i_{fa}., and (c) i_{ga}.

5.5.5 Instantaneous Power

The instantaneous powers at different locations in the system for 1-pu active-power flow are presented in Fig. 5–26. The oscillations in p_g are much smaller in magnitude when compared to the respective plots in all other topologies. The introduction of the SPVC has increased the number of pulses in p_{lD} and p_{lY}. This has transformed the behaviour of this 12-pulse HVDC arrangement almost into an equivalent 24-pulse arrangement, thus driving the lowest significant harmonic to the 23rd and 25th instead of the 11th and the 13th. In a sense, the SPVC is performing instantaneous power compensation [103].

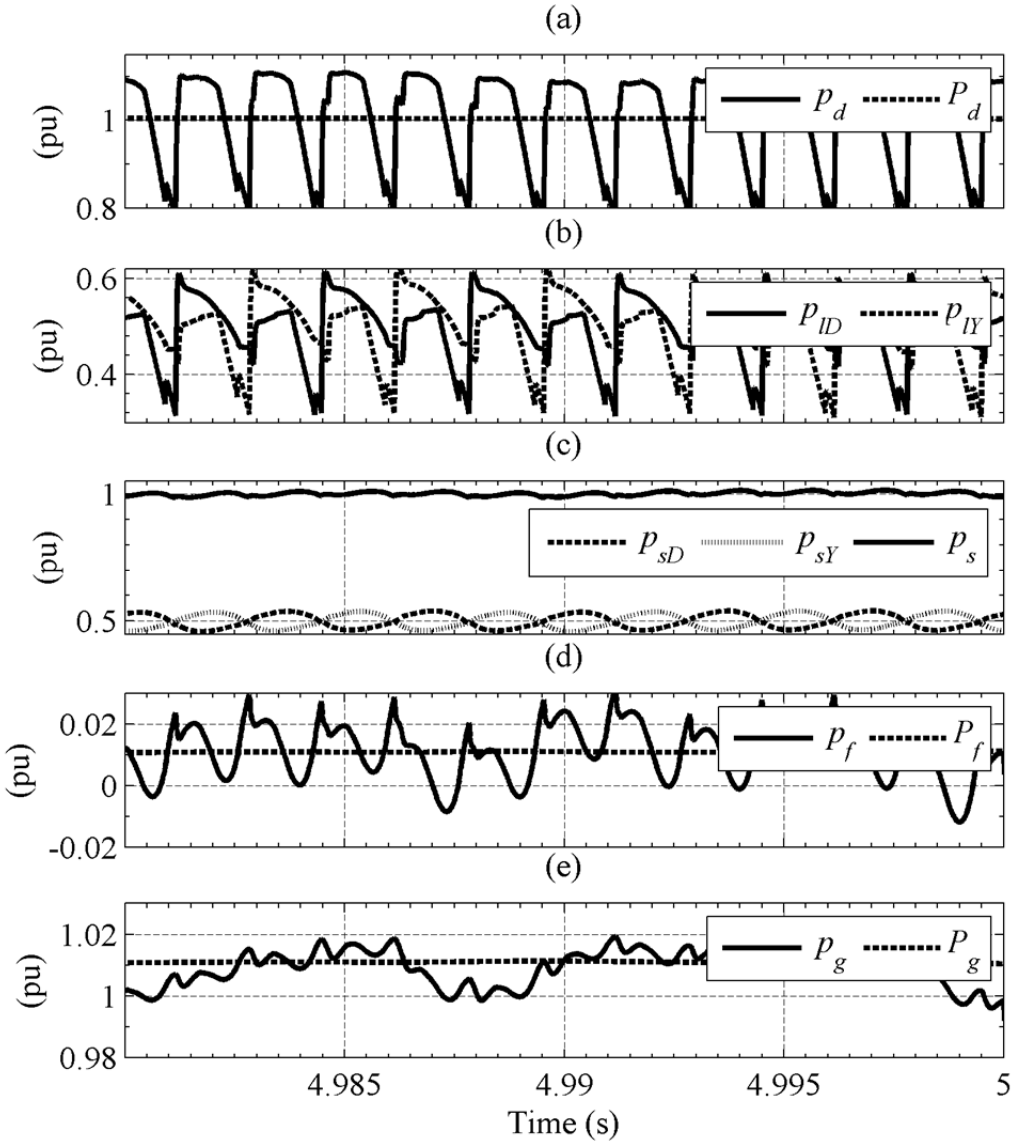

Fig. 5–26. Instantaneous powers at 1-pu active-power flow at different locations in the system with SPVC.

The instantaneous powers at 0.5-pu active-power flow are shown in Fig. 5–27. Similar observations can be made when compared with other approaches. The ripple in p_s is somewhat larger than that in the 1-pu active-power case. This is why the 11th and 13th harmonics for 0.5-pu active power were reported to be higher in the preceding section than those with 1-pu active power.

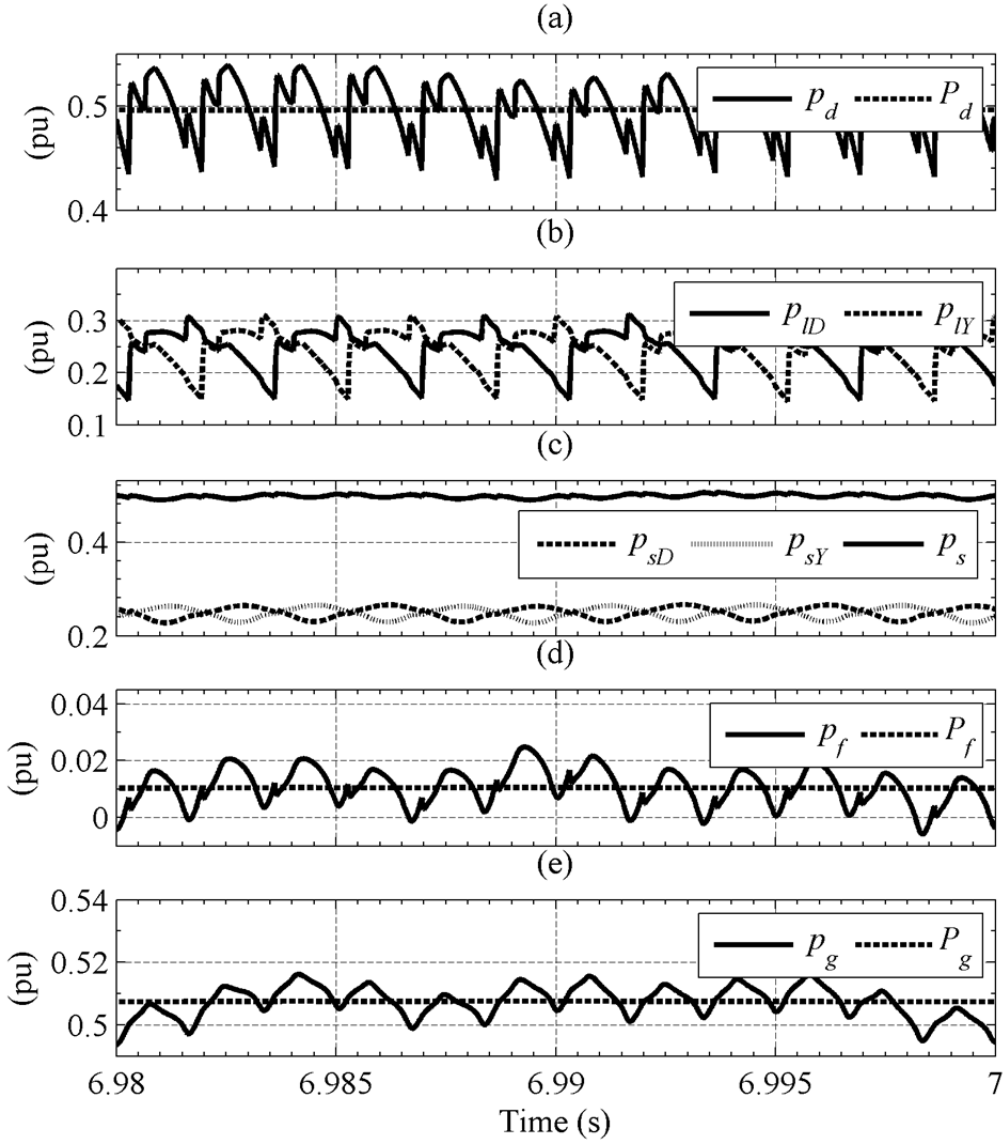

Fig. 5–27. Instantaneous powers at 0.5-pu active-power flow at different locations in the system with SPVC.

5.6 Simulation Results for Case II

5.6.1 Active and Reactive Powers

The active and reactive powers for this case are plotted in Fig. 5–28. With reference to Fig. 5–28 (a), P_s remains at 1 pu throughout the simulation and Q_{sR} changes at 3 s, when the SPVC is activated, to 0 pu as per the command to the SPVC. Q_{sR} is changed to 0.3 pu at 5 s, and the SPVC successfully follows the reference as it rises to a new steady-state value of 0.3 pu.

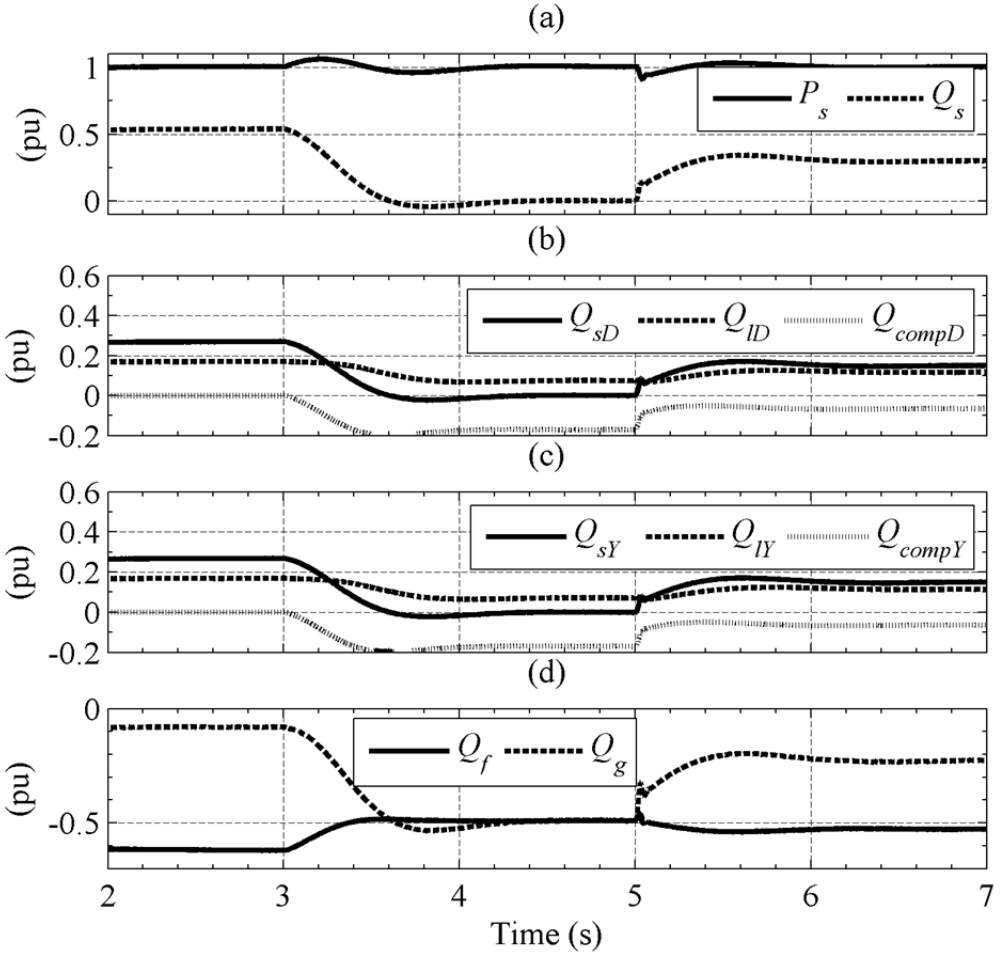

Fig. 5–28. Active and reactive power behaviour for case II.

The individual reactive powers of the *D* and *Y* branches are plotted in Fig. 5–28 (b) and (c) respectively. Both are identical and are at their steady-state values before the start of series compensation. After the SPVC is connected at 3 s, Q_{sD} and Q_{sY} drop to 0 pu and Q_{compD} and Q_{compY} attain values to nullify the reactive power consumed by the converter terminal and the converter-transformer leakage reactance. At 5 s, Q_{sR} is stepped up to 0.3 pu and the compensator changes the injected voltage magnitude and phase to attain a value of 0.3 pu for Q_s.

The important observation to make here is the reduction in Q_{lD} and Q_{lY}, as the SPVC is connected. With Q_{sR} equal to 0 pu, Q_{lD} and Q_{lY} drop to less than half of their pre-series-compensation values. Thus, the reactive-power contribution from the SPVC is smaller than in the case of CCC HVDC and the GCSC, as there was no change observed in Q_{lD} and Q_{lY} when the other compensators were connected. After the change in Q_{sR}, the compensator adjusts its voltage injection magnitude and phase to influence the reactive-power consumption of the converter terminals and thereby bring Q_s to 0.3 pu.

Finally, Q_f is utilized to compensate for Q_s before the start of series compensation. After the addition of the SPVC, the entire amount of reactive power becomes surplus and is exported to Q_g. However, after the change in Q_{sR}, a part is exported to the grid and the rest is supplied to the converter terminal.

5.6.2 Control Loop Operation

The satisfactory behaviour of the control loops for α control, AC-voltage control, and $v_{compdcjR}$ is depicted in Fig. 5–29 (a), (b), and (c) respectively. $v_{compdcDR}$ and $v_{compdcYR}$ (panel (c)) behave identically in the case of full and partial compensation.

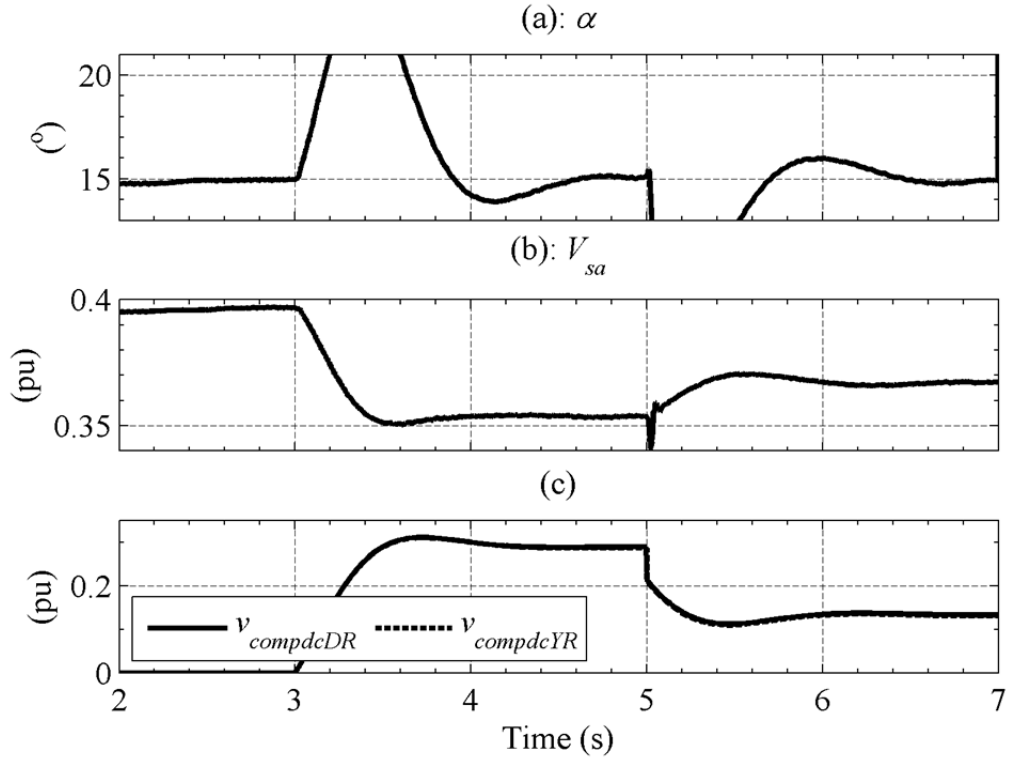

Fig. 5–29. Control loop behaviour for case II.

5.6.3 Instantaneous Currents and Voltages

The instantaneous current and voltages in phase *a* on the converter side in the *D* branch are plotted in Fig. 5–30. Panel (b) and (c) are identical to Fig. 5–13 (a) and (b) and need no further discussion. Panel (c) shows the instant when the reactive power demand on the compensator is relaxed, hence a smaller voltage is injected as compared to the full compensation case. This results into a larger phase difference between e_{Da} and i_{lDa}, indicative of non-zero reactive-power consumption in this case.

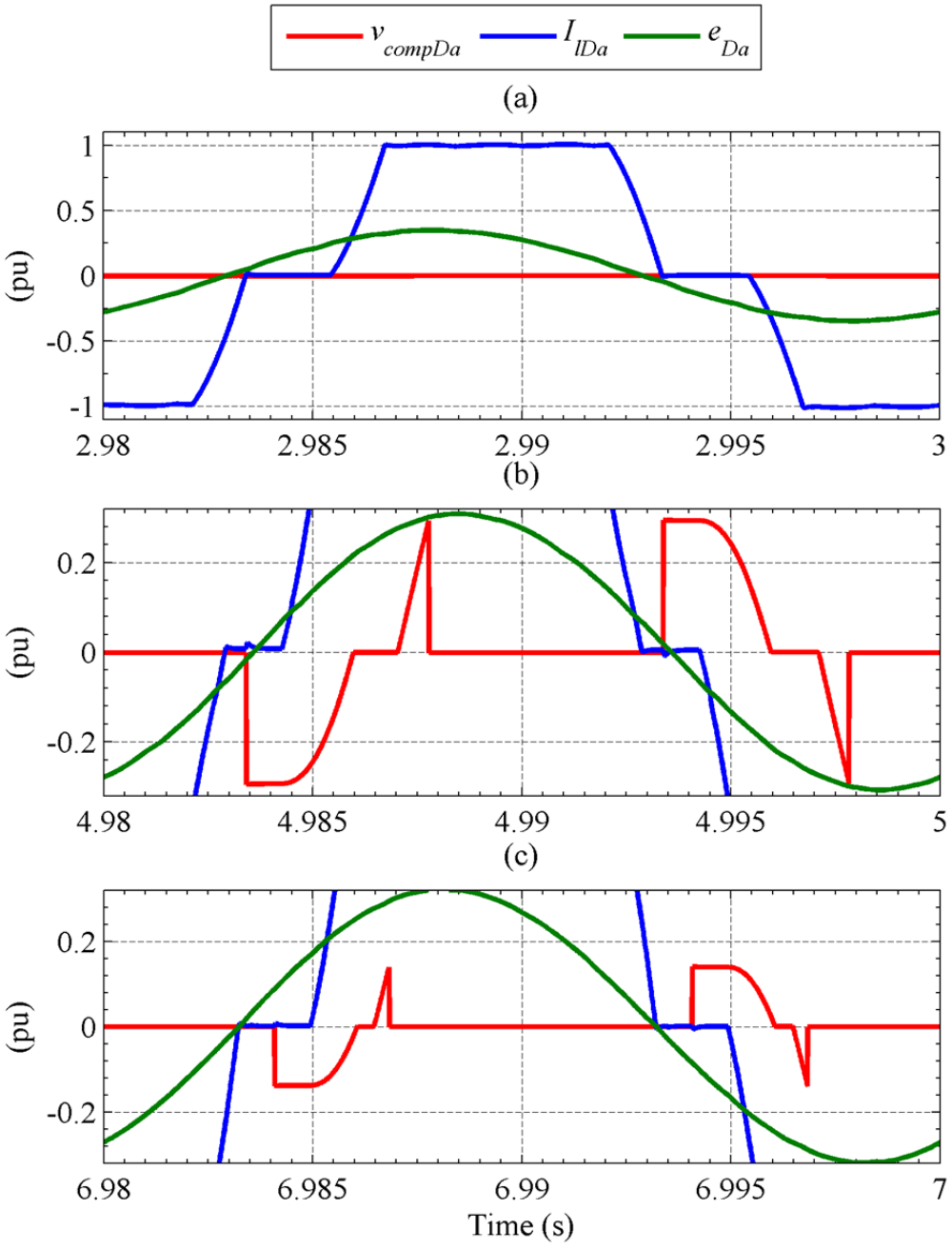

Fig. 5–30. Instantaneous currents and voltages on the converter side (a) without-, (b) with full, and (c) with partial compensation.

The commutating voltages for the first two periods for case II (i.e. without and with full compensation) are identical to those in case I (plotted in Fig. 5–14 (a) and (b)). The same is plotted in Fig. 5–31 for the period with partial compensation.

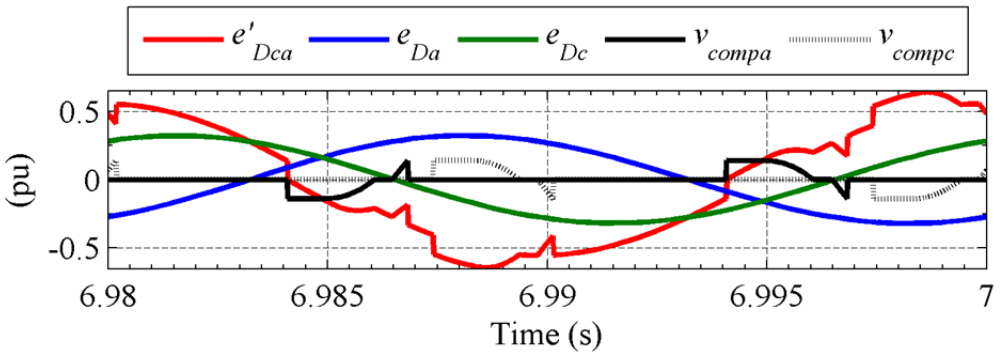

Fig. 5–31. Commutating voltage for case II with partial compensation.

As can be seen, the commutating voltage crosses over when the difference between the two phase voltages is smaller as compared to the case with full compensation. This wave-shape of the commutating voltage is attributable to the series voltage injection in phase *a* and phase *c*.

The mechanism of current commutation for the case with partial compensation is depicted in Fig. 5–32. It is similar to the plots for case I (shown in Fig. 5–15). The difference is the smaller voltage injected in case II as compared to case I.

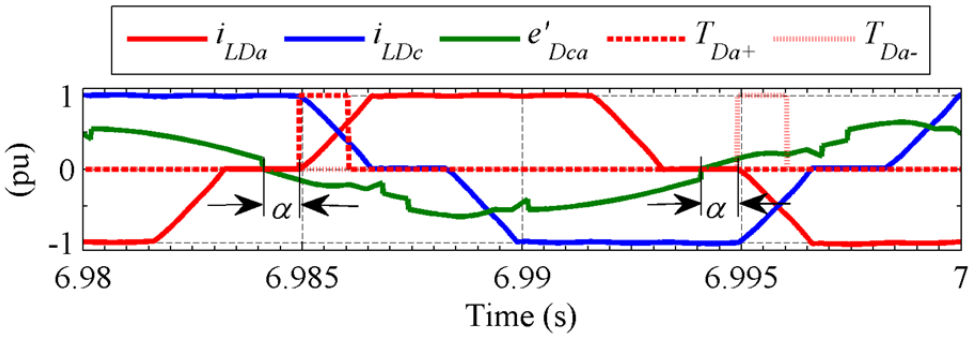

Fig. 5–32. Current commutation from phase *c* to *a* for case II with Q_{sR} = 0.3 pu.

The grid-side currents for the first two intervals of case II are similar to those in case I. These currents for partial compensation are plotted in Fig. 5–33. There is a distinct phase difference between the individual branch currents as well as their sum with respect to the concerned phase voltage. This is because partial compensation is being done.

The blocking voltages that appear across the thyristors in the main AC/DC converter bridges and IGBTs are plotted in Fig. 5–34 (a) and (b) respectively for the duration with partial compensation. It is to be noted that the voltage rating of the SPVC is directly dependant on the amount of compensation being done by it. It is known that

the CCC HVDC employs a hybrid approach for reactive/harmonic compensation, where part of reactive-compensation requirement is provided by the capacitors, thereby limiting their size and voltage rating. This can be done in the SPVC as well where lighter passive filters would work in conjunction with the proposed compensator.

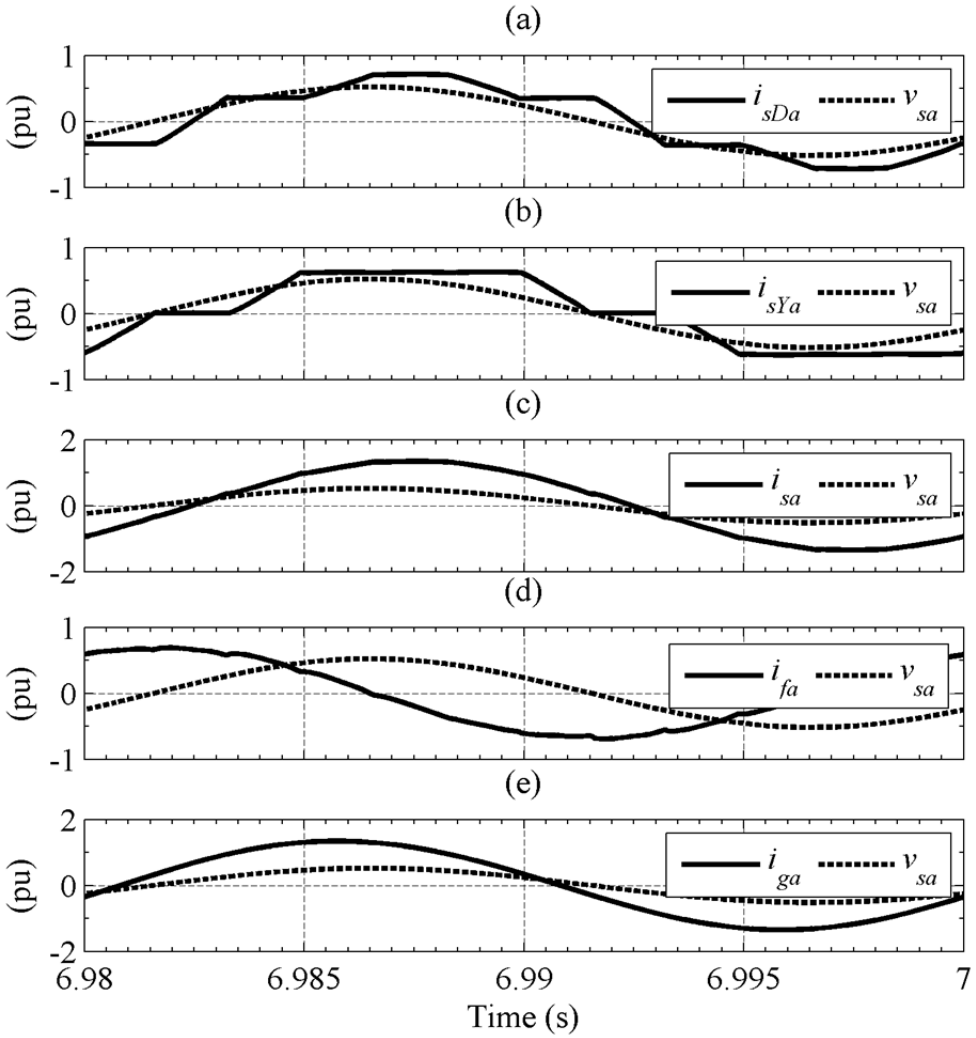

Fig. 5–33. Grid side current for phase *a* for case II with Q_{sR} = 0.3 pu.

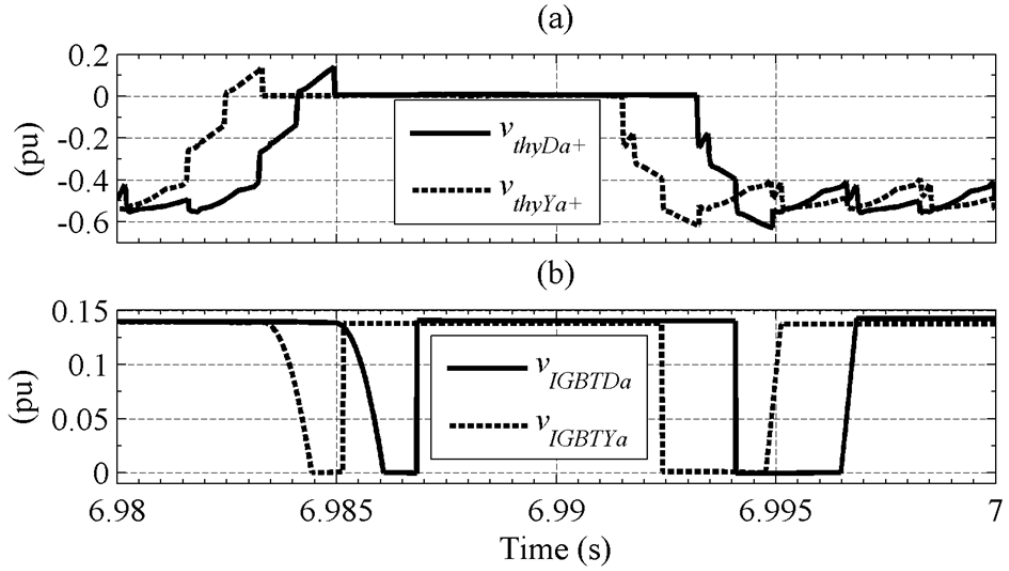

Fig. 5–34. Blocking voltages for phase *a* for case II with Q_{sR} = 0.3 pu.

5.6.4 Current harmonics

The current harmonics for 1-pu active power and Q_{sR} = 0 pu have been presented already in section 5.5.4. The harmonic picture for Q_{sR} = 0.3 pu is being presented here.

Harmonic spectra of i_{lDa} and i_{sDa} are depicted in Fig. 5–35 (a) and (b) respectively. The THD figure as well as the amplitude of significant harmonics seems to increase, when compared to the harmonics for full reactive compensation (Fig. 5–20 (a) and (b)). The corresponding harmonic spectra for the *Y* branch are shown in Fig. 5–36 and present a similar rise in THD and low-order harmonic magnitudes, when compared to the full-compensation case (Fig. 5–22). Finally, the frequency spectra of the total current into the converter transformers, the shunt passive filter current, and the grid current are depicted in Fig. 5–37 (a), (b), and (c) respectively. A comparison with Fig. 5–24 reveals that the harmonic performance has improved further. The THD in i_{sa} decreases to 1.25% from 1.64% which means further reduction in the requirements on the shunt passive filter. This leads us to deduce that the worst-case scenario where maximum harmonic compensation may be required from the shunt passive filter is when the SPVC is providing full reactive compensation at rated active-power flow.

5.6.5 Instantaneous Power

The instantaneous powers at different points in the system for the instance with Q_{sR} = 0.3 pu are depicted in Fig. 5–38. The ripple in p_d in panel (a) is reduced when compared to the case with full compensation in Fig. 5–26 (a).

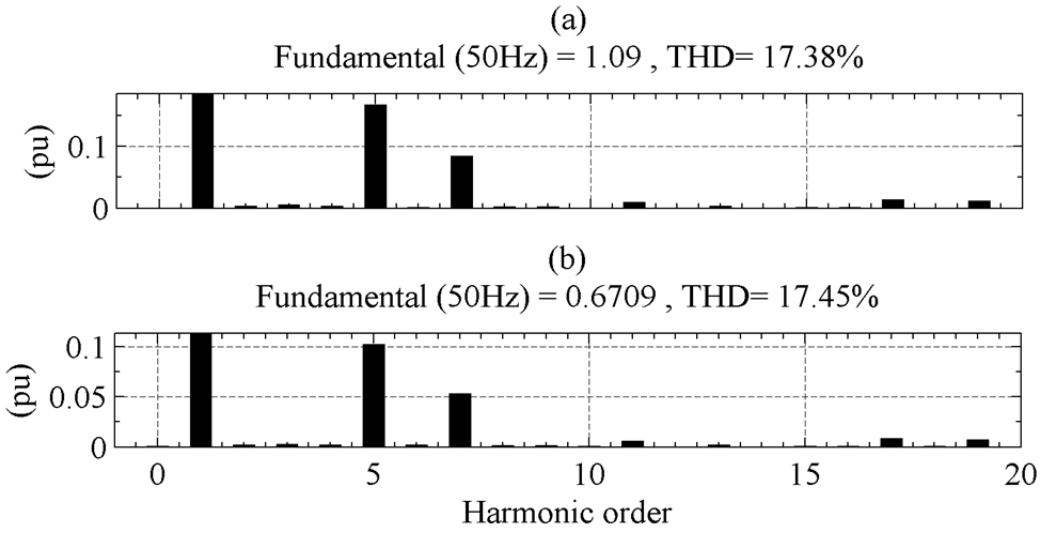

Fig. 5–35. Harmonic spectra with Q_{sR} = 0.3 pu. (a) i_{lDa}, and (b) i_{sDa}.

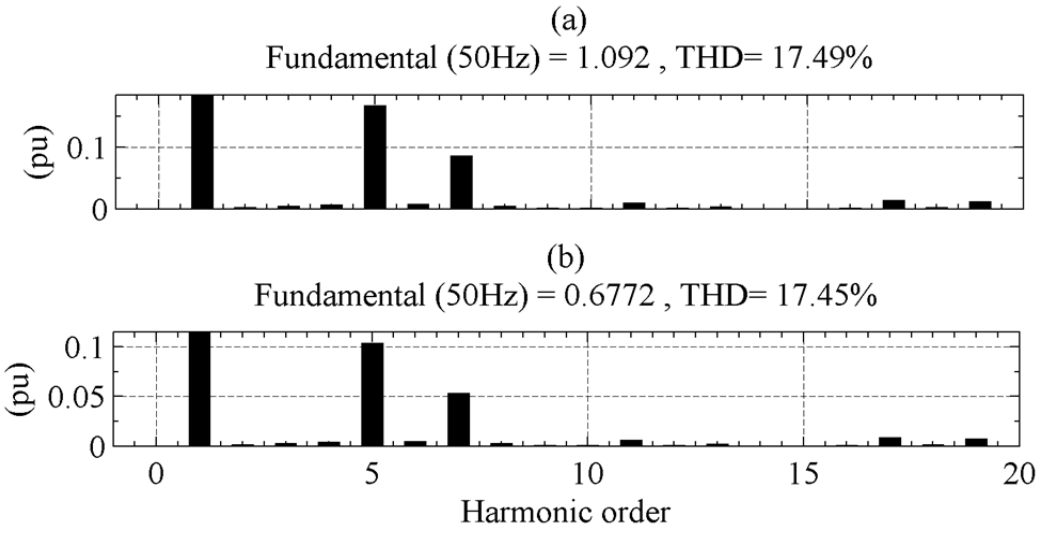

Fig. 5–36. Harmonic spectra with Q_{sR} = 0.3 pu. (a) i_{lYa}, and (b) i_{sYa}.

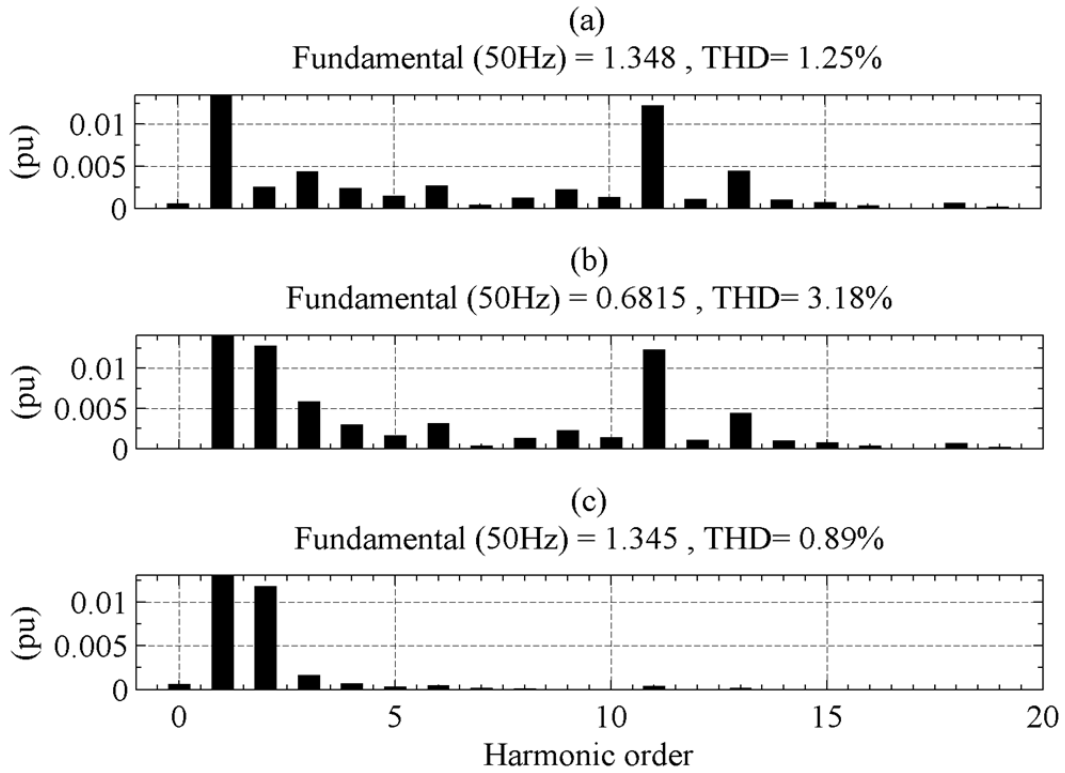

Fig. 5–37. Harmonic spectra with Q_{sR} = 0.3 pu. (a) i_{sa}, (b) i_{fa}, and (b) i_{ga}.

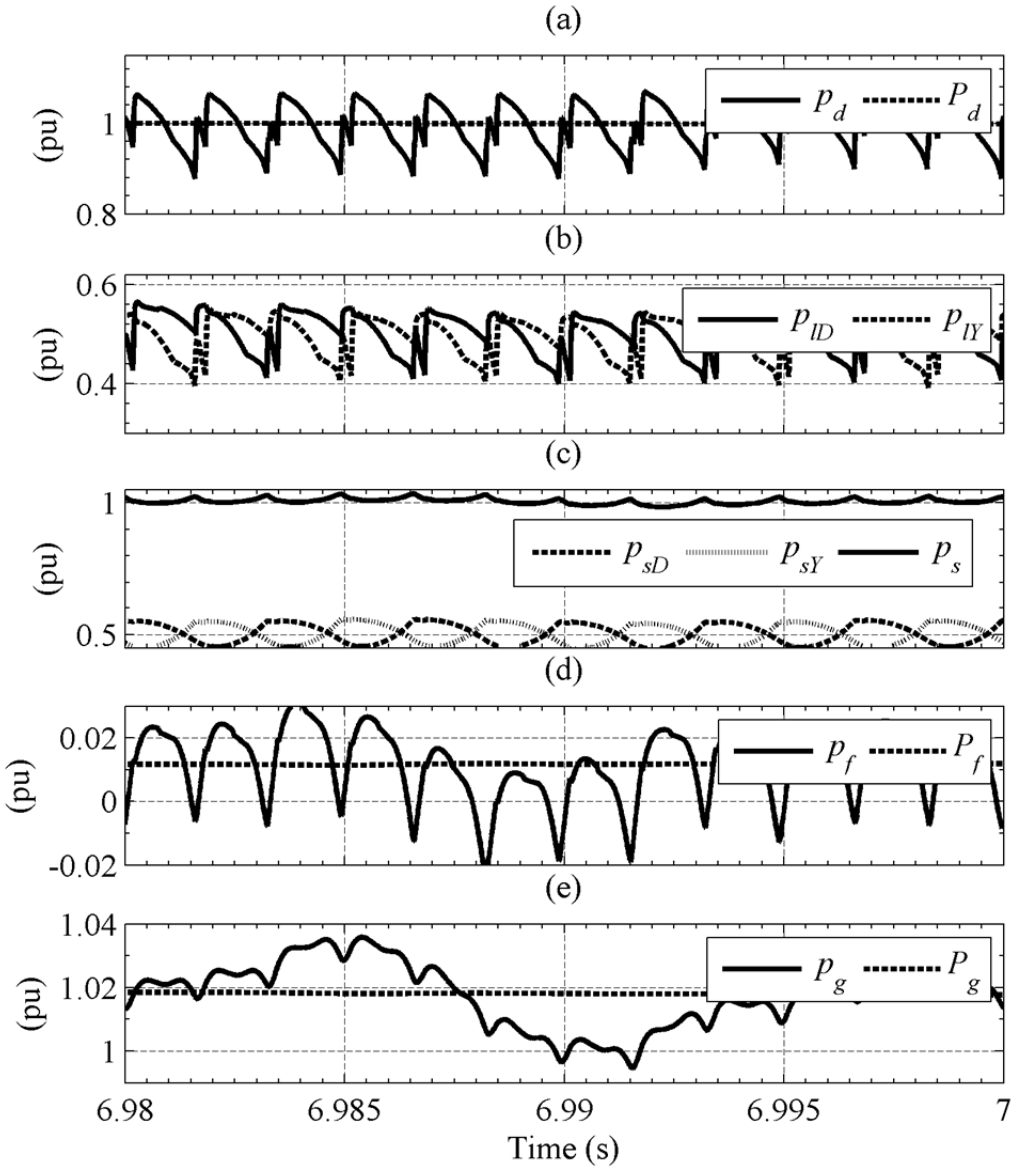

Fig. 5–38. Instantaneous powers at 1-pu active power and partial reactive-power compensation at different locations in the system with the SPVC.

5.7 Comparison of Harmonic Figures

The important harmonic numbers for the *D*-branch currents for all the topologies discussed up to this point are listed in TABLE 5–1, with the figures for the SPVC listed in the right-most column. The column header is "SPVC1", where "1" refers to the injection strategies implemented in simulations in this chapter. The succeeding chapter discusses another strategy for the control of the SPVC, and similar tables in the said chapter will have "SPVC2" as the column header. The THD in i_{lDa} at 1-pu active power and full reactive compensation is reduced significantly with the SPF approach. There is a reduction of almost 25%. Obviously, the THD advantage is much higher when compared to the CCC and GCSC topologies. Similarly, the magnitudes of significant

harmonics is reduced significantly in comparison with the all the other topologies. A pattern of rising harmonic benefit is observed with increasing harmonic number. For instance, the ratio of the 5^{th} harmonic magnitudes with SPF and SPVC1 is 0.8086, 0.5534 for the 7^{th} harmonic, 0.3714 for the 11^{th} harmonic, and 0.2236 for the 13^{th} harmonic.

TABLE 5–1
Important Harmonic Figures in The *D* Branch

	P_s (pu)	Parameter	Value SPF	CCC	GCSC	SPVC1
i_{lDa}	1	THD (%)	20.40	21.02	22.99	15.19
		5^{th} (pu)	0.1855	0.1905	0.1995	0.1500
		7^{th} (pu)	0.1151	0.1180	0.1341	0.0637
		11^{th} (pu)	0.0377	0.0430	0.0612	0.0140
		13^{th} (pu)	0.0246	0.0275	0.0440	0.0055
	0.5	THD (%)	24.54	24.93	25.62	23.16
		5^{th} (pu)	0.1035	0.1048	0.1054	0.1014
		7^{th} (pu)	0.0710	0.0710	0.0731	0.0647
		11^{th} (pu)	0.0379	0.0393	0.0418	0.0301
		13^{th} (pu)	0.0276	0.0279	0.0307	0.0247
	1 par.	THD (%)	-	-	21.53	17.38
		5^{th} (pu)	-	-	0.1940	0.1677
		7^{th} (pu)	-	-	0.1201	0.0846
		11^{th} (pu)	-	-	0.0480	0.0098
		13^{th} (pu)	-	-	0.0312	0.0032
i_{sDa}	1	THD (%)	20.28	20.92	23.09	14.95
		5^{th} (pu)	0.1147	0.1189	0.1239	0.0919
		7^{th} (pu)	0.0712	0.0718	0.0824	0.0392
		11^{th} (pu)	0.0230	0.0272	0.0384	0.0090
		13^{th} (pu)	0.0151	0.0166	0.0268	0.0038
	0.5	THD (%)	24.25	24.43	26.09	23.07
		5^{th} (pu)	0.0640	0.0650	0.0652	0.0622
		7^{th} (pu)	0.0442	0.0435	0.0453	0.0405
		11^{th} (pu)	0.0231	0.0246	0.0258	0.0185
		13^{th} (pu)	0.0171	0.0170	0.0191	0.0157
	1 par.	THD (%)	-	-	21.41	17.45
		5^{th} (pu)	-	-	0.1194	0.1030
		7^{th} (pu)	-	-	0.0745	0.0534
		11^{th} (pu)	-	-	0.0293	0.0059
		13^{th} (pu)	-	-	0.0193	0.0023

For 0.5-pu power flow, the THD increases to a little less than that with the SPF with the significant-harmonic magnitudes following suit. The harmonic benefit defined above does not exhibit the same increasing pattern as observed in the 1-pu active-power case.

The advantage for the 5th and the 11th harmonic is negligible, however, that for the 7th and 13th is higher.

The THD in i_{lDa} goes up to 17.38% when the SPVC is partially compensating for the reactive power. This value is still lower than the SPF topology. The magnitudes of the 5th and the 7th harmonics increase in comparison with those with full reactive compensation. However, the magnitudes of the 11th and the 13th harmonics are smaller than when the SPVC is fully compensating for the reactive power. The rate of reduction in the harmonic magnitudes is even higher than that with the SPVC compensating for the entire reactive-power demand.

The comments above also apply to the numbers for i_{sDa} flowing in the primary winding of the converter transformer. The same pattern is observable in the numbers for the *Y*-branch currents, i_{lYa} and i_{sYa}, as seen in TABLE 5–2.

The important harmonic numbers for i_{sa} are presented in TABLE 5–3. The THD with the SPVC is only 1.64% against 4.31% with the SPF. This is an improvement of 61.95%. The 5th and the 7th harmonics are diminished like all other topologies. However, due to the reduced magnitudes of the 11th and the 13th harmonics in i_{sDa} and i_{sYa} (reported above), the magnitudes of the same harmonics in i_{sa} are much smaller as compared to the SPF measurements. The advantage factor for the 11th harmonic is 0.3532, and 0.2600 for the 13th harmonic. This is responsible for the large THD benefit with the SPVC approach. The THD as well as the magnitudes of the 11th and the 13th harmonics rise with 0.5 pu active power flow, as was observed during the discussion of the branch currents.

The THD for the case when the SPVC is partially compensating for the reactive power is 1.25%, a number which is even lower than 1.64% (THD when the SPVC was compensating for the entire reactive-power demand). The THD advantage now becomes 70.10% (from 61.95% with full compensation).This is because the magnitudes of the 11th and the 13th harmonics in i_{sDa} and i_{sYa} for the partial-compensation case were lower than those with full compensation. This is the reason for increased harmonic benefit with partial compensation.

The discussion above favours the use of partial compensation to reduce the harmonic load on the shunt passive filter. In a sense, it is similar to the approach followed in practical implementations of CCC HVDC; where the series capacitors compensate for a part of the reactive power with the rest being provided by smaller shunt passive filters. Allowing a specific flow of reactive power through the converter transformers would increase the size by a specific factor; however, lower harmonic flow through their windings would offer certain design benefits. A trade-off between transformer size and shunt-filter size is, therefore, evident. The reduction in the size of the shunt passive filter is most likely to outweigh the increase in the size of the converter transformer for handling more reactive power.

TABLE 5–2
Important Harmonic Figures in The *Y* Branch

	P_s (pu)	Parameter	Value			
			SPF	**CCC**	**GCSC**	**SPVC1**
i_{lYa}	1	THD (%)	20.56	20.99	23.09	14.96
		5^{th} (pu)	0.1882	0.1898	0.2023	0.1469
		7^{th} (pu)	0.1117	0.1188	0.1296	0.0669
		11^{th} (pu)	0.0388	0.0432	0.0634	0.0123
		13^{th} (pu)	0.0229	0.0282	0.0409	0.0060
	0.5	THD (%)	24.74	24.83	25.62	23.11
		5^{th} (pu)	0.1043	0.1038	0.1056	0.1005
		7^{th} (pu)	0.0697	0.0715	0.0725	0.0662
		11^{th} (pu)	0.0382	0.0391	0.0424	0.0291
		13^{th} (pu)	0.0264	0.0284	0.0298	0.0262
	1 par.	THD (%)	-	-	21.51	17.49
		5^{th} (pu)	-	-	0.1940	0.1683
		7^{th} (pu)	-	-	0.1191	0.0861
		11^{th} (pu)	-	-	0.0475	0.0103
		13^{th} (pu)	-	-	0.0302	0.0034
i_{sYa}	1	THD (%)	20.50	20.95	23.05	14.93
		5^{th} (pu)	0.1164	0.1174	0.1252	0.0909
		7^{th} (pu)	0.0691	0.0735	0.0802	0.0414
		11^{th} (pu)	0.0240	0.0267	0.0392	0.0076
		13^{th} (pu)	0.0142	0.0174	0.0253	0.0037
	0.5	THD (%)	24.61	24.72	25.52	23.02
		5^{th} (pu)	0.0646	0.0642	0.0653	0.0622
		7^{th} (pu)	0.0431	0.0442	0.0448	0.0410
		11^{th} (pu)	0.0237	0.0242	0.0263	0.0180
		13^{th} (pu)	0.0164	0.0175	0.0184	0.0162
	1 par.	THD (%)	-	-	21.45	17.45
		5^{th} (pu)	-	-	0.1200	0.1041
		7^{th} (pu)	-	-	0.0737	0.0533
		11^{th} (pu)	-	-	0.0294	0.0063
		13^{th} (pu)	-	-	0.0187	0.0021

TABLE 5–3
Important Harmonic Figures in the Combined Terminal Current

	P_s (pu)	Parameter	Value			
			SPF	CCC	GCSC	SPVC1
i_{sa}	1	THD (%)	4.31	4.87	6.97	1.64
		5^{th} (pu)	0.0027	0.0015	0.0021	0.0024
		7^{th} (pu)	0.0027	0.0021	0.0030	0.0025
		11^{th} (pu)	0.0470	0.0539	0.0776	0.0166
		13^{th} (pu)	0.0293	0.0340	0.0522	0.0075
	0.5	THD (%)	8.51	8.78	9.69	7.20
		5^{th} (pu)	0.0017	0.0008	0.0003	0.0011
		7^{th} (pu)	0.0015	0.0010	0.0006	0.0016
		11^{th} (pu)	0.0468	0.0487	0.0520	0.0365
		13^{th} (pu)	0.0334	0.0345	0.0375	0.0319
	1 par.	THD (%)	-	-	5.31	1.25
		5^{th} (pu)	-	-	0.0009	0.0015
		7^{th} (pu)	-	-	0.0009	0.0004
		11^{th} (pu)	-	-	0.0587	0.0123
		13^{th} (pu)	-	-	0.0379	0.0045

5.8 Conclusion

A new transformer-less series compensator has been introduced in this chapter. The details of its construction along with the control strategy have been provided. Simulation results have been presented demonstrating the capability of the proposed compensator to adequately follow the reactive-power reference for varying active-power flow. It has also been shown that the proposed compensator improves the harmonic behaviour of the system currents drastically.

The total capacitance used in the proposed compensator is 60 μF (10 μF/phase) which is very small when compared to the total capacitance employed in the shunt passive filter and capacitor banks which is 272.98 μF. The total capacitance in CCC HVDC would be 510 μF where series capacitors would compensate for the entire reactive-power demand of the terminal at rated power flow.

The peak voltage on the DC-link capacitors in the proposed compensator for full reactive-power compensation and rated active-power flow is of the order of 150 kV. This is much smaller than that of the shunt arrangement which is 275 kV. This difference is significant for insulation design.

The proposed compensator does not employ any resistances and hence does not have the inherent power loss as in the shunt arrangement. The switching frequency is much lower than that of STATCOM or SSSC arrangements, minimizing the switching

losses. Most of the switching operations in the proposed compensator are either performed at zero voltage or zero current reducing the switching losses.

The proposed compensator employs six single-phase bridges which would add to the weight and area. However, almost 50-60% of the area in a conventional LCC HVDC terminal is covered by the inductors and capacitors of the shunt passive filters. There is a possibility of drastic reduction in the size and volume of the converter terminal with the proposed compensator.

The control system of the proposed compensator requires the measurement of the compensator DC-link voltage and AC currents on the secondary sides of the converter transformers, which would require additional instruments, adding to the size and weight of the converter terminal. A phase-angle approach employing this kind of compensator would not need these measurements and, thus, would be less instrument-intensive. This is the topic of the next chapter.

The capacitor size used with the GCSC is the same as for the SPVC. However, the peak-to-peak voltage rating required for the GCSC capacitor is slightly higher than the peak voltage for the SPVC DC-link capacitor. The same holds true for the power-electronic switches. This has to be noted that the GCSC would require non-polarized capacitor while the SPVC can work with polarized capacitors, which are smaller in size.

6 The Phase-Angle Control of SPVC

An alternative control strategy for the SPVC based on phase information has been developed and explained in this chapter. Simulation results with the new control strategy have been presented. The impact of the new control on the harmonic behaviour is discussed after comparisons with the previous approaches. Experimental results from a small-scale laboratory setup are briefly discussed. An estimation of size advantage is presented at the end.

The control of SPVC in the previous chapter employed measurements of the SPVC DC-link voltage and phase currents on the secondary side of the converter transformers. This would entail the use of numerous voltage and current transducers with auxiliary equipment. The cost, weight, and volume of the converter terminal would increase as a consequence. In this chapter, we propose a phase-angle approach to the control of the SPVC. This approach uses a phase-locked loop based on the measurement of the voltage on the primary side of the converter transformers and calculates the timing of the instants at which the SPVC in each phase should switch into discharge, recharge, and bypass modes. The calculations for the duration of these modes are also performed. Experimental results employing the strategy are also presented. Experimental results are presented, which validate the theoretical foundation and simulation results. In the end, estimates of reduction in area are presented.

The schematic arrangement of the SPVC is as presented in Fig. 5–1. The control loop for input AC voltage (Fig. 2–6) is used as it is. However the control loops for active-power flow (Fig. 3–2) is modified and will be discussed in the next section. Also, the reactive-power control loop for the SPVC (Fig. 5–10) has to be modified as the scheme proposed in this chapter will use phase-angle control instead of voltage references, measurements, and comparisons.

6.1 Switching Strategy

The starting point for developing the switching strategy is proposed to be the duration of the charging mode of the compensator. The sequence of this development is as under:

- Calculate the charging duration
- Calculate instant of discharge (for commutation)

- Calculate the timing for firing the concerned thyristor in the main AC/DC converter
- Calculate duration of the discharge
- Calculate the instants for charging-mode switching

Once the duration and timing of discharge and charge of the SPVC in any phase is calculated, it would be switched to bypass mode during the rest of the time in the cycle.

6.1.1 Charging Duration

As discussed in the previous chapter, the higher the voltage on the SPVC DC-link, the earlier would be the injection of the same prior to commutating-voltage crossover. The reactive-power consumption of the main AC/DC converter would go down as a consequence and the SPVC would be compensating for higher reactive power, relieving the grid of the reactive load.

This concept was implemented in the previous chapter in developing the reactive-power control loop given in Fig. 5–10. As we are dealing with timing and phase information here, the same control loop is re-designed as in Fig. 6–1. The only difference is that the output of the control-loop is the charging duration ($\gamma_{chargejk}$) in radians. The switch combinations for charging in the positive and negative half-cycles are as given in Fig. 5–5.

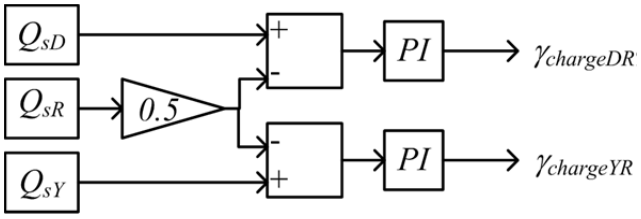

Fig. 6–1. Control loop for generation of charging duration of the SPVCs in the *D* and *Y* branches.

The greater the difference between the reference reactive power and the individual reactive powers of the *D* and *Y* branches, the higher will be the charging duration. The charging will follow the patterns given in Fig. 5–6 (a) and (b) for positive and negative half-cycles respectively. The voltage injected by the SPVC during the positive half-cycle in charge mode is given by:

$$v_{compjk} = v_{compdcjk} = v_{compdcjkT_1} + \frac{1}{C}\int_{T_1}^{T_2} i_{ljk}\,dt \tag{6.1}$$

where, $v_{compdcjkT1}$ is the voltage available on the SPVC DC-link before the start of charging and would be brought down to zero for reasons to be discussed in the sub-section on discharge mode. T_1 is the instant at which the charging would start and T_2 is

the instant at which the charging would stop. Before and after these instants, the SPVC switches would be in the bypass mode described in section 5.2.3.

Charging can be carried out at any time when the concerned phase is carrying current. We propose to distribute the charging period around the mid-point of the conduction period equally. The implication is that the phase current will be equal to the thyristor converter DC-link current and will hold a constant value due to the heavy inductance. This will simplify (6.1) at the time of completion of charging interval to:

$$v_{compjk} = v_{compdcjk} = \frac{1}{C} I_d (T_2 - T_1) = \frac{I_d(\gamma_{chargejk})}{\omega C} \tag{6.2}$$

Similar reasoning and the use of (6.1) for the negative half-cycle would result in:

$$v_{compjk} = -v_{compdcjk} = -\frac{I_d(\gamma_{chargejk})}{\omega C} \tag{6.3}$$

Equations (6.2) and (6.3) shed light on a few facts:

1. The peak voltage available at the end of a given charging period is directly proportional to the active power being transferred. For smaller active-power flow, $\gamma_{chargejk}$ has to be higher to achieve higher voltage on the compensator DC link and, consequently, higher reactive-power compensation.
2. A smaller capacitor will charge to the desired level more quickly than a larger capacitor.

6.1.2 Instant of Discharge

Once we have the voltage available on the SPVC DC link, we should now be able to inject it at an appropriate time before commutation in the positive and negative half cycles. The switch combinations for discharge in the positive and negative half-cycle would be as given in Fig. 5–3, with the conduction paths given in Fig. 5–4.

We need a reference for calculation of instant at which the discharge should start. We select the phase of the line voltage v_{sab}. This is the output of a phase-locked loop (PLL) and is denoted by θ_{ab}. It is a resetting ramp signal varying between 0 and 2π, synchronized to the positive-going zero crossing of v_{sab}. The line voltages on the secondary side of the *YY* transformer behind their leakage reactances would be in phase with the ones on the primary side, while those on the secondary side of the *YD* transformer would lag by 30° (π/6 radians).

It should be kept in mind that the current always commutates in the sequence $a - b - c - a$ in the upper and lower halves of the thyristor bridge in Fig. 2–2. At the positive-going zero crossing of v_{sab} ($\theta_{ab} = 0$), phase b on the secondary side of the *YY*

transformer would become negative with respect to phase *a*, implying that the negative current flowing in phase *a* should commutate to phase *b*. Therefore, an assisting-polarity voltage would have to be injected into phase *b* before $\theta_{ab} = 0$, as shown in Fig. 5–4 (b).

Let T_3 be the instant at which the SPVC would switch to discharge combination. At this instant, the voltage on the SPVC DC link would be exactly equal to the instantaneous value of v_{lYab}, so that the injection would instantly cause crossover of the voltage at the converter terminals. This condition is mathematically specified as:

$$v_{lYab}(T_3) = -V_{compdcYb} \tag{6.4}$$

where, $V_{compdcYb}$ is the peak voltage on the SPVC DC-link.

Putting (6.3) into (6.4) and knowing that v_{lYab} is a sinusoidal signal with a peak of V_{lYabM}, we arrive at:

$$\omega T_3 = -\sin^{-1}\left(\frac{I_d \gamma_{chargeYb}}{V_{lYabM}\omega C}\right) \tag{6.5}$$

We define a new resetting ramp signal, θ_{comp}, which should lead θ_{ab} by the angle given by:

$$\theta_{comp} = \theta_{ab} + \sin^{-1}\left(\frac{I_d \gamma_{chargeYb}}{V_{lYabM}\omega C}\right) \tag{6.6}$$

θ_{comp} will be elevated above θ_{ab} depending upon the second term on the right-hand side of (6.6). This could make it difficult to pinpoint a reference for the timing of various switching operations throughout the system. To alleviate this problem, an algorithm is proposed which will shift θ_{comp} in time rather than in value. It would now become a ramp varying from 0 to 2π, leading θ_{ab} by the time depending upon (6.6). The algorithm is:

$$\begin{aligned} &\text{If } \theta_{comp} > 2\pi \\ &\text{then } \theta_{comp} = \theta_{comp} - 2\pi \\ &\text{If } \theta_{comp} < 0 \\ &\text{then } \theta_{comp} = \theta_{comp} + 2\pi \end{aligned} \tag{6.7}$$

When θ_{comp} hits zero, the switches in the SPVC in phase *b* would be switched according to Fig. 5–4. The timing of discharging voltage injections in other SPVCs in the *Y* branch can be calculated by observing the natural order of commutation in the thyristor bridge.

The corresponding injections in the *D* branch can be timed by delaying them by an angle of $\pi/6$ radians.

6.1.3 Timing of Thyristor Firing

The next step is to calculate when the concerned thyristor should be fired to start current commutation. As the injection of the voltage at the timing mentioned above forces converter terminal voltage crossover, the thyristor should be fired after a delay given by α. So, another resetting-ramp signal θ_{thy} is generated, similar to θ_{comp} and θ_{ab}, which is calculated as:

$$\theta_{thy} = \theta_{comp} - \alpha \tag{6.8}$$

The result of (6.8) is manipulated using (6.7) for similar reasons given in section 6.1.2. The lower thyristor in the *b* leg in *Y* branch would be fired at $\theta_{thy} = 0$. The rest of the thyristors would be fired in the natural order of commutation with equal intervals $\pi/3$ radians. The corresponding thyristors in the *D* branch would be fired with delays of $\pi/6$ radians.

6.1.4 Duration of Discharge

Next is the duration for which the switches in the SPVC should remain in the discharge position after which they revert to the bypass mode. The injection of series voltage causes crossover, however, the phase in question does not have any current flowing through it until a lapse given by (6.8). The current starts to commutate as soon as the thyristor is fired. At this instant, the SPVC DC link starts to discharge bringing the voltage down according to:

$$v_{compYb} = v_{compdcYb} = v_{compdcYbT_3} - \frac{1}{C}\int_{T_3}^{T_4} i_{lYb}\,dt \tag{6.9}$$

where, T_4 is the time at which the SPVC switches to bypass mode. The current is not constant as in the case of charging. It was discussed that the SPVC DC-link voltage should be zero prior to the start of charging, so the interval $T_4 - T_3$ should be long enough to discharge the capacitor completely. We propose:

$$\gamma_{dicharge} = \omega(T_4 - T_3) = \alpha + \gamma_{charge} + \pi/12 \tag{6.10}$$

where, $\gamma_{discharge}$ is the duration of discharge in radians. A factor of $\pi/12$ radians (15°) has been added to force the discharging current through SPVC DC-link to reduce it to minimum level.

6.1.5 Timing of Charge

As discussed in section 6.1.1, the timing of charge would be distributed equally about the midpoint of the conduction period of the concerned phase in a half-cycle. The conduction period starts when the thyristor in the concerned branch is fired. The instant for firing is derived in (6.8). We know that the conduction period in a half-cycle is $2\pi/3$ radians (120°), so the charging should be distributed around $\pi/3$ radians. This is expressed mathematically for the charging of compensator DC link in *b* phase in the *Y* branch during the negative half-cycle of the current as:

$$\frac{\pi}{3} - \frac{\gamma_{charge}}{2} < \theta_{thy} < \frac{\pi}{3} + \frac{\omega\gamma_{charge}}{2} \tag{6.11}$$

The remaining charging instants in the *Y* branch can be calculated by similar reasoning in the natural order of commutation. Of course, corresponding charging intervals in the *D* branch will be delayed by $\pi/6$ radians.

6.2 Simulation Setup

The setup is exactly the same as in section 5.4 in the previous chapter. Two cases have been simulated, in each of which, either of the active- or reactive-power references change with the other fixed during simulation. The important quantities in each case are plotted and discussed.

6.2.1 Case I: Changing Active-Power and Constant Reactive-Power Reference

Like the previous chapters, the active-power reference is changed and the performance of the compensator is analysed. The simulations start with P_s = 1 pu with the SPVC bypassed. The SPVC is connected at 3 s. At 5 s, the active-power reference is changed to 0.5 pu and the performance of the SPVC is analysed.

6.2.2 Case II: Constant Active-Power and Changing Reactive-Power Reference

This case is similar to the cases in the previous chapters where the reactive-power reference was set to 0 pu at the time of connection of the SPVC (at 3 s). This reference changed to 0.3 pu (representative of partial compensation) at 5 s. The active power remained at 1 pu throughout this case.

6.3 Simulation Results for Case I

6.3.1 Active and Reactive Powers

Active and reactive powers at different points in the system are presented in Fig. 6–2. A comparison with Fig. 5–11 shows that the results are similar. This is predictable as the principal of series voltage injection is the same. However, the strategy to time and control these is based on phase-angle detection and calculation rather than voltage measurements and comparisons.

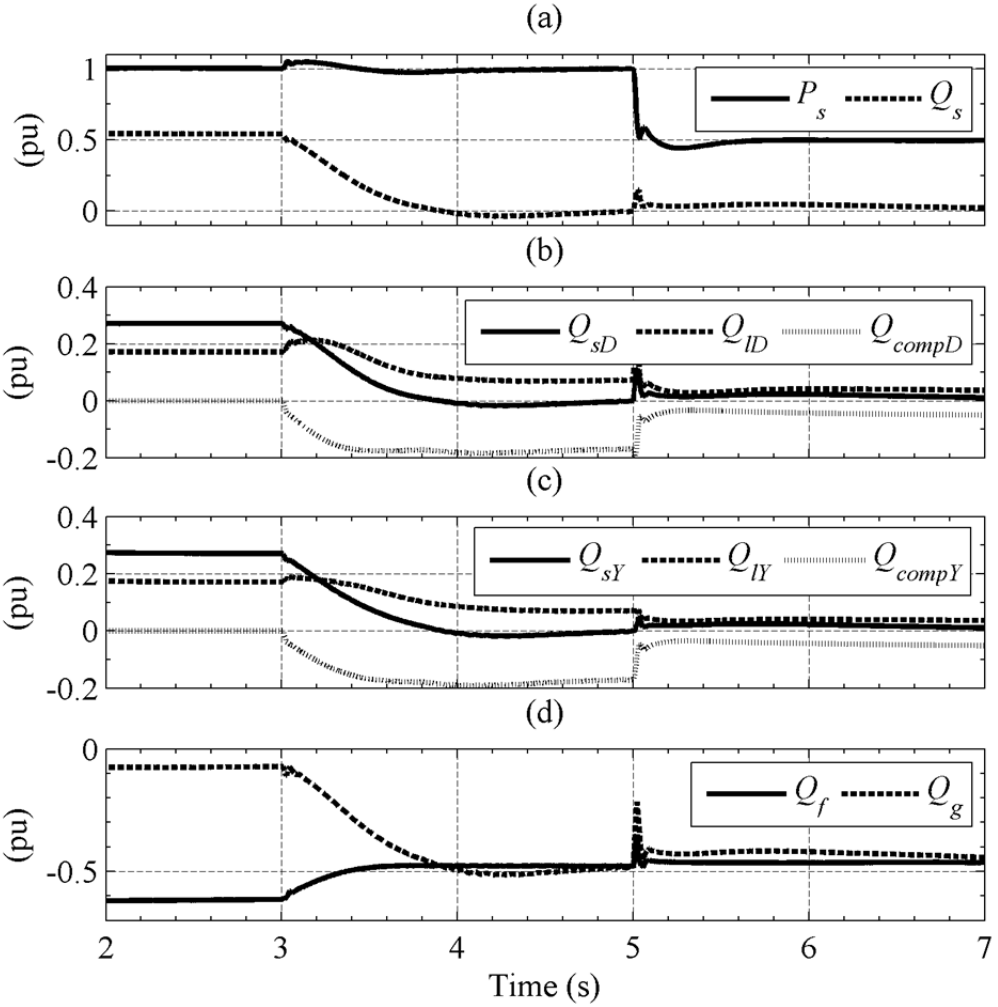

Fig. 6–2. Active and reactive powers at different points in the system for case I.

6.3.2 Control Loop Operation

The operation of the control loops for this case is depicted in Fig. 6–3. The active-power control loop and AC-voltage control loop discussed in the preceding chapters keep α (panel (a)) and V_{sa} (panel (b)) in control. Panel (c) shows the variations in the reference charging duration for the SPVCs in the *D* and *Y* branches. Before the start of series

compensation, this charging duration is zero. When the SPVC is connected, $\gamma_{chargeDR}$ and $\gamma_{chargeYR}$ rise in conjunction with the reactive-power reference and settle at 0.21 radians, when the error between the reactive-power reference and actual flow is brought to 0 pu. As the active-power reference and consequently the current through the SPVC is reduced, a higher charging time is required even for a lower voltage on the SPVC DC link (refer to Fig. 5–12 (c)).

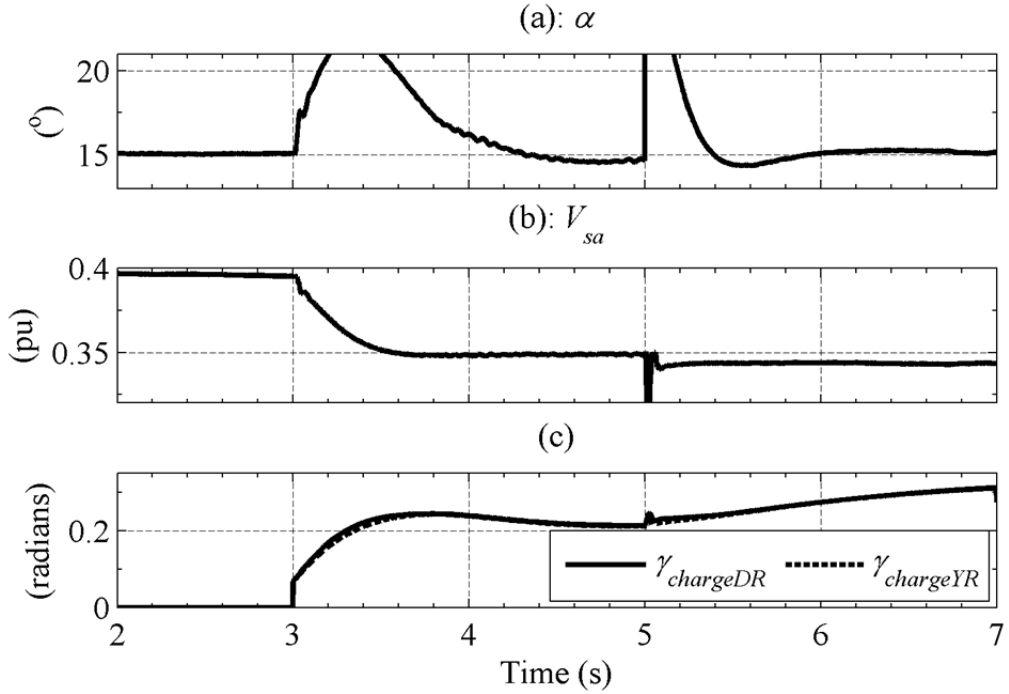

Fig. 6–3. Behaviour of control loops (a) α, (b) rms value of phase *a* voltage on the converter-transformer primary side, and (c) reference value of charging duration of SPVC DC-link capacitor.

6.3.3 Instantaneous Currents and Voltages

Single-cycle snapshots of instantaneous current and voltage on the secondary side of the *YD* transformer are given in Fig. 6–4. The situation is identical in *YY*-transformer secondary except a 30° phase lead. As in the previous chapter, the injection of voltage by the SPVC forces crossover of the converter terminal voltage instantaneously. The thyristor is then fired after α and the current commutates. The difference between the control algorithms in the previous and current chapter can be observed in the charging timing. The plots corresponding to the remaining plots for the quantities on the converter side in section 5.5.3 are not being reproduced here as they are similar to the ones in this approach, and do not need to be discussed.

The single-cycle plots of instantaneous phase-*a* currents and voltages for 1-pu active power are given in Fig. 6–5. These are similar to the plots in Fig. 5–16. The same plots when observed at 0.5-pu active power are given in Fig. 6–6. Comparing panel (c) and (d) of Fig. 6–5 and Fig. 6–6, we find that the harmonic content in i_{sa} and i_{fa}

increases with decreased active-power flow. This effect was also observed in the previous chapters and is due to limited reactive-power consumption by the leakage reactances of the converter transformers at smaller current flow.

The instantaneous voltages appearing across thyristors in the main AC/DC converter and IGBTs in the SPVC are not being shown here as the system voltages and currents are at the same level as in section 5.5.

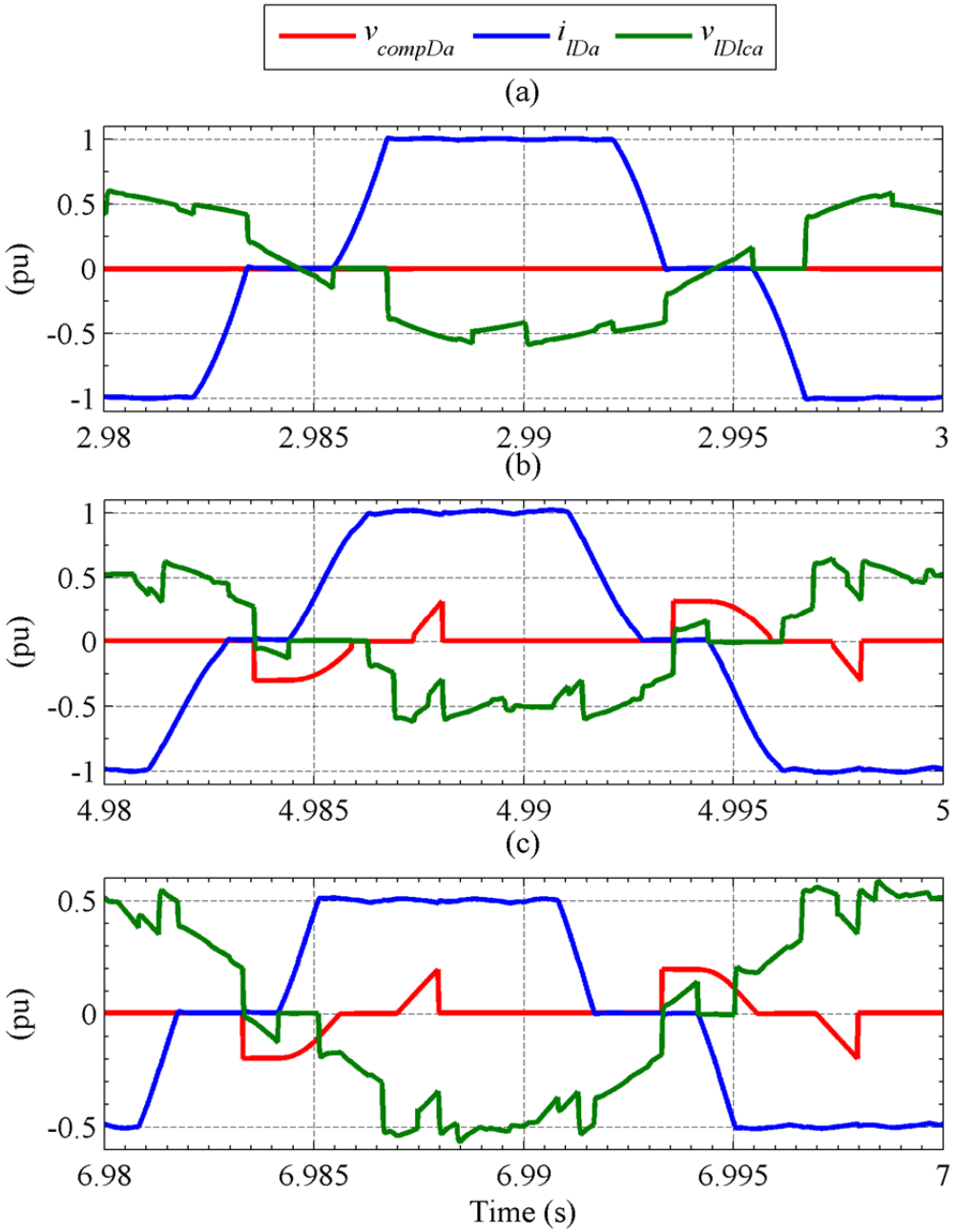

Fig. 6–4. Single-cycle plots of selected variables on the converter side (a) without series compensation at full load, (b) with series compensation at full load, and (c) with series compensation at 0.5-pu load.

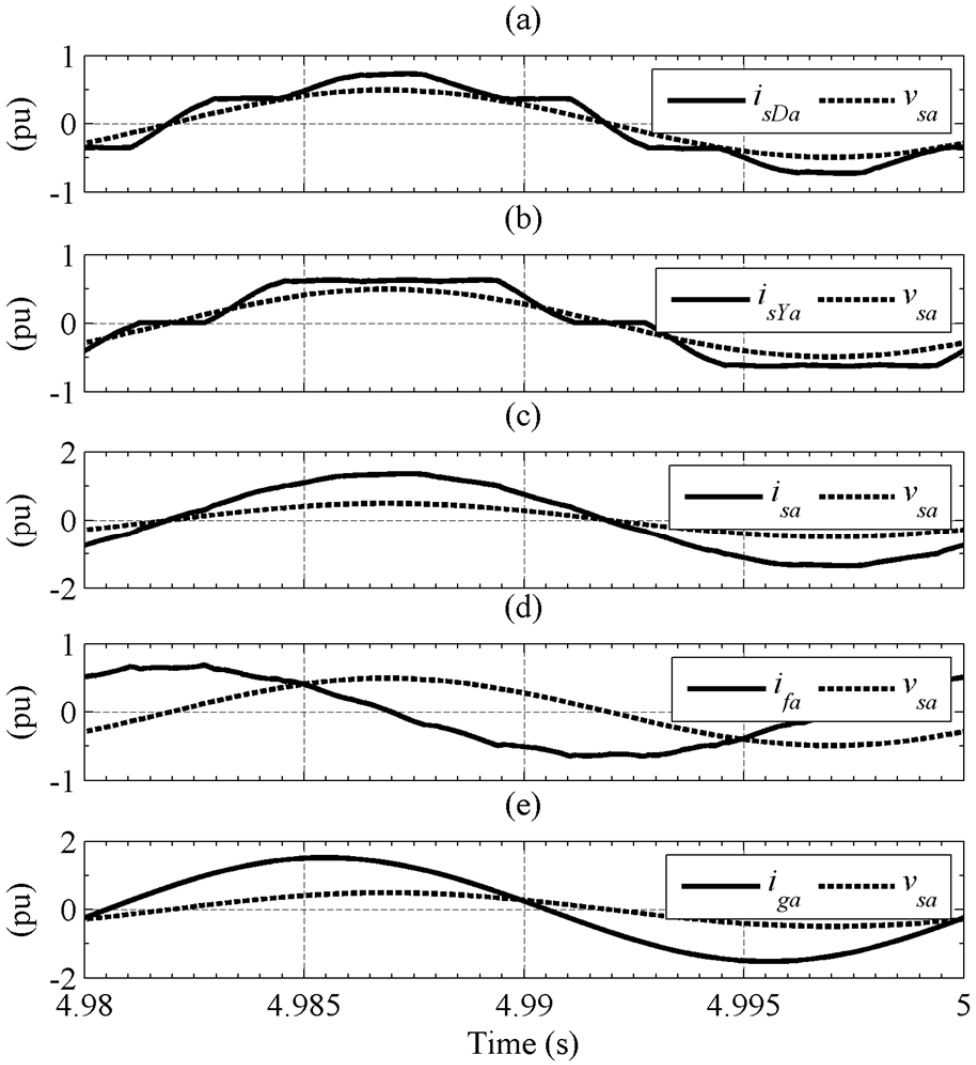

Fig. 6–5. Grid-side currents for phase *a* with full compensation at full load.

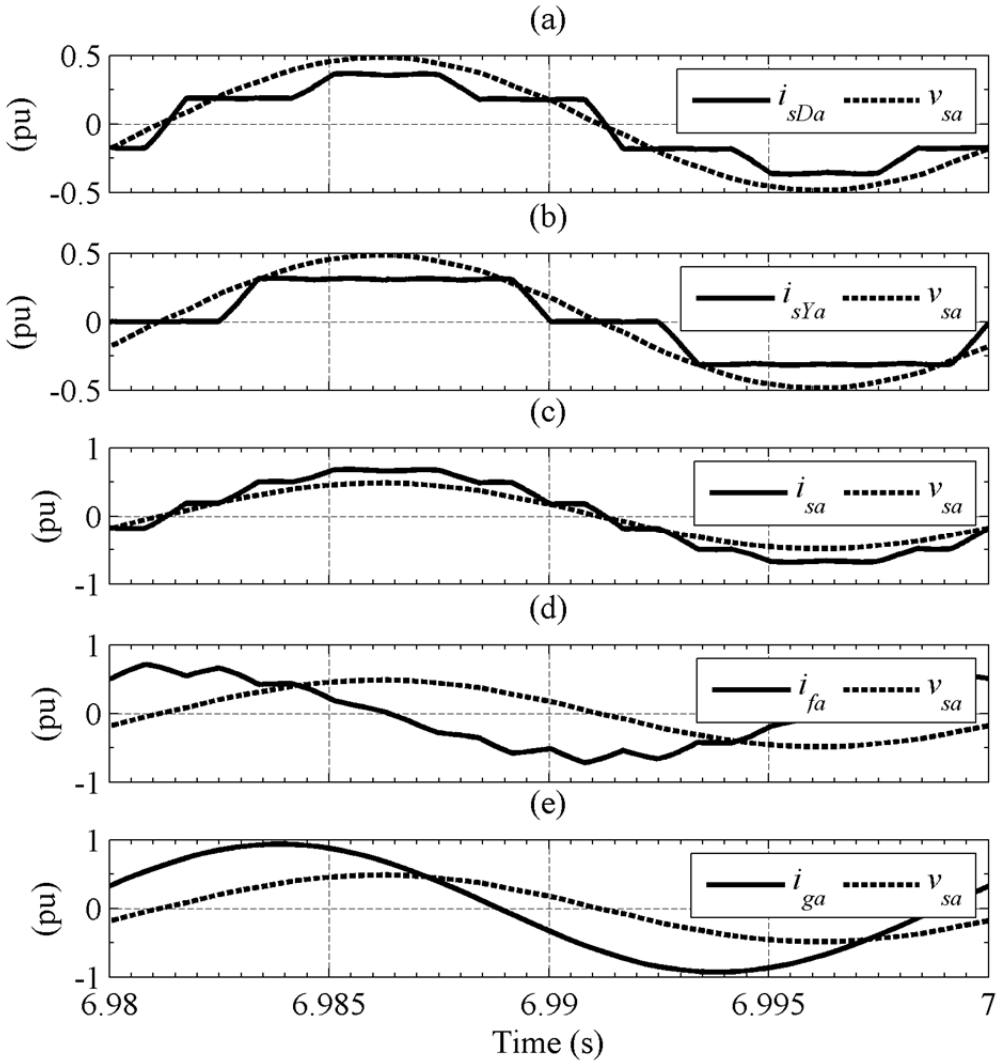

Fig. 6–6. Grid-side currents for phase *a* with full compensation at 0.5-pu load.

6.3.4 Current Harmonics

The harmonic spectra of i_{lDa} and i_{sDa} for 1-pu active power are given in Fig. 6–7 (a) and (b) respectively. Comparison with corresponding spectra in Fig. 5–20 reveals that THD has increased by almost 1% in both. The harmonic spectra of both these currents at 0.5-pu active-power flow are presented in Fig. 6–8. Predictably, the THD has increased, but the amplitudes of the harmonics are much lower than the ones in Fig. 6–7.

Similarly, harmonic spectra of i_{lYa} and i_{sYa} for rated power flow are shown in Fig. 6–9 (a) and (b) respectively. These exhibit increased THD compared to the corresponding spectra presented in Fig. 5–22. The harmonic spectra of the same currents for 0.5-pu power flow are given in Fig. 6–10. These exhibit similar high THD as observed in the case of *D* branch.

The harmonic content in the total current into the converter transformers, that flowing into the shunt filter, and the grid current are presented in Fig. 6–11. The THD in

i_{sa} is a little more than that in case I in the previous chapter (refer to Fig. 5–24 (a)), however, it is much smaller than the conventional shunt, CCC, and GCSC cases. The harmonic content is reproduced for 0.5-pu active power in Fig. 6–12. Again, the harmonic content in i_{sa} is a little higher than what was seen in Fig. 5–25 (a). However, it is much lower than other topologies.

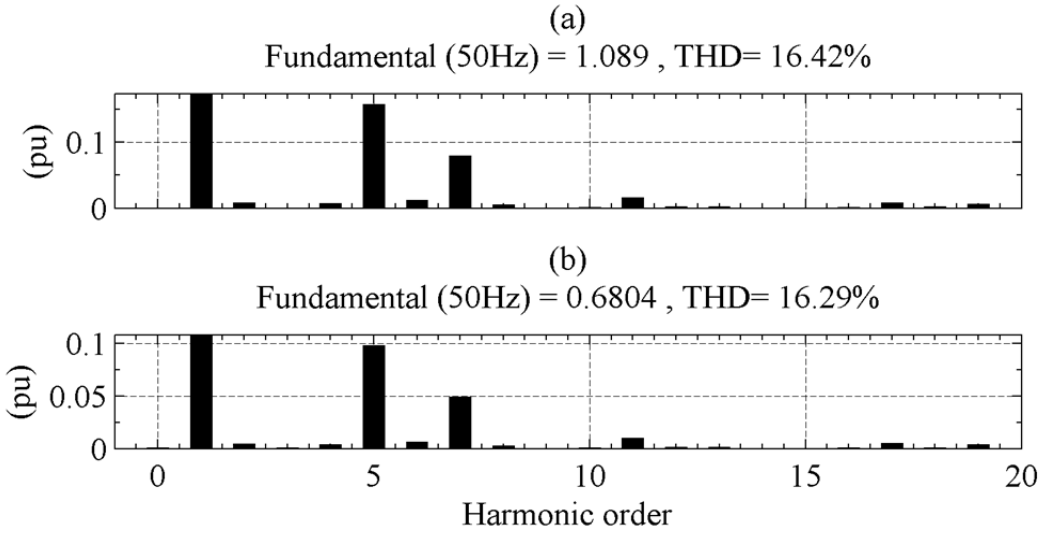

Fig. 6–7. Harmonic spectra for 1-pu power flow (a) i_{lDa} (b) i_{sDa}.

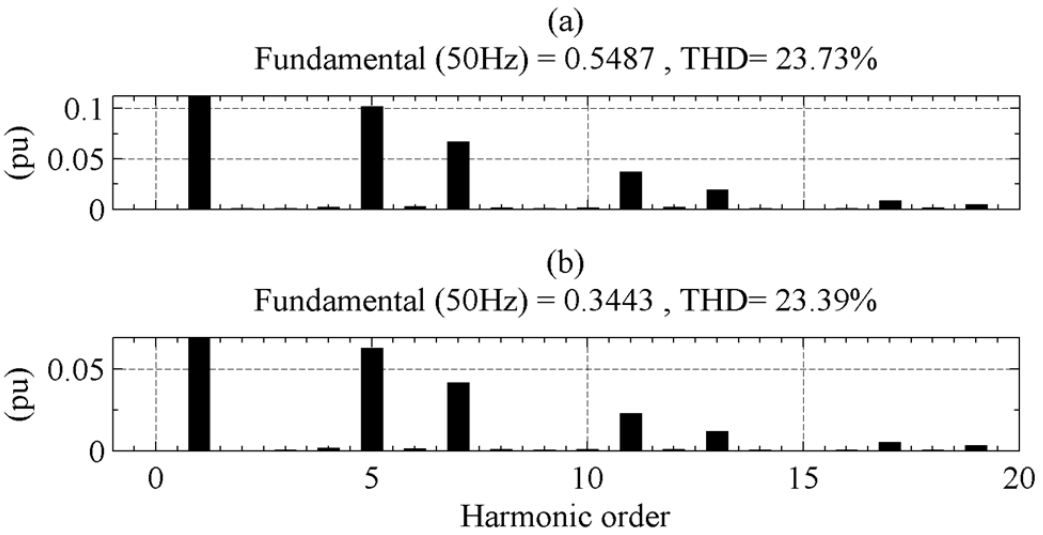

Fig. 6–8. Harmonic spectra for 0.5-pu power flow (a) i_{lDa} (b) i_{sDa}.

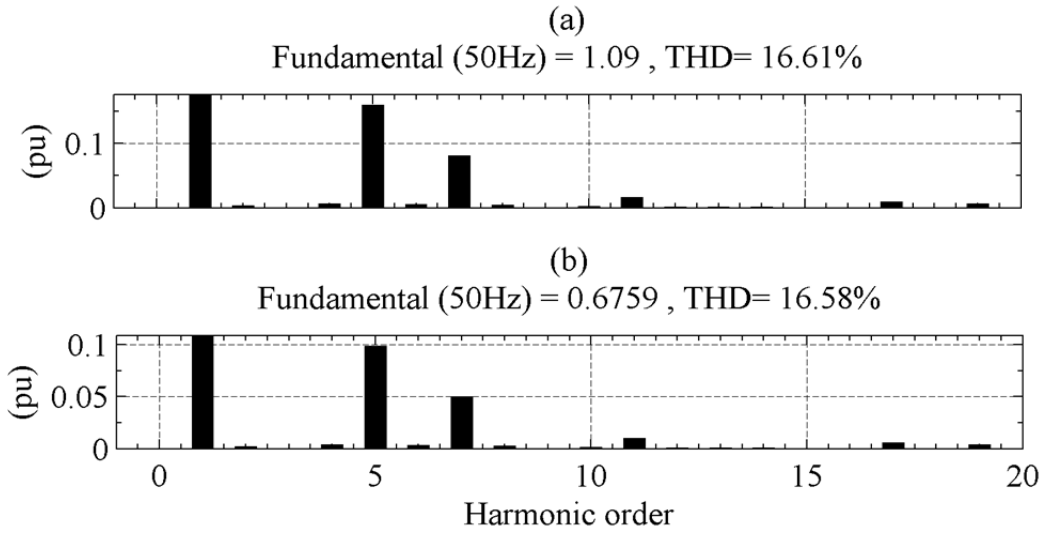

Fig. 6–9. Harmonic spectra for 1-pu power flow (a) i_{lYa} (b) i_{sYa}.

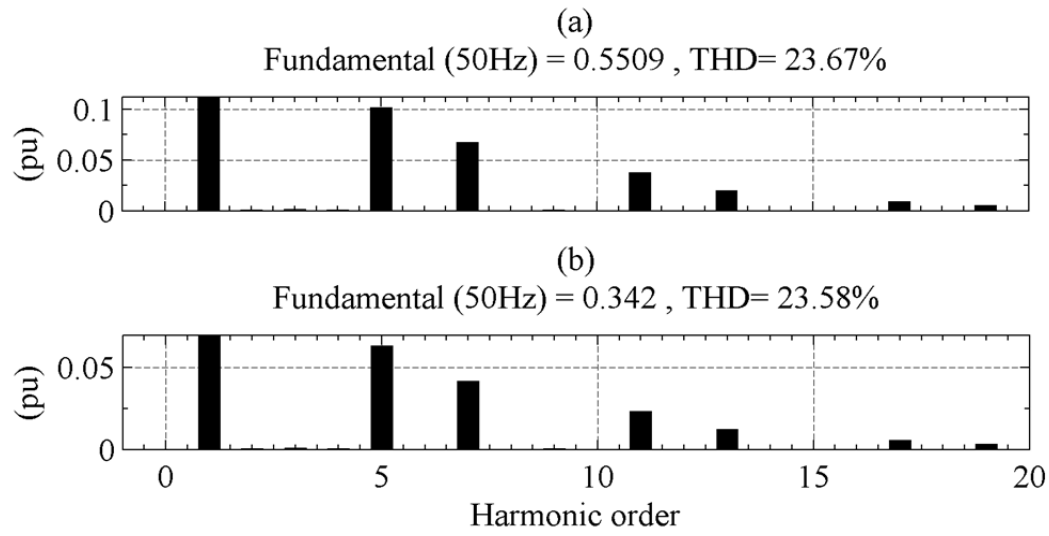

Fig. 6–10. Harmonic spectra for 0.5-pu power flow (a) i_{lYa} (b) i_{sYa}.

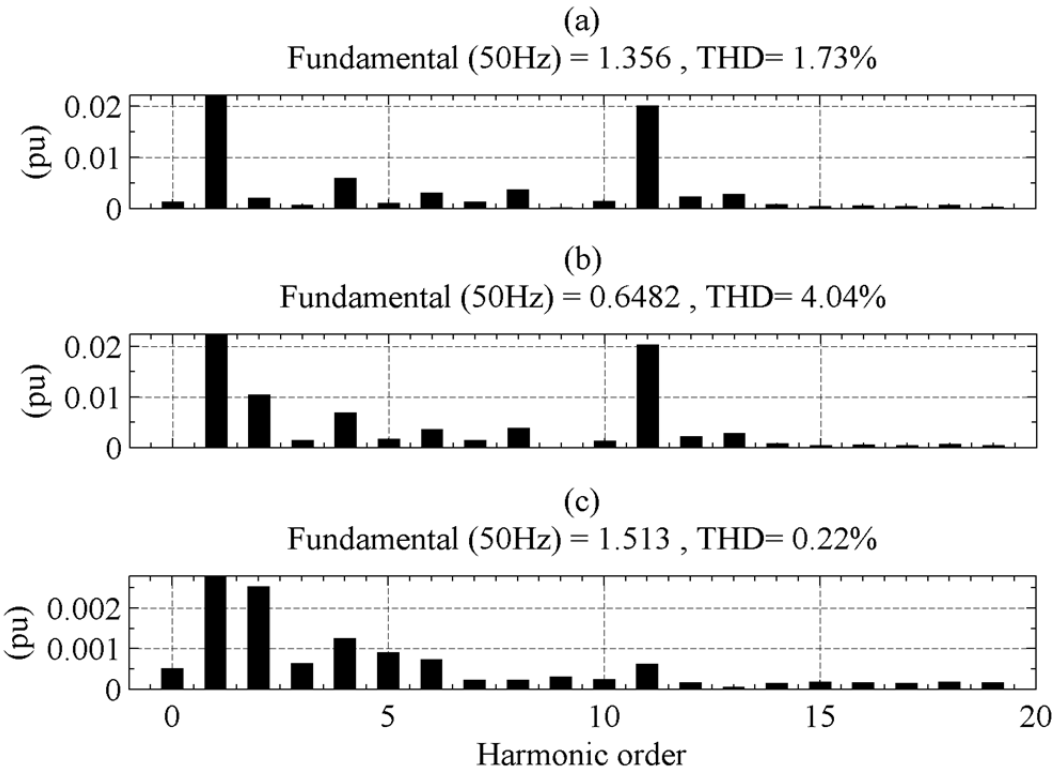

Fig. 6–11. Harmonic spectra for 1-pu power flow (a) i_{sa} (b) i_{fa}, and (c) i_{ga}.

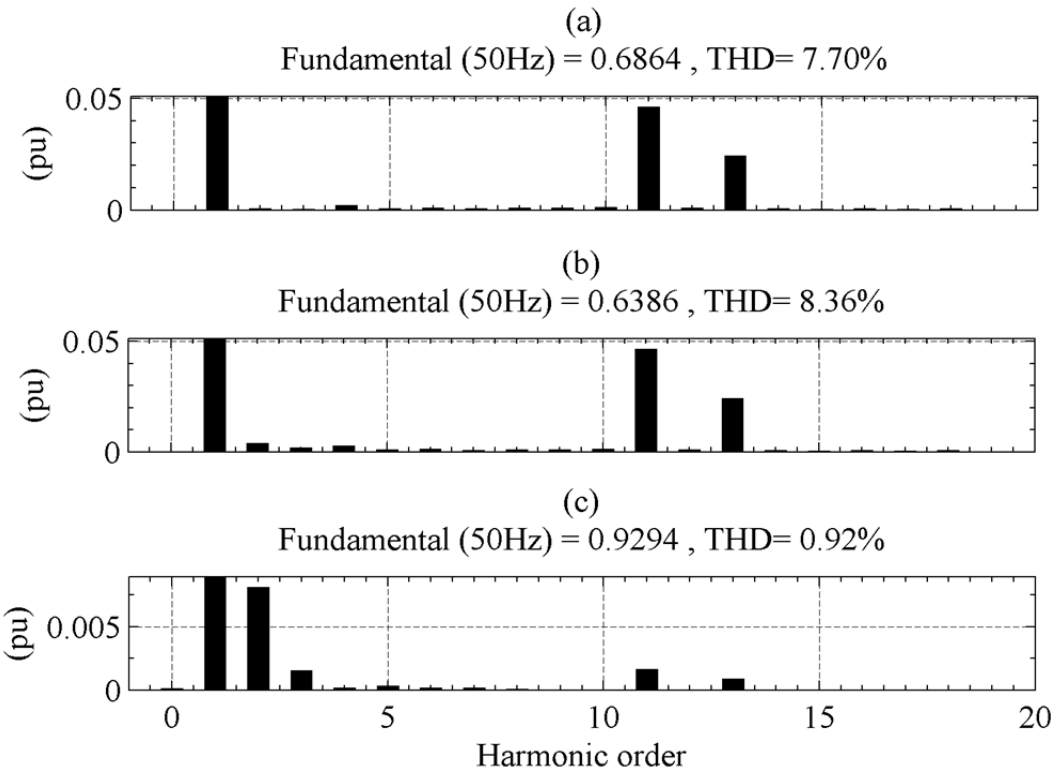

Fig. 6–12. Harmonic spectra for 0.5-pu power flow (a) i_{sa}, (b) i_{fa}, and (c) i_{ga}.

6.3.5 Instantaneous Power

The instantaneous-power picture of the system at 1-pu active power is given in Fig. 6–13. A comparison with Fig. 5–26 shows that the ripples in p_{sD} and p_{sY} are not as exactly in anti-phase position (Fig. 6–13 (c)) as in the Fig. 5–26 (c) resulting in a slightly higher ripple in p_s. This leads us to conclude that the recharging of the SPVC DC link was better placed in the preceding chapter than here. However, as we have full control on where to place the recharging, the procedure adopted in this chapter is much better. This timing could be altered in the control algorithm to achieve better results. The instantaneous powers for 0.5 pu P_s are given in Fig. 6–14 and exhibit larger ripple in p_{sD} (panel (c)) compared to that in Fig. 5–27 (c). This is the reason for larger THD in i_{sa} in this chapter than the previous chapter.

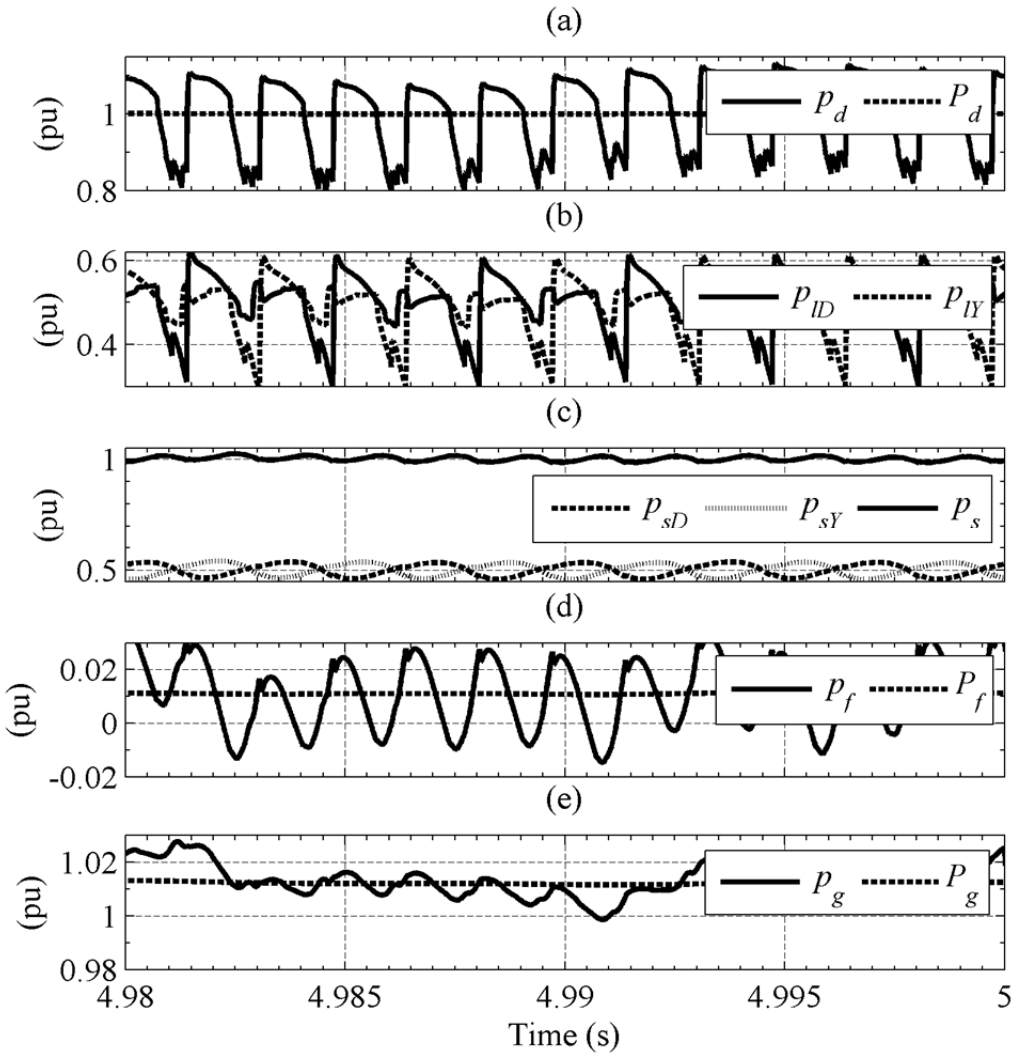

Fig. 6–13. Instantaneous powers at 1-pu active power at different locations in the system with SPVC.

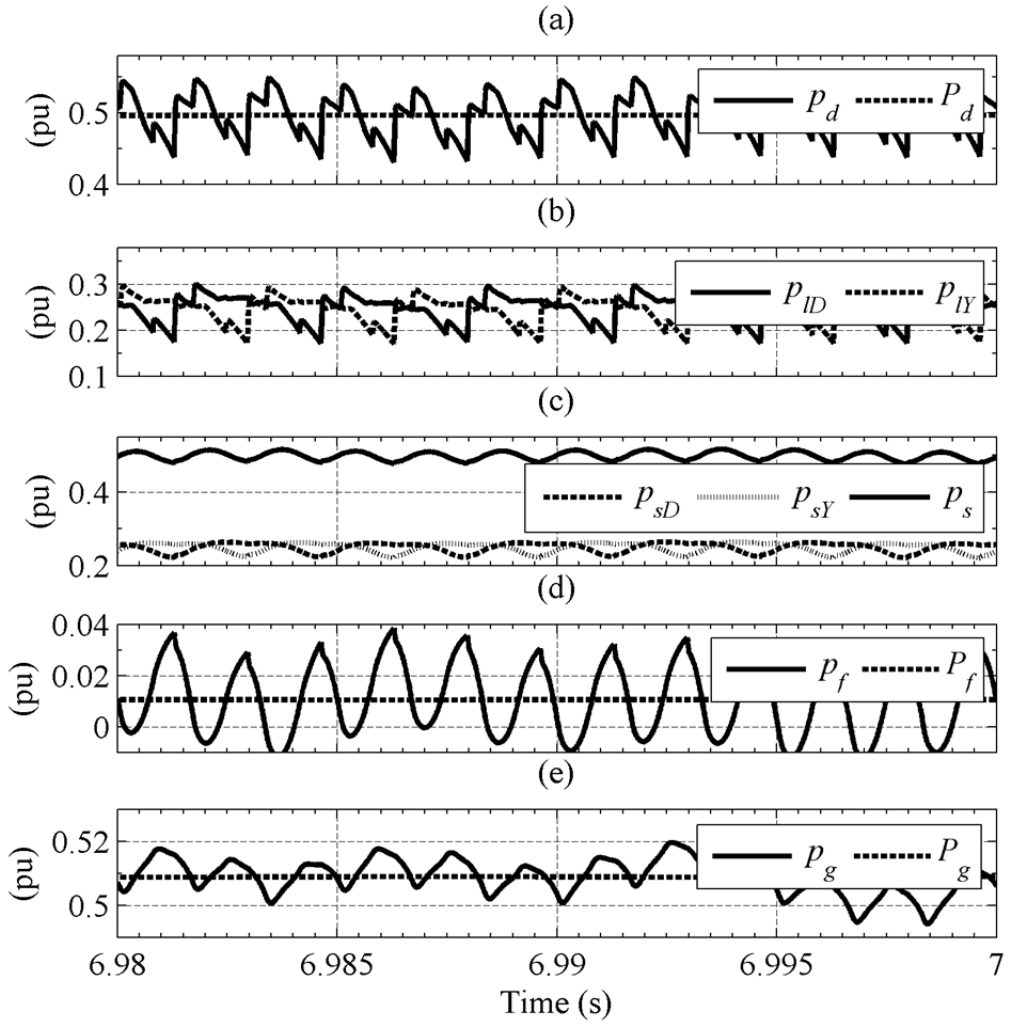

Fig. 6–14. Instantaneous powers at 0.5-pu active power in the system with SPVC.

6.4 Simulation Results for Case II

The first two periods in this simulation are identical to case I (period without SPVC and period with SPVC fully compensating for reactive power). Therefore, we will only present the plots for the third period, with SPVC partially compensating for reactive power.

6.4.1 Active and Reactive Powers

The active and reactive powers for this case are shown in Fig. 6–15. At the transition of Q_{sR} from 0 to 0.3 pu, the SPVC adjusts its voltage injection in such a manner that Q_{lD} and Q_{lY} increase. Consequently, Q_{sD} and Q_{sY} rise, whose sum is Q_s. It settles to 0.3 pu after a transient period.

6.4.2 Control Loop Operation

The behaviour of different variables due to the control loops is given in Fig. 6–16, which is similar to what has been discussed for Fig. 5–29. The difference is the reference value of the charging duration for the SPVCs in the two branches (panel (c)). As expected, this reference value decreases as the demand for reactive compensation goes down.

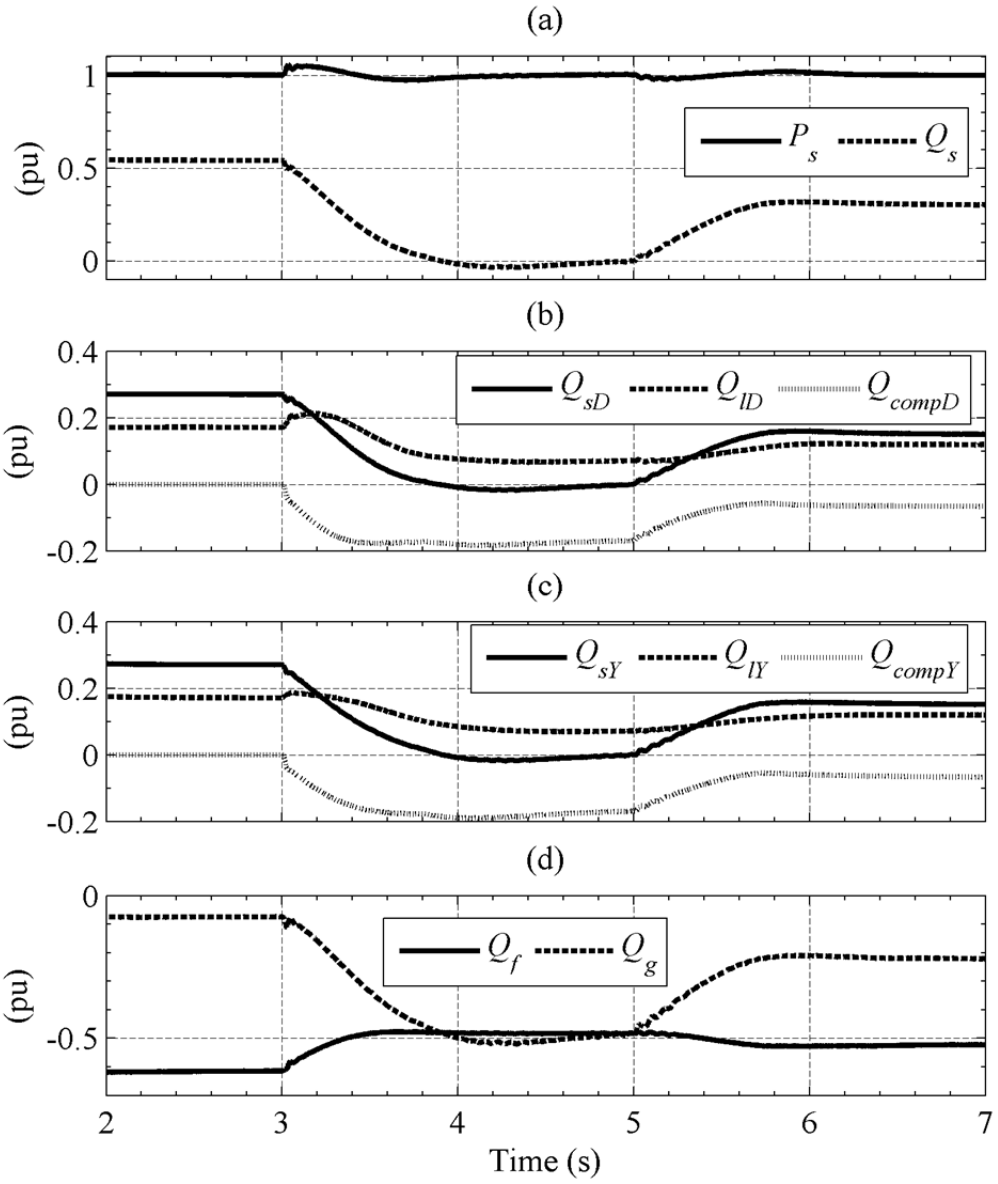

Fig. 6–15. Active- and reactive-power behaviour for case II.

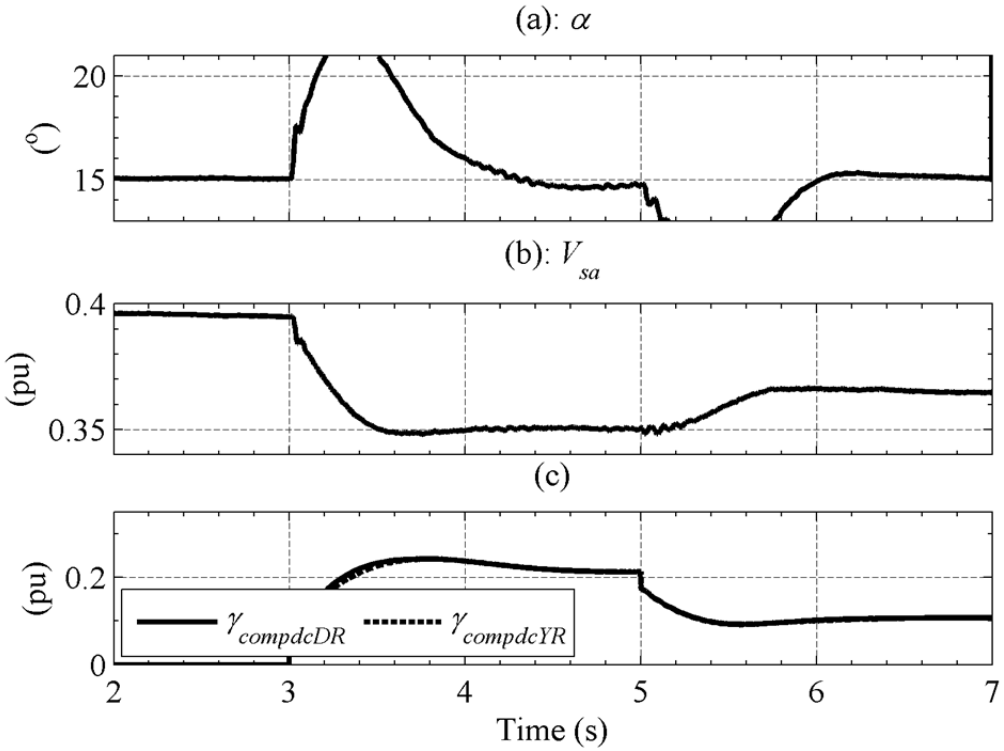

Fig. 6–16. Control loop behaviour for case II.

6.4.3 Instantaneous Currents and Voltages

The converter side variables during the period with partial compensation in the *D* branch are shown in Fig. 6–17. The duration of charging, and therefore, the peak of injected voltage have gone down in comparison with the full-compensation case at full load plotted in Fig. 6–4 (b). This also leads us to conclude that if we want to use the SPVC in conjunction with shunt passive filters like in the case of CCC HVDC, the required voltage rating for the SPVC capacitors and power-electronic components will also be reduced. It can be seen that the series injection for recharging is not spread around the centre of the current half-cycle as intended. The reason is that the conduction period is not exactly 120° in a half-cycle due to larger commutation duration.

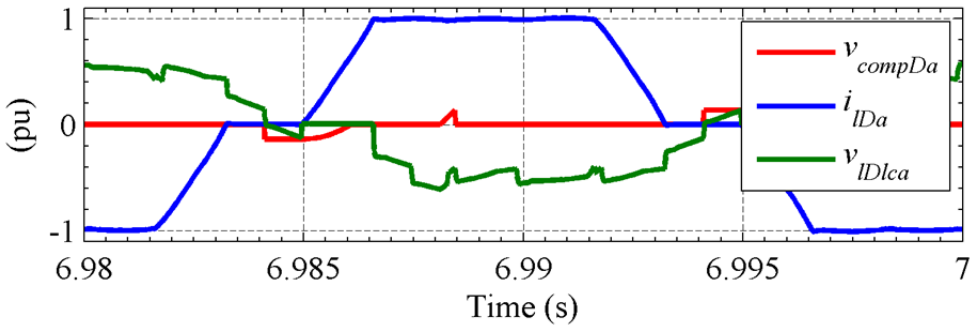

Fig. 6–17. Single-cycle plots of selected variables on the converter side with partial series compensation at 1-pu load.

The instantaneous voltage and current picture with partial compensation being done by the SPVC is given in Fig. 6–18. The currents i_{sDa}, i_{sYa}, and i_{sa} lag v_{sa} by a small angle indicative of reactive-power flow into the two converter transformers.

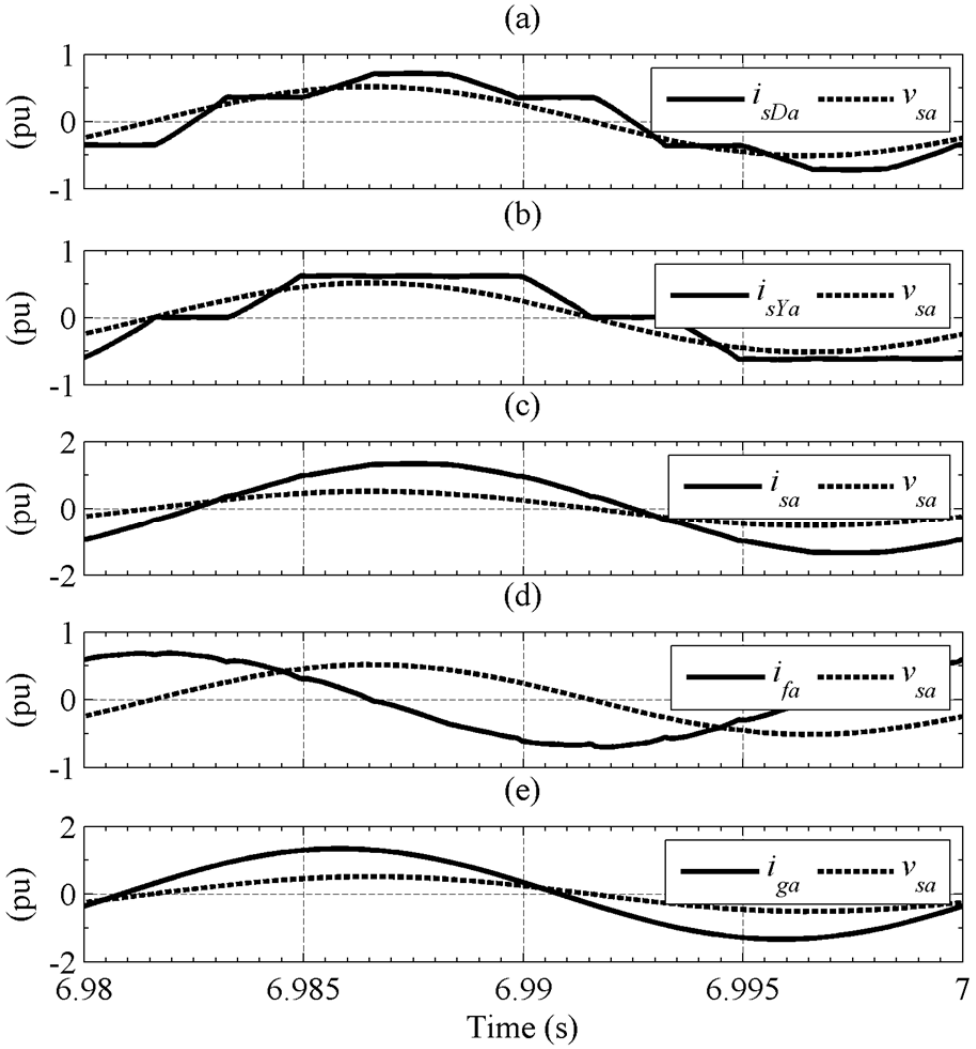

Fig. 6–18. Grid-side currents for phase *a* with partial compensation at full load.

6.4.4 Current Harmonics

The harmonic spectra of i_{lDa} and i_{sDa} for the period with partial compensation are given in Fig. 6–19. The THDs are higher as compared to the case with full compensation (Fig. 6–7). The harmonic spectra for corresponding currents in *Y* branch are presented in Fig. 6–20. These also exhibit higher THD when compared to the corresponding spectra with full compensation in case I (Fig. 6–9).

The harmonics in i_{sa}, i_{fa}, and i_{ga} for this case are shown in Fig. 6–21. The THD in i_{sa} has gone down to 1.26% against 1.73% in the full compensation case (Fig. 6–11 (a)). In fact, it is almost the same as in case II in chapter 5 (Fig. 5–37 (a)).

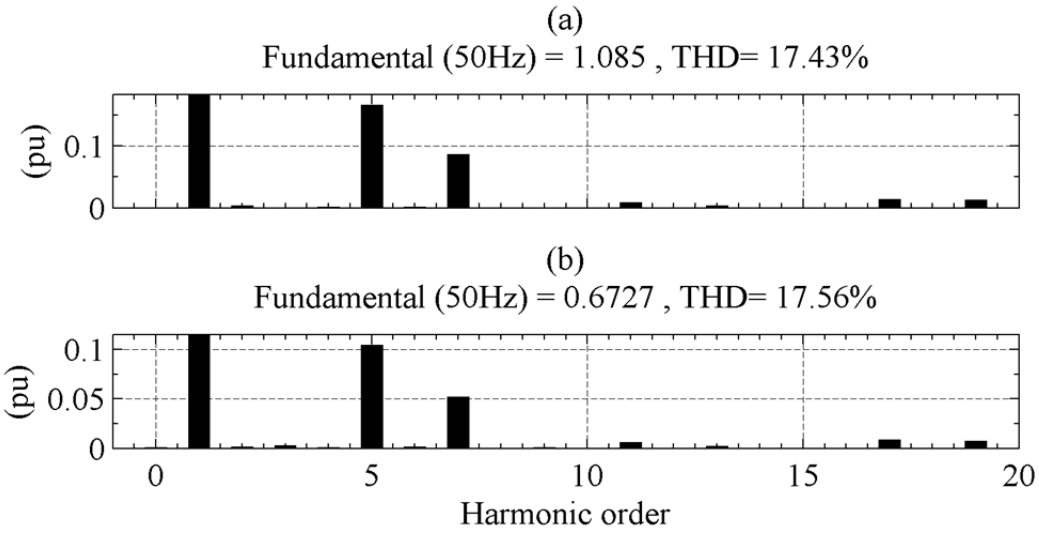

Fig. 6–19. Harmonic spectra for Q_s = 0.3 pu (a) i_{lDa} (b) i_{sDa}.

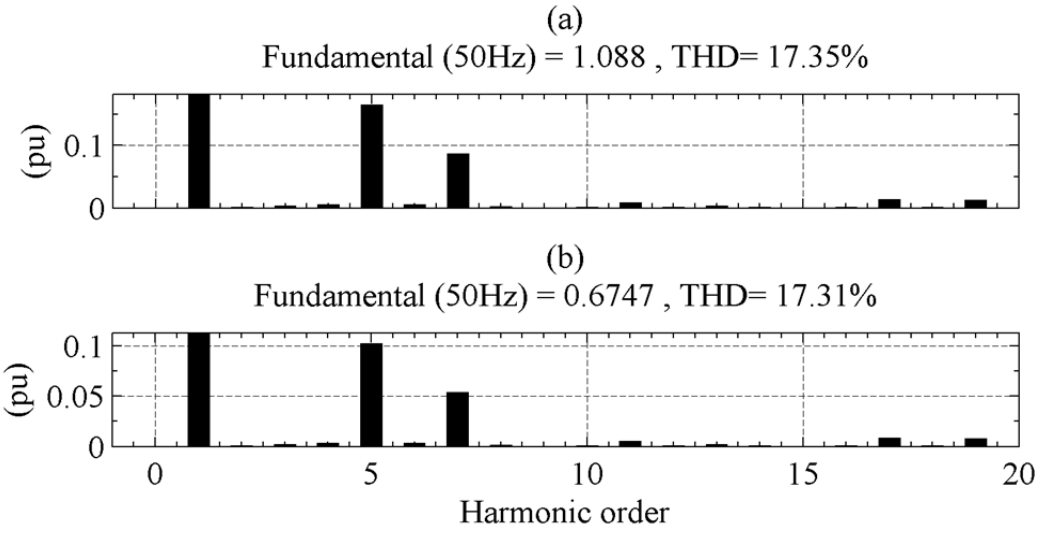

Fig. 6–20. Harmonic spectra for Q_s = 0.3 pu (a) i_{lYa} (b) i_{sYa}.

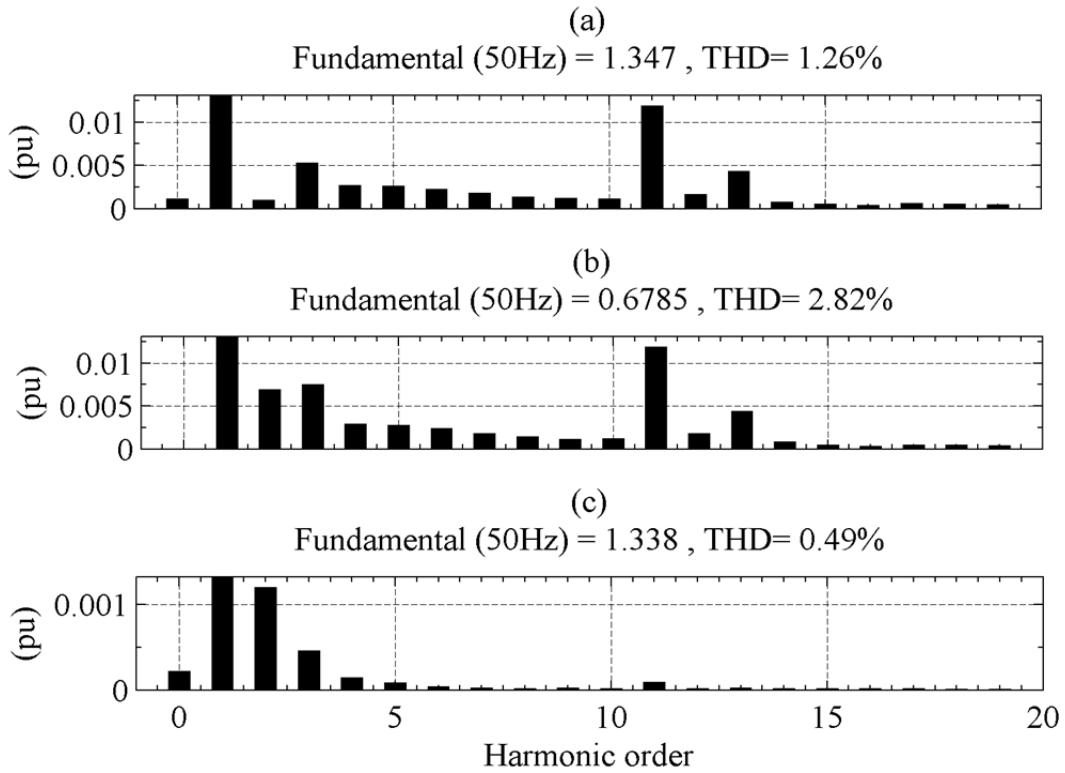

Fig. 6–21. Harmonic spectra for Q_s = 0.3 pu (a) i_{sa}, (b) i_{fa}, and (c) i_{ga}.

6.4.5 Instantaneous Powers

The instantaneous-power picture with P_s = 1 pu and Q_{sR} = 0 pu has been presented in section 6.3.5. The same is presented in Fig. 6–22 for the interval with Q_{sR} = 0.3 pu. A comparison with Fig. 5–38 shows that the change in the timing of recharging interval has had a positive effect on the instantaneous power oscillations (refer to p_s in Fig. 6–22 (c) and Fig. 5–38 (c)). This results into better harmonic cancellation (as reported in Fig. 6–21 (c)) as compared to Fig. 5–37 (c).

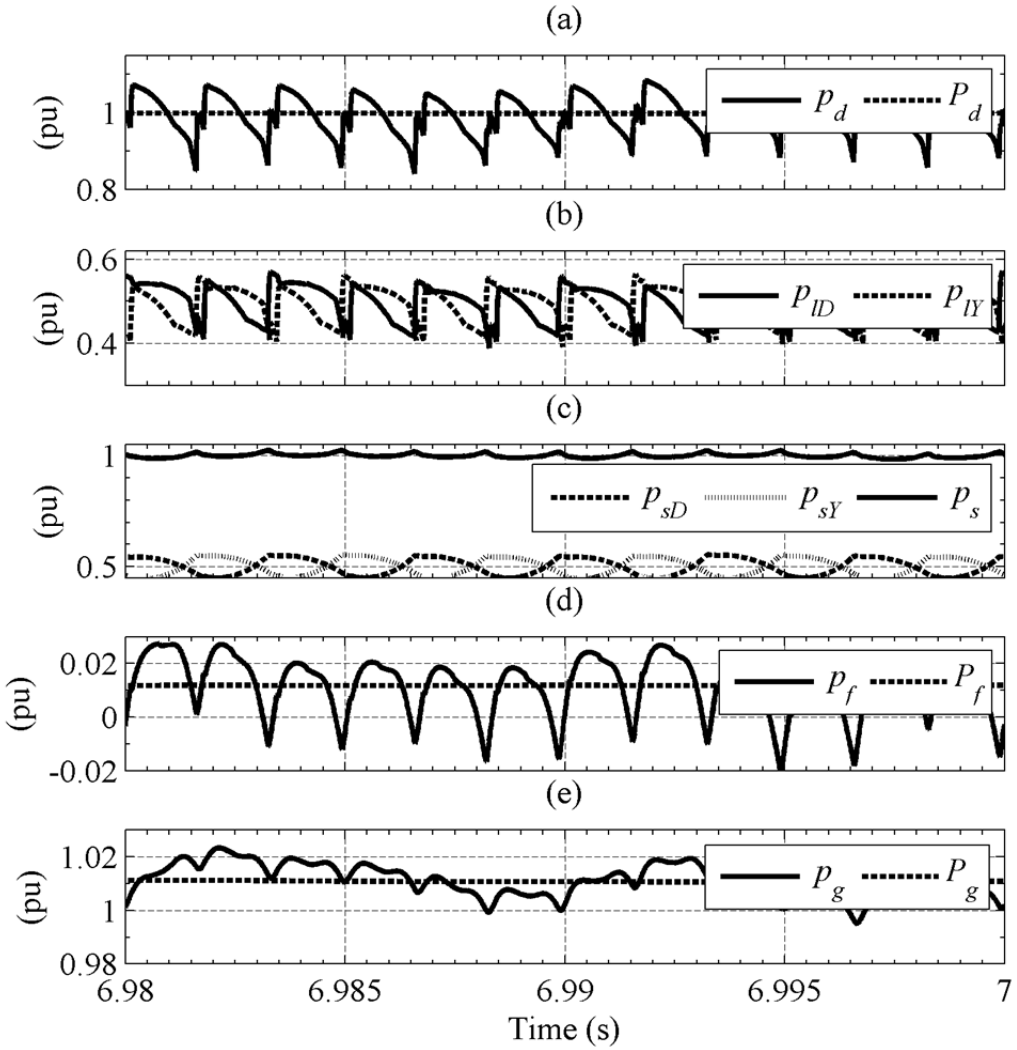

Fig. 6–22. Instantaneous powers at P_s = 1 pu and Q_s = 0.3 pu with SPVC.

6.5 Comparison of Harmonic Figures

Most of the discussion with regards to the comparison of the SPVC harmonic performance with other topologies has been handled in the preceding chapter. The harmonic performance of the two SPVC-control methodologies will be discussed here.

The important harmonic characteristics in the currents in the *D* branch are presented in TABLE 6–1. The header for the right-most column "SPVC2" is used to distinguish the harmonic performance obtained with the control methodology adopted in this chapter. The column with the header "SPVC1" contains the data form the control methodology in the preceding chapter. The THD in i_{lDa} is 16.42% for full load with full compensation (has gone up from 15.19% with the control methodology of the previous chapter). The magnitudes of the 5th, the 7th, and the 11th harmonics have also increased. However, the 13th harmonic is reduced in magnitude as compared to the SPVC1 case. The same holds true for the case when active power is reduced to 0.5 pu. The figures for

the case when active power is 1 pu and the SPVC is providing partial compensation are almost identical to the SPVC1 case, with the SPVC1 approaches slightly better than the SPVC2 approach. All the harmonics are slightly higher in magnitude with SPVC2 than with SPVC1, with the exception of the 13th harmonic. When the SPVC is acting in partial-compensation mode at 1-pu active power, the THD is almost identical to that with SPVC1 control methodology. The 5th and the 11th harmonics are slightly smaller and the 7th and the 13th harmonics are slightly larger than the numbers observed with SPVC1 approach. Similar behaviour is observed in i_{sDa} for all the cases discussed above. The important harmonic characteristics for the *Y* branch are listed in TABLE 6–2. These are similar to what was observed in the *D* branch and do not need further discussion.

TABLE 6–1
Important Harmonic Figures in The *D* Branch

	P_s (pu)	Parameter	Value				
			SPF	**CCC**	**GCSC**	**SPVC1**	**SPVC2**
i_{lDa}	1	THD (%)	20.40	21.02	22.99	15.19	16.42
		5th (pu)	0.1855	0.1905	0.1995	0.1500	0.1600
		7th (pu)	0.1151	0.1180	0.1341	0.0637	0.0817
		11th (pu)	0.0377	0.0430	0.0612	0.0140	0.0166
		13th (pu)	0.0246	0.0275	0.0440	0.0055	0.0023
	0.5	THD (%)	24.54	24.93	25.62	23.16	23.73
		5th (pu)	0.1035	0.1048	0.1054	0.1014	0.1031
		7th (pu)	0.0710	0.0710	0.0731	0.0647	0.0670
		11th (pu)	0.0379	0.0393	0.0418	0.0301	0.0378
		13th (pu)	0.0276	0.0279	0.0307	0.0247	0.0189
	1 par.	THD (%)	-	-	21.53	17.38	17.43
		5th (pu)	-	-	0.1940	0.1677	0.1667
		7th (pu)	-	-	0.1201	0.0846	0.0861
		11th (pu)	-	-	0.0480	0.0098	0.0090
		13th (pu)	-	-	0.0312	0.0032	0.0041
i_{sDa}	1	THD (%)	20.28	20.92	23.09	14.95	16.29
		5th (pu)	0.1147	0.1189	0.1239	0.0919	0.0994
		7th (pu)	0.0712	0.0718	0.0824	0.0392	0.0501
		11th (pu)	0.0230	0.0272	0.0384	0.0090	0.0101
		13th (pu)	0.0151	0.0166	0.0268	0.0038	0.0014
	0.5	THD (%)	24.25	24.43	26.09	23.07	23.39
		5th (pu)	0.0640	0.0650	0.0652	0.0622	0.0641
		7th (pu)	0.0442	0.0435	0.0453	0.0405	0.0412
		11th (pu)	0.0231	0.0246	0.0258	0.0185	0.0239
		13th (pu)	0.0171	0.0170	0.0191	0.0157	0.0118
	1 par.	THD (%)	-	-	21.41	17.45	17.56
		5th (pu)	-	-	0.1194	0.1030	0.1049
		7th (pu)	-	-	0.0745	0.0534	0.0522
		11th (pu)	-	-	0.0293	0.0059	0.0065
		13th (pu)	-	-	0.0193	0.0023	0.0020

TABLE 6–2
Important Harmonic Figures in The *Y* Branch

	P_s (pu)	Parameter	Value				
			SPF	**CCC**	**GCSC**	**SPVC1**	**SPVC2**
i_{lYa}	1	THD (%)	20.56	20.99	23.09	14.96	16.61
		5^{th} (pu)	0.1882	0.1898	0.2023	0.1469	0.1597
		7^{th} (pu)	0.1117	0.1188	0.1296	0.0669	0.0786
		11^{th} (pu)	0.0388	0.0432	0.0634	0.0123	0.0158
		13^{th} (pu)	0.0229	0.0282	0.0409	0.0060	0.0027
	0.5	THD (%)	24.74	24.83	25.62	23.11	23.67
		5^{th} (pu)	0.1043	0.1038	0.1056	0.1005	0.1020
		7^{th} (pu)	0.0697	0.0715	0.0725	0.0662	0.0681
		11^{th} (pu)	0.0382	0.0391	0.0424	0.0291	0.0372
		13^{th} (pu)	0.0264	0.0284	0.0298	0.0262	0.0197
	1 par.	THD (%)	-	-	21.51	17.49	17.35
		5^{th} (pu)	-	-	0.1940	0.1683	0.1657
		7^{th} (pu)	-	-	0.1191	0.0861	0.0866
		11^{th} (pu)	-	-	0.0475	0.0103	0.0088
		13^{th} (pu)	-	-	0.0302	0.0034	0.0038
i_{sYa}	1	THD (%)	20.50	20.95	23.05	14.93	16.58
		5^{th} (pu)	0.1164	0.1174	0.1252	0.0909	0.0988
		7^{th} (pu)	0.0691	0.0735	0.0802	0.0414	0.0487
		11^{th} (pu)	0.0240	0.0267	0.0392	0.0076	0.0098
		13^{th} (pu)	0.0142	0.0174	0.0253	0.0037	0.0017
	0.5	THD (%)	24.61	24.72	25.52	23.02	23.58
		5^{th} (pu)	0.0646	0.0642	0.0653	0.0622	0.0631
		7^{th} (pu)	0.0431	0.0442	0.0448	0.0410	0.0421
		11^{th} (pu)	0.0237	0.0242	0.0263	0.0180	0.0230
		13^{th} (pu)	0.0164	0.0175	0.0184	0.0162	0.0122
	1 par.	THD (%)	-	-	21.45	17.45	17.31
		5^{th} (pu)	-	-	0.1200	0.1041	0.1025
		7^{th} (pu)	-	-	0.0737	0.0533	0.0536
		11^{th} (pu)	-	-	0.0294	0.0063	0.0055
		13^{th} (pu)	-	-	0.0187	0.0021	0.0023

The behavioural pattern with regards to harmonics for i_{sa} is tabulated in TABLE 6–3. The THD in the full-load fully-compensated case is slightly larger with SPVC2 than that with SPVC1. The magnitude of the 11^{th} harmonic is slightly larger with SPVC2 than that with SPVC1. The situation reverses when it comes to the magnitude of the 13^{th} harmonic which is less than half the value of what was obtained with SPVC1. The pattern is almost the same with 0.5-pu active power and full compensation being provided by the SPVC. The THD and harmonic magnitudes with 1-pu active power and partial series compensation is almost identical to the SPVC1 approach; with the magnitudes of the 11^{th} and the 13^{th} harmonics being a little less with SPVC2 than with SPVC1.

TABLE 6–3
Important Harmonic Figures in the Combined Terminal Current

	P_s (pu)	Parameter	Value				
			SPF	**CCC**	**GCSC**	**SPVC1**	**SPVC2**
i_{sa}	1	THD (%)	4.31	4.87	6.97	1.64	1.73
		5^{th} (pu)	0.0027	0.0015	0.0021	0.0024	0.0010
		7^{th} (pu)	0.0027	0.0021	0.0030	0.0025	0.0015
		11^{th} (pu)	0.0470	0.0539	0.0776	0.0166	0.0198
		13^{th} (pu)	0.0293	0.0340	0.0522	0.0075	0.0030
	0.5	THD (%)	8.51	8.78	9.69	7.20	7.70
		5^{th} (pu)	0.0017	0.0008	0.0003	0.0011	0.0010
		7^{th} (pu)	0.0015	0.0010	0.0006	0.0016	0.0009
		11^{th} (pu)	0.0468	0.0487	0.0520	0.0365	0.0469
		13^{th} (pu)	0.0334	0.0345	0.0375	0.0319	0.0240
	1 par.	THD (%)	-	-	5.31	1.25	1.26
		5^{th} (pu)	-	-	0.0009	0.0015	0.0026
		7^{th} (pu)	-	-	0.0009	0.0004	0.0018
		11^{th} (pu)	-	-	0.0587	0.0123	0.0119
		13^{th} (pu)	-	-	0.0379	0.0045	0.0043

A visual representation of the comparative THD values is shown in Fig. 6–23. A rising trend can be observed in all the cases from SPF to GCSC. However, this changes with SPVC1 and SPVC2 topologies as the THD values for full power with full and partial compensation cases is reduced significantly. However, the reduction in THD values is not as drastic when the active power flow is reduced. This is because of lesser effect of SPVC on the overlap angle at lower load.

Comparisons of the most significant harmonics in i_{sa} (i.e. the 11^{th} and the 13^{th}) are also important. These can be observed in Fig. 6–24 and Fig. 6–25. A similar trend appears where the 11^{th} and the 13^{th} harmonics increase in magnitude from SPF to GCSC topologies; but decrease significantly with the use of SPVC1 and SPVC2. A second observation is the change in the harmonic magnitude with the change in active power. The change is not significant with the classical SPF compensation. For CCC and GCSC, the 11^{th} harmonic magnitude drops with drop in active power. It however is higher in magnitude than that with SPF. This change is more prominent with SPVC1 and SPVC2 approaches; even though the harmonic magnitudes with half power are still observed to be lower than those with SPF approach. The magnitude of the 11^{th} is lower with SPVC1 and that of the 13^{th} is lower with SPVC2 for all cases. The SPF and CCC cannot perform partial reactive-power compensation as ordered. The GCSC, SPVC1, and SPVC2 can be compared for this case. The THD and significant harmonic amplitudes for this case are almost the same for SPVC1 and SPVC2 and much lower than the corresponding values with the GCSC.

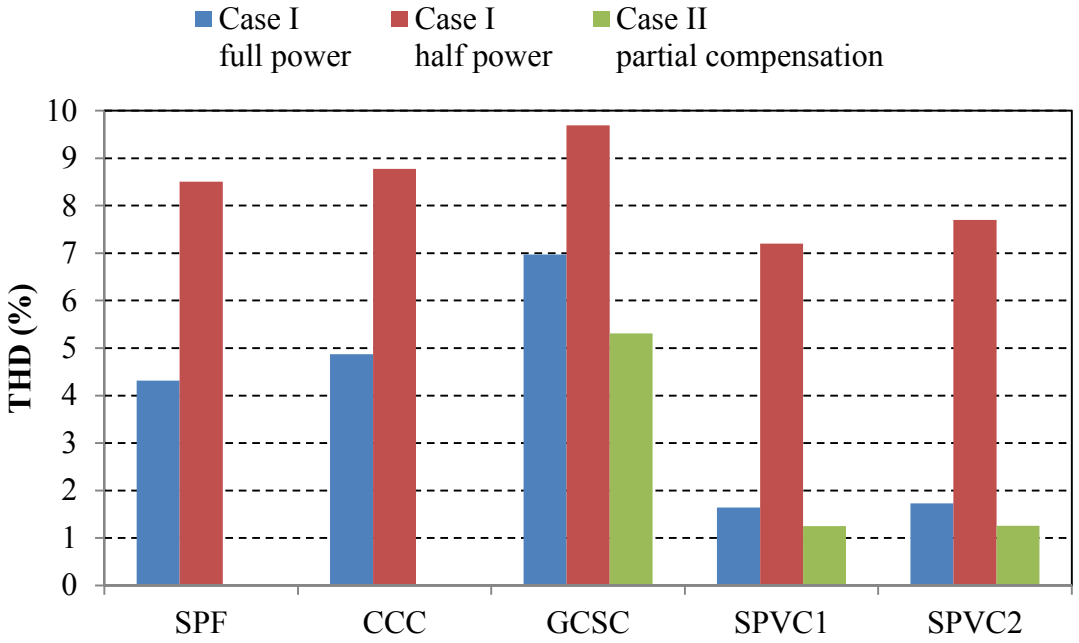

Fig. 6–23. Comparative THD values for i_{sa} for different compensation solutions

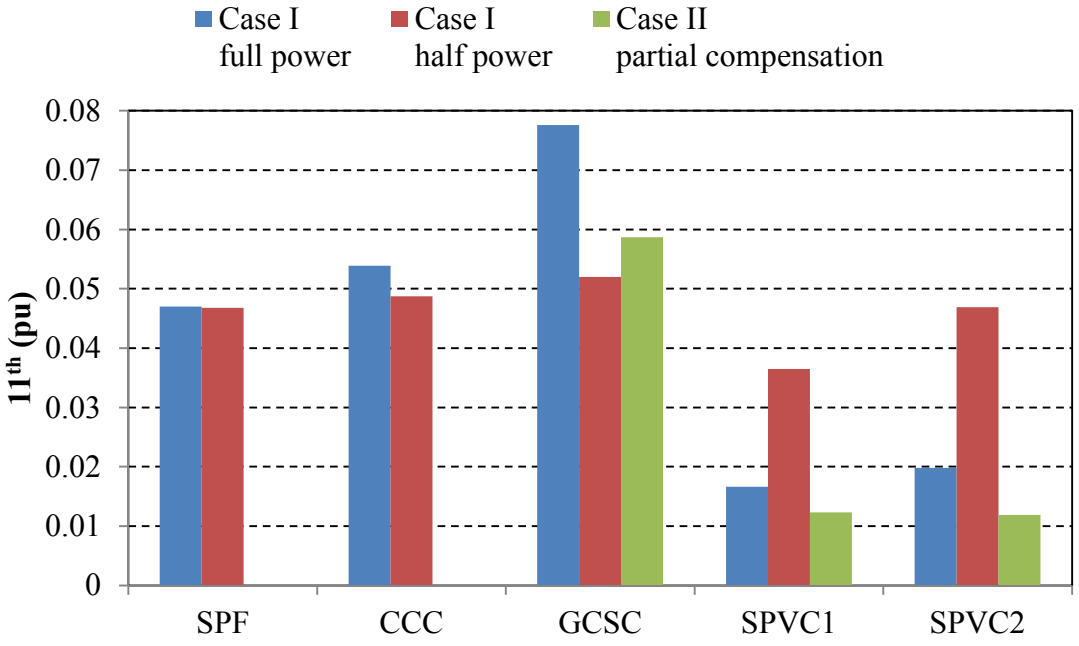

Fig. 6–24. Comparison of 11th harmonic values for different compensation solutions

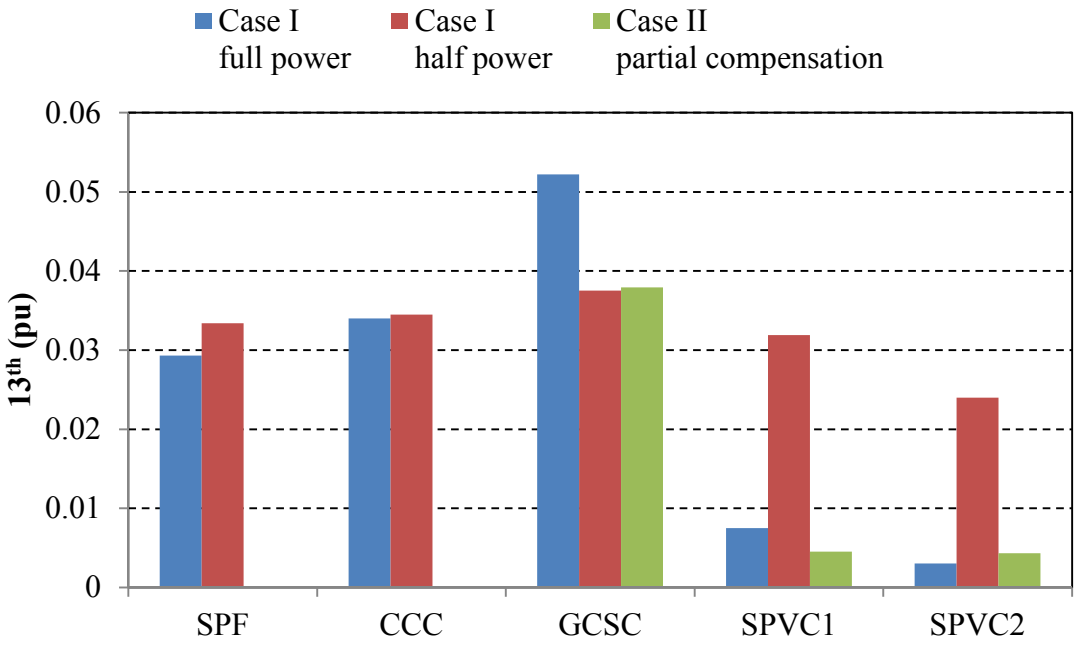

Fig. 6–25. Comparison of 13th harmonic values for different compensation solutions

In brief, the SPVC1 approach showed a better harmonic performance than SPVC2 and would reduce the size of the shunt filters to a larger extent than SPVC2. However, with the phase-angle-control capability achieved with SPVC2, it is possible to get better results by locating the charging instants at more suitable points in time. The charging can even be distributed into more than one distinct period in the conduction zone of a specific SPVC leg to achieve better active-power filtering, and hence, better harmonic behaviour.

6.6 Proof of Concept

An experimental setup was built to validate the results of the simulations carried out in this chapter. The construction and results of the experiments performed are presented in this section.

6.6.1 Experimental Setup

The schematic of the experimental setup is shown in Fig. 6–26. As can be seen, this is a 6-pulse system with the proposed SPVC connected in each phase. The inverter side was emulated by a programmable DC load. This load could act in constant-voltage or constant-current modes. The controller was a custom DSP board with the capability of forcing values on to certain variables in the program. The AC voltage was 200 V rms line to line. A few pictures of the experimental setup are given in Fig. 6–27 through Fig. 6–34 with the explanations in the captions.

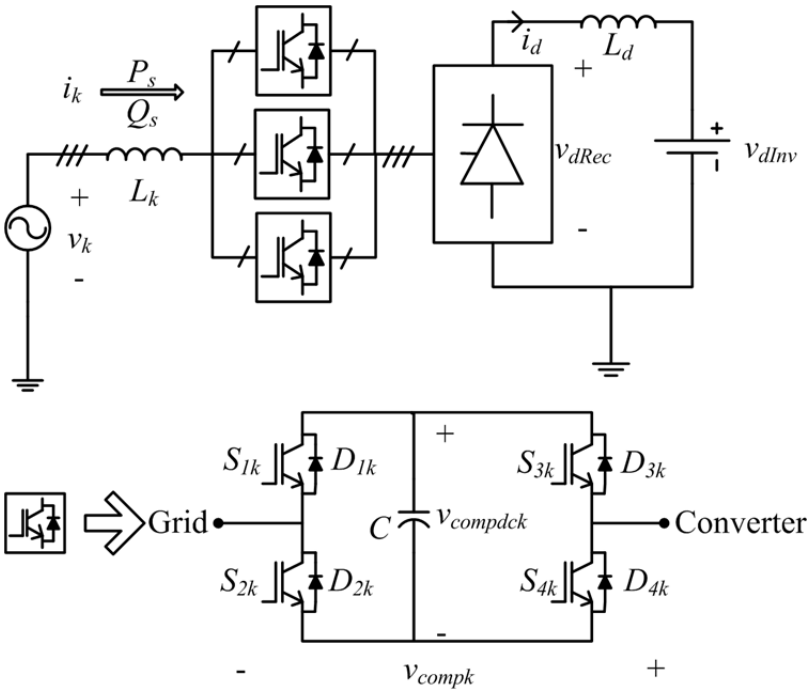

Fig. 6–26. Schematic of the experimental setup. L_k = 10 mH, L_d = 80 mH, and C = 50 μF

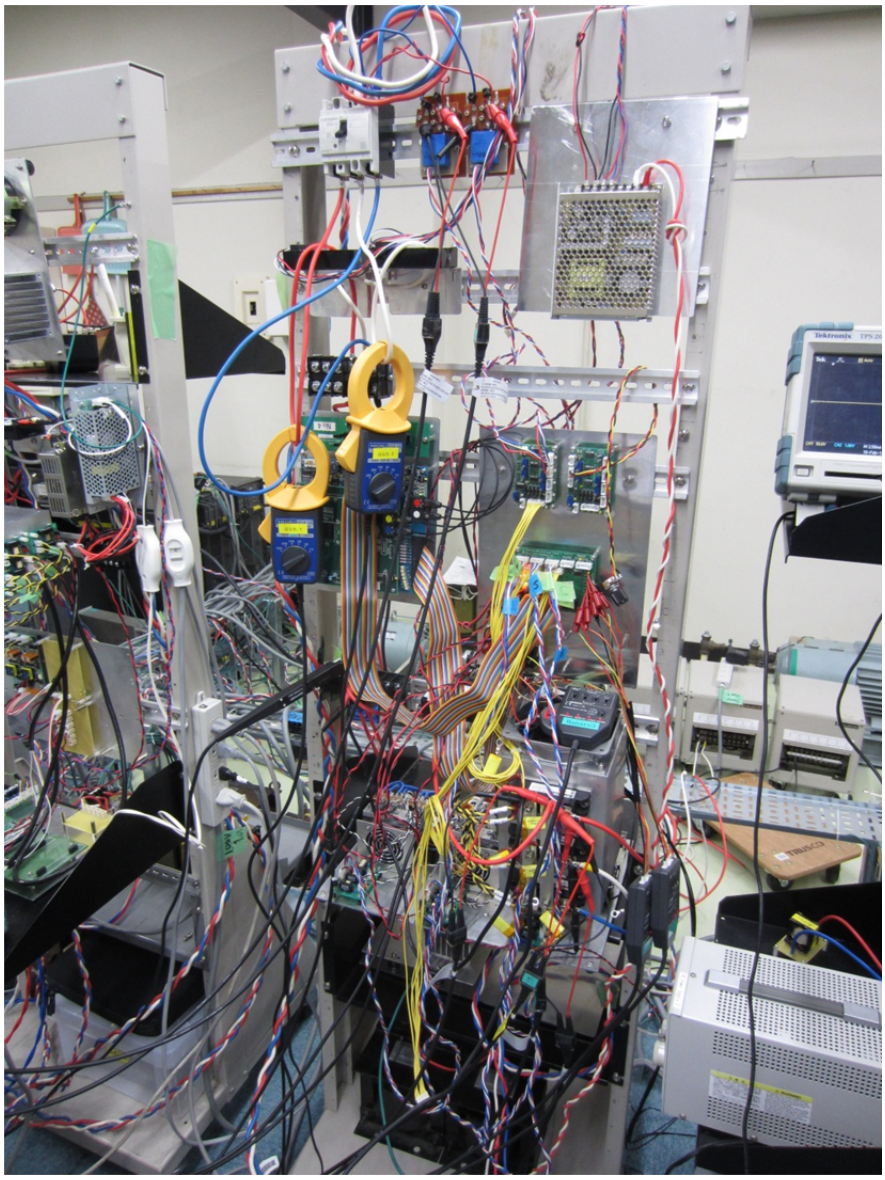

Fig. 6–27. Photograph of the experimental setup.

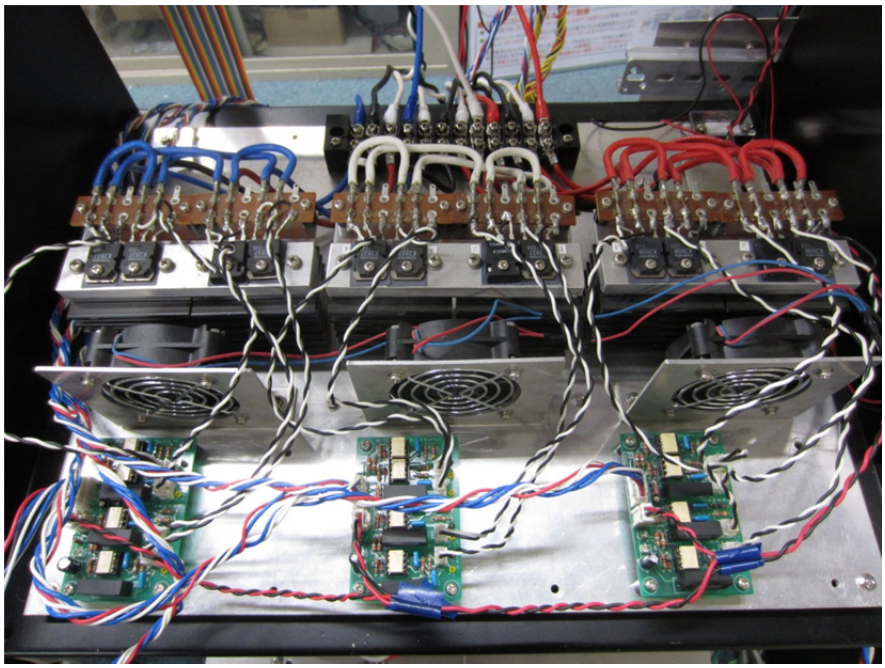

Fig. 6–28. The 3-phase series compensator with associated gate drivers and cooling fans.

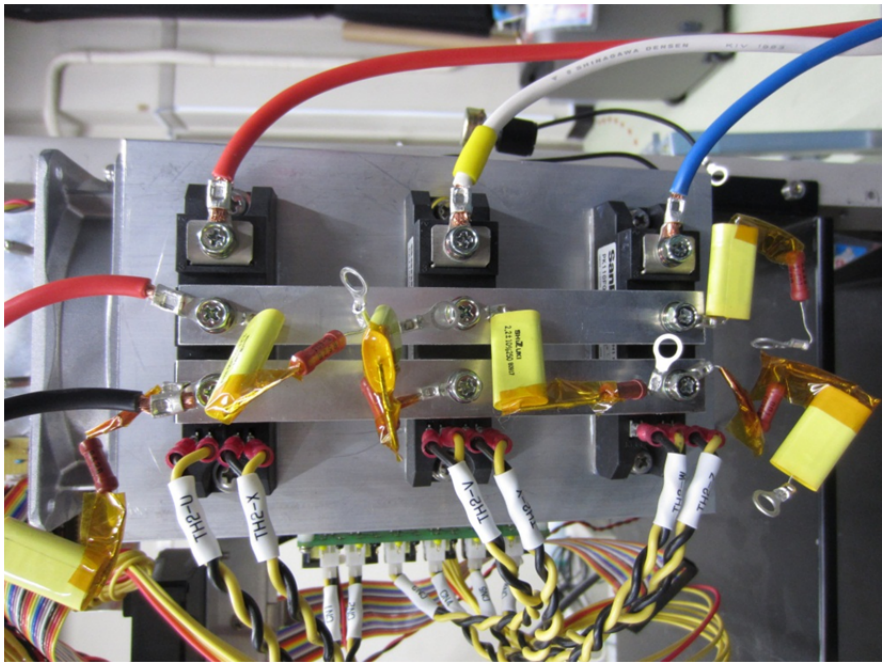

Fig. 6–29. The 6-pulse thyristor rectifier with the gate driver and cabling.

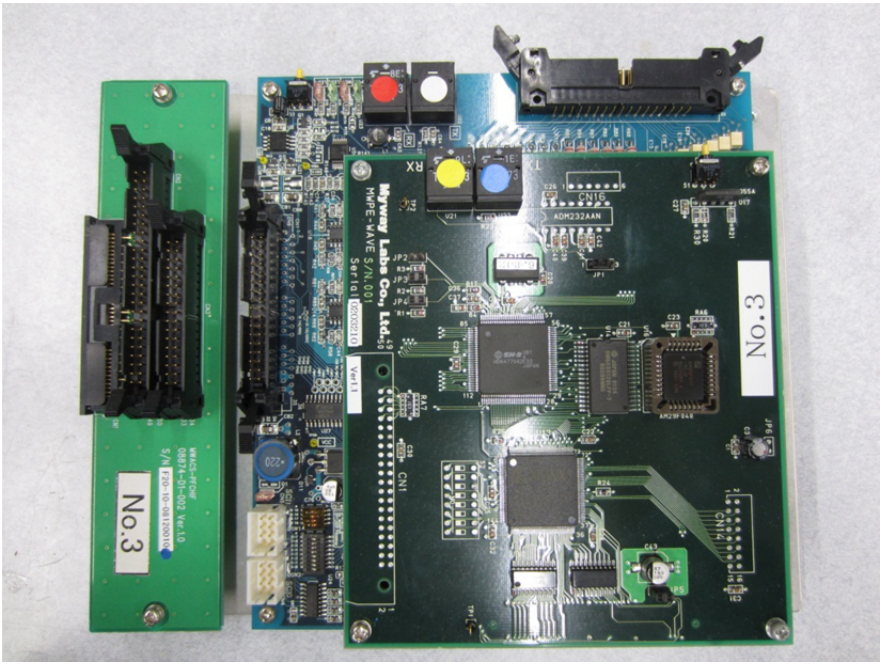

Fig. 6–30. The DSP control board

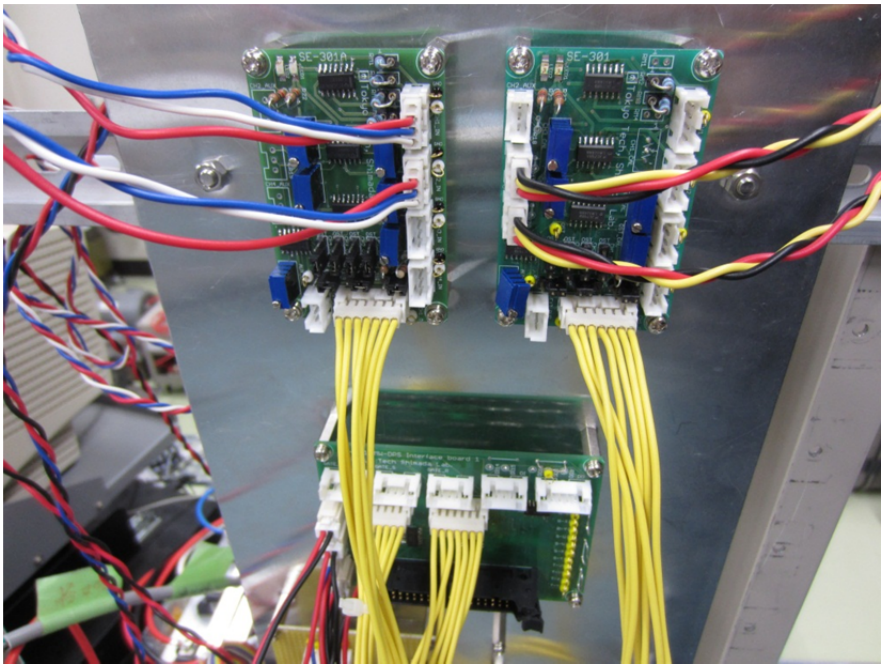

Fig. 6–31. Control and signal interface boards

Fig. 6–32. The AC inductors

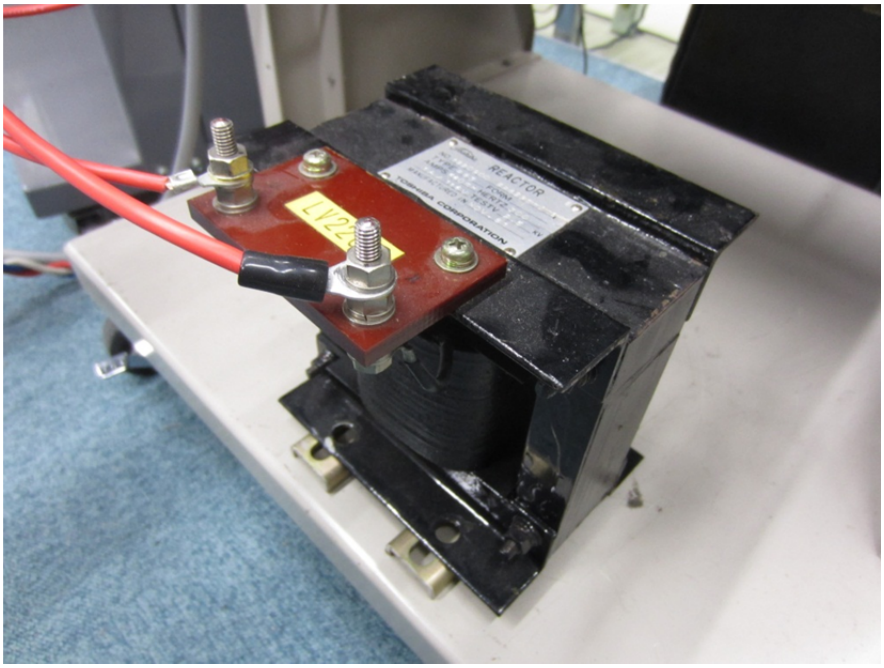

Fig. 6–33. The DC inductor

Fig. 6–34. The SPVC DC-link capacitor

6.6.2 Simplifications

The following simplifications were made to reduce the task load on the controller:

1. The programmable DC load was used in constant-current mode as mentioned above. The effect was the removal of the control loop in Fig. 3–2 and a constant value of $\alpha = 15°$ could be used throughout the experiments.
2. The value of γ_{charge} was forced manually, thus eliminating the requirement of the control loop in Fig. 6–1. The first set of measurements was collected with $\gamma_{charge} = 0$ to get the active and reactive powers for uncompensated case. γ_{charge} was gradually increased with one set of readings taken for each of its value.
3. No shunt passive filter arrangement was used. The active and reactive-power measurements were taken at the source.
4. The source AC voltage was held constant to eliminate the need of the control loop in Fig. 2–6 as well as controlling equipment.

6.6.3 Procedure

As mentioned above, the value of γ_{charge} was gradually increased starting from zero to ascertain the uncompensated system parameters first and then the effect of gradually increasing compensation voltages. The physical measurements were that of voltage and current. The data were recorded using a multi-channel recorder for a period of 10 cycles with a recording time step of 10 μs. Thereafter, the data were converted into comma-separated-variable (CSV) format by the software provided by the recorder manufacturer. Afterwards, it was imported into MATLAB® workspace and calculations for active and reactive power, as well as harmonic analyses were performed using

Simulink® models with standard blocks from SimPowerSystems® library. Two sets of experiments were performed, the first for I_d = 3 A (case I) and the second for I_d = 5 A (case II).

6.6.4 Results for Case I

The values of important parameters in the system are tabulated in TABLE 6–4. The first row corresponds to the measurements and calculations without SPVC. P_s and Q_s values are the uncompensated values.

TABLE 6–4
Experimental Results for Case I

γ_{charge} (rad)	V_{dRec} (V)	V_{dInv} (V)	V_{comp} (V)	P_s (W)	Q_s (VAR)	Q_{comp} (VAR)
0.0000	246.4	245.6	0.0	780	300	0
0.0499	248.4	247.5	12.0	786	267	12
0.0700	249.8	249.0	17.5	788	258	20
0.0901	251.1	250.3	20.5	795	243	22
0.1100	251.6	250.8	23.5	795	231	27
0.1300	252.3	251.4	26.2	795	225	30
0.1499	254.1	253.3	29.0	801	216	36
0.2499	257.8	257.0	49.5	816	162	66
0.3499	256.8	256.0	66.5	810	102	96
0.4000	261.4	260.6	75.5	822	78	120

As γ_{charge} started to increase, it was observed that V_{dRec} also increased. The programmable DC load increased V_{dInv} to keep I_d at 3 A. Consequently, the DC-link power as well as P_s increased. The action of SPVC reduced Q_s and increased Q_{comp}. However, the decrease in Q_s was more than the corresponding increase in Q_{comp}. With maximum compensation being provided by SPVC (corresponding to the last row in TABLE 6–4), Q_s dropped by 222 VAR (from 300 VAR to 78 VAR) and the increase in Q_{comp} was 120 VAR (from 0 VAR to 120 VAR). Therefore, the SPVC was not only acting as a reactive-power compensator but also as a reactive-power inhibitor.

Selected instantaneous variables corresponding to experimental data in the first and last row of TABLE 6–4 are plotted in Fig. 6–35 and Fig. 6–36, respectively. It is clear that there is a gap between the zero-crossing of v_{ab} and the start of current commutation to phase *b* without SPVC. The series voltage injected by the SPVC forces commutating voltage to cross earlier and allows the current to commutate earlier, resulting into lower reactive power seen by the source. It is also evident that the discharge and charge instants and timings are as seen in the simulation results.

The harmonic analysis of i_b is presented in TABLE 6–5. The term "Before" refers to the uncompensated system (Fig. 6–35) and the term "After" refers to the case with maximum compensation (Fig. 6–36). The difference in the amplitudes without and

with SPVC is not significant. However, the phase shift in the harmonics is not proportional to the phase shift in the fundamental waveforms. The total current in a 12-pulse configuration is the sum of two such currents translated to the primaries. The altered phase of the harmonics in the constituent currents from the *D* and *Y* branches would help cancel the harmonics more effectively.

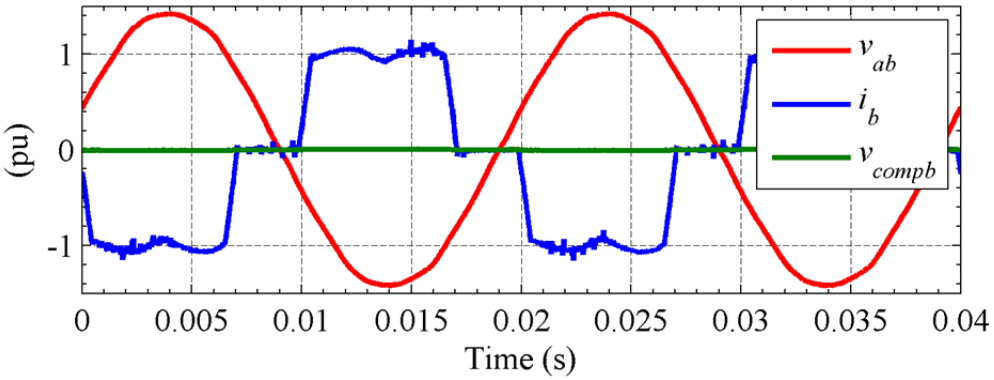

Fig. 6–35. Instantaneous waveforms for case I without compensation.

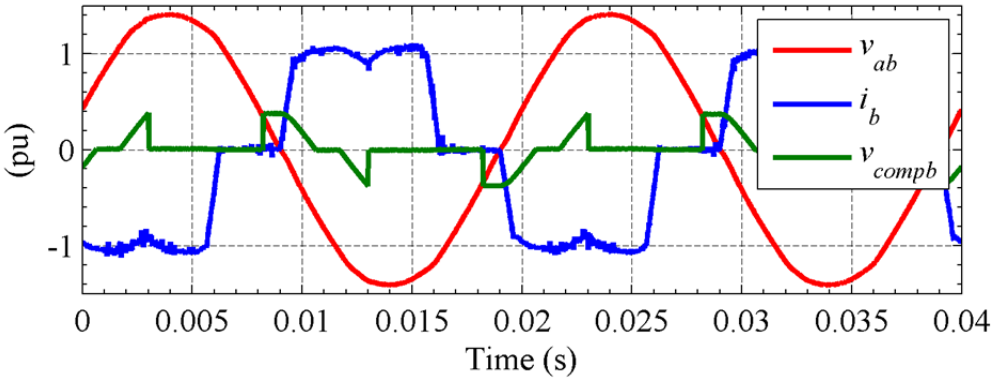

Fig. 6–36. Instantaneous waveforms for case I with maximum compensation.

TABLE 6–5
Harmonic Analysis for Case I

Harmonic order	**Magnitude (A)**		**Phase (°)**	
	Before	**After**	**Before**	**After**
Fundamental	3.3530	3.3400	–151.2	–138.3
5^{th}	0.7285	0.7272	140.9	–158.7
7^{th}	0.3764	0.3691	–150.0	–60.8
11^{th}	0.2526	0.2492	138.3	–87.9
13^{th}	0.1864	0.1716	–158.8	11.08

6.6.5 Results for Case II

The important parameters for this case with gradually increasing values of γ_{charge} are given in TABLE 6–6. The steady-state value of P_s increases as γ_{charge} increases from 0 to 0.13 radians. This is because the reduction in reactive-power demand on the source enables more active-power flow possible which is indicated by increased V_{dRec}. V_{dInv} increases to keep I_d at a constant level of 5 A. However, increased values of these voltages produce larger DC-link power as well as larger P_s. On the other hand, Q_s continues to drop as more and more compensation is provided by the SPVC with increasing injected voltage. Again, the change in Q_s is 195, whereas that in Q_{comp} is 105.

TABLE 6–6
Experimental Results for Case II

γ_{charge} (rad)	V_{dRec} (V)	V_{dInv} (V)	V_{comp} (V)	P_s (W)	Q_s (VAR)	Q_{comp} (VAR)
0.0000	236.7	235.6	0.0	1251	546	0
0.0499	242.8	241.6	25.5	1275	468	48
0.0901	247.6	245.5	40.0	1306	411	75
0.1300	250.1	249.0	50.0	1320	351	105

The instantaneous plots of selected variables for this case without and with SPVC connected are shown in Fig. 6–37 and Fig. 6–38 respectively. These are similar to the plots for case I (Fig. 6–35 and Fig. 6–36).

The harmonic analysis of i_b in case II is given in TABLE 6–7. Like in case I, the change in the magnitude of the harmonics is insignificant. However, the change in the phase is significant and is responsible for a more effective cancellation of these when the currents add up in the primaries of the converter transformers.

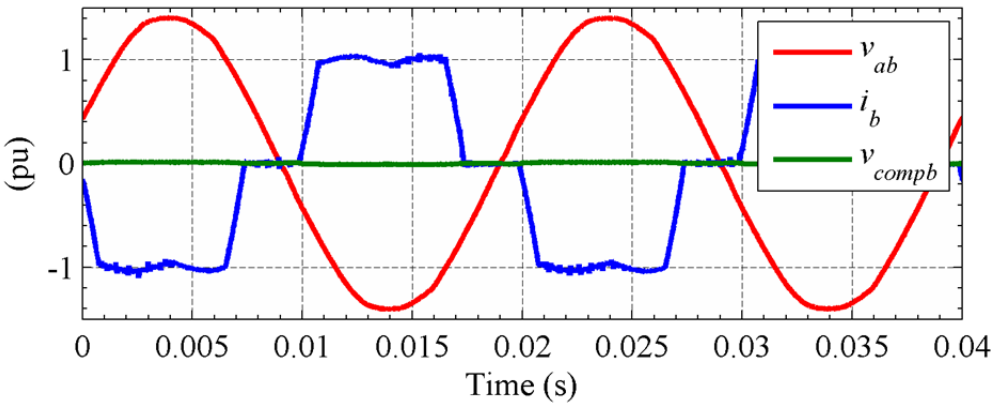

Fig. 6–37. Instantaneous waveforms for case II without compensation.

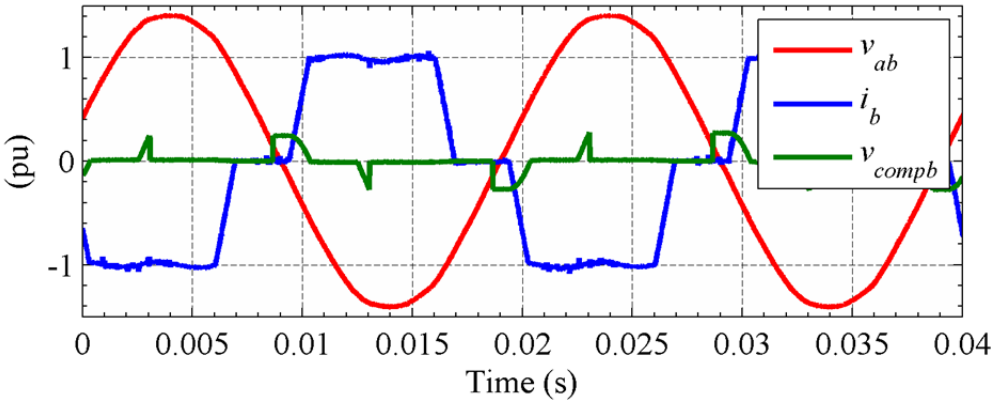

Fig. 6–38. Instantaneous waveforms for case II with maximum compensation.

TABLE 6–7
Harmonic Analysis for Case II

Harmonic order	Magnitude (A)		Phase (°)	
	Before	After	Before	After
Fundamental	5.511	5.499	–154.9	–144.7
5th	1.093	1.079	121.9	172.6
7th	0.6066	0.6167	–179.7	–110.5
11th	0.3194	0.3264	93.4	–153.8
13th	0.2312	0.2199	147.3	–82.4

6.7 Estimated Area Reduction

We will get a rough idea about the reduction in area requirements for an HVDC station incorporating the SPVC as a reactive/harmonic compensator. This will be estimated on the basis of Fig. 1–5 and TABLE 1–1.

The additional equipment required is the SPVC. Even though the SPVC compensator would have much smaller peak and rms current and voltage ratings than the main AC/DC conversion bridges, we assume conservatively that it will take up almost the same area as the main AC/DC converters. This leads us to add 18%. The estimated reductions are as under:

1. The shunt capacitor banks purely intended for reactive-power compensation would no longer be required giving a saving of 28%.
2. The impedance of the tuned and high-pass filters is capacitive at fundamental frequency, i.e. these behave as sources of fundamental-frequency reactive power. In a conventional shunt-compensated terminal, the capacitors are large in order to share more of the reactive power. This would no longer be required with the use of SPVC. As the filtering requirement is not fully eliminated and they have to employ capacitors, smaller capacitors can be incorporated in the

design of the passive filters. We assume a conservative reduction of 40% on the size of the tuned and high-pass filters.

3. As the SPVC would improve the harmonic behaviour of the terminal, a 10% reduction in the size of 11^{th} and 13^{th} harmonic is assumed.

Based on the assumptions made above, the reduced areas of the respective system components are given in TABLE 6–8. This means that there would roughly be an estimated reduction of 37% in the area taken up by the concerned system components.

TABLE 6–8
% Area Reduction due in Terminal Size with SPVC

Equipment	**% Area**	
	SPF	**SPVC**
Thyristor valve hall	18	18
SPVC	0	18
High-pass filter	20	10
11^{th} harmonic filter	21	10
13^{th} harmonic filter	13	7
Shunt capacitors	28	0
Total	**100**	**63**

It has to be emphasized that these estimates cannot be verified before the design of the new tuned and high-pass filters with smaller capacitors; which is beyond the scope of this work.

It should also be noted that the calculations involve the total area taken up by the main AC/DC converters, SPVC, filters, and shunt capacitors. The AC and DC switchyard layout also take up space and have not been considered for this estimate. The ultimate design of an offshore platform could alter the switchyard layout; therefore, a definitive statement about the overall area reduction cannot be made.

6.7.1 Alternative Calculation

An interesting comparison in [104] provides a good understanding for performing the calculations of site area requirement. The authors belong to Asea Brown Boveri (ABB), one of the major suppliers of turnkey HVDC projects for more than 50 years. They present a comparison of two projects of equivalent power and voltage ratings on the AC and DC sides, one of which is based on LCC HVDC technology and the other on the more recent two-level VSC HVDC technology. The LCC HVDC project was commissioned in 2001 and the VSC HVDC project in 2012. Both the projects are rated at 500 MW, 400 kV DC. Later the authors calculate the parameters for the more recent modular multi-level converter based VSC HVDC (MMC HVDC) technology and compare them to the parameters of LCC and VSC topologies. The LCC HVDC parameter values have been taken as base for calculation of percentage values.

It can be seen here again that the valve building occupies only 2.59% of the total site area with the rest taken up by the AC and DC switchyards and filtering equipment. The relative size of the valve building to the total site area for two-level VSC HVDC is higher at 6.42%. This is because of the lower area required by the harmonic filters. The valve building area is almost twice as big as that in the case of LCC HVDC.

TABLE 6–9
Comparison of LCC HVDC and VSC HVDC Project Site Parameters

Parameter	**LCC HVDC**	**VSC HVDC**
HVDC site footprint	225m × 120m	180m × 150m
HVDC site area	27,000 m^2	20,700 m^2
(per cent)	(100%)	(77%)
Maximum building height	20 m	24m
(per cent)	(100%)	(120%)
Converter building footprint	35m × 20m	38m × 35m
Converter building area	700 m^2	1,330 m^2
(per cent)	(100%)	(190%)
Converter building area as per cent of site area	2.59%	6.42%

If the LCC HVDC is equipped with SPVC which consist of 6 full bridges, one in each phase leg between the converter transformers and the thyristor bridges, the total number of valves would be 24. The total number of valves in a symmetrical monoplar VSC HVDC station is 6. The ratio becomes 4. The voltage rating of a valve is one of the major determining factors for the size. The approximate size would be:

$$A_{SPVC} = 4 \times k_{valve} \times A_{VSC,HVDC} \times \frac{V_{SPVC}}{V_{VSC,HVDC}} \tag{6.12}$$

where, k_{valve} is the ratio of the area covered by the valves in the converter building to the total area of the converter building. We assume a value of 0.8 for this constant.

Putting in the values A_{SPVC} is calculated to be equal to 1600 m^2. The area of the thyristor building for a 1000 MW system would be double that of a 500 MW station and is calculated to be 1400 m^2. This is almost the same area as calculated for SPVC valves validating the assumptions made in the calculations in TABLE 6–8.

6.8 Conclusion

A phase-angle approach to control the instants and timing of series-voltage injection by the SPVC has been presented in this chapter. Simulation results show that the

mathematical development performs according to the concept developed in the preceding chapter.

Experimental results from a small-scale laboratory setup validate the SPVC concept. The results also verify the claim that the reactive-power consumption of the thyristor converters is reduced with the injection of series voltages.

It has been observed that the harmonic performance is comparatively worse than that in the preceding chapter. This is because we aimed to inject recharging voltages about the midpoint of the conduction period in a single half-cycle. It was observed that the location of recharging pulses was not absolutely about the midpoint of the conduction period. It is possible that the location of recharging pulses discussed in the previous chapter is a better option. The control is developed in such a manner that these charging injections can be located anywhere in the conduction zone of a specific phase. Further testing by displacing these injections can reveal more about the harmonic performance.

The number of SPVC modules for a standard 12-pulse LCC HVDC terminal is six. The module in each phase has 8 power-electronic switches (4 IGBTs and 4 diodes). This makes a total of 48 additional power-electronic devices compared to the removal of most of the capacitance in the shunt passive filters. Theoretically, it is possible to control the entire reactive-power demand of the terminal with SPVCs in one of the two branches. This would reduce the number of power-electronic switches to half of what it is in the proposed form. It may have the implication of higher injected-voltage magnitudes, as well as different harmonic content.

The higher number of power-electronic switches would offset the gain in size and volume achieved through the removal of shunt capacitor banks. How much benefit it offers needs to be investigated further.

The switching losses would be much lower as compared to the STATCOM or SSSC solutions. However, the conduction losses remain a concern as current would always flow through a pair of power-electronic devices whenever a phase is carrying current. This needs further investigation.

7 Conclusions and Future Work

Some concluding remarks and a few proposals for future work are briefly discussed in this chapter.

7.1 Conclusions

The main conclusions from the work presented above are as under:

7.1.1 Application of the Gate-Commutated Series Capacitor to LCC HVDC

An alternative to CCC HVDC for reactive-power compensation of LCC HVDC was proposed. It was based on the Gate-Commutated Series Capacitor (GCSC). The capability of the proposed compensator to follow the reactive-power reference irrespective of the active-power flow was demonstrated through simulations.

It was observed that the GCSC approach had a negative impact on the harmonic behaviour of the system even in comparison with CCC HVDC topology. This would necessitate larger passive harmonic filters on the AC side.

7.1.2 The Series Pulsed-Voltage Compensator (SPVC)

A series compensator which injects series voltages to inhibit and compensate for the large reactive-power consumption of a line-commutated converter based HVDC (LCC HVDC) rectifier terminal has been proposed. The details of its construction as well as operation & control have been explained. The control & operation of the compensator with phase-angle control has also been explained. The proposed compensator would use very small capacitors as compared to those used in the conventional shunt-compensated topology or the capacitor-commutated converter based HVDC (CCC HVDC). The name Series Pulsed Voltage Compensator (SPVC) was suggested for the proposed compensator. It was indicated that the SPVC could utilize polarized capacitors as opposed to the ones in the shunt passive filters, leading to more compactness.

It was observed that the SPVC also contributed positively to the harmonic behaviour of LCC HVDC terminal. This would help reduce the size of tuned and high-pass filters on the AC side.

The GCSC could not use polarized capacitors, which could offset the gains obtained by the use of fewer power-electronic switches. The peak-to-peak voltage ratings of these capacitors would be higher than the peak voltage rating of the SPVC capacitors, as indicated by the simulation results.

The proposal was tested on a small-scale laboratory setup with a few simplifications and insightful results were obtained.

7.2 Future Work

In the lines below, a few proposals for taking the work in this research forward are being presented.

7.2.1 Improvement in Harmonic Compensation with the SPVC

The harmonic compensation achieved with the two control strategies discussed in chapters 5 and 6 was different. Further work needs to be done to improve the harmonic performance of SPVC and make it more predictable. The SPVC discharges during the commutation process and charges when the current is flowing through the concerned phase. It is possible to achieve better harmonic compensation if the frequency of charge and discharge per half-cycle increases. Further investigation of the matter should be taken up to further reduce the shunt harmonic filter requirement.

7.2.2 Power-Flow Control with the SPVC and Diode Rectifier

The SPVC can be used, in principal, to control the flow of power. This makes the need for the thyristor on the rectifier redundant. Further work should be done to demonstrate the capability. This could further simplify the control of HVDC rectifier terminal in addition to reduction in size and costs.

7.2.3 Reduction in the Number of Switches in the SPVC

The SPVC proposed in this work is comprised of a full bridge in each phase. It may be possible to use a half-bridge arrangement to achieve the same functionality. The two-switch-per-phase option, the GCSC, contributes negatively to the harmonic problem. Mixing the two approaches of the SPVC and GCSC can be interesting

7.2.4 Series Compensator on the DC Side of HVDC Link for Harmonic Compensation

It may be possible to achieve harmonic compensation at the least, through the use of a compensator connected in series on the DC link of the main HVDC converter.

7.2.5 Black Start of Wind Farm using LCC HVDC

LCC HVDC is, in a manner, analogous to an induction generator. Historically, the induction generator is understood to require a source to start the export of power, so does LCC HVDC. However, an induction machine can start feeding a dead network with the help of shunt capacitor banks. Similar capacitor banks are connected to any LCC HVDC terminal and it should be possible to start-up such networks, provided that the DC Link is live. Simulation and implementation of this idea should be carried out.

7.2.6 GCSC with Lower Harmonic Pollution

The implementation of the GCSC discussed in this work aggravates the harmonic problem. Other control techniques for GCSC should be investigated, which could achieve reactive-power compensation but with reduced harmonic content.

Appendices

A Active Power Filtering of SPVC-Compensated LCC HVDC with Conservative Power Theory

The details of shunt active-power filtering using the modified conservative power theory applied to series-compensated HVDC link are discussed in the appendix. Simulation results, in addition to mathematical modelling of the modified theory are presented.

The work in the thesis presented the LCC HVDC terminals with shunt passive filters. It was observed that the shunt passive filter would always inject reactive power into the system based on the voltage at the point of connection of the filter, irrespective of the demand of reactive power from the converters. This signifies the classic behaviour of these filters which necessitates switching of capacitor banks based on the reactive-power demand.

In this appendix, we present a shunt active-power filter (SAPF) [105-107] based on the conservative power theory (CPT) [108]. The theory is one of a series of theories related to the definitions of different power terms with non-sinusoidal currents and voltages [109-112]. In the beginning, it was an academic exercise. But with the emergence of non-linear loads, it has become very important to compensate for the polluting currents and non-active power flow. This is necessary to ensure voltage quality at any connection point on the grid and maximum power-transmission capacity in today's already-congested grids.

The simulations in this chapter would also highlight the precise advantage of the SPVC proposed in the previous chapters, as the SAPF would only inject currents to eliminate harmonic-/reactive-power flow in the grid.

A.1 Conservative Power Theory

Conservative power theory is a recent addition to other theories related to understanding and compensating non-sinusoidal systems [113]. We will only discuss and present the concepts and equations of interest to the compensation requirements of our system. As with several other theories, the conservative power theory defines the instantaneous power first which is given by:

$$p = \underline{v} \circ \underline{i} = \sum_{k=1}^{3} v_{spk} i_{sk} = \sum_{k=1}^{3} p_k \tag{A.1}$$

where, p is the total instantaneous power, $\underline{v}$ is the vector of three phase-voltages measured from an arbitrary point which minimizes its **norm**, $\underline{i}$ is the vector of three-phase currents, v_{spk} is the k-phase voltage at the point of connection of the SAPF, i_{sk} is the line current in phase k into the load, and p_k is the instantaneous power in phase k. Next, the theory introduces the concept of instantaneous reactive energy given by:

$$w = \underline{\widehat{v}} \circ \underline{i} = \sum_{k=1}^{3} \widehat{v}_{spk} i_{sk} = \sum_{k=1}^{3} w_k \tag{A.2}$$

where, w is the total instantaneous reactive energy, $\widehat{v}_{spk}$ is the unbiased voltage integral in phase k, and w_k is the instantaneous reactive energy in phase k.

The unbiased integral is formulated as:

$$\widehat{v}_{spk} = v_{spk\int} - \overline{v}_{spk\int} = \int_0^t v_{spk}(\tau) d\tau - \frac{1}{T} \int_0^T \left(\int_0^t v_{spk}(\tau) d\tau \right) dt \tag{A.3}$$

Average values of quantities in (A.1) and (A.2) are of interest to this theory and are calculated using:

$$P = \sum_{k=1}^{3} P_k = \sum_{k=1}^{3} \left(\frac{1}{T} \int_0^T v_{spk} i_{sk} dt \right) \tag{A.4}$$

$$W = \sum_{k=1}^{3} W_k = \sum_{k=1}^{3} \left(\frac{1}{T} \int_0^T \widehat{v}_{spk} i_{sk} dt \right) \tag{A.5}$$

where, P is the total average power, P_k is the average power of phase k, W is the total average reactive energy, and W_k is the average reactive energy in phase k.

Next is the collective rms value or vector norm of the voltages, unbiased voltage integrals or currents which is calculated using the formula:

$$\boldsymbol{X} = \|\underline{x}\| = \sqrt{\sum_{k=1}^{3} \langle x_k, x_k \rangle} = \sqrt{\sum_{k=1}^{3} X_k^2} \tag{A.6}$$

where, $\boldsymbol{X}$ is the vector norm or collective rms value; $\underline{x}$ is the vector of the voltages, unbiased voltage integrals, or currents in the three phases; x_k is the variable under consideration which can be a voltage, an unbiased voltage integral, or current in phase k; and X_k is the rms value of the variable under consideration in phase k.

With all the terms defined above, current is decomposed into three parts. These are the active current, the reactive current, and the void current. The active current is defined as the current which is in phase with the respective phase voltage:

$$\underline{i}_a = \frac{P}{\boldsymbol{V}^2}\underline{v} \tag{A.7}$$

where, $\underline{i}_a$ is the vector of active currents. It can be seen that the active currents would be in phase with the phase voltages and will possess harmonics in the same proportions as present in the voltages. The reactive current is defined as:

$$\underline{i}_r = \frac{W}{\widehat{\boldsymbol{V}}^2}\underline{\widehat{v}} \tag{A.8}$$

where, $\underline{i}_r$ is the vector of reactive currents. The reactive current in each phase would be proportional to the unbiased voltage integral and would possess a similar wave-shape. In the case of purely sinusoidal voltages, the unbiased integrals of the voltages would be pure sinusoids and would lag the phase voltages by 90°, hence the reactive currents would also be sinusoidal and lag the phase voltages by 90°. This is equivalent to the quadrature current in the dq theory. The last set of currents to be calculated is that of the void currents and is obtained by:

$$\underline{i}_v = \underline{i} - \underline{i}_a - \underline{i}_r \tag{A.9}$$

where, $\underline{i}_v$ is the vector of three void currents.

The outputs of compensation by a shunt compensator using this theory are:

1. If the reactive current is supplied by a compensator, the fundamental component of phase voltage and phase currents would become in phase and the compensator would supply the average reactive-energy demand.
2. If the void part of the current is supplied by the shunt compensator, the source currents would become proportional to the phase voltages and the compensator would supply the oscillations in the reactive energy.
3. If the void and the reactive currents are supplied by the compensator, the currents would possess the same wave-shape as the phase voltages and their

fundamental components would be in phase with the phase voltages. This is equivalent to full compensation on the part of CPT theory.

A.2 Simulation Setup

The simulations were done using MATLAB®/Simulink®/SimPowerSystems®. The setup and the control system for the LCC-HVDC terminal and SPVC are the same as given in chapter 6. The only modification is the replacement of the shunt passive filter with three current sources (one in each phase and connected in *Y*) with their current outputs controlled by the outputs of the equations in section A.1.

As stated above, full compensation in CPT is the removal of reactive and void currents from the source. But the void currents depend on how the active and reactive currents are defined. We know that due to non-sinusoidal nature of i_s, the voltage drop across Z_g would make v_{sk} non-sinusoidal. If these voltages are used to calculate active and reactive currents using the equations in section A.1, the void currents are not calculated so as to make i_g sinusoidal, due to which v_{sk} would stay non-sinusoidal. We have observed that the shunt passive filter acts in such a way that the harmonics are stopped from flowing in Z_g and thus i_g and v_{sk} become sinusoidal.

In order for the CPT-based compensator to replicate this effect, a modification to the theory is proposed here. The fundamental positive sequence of v_{sk} is detected and a set of voltages v'_s (consisting of v'_{sa}, v'_{sb}, and v'_{sb}) is synthesized as shown in Fig. A–1. The output of the phase-locked loop (PLL) in Fig. A–1, θ_a, is the saw-tooth waveform ramping from 0 to 2π in a cycle and then resetting to 0. The synthesized voltages would be phase locked to and have the same peaks value as that of the fundamental positive sequence of v_{sk}. The synthesized voltages would then be used in the calculations in section A.1. As a result, the results of calculations in (A.3), (A.7), and (A.8) would all be purely sinusoidal without any harmonic content.

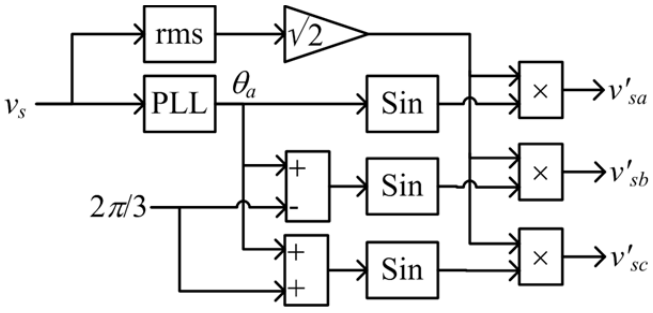

Fig. A–1. Fundamental positive-sequence detection for use with CPT.

Any one of reactive and void currents, or the sum of these two can become the reference for the SAPF in CPT. In this setup, we have used the sum of the two so that the shunt compensator would compensate for reactive-power into the converter transformers as well as current harmonics. This way, the effect of SPVC on the shunt-filter requirements would be highlighted.

Only one case has been simulated. The active- and reactive-power references are the same as in case I in the preceding chapter, i.e. the active-power reference drops form 1 pu to 0.5 pu at 5 s and the reactive-power reference remains at 0 pu throughout. The SPVC would be connected at 3 s. However, the instant of connection of the CPT-based SAPF is added to the plots, which becomes active at 1 s. This is to show its effect on the waveforms of voltages at its point of connection. The focus in presenting the results would be to show the performance of the control of the SAPF based on the calculations of CPT.

A.3 Simulation Results

A.3.1 Active and Reactive Powers

The active and reactive powers at different points in the system are shown in Fig. A–2. Before 1 s, the shunt compensator is not connected and the grid is supplying the entire demand of reactive power. At 1 s, SAPF is connected and immediately takes up the reactive-power demand of the HVDC terminal. Q_g is quickly reduced to zero. When the SPVC is connected at 3 s, it neutralizes Q_s to zero and therefore Q_f also drops to zero. After the transition of active-power reference to 0.5 pu, the SPVC adjusts to keep Q_s at 0 pu after a transient period; and Q_f is seen returning to 0 pu.

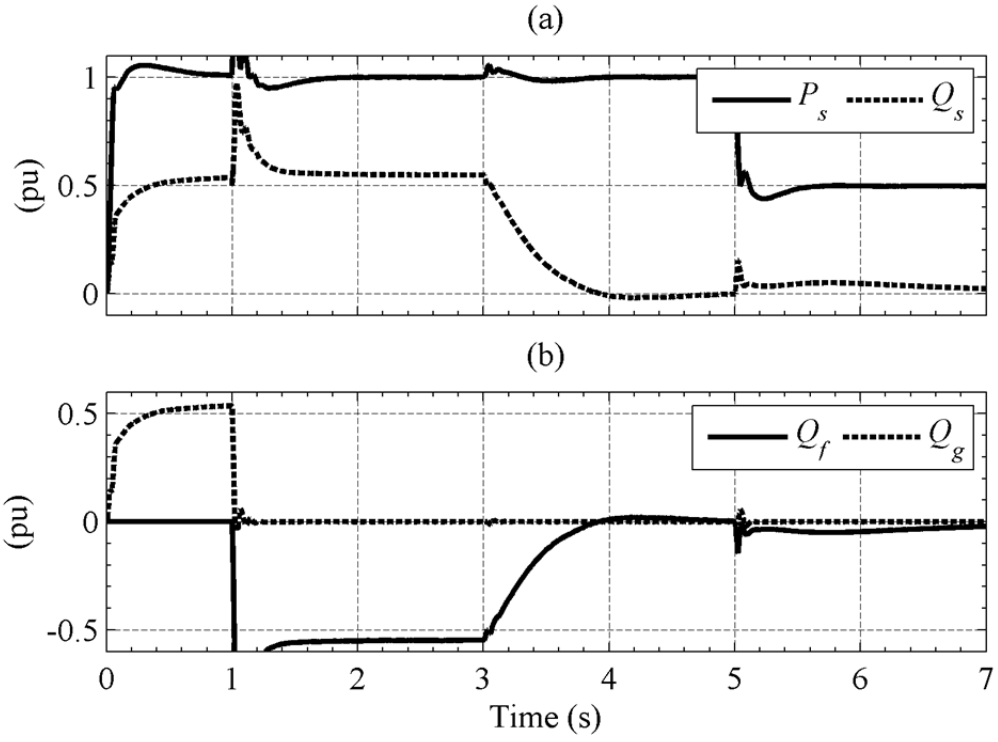

Fig. A–2. Active and reactive powers.

A comparison of Fig. A–2 (b) with Fig. 6–2 (d) shows that the shunt passive filter in the preceding chapter supplies reactive power irrespective of the demand by the

terminal. The only change in the reactive-power output is due to the change in voltage at the point of connection. This necessitates switching whereas the SAPF controls its reactive-power output in such a manner so that the reactive-power demand of the terminal is met at all times. If the SPVC is not working, Q_f balances Q_s. Q_s goes to zero when the SPVC is activated making the SAPF change its output to zero as well.

A.3.2 Instantaneous Waveforms

The instantaneous grid-side currents and voltages of interest for all periods are plotted in Fig. A–3. The period without SAPF and SPVC is shown in panel (a). As there is no current injection by the SAPF, i_{sa} and i_{ga} overlap. The waveform of v_{sa} is also worth noticing as it is non-sinusoidal.

Panel (b) depicts the situation when the SAPF is active, whereas the SPVC is not connected. i_{sa} has the general 12-pulse current waveform and is displaced in phase from v_{sa}. The SAPF supplies the reactive as well as the harmonic content required to bring i_{ga} in phase with v_{sa} and also to make it purely sinusoidal. As a consequence v_{sa} becomes purely sinusoidal.

The situation when the active power is 1 pu and both the SAPF and the SPVC are connected is shown in panel (c). The harmonic-cancellation mechanism of the SPVC makes i_{sa} almost sinusoidal, thereby drastically reducing the requirement on the SAPF to supply smaller harmonic current to make i_{ga} and v_{sa} purely sinusoidal.

Finally, panel (d) presents the situation with 0.5-pu active power where i_{sa} contains relatively higher harmonic content making the SAPF inject more current to make i_{ga} and v_{sa} sinusoidal.

A.3.3 Reference Generation in SAPF

The results of calculations using CPT are plotted in Fig. A–4. This is the situation where the algorithms are calculating the compensation demand ($i_{sareactive} + i_{savoid}$) and the SAPF has not been connected. The important thing in panel (a) is the waveform of v_{sa}. As it is non-sinusoidal, direct use of v_{sa} would result into an active current (which should be supplied by the grid according to CPT) with exactly the same waveform as dictated by (A.7). But v'_{sa} is purely sinusoidal and yields purely sinusoidal $i_{saactive}$ and $i_{sareactive}$ when used in (A.7) and (A.8). Comparison of panels (c) and (e) is interesting as p_g is the actual instantaneous power of the grid and p is that flowing into the two converter transformers calculated using (A.1). They are not identical even though the SAPF is not connected. The reason, again, is the use of v'_{sa} in calculating p and w.

The same plots are repeated in Fig. A–5 for the interval when the SAPF is active and the SPVC is still inactive. As the SAPF starts to inject the reference currents, i_g becomes sinusoidal (Fig. A–3 (b)) which makes *vsa* sinusoidal (Fig. A–5 (a)). There remains no difference between v_{sa} and v'_{sa} in contrast to what was observed in Fig. A–4 (a). The waveform of i_{savoid} has also changed because the improvement of voltage waveform on the point of connection of the SAPF changes i_{sa} waveform (Fig. A–3 (a)

and (b)). So do the waveforms of p and w. The average values, P and W, for using reference currents can be seen to go down as seen in Fig. A–5 (c) and (d) respectively. The oscillations in p_g have also decreased in contrast to the case without SAPF (Fig. A–5 (e)).

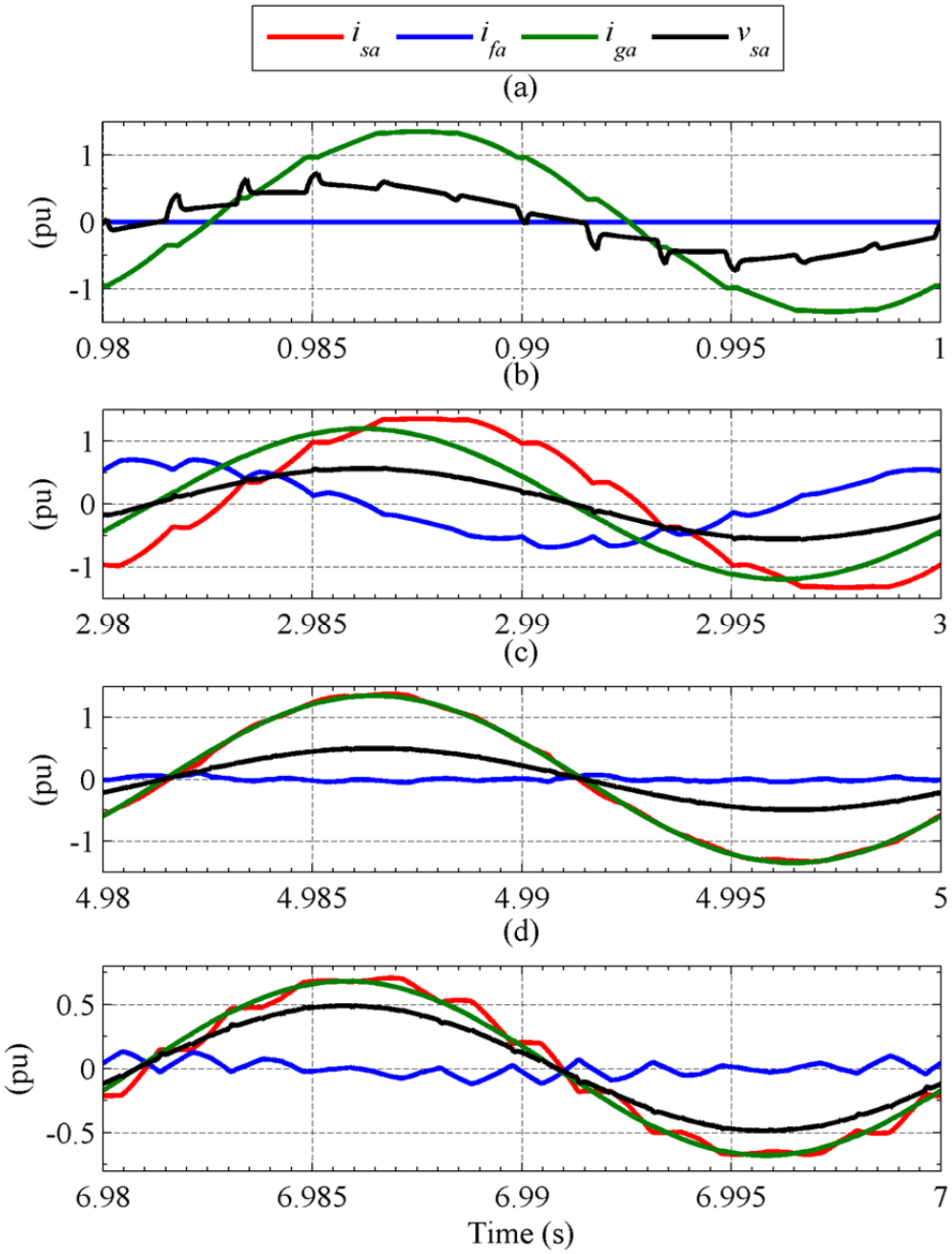

Fig. A–3. Single-cycle plots of grid-side currents and voltages at (a) full power without SAPF and SPVC, (b) full power with SAPF and without SPVC, (c) full power with SAPF and SPVC, and (d) half power with SAPF and SPVC.

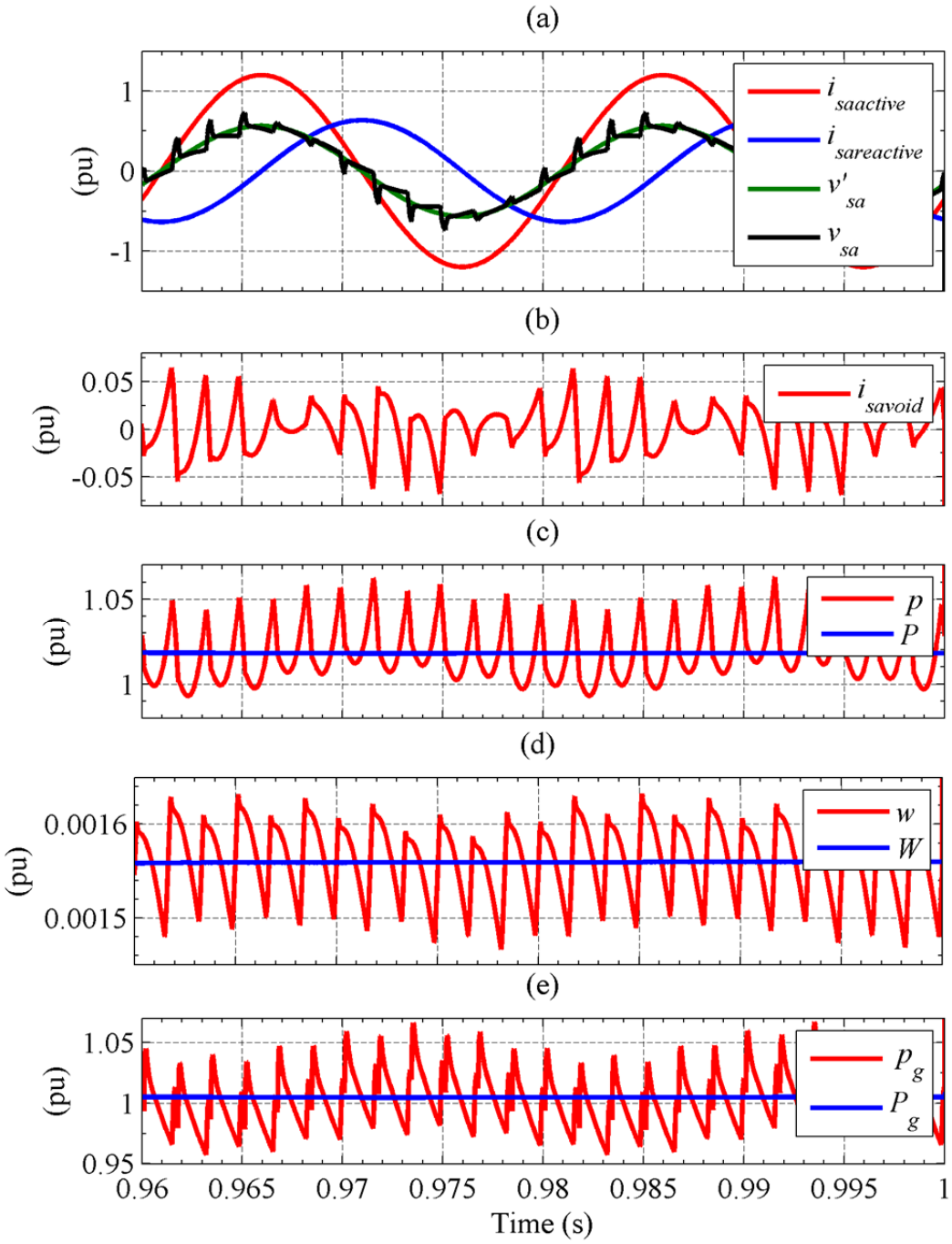

Fig. A–4. Results of CPT calculations with SAPF and SPVC inactive.

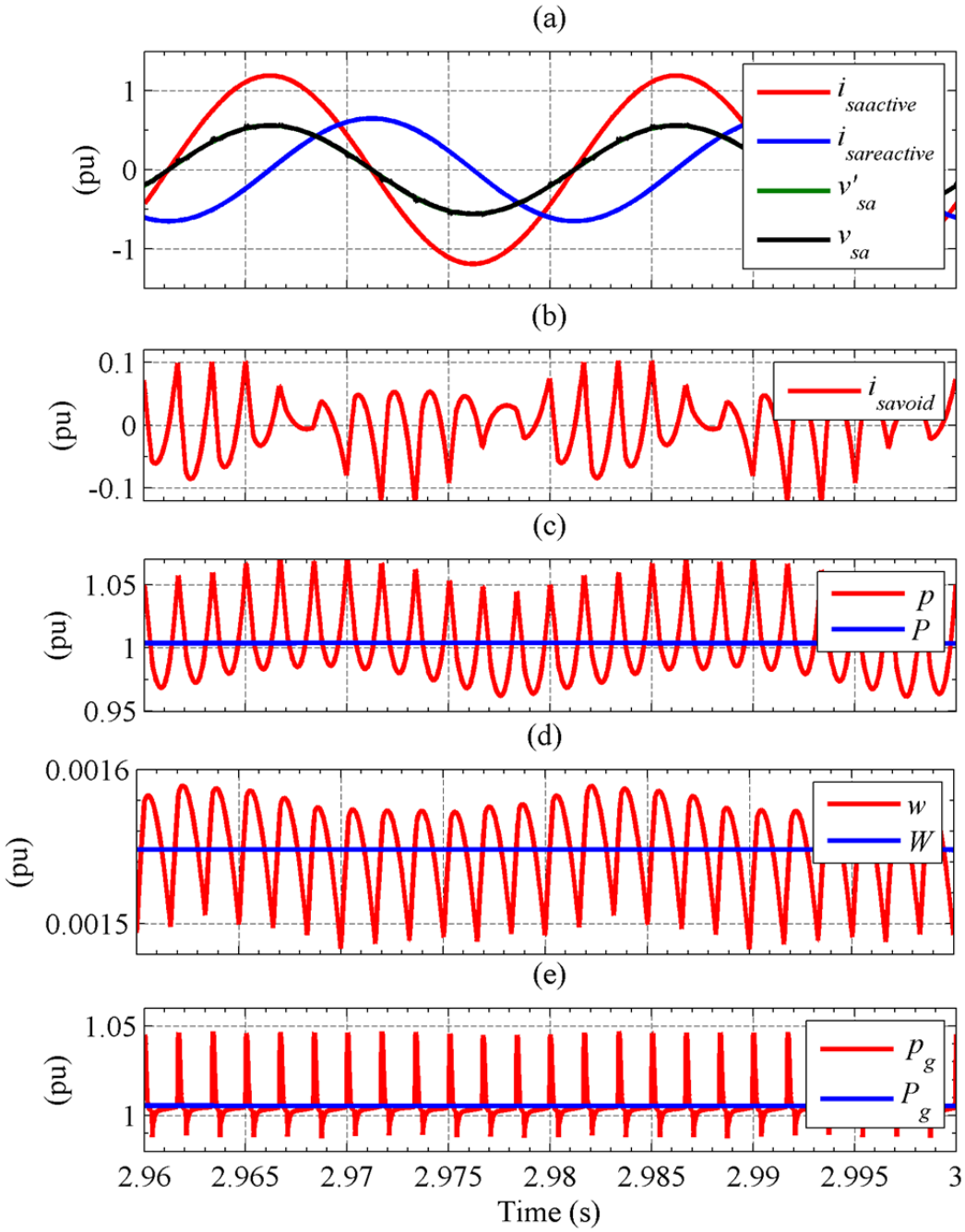

Fig. A–5. Results of CPT calculations with SAPF active and SPVC inactive.

The next period of interest is the one when the active power is 1 pu and the SPVC is also connected along-with the SAPF. This is depicted in Fig. A–6. Due to the reactive compensation done by SPVC, $i_{sareactive}$ goes down to 0 (panel (a)) and the only current that has to be injected by the SAPF is i_{savoid} (panel (b)). The harmonic-compensation capability of the SPVC reduces the peak-to-peak value of i_{savoid} as well. The SPVC also alters the instantaneous waveforms of p and w (panel (c) and (d) respectively) bringing down the oscillation amplitudes in both. The combined action of

SPVC and SAPF also alters p_g (panel (e)) in such a manner that the spikes are on the negative side of the average value in contrast to what was observed in Fig. A–5 (e).

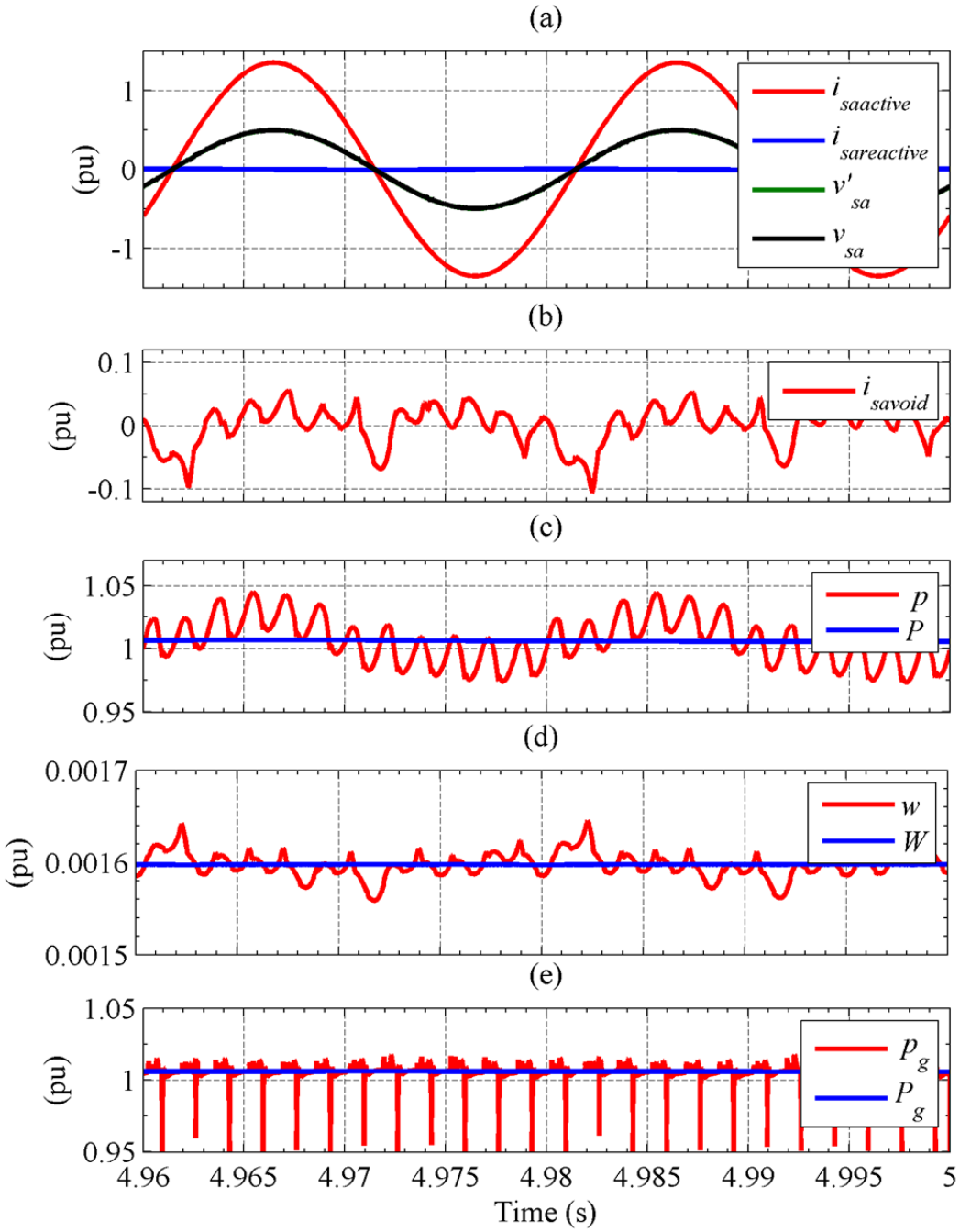

Fig. A–6. Results of CPT calculations with SAPF and SPVC active and P_s = 1 pu.

Finally, instantaneous plots from the last interval with both SPVC and SAPF connected and active power equal to 0.5 pu are shown in Fig. A–7. The reactive power is still being supplied by SPVC, therefore $i_{sareactive}$ is almost zero (panel (a)). The void current has a somewhat different wave-shape (Fig. A–7 (b)) from the case with full active power (Fig. A–6 (b)). The oscillation amplitudes in p and w (Fig. A–7 (c) and

(d)) are also very small. The combined action of SAPF and SPVC transforms p_g (Fig. A–7 (e)) in such a manner that oscillations in p_g are reduced to negligible proportions.

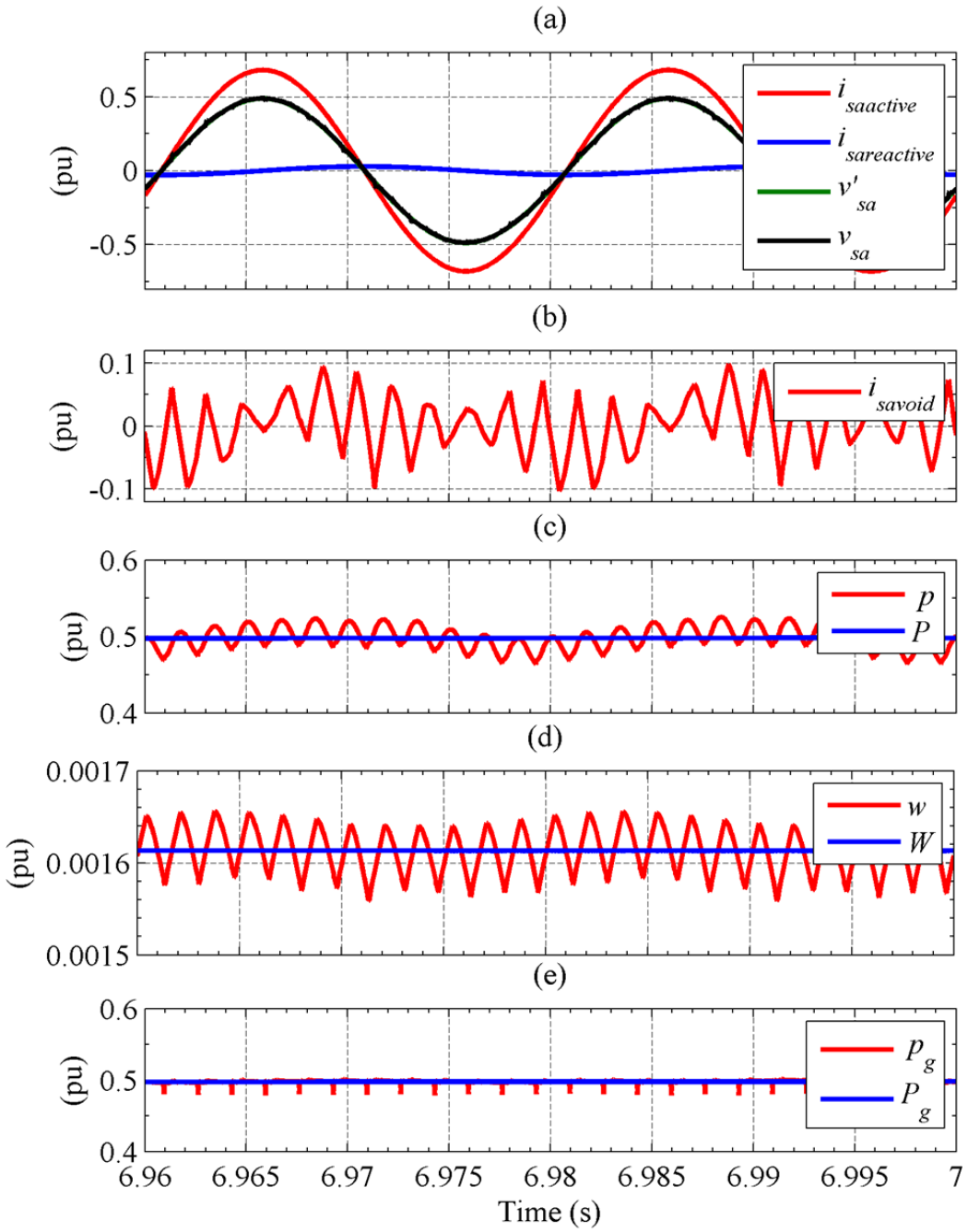

Fig. A–7. Results of CPT calculations with SAPF and SPVC active and P_s = 0.5 pu.

A.3.4 Current Harmonics

In this section, we will briefly discuss the performance of the SAPF and the effect of SPVC on the requirements for SAPF. The harmonics in i_{sa}, i_{fa}, and i_{ga} for the interval when the SAPF is connected and SPVC is not are given in Fig. A–8 (a), (b), and (c)

respectively. The 11th and the 13th are the dominant harmonics in i_{sa} which are being compensated by the SAPF and their flow into the grid is almost negligible at less than 2%.

The second interval is when P_s = 1 pu and both the SAPF and SPVC are connected. The harmonic content is displayed in Fig. A–9. The THD in i_{sa} has gone down from 4.52% to 3.08% (panel (a)). However, the harmonic frequency distribution has changed. The 11th harmonic has gone down to 2% from over 4.5% in the case without the SPVC. The 13th harmonic has been reduced to a negligible level from almost 3%. The SAPF control provides adequate blocking of the remaining harmonics (panel (b)). The fundamental component in SAPF current is almost zero because the fundamental-frequency reactive power is being fully compensated by the SPVC. The distortion in i_{ga} is negligible as observed in panel (c).

The situation when P_s = 0.5 pu is depicted in Fig. A–10. Expectedly, THD in i_{sa} has gone up (panel (a)) and is being compensated by SAPF (panel (b)) to make i_{ga} harmonic free (panel (c)).

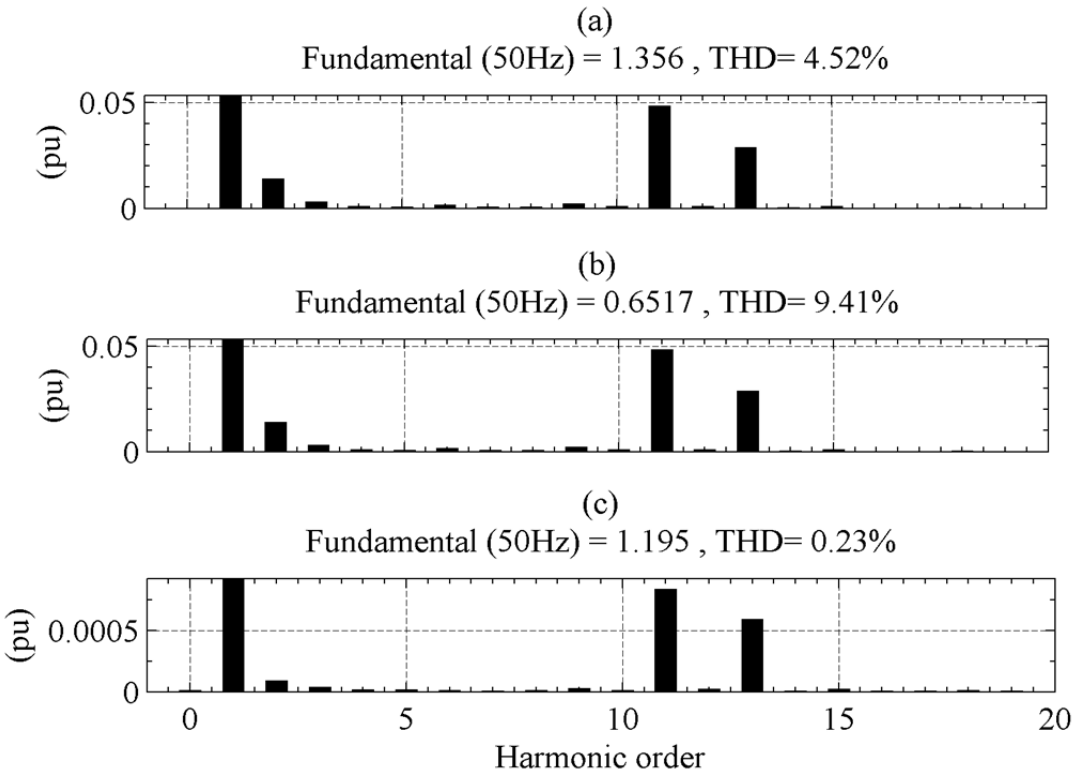

Fig. A–8. Harmonic spectra with SAPF connected and SPVC inactive and P_s = 1 pu. (a) i_{sa}, (b) i_{fa}, and (c) i_{ga}.

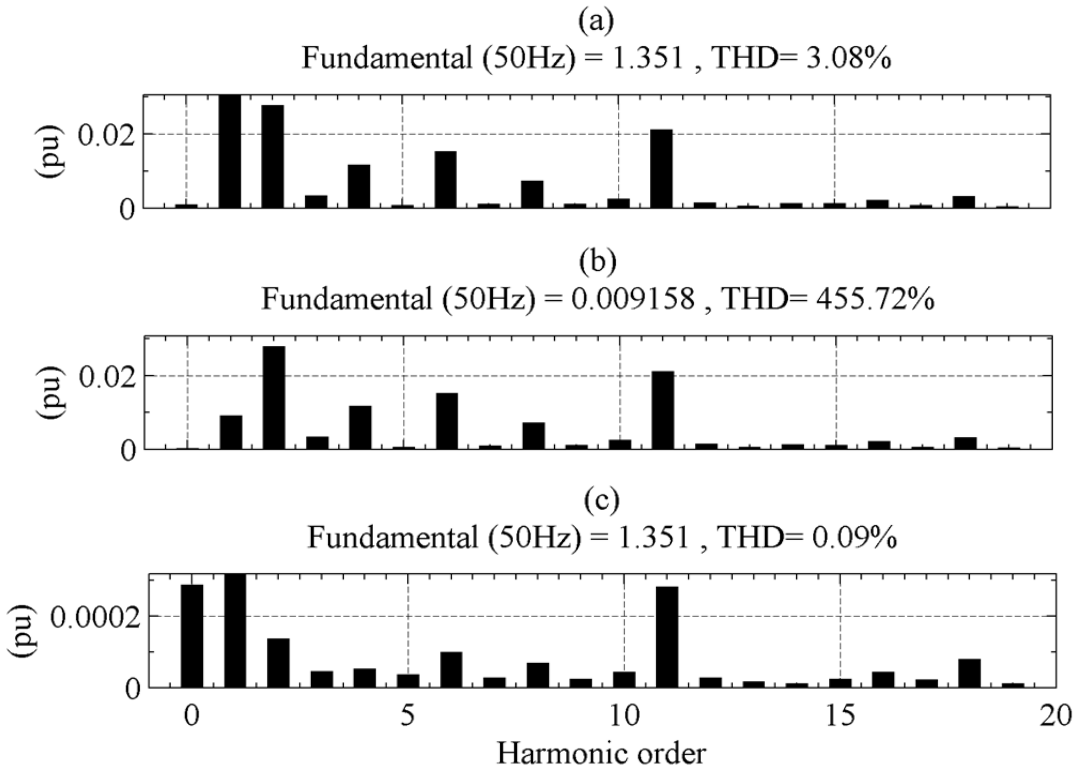

Fig. A–9. Harmonic spectra with SAPF and SPVC connected and P_s = 1 pu. (a) i_{sa}, (b) i_{fa}, and (c) i_{ga}.

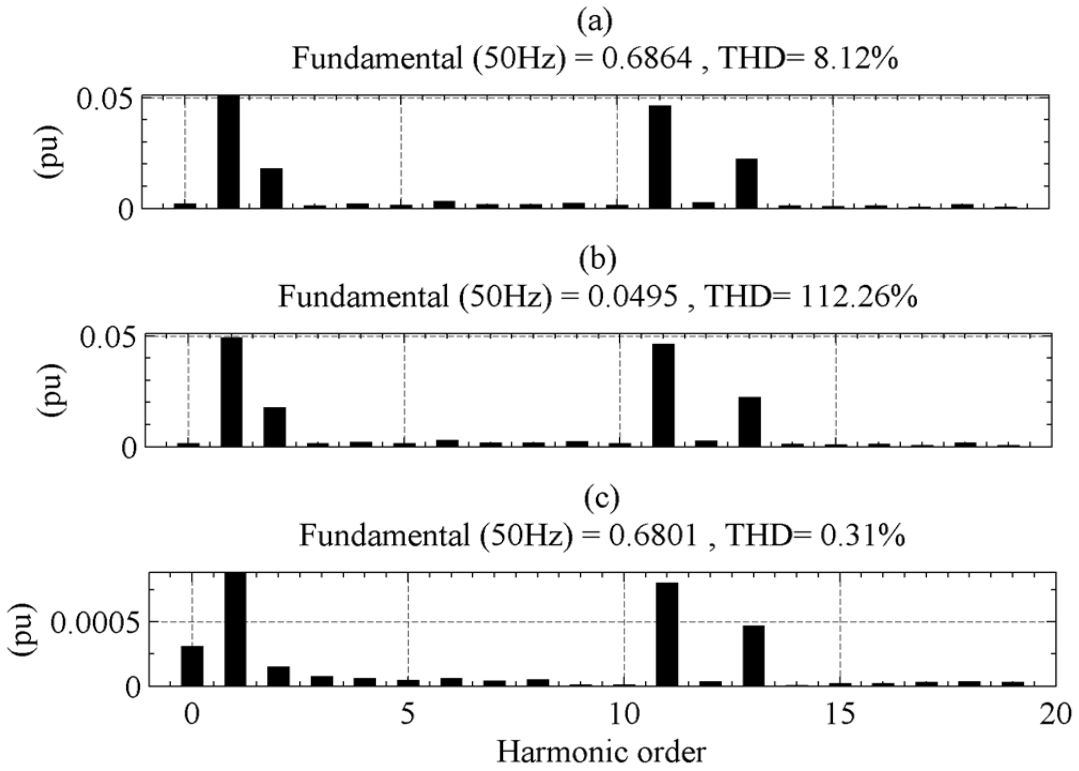

Fig. A–10. Harmonic spectra with SAPF and SPVC connected and Ps = 0.5 pu. (a) isa, (b) ifa, and (c) iga.

A.4 Conclusion

The control and operating principal of the Shunt Active-Power Filter (SAPF) employing the Conservative Power Theory (CPT) has been explained and simulated successfully in conjunction with Series Pulsed-Voltage Compensator (SPVC). It was observed that the SAPF would have to inject reactive and harmonic currents in the absence of SPVC and the rating would have to be large. With the SPVC supplying reactive power, the only job for the SAPF or even a shunt passive filter would be to inject comparatively-smaller harmonic currents. This would bring down the size, cost, and losses in these harmonic filters.

It was noted that the use of synthesized voltages in place of actual voltages at the point of connection of the SAPF made the compensator inject currents which would make the grid current, and consequently, the grid voltage sinusoidal.

The simulations have been carried out using SAPF made up of ideal controlled-current sources following references generated by the control to prove the concept. Simulations employing an actual power-electronic converter for SAPF operation would reveal more about the limitations and benefits of the use of CPT in such a system. The reader is referred to [95] for detailed simulations employing power-electronic converter.

B Tuning of Control Loops in CIGRÉ Benchmark for HVDC Studies

Two proposals for modifying the inverter- and the rectifier-side controls in order to improve the fault ride-through capability of conventional HVDC link are presented in this appendix. Simulation results validating the proposals have also been proposed.

The simulations carried out during this work reveal that a lot can be done in the tuning of control loops to improve the response of the link to various kinds of AC faults in addition to what has already been proposed [114, 115]. Two suggestions for improving the fault ride-through capability have been put forward based upon the observations of various variables in the control loops of the system. The arrangement of the simulation setup in both cases is the same and is depicted in in Fig. B–1. The entire link including the complete converter components on the inverter side have been included. The impedances Z_{g2} and Z_{f2} are the grid and shunt-filter impedances respectively on the inverter AC side. The reader is referred to [116] for details.

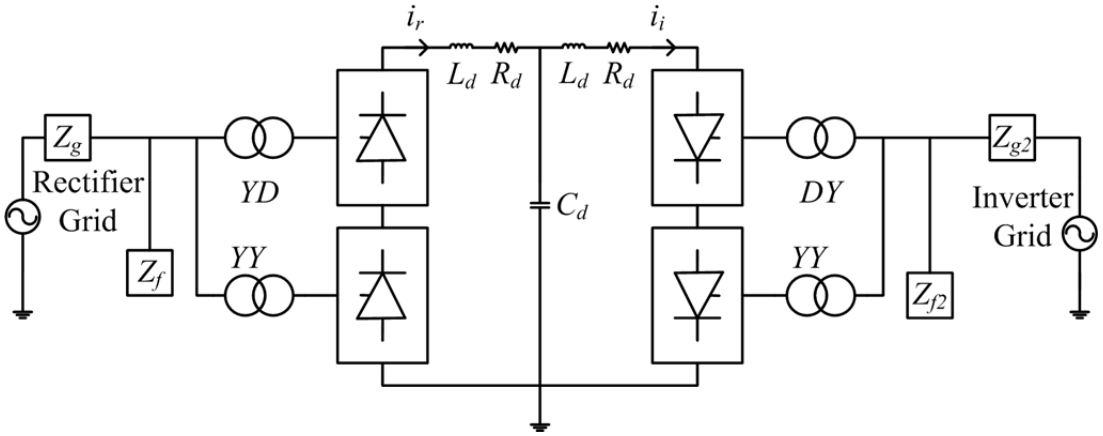

Fig. B–1. Schematic arrangement of simulation setup for control tuning tasks.

In both cases, the fault occurs at the filter bus on the inverter side. The behaviour of the original system and that with the proposed changes is presented turn by turn for both the proposals. The simulation platform for this appendix was PSCAD®.

B.1 First Proposal

The simulations start after the system having settled to steady-state values. A three-phase-to-ground fault occurs at 0.1 s. The duration of the fault is 100 ms (equivalent to 5 power cycles). The fault is cleared at 0.2 s and the system recovers to its steady-state values again.

B.1.1 The Original System without Control Modification

The results of the simulation on the original system are presented in Fig. B–2. The rectifier and inverter currents show a spike after the occurrence of the fault (panel (a) and (b) respectively) but are quickly brought down due to the control loops as observed in panel (c), which shows the current order for the rectifier current. This is reflected in the angle order for the rectifier shown in panel (d).

The current order for rectifier drops down quickly to a minimum level (0.55 pu) and stays there for the duration of the fault. This is because of the mechanism of generating this current order which is depicted in Fig. B–3. The minimum of the current reference generated by the control loops and the Voltage Dependant Current Order Limit (VDCOL) block is chosen as the current order for the rectifier.

The VDCOL block is implemented as a transfer function which depends on the inverter AC voltage. For voltage below 0.4 pu, the output is kept constant at 0.55 pu. The output of VDCOL changes from 0.55 pu to 1 pu linearly as the input changes from 0.4 pu to 0.9 pu. The gain of the block is 1 after the upper input threshold has been reached. This transfer function is graphically presented in Fig. B–4.

As the fault is cleared at 0.2 s, the rectifier current order rises sharply, forcing a quick reduction in the firing-delay angle at the rectifier. As a consequence, the current at the rectifier and the inverter terminals rises steeply. In fact, this steep rise in current forces another commutation failure and current spikes equal in magnitude to the ones at the time of occurrence of fault are observed. This drives down the voltage and hence the VDCOL output also goes down bringing down the current again. The link is restored after the next attempt. These events elongate the recovery period, which is almost 200 ms, twice the duration of the fault itself.

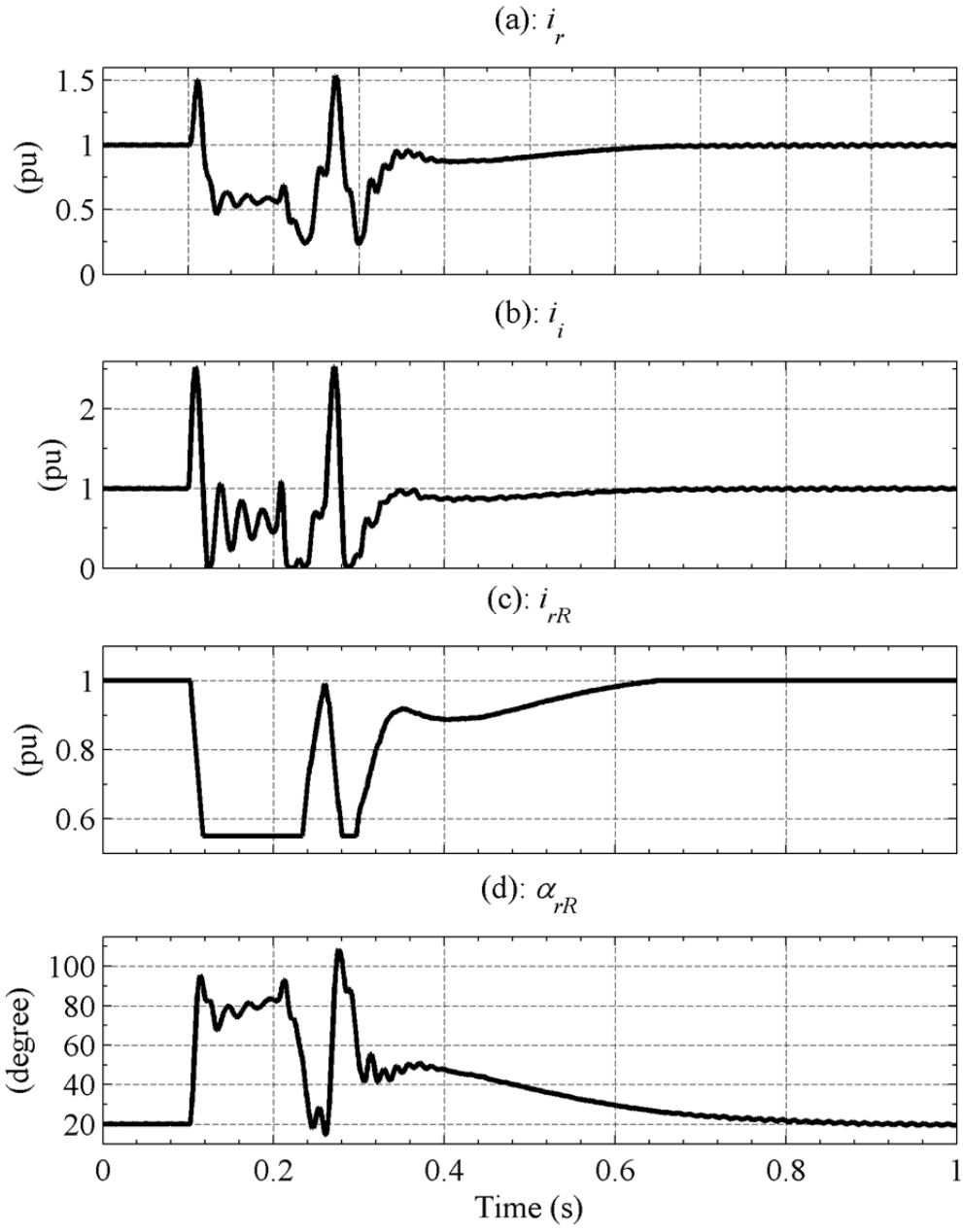

Fig. B–2. Simulation results of the original system.

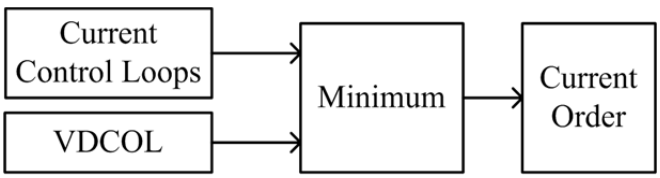

Fig. B–3. Mechanism for generation of current order for rectifier.

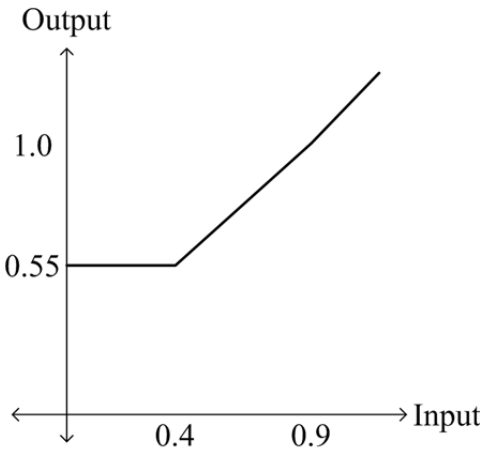

Fig. B–4. Input versus output for the VDCOL block in Fig. B–3.

B.1.2 The System with Suggested Control Modification

Considering the oscillation in rectifier angle order observed in Fig. B–2 (d), a modification to the control loop in Fig. B–3 is proposed. The modified loop is shown in Fig. B–5. A pole has been added which performs low–pass filtering of the signal at its input.

The results of simulation with this modified control are given in Fig. B–6. It can be seen that there is no oscillation in rectifier current order between 0.2 and 0.3 s in contrast to the previous case (panel (c)) and no oscillation in rectifier angle order (panel (d)). As a consequence, there are no commutation failures and, consequently, no current spikes in rectifier and inverter currents (panel (a) and (b) respectively). The link recovers to its normal state at around 0.3 s, which means an improvement of 100 ms from the original system. The recovery time has, thus, been halved.

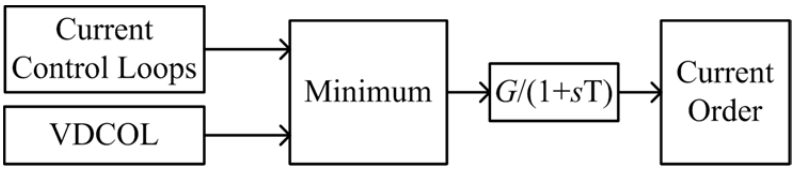

Fig. B–5. Proposed modification in current–order control loop. G = 1 and T = 0.05 s.

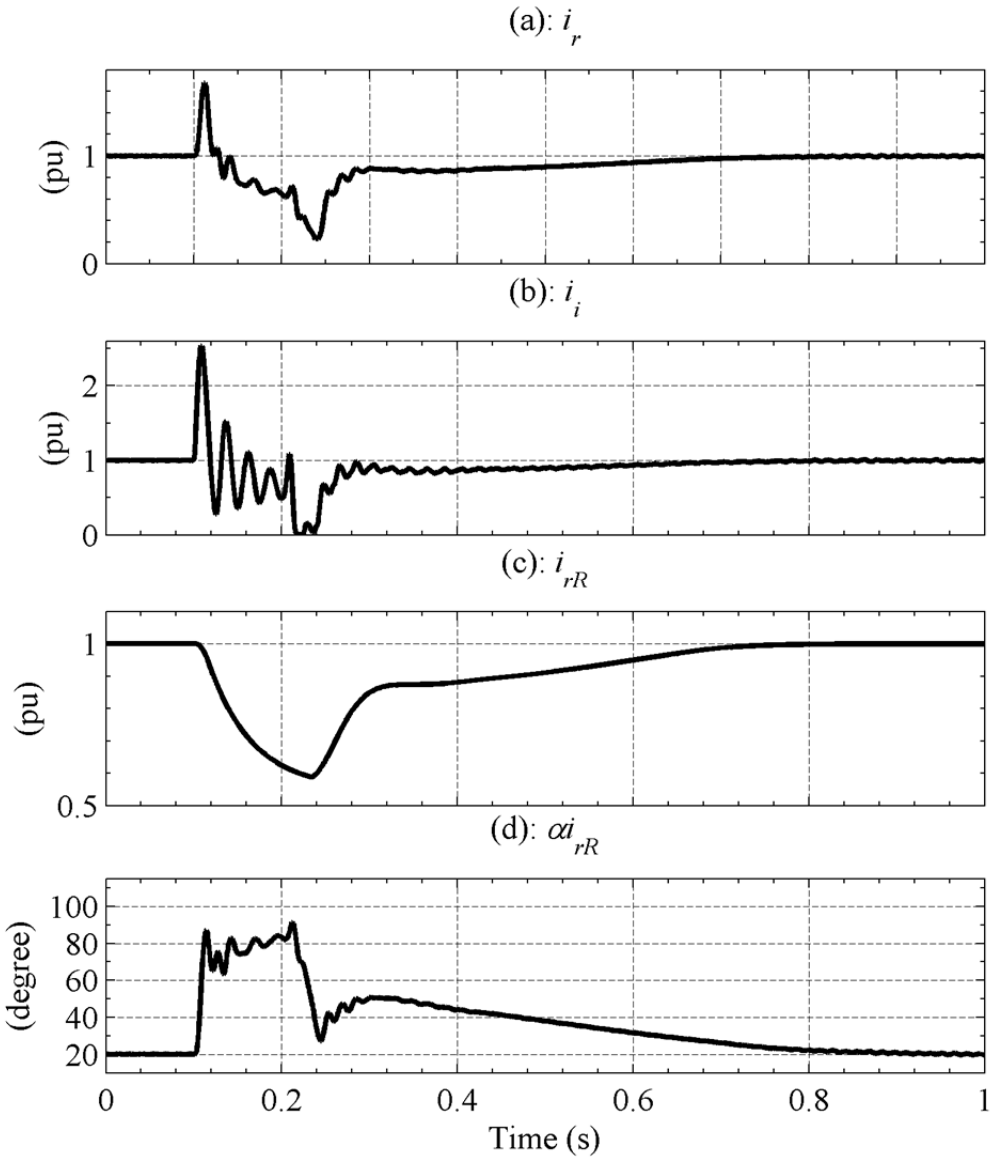

Fig. B–6. Simulation results for modified system.

B.1.3 The system with further Control Modification

Close observation of Fig. B–6 reveals that the rectifier current peak at the time of fault is higher than the original system (almost 1.75 pu against 1.5 pu). The reason is that the action of the low-pass filter in the proposed loop (Fig. B–) slows down the decline in current order (Fig. B–6 (c)), which it should not. As a result the angle order for rectifier does not rise steeply to reduce the current on the rectifier side (Fig. B–6 (d)).

The discussion above leads us to deduce that the current order for the rectifier should decline as quickly as in the original system, whereas its rise should be as per the proposed system. This leads us to a new design of the control loop. The re-designed loop is drawn in Fig. B–7. The location of the pole has been changed from the output of the minimum block to its input. Secondly, the input to the low-pass filter has been taken

from the output of VDCOL calculations. The minimum of these three inputs is now selected as the current order to the rectifier terminal.

Simulation results with this modified control loop are given in Fig. B–8. The initial current spike in the rectifier DC current at the time of occurrence of fault has now come down to 1.5 pu (Fig. B–8 (a)) like in Fig. B–2 (a), whereas, the recovery from the fault between 0.2 s and 0.3 s is as seen with the modification proposed in section B.1.2 (Fig. B–6 (a)). The recovery of the inverter side from fault (Fig. B–8 (b)) is similar to that in Fig. B–6 (b).

This can be explained by observing the current and angle orders to the rectifier depicted in Fig. B–8 (c) and (d) respectively. At the time of occurrence of fault, the current order falls with the same slope as depicted in Fig. B–2 (c), so the rise in angle order is as steep as the one in Fig. B–2 (d). However, the rise in angle order after the recovery from fault is like the one plotted in Fig. B–6 (c). Consequently, the drop in angle order resembles that in Fig. B–6 (d). This control modification has, thus, allowed a fast reduction in rectifier current at the occurrence of the fault and fast and commutation-failure-free recovery after fault clearance.

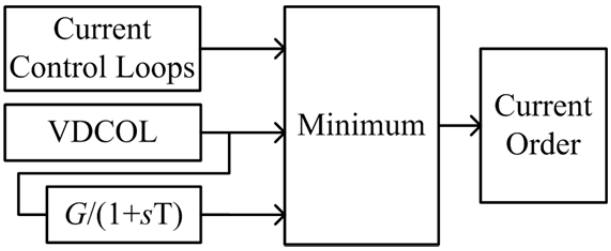

Fig. B–7. Further modification in current-order control loop. G = 1 and T = 0.05 s.

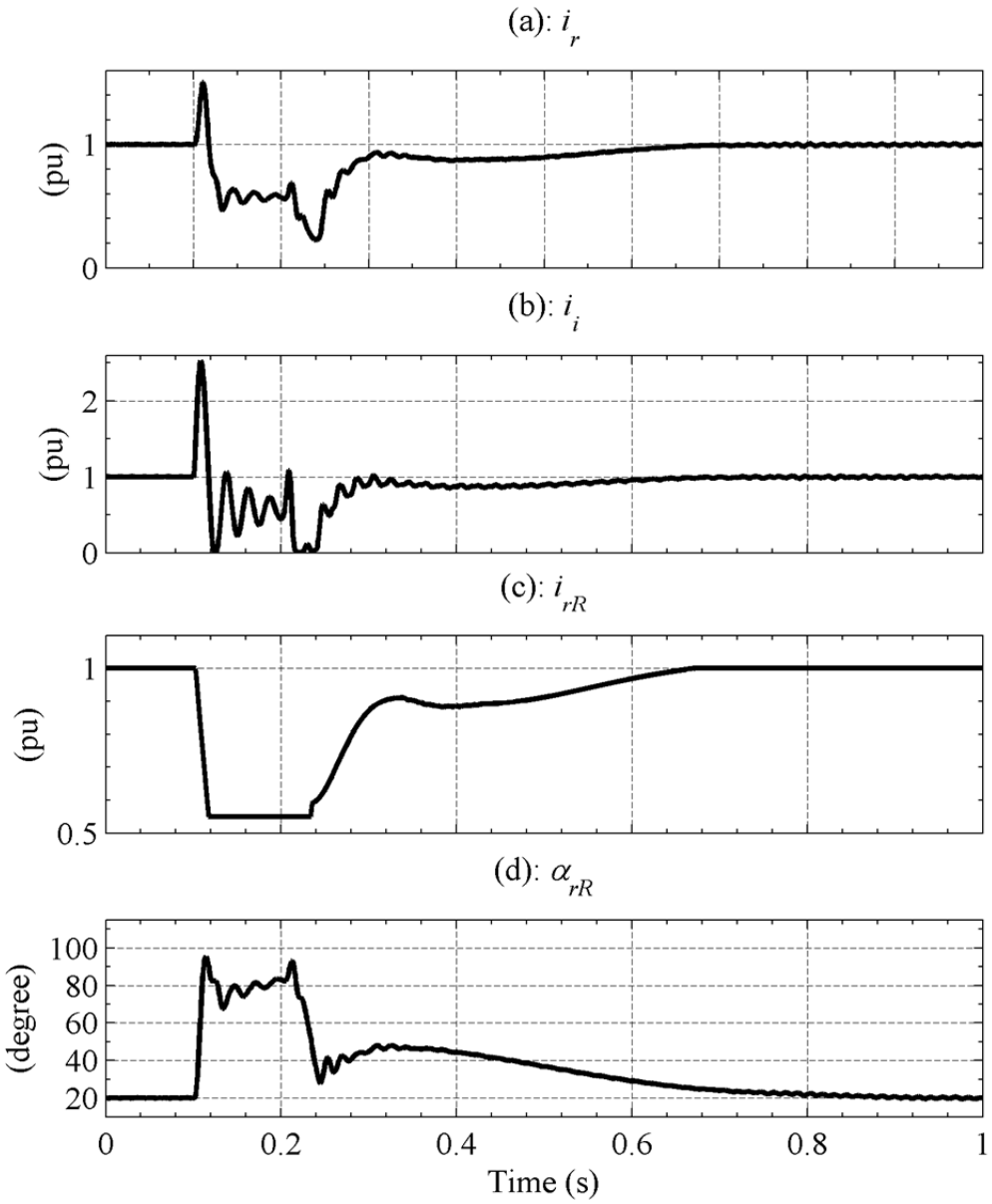

Fig. B–8. Simulation results for system with further modification.

B.2 Second Proposal

B.2.1 Analysis of Inverter Controls for Original System

Close inspection of Fig. B–2 (b), Fig. B–6 (b), and Fig. B–8 (b) show that the inverter current hits zero before starting to recover. In the case of Fig. B–2 (b), the first attempt for recovery fails resulting into a current spike as large as the fault-current spike. This is avoided with the proposed modification in sections B.1.2 and B.1.3. However, the recovery time could be improved further if the inverter would not encounter commutation failures just after the clearance of the fault. Based on the observation of current order in Fig. B–2 (c), it can be deduced that VDCOL and current order for the

rectifier are not responsible for these failures. The reason is that the current order is still at the lower threshold of 0.55 pu when the inverter current drops to 0 pu and starts to rise afterwards. Therefore, further investigation should be done in the inverter controls to eliminate this problem and speed-up the recovery process even further.

To investigate the problem, the α-orders to the rectifier and inverter terminal along with the actual values are plotted in Fig. B–9 (a) and (b) respectively. It is obvious that, during the fault and recovery stages, the rectifier α values track the reference accurately, whereas, those at the inverter side do not. The inverter α values increase very quickly and attain higher values than commanded by the control. This causes a quick rise in v_i as shown in Fig. B–10 (a). This causes an abrupt increase in the rectifier current order and α_{rR} resulting into a steep rise in v_r as seen in Fig. B–10 (b). This causes i_i to rise sharply.

The control design for α_{iR} is shown in Fig. B–11. As α_{iR} is formulated using the measurement of extinction angle (γ), the consequence of firing-delay angle not following the command would simply be commutation failure. As i_i starts to increase during recovery, γ_i increases due to larger overlap as shown in Fig. B–12. This is why α_{iR} stays at a low value, but the actual firing delay angles increase beyond the required level and therefore, there is no time left for extinction, hence the commutation failures.

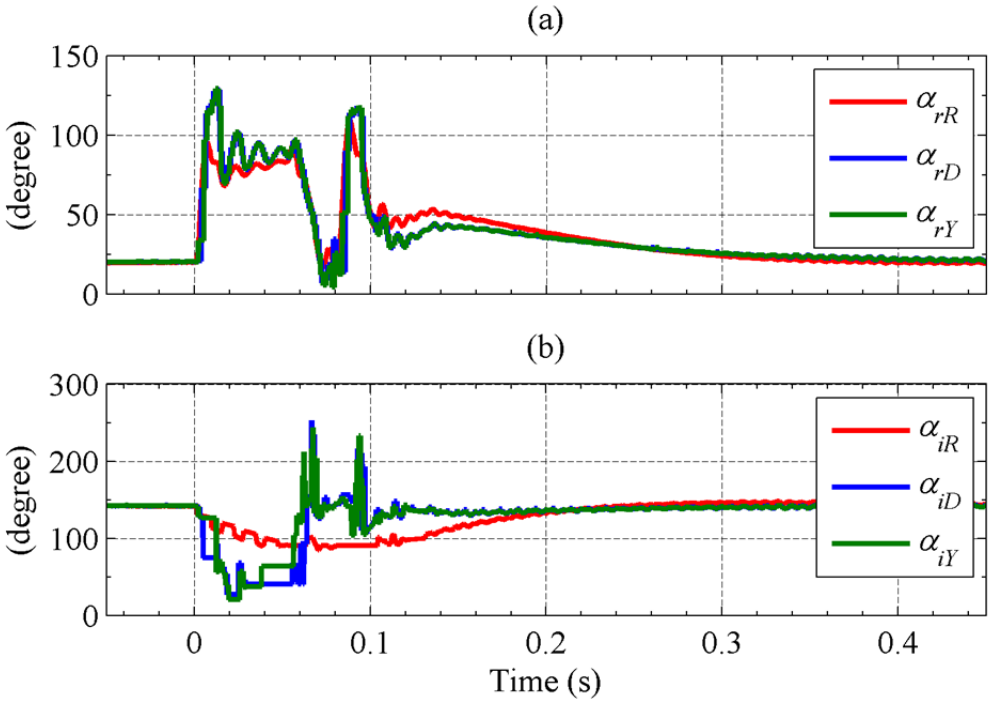

Fig. B–9. Reference and actual α values at the (a) rectifier, and (b) inverter.

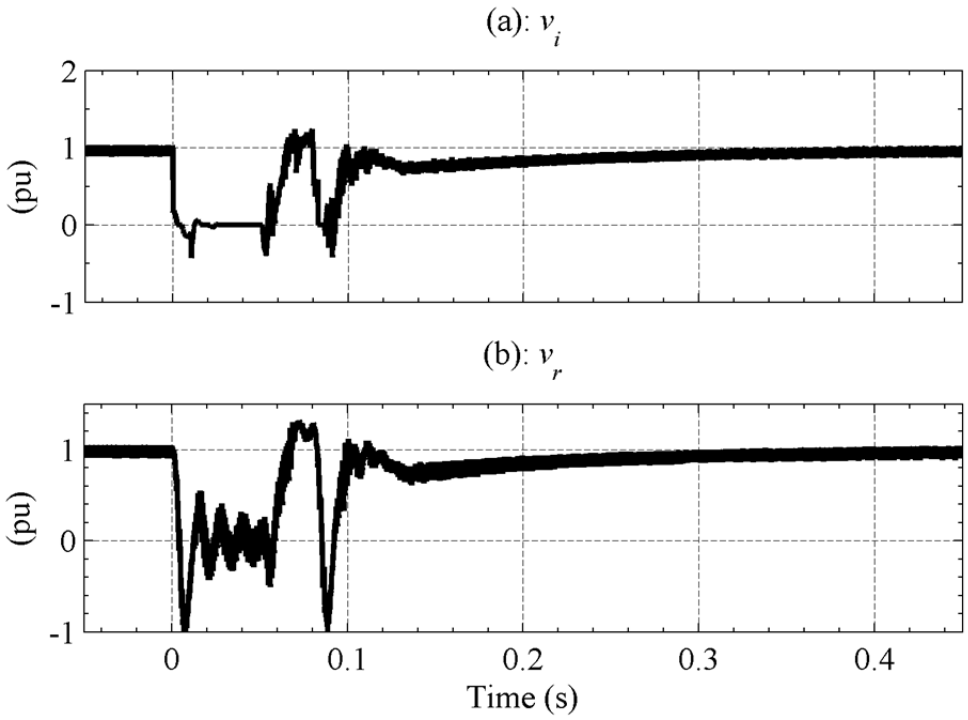

Fig. B–10. DC-link voltages at the (a) inverter, and (b) rectifier.

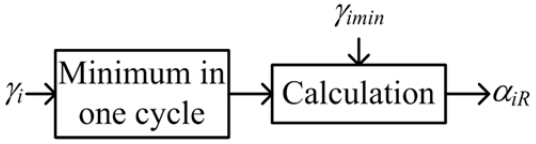

Fig. B–11. Control loop for generation of α_{iR}. γ_{imin} is the minimum extinction angle.

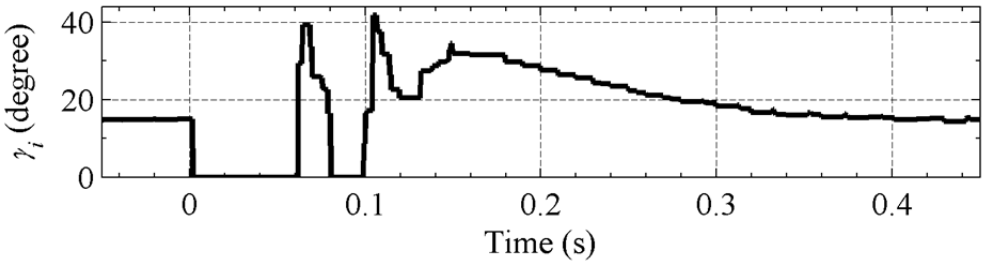

Fig. B–12. Instantaneous plot for inverter extinction angle.

The need is, therefore, to reduce the error in α_{ij} and α_{iR}. The phase-locked oscillators (PLO) in the converter bridges in the simulation model has a proportional gain (K_P) equal to 10 and an integral gain (K_I) equal to 50. Based on these values, the closed-loop transfer function (T(s)) is given by:

$$T(s) = \frac{0.9091(s+5)}{(s+4.545)} \tag{B.1}$$

The unit step response y(t) for this T(s) would be:

$$y(t) = 1 - 0.0909e^{-t/0.22} \tag{B.2}$$

The initial error is thus 9.09% with a time-constant equal to 0.22. The error would thus decay in 1.1 s which is quite slow considering the situation under discussion.

In principle, this response should affect the response of the angle orders against the reference on the rectifier side as well. But, as observed in Fig. B–9 (a), it does not. The reason for this not happening on the rectifier side is the difference in the nature of inputs to the angle-order loops for the inverter and the rectifier. The control loop for generation of α_{rR} is depicted in Fig. B–13.

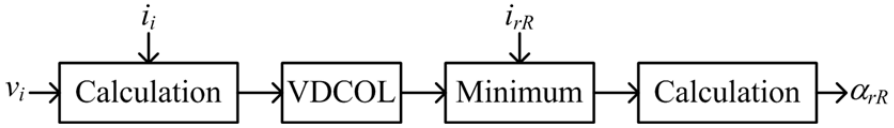

Fig. B–13. Control loop for generation of α_{rR}.

The inputs i_i, v_i, and i_{rR} pass through low-pass filters and do not have any steps. This is why α_{rR} does not have any high-frequency component and thus can be tracked accurately. However, γ_i and γ_{imin} do not pass through any filter and calculations yield an output with high-frequency components, which cannot be tracked by the control.

B.2.2 Proposal for Improvement

The closed-loop transfer function in (B.1) is the result of calculation based on the values of K_P and K_I in the PLO. The mathematical form in term of variable K_P and K_I is given by:

$$T(s) = \frac{1}{K_P + 1}\left(\frac{sK_P + K_I}{s + \dfrac{K_I}{K_P + 1}}\right) \tag{B.3}$$

The unit-step response of this transfer function is:

$$y(t) = 1 - \frac{1}{K_P + 1} e^{-t/\left(\frac{K_P + 1}{K_I}\right)} \tag{B.4}$$

One way to improve the response is to decrease the time-constant in (B.4) by increasing K_I. However, the initial error is independent of K_I. We, therefore, propose to

increase the value of K_P from 10 in the original system to 100 and keep the same value of K_I (i.e. 50). This would adversely affect the time-constant, which would rise to 2.2 s from 0.22 s. However, the initial error would now be 0.99% and the issue of larger time-constant would not affect the performance adversely. This change would be done on the PLOs on the inverter side only as the rectifier side was observed to be performing properly.

The instantaneous currents and voltages on the rectifier and inverter sides with the proposed modification in the control are presented in Fig. B–14. It is obvious that the proposed modification has eliminated the post-fault commutation failures. The current i_r and i_i build up to the required level steadily after the clearance of fault at 0.2 s (panel (a) and (b) respectively). Also, the voltages v_r and v_i build up without any further short-circuit in the same interval. The impact of changing K_P on α_{iD} and α_{iD} is plotted in Fig. B–15. The error between the ordered value and the actual values is smaller in this case.

Finally, the impact of this modification on the inverter extinction angle is shown in Fig. B–16. As the fault is cleared, the extinction angle shoots up due to build-up of i_i. The α values, by following the reference more closely, are able to provide suitable commutation margins to avoid post-fault commutation failures and the recovery process is smoother and faster.

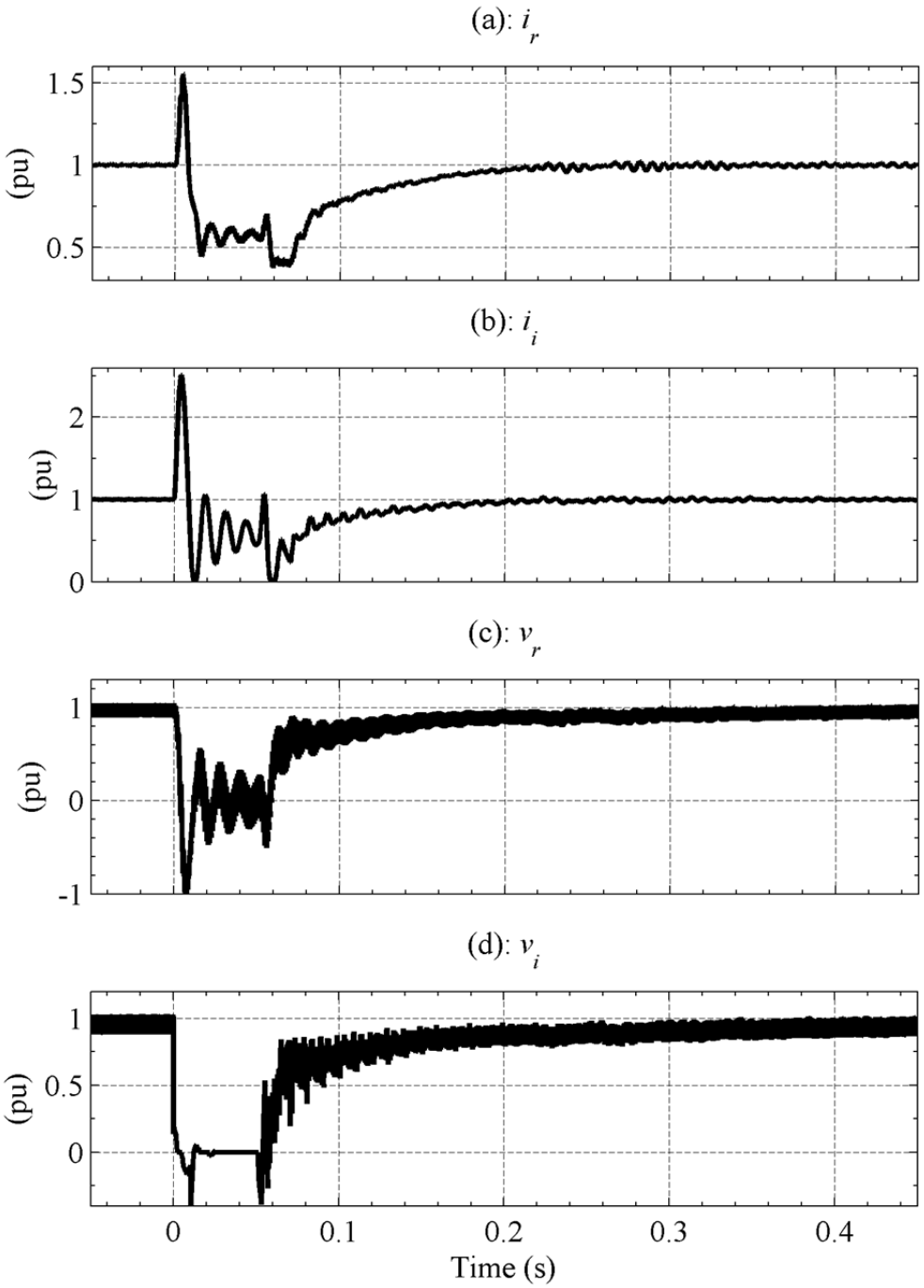

Fig. B–14. Instantaneous currents and voltages at the rectifier and inverter terminals with the proposed modification.

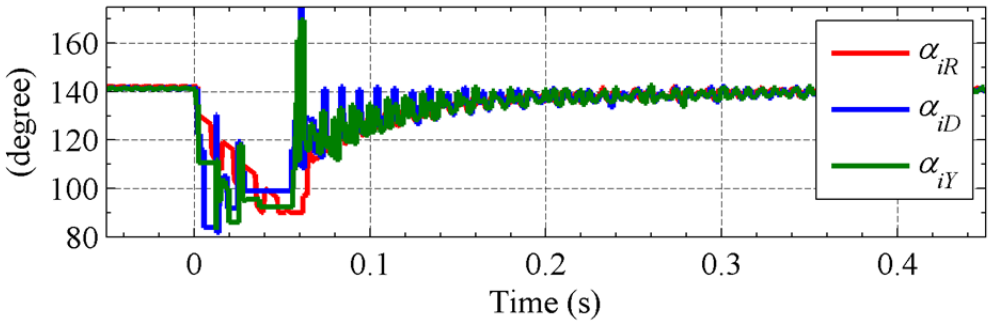

Fig. B–15. The reference and actual firing-delay angles with the proposed modification.

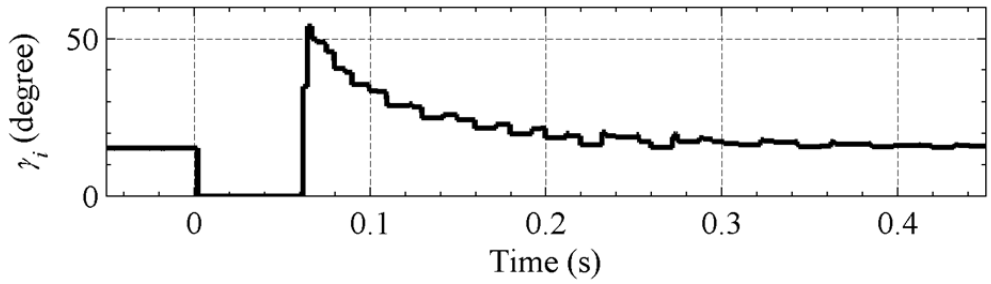

Fig. B–16. Instantaneous plot for inverter extinction angle after the proposed modification.

B.3 Conclusion

Two proposals for modification of controls in the CIGRÉ benchmark model for HVDC studies (as implemented in PSCAD® as an example) have been proposed in this chapter.

The first proposal involved altering the reference-current-generation mechanism on the rectifier side. The two-step development of the control made sure that the behaviour of the system was adequate and fast enough to bring down the rectifier current quickly, and that the post-fault ramping rate for rectifier current was gradual enough to avoid post-fault commutation failures at the inverter side.

The second proposal focussed on control modifications on the inverter side as it was the location of the post-fault commutation failures. Any modification on local controls would be more suitable and practical than to send information to the other end of the link. The changes made in the first proposal were discarded and the gains in one of the phase-locked oscillators on the inverter side were changed to minimize the initial error in response to a step change in the input. It was observed that the changes made had the desired impact on the recovery of the link after fault clearance. The link recovered to steady-state smoothly and quickly without any post-fault commutation failures.

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