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Control, Dynamics and Operation of Multi-terminal VSC-HVDC Transmission Systems

Thesis for the degree of Philosophiae Doctor

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Abstract

In recent years, there has been an increased development and deployment of renewable energy resources to meet the ever increasing electric power demand and to limit the use of fossil fuels. This has spurred offshore wind farm development, particularly in the North Sea, due to the vast offshore wind energy potential. Large scale wind farms in the North Sea pose grid integration challenges such as the need for long distance sub sea power transmission and managing the variability of wind power variation on in the power grid. These challenges can be properly met by the use of multi-terminal voltage source converter high voltage dc transmission (MTDC) grid. Even though the North Sea region is envisioned as the immediate target of application, MTDC can also be used as the highway of power in onshore systems, thereby connecting loads and generation sites involving very long distances.

MTDC system consists of three or more HVDC converter stations connected to a common dc transmission network. Currently there are two types of converters used in HVDC, namely: line commutated converter (LCC) type and voltage source converter (VSC) type. VSC-HVDC is superior to LCC-HVDC for MTDC applications due to its flexibility and relative simplicity in power control, its bi-directional power transmission capability while keeping the dc voltage polarity unchanged and due to its reactive power support capabilities. Hence most recent research works in the area of MTDC have focused on VSC based systems only. Several R&D works have been done in the area of MTDC transmission, especially in its control aspects, in the past. In most cases however, only qualitative approaches have been used to describe the operational characteristics of the various proposed control strategies. In particular, studies exploring the quantitative analysis of the steady-state and dynamic operational characteristics of MTDC grids have been missing in the literature.

The research work described in this thesis was started with the objective of filling some of these gaps, i.e. (1) to investigate the various control strategies of VSC for use in dc grids using both qualitative and quantitative approaches, (2) to propose improvements in the control and operation of MTDC systems and (3) to increase understanding of the dynamic behavior of MTDC systems.

The main contributions of the research work can be put into three areas, namely MTDC control, MTDC operation and MTDC analysis.

In the area of MTDC control grid frequency support strategy by MTDC has been proposed and analyzed. The control strategy enables exchange of primary reserves between asynchronous ac grids connected by MTDC without involving the use of communication systems between converter stations.

In the area of MTDC operation a method for precise control of steady-state power flow in MTDC has been proposed and tested with simulation models. The method enables power injection control in MTDC based on the power dispatch and is appli-

cable to any MTDC transmission topology.
The contributions in the area of MTDC analysis comprise of three parts, namely: (1) steady-state MTDC interaction, (2) state-space modeling of a generalized MTDC topology and (3) large-disturbance stability analysis of MTDC. Methods have been proposed for each of the aforementioned MTDC analysis aspects and tested with various simulation models. In the integrated ac/dc system events, such as load insertion/rejection in the ac grid will have impacts on grid frequencies as well as dc-bus voltages in the MTDC. The steady-state interaction analysis is used to estimate the steady-state changes (of frequencies, dc-bus voltages, transfered nodal powers) that come as a result of such events. The state-space modeling approach has been used to study the dynamic aspect of MTDC. The large-disturbance stability analysis has been principally proposed to study the impact of ac short circuit fault close to a converter terminal in rectifier mode of operation. Ac faults occurring close to inverters connected to MTDC transmission result in excess power in the MTDC during the fault duration. This however can be tackled by using fast acting dc voltage controllers and hence excess power in the dc grid may not as sever problem as shortage of power.
In addition, secondary control of MTDC based upon steady-state sensitivity analysis has been proposed in the thesis. The method enables accurate compensation of power flow deviations in MTDC occurring due to the action of primary control.
Various representative case models have been used to show the merits claimed for each of the proposed control methods, and to verify the validities of the proposed operational strategies and MTDC analysis approaches. Finally a hypothetical dc grid scenario has been used to demonstrate the various potential benefits of employing MTDC in the North Sea region.

Preface

This thesis summarizes the research work I have been doing as PhD student at Norwegian University of Science and Technology (NTNU), Electric Power Engineering Department. My stay as PhD student which lasted for four years (between 2008 and 2012) has been a fruitful one. I have not only been able to benefit from the academically conducive environment but also enjoyed the very friendly social life I have been sharing with my colleagues. I would like to give the credit to several people who were involved in giving me the opportunity to start my PhD study, who helped me to get through it and who guided me to complete it successfully.

First of all I would like to acknowledge the Norwegian Research Council (NRC) and Electric Power Engineering Department, NTNU for financially supporting my PhD study program and the research work. Next, I would like to express my deepest gratitude to my supervisor Prof. Kjetil Uhlen and my co-supervisor Prof. Tore Undeland for giving me the opportunity to explore an interesting topic and for trusting me that I would be able to successfully complete the PhD study program. I would like to thank them for their advice and guidance which I was able to get whenever I needed it despite their often tight time schedule. I appreciate the regular follow up of my research work by my supervisor Prof. Kjetil Uhlen which, together with his guidance, enabled the publications of my research results in timely manner.

I like to thank all my fellow PhD students with whom I had the opportunity to discuss academic matters and spend memorable times together during various social events. I could not list all the names of my colleagues and friends who made my PhD study time easier and more enjoyable. I just say thank you for all the cabin trips, skiing trips and other social events we had together. I would like to thank Eva Schmidt, for kindly helping and consulting in administrative matters.

Nomenclatures and Abbreviations

Abbreviations

ACE	Area control error
ENTSO-E	European Network of Transmission System Operators for Electricity
LCC	Line commutated converter
MTDC	Multi-terminal HVDC/ multi-terminal VSC-HVDC
PCC	Point of common coupling
PI	Proportional-integral control
PLL	Phase-locked loop
RG	Regional group
TSO	Transmission system operator
VSC	Voltage source converter

Symbols

All symbols representing scalar physical quantities are written in italics. Vector variables and parameters are given the same symbols as their scalar counters. To make a clear distinction, vectors and matrices are written in bold face letters and without italics. For reference parameters the same symbols are used as their physical variable courters with asterisk superscripts added to them.

V_x	Ac voltage at PCC
V_c	Internal ac voltage of VSC
U	Dc voltage at dc-bus of VSC (converter)
P_c	Converter power injection (into dc-bus) measured from dc side of the VSC
P'_c	Converter power injection (into dc-bus) measured from ac side of the VSC (i.e. at PCC)
P_{Loss}	Converter power losses including ac and dc filter losses
P_x	Converter power injection into dc-bus plus the dc filter capacitance
P_y	Converter power injection next to total dc-bus capacitance
P_g	Power injected by aggregated generator into ac grid network
P_z	Total power by supplied by ac grid to all VSC units which interconnect the ac grid to MTDC network
P_{cN}	Rated power capacity of converter
P_{gN}	Rated generation capacity of ac grid
ρ_g	Frequency droop constant of ac grid
ρ_{DC}	Dc voltage droop constant of VSC terminal
ρ_f	Frequency droop constant of VSC terminal
R_g	Frequency response constant of ac grid
R_{DC}	Dc voltage response constant of VSC terminal
R_f	Frequency response constant of VSC terminal
R_o	Equivalent output impedance of VSC terminal (as observed from dc-bus side)
C_b	Dc filter capacitance of VSC
C_L	Dc line equivalent capacitance as seen from dc-bus of a VSC terminal
L	Ac series filter inductance of VSC

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1 INTRODUCTION

1.1 Background

In recent years the use of wind energy has been increasing in many parts of the world and particularly in Europe. Two distinct reasons are attributed to this. On the one hand, most of the sites with hydro power potential have already been used up, pushing up the demand for other alternative renewable energy sources. On the other hand, the use of fossil fuel and nuclear energy is facing increasing resistance from the society at large due to concerns of environmental impacts. Onshore development of wind farms is however facing similar situation, i.e. suitable sites for onshore wind farms are being used up and there are also some objections against wind farms located close to inhabited areas for reasons such as visual pollution, noise disturbances and impacts on migratory birds. As a result, offshore sites are becoming more attractive for developing wind farms [1]. Apart from being an environmentally friendly energy source, offshore wind farms improve energy security by reducing dependency on imported fossil fuels [3]. Offshore wind farms are naturally located at large distances from load centers hence posing a challenge of grid integration. ac cable connections are usually feasible if the transmission distance is not more than $50 - 60$ km [24]. With increasing transmission distance, the reactive power flow will be higher due to line capacitances. This results in large line losses and hence ac transmission will not be a viable option [72](chapter 10). Due to its suitability for such applications, VSC-HVDC technology is more and more often used for grid integration of offshore wind farms.
Traditionally, HVDC technologies have been employed with the objective of achieving one or more of the following purposes.
1. Reduction of line losses while transmitting bulk power across long distances
2. Power exchange between asynchronous ac systems
3. Subsea power transmission in medium and long distance range
Since the HVDC converters introduce power losses by themselves, there is a break even distance for which the use of HVDC transmission becomes more beneficial over the use of ac power transmission solution. This distance is roughly around 600 km for overhead transmission and 50 km for cable based solution. This explains why HVDCs are more often used for offshore systems than for land based systems. In recent years, however, the use of HVDC on land has also been increasing mainly due to the relative ease of getting concessions for cable transmission than for overhead lines. This is primarily due to increased public resistance against overhead lines compared with cable transmission. While this may be one positive factor for developing cable based HVDC transmission on land, the high cost of this solution compared to overhead ac transmission lines has remained to be the main drawback

of cable based HVDC transmission for land based applications.
In places where several point-to-point connected HVDC lines are needed or planned within close distances (to each other) it would be appropriate to ask if a multi-terminal HVDC connection could be employed instead of the traditional point-to-point configuration. The North Sea region is such an area where the use of multi-terminal HVDC (MTDC) should be considered. There are two main reasons for this. First, development of offshore wind farms in particular has contributed to increased demand for subsea HVDC transmission. With vast amount of wind power resources, several offshore wind farms have been developed in the North Sea region and several more large scale wind farms are expected to be developed in the region in the near future. Horns Rev II, Thanet and Gunfleet Sands are some of the wind farms in the region already in operation. In 2010 a license was granted to a consortium of developers to develop a wind farm in Doggerbank [18]. The wind farm is projected to develop up to 9 gigawatt of power, as part of a planned nine zone project of 32 gigawatt - an amount equal to a quarter of the current power demand in UK. All these wind farms will use VSC based HVDC technology for transmitting power from the generation sites to the load centers within the land based grid systems.
The second reason which makes MTDC attractive for the North Sea region is that offshore oil and gas extraction activities in this region have created additional market for HVDC connections between the onshore power grid and loads at offshore platforms. Troll-A and Valhall HVDC connections, which went operational in 2005 and 2011 respectively, show the trend of electrifying the offshore oil/gas platforms from onshore, thereby replacing the power supplied by gas fired turbines on the platforms [52],[17].
With the newly emerging markets for offshore HVDC transmission, connecting several HVDC links into a multi-terminal dc grid can offer several additional advantages. To mention some, it can increase the reliability of power transmission by providing alternative transmission paths, and it can also facilitate power trading by connecting several market areas. HVDC links are also being used to exchange balancing services (secondary and tertiary control) across ac interconnections. This is commonly utilized for example on the Skagerrak HVDC link between Norway and Western Denmark. Though many potential advantages of meshed HVDC in the North Sea and beyond are pointed out, the technology is still under development and some crucial elements such as dc fault protection technology has yet to be fully developed. Moreover, deeper understanding of system control, operation and dynamics is needed before implementing the technology for commercial use. This is the focus of the research work described in this thesis.

1.2 Overview of the HVDC Technologies

When electricity supply was made available for commercial use for the first time towards the end of the 19^{th} century power was generated, transmitted and consumed in the form of direct current (DC) electricity. Later on, the invention of power transformers and alternator machines offered a much superior alternative of long distance power transmission in the form of alternating current (AC) electricity. As a result, the use of ac electricity became the standard in power generation, transmission and distribution systems.
With the development of mercury-arc ac/dc converters by the mid of the 20^{th} century, however, dc electricity made a comeback into power systems as an alternative solution for long distance power transmission. This time finding its application in the high voltage range, the term high voltage dc (HVDC) transmission was coined to refer to the new technology. Later on, mercury-arc based switches in ac/dc converters were replaced by thyristor switches. The thyristor based HVDC transmission, also called line commutated converter HVDC (LCC-HVDC), has been widely used in the past five decades. Due to its wide spread use and long history of application in power systems, LCC-HVDC is also referred to as classical HVDC.
Voltage source converter (VSC) based HVDC transmission (referred hereafter as VSC-HVDC) on the other hand is a relatively new arrival, with its first commercial use being the connection of the 40 MW wind farm at Näs (at the southern part of Gotland which is the largest Swedish island) to city of Visby at the center of the island [29]. This HVDC interconnection was made by ABB with its VSC-HVDC brand called HVDC Light. The connection has a power rating of 50 MW and has a pair of extruded dc cables of 70 km length. The maximum power capacity and voltage rating of VSC-HVDC has been steadily increasing since its first time use about thirteen years ago and by the time this thesis was written, ABB - one of the two leading commercial suppliers of this technology - claims to provide VSC-HVDC solutions with ratings up to 1200 MW/ $\pm$ 500 kV [10]. However, the largest HVDC Light connections currently in service have a rating of 400 MW/ $\pm$ 320 kV. The other major competitor in the market - Siemens - has completed its first ever HVDC PLUS (Siemens' brand name for their VSC-HVDC solution) project in 2010 which has a rating of 400 MW/ $\pm$ 200 kV [80]. Alstom - an other supplier of power generation and transmission equipments - has recently joined the VSC-HVDC market with its brand HVDC MaxSine [6],[11]. Alstom has been awarded its first VSC-HVDC project, the 1440 MW South-West Link, by the Swedish transmission system operator (TSO) Svenska Kraftnät in January 2012 with expected completion year of 2014 [8]. Currently the relatively low level of the maximum power capacity of available VSC-HVDC solutions means that LCC-HVDC still remains the dominant technology for long distance bulk power transmission due to lower investment costs and much higher maximum power transfer capacities. VSC-HVDC links, however, have

some unique advantages such as black start capability, reactive power support and smaller footprint of area which make them more suitable for offshore applications [89].

1.3 State of the Art of Multi-terminal HVDC (MTDC)

The use of HVDC technology have traditionally been limited to point-to-point interconnections. In recent years, however, there has been an increasing interest in R&D of MTDC systems partly due to technological advances in power electronics and VSC systems and partly due to the grid integration challenges that are coming with remotely located generation sites. Multi-terminal means, in this context, three or more converter stations are interlinked by a dc transmission network. Since there are two types of HVDC converters (LCC and VSC types), two types of dc grids are possible: one based on LCC -HVDC and the other based on VSC-HVDC. Some researches have also proposed hybrid MTDC transmission consisting of both LCC technology as well as VSC technology. Though combining the two technologies is an interesting issue from application point of view, this is not expected to make the operational and protection challenges one would face with such a system compared to similar challenges in the non-hybrid MTDC technologies.
There have been many research and development activities around MTDC in the past. While LCC based MTDC has been studied for many decades, VSC based MTDC is a relatively new topic (together with the VSC-HVDC technology) which has been getting increasing attention since the turn of the century. The first use of MTDC using LCC technology was the Quebec-New England HVDC Transmission. This interconnection was initially implemented as a two-terminal LCC-HVDC connection between La Grande II hydro power station in the James Bay area and load center in Montreal. The interconnection consisted of two LCC type converter stations each with a rating of 690 MW and was commissioned in 1986 [12]. Later on the line was extended further from Comerford to a new 1800 MW converter terminal at Sandy Pond, Massachusetts in 1992 making it in effect a three terminal LCC-HVDC system extending to the Boston area.
MTDC using VSC technology was, for the first time, deployed in 1999 Shin-Shinano substation in Japan. [85]. This system consists of three VSC-HVDC terminals with back-to-back connection and have been used for power exchange between 60 Hz and 50 Hz ac grids of Japan. Due to lack of dc transmission line/ cable in this system, however, it may not fully represent a typical multi-terminal VSC-HVDC grid system.
While the advantages of using MTDC in some specific cases (such as the North Sea region) can clearly be observed, the technology has yet to mature before implementing it for commercial use. Despite encouraging works in the literature on control and

protection of VSC based MTDC, there still remain several aspects of this system which need further investigation and understanding.
Several of the research works in the area of dc grid have focused on control of VSC terminals. As a result, different control strategies for MTDC operation are suggested in the literature. The major ones are dedicated dc swing bus control ([87],[88]), voltage margin control ([85], [84],[69]), and dc-bus voltage droop for power balance in the dc grid ([56],[56],[73]). These control strategies characterize how the converters respond to changes in power flow in the dc grid. The dc voltage droop control has been favored by many due to its better performance with dc voltage regulation of MTDC and due to its ability to facilitate provision of N-1 security.
Many studies in the literature have explored power flow analysis in dc grid with some of them including power flow analysis of ac/dc systems [39],[65],[40],[38],[28]. There have also been some research works reported in the literature on small-signal stability of MTDC [32],[68],[26],[14]. These studies, however, have typically been based on specific MTDC topologies consisting of three to four converter terminals and did not provide a generalized approach for analyzing any MTDC system regardless of the dc grid connection topology.
In references [15] & [50] the challenge of precise steady-state power flow control in MTDC transmission systems, employing dc voltage droop control, has been mentioned. It was correctly described in [15] that the difficulty arises due to unequal dc-bus voltages unlike that of grid frequency which is the same throughout the ac grid. Some studies have also been conducted in the area of MTDC fault handling and protection. While some of the studies in this area were focused on dc circuit breaker technology, some others were focused on the use of traditional breakers on the ac side of the VSC-HVDC station to interrupt dc fault currents.
Enhancement of MTDC control and operation methods was selected as one potential area of contribution from the research work. Moreover, it was observed that most of the previous studies have persistently used a qualitative approach to study the overall interaction of various converter terminals constituting the dc grid. In relation to this, interactions between VSC-HVDC terminals constituting the dc grid and interaction of the dc grid with the ac grids it is connected to has barely been studied in the literature. Hence the research described in this thesis work was started to fill these gaps.

1.4 Contributions of the Research Work

The contributions of the research work reported in this thesis can be grouped into three different aspects of MTDC system. These are (1) in the area of MTDC control, (2) in the area of MTDC operation, and (3) in the area of steady-state and dynamic

analysis of MTDC transmission systems.

1. Contribution in the area of MTDC control
A control method for primary reserves exchange between asynchronous ac grids connected to an MTDC system has been proposed. The method does not require the use of fast communication between various terminals of the dc grid.

2. Contribution in the area of MTDC operation
Dc voltage droop control in MTDC poses a challenge of getting the power flow profile to the desired levels. In the research work a method for achieving precise steady-state power flow in MTDC has been proposed. Based on this method, precise secondary control implementation scheme for MTDC has been outlined and analyzed.

3. Contribution in the area of MTDC analysis
Analytical modeling approaches have been proposed for steady-state and dynamic analysis of MTDC systems. The contributions comprise of (a) analytical expression for the distribution of primary power flow exchange in MTDC (b) analytical expression for steady-state ac/dc interactions for arbitrary connection topology (c) a new approach for state-space modeling of arbitrary dc grid topology (d) a new method for large-disturbance stability analysis of MTDC system.

With the help of different example MTDC systems modeled in PSCAD/EMTP simulation software package, the merits claimed for each of the proposed control methods and the validity of proposed analysis approaches have been verified.

1.5 Outline of the Thesis

The outline of the thesis is as follows. In chapter two various control methods of VSC-HVDC terminals are explored. This is followed by operational and steady-state analysis of MTDC in chapter three. Chapter four investigates dynamic analysis of MTDC systems with focus on large-disturbance analysis and state-space modeling of MTDC systems. In chapter five potential benefits of MTDC in the North Sea area are discussed. This is done with the help of simulation results for a hypothetical scenario of MTDC transmission in the North Sea region. Finally, conclusions are drawn in chapter six.

1.6 List of Publications

Some of the results of this research work were published in various journals and conference proceedings. These publications are listed below.

Journal Papers

1. T. Haileselassie, K. Uhlen, *'Impact of dc Line Voltage Drops on Power Flow of MTDC Using Droop Control, IEEE Transactions on Power Systems'*, Early access articles, March 2012.

2. T. Haileselassie, K. Uhlen, *'Power System Security in a Meshed North Sea HVDC Grid'*, Proceedings of the IEEE, accepted for review.

Conference Papers

3. T. Haileselassie, K. Uhlen, *'Precise Control of Power Flow in Multiterminal VSC-HVDCs Using Dc Voltage Droop Control'*, IEEE-PES General Meeting 2012, San Diego, USA, 22-26 July 2012.

4. T. Haileselassie, R. E. Torres-Olguin, T. K. Vrana, T. Undeland *'Main Grid Frequency Support Strategy for VSC-HVDC Connected Wind Farms with Variable Speed Wind Turbines'*, Proceedings of the 2011 IEEE Trondheim PowerTech, Trondheim, Norway, 19-23 June 2011.

5. T. Haileselassie, K. Uhlen, *'Primary Frequency Control of Remote Grids Connected by Multi-terminal HVDC'*, Proceedings of the IEEE-PES General Meeting 2010, Minnesota, USA, 25-29 July 2010.

6. T. Haileselassie, M. Molinas, T. Undeland, *'Multi-Terminal VSC-HVDC System for Integration of Offshore Wind Farms and Green Electrification of Platforms in the North Sea'*, Proceedings of Nordic Workshop on Power and Industrial Electronics (NORPIE'08), Espoo, Finland, 9-11 June 2008.

7. T. Haileselassie, K. Uhlen, *'Frequency Sensitivity Analysis of ac Grids Connected to MTDC Grid'*, Proceedings of the 9th IET International Conference on AC and DC Power Transmission (ACDC 2010), 19-21 October 2010.

8. T. Haileselassie, K. Uhlen, J. O. Tande, O. Anaya-Lara, *'Connection Scheme for North Sea Offshore Wind Integration to UK and Norway: Power Balancing and Transient Stability Analysis'*, Proceedings of the 2011 IEEE Trondheim PowerTech, Trondheim, Norway, 19-23 June 2011.

9. T. Haileselassie, K. Uhlen, *'Control of Multi-terminal HVDC and Its Impact on Multi-national Power Market'*, Proceedings of Cigré International Symposium, Recife, Brazil, 3-6 April 2011.

10. T. Haileselassie, K. Uhlen, *'Control of Multiterminal HVDC Transmission for Offshore Wind Energy'*, Nordic Wind Power Conference, Bornholm, Danemark, 7-11 September 2009.

11. T. Haileselassie, K. Uhlen, *'Power Flow Analysis of Multi-terminal HVDC Networks'*, Proceedings of the 2011 IEEE Trondheim PowerTech, Trondheim, Norway, 19-23 June 2011.

12. T. K. Vrana, R. E. Torres-Olguin, B. Liu, and T. Haileselassie, *'The North Sea Super Grid - A Technical Perspective,'* Proceedings of the 9th IET International Conference on AC and DC Power Transmission (ACDC 2010), 19-21 October 2010.

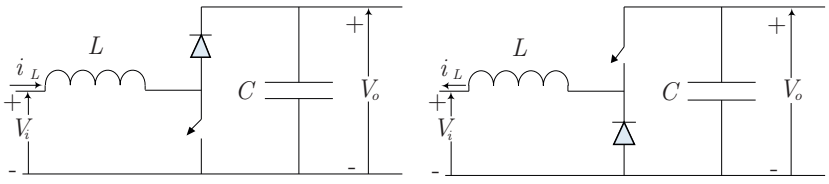
13. L. Zeni, T. Haileselassie, G. Stamatiou, A. G. Eriksen, J. Holbøll, O. Carlsson, K. Uhlen, P. E. Sørensen, Nicolaos A. Cutululis, *'DC Grids for Integration of Large Scale Wind Power'* Proceedings of EWEA OFFSHORE 2011, 29 November-1 December 2011.

2 CONTROL OF VSC-HVDC TERMINALS

This chapter deals with various types of controls used in VSC-HVDC terminal operation. As an introduction to this chapter, the first section discusses the fundamental principles of operation of VSC along side with its application areas. The different types of approaches used for VSC modeling are also discussed here. This is followed by a discussion on the two types of ac grids, namely: active ac grid and passive ac grid. Section 2.3.2 discusses the inner current controller, which is the most basic component of VSC control during connection to an active ac grid. This is followed by discussion on the various types of outer controllers which build upon the hierarchy of the complete HVDC control system. Control of VSC in a two-terminal configuration and frequency support of ac grid by a point-to-point VSC-HVDC interconnection are discussed in sections 2.5 and 2.6 respectively.

2.1 VSCs: Principle of Operation and Application Areas

Voltage source converter (VSC) is a bidirectional ac/dc power converter which utilizes fully controllable switching semiconductor devices. Voltage source converters can be single phase VSC or three-phase VSC. Three-phase VSC is more prevalent than the single phase type and hence the acronym VSC is commonly used to refer to three-phase VSC. The working principles of VSC can easily be understood by tracing back its structure to buck and boost dc/dc converters. Buck converter and boost converter are switch mode power converters used for stepping up and stepping down of dc voltage levels respectively.



(a) Step - up converter *(b) Step - down converter*

Figure 2.1: Step-up (boost) and step down (buck) converters

In Fig 2.1 the symbols L and C refer to the current smoothing inductive filter and voltage smoothing capacitive filter respectively. The step-down converter in Fig 2.1(b) is laterally inverted for the sake of convenience in comparing its structure with the step-up converter. As a result, the power flows in the two dc/dc converters

have opposite directions. By merging the two types of dc/dc converters we get the bidirectional DC/DC converter shown in Fig 2.2. When current in the inductor is flowing from the left to the right, only the step-up converter part will be active while the step-down converter remains inactive. Similarly when current flow direction in the inductor is reversed, the step-down converter will be active while the step-up converter remains inactive. Normal operation of the bi-directional DC/DC converter requires the voltage on the left side (V_i) to be less than the voltage on the right side (V_o). This constraint means that the input side voltage of this converter can also be an ac voltage of amplitude less than (V_o), making it in effect a switch-mode bidirectional ac/dc converter. The system in Fig 2.2 (excluding the capacitor) is commonly called half-bridge. By connecting two half-bridge switch mode converters

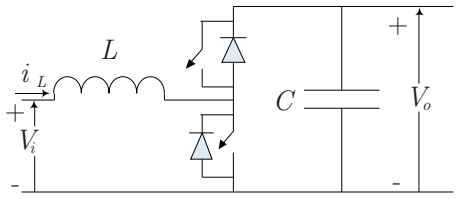


Figure 2.2: Bidirectional switch mode converter

to a common dc-bus we get the full-bridge converter topology. Both half-bridge and full-bridge topologies can be used for power conversion between a single phase system and a dc link. The later one is, however, used more commonly. Fig 2.3 shows the schematic of a full-bridge VSC. Three half-bridges, each connected to different

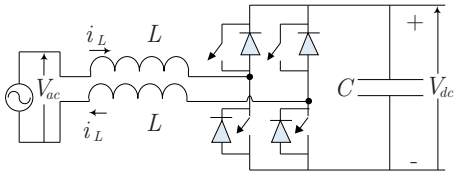


Figure 2.3: Full-bridge switch mode converter topology

phases of a three-phase system make up the three-phase switch mode converter (commonly referred simply as VSC). The most common application of VSCs is in induction machine drive systems. Due to their lower prices and ruggedness, induction motors have been the most widely used machines both in small and large applications for a long time. However, applications requiring precise speed control had to rely upon dc motors due to their superior controllability. Developments in

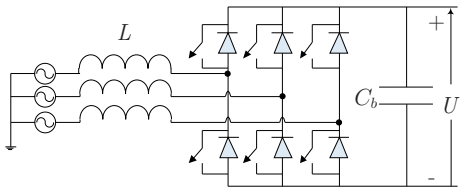


Figure 2.4: Three-phase VSC

semiconductor technology as well as micro controllers has led to the arrival of VSC driven induction motors with very fast and precise control of torque and speed. As a result, VSC drive systems have in recent years been taking over dc motors both in small house appliances as well as in large industrial applications.

Application of VSCs is not only limited to drive systems but also includes medium and high voltage power transmission systems. The main applications of VSCs in medium and high voltage areas include reactive power compensation, high voltage dc transmission (HVDC), dynamic voltage restoration and active power filtering. A VSC used for reactive power support is commonly referred to as static compensator (STATCOM) as opposed to the mechanically rotating compensator (also called synchronous compensator). Compared to synchronous compensator, a STATCOM has the advantages of lower losses (due to absence of moving parts) and faster controllability. On the down side, STATCOM has lower short circuit capability compared to synchronous compensator and no inertia. VSCs have also been used in HVDC application (commonly referred to as VSC-HVDC) in the last decade. Table 2.1 shows the list of some of the major HVDC connections around the world which employed VSC technology [5].

2.2 VSC Modeling Approaches

VSCs can be modeled either in detail, i.e. including all semiconductor components or by a time-averaged approach. In detailed modeling of VSC, each set of semiconductor device acting as a single unit is represented in the electrical model. Detailed modeling of VSCs requires electromagnetic transient simulation tools such as PSCAD, ATP, PSIM or SimPower toolbox of Matlab. In the detailed VSC model, it will also be shown clearly whether the VSC is of two-level or multilevel type.
The detailed modeling of VSCs is usually required for analyzing pulse width modulation (PWM) techniques, different VSC topologies (such as various multilevel VSCs), high frequency harmonic components and for accurate study of VSC losses.

Table 2.1: List of HVDC Light projects currently in service

Project	In Service	Rating & distance	Connection	Application
HÄLLSJÖN Sweden	1997	3 MW/ ± 10 kV 10 km(overhead)	Hällsjön-Grängesberg	Pilot system
GOTLAND Sweden	1999	50 MW/ ± 80 kV 70 km	Näs-Bäcks	Wind, Undergrounding
DIRECTLINK Australia	2000	3 × 60 MW/ ± 80 kV 65 km	Terranora-Mullumbimby	Undergrounding
TJÆREBORG Denmark	2000	7, 2 MW/ ± 9 kV 4, 4 km	Enge-Tjaereborg	Wind, Undergrounding
EAGLE PASS USA	2000	36 MW/ ± 15, 9 kV NA, (back-to-back)	Eagle Pass (both sides)	Grid reliability
CROSS SOUND USA	2002	330 MW/ ± 150 kV 40 km	New Haven-Shoreham	Grid reliability
MURRAYLINK Australia	2002	220 MW/ ± 150 kV 180 km	Berri-Red Cliffs	Wind, Undergrounding
TROLL A Norway	2005	2 × 41 MW/ ± 60 kV 67 km	Kollsnes-Troll	Offshore
ESTLINK Estonia-Finland	2006	350 MW/ ± 150 kV 105 km	Espoo-Harku	Grid reliability, Undergrounding
BORWIN1 Germany	2009	400 MW/ ± 150 kV 70 km	Diele-Borkum 2	Offshore wind,
Caprivi Link Namibia	2009	300 MW/ 350 kV 970 km (overhead)	Zambezi-Gerus	Grid reliability
VALHALL Norway	2010	50 MW/ 150 kV 70 km	Lista-Valhall	Offshore

In time-averaged VSC modeling, there is no distinction between the different types of modulation and the different number of switching levels (two-level and multilevel). On the other hand, all phenomena related to the fundamental frequency voltage and current components can be sufficiently studied by use of time-averaged VSC models. Time-averaged VSC model consists of controllable three-phase ac voltage sources connected to the ac circuit and a controllable current source connected to the dc circuit. Time-averaged VSC model is shown in Fig. 2.5. V_a, V_b and V_c refer to the three phase voltages generated by the VSC behind the inductive ac filter whereas i_a, i_b and i_c refer to the resulting phase currents flowing from the ac grid into the VSC. L and r represent the inductance and resistance of the series connected ac filter of the VSC while C represents the dc-bus capacitance which acts as a shunt filter. U and I_{DC} represent the dc-bus voltage and the dc current that flows out of the dc-bus into the dc cables. I_o is the current injected by the VSC into the dc grid and measured behind the dc-bus capacitor.

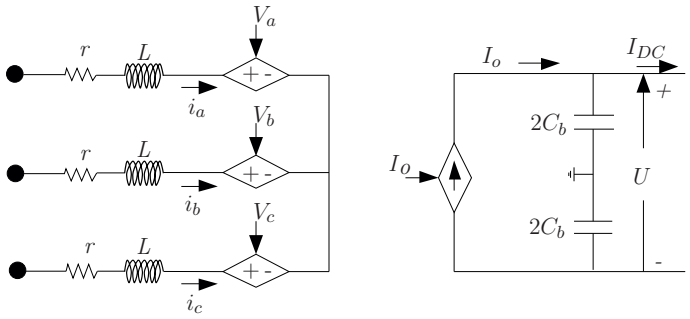


Figure 2.5: Time averaged VSC model

The ac and dc circuits of the time averaged VSC model, i.e. the left side and the right side of Fig. 2.5, are related by conservation of power. This means the sum total of power consumed by the three controllable phase voltage sources (V_a, V_b and V_c) equals the power injection by the controllable current source I_o into the dc-bus. Further more the three phase voltages are controlled by their respective modulation indexes, namely: m_a, m_b and m_c. The relationship between the ac and dc circuits in Fig. 2.5 can be summarized as follows:

$$\left.\begin{aligned} V_a &= \tfrac{m_a U}{2} \\ V_b &= \tfrac{m_b U}{2} \\ V_c &= \tfrac{m_c U}{2} \end{aligned}\right\} \tag{2.1}$$

$$I_o = \frac{m_a i_a + m_b i_b + m_c i_c}{2} \tag{2.2}$$

Time-averaged modeling of VSC can be implemented in both electromagnetic transient simulation tools (such as PSCAD, ATP, PSIM and SimPower toolbox of Matlab) and power flow simulation tools (such as PSS/E, Power Factory, SIMPOW). Although it is not always the case, in time-averaged VSC modeling quite often it is assumed that the currents in the three phases are balanced, i.e. the sum total of the instantaneous currents of all the three phases is zero. In such a case, the neutral point of the controllable ac voltage sources in Fig. 2.5 can remain floating. If, on the other hand, the ac currents under investigation have zero sequence current (and hence resulting in unbalanced condition), then the neutral point of the ac voltage sources in Fig. 2.5 should be grounded for accurate representation of the three-phase current flow.
Due to the absence of switching components and the associated high frequency phenomena, much larger time steps can be used in simulation of the time-averaged VSC model compared to the time steps needed for detailed VSC modeling. This, in effect, reduces the simulation time by a large factor. Moreover, the fewer number of electrical components used in the time-averaged modeling means that smaller amount of memory is used while running the simulation in comparison with the detailed VSC simulation. These advantages become even more crucial particularly when the simulated system consists of several VSC units. Multi-terminal VSC-HVDC system is a representative case where the use of time-averaged modeling enables much faster simulation compared to the detailed modeling. Due to these advantages, time-averaged VSC modeling has been used in the simulations throughout this thesis work.

2.3 VSC Control

2.3.1 Passive and Active AC Grid Connection of VSCs

There are two types of ac connections to VSCs, namely active ac grid connections and passive ac grid connections. In active grid connection VSC must synchronize

to a system frequency and the VSC can influence the frequency only partly. An active ac grid connection (also called active front end converters) involves ac grid which is active (live) even before the VSC is connected to it. This means that the ac grid has active sources such as synchronous generators and/or other components that inject power into the ac grid. On the other hand in passive ac grid connection the VSC defines the frequency. This means the ac grid relies primarily on the VSC for ac voltage control. Apart from ac loads, passive ac grid connection may also consist of distributed generation systems which depend on the ac voltage of a large VSC unit (possibly VSC-HVDC station) for synchronizing into the grid and inject power. Passive grid connected VSCs are equipped with ac voltage control which enables to provide ac voltage of fixed frequency and fixed magnitude at the point of common coupling (PCC). PCC is defined as the junction point where the VSC unit is connected to the ac grid. The ac voltage controller enables the VSC to act as the slack bus of the connected ac grid. VSC connected to passive grid has a relatively simple control scheme. By comparison to passive grid connection, active ac grid connection of VSC requires a more sophisticated controller. A good example of passive grid connection is a VSC-HVDC link supplying power to an island or to an offshore platform. VSC-HVDC linked wind farm is another example. In the case of VSC-HVDC connected wind farm, each individual wind turbine - converter unit has to synchronize its ac voltage to that of the VSC-HVDC terminal. In Fig. 2.6, single-line diagram of passive ac grid connected VSC and the corresponding ac voltage control are shown. Point x defines the connection point between the VSC and the ac grid, i.e. x is the PCC in this case.

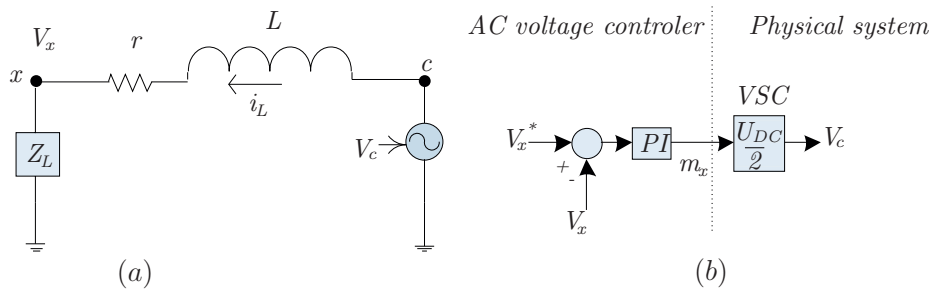


Figure 2.6: Single-line diagram of passive ac grid and corresponding ac voltage controller

The PCC is usually located next to the ac inductive filter, as in the case of Fig. 2.6(a). V_c and V_x refer to the internal ac voltage generated by the VSC and the ac voltage at PCC respectively. Z_L represents the passive load impedance and i_L refers to the load current. The purpose of the ac voltage controller is to maintain

the voltage at PCC close to the given reference (V_x^* in Fig. 2.6(b)). Most commonly proportional-integral (PI) or proportional (P) controller is used to achieve this purpose. The output from the controller is the modulation index (m_x) which is then provided to the pulse width modulator (PWM).
As mentioned before, in active ac grid connection system frequency is defined by the VSC-HVDC terminal. As a result, the converter should be equipped with synchronization mechanism to inject active and reactive power into the ac grid. In such a case, the VSC controls two distinct quantities, namely: active current and reactive current. Active current is the ac current component which is associated with active power injection. Similarly, the reactive current is the ac component associated with the reactive power injection.

2.3.2 Inner Current Control Loop of Active Grid Connection

The inner current controller is the most fundamental part of VSC control for active ac grid connection (referred also as active front end connection). Inner current controller is always equipped with a phase lock loop (PLL) for detection of phase angle and frequency. While in many cases the PLL requires ac voltage measurements from PCC, there have also been sensorless types of PLLs proposed in the literature which depend entirely on the ac current measurements for estimation of frequency and phase angle [25].
Based upon the reference frames used, there are two alternative approaches for VSC control with active front end. The first one, here referred as $m - \phi$, involves direct control of the amplitude (m) and phase angle (ϕ) of the VSC output voltage with respect to the ac voltage at PCC. The other alternative, usually referred as $d - q$ control, is depends upon synchronously rotating reference frame for observing all the ac voltage and current quantities involved in the VSC control.
Conceptually, the $m - \phi$ control is directly linked to the phasor representation of VSC. This can be understood by looking at the diagrams in Fig. 2.7. The current flowing from the ac grid into the VSC is given by

$$I\angle\theta = \frac{V_x\angle 0 - V_c\angle\phi}{r + j\omega L} \tag{2.3}$$

From the vector diagram in Fig. 2.7 (b), it can be observed that the voltage drop across the inductive filter is composed of two parts, namely: voltage drop across the resistance (r) and voltage drop across the inductive reactance ($j\omega L$). In high voltage applications, the voltage drop of VSC due to the inductive reactance is typically more than ten-times the voltage drop across the resistance. As a result, the resistive part of the filter impedance can be neglected without losing much accuracy of the power

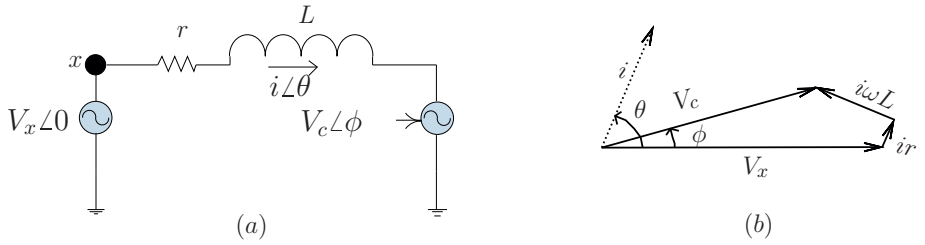


Figure 2.7: Power flow in active grid connected VSC: (a) Single-line diagram (b) Phasor diagram

flow relationship. Hence (2.3) can be approximately written as

$$\left.\begin{aligned} i\angle\theta &\simeq \tfrac{V_x\angle 0 - V_c\angle\phi}{j\omega L} \\ &\simeq -\tfrac{V_c\sin\phi}{\omega L} - j\tfrac{V_x - V_c\cos\phi}{\omega L} \end{aligned}\right\} \tag{2.4}$$

The apparent power (S) flow into the VSC is given by

$$\left.\begin{aligned} S &= V_x\angle 0\,(i\angle\theta)^* \\ &= V_x\Big(-\tfrac{V_c\sin\phi}{\omega L} - j\tfrac{V_x - V_c\cos\theta}{\omega L}\Big)^* \\ &= -\tfrac{V_xV_c\sin\phi}{\omega L} + j\tfrac{V_x(V_x - V_c\cos\theta)}{\omega L} \end{aligned}\right\} \tag{2.5}$$

Let m_c refer to the modulation index phasor. Substituting $\frac{m_cU}{2}$ in place of V_C, we get the apparent power in terms of the modulation index as follows:

$$S = P + jQ = -\frac{V_xm_cU\sin\phi}{2\omega L} + j\frac{V_x\,(2V_x - m_cU\cos\theta)}{2\omega L} \tag{2.6}$$

The sensitivity of apparent power with respect to phase angle (ϕ) and modulation index (m_c) are as follows:

$$\frac{\partial S}{\partial m_c} = \frac{\partial P}{\partial m_c} + j\frac{\partial Q}{\partial m_c} = -\frac{V_xU\sin\phi}{2\omega L} - j\frac{V_xU\cos\phi}{2\omega L} \tag{2.7}$$

$$\frac{\partial S}{\partial \phi} = \frac{\partial P}{\partial \phi} + j\frac{\partial Q}{\partial \phi} = -\frac{V_xUm_c\cos\phi}{2\omega L} + j\frac{V_xUm_c\sin\phi}{2\omega L} \tag{2.8}$$

At rated operating conditions, the modulation index phasor m_c is close to one while the power angle in radians, ϕ, is a small number (i.e, $|\phi| << 1$). Hence from (2.7) and (2.8) the following inequality can be derived:

$$\left.\begin{aligned} \sin\phi|_{\phi\to 0} &\ll m_c\cos\phi|_{\substack{\phi\to 0\\ m_c\to 1}} \\ \left.\tfrac{V_x U\sin\phi}{2\omega L}\right|_{\phi\to 0} &\ll \left.\tfrac{V_x U m_c\cos\phi}{2\omega L}\right|_{\substack{\phi\to 0\\ m_c\to 1}} \\ \left.\left|\tfrac{\partial P}{\partial m_c}\right|\right|_{\substack{\phi\to 0\\ m_c\to 1}} &\ll \left.\left|\tfrac{\partial P}{\partial\phi}\right|\right|_{\phi\to 0} \end{aligned}\right\} \tag{2.9}$$

From (2.9) we can observe that the active power flow via the VSC is highly sensitive to changes in power angle (ϕ) and only slightly sensitive to the magnitude of the modulation index phasor (m_c). Following similar procedure as in (2.7), comparison of the sensitivities of reactive power flow with respect to the two parameters (ϕ and m_c) gives the inequality given by

$$\left.\left|\frac{\partial Q}{\partial\phi}\right|\right|_{\phi\to 0} \ll \left.\left|\frac{\partial Q}{\partial m_c}\right|\right|_{\substack{\phi\to 0\\ m_c\to 1}} \tag{2.10}$$

From equation (2.10) we see that reactive power flow is highly sensitive to m_c and only slightly affected by changes in the power angle ϕ. Hence active power/current control is achieved through control of the power angle parameter ϕ whereas reactive power/current is controlled by the magnitude of the modulation index m_c. The $m-\phi$ control requires that only positive sequence current and voltage are involved in the VSC power flow.

The $d-q$ control approach is based upon representing the three-phase ac quantities by an equivalent set of two-phase quantities resulting in identical resultant space vector (called virtual flux) as the original three-phase space-time phasor representation [66]. The $d-q$ control approach originated from electric machine and drives application areas and became the most dominant control approach in many application involving VSCs. The $d-q$ control approach often assumes that all the ac quantities under consideration (voltages and currents) are balanced all the time. If the vector X_a, X_b and X_c refer to hypothetical three-phase quantities, the vector $X_{\alpha\beta}$ is given by the sum total space-vector of the three phases with 120^o separation apart from each other. *abc* and $\alpha-\beta$ reference frames are shown in Fig. 2.8.

The phase transformation from stationary *abc* to stationary $X_{\alpha\beta}$ frame of reference is by Clark transformation as

$$X_{\alpha\beta} = X_\alpha + jX_\beta = k\left[X_a + X_b e^{j\frac{2\pi}{3}} + X_c e^{j\frac{4\pi}{3}}\right] \tag{2.11}$$

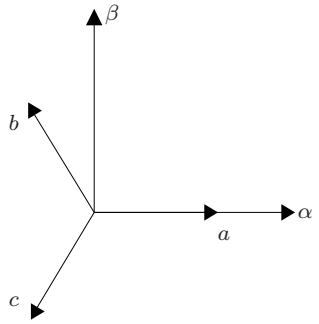


Figure 2.8: Stationary reference frames: *abc* and $\alpha - \beta$

where k is a constant number.
In matrix form Clark transformation is given by

$$\begin{bmatrix} X_\alpha \\ X_\beta \end{bmatrix} = k \begin{bmatrix} 1 & \frac{-1}{2} & \frac{-1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{-\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} X_a \\ X_b \\ X_c \end{bmatrix} \tag{2.12}$$

A vector in $\alpha - \beta$ reference frame can further be expressed interims of another two phase reference frame with a phase shift of θ with respect to the $\alpha - \beta$ reference frame. The new reference frame is here referred as $d - q$ reference frame. A phasor expressed in $\alpha - \beta$ and $d - q$ reference frames is shown in Fig. 2.9.

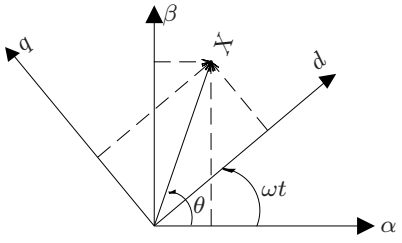


Figure 2.9: Vector transformation between two-axes reference frames with displacement of angle ωt

If k is taken as $\sqrt{2/3}$, the power calculated in the $d-q$ reference frame will have the same magnitude as the power calculated from *abc* reference frame and the transfor-

mation is said to be power invariant [45](pp.328). On the other hand if $k = \frac{2}{3}$ is chosen, the amplitude of the phase voltages in both $d-q$ and abc reference frames will be the same and the transformation is said to be voltage invariant. In this thesis work, voltage invariant Park and inverse Park transformations have been used. Now with the concept of $d-q$ transformations in mind, we will discuss the mathematical representation of VSC in synchronously rotating $d-q$ reference frame. A single-line diagram of a VSC terminal is shown in Fig. 2.10.

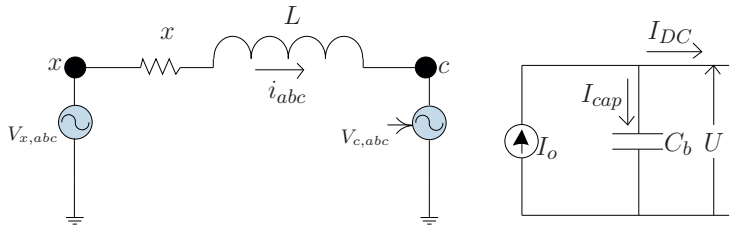


Figure 2.10: Single-line representation of VSC

In Fig. 2.10 L and r represent the total inductance and resistance coming from transformer and phase reactor. Point x is the PCC of the VSC and the ac system. This is the reference point for measuring ac quantities. $V_{x,abc}$ and $V_{c,abc}$ refer to ac voltage at points x and c respectively. c is a fictitious measurement point for converter output voltage. Bear in mind that in practice it is not possible to measure the fundamental frequency voltage ($V_{c,abc}$) just next to the semiconductors (at point c) due to the presence of high frequency harmonics at this location.
Now if we apply Kirchhoff's Voltage Law (KVL) across points x and c, we get

$$V_{x,abc} - V_{c,abc} = ri_{abc} + L\frac{di_{abc}}{dt} \tag{2.13}$$

Applying voltage invariant Clark transformation gives

$$V_{x,\alpha\beta} - V_{c,\alpha\beta} = ri_{\alpha\beta} + L\frac{di_{\alpha\beta}}{dt} \tag{2.14}$$

Park's transformations of $V_{x,abc}$, $V_{c,abc}$ and i_{abc} are given by

$$\left.\begin{aligned} V_{x,\alpha\beta} &= V_{x,dq}e^{j\omega t} \\ V_{c,\alpha\beta} &= V_{c,dq}e^{j\omega t} \\ i_{\alpha\beta} &= i_{dq}e^{j\omega t} \end{aligned}\right\} \tag{2.15}$$

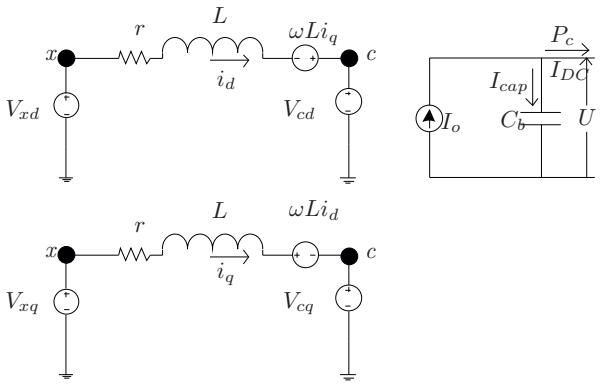


Figure 2.11: Dynamic circuit of VSC in dq reference frame

where ω is operating frequency of the ac network. Substituting (2.15) in (2.14) we get

$$\left.\begin{aligned} V_{x,dq}e^{j\omega t} - V_{x,dq}e^{j\omega t} &= ri_{dq}e^{j\omega t} + L\frac{d\left(i_{dq}e^{j\omega t}\right)}{dt} \\ &= ri_{dq}e^{j\omega t} + j\omega Li_{dq}e^{j\omega t} + e^{j\omega t}L\frac{di_{dq}}{dt} \end{aligned}\right\} \tag{2.16}$$

Diving all the terms in (2.16) by $e^{j\omega t}$ results in

$$V_{x,dq} - V_{c,dq} = ri_{dq} + j\omega Li_{dq} + L\frac{di_{dq}}{dt} \tag{2.17}$$

The expanded form of (2.17), after rearranging, becomes

$$L\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} V_{xd} \\ V_{xq} \end{bmatrix} - \begin{bmatrix} V_{cd} \\ V_{cq} \end{bmatrix} - r\begin{bmatrix} i_d \\ i_q \end{bmatrix} - \omega L\begin{bmatrix} 0 & 1 \\ -1 & 0 \end{bmatrix}\begin{bmatrix} i_d \\ i_q \end{bmatrix} \tag{2.18}$$

$\left[\begin{smallmatrix} 0 & 1 \\ -1 & 0 \end{smallmatrix}\right]$ is the matrix form of the imaginary unit j and has an effect of displacing phasors by 90°. Based on (2.18), the d and q axes equivalent circuits of the VSC, as seen from the ac network side, are given by Fig. 2.11. The apparent power exchange, S, observed from reference point x and in $d-q$ reference frame is given by

$$\left.\begin{aligned} S &= \tfrac{3}{2}V_{x,dq}i^*_{dq} \\ &= \tfrac{3}{2}(V_{xd} + jV_{xq})(i_d - ji_q) \\ &= \tfrac{3}{2}\left\{(V_{xd}i_d + V_{xq}i_q) + j(V_{xq}i_d - V_{xd}i_q)\right\} \end{aligned}\right\} \tag{2.19}$$

For a steady-state operation, active power exchange, P_c', at the ac side (at PCC) will be equal to the power exchange at the dc-bus, P_c (neglecting the semiconductor and filter losses). This is mathematically given as follows:

$$\left.\begin{aligned} P_c' &= P_c \\ \tfrac{3}{2}(V_{xd}i_d + V_{xq}i_q) &= UI_{DC} \end{aligned}\right\} \tag{2.20}$$

From equation (2.20), the dc current at steady-state becomes

$$I_{DC} = \frac{P_c'}{U} = \frac{3\left(V_{xd}i_d + V_{xq}i_q\right)}{2U} \tag{2.21}$$

The converter as seen from the dc network side will be a constant current source of magnitude I_{DC}. When active ac network is connected with VSC, the use of $d-q$ reference frame in the control design and implementation enables to make a fully decoupled linear control of active and reactive currents.. The $d-q$ reference frame is selected in such a way that the d-axis is aligned to the voltage phasor of phase-A of point x. This means that the PLL should be phase locked to phase-A voltage phasor of the reference point, x. This results in

$$\left.\begin{aligned} V_{xq} &= 0 \\ V_{xd} &= V_x \end{aligned}\right\} \tag{2.22}$$

Hence active power (P_c') and reactive power (Q) of the VSC measured at the PCC (point x) become as follows:

$$\left.\begin{aligned} P_c' &= \tfrac{3}{2}V_{xd}i_d \\ Q_{dq} &= -\tfrac{3}{2}V_{xd}i_q \end{aligned}\right\} \tag{2.23}$$

The inner current controller is developed based upon (2.23) and the differential equation (2.18). In Fig. 2.12 the complete diagram of VSC including the inner and outer controllers is shown. Fig. 2.13 shows the simplified representation of d-axis and q-axis current controllers with the converter-filter model.

The converter has a delay of $e^{-T_\omega s} \simeq \frac{1}{1+T_\omega s}$ due to the sinusoidal pulse width modulator. T_ω is the switching and hence the inverse of the switching frequency (f_s) (i.e. $T_\omega = \frac{1}{2f_s}$). Proportional integral (PI) controllers are used for closed loop control and the zeros of the PI controllers are selected to cancel the dominant pole in the external circuit. For a typical VSC, the time constant due to the series filter, $\tau = L/r$ is much higher than the switching delay T_ω and hence will be the dominant pole to be

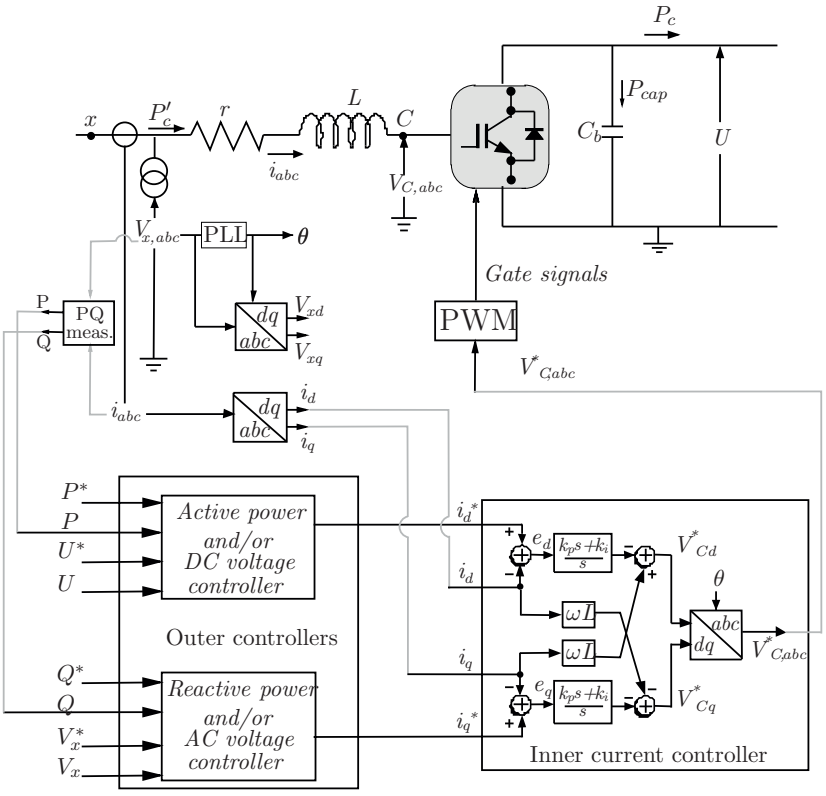


Figure 2.12: Complete diagram of VSC with inner and outer controllers

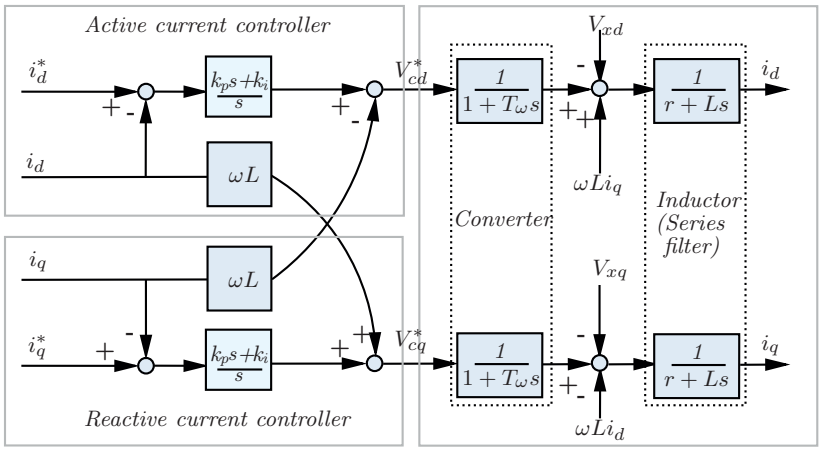


Figure 2.13: Simplified representation of inner current controller

canceled by the zero of the PI controller. The cross coupling currents in (2.18) are compensated by feed-forward terms in the controllers as shown in Fig. 2.13. i_d^* and i_q^* are reference currents for the d-axis and q-axis current controllers respectively.

The references of the inner current controller come from two outer controllers. The first outer controller consists of either of ac voltage controller or reactive power controller and the second one consists of either of dc voltage controller or active power controller. Active current (i_d) is used to control either of active power controller or dc voltage level controller. Similarly, the reactive current (i_q) is used to control either of reactive power flow into stiff grid connection or ac voltage support in weak grid connection. For further detailed discussions on inner current control of VSC, the reader is referred to [60] & [76].

2.3.3 Active Power Control

In the previous section it was discussed that for a synchronously rotating frame whose d-axis is aligned with the phase-A of the ac voltage at PCC, the q-axis component of the voltage measured at PCC becomes zero. As a result, power injection into the VSC becomes $P_c \simeq P_c' = \frac{3}{2} V_{xd} i_d$. In addition, the resultant voltage V_{xd} - which for the specified reference frame becomes equal to V_{xd} - is not desired to show large variations at any normal operating conditions. Hence, active power flow can be controlled by active current (i_d) as shown in Fig. 2.14.

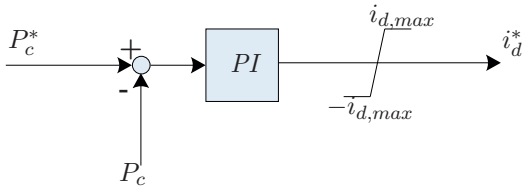


Figure 2.14: PI controller for active power control

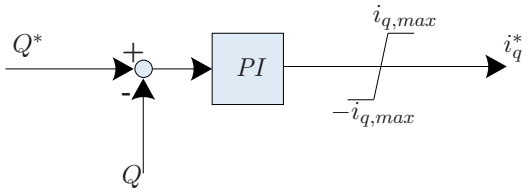


Figure 2.15: PI controller for reactive power control

The output of the active power controller (i_d^*) will be the reference input to the d-axis current controller of the inner current loop in Fig. 2.13.
In order to limit the magnitude of current in the VSC with in the allowable range, the output of the active power controller is followed by a limiter function (also called anti-wind up limiter) of $\pm i_{dmax}$ limits. The rated amplitude of the single phase current defines this limit as

$$i_{max} = i_N \tag{2.24}$$

2.3.4 Reactive Power Control

The reactive power from (2.19) is given by

$$Q_{dq} = -\frac{3}{2} V_{xd} i_q \tag{2.25}$$

The reactive power is controlled by reactive current (i_q) and is implemented as in Fig. 2.15. As in the case of active power control, i_q^* will be the reference input for the reactive current controller of the inner current loop in Fig. 2.13.
i_q^* is limited to $\pm i_{qmax}$ in such a way that the total converter current ($|i_{dq,max}|$) should

not exceed the rated current (i_N). Priority is often given to transfer of active power than reactive power. Hence, the reactive current limit becomes

$$i_{q,max} = \sqrt{{i_N}^2 - i_d^{*2}} \tag{2.26}$$

2.3.5 Integral Control of Dc-bus Voltage

From input-output power balance of the VSC-HVDC terminal shown in Fig. 2.12 we get the relation

$$\left.\begin{aligned} P_c' - P_c - P_{cap} - P_{Loss} = 0 \\ \tfrac{3}{2} V_{xd} i_d - P_c - P_{Loss} - U i_{cap} = 0 \end{aligned}\right\} \tag{2.27}$$

where P_c refers to the power transfered to the dc lines beyond the dc filter capacitance, i_{cap} refers to the current flowing into the dc filter capacitor and P_{Loss} refers to the power losses of the VSC including the inductive filter losses. From (2.27) the current through the capacitor becomes

$$i_{cap} = \left(\frac{3V_{xd} i_d}{2U} - \frac{P_c + P_{Loss}}{U}\right) \tag{2.28}$$

And the same current in terms of voltage across the capacitor is given by

$$i_{cap} = C_b \frac{dU}{dt} \tag{2.29}$$

From (2.28) and (2.29) the differential equation for the dc voltage becomes

$$\left.\begin{aligned} \tfrac{dU}{dt} &= \tfrac{1}{C_b}\left(\tfrac{3V_{xd} i_d}{2U} - \tfrac{P_c + P_{Loss}}{U}\right) \\ &= \tfrac{3V_{xd} i_d}{2C_b U}\left(i_d - \tfrac{2P_L}{3V_{xd}}\right) \end{aligned}\right\} \tag{2.30}$$

From equation (2.30) it can observed that dc voltage can be regulated by control of active current (i_d). $P_c + P_{Loss}$ in (2.30) can optionally be compensated by a feed forward control in the dc voltage regulator; but PI controller without a feed forward control can also work as well. In Fig. 2.16 block diagram of PI regulator for dc voltage control is shown. The integral dc voltage controller enables to maintain the dc-bus voltage constant (i.e. equal to the reference dc voltage U^*) irrespective of the fluctuations in power flow via the VSC as long as the power flow is within the capacity limits of the VSC-HVDC terminal. Hence the controller in Fig. 2.16 can also be called constant dc voltage controller.

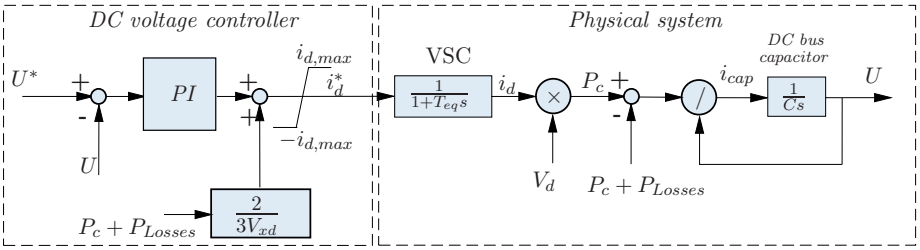


Figure 2.16: Block diagram of dc voltage PI controller

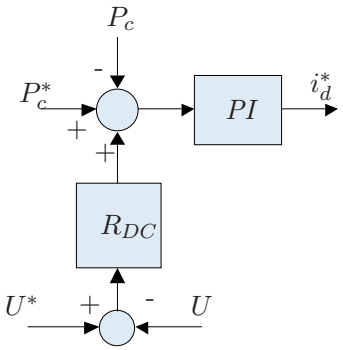


Figure 2.17: Block diagram of dc voltage droop controller

2.3.6 DC Voltage Droop Control

In sections 2.3.3 and 2.3.5 it was shown that both active power control and dc voltage control are achieved by controlling the reference to the active current controller i_d^*. If we combine the two types of controllers we get the dc voltage droop controller, shown in Fig. 2.17.

The dc voltage droop controller is characterized by power flow which changes linearly with the changes in dc-bus voltage. The constant R_{DC} in Fig. 2.17 determines the sensitivity of the active current controller to changes in dc-bus voltage in comparison with the power control error. Hence this constant can also be referred as dc voltage response (analogous to frequency response of synchronous generator). Frequency response in ac system is defined as the increment in MW of the generated power in response to decrement of the grid frequency by 1 Hz [45], [72]. (NB! Frequency response in this context means the response of a power system or equipment to a

change in system frequency and does not mean the frequency spectrum of a transfer function.) Similarly dc voltage response can be defined as increment in MW of injected power into the dc circuit in response to decrement of the dc-bus voltage by 1 kV.

2.3.7 AC Voltage Regulation

A weak grid can be defined as a connection that has significant line impedance in per-unit. This creates considerable voltage variations with changing active power flow. Therefore if the ac network connected to the VSC-HVDC terminal is a weak grid, the ac voltage at PCC must be regulated by the converter. Let $\widehat{i}$,$\widehat{V}_x$, and $\widehat{V}_C$ represent the phasors of the ac current flow into the VSC, the ac voltage at PCC and the internal ac voltage of the VSC respectively.

By applying Kirchhoff's voltage law (KVL) across the series ac filter (in Fig. 2.7) we get

$$\widehat{V}_x - \widehat{V}_s = (r + j\omega L)\widehat{i}_s \tag{2.31}$$

The current phasor $\widehat{i}_s$ is given by

$$\left.\begin{aligned} \widehat{i}_s &= \left(\tfrac{S}{V_x}\right)^* \\ &= \left(\tfrac{P+jQ}{V_x}\right)^* \\ &= \left(\tfrac{P-jQ}{V_x}\right) \end{aligned}\right\} \tag{2.32}$$

Substituting (2.32) into (2.31) gives

$$\left.\begin{aligned} \widehat{V}_x &= \widehat{V}_C + (r + j\omega L)\widehat{i}_s \\ &= \widehat{V}_C + (r + j\omega L)\left(\tfrac{P-jQ}{V_x}\right) \\ &= \widehat{V}_C + \left(\tfrac{Pr+Q\omega L}{V_x}\right) + j\left(\tfrac{P\omega L-Qr}{V_x}\right) \end{aligned}\right\} \tag{2.33}$$

The magnitude of ac voltage at PCC shows negligible amount of changes due to the imaginary (quadrature) component of the right side of equation (2.33). Therefore, the voltage at PCC is approximately given by

$$\widehat{V}_x = \widehat{V}_C + \left(\frac{Pr + Q\omega L}{V_x}\right) \tag{2.34}$$

Since the active power, P, is separately controlled, it can not be used to control the voltage $\widehat{V}_x$. Hence from (2.34), Q becomes the only available parameter for controlling the ac voltage at PCC. This relation is mathematically written as

$$\Delta V_x = \frac{\omega L}{V_x}\Delta Q \tag{2.35}$$

The block diagram of the ac voltage controller is given by Fig. 2.18.

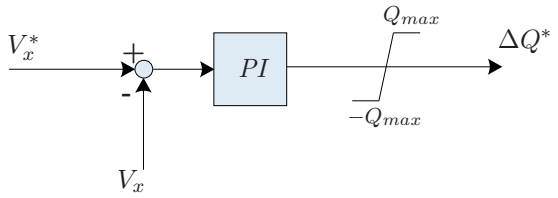


Figure 2.18: Ac voltage control by reactive power compensation

2.4 U vs P Characteristics of the Various VSC Control Modes

In ac grids each generation unit is mainly characterized by its rated power generation capacity and its steady-state frequency response characteristics. In case of VSC-HVDC grids, each converter station is characterized by its rated power transfer capacity, rated dc voltage level and its dc voltage response characteristic. The dc voltage characteristic of a VSC-HVDC terminal is determine by the type of outer controller employed for providing reference to the active current controller. It was discussed previously that there are three possible options for the outer current controller; namely: constant power controller, constant dc voltage controller and dc droop control. In this section we will look at the U vs P characteristics of the three aforementioned types of VSC-HVDC control modes.
Constant power controller and its corresponding dc voltage characteristic are shown in Fig. 2.19.

The dc voltage characteristics of constant power control mode is such that the power flow via the VSC-HVDC terminal (P_c) remains constant and equal to the

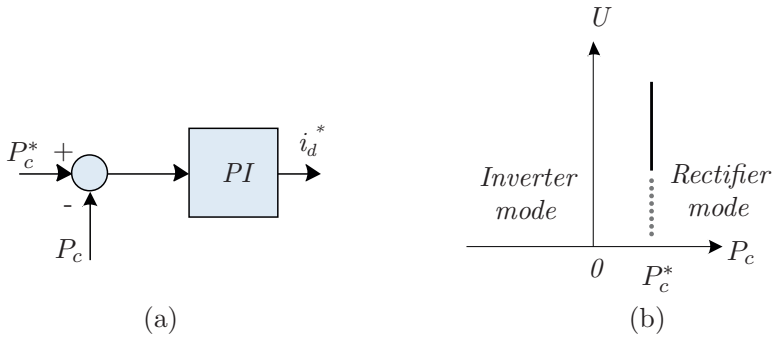


Figure 2.19: Constant power controller: (a) control schematic (b) dc voltage characteristics

power reference (P_c^*) regardless of the level of the dc voltage (U), hence the vertical characteristic line in Fig. 2.19. Due to the defined direction of the current flow in the development of active current controller in section 2.3.2, positive power flow corresponds to rectifier mode of operation and negative power flow corresponds to inverter mode of operation.
At steady-state, power flow via a VSC-HVDC terminal with constant power controller is

$$P_c = P_c^* \tag{2.36}$$

i.e, the steady-state power flow equals the applied power reference. Constant dc voltage controller and its characteristics are shown in Fig. 2.20.

The dc characteristic curve of a constant dc voltage controller is horizontal line corresponding to the dc voltage reference U^*. The steady-state characteristics of constant dc voltage control mode is

$$U = U^* \tag{2.37}$$

Dc voltage droop controller has the dc voltage vs power characteristic line as shown in Fig. 2.21.

The slope of dc droop characteristic can be given interims of the dc voltage response (R_{DC}) as in Fig. 2.21(b) or in terms of the dc voltage droop constant (ρ_{DC}) as in Fig. 2.21(c). The droop constant ρ_{DC} is used together with voltage and power measured in per-units. The relation between these two constants is given by

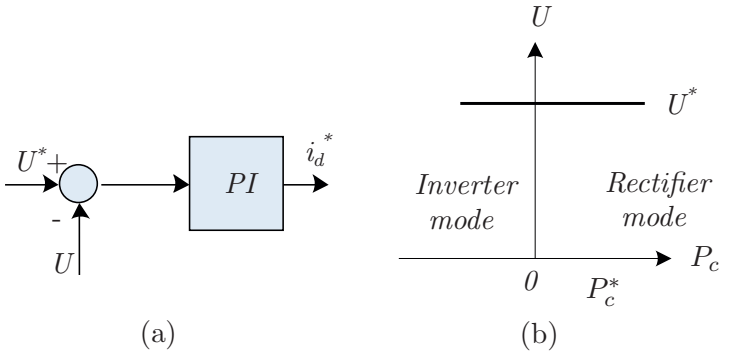


Figure 2.20: Constant dc voltage controller: (a) control schematic (b) dc voltage characteristics

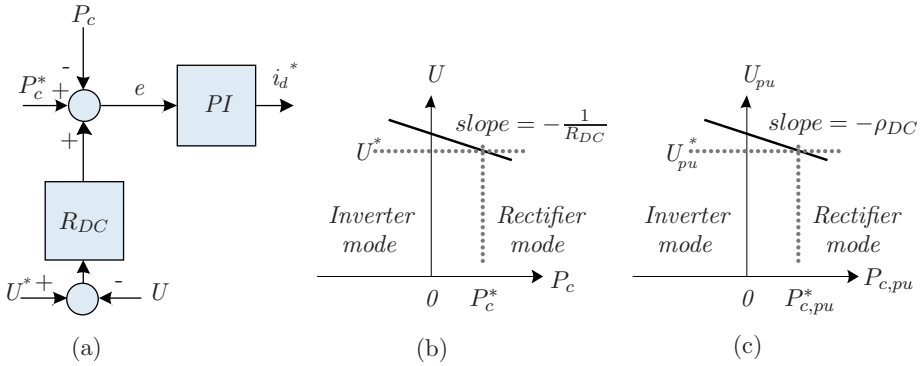


Figure 2.21: Dc voltage droop controller: (a) control schematic (b) dc voltage characteristics (in physical units) (c) dc voltage characteristics (in per-unit)

$$R_{DC} = -\frac{P_{cN}}{U_N \rho_{DC}} \tag{2.38}$$

where P_{cN} and U_N refer to the rated power capacity of the VSC-HVDC terminal and its rated operating dc voltage.

Assuming proportional + integral (PI) control is used, the steady-state error signal of the dc droop controller e equals zero, hence we get the following equations:

$$P_c^* - P_c + R_{DC}\,(U^* - U) = e = 0 \tag{2.39}$$

$$P_{c,pu}^* - P_{c,pu} + \frac{1}{\rho_{DC}}\left(U_{pu}^* - U_{pu}\right) = e = 0 \tag{2.40}$$

The subscript pu in Fig. 2.21(c) and (2.40) refer to per-unit quantities.
The steady-state relations of all the three possible control modes discussed above can indeed be represented by the droop equation (2.39). For constant power control mode the dc voltage response (R_{DC}) is zero (or $\rho_{DC} = \infty$). Constant dc voltage control on the other hand can be represented by a droop constant(ρ_{DC}) of zero (or $R_{DC} = \infty$).

2.5 Operation of Two-terminal VSC-HVDC Transmission

In section 2.3.2, the basics of inner and outer controllers were discussed. Active power controller and dc voltage controller were studied without referring to the interaction of the VSC with other power injecting nodes connected to the same dc circuit. In this section we will analyze the interaction of the various possible control configurations of a two terminal VSC-HVDC. Analysis of the interactions of two terminals gives substantial information on the characteristics of a multi-terminal VSC-HVDC employing various control configurations.
In Fig. 2.22 a two-terminal VSC-HVDC link is shown. A steady-state power flow in the direction of left to right is assumed. Hence the converter on the left side of the HVDC line operates in rectifier mode (i.e. power sending terminal or source terminal) while the converter on the right side operates in inverter mode (i.e. power receiving terminal or load terminal).

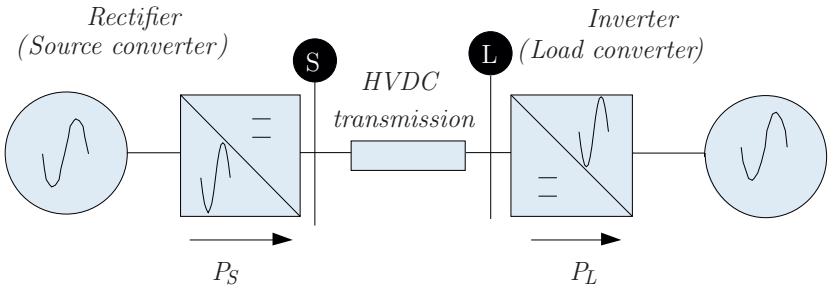


Figure 2.22: Two terminal VSC-HVDC link

In section 2.4 it was discussed that there are three possible types of control modes for operating a single VSC-HVDC terminal. This means that for a two-terminal VSC-HVDC system there will be $3 \times 3 = 9$ possible control configurations. These are listed in Table 2.2.

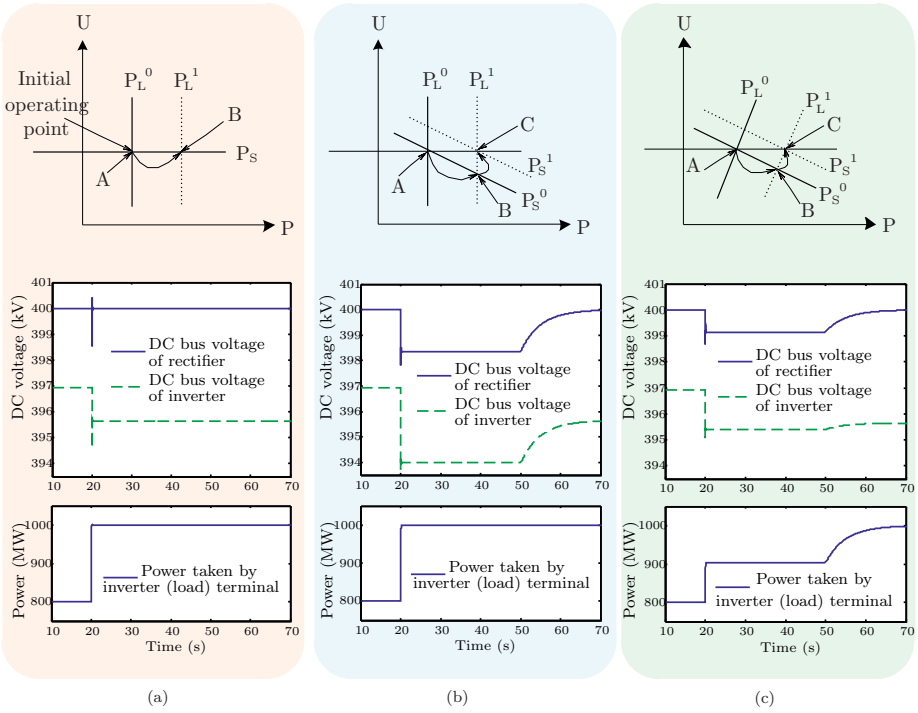
Table 2.2: Various control configurations for two-terminal VSC-HVDC

	Control modes		
No.	Rectifier	Inverter	Remarks
1	Constant power	Constant power	Not viable
2	Constant power	dc droop	Viable but with risk of dc over voltage
3	Constant power	Constant dc voltage	Viable but with risk of dc over voltage
4	dc droop	Constant power	Good performance, Power flow control by inverter
5	dc droop	dc droop	Good performance, Power flow control by both
6	dc droop	Constant dc voltage	Ok, Power flow control by rectifier
7	Constant dc voltage	Constant power	Good performance, Power flow control by inverter
8	Constant dc voltage	dc droop	Ok, power flow control by inverter
9	Constant dc voltage	Constant dc voltage	Not viable

From the nine different control configurations of a two-terminal VSC-HVDC system, two of them, i.e. no. 1 and 9 in Table 2.2, are not viable options since these control configurations do not result in a stable and fully controllable steady-state operation. All the rest of the control configurations, i.e. no. 2 to 8, result in a stable steady-state operation of the system. Despite the stable steady-state operation, control configurations 2 and 3 incur the risk of dc over voltage in some circumstances. This happens when the inverter terminal fails to take power from the dc circuit while the rectifier terminal continues to inject power into the dc circuit. This type of situation may arise from ac fault occurring on the ac side of the inverter, from failure of the inverter itself or from open circuit fault of the dc transmission line linking the two converter stations. dc over voltage caused by such events can be averted by employing dc voltage control at the rectifier side of the HVDC transmission system.

Hence, for two terminal VSC-HVDC system, the control configurations from 4 to 8 in the list of Table 2.2 are recommended.
A VSC-HVDC terminal connected to passive grid is essentially a constant power terminal when observed from the dc-bus side. This is because the power flow via such converter station is determined by the loads connected in the passive ac grid and is independent of the dc-bus voltage under normal circumstances. As it was discussed in section 2.3.1, a passive grid connected VSC-HVDC is equipped with ac voltage controller which enables it to maintain the ac voltage at PCC constant regardless of any dc voltage variations. It should also be noted that the use of the term 'constant power' in the context of this discussion refers to the independence of power with respect to dc-bus voltage and does not imply the invariance of power flow with respect to time. If the VSC-HVDC is used to transfer power in both directions at various times, the control configuration may need to be changed depending on the direction of the power flow to avoid possibility of dc over voltage condition.
Control configuration 5 in Table 2.2 offers an additional advantage of keeping the same controller for all operating conditions. This is because both terminals have the same type of controllers, namely dc voltage droop control, which always results in a stable operation without the risk of dc over voltage. The disadvantage is that power reference and dc voltage reference must be adjusted carefully on both converter terminals in order to achieve the desired power flow level. For all the rest of control configurations (four, six seven and eight in Table 2.2) power flow is controlled exclusively by one terminal and the other one compensates for the power deficit/surplus in the dc circuit - making it a relatively straight forward power flow control approach.
To compare the performances of different control configurations, we look at the responses of three selected control configurations, i.e. no. four, five and seven in Table 2.2. Consider that in Fig. 2.22, the initial steady-state power flow is 800 MW from left to right. Now it is desired to increase the power flow to 1000 MW; hence an increment of 200 MW. This is achieved in different ways depending on the type of control configuration employed. Fig. 2.23 summarizes the comparison of the responses of the three control configurations and the transitions involved to achieve the required increment in power flow.

In Fig. 2.23 the rectifier and inverter characteristic lines are shown by P_S (source power) and P_L (load power) respectively. Subscripts 0 and 1 are used to show the initial and final characteristic lines. Point A refers to the initial operating point, which is the intersection point of the initial dc characteristic lines of the rectifier and inverter terminals. The power reference of the inverter is changed by $\Delta P_L^* = 200\,\text{MW}$ which results in the inverter characteristic line moving from P_L^0 to P_L^1. This event results in a transition of the steady-state operating point from A to B in Fig. 2.23. The change of the inverter power reference results in different types of responses for



(a) (b) (c)

Figure 2.23: Responses of different control configurations: (a) corresponds to config. eight (b) corresponds to config. four and (c) corresponds to config. five in Table 2.2

the various control configurations. In the first case (Fig. 2.23 (a)), where the rectifier and inverter operate in constant dc voltage and constant power control mode respectively, the desired change in power flow is achieved in one step simply by applying the change in power reference ΔP_L^* to inverter terminal. This is evident from Fig. 2.23 (a-bottom) where the dc-bus voltage of the rectifier is restored instantaneously while the power flow into the inverter increases from 800 MW to 1000 MW, as it was desired. Similarly in Fig. 2.23(b), where the rectifier and inverter operate in dc voltage droop and constant power control mode respectively, the desired change in power flow is achieved by simply applying the relevant change in power reference to the inverter terminal. This however, results in decrement of the dc voltage as depicted by Fig. 2.23(b-top).
If restoration of the dc-bus voltage to the initial level is needed, this is achieved by changing the dc voltage reference and/or the power reference of the droop controller

of the rectifier. This action results in moving of the rectifier dc voltage characteristic line from P_S^0 to P_S^1. Consequently the steady-state operating point moves from point B to C. It can be observed in Fig. 2.23 (b) that the desired change in power is achieved by changing the power reference of the inverter whereas dc-bus voltage is restored by adjusting the rectifier dc voltage references.
The responses shown in Fig. 2.23 (c) correspond to the control configuration where both the rectifier and inverter are assigned to operate in dc voltage droop control mode. Due to the use of different dc voltage droop constants, the slopes of the two dc voltage characteristic lines (i.e. P_S and P_L in Fig. 2.23 (c)-top) are different. For this type of control configuration, the mere change of the inverter power reference alone does not result in the desired change in power flow. This is depicted by the increment in power flow from the initial level of 800 MW to around 915 MW which is considerably lower than the desired level of 1000 MW. the desired power flow level is achieved by adjusting the rectifier dc characteristic line from B to C as shown in Fig. 2.23 (c). This implies that additional control action is necessary to achieve the desired level of power flow.
In all the three cases of responses shown in Fig. 2.23, all transitions (i.e. A to B and B to C) are caused by change in power and/or dc voltage references of the converter controller (as active grid connection has been used for both terminals where power flow can be controlled actively). The shift in dc voltage characteristic line however can also be caused by uncontrolled events such as outage of ac load connected to the inverter (if it is connected to passive ac grid), outage of converter or simply due to an outage of the dc line. The response of the VSC-HVDC system to such events (and hence the transition from A to B) will be referred to as primary control response, or simply primary control. This is analogous to the primary control in ac grids [45]. Primary control in both ac and dc grids is the response of the system to power imbalance caused by unexpected events such as faults, outages and load changes. In ac grids primary control response almost always involves a steady-state change in system frequency. If the magnitude of the steady-state change in frequency is above a certain threshold, generation will be adjusted at one or more power stations so as to restore the operating ac frequency to the nominal level. This is usually referred as secondary control since it occurs some time after the action of primary control. The time delay in the example case of Fig. 2.23 is half minute (this is selected arbitrarily in the example scenario). The purpose of secondary control is both to restore system frequency to nominal level and also to free up some of the primary reserves already actuated by change in frequency. Similarly, in dc grid which employs dc voltage droop control a primary control always is accompanied by a steady-state change in dc voltage. Hence dc grids also need secondary control for restoring the dc voltage and for achieving the desired level of power flow at specific converter terminals. Like in ac grids, the secondary control in dc grid should act slowly in order to avoid too fast changes in power flow and possible adverse interaction with ac grid. This is

depicted in the time plots of Fig. 2.23(b) and Fig. 2.23(c).

2.6 Frequency Support of AC Grid by VSC-HVDC Link

In [78] primary frequency response enhancement by use of LCC-HVDC link has been proposed. Moreover in [42] primary frequency control using VSC based MTDC has been proposed. The method, however, requires fast communication of system between the various dc terminals and a centralized control unit. Due to their high degree of controllability, VSC-HVDC terminals can be utilized to provide primary frequency support to ac grids [81]. A VSC-HVDC connected to an active ac grid can indeed be considered as a virtual synchronous generator since the power injection into the ac grid is fully controllable, which makes it easy to employ frequency droop control. Fig. 2.24 (a) and (b) show implementation of frequency droop control for VSC-HVDC equipped with constant power control and dc voltage droop control respectively. The method proposed here is entirely dependent upon locally measured signals and does not need communication between various dc terminals.

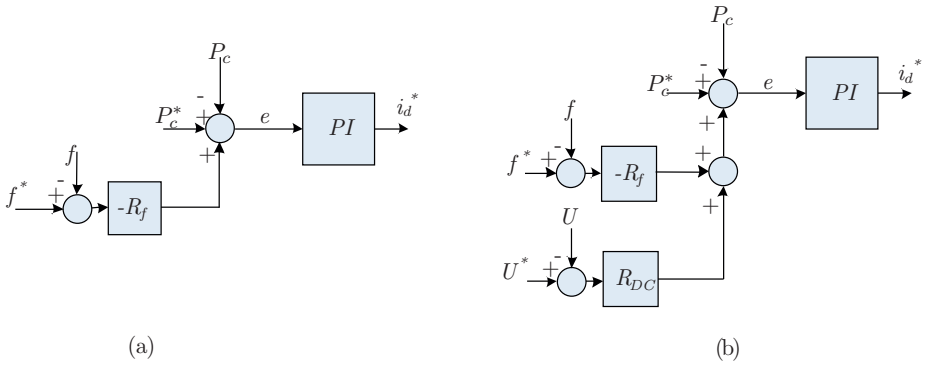


Figure 2.24: Frequency droop control implementation on VSC-HVDC terminal with : (a) constant power control (b) dc voltage droop control

In Fig. 2.24 the symbols P_c^*, f^* and U^* refer to power reference, frequency reference and dc voltage reference respectively. R_{DC} and R_f refer to dc voltage response and frequency response of the VSC-HVDC terminal. i_d^* is the reference to the active current controller discussed in section 2.3.2. Note that the two droop controls in Fig. 2.24(b) have opposite sign due to the fact that frequency decrement results in power flow increment from dc-bus to ac grid while the dc voltage decrement results in power flow increment in the opposite direction.

The control configuration in Fig. 2.24(b) can represent the steady-state behavior of the various possible control configurations. Fig. 2.24(a) for example can be represented by dc voltage response equal to zero ($R_{DC} = 0$). In the linear region of the controller shown in Fig. 2.24(b) the steady-state control error equals zero $e = 0$. This is mathematically given by

$$(P_c^* - P_c) - R_f\,(f^* - f) + R_{DC}\,(U^* - U) = 0 \tag{2.41}$$

Hence the power injection by the VSC-HVDC terminal (P_c) becomes as follows:

$$P_c = P_c^* - R_f\,(f^* - f) + R_{DC}\,(U^* - U) \tag{2.42}$$

From equation (2.42) it is clear that infinitely many combinations of the references P_c^*, f^* and U^* can give the same level of power transfer (P_c). This apparently poses a challenge of precise power flow control since three parameters affect the resulting power flow control. On the other hand by eliminating the frequency control error ($f^* - f$) and dc voltage control error ($U^* - U$), precise power flow control can be achieved. Each of the frequency reference f^* is normally a constant universally applied for all generator and converter units in the ac grid. The dc voltage reference however concerns the dc-bus of each individual VSC-HVDC station and hence should be selected carefully so as to avoid any dc voltage control error resulting in power injection levels different from the desired ones (this is due to the unequal dc-bus voltages caused by power flow inside the dc grid). How this can be done for a MTDC will be discussed in the next chapter.
Grid frequency support by VSC-HVDC link enables exchange of primary reserves between asynchronous ac grids. To demonstrate this with an example, let us consider the two-terminal VSC-HVDC shown in Fig. 2.25. The ac grids in the figure are characterized by generation capacity (P_{gN}), frequency droop constant (ρ_G) and operating frequency (f). The converters are specified by rated power (P_{cN}), rated dc voltage (U_N), dc voltage droop constant (ρ_{DC}), and frequency droop constant (f_{DC}).

The two asynchronous ac grids in Fig. 2.25 have rated generation capacities of 4 GW and 2.5 GW respectively. Frequency droop constant of 0.04 has been assigned for both ac grids as well as for both VSC-HVDC terminals. The dc voltage droop constant is assigned to be 0.05 for both converters. The VSC-HVDC transmission has rated operating dc voltage of 400 kV and rated power capacity of 1000 MW. The initial steady-state power flow via the dc transmission is 750 MW. Moreover, the initial local loads of the two ac grids are 2.4 GW and 2 GW respectively. The dc line has a resistance of 3.2 Ω. When the local load of either of the two ac grids

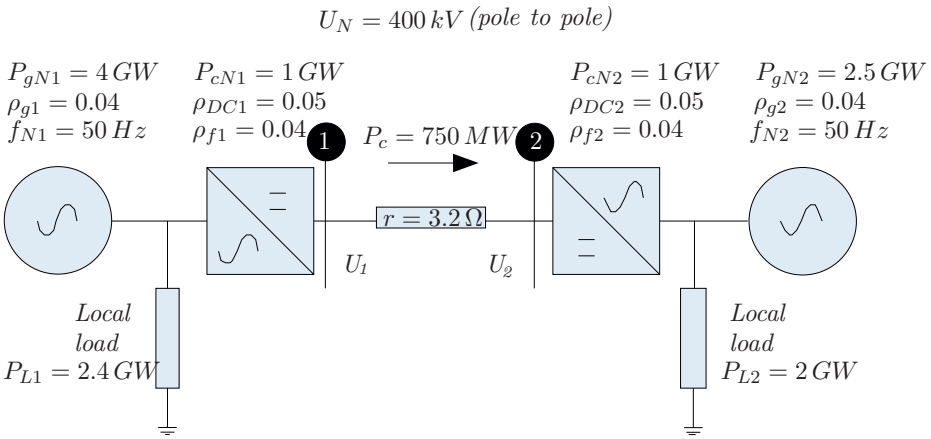


Figure 2.25: VSC-HVDC link with bi-directional grid frequency support

is increased, the ac frequency drops and local generation increases as a result. In the presence of frequency droop control within the converter controllers, there will be additional power transfer from the dc link which results in improvement of the frequency response. This can be demonstrated with two simulation cases of the system in Fig. 2.25. In the first simulation case the two converters are equipped with dc voltage droop control but not with frequency droop control. At $t = 100\,\text{s}$ the local load in ac grid-2 is increased from 2 GW to 2.2 GW, - a load change of 200 MW (equivalent to 8 % of the rated ac grid generation capacity). This is followed by decrement in the steady-state frequency. At $t = 150\,\text{s}$ the local load in ac grid-1 is increased from 2.5 GW to 2.9 GW - a load change of 400 MW (10% of rated grid generation capacity). In Fig. 2.26 the responses of the two ac grids to the load increments are shown.

As one might expect, in this case of simulation the power transfer via the dc link is not affected by the changing loads in ac grids 1 and 2. On the other hand, when frequency droop control is employed for the two VSC-HVDC terminals, the frequency responses of both ac grids improve. This can be seen from time plots of Fig. 2.27, which corresponds to the simulation case where both terminals of the HVDC link employ frequency droop control along side with dc voltage droop control. Especially the improvement in the frequency dips for the load increments is easily observable from the time plots of the second simulation case.

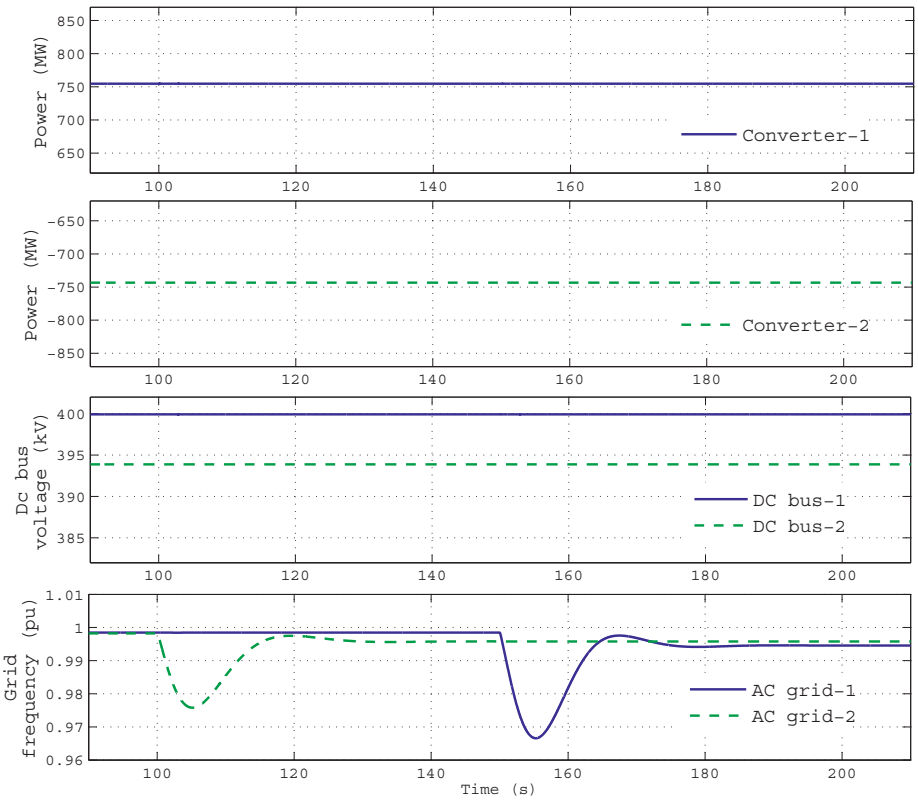


Figure 2.26: Grid frequency responses to load events at 100 s and 100 s in the absence of frequency support by VSC-HVDC link

2.7 Steady-state Interaction of Two terminal VSC-HVDC Connection

From Fig. 2.27 it is noticed that by using both dc voltage droop and frequency droop control at both ends of the dc link, some degree of coupling between the frequencies of the two asynchronous ac grids is achieved. For closer comparison of the two cases, the frequency responses in the presence and absence of frequency support by the dc link are shown in the plots of Fig. 2.28. The dynamic frequency responses of the two grids have particularly shown considerable improvement after the use of frequency support by the dc link. This is evidenced by the smaller frequency dips in Fig. 2.28 after the use of frequency droop controllers at both converter terminals.

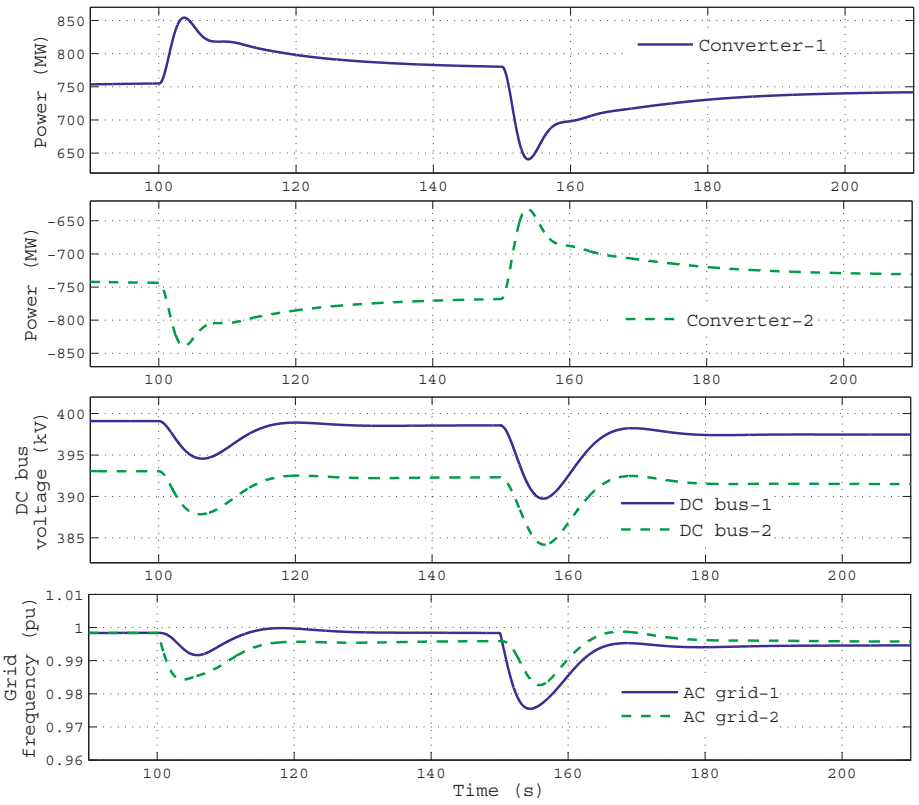


Figure 2.27: Grid frequency responses to load events at 100 s and 100 s in the presence of frequency support by VSC-HVDC link

The differences in the steady-state frequencies however are not observable from the plots due to the large sizes of the of the ac grids in comparison with the converter units. For estimating the steady-state frequency changes, analytical equation can be derived and used. This will be presented in the following discussion.
At steady-state, the power balances for the two ac grids are expressed by

$$\left.\begin{aligned} \Delta P_{L1} &= \Delta P_{g1} - \Delta P_{c1} \\ \Delta P_{L2} &= \Delta P_{g2} - \Delta P_{c2} \end{aligned}\right\} \tag{2.43}$$

where ΔP_{g1} and ΔP_{g2} refer to the changes in generated power inside grid-1 and grid-2 respectively. Similarly ΔP_{L1} and ΔP_{L2} represent the change in load in the respective ac grids. ΔP_{c1} and ΔP_{c2} represent the change in transfered power at the

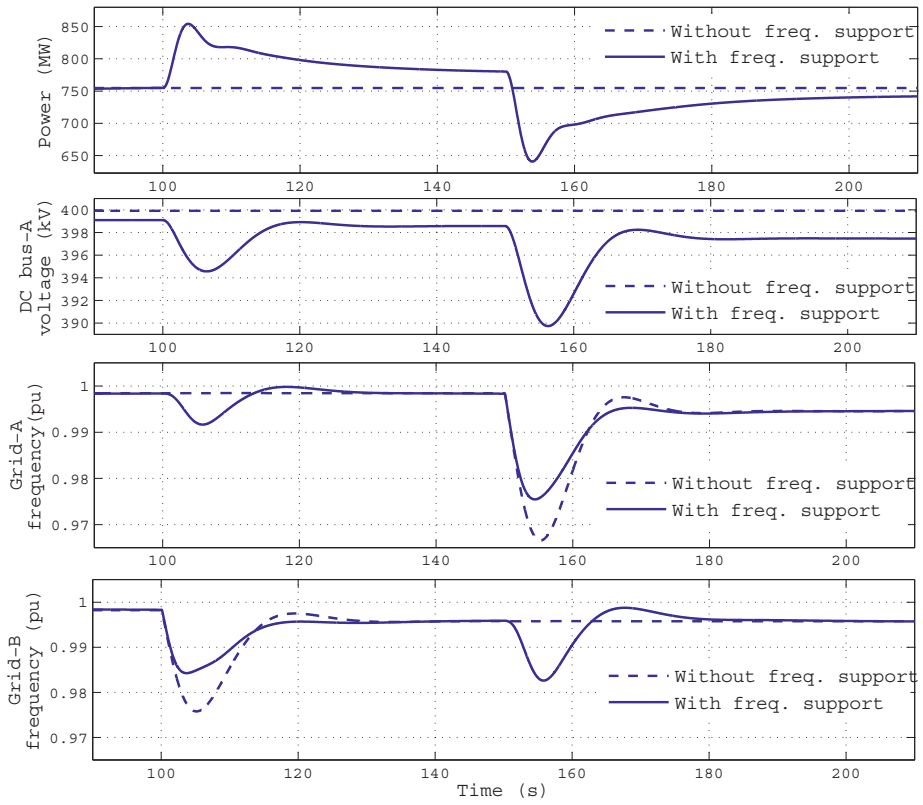


Figure 2.28: Comparison of grid frequency responses in the presence and absence of frequency support by dc link

two VSC-HVDC terminals. The changes in generation are expressed by

$$\left.\begin{aligned}\Delta P_{g1} &= -\frac{P_{gN1}}{\rho_{g1} f_{N1}} \Delta \left(f_1^* - f_1\right) \\ \Delta P_{g2} &= -\frac{P_{gN2}}{\rho_{g2} f_{N2}} \Delta \left(f_2^* - f_2\right)\end{aligned}\right\} \tag{2.44}$$

where P_{gN}, ρ_G and f_N refer to the rated power capacity, frequency droop constant and rated frequency of an ac grid respectively. f^* refers to the frequency reference of the ac grid. Similarly from (2.41) the changes in converter powers at the two terminals are

$$\left.\begin{aligned}\Delta P_{c1} &= -\tfrac{P_{cN1}}{\rho_{f1} f_{N1}}\Delta\left(f_1^* - f_1\right) + \tfrac{P_{cN1}}{\rho_{DC1} U_{N1}}\Delta\left(U_1^* - U_1\right) + \Delta P_1^* \\ \Delta P_{c2} &= -\tfrac{P_{cN2}}{\rho_{f2} f_{N2}}\Delta\left(f_2^* - f_2\right) + \tfrac{P_{cN2}}{\rho_{DC2} U_{N2}}\Delta\left(U_2^* - U_2\right) + \Delta P_2^*\end{aligned}\right\} \tag{2.45}$$

where P_{c1} and P_{c2} refer to the power injection into dc-bus by the two converter stations. Here we are more interested in the impact of abrupt changes in ac load and hence we assume that all references remain constant. Moreover we consider per-unit values for the frequencies (f_{pu}) and dc voltages (U_{pu}) while keeping the use of MW for power variables. Hence from (2.44) and (2.45) and substituting (2.38) we get

$$\left.\begin{aligned}\Delta P_{g1} &= -\tfrac{P_{gN1}}{\rho_{g1}}\Delta f_{pu1} \\ \Delta P_{g2} &= -\tfrac{P_{gN2}}{\rho_{g2}}\Delta f_{pu2}\end{aligned}\right\} \tag{2.46}$$

$$\left.\begin{aligned}\Delta P_{c1} &= -\tfrac{P_{cN1}}{\rho_{f1}}\Delta f_{pu1} + \tfrac{P_{cN1}}{\rho_{DC1}}\Delta U_{pu1} \\ \Delta P_{c2} &= -\tfrac{P_{cN2}}{\rho_{f2}}\Delta f_{pu2} + \tfrac{P_{cN2}}{\rho_{DC2}}\Delta U_{pu2}\end{aligned}\right\} \tag{2.47}$$

To simplify the analysis, we ignore the dc line losses and hence $\Delta P_{c1} = -\Delta P_{c2} = -\Delta P_c$ and $\Delta U_{pu1} = \Delta U_{pu2} = \Delta U_{pu}$. In addition, the rated converter power capacity of the two VSC-HVDC terminals are equal ($P_{cN1} = P_{cN2} = P_{cN}$). This further simplifies (2.47) into

$$\left.\begin{aligned}\Delta P_c &= P_{cN}\left(\tfrac{\Delta f_{pu1}}{\rho_{f1}} - \tfrac{\Delta U_{pu}}{\rho_{DC1}}\right) \\ &= -P_{cN}\left(\tfrac{\Delta f_{pu2}}{\rho_{f2}} - \tfrac{\Delta U_{pu}}{\rho_{DC2}}\right)\end{aligned}\right\} \tag{2.48}$$

From (2.48) the dc voltage in terms of the ac grid frequencies is expressed as

$$\left.\begin{aligned}\Delta U_{pu} &= \underbrace{\left(\frac{\rho_{DC1}\rho_{DC2}}{\rho_{DC1} + \rho_{DC2}}\right)}_{k}\left(\tfrac{\Delta f_{pu1}}{\rho_{f1}} + \tfrac{\Delta f_{pu2}}{\rho_{f2}}\right) \\ &= \begin{bmatrix} \frac{k}{\rho_{f1}} & \frac{k}{\rho_{f2}} \end{bmatrix}\begin{bmatrix} \Delta f_{pu1} \\ \Delta f_{pu2} \end{bmatrix}\end{aligned}\right\} \tag{2.49}$$

Substituting (2.48) and (2.49) into (2.43) we get the equation

$$\begin{bmatrix} \Delta P_{L1} \\ \Delta P_{L2} \end{bmatrix} = - \begin{bmatrix} \frac{P_{gN1}}{\rho_{g1}} + \frac{P_{cN}}{\rho_{f1}} \left(\frac{\rho_{DC2}}{\rho_{DC1}+\rho_{DC2}} \right) & -\frac{P_{cN}}{\rho_{f2}} \left(\frac{\rho_{DC2}}{\rho_{DC1}+\rho_{DC2}} \right) \\ -\frac{P_{cN}}{\rho_{f1}} \left(\frac{\rho_{DC2}}{\rho_{DC1}+\rho_{DC2}} \right) & \left(\frac{P_{gN2}}{\rho_{g2}} + \frac{P_{cN}}{\rho_{f2}} \frac{\rho_{DC1}}{\rho_{DC1}+\rho_{DC2}} \right) \end{bmatrix} \begin{bmatrix} \Delta f_{pu1} \\ \Delta f_{pu2} \end{bmatrix} \tag{2.50}$$

Hence the relationship between the load changes and resulting frequency changes can be computed by

$$\begin{bmatrix} \Delta f_{pu1} \\ \Delta f_{pu2} \end{bmatrix} = - \begin{bmatrix} \frac{P_{gN1}}{\rho_{g1}} + \frac{P_{cN}}{\rho_{f1}} \left(\frac{\rho_{DC2}}{\rho_{DC1}+\rho_{DC2}} \right) & -\frac{P_{cN}}{\rho_{f2}} \left(\frac{\rho_{DC2}}{\rho_{DC1}+\rho_{DC2}} \right) \\ -\frac{P_{cN}}{\rho_{f1}} \left(\frac{\rho_{DC2}}{\rho_{DC1}+\rho_{DC2}} \right) & \left(\frac{P_{gN2}}{\rho_{g2}} + \frac{P_{cN}}{\rho_{f2}} \frac{\rho_{DC1}}{\rho_{DC1}+\rho_{DC2}} \right) \end{bmatrix}^{-1} \begin{bmatrix} \Delta P_{L1} \\ \Delta P_{L2} \end{bmatrix} \tag{2.51}$$

For the dc transmission system shown in Fig. 2.25, the control parameters used are listed as follows:

$$\left.\begin{array}{l} P_{cN} = 1000\,\text{MW} \\ P_{gN1} = 4000\,\text{MW} \\ P_{gN2} = 2500\,\text{MW} \\ \rho_{g1} = \rho_{g2} = 0.04 \\ \rho_{DC1} = \rho_{DC2} = 0.05 \\ \rho_{f1} = \rho_{f2} = 0.04 \end{array}\right\} \tag{2.52}$$

Substituting the parameters from (2.52) into (2.51), we get

$$\left.\begin{array}{l} \begin{bmatrix} \Delta f_{pu1} \\ \Delta f_{pu2} \end{bmatrix} = \left(10^4 \begin{pmatrix} -11.2500 & 1.2500 \\ 1.2500 & -7.5000 \end{pmatrix} \right)^{-1} \begin{bmatrix} \Delta P_{L1} \\ \Delta P_{L2} \end{bmatrix} \\ \qquad = 10^{-4} \begin{pmatrix} -0.0906 & 0.0151 \\ 0.0151 & -0.1358 \end{pmatrix} \begin{bmatrix} \Delta P_{L1} \\ \Delta P_{L2} \end{bmatrix} \end{array}\right\} \tag{2.53}$$

From equations (2.49) and (2.53) the dc-bus voltage change for the example case becomes as

$$\Delta U_{pu} = -10^{-4} \times \begin{bmatrix} 1.321 & 1.887 \end{bmatrix} \begin{bmatrix} \Delta P_{L1} \\ \Delta P_{L2} \end{bmatrix} \tag{2.54}$$

For a load increment of 200 MW inside ac grid-2, equation (2.53) predicts frequency changes of -0.3×10^{-3} pu for grid-1 and -2.7×10^{-3} pu for grid-2. The corresponding frequency changes obtained from the simulation were -0.2×10^{-3} pu and -2.2×10^{-3} pu respectively. The differences between the predicted values and simulation results arise due to the fact that unequal variations of dc-bus voltages, caused

by line resistances, have been neglected. Besides, the converter and dc line losses which were not accounted in the analysis have some contributions to the deviations. The observed changes in dc-bus voltage were -1.3×10^{-3} pu for terminal-1 and -1.7×10^{-3} pu for terminal-2 respectively, compared to -1.9×10^{-3} pu which is the estimated dc voltage change according to (2.54). The set of analytical equations derived above, though not very accurate, provides a numerical approach for analyzing the interaction of the two ac grids connected due to primary reserves exchanges via the VSC-HVDC link. In chapter three an accurate analytical expression for generalized ac/dc connection topology will be discussed.

2.8 Frequency Support of AC Grid by HVDC Connected Wind Farm

In section 2.3.1 it was mentioned that passive grid connected VSC-HVDC link does not have direct control over power flow but rather responds passively to the power demand of (or power injection from) the ac grid. It however controls the ac voltage magnitude and frequency to which other smaller converters in the ac grid (if there are any) have to synchronize for normal operation. VSC-HVDC connected to a wind farm falls in the passive grid connection category since the converter station does not directly determine the amount of power flow. As a result, the converter can not directly participate in ac or dc grid support by using the control method discussed in the previous section. It can however change the ac frequency of the wind farm in response to the dc-bus voltage variations. The frequency variations in the wind farm can in turn be used to invoke increments in generated power by individual turbine-converter units, given that there is plenty of wind power which allow increased power production. This type of HVDC control has been described in [82],[16],[77]. Such type of control strategy can be implemented as shown in Fig. 2.29.

In Fig. 2.29 the converter on the right side of the HVDC link employs constant dc voltage control mode supplemented by frequency droop controller. f_g^* and f_g refer to the nominal frequency and measured frequency of the main grid respectively. The converter station on the left side controls the operating wind farm ac frequency based upon the dc voltage error $(U_1 - U_{DC}^*)$ and the nominal wind farm frequency (f_w^*). In the case of two-terminal VSC-HVDC connection, the effect of the dc line resistance can easily be offset by adding a feed forward element from the measured power flow (P_1). This is shown with the dashed line in Fig. 2.29. Individual wind turbine-converter units measure the wind farm frequency (f_w) and generate the mechanical (turbine) power reference (P_m^*) based on the nominal power reference (P_w^*) and the frequency error signal $(f_w^* - f_w)$.

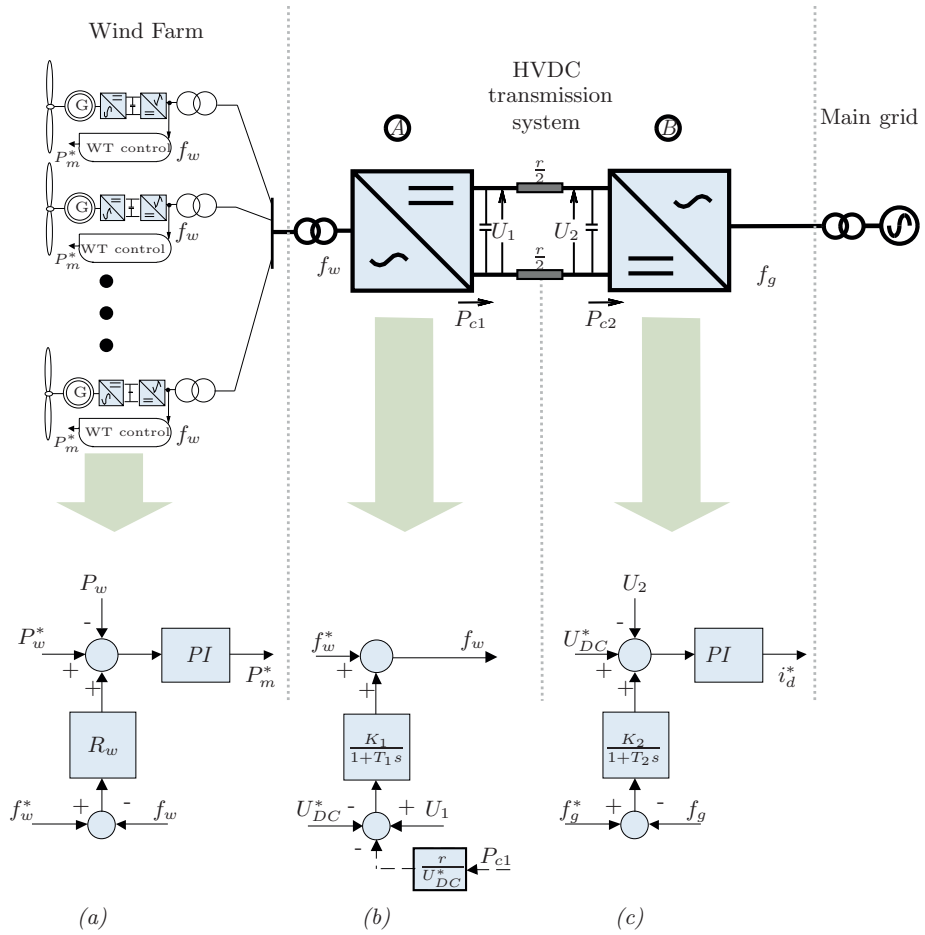


Figure 2.29: VSC-HVDC connected wind farm: (a) wind turbine-converter control (b) wind farm side VSC-HVDC terminal control (c) main grid side VSC-HVDC terminal control

From Fig. 2.29 the steady-state relationship between f_w and f_g can be described as

$$f_w = f_w^* + K_1 K_2 \left(f_g - f_g^* \right) \tag{2.55}$$

From (2.55) we find

$$\Delta f_w = K_1 K_2 \Delta f_g \tag{2.56}$$

Table 2.3: Some of the parameters used in the simulation model

Generation capacity of the main grid	1 GW
Generation capacity of the wind farm	3 MW × 100 = 300 MW
Rated frequency of the main grid	50 Hz
Rated frequency of the wind farm	50 Hz
Wind speed	12 m/s
R_w	25 MW/Hz
$\frac{K_1}{1+T_1 s}$	$\frac{1}{1+5s}$
$\frac{K_2}{1+T_2 s}$	$\frac{1}{1+5s}$

For $K_1 = K_2 = 1$ the steady-state frequency variation of the wind farm equals the corresponding frequency variation at the main grid. To check the viability of such approach we will look at the responses of a simulation model of Fig. 2.29. In Table 2.3 some of the parameters used in the simulation model are listed.

Initial power flow is 180 MW from the wind farm to the main grid. At $t = 68$ s a load of 25 MW is inserted in the main grid. The simulation results are shown in the plot of Fig. 2.30.

As it can be observed from the simulation results, the load insertion in the main grid results in frequency decrement which is followed by dc voltage reduction at the HVDC link. This in turn is reflected in the wind farm frequency and the wind turbines generate more power as a result. The main grid frequency and wind farm frequency are compared in Fig. 2.31. It is clear from Fig. 2.31 that the wind farm frequency is able to follow the main grid frequency but only with considerable time constant (A time constant of 5 s has been used for frequency droop control at converter-2 and for the wind farm frequency control at converter-1). The response of the main grid in the presence and absence of frequency support from the wind farm is shown in Fig. 2.32. It is observed from Fig. 2.32 that both the dynamic response (i.e. in the first few seconds) and steady-state response of the main grid frequency are enhanced by the frequency support of the windfarm.

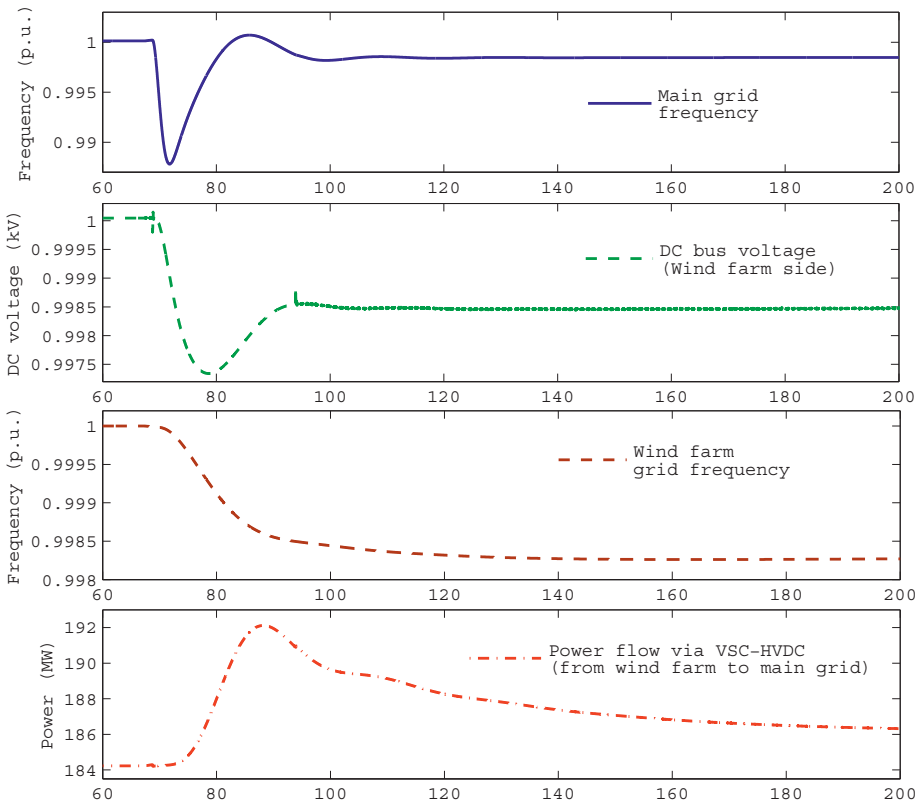


Figure 2.30: Response of VSC-HVDC connected wind farm to load insertion in the main grid

2.9 Chapter Summary

In this chapter various existing control methods of VSC-HVDC terminal have been studied. Two types of VSC-HVDC connections - namely: active grid connected VSC-HVDC link and passive grid connected VSC-HVDC link - have been discussed. It is pointed out that inner current loop is fundamental to any control of active grid connected VSC-HVDC link. Three possible control modes of VSC-HVDC terminal have been discussed. These are constant power control mode, constant dc voltage control mode and dc voltage droop control mode. A control strategy for primary reserves exchange between two asynchronous ac grids has been proposed. The pro-

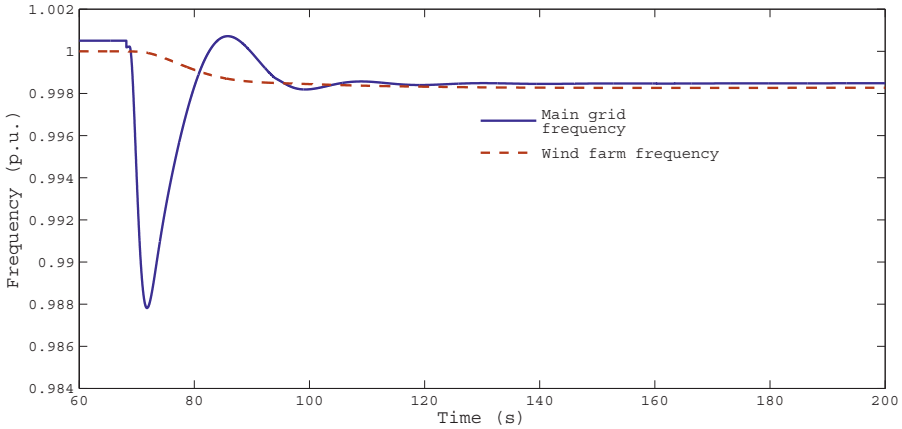


Figure 2.31: Comparison of the main grid frequency and wind farm frequency

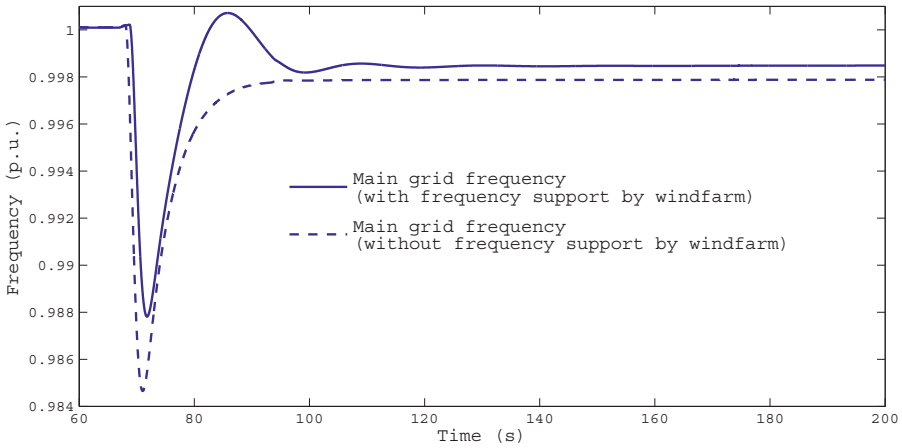


Figure 2.32: Comparison of the main grid frequency response with and without frequency support from windfarm

posed control employs both dc voltage droop and frequency droop control for each VSC-HVDC terminal. The control method depends entirely on local measurements and does not require fast communication between the different converter terminals connected by the dc grid or between the asynchronous ac grids.

3 OPERATION OF MTDC AND STEADY STATE ANALYSIS

In the previous chapter the various types of VSC control configurations that can be used in MTDC transmission system have been discussed. In this chapter the interplay of the VSCs during steady-state operation of MTDC will be discussed. The first section of this chapter deals with the different types of MTDC control configurations. This is followed by section 3.2 which discusses precise control of power flow in MTDC. Thereafter the impact of dc line resistances on primary dc power balancing of MTDC will follow in sections 3.4 and 3.3. steady-state interaction of ac/dc systems will be discussed in section 3.5.

3.1 Valid Control Configurations for Operation of MTDC

In section 2.5 it was discussed that at least one of the two converters must have dc voltage regulation mechanism for normal operation of a point-to-point VSC-HVDC connection. Similarly, in a multi-terminal VSC-HVDC configuration there must be dc voltage regulation for normal operation of the system. As described in the previous chapter there are two options for dc voltage control of a single VSC station; namely: constant dc voltage control and dc voltage droop control. It was also mentioned in section 2.5 that stable operation can not be achieved if both converters of the two-terminal VSC-HVDC are assigned to constant dc voltage control mode. The same condition applies to multi-terminal VSC-HVDC, i.e. there must not be more than one converter station in the dc grid assigned to constant dc voltage control mode. (If there are two converters with constant dc voltage control, there will be hunting phenomena, analogous to frequency hunting in ac grids in the presence of multiple synchronous generators with fixed frequency control). Taking the constraints mentioned above, we get three possible control modes of MTDC; namely: master-slave control, dc voltage droop control and master-slave with dc droop. Each of these are explained below.

1. *Master-slave control*: There is only one converter in the dc grid which is configured to constant dc voltage mode (This may also be dc voltage droop mode though not common). This terminal is called master terminal. All the others terminals in the dc grid are configured to constant power mode (called slave terminals). Power flow balance is maintained entirely by the master terminal. Outage of the master terminal will definitely lead to dc over voltage or under voltage problem and subsequently to outage of the entire dc grid. In addition, the master terminal may need to have considerably large power rating in order to accommodate all possible amounts

of power unbalance that may occur in the dc grid. This type of control has been explained in numerous research works [87],[36],[59],[75]. Due to lack of N-1 security for dc voltage regulation, the master-slave control configuration is not recommended for operation of MTDC. A modified version of this controller, called voltage margin control, has been proposed to tackle the problem of N-1 security by various authors [85],[86],[48],[20]. The proposed control scheme, however, has two drawbacks. On one hand, it is complex and involves several control parameters to be assigned. On the other hand it can result in large, abrupt transitions of power flow levels as dc voltage level goes out of the voltage margin at a specific operation.

2. *DC droop control*: There are two or more converters in the dc grid equipped with dc voltage droop controller. The rest of the terminals operate in constant power control mode. Converters with dc voltage droop control share the duty of instantaneous power balancing in the dc grid. Outage of one terminal is tolerated as long as the remaining droop controlled terminals have enough capacity to compensate for the power unbalance in the dc grid caused by the outage. This is analogous to frequency droop control of a multi-machine ac grid system. In both cases, the droop control scheme enables the provision of N-1 security. Moreover, large range of power fluctuations in the dc grid can be accommodated by this control method due to the aggregation of dc voltage responses from individual droop controlled converters. This type of control has been studied in several works [71],[74],[73],[55],[43],[15],[79],[90],[57],[37],[75].

3. *Master-slave with droop control*: The dc grid has one converter with constant dc voltage control (i.e. the master terminal) and one or more converters with dc voltage droop control. During normal operation, power balance is maintained entirely by the master terminal. If the outage of the master terminal occurs, the other terminals equipped with dc voltage droop control will take over the duty of dc voltage regulation (and hence the duty of primary power balancing). This type of MTDC control is explained in [19] and partially described in [21].

Comparing the merits of the three MTDC control configurations listed above (1-3), the second and third ones (i.e. dc droop control and master-slave with dc droop control) are preferable for operation of MTDC.
Dc voltage regulation by use of multiple dc terminals equipped with integral dc voltage controllers has been proposed in [34],[35]. This control approach, however, poses a challenge for appropriate sharing of power injection among the participating dc terminals and also may cause instability problems. Hence, this type of MTDC control will not be discussed in this thesis.

3.2 Precise Control of Power Flow in MTDC

In the discussion of section 3.1, it has been argued that dc voltage droop control is indispensable for secure operation of MTDC. The similarities of dc voltage droop control in dc and frequency droop control in ac grid has also been emphasized. There are, however, differences that need to be analyzed and taken into account.
In the absence of dc line losses (and associated dc line voltage drops), dc voltage droop control indeed becomes exactly analogous to frequency droop control in multi-machine ac grids. Under such condition the dc voltage is the same throughout the entire dc grid, just like frequency is in ac grids. In a real dc transmission system, however, there will always be, due to non-zero line resistances, differences in dc-bus voltages. Indeed, whenever there is a non-zero power flow in the dc grid, there will always be differences in dc-bus voltages at the various terminals. (The same voltage at all dc-buses in a real dc grid means no current flowing in the dc grid). From the dc grid power flow equations it is possible to demonstrate that a specific power injection pattern is associated with a unique set of dc-bus voltages and vice-versa. Even though the voltage differences between the dc-buses are small in comparison with the nominal voltage of the dc grid, their impact on power flow control is large due to amplification by the large gain of the dc voltage droop controllers (i.e. R_{DC} in Fig. 2.21).
The dc line voltage drops affect power flow in MTDC in two ways. The first one, which will be discussed in this section, is the challenge of precise power flow control in MTDC at steady-state conditions. This problem has been mentioned in [15] & [50]. The second mechanism, which will be discussed in the next section, is related to allocation of primary balancing power due to a sudden change of power flow in the MTDC network caused by outage of a VSC-HVDC terminal, disconnection of a dc line or insertion/rejection of a large ac load connected to a converter.

To understand the challenge of precise power control in MTDC, let us look at the dc voltage versus power (U vs P) characteristic curves of the three types of outer controllers discussed in section 2.4. These are shown in Fig. 3.1.

From Fig. 3.1 (a), it is clear that the power injection into the dc grid by a constant power mode terminal is always the same as the reference P_c^*. Similarly, a VSC-HVDC terminal equipped with integral control of dc-bus voltage (i.e. Fig. 3.1 (b)) will always have the same dc-bus voltage as the reference U^*. The power injection of such a terminal, however, is determined by the net power injection of all other terminals in the dc grid as well as the sum total of the power losses in the dc lines. This is what we refer to as the master terminal. The master terminal (if there is one in the dc grid) provides the net balance of power (deficit/surplus) with in a certain

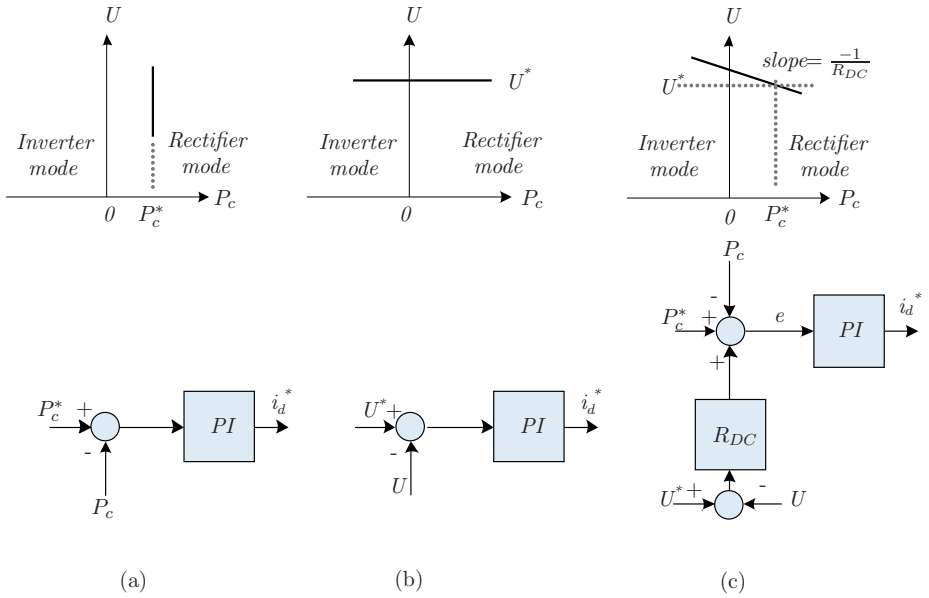


Figure 3.1: U versus P characteristics of different control configurations: (a) constant power control (b) constant dc voltage control (c) dc voltage droop control

time constant. This time constant is dependent upon the control parameters (i.e. proportional and integral constants) used as well as on the total capacitance of the dc grid (i.e. the sum of all dc filter capacitances and line capacitances in the dc grid). Hence in *master-slave* or *master-slave with dc droop* control configurations (as discussed in the previous section), the issue of precise power flow control may not be a challenge since power flow at individual terminals, except the master terminal, will be determined by the respective power references. It should be noted that in the presence of master terminal, dc voltage droop controlled converters appear almost as constant power controlled terminals due to little dc-bus voltage changes.
If the MTDC consists only of dc voltage droop and constant power terminals, there will be a challenge of getting desired power flow at the various droop controlled terminals. Dc voltage droop control of a converter requires two input references, namely: the dc voltage reference U^* and the power reference P_c^*. The actual power injection (P_c) is determined by the error signal e in Fig. 3.1 (c); which in turn is the total of the power control error signal ($P_c^* - P_c$) and voltage droop error signal ($(U^* - U) \times R_{DC}$). Hence the power injected by the VSC can suffer from a steady-state power flow control error ($P_c^* - P_c \neq 0$). Precise power flow control is a challenge

of getting the steady-state power flow profile to the same level as the one given by reference - which in turn is determined by the schedule (after power flow dispatch). The power flow dispatch is a result of market clearing, for example day-ahead power market (in deregulated system) or some kind of cost optimization technique. In the context of MTDC, the challenge for the operator is to determine the right values of references of the converters in such a way that the steady-state power flow in the entire dc grid becomes the same as the predetermined one from the given dispatch. In Fig. 3.1 (c), it is clear that if the dc voltage error signal is zero (i.e. $U^* - U = 0$), then precise power flow control can be achieved resulting in zero error for the power control (i.e. $P_c^* - P_c = 0$). This condition should be achieved for each dc droop controlled terminal in the entire dc grid. If one of the terminals fails to achieve this condition, the others will also experience steady-state power flow deviations. One possible cause of such power flow deviation is failing to consider the dc line voltage drops in the process of deciding the dc voltage references. This phenomenon will be demonstrated with the example dc grid network shown in Fig. 3.2.

The parameters shown in Fig. 3.2 are defined in Table 3.1.

Table 3.1: List of parameters used in Fig. 3.2

Parameter	Description
U_N	Rated dc grid voltage (in kV)
ρ_{DCi}	dc voltage droop constant of the i^{th} converter terminal (pu/pu)
P_{cNi}	Rated power capacity of i^{th} terminal (in MW)
l_{ij}	dc transmission distance between terminals i and j (in km)

In the five-terminal VSC-HVDC transmission model shown in Fig. 3.2, two of the VSC-HVDC terminals (i.e. terminal-3 and terminal-5) are set to be operated in constant power control mode whereas the other three VSC-HVDC terminals participate in the dc voltage droop control. It is important to stress that the use of term 'constant' here only means the invariability of power with respect to the dc voltage and not necessarily time invariability. Moreover, the power flow study in this section concerns only the steady-state conditions. Some numerical data such as size of converters and the various droop constants used in the simulation can be read from Fig. 3.2. The converter and dc transmission line parameters are also included in the same figure. Now, let us consider an arbitrary power flow schedule for the hypothetical dc grid. In Table 3.2, the desired power flow patter (i.e. the schedule) is given.

In the power flow schedule of Table 3.2 terminals 1, 3, 4 and 5 are desired to inject a power of 600 MW, −750 MW, 550 MW and −900 MW respectively into the dc grid.

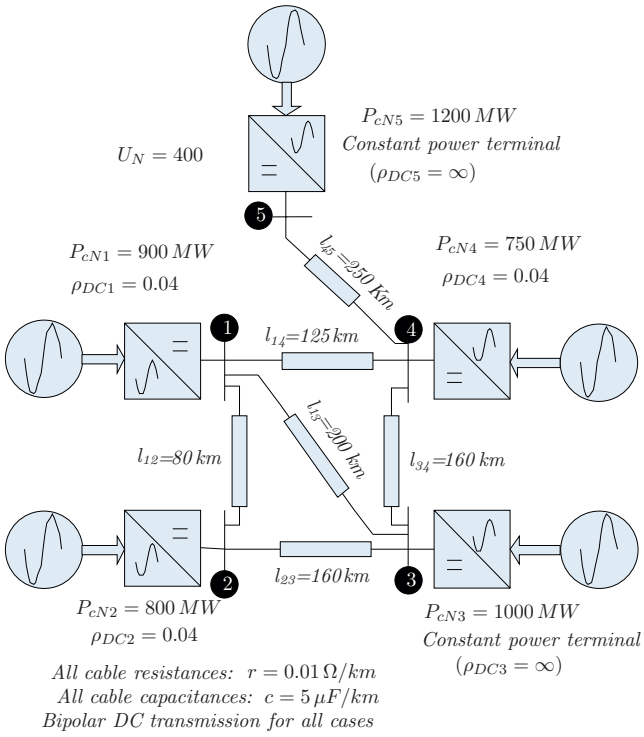


Figure 3.2: A hypothetical five-terminal VSC-HVDC with dc voltage droop control

Table 3.2: Desired power flow pattern (schedule)

Terminal No.	1	2	3	4	5
P_c^* (MW)	600	X	-750	550	-900

The minus signs show that power is taken away from the dc grid to ac grid via a VSC-HVDC terminal, implying inverter mode of operation. Terminals with positive power injection are in rectifier mode of operation. The 'X' in the second column of Table 3.2 shows a 'don't care' state. This is because terminal-2 is expected to inject the net balance of power needed into the dc grid so that the desired power flow will be achieved.

If we do not give any regard to the dc line voltage drops and the associated line losses, terminal-2 will be expected to inject a power of 500 MW into the dc grid. In Fig. 3.2 it is shown that the nominal dc grid voltage is 400 kV (±200 kV pole-to-

pole). Hence the dc voltage references will be assigned to 400 kV . The power and dc voltage references to be used in the simulation are listed in Table 3.3.

Table 3.3: Reference values used for simulation

Terminal No.	1	2	3	4	5
P_c^* (MW)	600	500	-750	550	-900
U^* (kV)	400	400	400	400	400

Terminals 3 and 5, which are constant power terminals, do not need dc voltage references although these were included in Table 3.3 for the sake of completeness. In order to better understand the influence of dc line resistance on power flow, two simulation cases will be considered for the study; one with no dc line resistances (i.e. ideal dc grid) and the other with dc line resistances as specified in Fig. 3.2. Simulation results of the ideal (i.e. lossless) five-terminal dc grid model are shown in Table 3.4. (See appendix A for details of the VSC model used in the simulations). As it would be expected, the power flow pattern of the ideal dc grid is seen to be the same as the desired (scheduled) power flow pattern given by Fig. 3.3 and Table 3.2.

Table 3.4: Simulation results for the set of references in Table 3.3 in an ideal dc grid

Terminal No.	1	2	3	4	5
P_c (MW)	600	500	-750	550	-900
U (kV)	400	400	400	400	400

When the dc line resistances are included in the simulation while maintaining the values of dc voltage references and power references as in the previous case, the power flow pattern becomes as shown in Fig. 3.4 and Table 3.5.

Table 3.5: Simulation results for the set of references in Table 3.3 and non-ideal dc grid

Terminal No.	1	2	3	4	5
P_c (MW)	578.821	466.793	-750.000	638.889	-900.000
U (kV)	400.377	400.664	397.511	398.104	386.460
P_c^* (MW)	600	500	-750	550	-900
P_{err} (MW)	-21.179	-33.207	0.000	88.889	0.000

From Table 3.5 it is clear that the set of reference values given by Table 3.3 does not enable us to get the desired power flow pattern given by Table 3.2. Large deviations of power flow are observed for terminals 1 and 4 whereas terminals 3 and 5 (i.e.

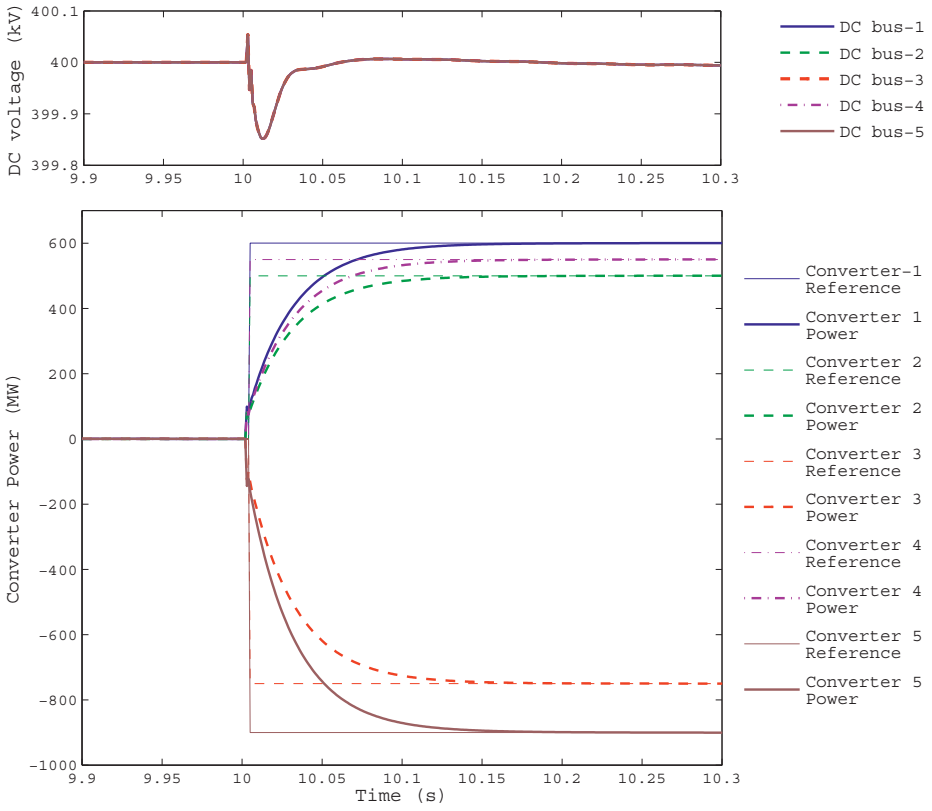


Figure 3.3: Power flow control responses in ideal (lossless) dc grid

terminals with fixed power control) showed no deviations, as can be expected. The power flow deviation in terminal-2 may be ignored, since this terminal was originally intended to cover the balance of power needed to get the desired power flow profile for the other terminals. The observed power flow deviations at terminals 1 and 4 are partly caused by the differences in the dc-bus voltages and partly due to the line losses which were not accounted for while assigning the power reference of terminal-2 (i.e. the slack bus). It is clear that in both cases the power flow deviation originates from the non-zero resistance of the dc lines. To find out which of the two mechanisms is the dominant factor, we will try to see the effects of the two separately with the five-terminal system as an example. In the first case we will account for the dc line losses but not for the dc-bus voltage differences. In the second case the dc-bus voltage differences will be accounted for while the dc line losses will not. Finally we

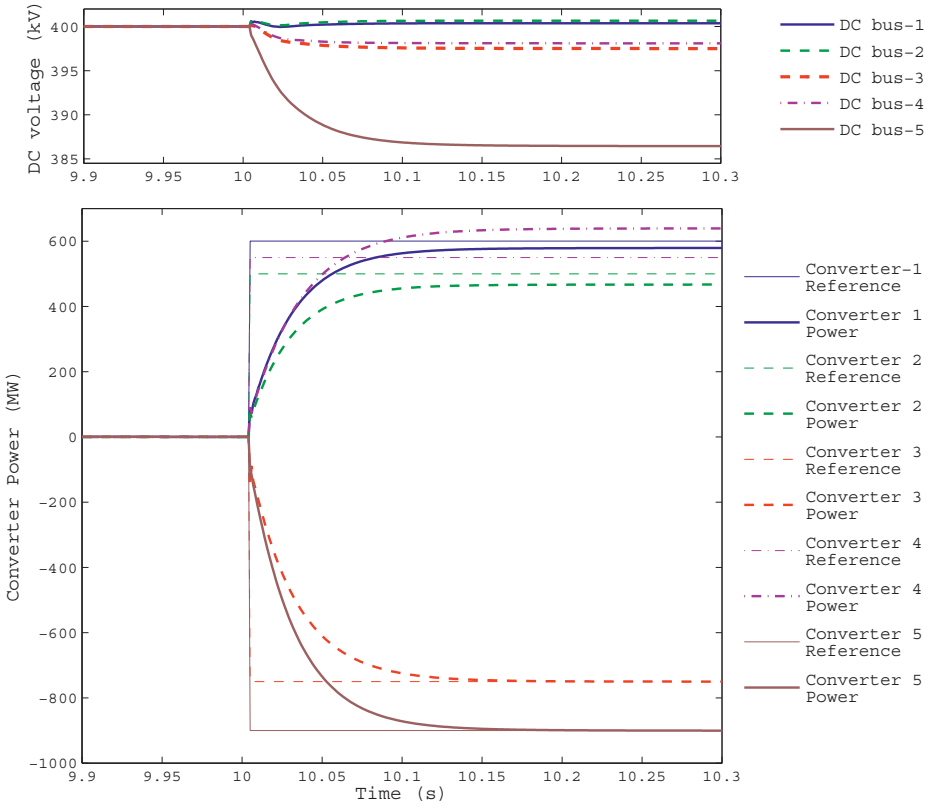


Figure 3.4: Power flow control responses in non-ideal dc grid

will simulate the case where both dc line losses and dc-bus voltage differences are accounted for.

First simulation case (only dc line losses are accounted for):
In order to compute the power losses in the system, it is necessary to make a dc power flow analysis of the system under consideration. In power flow analysis it is customary to assign the nominal voltage of the dc grid as the known voltage of the dc slack bus prior to the power flow calculations. Hence the complete input information for the load flow analysis becomes as shown in Table 3.6.

The 'X's in Table 3.6 show 'slack' variables, i.e. values that result from the power flow equations. The data in Table 3.6 and the dc grid resistances in Fig. 3.2 are

Table 3.6: Input data for the power flow analysis

Terminal No.	1	2	3	4	5
P_c (MW)	600	X	-750	550	-900
U (kV)	X	400	X	X	X

provided to a dc power flow algorithm and the resulting solution is given in Table 3.7. Various algorithms of dc load flow analysis are proposed in the literature [46], [65],[83].

Table 3.7: Results from the dc power flow analysis

Terminal No.	1	2	3	4	5
P_c (MW)	600	535.938	-750	550	-900
U (kV)	399.550	400.000	396.613	396.928	385.247

From Table 3.7 it is now clear that the dc grid will have a total line loss of 36 MW for a total power transfer of $750 + 900 = 1650$ MW between the various converters. This is around 2.2% transmission loss for the entire dc grid (or alternatively a transmission efficiency of 97.8%) for the given power flow profile. It should be noted that the converter losses are not included here, since all power measurements so far are measured from the dc-bus side. Although in practice power measurements are done at PCC (i.e. ac side of the converter), here we stick to power measurement from the dc-bus side so that the impact of the dc line resistances can be investigated separately from the converter losses.
Back in the PSCAD simulation of the five-terminal dc grid, now we change the power reference of terminal-2 from its previous value of 500 MW to 535.9 MW (computed from the power flow analysis). By doing so we are accounting for the dc line losses in the power reference assignment of the slack bus. The dc voltage reference (of each terminal) however will be kept at the same value as in the previous simulation case (i.e. 400 kV in all cases). Running the simulation with the change mentioned above, we get the steady-state power flow profile given by Table 3.8.

Table 3.8: Simulation results with power references adjusted for dc losses

Terminal No.	1	2	3	4	5
P_c (MW)	566.351	488.558	-749.999	629.696	-899.999
U (kV)	400.598	400.948	397.747	398.300	386.662
P_c^* (MW)	600	535.938	-750	550	-900
P_{err} (MW)	-33.649	-47.380	0.001	79.696	0.001

Second simulation case (only dc-bus voltage differences are accounted for):
For comparison, we look at the simulation where the dc voltage references are replaced by the voltage values from the load flow analysis (i.e. the second row in Table 3.7). This confirms that the dc-bus voltage differences are appropriately accounted for in the dc voltage reference assignments. The power reference of terminal-2, however, will be kept at 500 MW. The observed simulation results are shown in Table 3.9.

Table 3.9: Simulation results with references adjusted only for dc-bus voltage differences

Terminal No.	1	2	3	4	5
P_c (MW)	612.459	514.157	-750.000	559.194	-900.000
U (kV)	399.329	399.717	396.377	396.732	385.045
P_c^* (MW)	600	500	-750	550	-900
P_{err} (MW)	12.459	14.157	0.000	9.194	0.000

Comparing the power flow errors in Table 3.5, Table 3.8 and Table 3.9, it is easily noticeable that the errors reduced significantly when the appropriate dc voltage references were used in the simulation. This supports the argument that most of the power flow error is shown in Table 3.5 originates from inappropriate setting of the dc voltage references.

Third simulation case (both dc-bus voltage differences and dc line losses are accounted for):
Finally we run the dc grid simulation model one more time; this time taking into consideration both the dc-bus voltage differences as well as the total dc line power losses. This is done by using all the dc power flow analysis results in Table 3.7 for assigning dc voltage references and power references of the VSC-HVDC controllers. The resulting power flow profile is shown in Fig. 3.5 and Table 3.10.

Table 3.10: Simulation results with references adjusted for both dc-bus voltage differences and dc line losses

Terminal No.	1	2	3	4	5
P_c (MW)	600.001	535.930	-750.000	550.007	-900.000
U (kV)	399.550	400.000	396.613	396.928	385.247
P_c^* (MW)	600	535.938	-750	550	-900
$P_{c,err}$ (MW)	0.001	-0.008	0.000	0.007	0.000

From Table 3.10 it is noticeable that the observed power flow from the simulation matches very well the scheduled plan shown in Table 3.2. Previous power flow de-

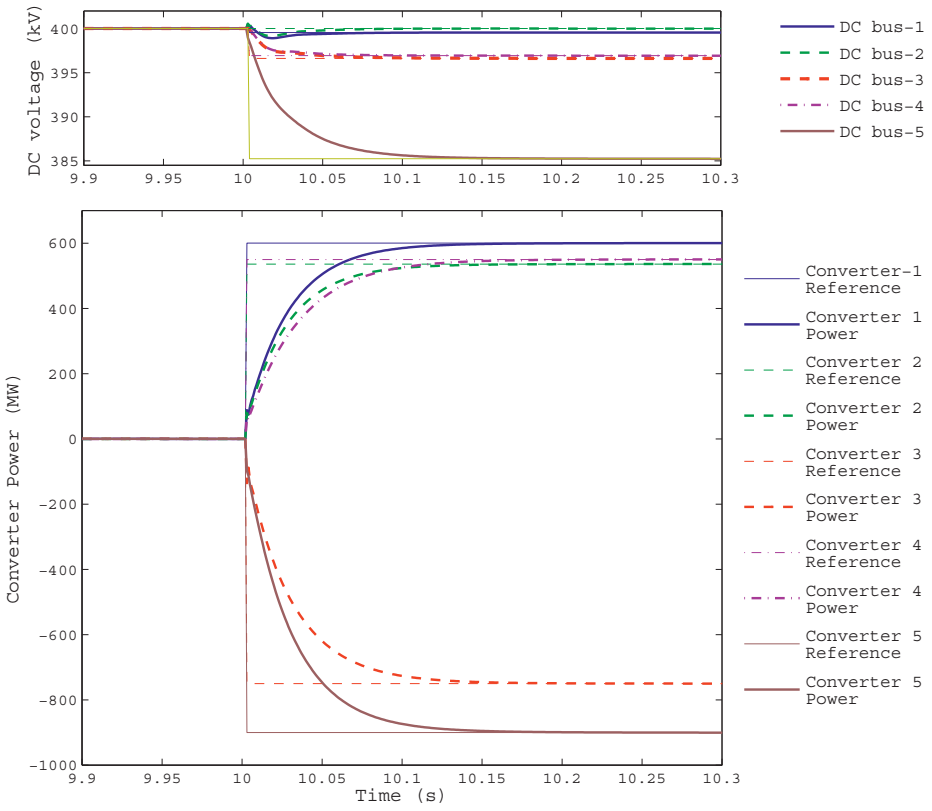


Figure 3.5: Power flow control responses in non-ideal dc grid (with impact of dc line resistances offset by appropriate assignment of the voltage and power reference values)

viations have been eliminated completely by accounting for both the line losses as well as the dc-bus voltage differences. In fact since the unknown dc-bus voltages and the unknown power of the slack bus are simultaneously found from the power flow analysis, all the required references are naturally obtained in just one process.

Comparing Table 3.8, Table 3.9 and Table 3.10, we can observe that roughly 90% of the power flow deviation in terminal-4 came from neglecting the dc-bus voltage differences whereas the rest 10% of the deviation came from neglecting the dc line losses. Even though the exact percentages of the contributions of the two factors on

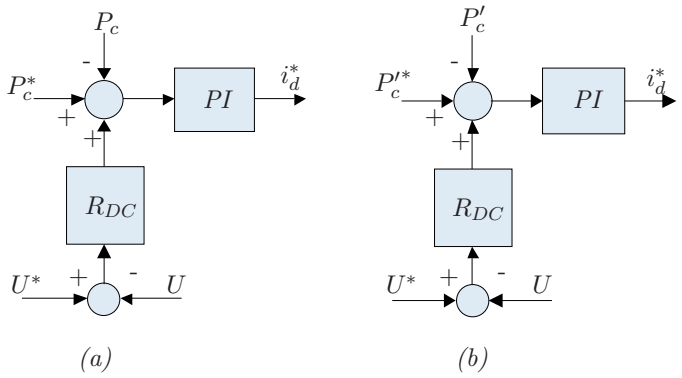


Figure 3.6: Two ways of implementing dc droop control: (a) power is measured at dc-bus (b) power is measured at PCC (i.e. on the ac side of the VSC)

power flow error depend on the dc grid topology and the specific power flow profile under consideration, it is possible to make a generalized conclusion that the dc-bus voltage differences contribute the much larger share of the power flow error.

Apart from the dc line resistances, the converter losses can also affect the power flow control depending on whether power measurement (for the control loop) is at PCC or at dc-bus. So far in the previous simulation cases it was considered that the power injections by the VSC-HVDCs are measured from the dc-bus side. In practice, however, it is much more common to measure the power flow from the ac side (i.e. at PCC). The power schedule also usually defines the power injections from the ac grid side. If such approach is applied to our example case of the five-terminal dc grid, the controllers in Fig. 3.6(b) should be employed instead of the one shown in Fig. 3.6(a) which was employed in all previous cases. Note that both the power references and the corresponding feedback signals in Fig. 3.6(b) refer to the ac side.

Now we keep the same power flow schedule given previously by Table 3.7. But this time we consider that all the power flow measurements are from the ac grid sides. The references used for the third simulation case above are also used here. This means that the ac and dc side converter powers are considered equal in this case. By doing so we are neglecting the converter power losses. The simulation results are shown in Table 3.11.

Once again, the simulation results in Table 3.11 show some power flow deviations in terminals 1, 2 and 4, from the one given by the schedule (though these are relatively

Table 3.11: Simulation results with references not adjusted for converter losses

Terminal No.	1	2	3	4	5
U^* (kV)	399.550	400.000	396.613	396.928	385.247
$P_c'^*$ (MW)	600	535.930	-750	550	-900
U (kV)	399.424	399.876	396.469	396.785	385.331
P_c (MW)	603.750	538.870	-754.200	553.050	-905.086
P_c' (MW)	607.394	542.138	-750.000	556.705	-899.999
$P'_{c,err}$ (MW)	7.394	6.208	0.000	6.705	0.001

modest amounts). In this case the deviations are caused by neglecting power losses of the converters. The remedy is to take the converter losses, together with the dc-bus voltage differences and dc line power losses, into account while determining the appropriate references of the VSC-HVDC controllers.
The ac and dc side power measurements (i.e. P_c' and P_c) of a VSC-HVDC are not exactly equal but are different by an amount equal to the converter power losses. This is depicted by the block diagram in Fig. 3.7 (b).

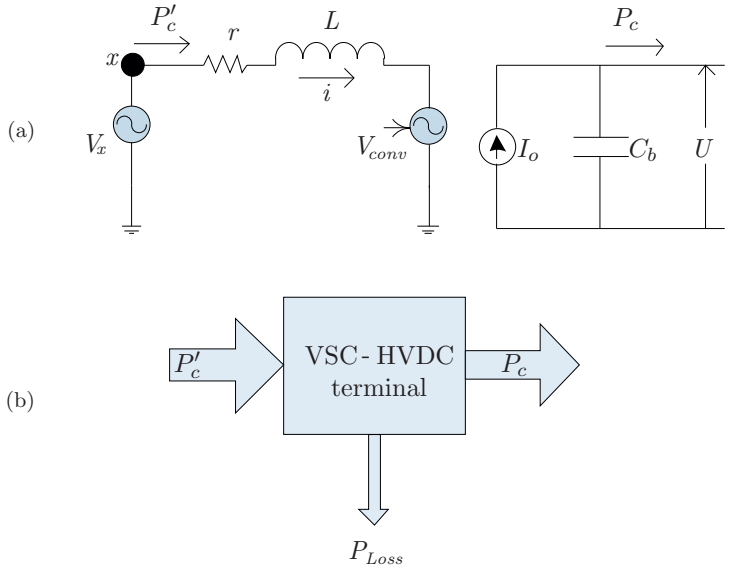


Figure 3.7: Relationship of ac and dc side power measurements of a VSC-HVDC: (a) single-line diagram of VSC. (b) block diagram of power flow in VSC

A crude way of modeling (at least part of) the VSC losses is by adding a series resistance on the ac side of the converter. In Fig. 3.7 (a) for example the series resistance r could represent the losses in both the inductive filter as well as the semiconductors. This approach, though simplistic, may suffice to show the impact of converter losses on dc grid power flow. From Fig. 3.7, the ac and dc side power measurements are related by

$$P'_c - P_c - P_{Loss} = 0 \tag{3.1}$$

The converter losses consist of two components: load independent part (which is constant) and load dependent part. In the discussion that follows, however, we will only refer to Fig. 3.7(a), and hence we will have only a load dependent power loss in this case. Converter loss modeling is out of the scope of this thesis and hence only a very simplistic loss model will be used here (i.e. the loss in the series resistance (r) of Fig. 3.7(a)). based on this, the losses in the VSC are computed as

$$\left.\begin{aligned} P_{Loss} &= 3i^2 r \\ &= 3\left(\tfrac{P'_c}{3V_x}\right)^2 r \\ &= \tfrac{r}{3}\left(\tfrac{P'_c}{V_x}\right)^2 \end{aligned}\right\} \tag{3.2}$$

Substituting (3.2) into (3.1), we get

$$P'_c - \frac{r}{3}\left(\frac{P'_c}{V_x}\right)^2 - P_c = 0 \tag{3.3}$$

Dividing all the terms in (3.3) by the rated power, P_{cN}, we get

$$\left.\begin{aligned} &\tfrac{P'_c}{P_{cN}} - \tfrac{r}{3P_{cN}}\left(\tfrac{P'_c}{V_x}\right)^2 - \tfrac{P_c}{P_{cN}} = 0 \\ &= P'_{c,pu} - \tfrac{r}{\left(3V_x^2/P_{cN}\right)} {P'_{c,pu}}^2 - \tfrac{P_c}{P_{cN}} \\ &= P'_{c,pu} - r_{pu} {P'_{c,pu}}^2 - P_{c,pu} = 0 \end{aligned}\right\} \tag{3.4}$$

where the subscripts pu show that the variables are in per-units. Rearranging (3.4) gives

$$P_{c,pu} = P'_{c,pu}\left(1 - r_{pu}P'_{c,pu}\right) \tag{3.5}$$

Hence if the ac side VSC power (P'_c) is known, the dc side power can be computed by (3.5). The ac side power can be described by

$$P'_{c,pu} = \frac{P_{c,pu}}{1 - r_{pu}P'_{c,pu}} \tag{3.6}$$

Since, $r_{pu}P_{DC,pu} \ll 1$, we can use the Taylor's approximation method $\frac{1}{1-r_{pu}P'_{c,pu}} \simeq 1 + r_{pu}P'_{c,pu}$. Hence, the expression in (3.6) can further be simplified as

$$\left.\begin{aligned} P'_{c,pu} &= \tfrac{P_{c,pu}}{1-r_{pu}P'_{c,pu}} \simeq \left(1 + r_{pu}P'_{c,pu}\right)P_{c,pu} \\ &\simeq \left(1 + r_{pu}P_{c,pu}\right)P_{c,pu} \end{aligned}\right\} \tag{3.7}$$

As mentioned before, all the relations (3.3)-(3.7) are based on a crude modeling of the converter losses which is used here only for demonstration purposes. For better accuracy, a more realistic modeling of converter losses must be used to get better results in estimation of ac or dc side power, provided that one of these two is known. Indeed the losses in VSC-HVDC should include not only the semiconductor and filter losses but also the power consumed locally at the converter station during operation [61],[62],[13]. Deriving the analytical expression of the total loss by adding up the losses in the individual components may be a laborious task and may not guarantee accuracy. An alternative approach is to establish an approximate analytical expression based upon empirical data for the total loss at various levels of transmitted power via the VSC-HVDC.
Once the relationship between the ac and dc side power measurements is established, the same expression can be used to compute the ac/dc power reference given that one of the two is known. In our example case, the ac side power references are known from the schedule and the dc side power and voltage references are unknown.

Table 3.12: Desired power flow pattern (schedule) defined at PCC of each VSC

Terminal No.	1	2	3	4	5
$P'_{c,sched}$ (MW)	600	X	-750	550	-900

The schedule given by Table 3.12 is similar to the previous one given by Table 3.2, with the exception of the measurement points. While in the previous case the power references were with respect to the dc side measurements, in the current case the

power references are with respect to ac side measurements. The computations of the dc side power references are summarized in Table 3.13. In the VSC models used in the simulation r_{pu} equals 0.01 (Refer the appendix for more information on this).

Table 3.13: Power reference calculation taking converter losses into consideration

Terminal No.	1	2	3	4	5
$P'_{c,sched}$ (MW)	600	?	-750	550	-900
P_{cN} (MW)	900	800	1000	750	1200
$P'_{c,pu}$ (pu)	0.66667	?	-0.75000	0.73333	-0.75000
$1 - r_{pu}P'_{c,pu}$ (pu)	0.99333	?	1.00750	0.99267	1.00750
P_c (MW)	596.026	X	-755.668	545.998	906.801

Now the dc-bus power injections are known for all terminals except for the slack bus, for which the unknown parameters are shown as question marks. The next step is to make power flow analysis of the dc grid with the specified dc power injections (i.e. the last row in Table 3.13). Hence, the input data for the power flow analysis is given in Table 3.14.

Table 3.14: Input data for the power flow analysis

Terminal No.	1	2	3	4	5
P_c (MW)	596.026	X	-755.668	545.998	906.801
U (kV)	X	400	X	X	X

The result of the power flow analysis is shown in Table 3.15.

Table 3.15: Result of dc power flow analysis

Terminal No.	1	2	3	4	5
P_c (pu)	596.026	557.111	-755.668	545.998	-906.801
U (kV)	399.498	400.000	396.546	396.829	385.054

From (3.7) and the result of the power flow analysis, the ac side power reference of terminal-2 (the slack bus) can be computed. Table 3.16 shows the complete list of references that must be applied for the VSC-HVDC controllers.

It was previously mentioned that in the current simulation case the power is controlled from the ac side. Hence, only the ac power references and the dc voltage references in Table 3.16 will be relevant for the VSC-HVDC controllers. With such set of references used in the five-terminal VSC-HVDC transmission model, the simulation results shown in Table 3.17 are obtained.

Table 3.16: Power references adjusted for converter loss compensations based on (3.6) and (3.7)

Terminal No.	1	2	3	4	5
U^* (kV)	399.498	400.000	396.546	396.829	385.054
P_c^* (MW)	596.026	557.111	-755.668	545.998	-906.801
$P_c'^*$ (MW)	600	560.991	-750	550	-900

Table 3.17: Simulation results when power and dc voltage references from Table 3.16 are applied

Terminal No.	1	2	3	4	5
U (kV)	399.527	400.028	396.581	396.863	385.112
P_c (MW)	594.850	556.087	-754.199	544.867	-905.087
P_c' (MW)	598.393	559.559	-750.000	548.418	-899.999
$P'_{c,sched}$ (MW)	600	560.991	-750	550	-900
$P'_{c,err}$ (MW)	-1.607	-1.432	0.000	-1.582	0.001

The results listed Table 3.17 shows that the accuracy of the power flow control improves substantially when the converter power losses are considered together with the dc-bus voltage difference and dc line losses. This approach is, of course, relevant only when the power controllers refer to the ac sides of the VSC-HVDCs - which is often the case.

In the demonstration above, approximate analytical expressions have been used for computing the missing parameters. In practice however, the power flow analysis includes both the dc grid as well as ac grid connected to it and hence the results of the power flow analysis include all missing parameters of the ac and dc grids constituting the entire power system under consideration. In references [39],[65], [40], [38] and [28] for example, different approaches for integrated ac/dc power flow analysis have been presented. By using the results from integrated ac/dc power flow analysis, the errors shown in Table 3.17 may be reduced and the overall accuracy of the steady-state power injection control in multi-terminal VSC-HVDC can possibly be further improved.

3.3 Impact of DC Line Voltage Drops on Primary Control of MTDC Transmission

3.3.1 Distribution of Balancing Power in an Ideal Lossless DC Grid

In the previous section the influence of dc resistance on achieving precise power flow control in dc grid was discussed. In this section the impact of dc line resistances on the steady-state control response (i.e. on primary control of dc grid) will be investigated.
Frequency droop constant (ρ_g) of a synchronous generator unit in an ac grid is defined as the ratio of the change in frequency in per-unit (Δf_{pu}) to the resulting change in generated power in per-unit($\Delta P_{g,pu}$) caused by the change in frequency. This is mathematically given by

$$\frac{\Delta f_{pu}}{\Delta P_{g,pu}} = \rho_g \tag{3.8}$$

In multi-machine ac grids, the frequency vs power relationship is more often given by physical units rather than in per-unit. Frequency response of an ac grid is defined as the change in power generation (ΔP_g) in MW in response to a change of 1Hz of the ac grid frequency (Δf). this is mathematically given as

$$\frac{\Delta P_g}{\Delta f} = R_f \tag{3.9}$$

Frequency droop constant (ρ_g) and frequency response (R_g) are related by

$$R_g = \frac{P_{gN}}{f_N \rho_g} \tag{3.10}$$

where P_{gN} and f_N refer to the rated power capacity of the generation unit and the rated (nominal) operating frequency respectively. In frequency droop control of multi-machine ac grid, the steady-state responses of the synchronous generator controllers are dependent upon the observed steady-state frequency changes and the employed droop constants for each generator unit. The steady-state change in frequency observed by each generator controller is the same regardless of its location in the ac grid. In other words, the steady-state change in frequency is universally the same throughout the ac grid. This enables us to compute the aggregate frequency response ($R_{g,agg}$) of an ac grid from the frequency responses of individual generation units [45](chapter 8):

$$\left.\begin{aligned} R_{g,agg} = \frac{\Delta P_{g,agg}}{\Delta f} = \frac{1}{\Delta f}\sum_{i=1}^{n}\Delta P_{gi} = \frac{1}{\Delta f}\sum_{i=1}^{n}\frac{P_{gNi}\Delta f}{f_N \rho_{gi}} \\ = \frac{1}{f_N}\sum_{i=1}^{n}\frac{P_{gNi}}{\rho_{gi}} \end{aligned}\right\} \tag{3.11}$$

where n is the number of synchronous generators constituting the ac grid. The subscript agg in (3.11) refers to the aggregation of parameters related to individual generation units.

Like frequency response of synchronous generator in an ac grid, dc voltage response of VSC-HVDC station in a dc grid can be defined in a similar manner (assuming that dc voltage droop control is to be employed). Dc voltage response is the change in MW of power injected into the dc grid by the converter station as a response to a dc-bus voltage change of 1 kV. Dc voltage droop constant is defined as the ratio of change in dc-bus voltage in per-unit to the corresponding change in converter power flow in per-unit. This is given by

$$\frac{\Delta P_{c,pu}}{\Delta U_{pu}} = \rho_{DC} \tag{3.12}$$

Dc voltage droop constant (ρ_{DC}) and dc voltage response (R_{DC}) are related by (3.13).

$$R_{DC} = \frac{P_{cN}}{U_N \rho_{DC}} \tag{3.13}$$

P_{cN} and U_N refer to the rated power capacity and rated operating dc voltage level of the VSC-HVDC terminal under consideration. R_{DC} is the dc voltage response of a dc grid (analogous to the frequency response (R_g) in ac grids); i.e. R_{DC} is a measure of how much power in MW will be injected by a VSC-HVDC terminal as a response to a dc-bus reduction of 1 kV.

For the sake of convenience in writing long equations, from now on we use R instead of R_{DC}. Hence the dc droop equation of (2.39) re-written in small-signal form becomes as

$$\Delta P_c = \Delta P_c^* + R_{DC}\left(\Delta U^* - \Delta U\right) \tag{3.14}$$

From (3.14) it is observed that the power flow of the dc terminal can be controlled either by changing the power reference (P_c^*) or by changing the dc voltage reference (U^*). Now let us focus on the impact of change in power reference (i.e. ΔP_c^*). Assuming that the dc voltage reference U^* remains fixed (and hence $\Delta U^* = 0$), the relation given by (3.14) can be simplified as

$$\Delta P_c = \Delta P_c^* - R_{DC}\Delta U \tag{3.15}$$

In a lossless dc grid (hereafter referred to as ideal dc grid), the algebraic sum of all nodal injected powers is zero:

$$\sum_{i=1}^{n} P_{ci} = 0 \tag{3.16}$$

The small-signal equivalent of (3.16) is given by (3.17).

$$\sum_{i=1}^{n} \Delta P_{ci} = 0 \tag{3.17}$$

After substituting (3.15) into (3.17) we get (3.18).

$$\sum_{i=1}^{n} \Delta P_{ci}^{*} - \sum_{i=1}^{n} (R_{DCi} \Delta U_i) = 0 \tag{3.18}$$

Moreover, in ideal dc grid, all dc-bus voltages are equal to one another and all changes in dc-bus voltages are also equal to each other:

$$\underset{i \in \{1,\ldots,n\}}{\Delta U_i} = \Delta U \tag{3.19}$$

Substituting (3.19) into (3.18) gives

$$\Delta U = \underset{i \in \{1,\ldots,n\}}{\Delta U_i} = \frac{\sum\limits_{i=1}^{n} \Delta P_{ci}^{*}}{\sum\limits_{i=1}^{n} R_{DC}} = \frac{\sum\limits_{i=1}^{n} \Delta P_{ci}^{*}}{R_{DC,agg}} \tag{3.20}$$

where $R_{DC,agg}$ is the aggregated dc voltage response of the dc grid (analogous to aggregated frequency response of ac grids).

Following the same analogy of the aggregate frequency response in ac grids ($R_{f,agg}$), aggregate dc voltage response ($R_{DC,agg}$) is computed as

$$R_{DC,agg} = \frac{1}{U_N} \sum_{i=1}^{n} \frac{P_{cNi}}{\rho_{DCi}} \tag{3.21}$$

From equation (3.15), steady-state power deviation at terminal-j, as a function of voltage deviation, is given by (3.22).

$$\Delta P_{cj} = \Delta P_{cj}^{*} - R_{DCj} \Delta U_j \tag{3.22}$$

Substituting (3.21) into (3.22), we get

$$\Delta P_{cj} = \left(1 - \frac{R_{DCj}}{R_{DC,agg}}\right) \Delta {P_{cj}}^{*} - \frac{R_{DCj}}{R_{DC,agg}} \left(\sum_{i=1, i \neq j}^{n} \Delta P_{ci}^{*} \right) \tag{3.23}$$

In matrix form, (3.23) is re-written as

$$\begin{bmatrix} \Delta P_{c1} \\ \vdots \\ \Delta P_{cj} \\ \vdots \\ \Delta P_{cn} \end{bmatrix} = \underbrace{\begin{bmatrix} 1-\frac{R_{DC1}}{R_{DC,agg}} & \cdots & -\frac{R_{DC1}}{R_{DC,agg}} & \cdots & -\frac{R_{DC1}}{R_{DC,agg}} \\ \vdots & \ddots & \vdots & \ddots & \vdots \\ -\frac{R_{DCj}}{R_{DC,agg}} & \cdots & 1-\frac{R_{DCj}}{R_{DC,agg}} & \cdots & -\frac{R_{DCj}}{R_{DC,agg}} \\ \vdots & \ddots & \vdots & \ddots & \vdots \\ -\frac{R_{DCn}}{R_{DC,agg}} & \cdots & -\frac{R_{DCn}}{R_{DC,agg}} & \cdots & 1-\frac{R_{DCn}}{R_{DC,agg}} \end{bmatrix}}_{\mathbf{A}} \begin{bmatrix} \Delta P^*_{c1} \\ \vdots \\ \Delta P^*_{cj} \\ \vdots \\ \Delta P^*_{cn} \end{bmatrix} \tag{3.24}$$

Equation (3.24), indicates that the power flow of terminal-j can be affected both by a change in power reference of the same terminal (ΔP^*_{cj}) and also by a change in power reference of another terminal (ΔP^*_{ci}), but with differing signs and proportionality constants for the two cases. Moreover, it can be observed from (3.23) that in the absence of line voltage drops, distribution of balancing power will exclusively be dependent on the dc voltage response (R_{DCj}) of the individual dc terminal and the total dc voltage response ($R_{DC,agg}$) of the entire dc grid system, regardless of the location in the dc grid where the change in power reference has occurred.

3.3.2 Distribution of Balancing Power in a Non-ideal DC Grid

A dc grid whose lines have non-zero resistances exhibits unequal variations in dc-bus voltages hence making the analogy between dc voltage droop control and frequency droop control imperfect. This means that (3.24) explains the actual dc grid response only when the dc line resistances are negligible. For all other cases the equation fails to explain the responses of the various VSC-HVDC terminals (due to unequal variations of the dc-bus voltages).

For the sake of convenience in mathematical notation in the following analysis, we resort to the use of vector notation. In order to differentiate the vector quantities from the scalar ones, vectors and matrices will be written in bold face letters. Hence the vectors $\mathbf{P}_c$, $\mathbf{U}$, and $\mathbf{P}^*_c$ are defined as

$$\mathbf{P}_c = \begin{bmatrix} P_{c1} \\ \vdots \\ P_{ci} \\ \vdots \\ P_{cn} \end{bmatrix}, \quad \mathbf{U} = \begin{bmatrix} U_1 \\ \vdots \\ U_i \\ \vdots \\ U_n \end{bmatrix}, \quad \mathbf{P}^*_c = \begin{bmatrix} P^*_{c1} \\ \vdots \\ P^*_{ci} \\ \vdots \\ P^*_{cn} \end{bmatrix} \tag{3.25}$$

where n is the total number of terminals in the MTDC transmission system.

Other vectors such as $\Delta\mathbf{P}_c$, $\Delta\mathbf{U}$, $\Delta\mathbf{P}_c^*$ and $\Delta\mathbf{R}_{DC}$ are defined in a similar manner. The nodal current injection into the dc grid is given by the vector $\mathbf{I}_{DC}$ expressed as

$$\mathbf{I}_{DC} = \mathbf{Y}\mathbf{U} \tag{3.26}$$

The power injection vector ($\mathbf{P}_c$) is given by

$$\left.\begin{aligned} \mathbf{P}_c &= \mathbf{U} \otimes \mathbf{I}_{DC} \\ &= \mathbf{U} \otimes (\mathbf{Y}\mathbf{U}) \end{aligned}\right\} \tag{3.27}$$

where $\mathbf{Y}$ refers to the admittance matrix of the dc grid and the symbol $\otimes$ is entry-wise (point-to-point) matrix multiplication operator, also called Hadamard product operator. Differentiation of the power flow equations of individual terminals with respect to the nodal voltage vector $\mathbf{U}$ results in the Jacobian matrix ($\mathbf{J}_{DC}$) of the dc grid:

$$\mathbf{J}_{DC} = \frac{\partial \mathbf{P}_c}{\partial \mathbf{U}} \tag{3.28}$$

Consider that the dc grid has an initial state given by $(\mathbf{P}^o, \mathbf{U}^o)$. The linearization of power flow equation around the initial steady-state point gives

$$\left.\begin{aligned} \mathbf{U} &= \mathbf{U}^o + \Delta\mathbf{U} \\ \mathbf{P}_c &= \mathbf{P}_c^o + \Delta\mathbf{P}_c = \mathbf{U}^o \otimes (\mathbf{Y}\mathbf{U}^o) + \mathbf{J}_{DC}\Delta\mathbf{U} \end{aligned}\right\} \tag{3.29}$$

Hence, the relationship between the vectors representing small-signal dc voltage ($\Delta\mathbf{U}$) and small-signal nodal power ($\Delta\mathbf{P}_c$) is given by

$$\Delta\mathbf{P}_c = \mathbf{J}_{DC}\Delta\mathbf{U} \tag{3.30}$$

If the vector ($\Delta\mathbf{P}_c$) is known, the voltage vector ($\Delta\mathbf{U}$) can be found as follows:

$$\Delta\mathbf{U} = {\mathbf{J}_{DC}}^{-1}\Delta\mathbf{P}_c \tag{3.31}$$

The dc Jacobian matrix can be computed by partially derivating individual elements of vector $\mathbf{P}_c$ with respect to individual elements of vector $\mathbf{U}$. Another alternative is to apply vector calculus methods which result in

$$\left.\begin{aligned} \mathbf{J}_{DC} &= \tfrac{\partial \mathbf{P}_c}{\partial \mathbf{U}} \\ &= \operatorname{diag}(\mathbf{U})\,\mathbf{Y} + \operatorname{diag}(\mathbf{Y}\mathbf{U}) \end{aligned}\right\} \tag{3.32}$$

The operator diag refers to a mathematical operation which transforms a vector into a diagonal matrix.
For a flat dc voltage profile ($U_1 = U_1 \cdots = U_n = U_f$), it is clear that the current in the dc grid becomes zero ($\mathbf{I} = (\mathbf{YU}) = \mathbf{0}$). Hence, the corresponding dc Jacobian matrix becomes

$$\left.\begin{aligned}\mathbf{J_{DC}} &= \operatorname{diag}(\mathbf{U})\,\mathbf{Y} + \operatorname{diag}(\mathbf{YU}) \\ &= \begin{bmatrix} U_f & \cdots & 0 & \cdots & 0 \\ \vdots & \ddots & \vdots & \ddots & \vdots \\ 0 & \cdots & U_f & \cdots & 0 \\ \vdots & \ddots & \vdots & \ddots & \vdots \\ 0 & \cdots & 0 & \cdots & U_f \end{bmatrix} \mathbf{Y} + \operatorname{diag}\left(\mathbf{Y} \begin{bmatrix} U_f & \cdots & U_f & \cdots & U_f \\ \vdots & \ddots & \vdots & \ddots & \vdots \\ U_f & \cdots & U_f & \cdots & U_f \\ \vdots & \ddots & \vdots & \ddots & \vdots \\ U_f & \cdots & U_f & \cdots & U_f \end{bmatrix} \right) \\ &= U_f\mathbf{Y} + 0 = U_f\mathbf{Y}\end{aligned}\right\} \tag{3.33}$$

Re-writing the dc droop equation of (2.39) in vector form we get

$$\mathbf{P}_c^* - \mathbf{P}_c - \operatorname{diag}(\mathbf{R}_{DC})\,(\mathbf{U}^* - \mathbf{U}) = 0 \tag{3.34}$$

The small-signal equivalent form of (3.34) is given by

$$\Delta\mathbf{P}_c{}^* - \Delta\mathbf{P}_c - \operatorname{diag}(\mathbf{R}_{DC})\,(\Delta\mathbf{U}^* - \Delta\mathbf{U}) = 0 \tag{3.35}$$

We consider that the dc voltage references remain unchanged ($\Delta\mathbf{U}^* = \mathbf{0}$). Substituting (3.31) into (3.35), we get

$$\Delta\mathbf{P}_c = \Delta\mathbf{P}_c{}^* - \operatorname{diag}(\mathbf{R}_{DC})\,\mathbf{J}_{DC}{}^{-1}\Delta\mathbf{P}_c \tag{3.36}$$

Equation (3.36) can further be simplified as

$$\Delta\mathbf{P}_c = \mathbf{B}\Delta\mathbf{P}_c{}^* \tag{3.37}$$

where $\mathbf{I}$ is identity matrix and the matrix $\mathbf{B}$ is given by

$$\mathbf{B} = \mathbf{J}_{DC}(\mathbf{J}_{DC} + \operatorname{diag}(\mathbf{R}_{DC}))^{-1} \tag{3.38}$$

From (3.32) and (3.37), the dc voltage change ($\Delta\mathbf{U}$) becomes

$$\left.\begin{aligned}\Delta\mathbf{U} &= \mathbf{J}_{DC}{}^{-1}\Delta\mathbf{P}_c \\ &= \left(\mathbf{I} + \operatorname{diag}(\mathbf{R}_{DC})\,\mathbf{J}_{DC}{}^{-1}\right)\Delta\mathbf{P}_c{}^* \\ &= \mathbf{J}_{DC}{}^{-1}\mathbf{J}_{DC}(\mathbf{J}_{DC} + \operatorname{diag}(\mathbf{R}_{DC}))^{-1}\Delta\mathbf{P}_c^* \\ \Delta\mathbf{U} &= (\mathbf{J}_{DC} + \operatorname{diag}(\mathbf{R}_{DC}))^{-1}\Delta\mathbf{P}_c^*\end{aligned}\right\} \tag{3.39}$$

Comparing (3.24) and (3.36), the differences in the two equations is marked by the differences between the matrices **A** and **B**. As discussed previously, the matrix **A** is independent of dc grid topology since an ideal grid was assumed to establish the mathematical relation. In contrast, the constant matrix **B** is dependent upon dc line resistances and upon dc grid topology. This is reflected by the presence of the dc Jacobian matrix ($\mathbf{J}_{DC}$) in (3.39). Due to the line voltage drop considerations, equation (3.39) gives an accurate mathematical model of the interaction between power control reference changes and the resulting observed power flow pattern in the dc grid. To demonstrate this, we will look at simulation results of the dc grid shown in Fig. 3.8 which consists of dc lines with non-zero resistances.

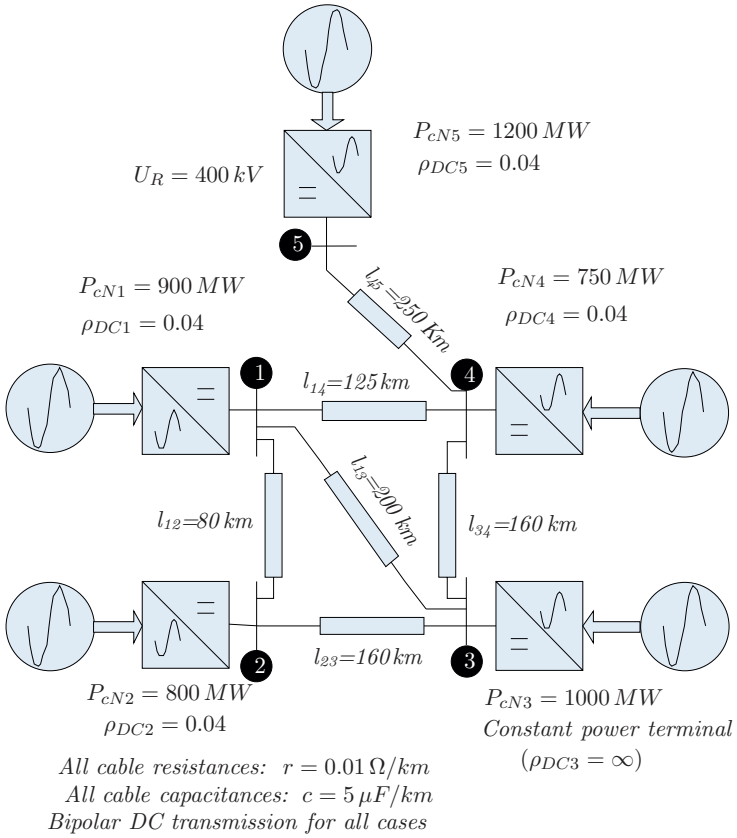


Figure 3.8: Five-terminal VSC-HVDC with non-zero dc line resistances

Parameters used in the simulation are shown in Table 3.18.

Table 3.18: Parameters of HVDC terminals used in the simulation

Terminal No.	1	2	3	4	5
P_{cN} (MW)	900	800	1000	750	1200
U_N (kV)	400	400	400	400	400
ρ_{DC}	0.04	0.04	∞	0.04	0.04
R_{DC} (MW/kV)	56.25	50	0	46.88	75

The initial steady-state power flow pattern is shown in Table 3.19. The admittance

Table 3.19: Initial steady-state condition of the MTDC in Fig. 3.8

Terminal No.	1	2	3	4	5
U (kV)	399.550	400.000	396.613	396.928	385.247
P_c (MW)	600.000	535.928	-750.00	550.005	-900.00

matrix ($\mathbf{Y}$) of the given dc grid is given by (3.40).

$$\mathbf{Y} = \begin{bmatrix} 1.2750 & -0.6250 & -0.2500 & -0.4000 & 0.0000 \\ -0.6250 & 0.9375 & -0.3125 & 0.0000 & 0.0000 \\ -0.2500 & -0.3125 & 0.8750 & 0.3125 & 0.0000 \\ -0.4000 & 0.0000 & -0.3125 & 0.9125 & -0.2000 \\ 0.0000 & 0.0000 & 0.0000 & -0.2000 & 0.2000 \end{bmatrix} 1/\Omega \tag{3.40}$$

From (3.40) and (3.32), the dc Jacobian matrix becomes

$$\mathbf{J}_{DC} = \begin{bmatrix} 510.9277 & -249.7186 & -99.8874 & -159.8199 & 0 \\ -250.0000 & 376.3398 & -125.0000 & 0 & 0 \\ -099.1532 & -123.9415 & 345.1453 & -123.9415 & 0 \\ -158.7711 & 0 & -124.0399 & 363.5821 & -79.3855 \\ 0 & 0 & 0 & -77.0494 & 74.7132 \end{bmatrix} \frac{\text{MW}}{\text{kV}} \tag{3.41}$$

From Table 3.18, the vector $\mathbf{R}_{DC}$ is described as

$$\mathbf{R}_{DC} = \begin{bmatrix} 56.25 & 50 & 0 & 46.88 & 75 \end{bmatrix}', \frac{\text{MW}}{\text{kV}} \tag{3.42}$$

Substituting (3.41) and (3.42) into (3.37), we find

$$\mathbf{B} = \begin{bmatrix} 0.6509 & -0.2906 & -0.2963 & -0.2503 & -0.1327 \\ -0.2586 & 0.6515 & -0.2743 & -0.2038 & -0.1081 \\ 0.0000 & 0.0000 & 1.0000 & 0.0000 & 0.0000 \\ -0.2072 & -0.1896 & -0.2347 & 0.7049 & -0.1565 \\ -0.1706 & -0.1561 & -0.1933 & -0.2430 & 0.3702 \end{bmatrix} \tag{3.43}$$

Similarly by replacing the relevant parameters in (3.24) we get

$$\mathbf{A} = \begin{bmatrix} 0.7534 & -0.2466 & -0.2466 & -0.2466 & -0.2466 \\ -0.2192 & 0.7808 & -0.2192 & -0.2192 & -0.2192 \\ 0.0000 & 0.0000 & 1.0000 & 0.0000 & 0.0000 \\ -0.2055 & -0.2055 & -0.2055 & 0.7945 & -0.2055 \\ -0.3288 & -0.3288 & -0.3288 & -0.3288 & 0.6712 \end{bmatrix} \tag{3.44}$$

Note that the third row in matrix **A** is identical to the third row in matrix **B**. This happens when the row under consideration corresponds to a VSC-HVDC terminal in constant power control mode.

Consider that the power reference of terminal-3 (ΔP^*_{c3}) in Fig. 3.8 is changed from

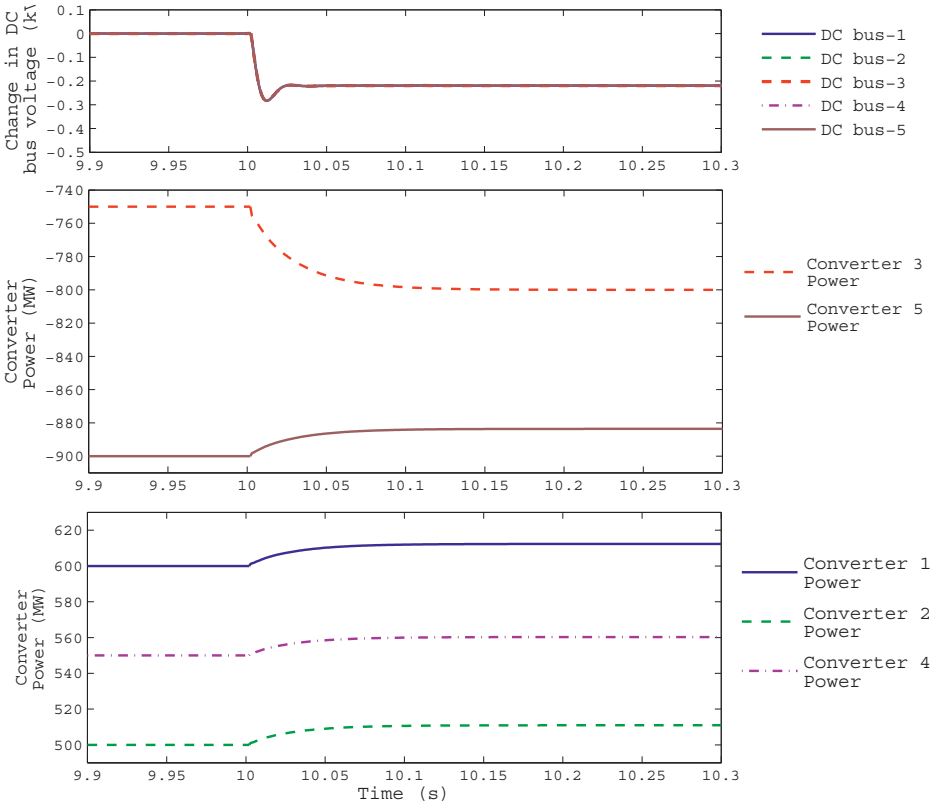


Figure 3.9: MTDC response to $\Delta P^*_{c3} = -50\,\text{MW}$ (with ideal dc grid model)

$-750\,\text{MW}$ to $-800\,\text{MW}$. This corresponds to $\Delta P^*_{c3} = -50\,\text{MW}$. The response of MTDC, when ideal dc grid is employed and after applying ΔP^*_{c3}, looks like Fig. 3.9. It is noticed that all terminals experience the same dc voltage change, as expected. It can be shown that the changes in nodal powers match very well with the estimation by equation (3.24).
When the MTDC has line resistances shown in Fig. 3.8, the response to the same step change (i.e. $\Delta P^*_{c3} = -50\,\text{MW}$) becomes as shown by Fig. 3.10. The primary

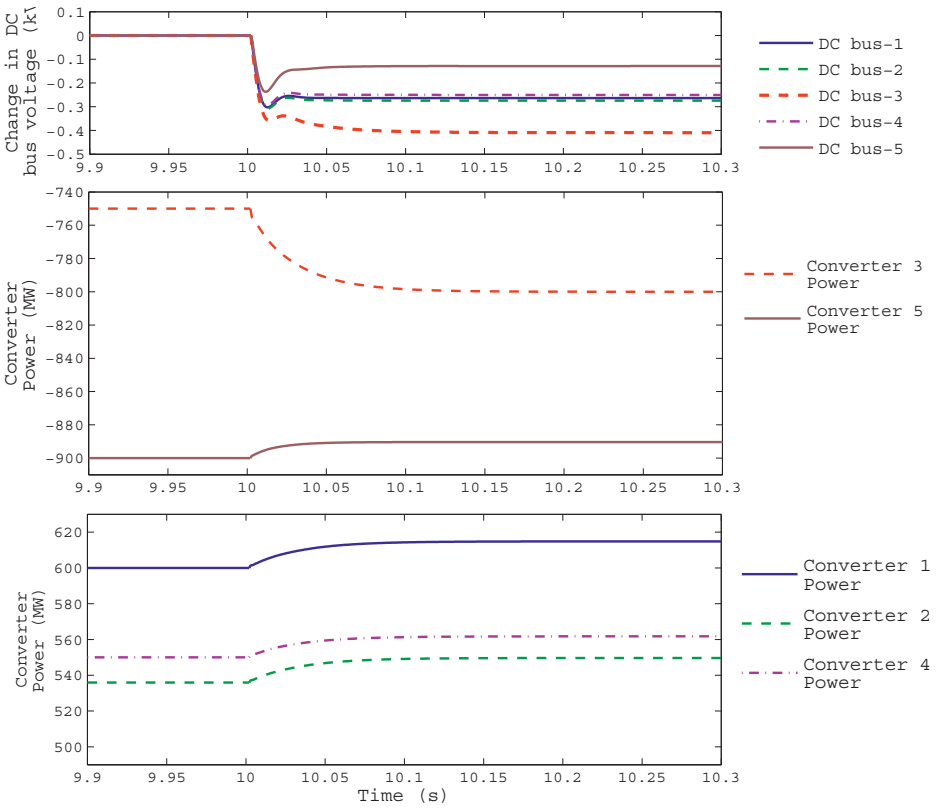


Figure 3.10: MTDC response to $\Delta P^*_{c3} = -50\,\text{MW}$ (with non-ideal dc grid model)

control response of the MTDC for ideal dc grid and non-ideal dc grid case are compared in Fig. 3.11. From the comparison it is clear that the dc line resistances result heavily influence the contributions of primary power balancing by participant converter units.

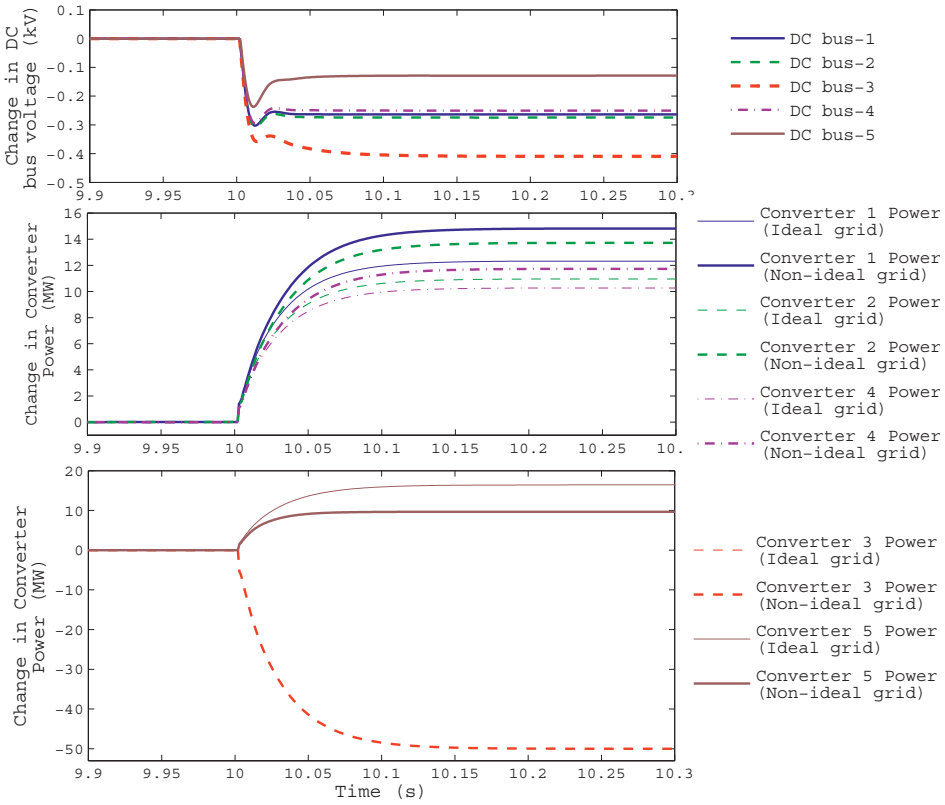


Figure 3.11: Comparison of MTDC responses with ideal dc grid and non-ideal dc grid

Let us now make numerical observations of the simulation results of the non-ideal dc grid. The numerical data of the non-ideal dc grid simulation results are shown in Table 3.20. After substituting $\Delta\mathbf{P}^* = \begin{bmatrix} 0 & 0 & -50 & 0 & 0 \end{bmatrix}'$ into (3.24) and (3.37) we find the estimated changes in power injections and dc-bus voltages using the ideal dc grid model approach (i.e. equation (3.24)) and non-ideal dc grid model approach (i.e. (3.37)). The estimations obtained are shown in Table 3.21. Simulation results for the ideal dc grid and non-ideal dc grid are compared in Fig. 3.11.

From Table 3.21 we can see that there are large differences in the results of the two power flow change estimation approaches (ideal dc grid model and non-ideal dc grid model). The ideal model predicts equal change in dc-bus voltage at all

Table 3.20: Simulation results for $\Delta P^*_{c3} = -50\,\text{MW}$

Terminal No.	U (kV)	P_c (MW)	ΔU (kV)	ΔP_c (MW)	P_{cN} MW)	$\frac{\Delta P_c}{P_{cN}}$ (pu/pu)
1	399.287	614.820	-0.2635	14.820	900	0.01647
2	399.726	549.651	-0.2745	13.723	800	0.01715
3	396.204	-800.00	-0.4092	-50.00	1000	-0.05000
4	396.677	561.746	-0.2505	11.741	750	0.01565
5	385.118	-890.33	-0.1289	9.666	1200	0.00806

Table 3.21: Estimated steady-state changes in nodal power and dc-bus voltage using ideal dc grid model and non-ideal dc grid model

Terminal No.	Estimation by ideal dc grid model, i.e. (3.20) & (3.24)			Estimation by non-ideal dc grid model, i.e. (3.36) & (3.39)		
	ΔU(kV)	ΔP_c(MW)	$\Delta P_c/P_{cN}$	ΔU(kV)	ΔP_c(MW)	$\Delta P_c/P_{cN}$
1	-0.2192	12.329	0.01370	-0.2633	14.813	0.01646
2	-0.2192	10.959	0.01370	-0.2743	13.716	0.01715
3	-0.2192	-50.000	0.05000	-0.4089	-50.000	0.05000
4	-0.2192	10.274	0.01370	-0.2504	11.736	0.01565
5	-0.2192	16.438	0.01370	-0.1289	9.664	0.00805

terminals while the more accurate estimation reveals large differences in dc-bus voltage variations. Moreover, the ideal dc grid model predicts the same changes in power flow measured in per-unit for all converters which have the same size of dc droop constant (ρ_{DC}). In the non-ideal grid estimation, we see that the terminal which observes the least change in dc-bus voltage experiences the least amount of change in power flow (among the converters which have equal dc voltage droop constants). This is most evident by comparing the per-unit balancing power contribution of terminal-5 (i.e. 0.00805 pu) and that of terminal-1 (i.e. 0.01646 pu). The corresponding change in dc voltage for terminal-5 is considerably smaller than the one experienced by terminal-1 (i.e. $-0.1289\,\text{kV}$ vs $-0.2633\,\text{kV}$)
Estimation errors of the two approaches are shown in Table 3.22 and Table 3.23.

The large estimation errors observed in Table 3.22 in the ideal dc grid model approach underpin the difference between frequency droop control of ac grids and dc voltage droop control of dc grids. The dc-bus voltages vary not only due to the dc droop characteristics of the local controllers but also due to changing power flow pattern in the dc network. The estimation errors shown in Table 3.23 come from the linearization of the power flow equations. The power flow linearization errors are generally small for a wide range of operating point. This contributes to the high

Table 3.22: Estimation errors of using ideal dc grid model (Equation (3.24))

Terminal No.	Lossless model (3.24)		PSCAD Simulation results		Estimation Errors	
	ΔU (kV)	ΔP_c (MW)	ΔU (kV)	ΔP_c (MW)	$\varepsilon(\Delta U)$ (%)	$\varepsilon(\Delta P_c)$ (%)
1	-0.2192	12.329	-0.2635	14.820	-16.81	-16.81
2	-0.2192	10.959	-0.2745	13.723	-20.15	-20.14
3	-0.2192	-50.000	-0.4092	-50.00	-46.43	0.000
4	-0.2192	10.274	-0.2505	11.741	-12.50	-12.50
5	-0.2192	16.438	-0.1289	9.6660	70.05	69.99

Table 3.23: Estimation errors of using non-ideal dc grid model (Equation (3.37))

Terminal No.	Lossy model (3.37)		PSCAD Simulation results		Estimation Errors	
	ΔU (kV)	ΔP_c (MW)	ΔU (kV)	ΔP_c (MW)	$\varepsilon(\Delta U)$ (%)	$\varepsilon(\Delta P_c)$ (%)
1	-0.2633	14.813	-0.2635	14.820	-0.076	-0.047
2	-0.2743	13.716	-0.2745	13.723	-0.073	-0.051
3	-0.4089	-50.000	-0.4092	-50.00	-0.049	0.000
4	-0.2504	11.736	-0.2505	11.741	-0.040	-0.051
5	-0.1289	9.664	-0.1289	9.6660	0.000	-0.031

accuracy of the proposed estimation method based on non-ideal dc grid model, as can be observed from the small estimation errors in Table 3.23.

The main cause of unequal per-unit contributions of balancing power is the unequal variations in the dc-bus voltages. The change in total dc line losses has little impact here. In fact if we sum up all the changes in nodal powers in Table 3.23, we get the change in sum total of the dc line losses in the entire dc grid. For the ideal dc grid this gives a sum total of zero, as one could expected, since there are no line losses in the system. For the non-ideal dc grid, however, the changes in nodal power add up to $-0.071\,\mathrm{MW}$, i.e. a very slight decrement in the total line losses. Comparing this with the applied change in reference (i.e. $\Delta P^*_{c3} = 50\,\mathrm{MW}$) we see that the *change in total of dc line losses* is negligible.

The impact of dc line resistances also means that the primary power balancing contributions in the dc grid depend on both the dc grid topology as well as the location where the original power surplus/deficit has occurred. Both of these phenomena are apparent by looking at the analytical expression of the steady-state interaction given by (3.37). The impact of the dc grid topology is reflected by the presence of the dc Jacobean matrix $\mathbf{J}_{DC}$ whereas the location at which the original change in

nodal power occurs is reflected in the positions of specific elements of the vector $\Delta\mathbf{P}^*$.

The conclusion is that dc line resistances and dc grid topology play essential roles in determining the distribution of primary balancing power in dc grids. This property is inherent to dc voltage droop control and makes the most significant distinction between dc voltage droop control and grid frequency control. Frequency change in ac grid is the same everywhere in the grid whereas dc voltage changes are different at various locations of a dc grid.

Some additional details of the impact of the dc grid topology on the steady-state interaction can be observed by looking closely at matrix $\mathbf{B}$ computed for the example dc grid under discussion:

$$\begin{bmatrix} \Delta P_{c1} \\ \Delta P_{c2} \\ \Delta P_{c3} \\ \Delta P_{c4} \\ \Delta P_{c5} \end{bmatrix} = \underbrace{\begin{bmatrix} 0.6509 & -0.2906 & -0.2963 & -0.2503 & -0.1327 \\ -0.2586 & 0.6515 & -0.2743 & -0.2038 & -0.1081 \\ 0.0000 & 0.0000 & 1.0000 & 0.0000 & 0.0000 \\ -0.2072 & -0.1896 & -0.2347 & 0.7049 & -0.1565 \\ -0.1706 & -0.1561 & -0.1933 & -0.2430 & 0.3702 \end{bmatrix}}_{\mathbf{B}} \begin{bmatrix} \Delta P^*_{c1} \\ \Delta P^*_{c2} \\ \Delta P^*_{c3} \\ \Delta P^*_{c4} \\ \Delta P^*_{c5} \end{bmatrix} \tag{3.45}$$

The cross diagonal terms in the matrix $\mathbf{B}$ of (3.45) indicate the interactions between the change in power reference of a specific terminal and the resulting change in injected power at other terminals. For example the elements in the first row of $\mathbf{B}$ indicate the sensitivity of the nodal power at terminal-1 with respect to changes in power reference at different VSC-HVDC terminals. The diagonal terms in the matrix are always positive and each diagonal element has the highest magnitude in the respective row. This is a reflection of the fact that power flow at any terminal is affected principally by the power reference at the same terminal and that the two are positively correlated. On the other hand, the rest of the elements in the row (i.e. the off-diagonal elements) have minus sign which indicate that power flow at one terminal is negatively correlated to the power reference of other terminals. One noticeable feature observed in (3.45) matrix is that $\mathbf{B}$ is diagonally asymmetric. If for example we increase the power reference P^*_{c1} by 1 MW, terminal-2 will respond by decreasing the power injected into the dc grid by 0.2586 MW. If instead we increase P^*_{c2} by 1 MW, however, terminal-1 will respond by decreasing the injected power by 0.2906 MW. This implies that terminal-1 is more sensitive to change in power reference occurring at terminal-2 than vice versa. It is also clear from (3.45) that terminal-3 (i.e. the terminal with constant power control mode) responds only to a non-zero value of ΔP^*_{c3}. From the matrix $\mathbf{B}$, it is possible to extract some information about marginal (incremental) transmission losses in the dc grid. To explain this, let us consider the generalized relation in (3.46) for an n terminal dc

grid:

$$\begin{bmatrix} \Delta P_{c1} \\ \vdots \\ \Delta P_{ci} \\ \vdots \\ \Delta P_{cn} \end{bmatrix} = \underbrace{\begin{bmatrix} S_{11} & \cdots & S_{1i} & \cdots & S_{1n} \\ \vdots & \ddots & \vdots & \ddots & \vdots \\ S_{i1} & \cdots & S_{ii} & \cdots & S_{in} \\ \vdots & \ddots & \vdots & \ddots & \vdots \\ S_{n1} & \cdots & S_{ni} & \cdots & S_{nn} \end{bmatrix}}_{\mathbf{B}} \begin{bmatrix} \Delta P^*_{c1} \\ \vdots \\ \Delta P^*_{ci} \\ \vdots \\ \Delta P^*_{cn} \end{bmatrix} \tag{3.46}$$

In (3.46), S_{ij} refers to the sensitivity of nodal power injection at terminal-i to the parameter ΔP^*_{cj}. It was discussed previously that the sum total of all nodal power injections gives the total transmission losses in the entire dc grid (i.e. $\Delta P_{DC-losses}$). This is mathematically given as

$$\Delta P_{DC-losses} = \sum_{i=1}^{n} \Delta P_{ci} \tag{3.47}$$

Hence combining (3.46) and (3.47), the total change in dc line losses, as a result of all the changes in power references, is expressed as

$$\Delta P_{DC,losses} = \sum_{i=1}^{n} \Delta P_{ci} = \sum_{j=1}^{n} \sum_{i=1}^{n} S_{ij} \Delta P^*_{cj} = \sum_{j=1}^{n} \left(\Delta P^*_{cj} \sum_{i=1}^{n} S_{ij} \right) \tag{3.48}$$

Now let us consider a non-zero change in power reference ΔP^*_{cj}, while keeping all the other power references unchanged ($\Delta {P_{ci}}^* = 0,\ i \in \left\{ \begin{array}{cccc} 1 & \cdots & n \end{array} \right\}, i \neq j$). The corresponding change in dc grid losses is

$$\Delta P_{DC-losses} = \Delta P^*_{cj} \sum_{i=1}^{n} S_{ij} \tag{3.49}$$

Hence, the sensitivity of total dc grid losses with respect to the parameter ΔP^*_{cj} is

$$\frac{\Delta P_{DC-losses}}{\Delta P^*_{cj}} = \sum_{i=1}^{n} S_{ij} \tag{3.50}$$

The relation in (3.50) indicates by how much the total dc line losses increase/decrease for a unit change in the power reference of terminal-j (ΔP^*_{cj}). Even more interesting is to know the 'cost' in terms of dc losses of injecting an additional unit power at terminal-j (ΔP_{cj}). It is necessary to keep in mind that the change in power reference (ΔP^*_{cj}) and the corresponding change in nodal power of terminal-j (ΔP_{cj}) are always different unless the terminal under consideration is in constant power control mode. From (3.46), we get $\Delta P_{cj} = S_{jj} \Delta P^*_{cj}$. The additional dc line losses incurred by increasing the power injection at terminal-j by ΔP_{cj} (which in turn is achieved by

increasing P^*_{cj} by an amount equal to ΔP^*_{cj}) is given by (3.48). Hence the ratio of the additional line losses to the incremental power injection at terminal-j is described as

$$\gamma_{marg,j} = \frac{\Delta P_{DC-losses}}{\Delta P_{cj}} = \frac{\Delta P^*_{cj} \sum_{i=1}^{n} S_{ij}}{\Delta P^*_{cj} S_{jj}} = \frac{\sum_{i=1}^{n} S_{ij}}{S_{jj}} \tag{3.51}$$

Equation (3.51) indicates the marginal dc loss ratio, $\gamma_{marg,j}$, (i.e. ratio of increment in total dc line losses to increment in injected power at terminal-j). If the marginal dc loss ratio is positive, it means that the total dc line losses will increase with larger injected power at terminal-j whereas if this ratio is negative, this means that a unit increment in injected power at terminal-j will result in decrement of the total dc line losses. Since the sensitivity matrix is computed for a specific steady-state operating point, the marginal dc loss ratio also changes with the operating point. For example in the case of the dc grid scenario shown in Fig. 3.8 and for the initial steady-state operating point described by Table 3.19, the marginal dc loss ratios of all the five terminals are computed from (3.45), (3.46) and (3.51). Table 3.24 shows the complete list.

Table 3.24: Marginal dc loss ratios for various terminals in the dc grid

Terminal No. (j)	1	2	3	4	5
$\sum_{i=1}^{5} S_{ij}$	0.0145	0.0152	0.0014	0.0078	-0.0271
S_{jj}	0.6509	0.6515	1.0000	0.7049	0.3702
$\gamma_{marg,j}$	0.0223	0.0233	0.0014	0.0111	-0.0732

From Table 3.24 , it is observed that the terminals 1 to 4 have positive marginal dc loss ratios, meaning a positive increment in power references at these terminals results in increased dc line losses. Terminal-5 on the other hand has negative value of marginal dc loss ratio implying that a positive increment in power reference at this terminal leads to lower aggregate dc line losses. Since this terminal is already in inverter mode of operation (i.e. taking away power from the dc grid into the ac grid), a positive increment in power reference implies a decrement in the amount of the power conversion from dc to ac. A more direct interpretation of the marginal dc for this particular terminal is as follows: a further increment in dc grid to ac grid power transfer at terminal-5 by 1 MW results in a dc line loss increment of 0.0732 MW. This can also be understood intuitively by following the notion that more power flow results in more transmission losses. It can also be seen that terminals 1, 2 and 4 also result in increased dc line losses when the power injections at these terminals are increased. Since these terminals are initially operated in rectifier mode, here

too intuition can be used to explain why the losses increase with increasing injected power at these terminals. The marginal dc loss ratio of terminal-3, however, may not be explained by the same intuition as in the previous cases. This is because this terminal, despite being initially operated in inverter mode of operation, has a positive value of marginal dc loss ratio. This means that further increment in dc-to-ac power transfer at terminal-3 leads to a reduction in aggregate dc line losses. This phenomenon can also be corroborated by looking at the simulation results in Table 3.20, where a change of $P^*_{c3} = -50$MW resulted in a total change in dc line losses of -0.066 MW. This corresponds to marginal dc loss ratio of $\gamma_{marg,3} = -0.066/-50 = 0.00132$ - which in turn is close to the one shown in Table 3.24 (third row,third column). This may look counter intuitive since we might expect an increase in dc losses with further increment of the dc-to-ac power flow at terminal-3. The explanation for this is as follows. When terminal-3 draws more power from the dc grid, the dc-bus voltages at various terminals decrease and as a result each of the converters equipped with dc voltage droop controllers (i.e. terminals 1, 2, 4 and 5) responds by providing a net positive increment in power flow into the dc grid. For terminals 1, 2 and 4 this is achieved by increasing their ac-to-dc power flow further. Terminal-5, however, responds by decreasing its dc-to-ac power flow so that the net change in power flow for this terminal becomes a positive power flow from AC-to-DC. By freeing up some of the dc-to-ac power flow at terminal-5, considerable amount of dc line losses are reduced (i.e. a reduction of 0.0732 MW of dc losses for each 1 MW given up by terminal-5). Hence, when terminal-3 takes away more power from the dc grid, the resulting total dc loss increment due to larger power flow at terminals 1, 2, 3 and 4 is exceeded by the total dc loss decrement due to the power given up by terminal-5.

The sensitivity relationship derived can be expanded so as to include changes in dc voltage references, in which case we re-write (3.35) as

$$\left.\begin{aligned} \Delta\mathbf{P}_c &= \Delta\mathbf{P}_c{}^* - \mathrm{diag}\left(\mathbf{R}_{DC}\right)\left(\Delta\mathbf{U} - \Delta\mathbf{U}^*\right) \\ &= \boldsymbol{\Delta}\mathbf{P}_c{}^* + \mathrm{diag}\left(\mathbf{R}_{DC}\right)\Delta\mathbf{U}^* - \mathrm{diag}\left(\mathbf{R}_{DC}\right)\Delta\mathbf{U} \end{aligned}\right\} \tag{3.52}$$

Substituting (3.30) into (3.52) we get

$$\left(\mathbf{J}_{DC} + \mathrm{diag}\left(\mathbf{R}_{DC}\right)\right)\Delta\mathbf{U} = \Delta\mathbf{R}^*_{DC} + \mathrm{diag}\left(\mathbf{R}_{DC}\right)\Delta\mathbf{U}^* \tag{3.53}$$

From (3.53), sensitivity relationship between dc-bus voltage vector ($\boldsymbol{\Delta}\mathbf{U}$) and the dc voltage reference vector ($\Delta\mathbf{U}^*$) is expressed as

$$\Delta\mathbf{U} = \left(\mathbf{J}_{DC} + \mathrm{diag}\left(\mathbf{R}_{DC}\right)\right)^{-1}\mathrm{diag}\left(\mathbf{R}_{DC}\right)\Delta\mathbf{U}^* \tag{3.54}$$

Similarly, sensitivity of nodal power injections with respect to dc voltage references is expressed by

$$\left.\begin{aligned}\Delta\mathbf{P} = \mathbf{J}_{DC}\Delta\mathbf{U} &= \underbrace{\mathbf{J}_{DC}(\mathbf{J}_{DC} + \operatorname{diag}(\mathbf{R}_{DC}))^{-1}}_{\mathbf{B}} \operatorname{diag}(\mathbf{R}_{DC})\,\Delta\mathbf{U}^{*} \\ &= \mathbf{B}\operatorname{diag}(\mathbf{R}_{DC})\,\Delta\mathbf{U}^{*}\end{aligned}\right\} \tag{3.55}$$

An expanded form of (3.55) is

$$\begin{bmatrix} \Delta P_{c1} \\ \vdots \\ \Delta P_{ci} \\ \vdots \\ \Delta P_{cn} \end{bmatrix} = \underbrace{\begin{bmatrix} N_{11} & \cdots & N_{1i} & \cdots & N_{1n} \\ \vdots & \ddots & \vdots & \ddots & \vdots \\ N_{i1} & \cdots & N_{ii} & \cdots & N_{in} \\ \vdots & \ddots & \vdots & \ddots & \vdots \\ N_{n1} & \cdots & N_{ni} & \cdots & N_{nn} \end{bmatrix}}_{\mathbf{N}} \begin{bmatrix} \Delta U_1^{*} \\ \vdots \\ \Delta U_i^{*} \\ \vdots \\ \Delta U_n^{*} \end{bmatrix} \tag{3.56}$$

The total dc line losses due to all changes in dc voltage references is given by

$$\Delta P_{DC-losses} = \sum_{i=1}^{n} \Delta P_{ci} = \sum_{j=1}^{n}\sum_{i=1}^{n} N_{ij}\Delta U_j^{*} = \sum_{j=1}^{n}\left(\Delta U_j^{*}\sum_{i=1}^{n} N_{ij}\right) \tag{3.57}$$

Now let us consider the case where all the dc voltage references are increased by the same amount $\Delta {U_j}^{*} = \Delta U,\ \ j \in \left\{\ 1\ \ \cdots\ \ n\ \right\}$. The corresponding increase in total dc line losses becomes

$$\left.\begin{aligned}\Delta P_{DC-losses} &= \sum_{j=1}^{n}\left(\Delta U_j^{*}\sum_{i=1}^{n} N_{ij}\right) \\ &= \Delta U^{*}\sum_{j=1}^{n}\sum_{i=1}^{n} N_{ij}\end{aligned}\right\} \tag{3.58}$$

Hence the change in aggregate dc line losses due to a unit increment in dc voltage reference of all VSC-HVDC terminals is expressed as

$$\frac{\Delta P_{DC-losses}}{\Delta U^{*}} = \sum_{j=1}^{n}\sum_{i=1}^{n} N_{ij} \tag{3.59}$$

In the five-terminal dc grid example case, substitution of the relevant parameters into (3.55) gives

$$\mathbf{N} = \begin{bmatrix} 36.6106 & -14.5315 & 00.0000 & -11.7339 & -09.9550 \\ -14.5479 & 32.5745 & 00.0000 & -09.5542 & -08.1058 \\ 00.0000 & 00.0000 & 00.0000 & 00.0000 & 00.0000 \\ -11.6569 & -09.4808 & 00.0000 & 33.0400 & -11.7376 \\ -09.5987 & -07.8069 & 00.0000 & -11.3922 & 27.7630 \end{bmatrix} \frac{\text{MW}}{\text{kV}} \tag{3.60}$$

The sum of all elements of the matrix $\mathbf{N}$ in (3.60), gives $-0.1131\,\text{MW/kV}$ which means the total dc grid losses will decrease by $-0.1131\,\text{MW}$ if all the dc voltage references are increased by 1 kV. To compare this prediction with simulation result, a change of 1 kV was applied to all VSC-HVDC terminals of Fig. 3.8 with the initial condition stated by Table 3.19. The resulting changes in dc voltage and power injections are shown in Table 3.25.

Table 3.25: Impact of increasing nominal dc voltage by 1 kV

Terminal	Initial		Final		Change	
No.	U(kV)	P_c(MW)	U(kV)	P_c(MW)	ΔU(kV)	ΔP_c(MW)
1	399.550	600.000	400.545	600.253	0.871	0.253
2	400.000	535.928	400.995	536.183	0.828	0.255
3	396.613	-750.00	397.615	-750.00	0.872	0.000
4	396.928	550.005	397.928	550.014	0.903	0.009
5	385.247	-900.00	386.269	-900.651	0.972	-0.651

From Table 3.25 the change in total dc line losses is $\sum_{i=1}^{5} \Delta P_{ci} = -0.134\,\text{MW}$, which is in good agreement with the estimated value of $-0.1131\,\text{MW}$ obtained from (3.58).

3.3.3 Effect of Scaling the DC Droop Constant

In chapter 2 it was discussed that the dc droop constant ρ_{DC} and dc voltage response R_{DC} are inversely related. Hence here we will simply look at the impact of scaling up/down $\mathbf{R}_{DC}$ on the primary balancing power distribution. In order to do so let us see how the matrix $\mathbf{B}$ changes with changing the vector $\mathbf{R}_{DC}$. Let $\mathbf{R^o}_{DC}$ represent the original dc voltage response vector. Consider a scaling factor m such that a new dc voltage response $\mathbf{R'}_{DC}$ is given by

$$\mathbf{R}' = m\mathbf{R^o} \tag{3.61}$$

The new aggregate dc voltage response $R'_{DC,agg}$ becomes

$$R'_{DC,agg} = \sum_{i=1}^{5} mR^o_{DC} = m\sum_{i=1}^{5} R^o_{DC} = R^o_{DC,agg} \tag{3.62}$$

From equation (3.61) and the definition of $\mathbf{B}$ in (3.55), we get

$$\mathbf{B}^o = \left(\mathbf{I} + \text{diag}\left(\mathbf{R}^o\right)\mathbf{J}_{DC}{}^{-1}\right)^{-1} \tag{3.63}$$

$$\mathbf{B}' = \left(\mathbf{I} + \mathrm{diag}\left(\mathbf{R}^o\right) \mathbf{J}_{DC}{}^{-1} m\right)^{-1} \tag{3.64}$$

where $\mathbf{I}$ is identity matrix. Equation (3.64) shows that the scaling factor m determines the impact of the dc line resistances on the sensitivity of nodal power injection to corresponding power references. At the same time, the analytical estimation based on the ideal dc grid model does not reveal any difference by changing the scaling factor m. This is evident from comparison of $\mathbf{A}^o$ and $\mathbf{A}'$ as

$$\mathbf{A}' = \begin{bmatrix} 1 - \frac{mR^o_{DC1}}{mR^o_{DC,agg}} & \cdots & -\frac{mR^o_{DC1}}{mR^o_{DC,agg}} & \cdots & -\frac{mR^o_{DC1}}{mR^o_{DC,agg}} \\ \vdots & \ddots & \vdots & \ddots & \vdots \\ -\frac{mR^o_{DCj}}{mR^o_{DC,agg}} & \cdots & 1 - \frac{mR^o_{DCj}}{mR^o_{DC,agg}} & \cdots & -\frac{mR^o_{DCj}}{mR^o_{DC,agg}} \\ \vdots & \ddots & \vdots & \ddots & \vdots \\ -\frac{mR^o_{DCn}}{mR^o_{DC,agg}} & \cdots & -\frac{mR^o_{DCn}}{mR^o_{DC,agg}} & \cdots & 1 - \frac{mR^o_{DCn}}{mR^o_{DC,agg}} \end{bmatrix} = \mathbf{A}^o \tag{3.65}$$

In Table 3.26 the changes in nodal powers are shown for $\Delta\mathbf{P}^* = \begin{bmatrix} 0 & 0 & 250 & 0 & 0 \end{bmatrix}'$ and for different values of m.

Table 3.26: Influence of the dc droop scaling factor on balancing power distribution

Terminal No.	ΔP_c (MW)			
	Estimated by ideal model (3.24)	Simulation results (of Fig. 3.8)		
	For all m	$m = 0.5$	$m = 1$	$m = 2$
1	-61.644	-69.622	-73.979	-78.213
2	-54.795	-63.474	-68.444	-73.792
3	250.000	250.000	250.000	250.000
4	-51.370	-55.644	-58.614	-62.638
5	-82.192	-60.695	-48.442	-34.873

The simulation results shown in Table 3.26 reveal that as scaling factor m increases, the primary control response of the system deviates further from the estimation by the ideal dc grid modeling approach. The conclusion is that larger values of m (and hence lower values of dc voltage droop constants) tend to amplify the impact of dc grid topology on primary control response of the dc grid. If the dc droop constants are too small, the dc voltage response of the grid becomes too sensitive to the grid topology and if the droop constants are too large the dc voltage response becomes less affected by the dc grid topology. Large dc voltage droop constants, however, require larger range of operating dc voltage and hence can reduce the maximum power transfer capacity of converters at low dc voltage levels (due to maximum

direct current limitations). Hence selection of the appropriate dc droop constants becomes an optimization problem between these two constraints.

3.4 Thevenin Equivalent Circuit Approach for Studying Steady-state Interaction of MTDC

3.4.1 Propagation of ΔU in a Radial DC Network

In the previous section the steady-state interactions between various terminals of MTDC grid have been studied based on analytical approach (i.e. linearization of the load flow equations). Here we will discuss an alternative proposed approach to study the steady-state interactions based on Thevenin equivalent modeling of individual VSC-HVDC terminals. The proposed approach enables to model an MTDC transmission system with relatively simple resistive network (without including controllers and the detailed model of VSC). From the model the steady-state interaction of the dc grid can be studied by observing the effects of injecting currents at various nodes of the dc network.
In order to get an intuitive understanding of the impact of dc line voltage drops on dc voltage droop control, let us consider the three-terminal dc grid shown in Fig. 3.12. r_{12} and r_{23} are dc line resistances and ΔU_1, ΔU_2, and ΔU_3 are changes in

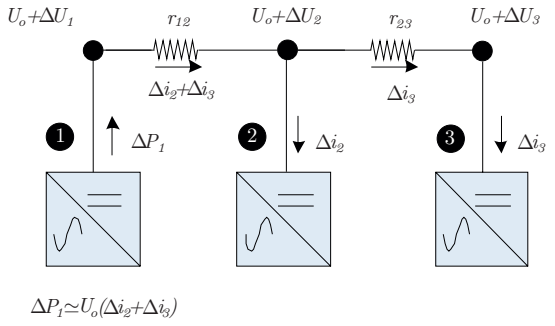


Figure 3.12: A radial three-terminal VSC-HVDC system

terminal (dc-bus) voltages due to power injection ΔP_{c1} at dc-bus 1. In order to inject the power ΔP_{c1}, the voltage at bus-1 must be raised from U_o to $U_o + \Delta U_1$. Due to the line resistances, however, the resulting changes in voltage at terminal-2

and terminal-3 will be smaller:

$$\left.\begin{aligned} \Delta U_2 &= \Delta U_1 - (\Delta i_2 + \Delta i_3)\, r_{12} \\ \Delta U_2 &= \Delta U_1 - (\Delta i_2 + \Delta i_3)\, r_{12} - (\Delta i_2)\, r_{23} \end{aligned}\right\} \tag{3.66}$$

From (3.66) it can be seen that as the location of dc voltage measurement gets further away from dc-bus 1 (i.e. from the location where the change in power flow has initially occurred), the observed change in dc voltage decreases. Hence for example if terminals-2 and 3 have equal power ratings and equal dc droop constants, terminal-2 will be forced to contribute a slightly larger share of the balancing power.

3.4.2 Dynamic Output Impedance of VSC-HVDC Terminals

Depending on the employed control schemes, VSC-HVDC terminals exhibit different dynamic output impedances. Dynamic output impedance R_o is an important element in modeling small-signal equivalent circuit of the dc grid including the converter terminals. Dynamic output impedance of a VSC-HVDC terminal is defined as

$$\left.\begin{aligned} R_o &= \tfrac{\Delta U}{\Delta I_{DC}} = \tfrac{\Delta U}{\Delta P_c/U} \\ &= U \tfrac{U_N}{P_{cN}} \left(\tfrac{\Delta U/U_N}{\Delta P_c/P_{cN}} \right) \\ &\approx \rho_{DC} \tfrac{U_N^2}{P_{cN}} = \tfrac{U_N}{R_{DC}} \end{aligned}\right\} \tag{3.67}$$

where U_N and P_{cN} refer to rated dc voltage and rated power capacity of the converter station. From (3.67), it can be seen that the dynamic output impedance of a converter station increases with decreasing power rating (P_{cN}) and with increasing dc droop constant (ρ_{DC}). A constant power terminal has a droop constant of ∞, the corresponding dynamic output impedance is ∞ (an open circuit). Likewise a terminal with constant dc voltage control has dc droop constant of zero, resulting in dynamic output impedance of 0 (a short circuit). In Fig. 3.13 representations of dynamic output impedances of converters in different control modes are shown.

3.4.3 Mutual Impedances and Propagation of ΔU

The three-terminal VSC-HVDC transmission shown in Fig. 3.12 can be represented by the small-signal model shown in Fig. 3.14. R_{o2} and R_{o3} represent the dynamic output impedances of the converters at terminal-2 and terminal-3 respectively. Changes

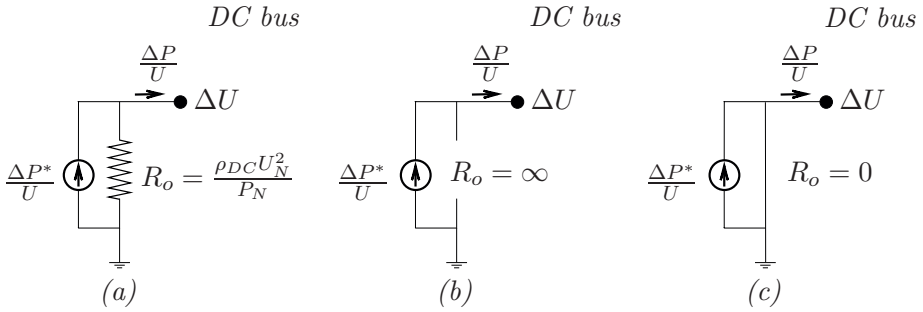


Figure 3.13: Dynamic output resistances of VSC-HVDC with: (a) droop controller (b) constant power controller (c) dc voltage regulator

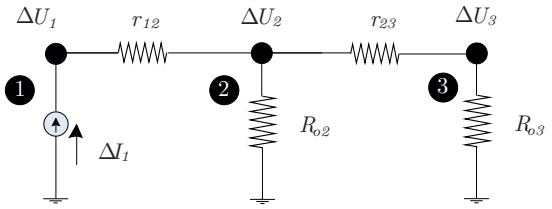


Figure 3.14: Small-signal equivalent circuit of the three-terminal VSC-HVDC in Fig. 3.12

in voltage at dc-bus 2 and 3 are computed as

$$\left.\begin{aligned} \Delta U_2 &= \tfrac{(R_{o3}+r_{23})R_{o2}}{R_{o2}+R_{o3}+r_{23}} I_1 \\ \Delta U_3 &= \tfrac{R_{o2}R_{o3}}{R_{o2}+R_{o3}+r_{23}} I_1 \end{aligned}\right\} \tag{3.68}$$

The ratio of ΔU_2 to ΔI_1 represents the mutual impedance between bus-2 and bus-1. Similarly the mutual impedance between bus-3 and bus-1 is given as the ratio of ΔU_3 to ΔI_1. The mutual impedance relationships are given by (3.69).

$$\left.\begin{aligned} Z_{12} = Z_{21} &= \tfrac{(R_{o3}+r_{23})R_{o2}}{R_{o2}+R_{o3}+r_{23}} \\ Z_{13} = Z_{31} &= \tfrac{R_{o2}R_{o3}}{R_{o2}+R_{o3}+r_{23}} \end{aligned}\right\} \tag{3.69}$$

In general, the mutual impedance between two nodes i and j is given by

$$Z_{ij} = Z_{ji} = \frac{U_i}{I_j} \tag{3.70}$$

where I_j is current injected at node j and U_i is the voltage observed at node i due to the current injection at node j. The voltage at node j due to the current injection I_j is

$$U_j = Z_{jj} I_j \tag{3.71}$$

where Z_{jj} is self impedance at node j. Hence from (3.70) and (3.71), we get

$$U_i = \frac{Z_{ij}}{Z_{jj}} U_j \tag{3.72}$$

Equation (3.72) shows that larger mutual impedances imply stronger propagations of changes in voltage from one side to the other. In the case of multi-terminal VSC-HVDC, this implies that VSC-HVDC terminals which have larger mutual impedances with respect to the location of power deficit/ surplus will contribute larger shares of balancing power in per-unit. In the case of simple, small circuits (for example as in the case of Fig. 3.12) mutual impedances can be found analytically without much difficulty. In the case of larger and complex networks however, it will be a very tedious task to compute the mutual impedances analytically. A suitable alternative is to use current injection method, where a dc current of known magnitude is injected at the desired node and the resulting nodal voltages are observed. From the nodal voltages and the injected current, the mutual impedances are computed by (3.70). A schematic of this procedure is shown in Fig. 3.15. The

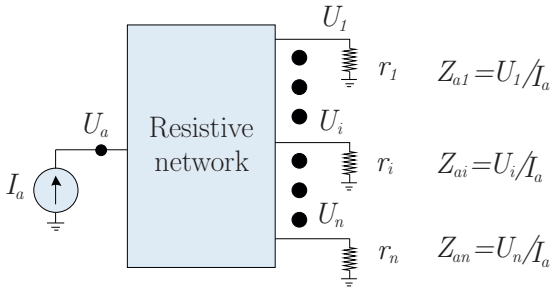


Figure 3.15: Computing mutual impedances by current injection method

small-signal equivalent circuit of the five-terminal VSC-HVDC (shown in Fig. 3.2) is given by Fig. 3.16. To compute the mutual impedance between terminal-3 and the other nodes, a current injection of $\Delta I_3 = \frac{\Delta P^*_{c3}}{U} = \frac{-50}{400} = -0.125\,\text{kA}$ is put in place of the dynamic output impedance R_{o3}. (This current is chosen deliberately to compare the resulting changes in dc-bus voltages with the observed ones from the detailed simulation in Table 3.20) The resulting nodal voltages are shown in the same figure. The mutual impedances are listed in Table 3.27. The changes in nodal power, after

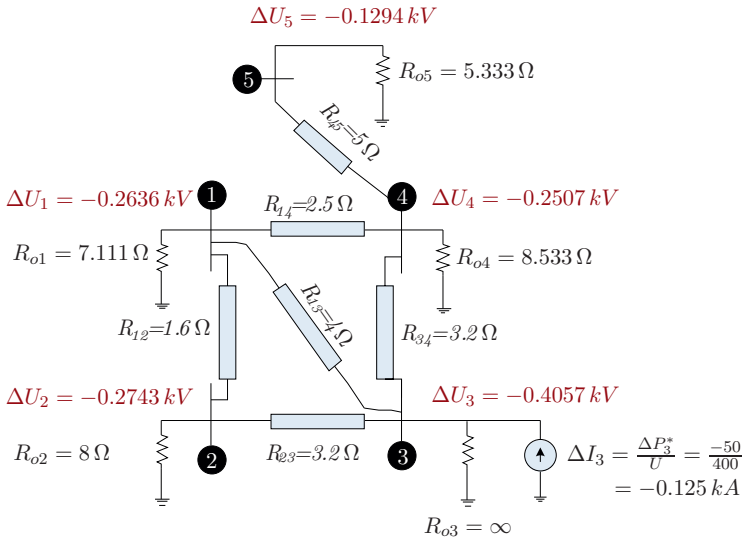


Figure 3.16: Mutual impedance between node-3 and other nodes

Table 3.27: Mutual impedances and primary balancing power distribution

Mutual Impedance (Ω)	ΔU (kV)	ΔP_c (MW)	$\Delta P_{c,pu}$ (pu)
$Z_{33} = 3.2456$	-0.409	-50.000	-0.0500
$Z_{32} = 2.1944$	-0.274	13.716	0.01715
$Z_{31} = 2.1088$	-0.263	14.813	0.01647
$Z_{34} = 2.0056$	-0.251	11.736	0.01565
$Z_{35} = 1.0352$	-0.129	9.664	0.00806

applying $\Delta P_{c3}^* = -50\,\text{MW}$, are also included (see Table 3.20). From Table 3.27 it is evident that the largest mutual impedance is between nodes 3 and 2 and hence terminal-2 contributed the largest amount of balancing power in per-unit. Similarly the smallest mutual impedance occurs between nodes 3 and 5 and this corresponds to the least per-unit contribution of balancing power as can be seen on the right column of the table. From the simulation results of the Thevenin equivalent dc grid modeling, it can be seen that the changes in dc-bus voltages match very well with the corresponding changes in dc-bus voltages observed from the dc grid model containing full VSC models.
The conclusion is that the knowledge of mutual impedances between different nodes

enables us to know which of the converters will respond strongly to power flow changes at a specific node in the dc grid.

3.5 Steady-state AC/DC Interactions in Primary Control

In section 2.6 we have seen that VSC-HVDC can be used to enhance the frequency response of ac grids. Since a VSC-HVDC terminal has the possibility of responding to dc voltage variations (by means of dc voltage droop control) and/or to frequency variations (by means of frequency droop control) the load-frequency interaction in one ac grid will affect other asynchronous ac grids connected to a common MTDC grid. In this section we will try to quantify the steady-state load-frequency interaction in the presence of MTDC interconnection. We will first analyze an interconnection where each VSC-HVDC terminal is connected to a unique ac grid and later on we will proceed to a general ac/dc interconnection topology where some of the VSC-HVDC terminals may be connected to the same ac grid.
In Fig. 3.17 an n-terminal dc network is connected to n-number of separate ac grids. The variables in Fig. 3.17 are defined in Table 3.28.

Table 3.28: Description of the variables shown in Fig. 3.17

Variable	Description	Unit
P_{gN}	Total generation capacity of ac grid	MW
R_g	Frequency response of ac grid	MW/Hz
P_g	Total generated power	MW
P_L	Total load power	MW
f	Grid frequency	Hz
P'_c	Ac to dc power flow via converter (measured from ac side)	MW
P_c	ac to dc power flow via converter (measured from dc side)	MW
P_{cN}	Power capacity of converter station	MW
R_{DC}	Dc voltage response of converter	MW/kV
R_f	Frequency response of converter	MW/kV
U	Dc-bus voltage	kV

From Fig. 3.17, the power balance relationship in ac grid i is given by

$$\Delta P_{gi} = \Delta P_{Li} + \Delta P'_{ci} \tag{3.73}$$

where P_{gi} and P_{Li} refer to total generated power and total load in ac grid-i. In

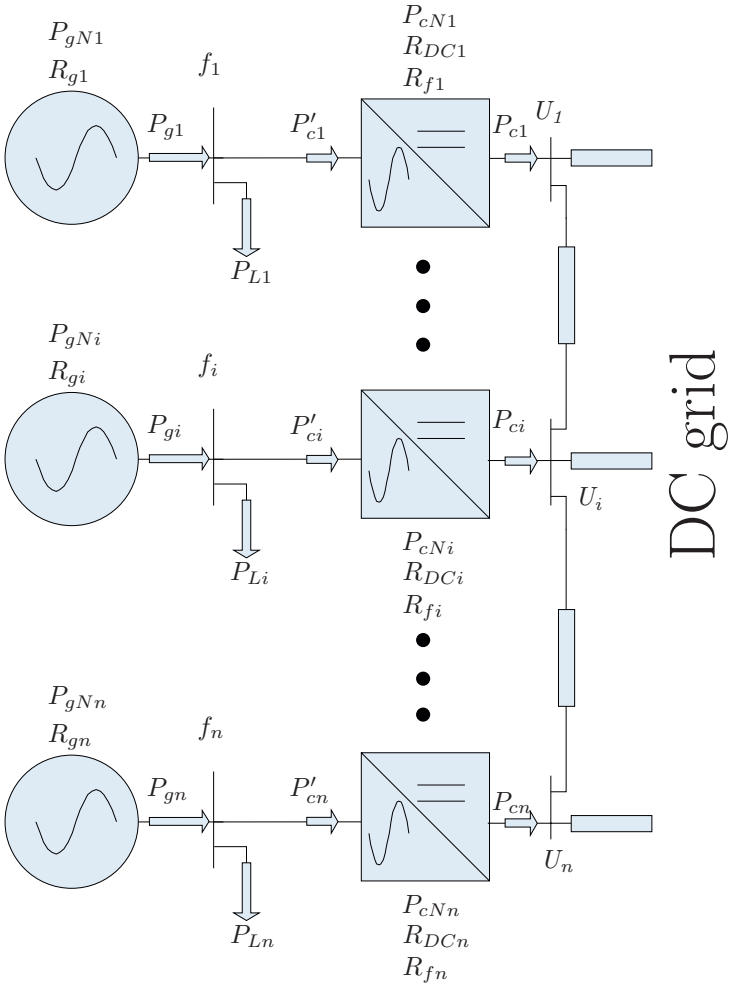


Figure 3.17: Ac/dc connection topology with each converter connected to a separate ac grid represented by a synchronous generator and a load

matrix/vector form (3.73) becomes.

$$\Delta \mathbf{P}_g = \Delta \mathbf{P}_L + \Delta \mathbf{P'}_c \tag{3.74}$$

Frequency droop relationship of ac grid i is described as

$$\Delta P_{gi} = \Delta {P_{gi}}^* - \Delta R_{gi} \Delta f_i \tag{3.75}$$

where ${P_{gi}}^*$ and R_{gi} refer to generation reference and frequency response constant of the aggregated ac grid-i. In matrix form (3.75) becomes

$$\Delta \mathbf{P}_g = \Delta {\mathbf{P}_g}^* - \text{diag}\left(\mathbf{R}_g\right) \Delta \mathbf{f} \tag{3.76}$$

where *diag* is matrix operator which converts a vector into a diagonal matrix.

The converter power input-output relationship for terminal-i is

$$\Delta P'_{ci} = \eta_i \Delta P_{ci} \tag{3.77}$$

where η_i is the (marginal) power conversion factor (compare with (3.7) in chapter 2). If the converter is in inverter mode of operation, *marginal power conversion efficiency* will be equal to η_i. On the other hand if the converter is in rectifier mode of operation, *marginal power conversion efficiency* will be equal to $1/\eta_i$. In matrix form (3.77) is re-written as

$$\Delta {\mathbf{P}'}_c = \text{diag}\left(\eta\right) \Delta \mathbf{P}_c \tag{3.78}$$

The steady-state expression of power flow control in converter-i is expressed as in (3.79). This assumes that the power measurement signal in the controller is taken from the dc-bus side. (See Fig. 3.6 for further details).

$$\Delta P_{ci} = \Delta {P_{ci}}^* + R_{fi} \Delta f_i - R_{DCi} \Delta U_i \tag{3.79}$$

In matrix form (3.79) is rewritten as (3.80 fro further explanations).

$$\Delta \mathbf{P}_c = \Delta {\mathbf{P}_c}^* + \text{diag}\left(\mathbf{R}_f\right) \Delta \mathbf{f} - \text{diag}\left(\mathbf{R}_{DC}\right) \Delta \mathbf{U} \tag{3.80}$$

Linearized power flow in the dc grid is expressed as follows (refer to section 3.3.2):

$$\Delta \mathbf{P}_c = \mathbf{J}_{DC} \Delta \mathbf{U} \tag{3.81}$$

From (3.81), the small-signal dc voltage vector ($\Delta \mathbf{U}$) is expressed as

$$\Delta \mathbf{U} = {\mathbf{J}_{DC}}^{-1} \Delta \mathbf{P}_c \tag{3.82}$$

Substituting (3.82) into (3.80) gives

$$\Delta \mathbf{P}_c = \underbrace{\left(\mathbf{I} + \text{diag}\left(\mathbf{R}_{DC}\right) {\mathbf{J}_{DC}}^{-1}\right)^{-1}}_{\mathbf{B}} \left(\Delta {\mathbf{P}_c}^* + \text{diag}\left(\mathbf{R}_f\right) \Delta \mathbf{f}\right) \tag{3.83}$$

There are two alternative approaches to compute the sensitivity matrix relating the vectors $\Delta {\mathbf{P}_g}^*$, $\Delta {\mathbf{P}_c}^*$ and $\Delta \mathbf{P}_L$ to the vectors $\Delta \mathbf{P}_g$, $\Delta \mathbf{P}_c$ and $\Delta \mathbf{f}$.

Approach 1:
Express $\Delta \mathbf{P}_g{}^*$, $\Delta \mathbf{P}_c{}^*$ and $\Delta \mathbf{P}_L$ in terms of the vectors $\Delta \mathbf{P}_g$, $\Delta \mathbf{P}_c$ and $\Delta \mathbf{f}$
From (3.76) vector $\Delta \mathbf{P}_g{}^*$ (power generation reference vector) is given as

$$\left.\begin{aligned} \Delta \mathbf{P}_g{}^* &= \Delta \mathbf{P}_g + \mathrm{diag}\,(\mathbf{R}_g)\,\Delta \mathbf{f} \\ &= \Delta \mathbf{P}_g + \mathbf{0}\Delta \mathbf{P}_c + \mathrm{diag}\,(\mathbf{R}_g)\,\Delta \mathbf{f} \end{aligned}\right\} \tag{3.84}$$

From (3.83) vector $\Delta \mathbf{P}_c{}^*$ (converter power reference vector) is given as

$$\left.\begin{aligned} \Delta \mathbf{P}_c{}^* &= \mathbf{B}^{-1}\Delta \mathbf{P}_c - \mathrm{diag}\,(\mathbf{R}_f)\,\Delta \mathbf{f} \\ &= \mathbf{0}\Delta \mathbf{P}_g + \mathbf{B}^{-1}\Delta \mathbf{P}_c - \mathrm{diag}\,(\mathbf{R}_f)\,\Delta \mathbf{f} \end{aligned}\right\} \tag{3.85}$$

From equations (3.74) and (3.78) vector $\Delta \mathbf{P}_L$ (load power vector) is expressed as

$$\left.\begin{aligned} \Delta \mathbf{P}_L &= \Delta \mathbf{P}_g - \Delta \mathbf{P'}_c \\ &= \Delta \mathbf{P}_g - \mathrm{diag}\,(\eta)\,\Delta \mathbf{P}_c + \mathbf{0}\Delta \mathbf{f} \end{aligned}\right\} \tag{3.86}$$

From (3.84), (3.85) and (3.86), we get

$$\left.\begin{aligned} \Delta \mathbf{P}_g{}^* &= \Delta \mathbf{P}_g + \mathbf{0}\Delta \mathbf{P}_c + \mathrm{diag}\,(\mathbf{R}_g)\,\Delta \mathbf{f} \\ \Delta \mathbf{P}_c{}^* &= \mathbf{0}\Delta \mathbf{P}_g + \mathbf{B}^{-1}\Delta \mathbf{P}_c - \mathrm{diag}\,(\mathbf{R}_f)\,\Delta \mathbf{f} \\ \Delta \mathbf{P}_L &= \Delta \mathbf{P}_g - \mathrm{diag}\,(\eta)\,\Delta \mathbf{P}_c + \mathbf{0}\Delta \mathbf{f} \end{aligned}\right\} \tag{3.87}$$

Equation (3.87) is rewritten as (3.88).

$$\begin{bmatrix} \Delta \mathbf{P}_g{}^* \\ \Delta \mathbf{P}_c{}^* \\ \Delta \mathbf{P}_L \end{bmatrix} = \begin{bmatrix} \mathbf{I} & \mathbf{0} & -\mathrm{diag}\,(\mathbf{R}_g) \\ \mathbf{0} & \mathbf{B}^{-1} & -\mathrm{diag}\,(\mathbf{R}_f) \\ \mathbf{I} & -\mathrm{diag}\,(\eta) & \mathbf{0} \end{bmatrix} \begin{bmatrix} \Delta \mathbf{P}_g \\ \Delta \mathbf{P}_c \\ \Delta \mathbf{f} \end{bmatrix} \tag{3.88}$$

From equation (3.88) we get

$$\begin{bmatrix} \Delta \mathbf{P}_g \\ \Delta \mathbf{P}_c \\ \Delta \mathbf{f} \end{bmatrix} = \underbrace{\begin{bmatrix} \mathbf{S}_{gg} & \mathbf{S}_{gc} & \mathbf{S}_{gL} \\ \mathbf{S}_{cg} & \mathbf{S}_{cc} & \mathbf{S}_{cL} \\ \mathbf{S}_{fg} & \mathbf{S}_{fc} & \mathbf{S}_{fL} \end{bmatrix}}_{\mathbf{S}} \begin{bmatrix} \Delta \mathbf{P}_g{}^* \\ \Delta \mathbf{P}_c{}^* \\ \Delta \mathbf{P}_L \end{bmatrix} \tag{3.89}$$

where the matrix $\mathbf{S}$ is given by

$$\mathbf{S} = \begin{bmatrix} \mathbf{S}_{gg} & \mathbf{S}_{gc} & \mathbf{S}_{gL} \\ \mathbf{S}_{cg} & \mathbf{S}_{cc} & \mathbf{S}_{cL} \\ \mathbf{S}_{fg} & \mathbf{S}_{fc} & \mathbf{S}_{fL} \end{bmatrix} = \begin{bmatrix} \mathbf{I} & \mathbf{0} & -\mathrm{diag}\,(\mathbf{R}_g) \\ \mathbf{0} & \mathbf{B}^{-1} & -\mathrm{diag}\,(\mathbf{R}_f) \\ \mathbf{I} & -\mathrm{diag}\,(\eta) & \mathbf{0} \end{bmatrix}^{-1} \tag{3.90}$$

The sub-matrix elements of $\mathbf{S}$ describe sensitivity matrices of output vectors ($\Delta\mathbf{P}_g$, $\Delta\mathbf{P}_c$ and $\Delta\mathbf{f}$) with respect to the different inputs ($\Delta{\mathbf{P}_g}^*$, $\Delta{\mathbf{P}_c}^*$ and $\Delta\mathbf{P}_L$). For example the sub matrix $\mathbf{S}_{fL}$ shows sensitivity of frequency vector ($\Delta\mathbf{f}$) with respect to load vector ($\Delta\mathbf{P}_L$).

Approach 2:
Express $\Delta\mathbf{P}_g$, $\Delta\mathbf{P}_c$ and $\Delta\mathbf{f}$ in terms of the vectors $\Delta{\mathbf{P}_g}^*$, $\Delta{\mathbf{P}_c}^*$ and $\Delta\mathbf{P}_L$
Substituting (3.76), (3.78) and (3.83) into (3.74) gives

$$\left.\begin{aligned}\Delta\mathbf{f} &= \underbrace{\left(\mathrm{diag}\left(\mathbf{R}_g\right)+\mathrm{diag}\left(\eta\right)\mathbf{B}\mathrm{diag}\left(\mathbf{R}_f\right)\right)^{-1}}_{\mathbf{D}}\left\{\Delta{\mathbf{P}_g}^*-\mathrm{diag}\left(\eta\right)\mathbf{B}\Delta{\mathbf{P}_c}^*-\Delta\mathbf{P}_L\right\}\\ &= \mathbf{D}\Delta{\mathbf{P}_g}^*-\mathbf{D}\mathrm{diag}\left(\eta\right)\mathbf{B}\Delta{\mathbf{P}_c}^*-\mathbf{D}\Delta\mathbf{P}_L\end{aligned}\right\} \tag{3.91}$$

Substituting (3.91) into (3.83) we get

$$\left.\begin{aligned}\Delta\mathbf{P}_c = \mathbf{B}\mathrm{diag}\left(\mathbf{R}_f\right)\mathbf{D}\Delta{\mathbf{P}_g}^*+\mathbf{B}\left(\mathbf{I}-\mathrm{diag}\left(\mathbf{R}_f\right)\mathbf{D}\mathrm{diag}\left(\eta\right)\mathbf{B}\right)\Delta{\mathbf{P}_c}^*\\ -\mathbf{B}\mathrm{diag}\left(\mathbf{R}_f\right)\mathbf{D}\Delta\mathbf{P}_L\end{aligned}\right\} \tag{3.92}$$

Substituting (3.92) into (3.86) results in

$$\left.\begin{aligned}\Delta\mathbf{P}_g = \left(\mathbf{I}-\mathrm{diag}\left(\eta\right)\mathbf{B}\mathrm{diag}\left(\mathbf{R}_f\right)\mathbf{D}\right)\Delta\mathbf{P}_L+\mathrm{diag}\left(\eta\right)\mathbf{B}\mathrm{diag}\left(\mathbf{R}_f\right)\mathbf{D}\Delta{\mathbf{P}_g}^*\\ +\mathrm{diag}\left(\eta\right)\mathbf{B}\left(\mathbf{I}-\mathrm{diag}\left(\mathbf{R}_f\right)\mathbf{D}\mathrm{diag}\left(\eta\right)\mathbf{B}\right)\Delta{\mathbf{P}_c}^*\end{aligned}\right\} \tag{3.93}$$

From equations (3.91), (3.92) and (3.93) we can find the sensitivity matrix $\mathbf{S}$, as the sub-matrices are readily available from theses equations. The load-frequency relation is given by

$$\Delta\mathbf{P}_L = -\left(\mathrm{diag}\left(\mathbf{R}_g\right)+\mathrm{diag}\left(\eta\right)\mathbf{B}\mathrm{diag}\left(\mathbf{R}_f\right)\right)\Delta\mathbf{f} \tag{3.94}$$

If the converter losses are ignored, the load-frequency relationship becomes

$$\Delta\mathbf{P}_L = -\left(\mathrm{diag}\left(\mathbf{R}_g\right)+\mathbf{B}\mathrm{diag}\left(\mathbf{R}_f\right)\right)\Delta\mathbf{f} \tag{3.95}$$

where $\mathbf{B}=\mathbf{J}_{DC}(\mathbf{J}_{DC}+diag\left(\mathbf{R}_{DC}\right))^{-1}$. From (3.95), the frequency vs load sensitivity matrix ($\mathbf{S}_{fL}$) becomes

$$\mathbf{S}_{fL} = -(\mathrm{diag}\left(\mathbf{R}_g\right)+\mathbf{B}\mathrm{diag}\left(\mathbf{R}_f\right))^{-1} \tag{3.96}$$

The first approach of computing $\mathbf{S}$ is less cumbersome than the second one. The second approach, however, gives analytical expression for each sub-matrix elements of $\mathbf{S}$ thereby enabling us to the effects of individual input parameter vectors on out

vectors.
The steady-state ac/dc analysis above has been done based on the assumption that each VSC-HVDC terminal is connected to a unique ac grid. In general, however, two or more terminals of an MTDC can possibly be connected to a common ac grid system. Because of this, the steady-state ac/dc interaction expressions derived above will not be applicable to all ac/dc interconnection topologies. Therefore, we will attempt to re-do the ac/dc analysis based on a generalized ac/dc interconnection shown in Fig. 3.18, where one ac grid may be connected to multiple VSC-HVDC stations of a MTDC. In Fig. 3.18 f_i refers to frequency of ac grid-i (as measured from

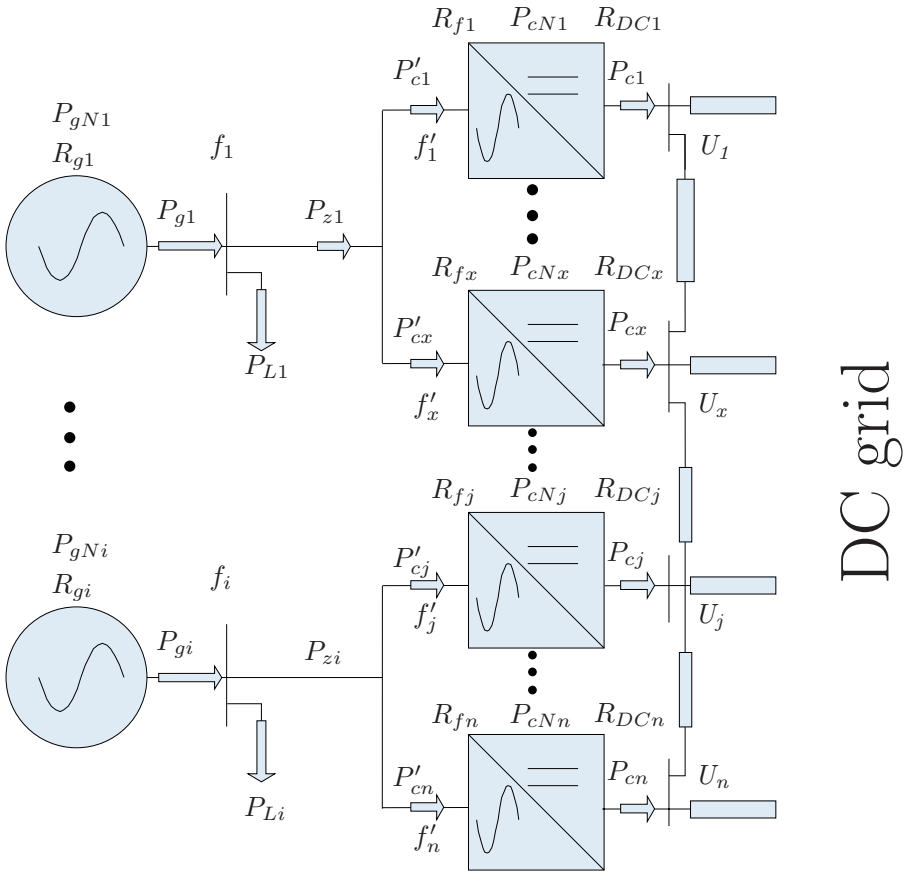


Figure 3.18: Generalized ac/dc connection topology

'grid perspective') while f_j' refers to frequency measured at dc terminal-j, with the prime superscript ($'$) indicating that this frequency is from 'converter perspective'. By doing so we get a unique frequency variable for each converter station including those which are connected to the same ac grid. For example dc terminals 1 and x have separate frequency measurements f_1' and f_x' while both of them are connected to ac grid-1, which in turn has grid frequency of f_1. At steady-state all these three frequency variables are expected to be equal (i.e. $f_1' = f_x' = f_1$). Moreover a new power variable (i.e. P_{zi}) is introduced for each ac grid to represent the total (net) power flow from ac grid to MTDC via all the VSC-HVDC stations interconnecting the two (ac grid and dc grid).

Now let us define $\mathbf{M}$ as a connection matrix between ac grids and VSC-HVDC terminals of the dc grid. (This type of matrix is more commonly termed as incidence matrix). The matrix element of $\mathbf{M}$ at position (i, j) will be assigned 1 if dc terminal-j is connected to ac grid-i and 0 if they are not directly connected. A careful observation of the relationship between $\mathbf{P}_z$ and $\mathbf{P}_c'$ reveals that the two are related by

$$\Delta\mathbf{P}_z = \mathbf{M}\Delta\mathbf{P}'_c \tag{3.97}$$

Similarly, $\mathbf{f}$ and $\mathbf{f}'$ are related by

$$\Delta\mathbf{f}' = \mathbf{M}^T\Delta\mathbf{f} \tag{3.98}$$

The superscript 'T' in (3.98) refers to matrix transposition operator. With the generalized ac/dc connection topology, ac grid power flow balance equation (3.73) is modified as

$$\Delta\mathbf{P}_g = \Delta\mathbf{P}_L + \Delta\mathbf{P}_z \tag{3.99}$$

Replacing (3.97) and (3.78) into (3.99) we find

$$\Delta\mathbf{P}_g = \Delta\mathbf{P}_L + \mathbf{M}\mathrm{diag}\left(\eta\right)\Delta\mathbf{P}_c \tag{3.100}$$

Similarly converter power flow equation (3.83) is modified for the generalized ac/dc connection topology as

$$\Delta\mathbf{P}_c = \mathbf{B}\left(\Delta{\mathbf{P}_c}^* + \mathrm{diag}\left(\mathbf{R}_f\right)\Delta\mathbf{f}'\right) \tag{3.101}$$

Substituting (3.98) into (3.101) we get

$$\Delta\mathbf{P}_c = \mathbf{B}\left(\Delta{\mathbf{P}_c}^* + \mathrm{diag}\left(\mathbf{R}_f\right)\mathbf{M}^T\Delta\mathbf{f}\right) \tag{3.102}$$

From (3.76), (3.100) and (3.102) we find

$$\begin{bmatrix} \Delta\mathbf{P}_g \\ \Delta\mathbf{P}_c \\ \Delta\mathbf{f} \end{bmatrix} = \underbrace{\begin{bmatrix} \mathbf{I} & 0 & -\mathrm{diag}\left(\mathbf{R}_g\right) \\ 0 & \mathbf{B}^{-1} & -\mathrm{diag}\left(\mathbf{R}_f\right)\mathbf{M}^T \\ \mathbf{I} & -\mathbf{M}\mathrm{diag}\left(\eta\right) & 0 \end{bmatrix}^{-1}}_{\mathbf{S}} \begin{bmatrix} {\Delta\mathbf{P}_g}^* \\ {\Delta\mathbf{P}_c}^* \\ \Delta\mathbf{P}_L \end{bmatrix} \tag{3.103}$$

The connection matrix of ac/dc system shown in Fig. 3.17 is always an identity matrix. Hence substituting $\mathbf{I}$ in place of $\mathbf{M}$ in (3.103) results in the same form of expression of $\mathbf{S}$ as (3.89).
If we want to look only at load-frequency relationship, we can compute analytical expression by combining (3.76), (3.78) and (3.83). The resulting expression is given by

$$\Delta\mathbf{f} = \underbrace{-\Big(\mathrm{diag}\left(\mathbf{R}_g\right) + \mathbf{M}\mathrm{diag}\left(\eta\right)\mathbf{B}\mathrm{diag}\left(\mathbf{R}_f\right)\mathbf{M}^T\Big)^{-1}}_{\mathbf{S}_{fL}}\Delta\mathbf{P}_L \tag{3.104}$$

If the converter losses are neglected, (3.104) becomes simplified as

$$\Delta\mathbf{f} = \underbrace{-\Big(\mathrm{diag}\left(\mathbf{R}_g\right) + \mathbf{M}\mathbf{B}\mathrm{diag}\left(\mathbf{R}_f\right)\mathbf{M}^T\Big)^{-1}}_{\mathbf{S}_{fL}}\Delta\mathbf{P}_L \tag{3.105}$$

The other sub-matrices of $\mathbf{S}$ can be computed in a similar manner.

Now let us consider the MTDC model shown in Fig. 3.19. The initial steady-state of the ac grids and the MTDC are given by Table 3.29 and Table 3.30 respectively.

Table 3.29: Initial steady-states and parameters of the ac grids in Fig. 3.19

AC grid No.	1	2	3	4
P_g (MW)	4645	3254	4554	2108
P_L (MW)	3503	4000	4000	3002
P_Z (MW)	1142	-746	554	-894
f (Hz)	50	50	50	50
P_{gN} (MW)	7000	6000	8000	4000
R_g (MW/Hz)	2800	2400	3200	1600
For all ac grids: $f_N = 50\,\mathrm{Hz}$ and $V_{LL,Rated} = 240\,\mathrm{kV}$				

The incidence (connection) matrix, $\mathbf{M}$, for the MTDC in Fig. 3.19 is given by (3.106).

$$\mathbf{M} = \begin{bmatrix} 1 & 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 1 \end{bmatrix} \tag{3.106}$$

Matrix $\mathbf{B}$ for the MTDC in Fig. 3.19 has already been computed in (3.43). $\mathbf{R}_g$, $\mathbf{R}_{DC}$, and $\mathbf{R}_f$, can be obtained from Table 3.29 and Table 3.30. Hence, after substituting

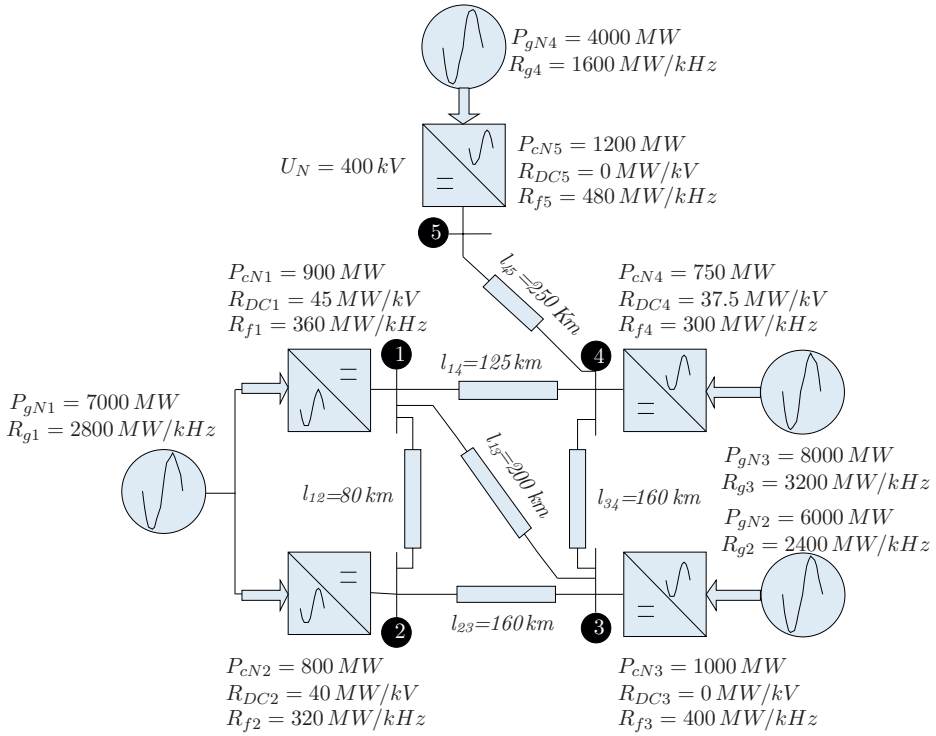


Figure 3.19: MTDC scenario with multiple VSC-HVDC connection to an ac grid

Table 3.30: Initial steady-states and parameters of the VSC-HVDC terminals in Fig. 3.19

Terminal No.	1	2	3	4	5
U (kV)	399.550	400.000	396.613	396.928	385.247
P_c (MW)	600.000	535.928	-750.00	550.005	-900.00
η	1.00557	1.00510	0.99333	1.00545	-0.99333
P_{cN} (MW)	900	800	1000	750	1200
R_{DC} (MW/kV)	45	40	0	37.5	0
R_f (MW/Hz)	360	320	400	300	480

the relevant parameters into (3.104), the load-frequency sensitivity matrix (S_{fL}) of

the MTDC in Fig. 3.19 becomes as

$$\begin{bmatrix} \Delta f_1 \\ \Delta f_2 \\ \Delta f_3 \\ \Delta f_4 \end{bmatrix} = \underbrace{10^{-3} \times \begin{bmatrix} -0.3356 & -0.0345 & -0.0188 & -0.0539 \\ 0.0000 & -0.3574 & 0.0000 & 0.0000 \\ -0.0187 & -0.0153 & -0.2963 & -0.0309 \\ 0.0000 & 0.0000 & 0.0000 & -0.4814 \end{bmatrix} \frac{\text{Hz}}{\text{MW}}}_{\mathbf{s}_{fL}} \begin{bmatrix} \Delta P_{L1} \\ \Delta P_{L2} \\ \Delta P_{L3} \\ \Delta P_{L4} \end{bmatrix} \tag{3.107}$$

Now let us consider a load increment of 200 MW in ac grid 4 (i.e. $\Delta \mathbf{P}_L = [0\ 0\ 0\ 200]'$). From (3.107) estimated changes in frequencies are given by

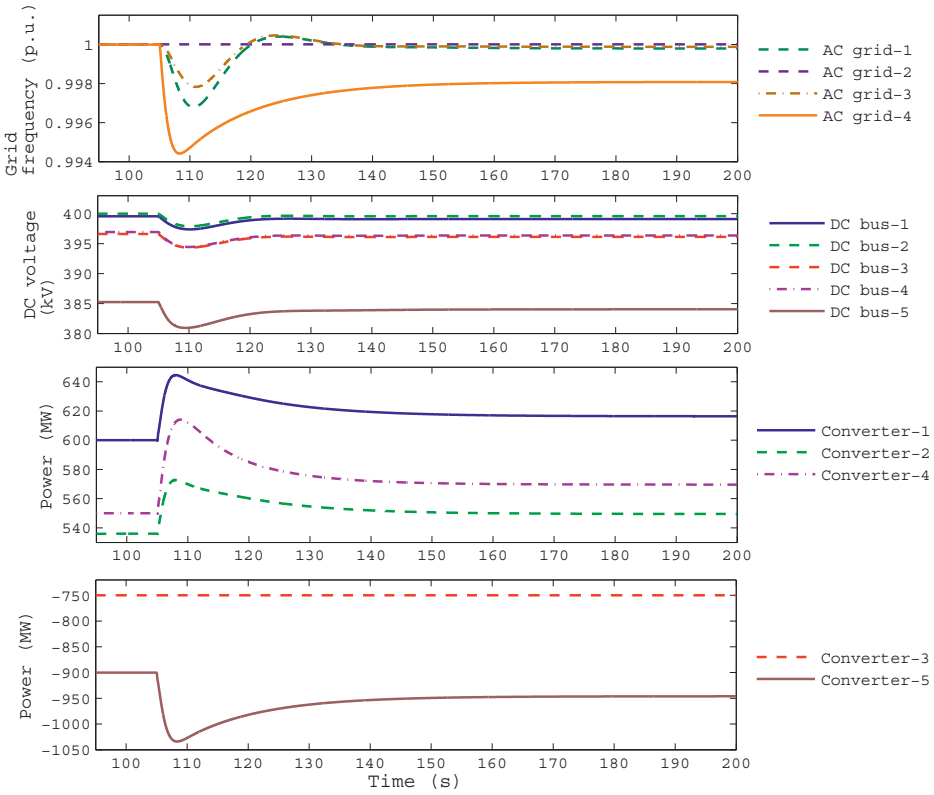


Figure 3.20: Ac/dc responses to load insertion of 200 MW in ac grid-4

$$\begin{bmatrix} \Delta f_1 \\ \Delta f_2 \\ \Delta f_3 \\ \Delta f_4 \end{bmatrix} = \begin{bmatrix} -10.77 \\ 00.00 \\ -06.18 \\ -96.28 \end{bmatrix} \text{mHz} \tag{3.108}$$

Time simulation of load insertion of 200 MW in the ac grid-4 of the MTDC model gives the results shown in Fig. 3.20, Table 3.31 and Table 3.32.

Table 3.31: Simulation results: steady-state power flow changes and frequencies in the ac grids

AC grid No.	1	2	3	4
ΔP_g (MW)	30	0	20	154
ΔP_L (MW)	0	0	0	200
ΔP_Z (MW)	30	0	20	-46
Δf (mHz)	-10.3	0.0	-6.0	-96.3

Table 3.32: Simulation results: steady-state dc voltage changes and power flows of the VSC-HVDC terminals

Terminal No.	1	2	3	4	5
ΔU (kV)	-0.4486	-0.4234	-0.4861	-0.5715	-1.2083
ΔP_c (MW)	16.5	13.6	0.0	19.6	-46.2

The observed changes in frequencies from the simulation results match accurately the frequency changes estimated by the proposed analytical expression of (3.104). The power injection at terminal-3 did not show any variation because this terminal has zero dc voltage constant. For the same reason, ac grid-2 did not show any frequency variation in response to the load increment in ac grid-4.

3.6 Secondary Control of MTDC

In the previous section primary control of MTDC transmission system was discussed. Here a proposed secondary control method for MTDC transmission systems will be discussed. Traditionally secondary control in ac systems is used to restore system frequency and to eliminate tie-line control error. Area control error refers to the deviation of power flow in a specific tie-line from the one given by the scheduled interchange between a control area and its neighbors. A control area is the area over which a TSO has jurisdiction over the balancing power of generation and demand. One or more generation units may participate in the secondary control action based

on a selected set of constant factors called *participation factors*. The schematic of secondary control in ac grid is shown in Fig. 3.21. In Fig. 3.21 $\Delta P_{g,comp}$ refers

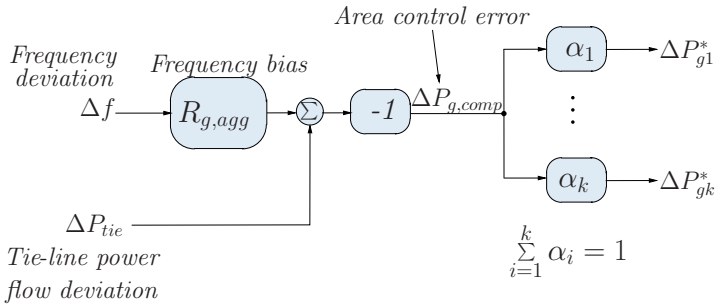


Figure 3.21: Secondary control in ac system

to the incremental power to be compensated by the generation units participating in secondary control. Given the frequency deviation (Δf), the area control error (ΔP_{tie}) and the aggregate frequency response of the ac grid ($R_{g,agg}$), the total power compensation demand ($\Delta P_{g,comp}$) can be computed as shown in the figure. Once the total power compensation demand is known, incremental power references will be generated using a set of participation factors (α's) and sent to participant generation units. The sum total of all participation factors gives 1 ($\sum_{i=1}^{k} \alpha_i = 1$).

Secondary control in dc grid can be performed in a more or less similar manner as that of secondary control in ac grid. The secondary control action in ac grid frees up some of the spinning reserves already activated due to primary frequency response. Likewise secondary control of MTDC will have the purpose of freeing up some converter units already activated by dc-bus voltage deviation from the initial set points attained by precise power flow control method. (See section 3.2 for further details). Secondary control of MTDC will resemble the tie-line control part of secondary control in ac systems. It should be reminded that due to line resistances dc-bus voltage measured variation at one dc-bus will not be sufficient to determine aggregate power control error in MTDC (a dc grid equivalent of Area Control Error in ac grid). Moreover, due to the influence of dc line resistances, a reduced form of the matrix-**B** will be needed to compute appropriate power references to the participant VSC-HVDC terminals. Block diagram of secondary control in MTDC is shown in Fig. 3.22.

In Fig. 3.22 $\Delta P_{DC,comp}$ refers to the total power compensation demand (or aggregate power control error) in the MTDC where as $\Delta P_{c,compk}$ refers to the power compensation assigned to converter-k. Like in secondary control of ac systems, participation

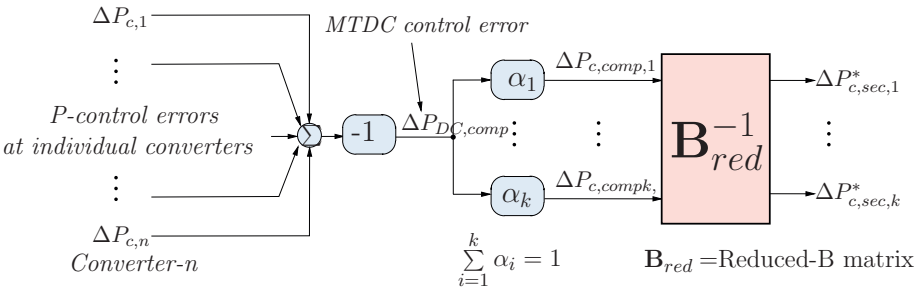


Figure 3.22: Secondary control in MTDC

factors are used here as well in a similar manner to compute power compensation assignments. The actual change in power reference to be used ($\Delta P^*_{c,sec}$) is computed using the reduced-B matrix and the power compensation vector ($\Delta \mathbf{P}_{c,comp}$). The reduced-B matrix ($\mathbf{B}_{red}$) is a square matrix obtained from the full $\mathbf{B}$ matrix (refer to equation (3.38)) by selecting the rows and columns which correspond to the VSC-HVDC terminals which participate in the secondary control. Let the expanded form of the matrix $\mathbf{B}$ be written as

$$\mathbf{B} = \mathbf{J}_{DC}(\mathbf{J}_{DC} + diag\,(\mathbf{R}_{DC}))^{-1} = \begin{bmatrix} b_{11} & \dots & b_{1x} & \dots & b_{1y} & \dots & b_{1n} \\ \vdots & \ddots & \vdots & \ddots & \vdots & \ddots & \vdots \\ b_{x1} & \dots & b_{xx} & \dots & b_{xy} & \dots & b_{xn} \\ \vdots & \ddots & \vdots & \ddots & \vdots & \ddots & \vdots \\ b_{y1} & \dots & b_{yx} & \dots & b_{yy} & \dots & b_{yn} \\ \vdots & \ddots & \vdots & \ddots & \vdots & \ddots & \vdots \\ b_{n1} & \dots & b_{nx} & \dots & b_{ny} & \dots & b_{nn} \end{bmatrix} \tag{3.109}$$

If for example only terminals x and y are to participate in the secondary control,the reduced-B matrix becomes

$$\mathbf{B}_{red} = \begin{bmatrix} b_{xx} & b_{xy} \\ b_{yx} & b_{yy} \end{bmatrix} \tag{3.110}$$

The appropriate power reference vector used in the secondary control (i.e. $\Delta \mathbf{P}_{c,sec}{}^*$)) is computed by (3.111)

$$\Delta \mathbf{P}_{c,sec}{}^* = \mathbf{B}_{red}{}^{-1} \alpha \Delta P_{DC,comp} \tag{3.111}$$

where α is the participation factor vector and $\Delta P_{DC,comp}$ is the total power to be compensated in the MTDC.

The steady-state power flow deviations in MTDC are originally caused by either uncontrolled events such as outage of a converter station or by operator actions such as changing of power reference at a terminal to increase/decrease the power injection (this can be considered as dc grid load changes). The simulated case of power injection change at terminal-3 of the five-terminal MTDC (in Fig. 3.8 in section 3.3.2) can be an illustrative example of an event which results in steady-state power flow deviations. It was observed that when terminal-3 power injection was changed from $-750\,\text{MW}$ to $-800\,\text{MW}$, all the other terminals (i.e. 1,2,4,5) responded by marginally increasing their respective power injections into the dc grid. This corresponds to an added 50 MW power demand in the MTDC. The resulting power flow after the action of primary control is in Table 3.33. (This is comes from simulation results discussed in section 3.3.2).

Table 3.33: Nodal power injection after primary control response to updated scheduled injection change ($\Delta P_3^* = -50\,\text{MW}$)

Terminal No.	1	2	3	4	5
ΔP_c(MW)	14.82	13.72	-50.00	11.74	9.67

For the sake of convenience, the $\mathbf{B}$ matrix of the MTDC under consideration is re-written in (3.112). This was computed in equation (3.43).

$$\mathbf{B} = \begin{bmatrix} 0.6509 & -0.2906 & -0.2963 & -0.2503 & -0.1327 \\ -0.2586 & 0.6515 & -0.2743 & -0.2038 & -0.1081 \\ 0.0000 & 0.0000 & 1.0000 & 0.0000 & 0.0000 \\ -0.2072 & -0.1896 & -0.2347 & 0.7049 & -0.1565 \\ -0.1706 & -0.1561 & -0.1933 & -0.2430 & 0.3702 \end{bmatrix} \tag{3.112}$$

Equation (3.112) will be used to determine the reduced-B matrix ($\mathbf{B}_{red}$). Now let us try to employ secondary control in such a way that power flow will be restored to original levels for some of the converter stations. We will consider two different cases of secondary control settings.

Case 1: Only terminal-1 is used in secondary control

Here the objective is to restore power injections of terminals 2, 4 and 5 (i.e. the terminals which participated in primary control) to their initial levels at the expense of further increment of power injection by terminal-1. The reduced-B matrix becomes

$$\mathbf{B}_{red} = 0.6509 \tag{3.113}$$

From Table 3.33 we can see that terminal-2,4 and 5 have contributed 13.72 MW, 11.74 MW and 9.67 MW of balancing power during primary control action. Hence the power compensation demand is given by

$$\Delta P_{DC,comp} = \sum (13.72 + 11.74 + 9.66) = 35.13 \ \text{MW} \tag{3.114}$$

Since there is only one converter used for secondary control, the only available participation factor (α_1) becomes 1. The required power reference change for terminal-1 is computed as

$$\Delta P^*_{c,sec1} = 0.6509^{-1} \times 1 \times 35.13 = 53.97\text{MW} \tag{3.115}$$

When the calculated secondary control reference signal is applied to terminal-1, the MTDC time-response looks like as in Fig. 3.23 and Table 3.34.

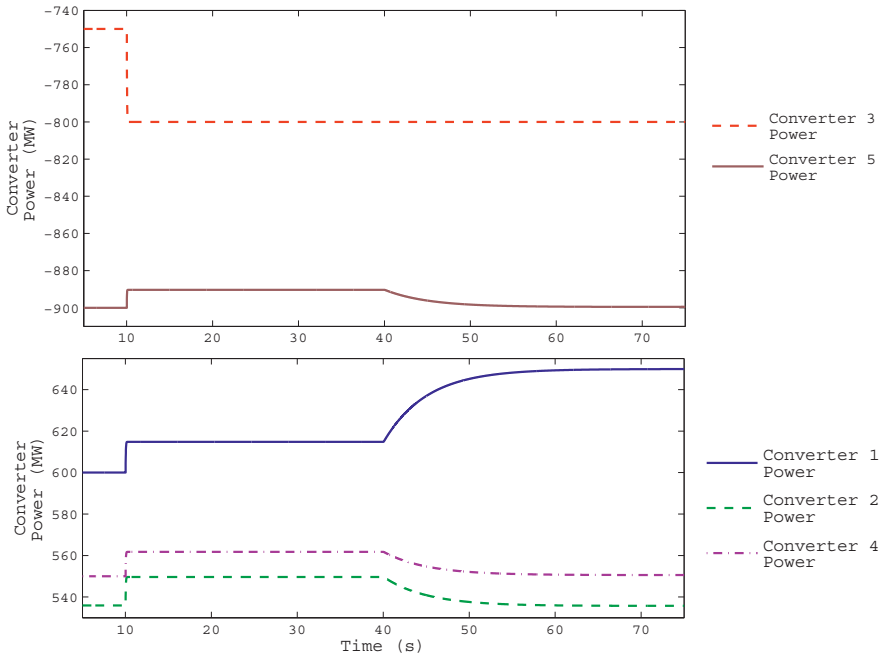


Figure 3.23: MTDC primary and secondary control responses: case 1

The changes in nodal power injection from the initial steady-state levels are shown in Fig. 3.24.

Table 3.34: Steady-state dc-bus voltage and nodal power injections: case 1

Terminal No.		1	2	3	4	5
Initial steady-state	U (kV)	399.550	400.000	396.613	396.928	385.247
	P_c (MW)	600.0	535.9	-750.0	550.0	-900.0
After primary control action	U (kV)	399.287	399.726	396.204	396.667	385.118
	P_c (MW)	614.8	549.7	-800.0	561.7	-890.3
After secondary control action	U (kV)	399.621	400.046	396.486	396.915	385.241
	P_c (MW)	649.9	535.7	-800	550.6	-899.5

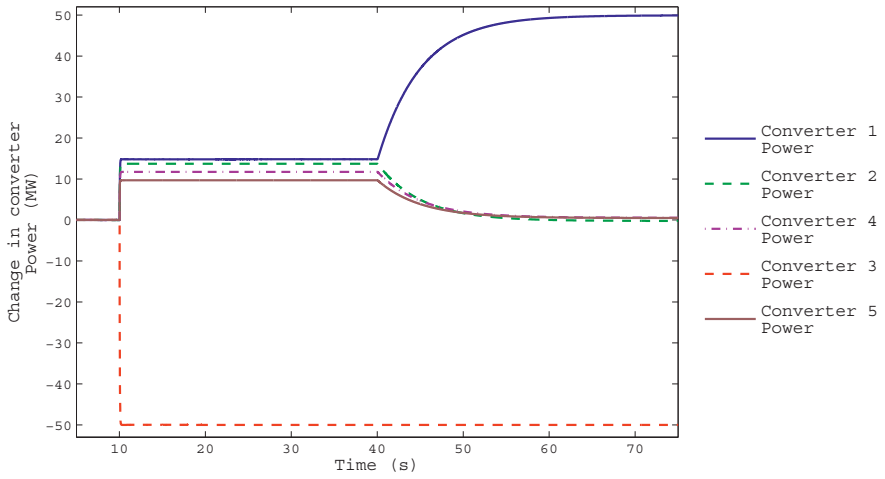


Figure 3.24: Changes in nodal power injections during primary and secondary control: case 1

Case 2: Terminals 1 and 2 are used in secondary control

Here the objective is to restore power injections of terminals 4 and 5 initial levels at the expense of further increment of power injection by terminals 1 and 2. The reduced-B matrix becomes

$$\mathbf{B}_{red} = \begin{bmatrix} 0.6509 & -0.2906 \\ -0.2586 & 0.6515 \end{bmatrix} \tag{3.116}$$

Terminals 4 and 5 have contributed 11.74 MW and 9.67 MW of balancing power during primary control action. Hence $\Delta P_{DC,comp}$ is computed as

$$\Delta P_{DC,comp} = \sum (11.74 + 9.67) = 21.41 \text{ MW} \tag{3.117}$$

Let us consider that both terminal-1 and 2 are intended to equally participate in the secondary control. Hence the resulting participation factor vector is

$$\alpha = \begin{bmatrix} \alpha_1 \\ \alpha_2 \end{bmatrix} = \begin{bmatrix} 0.5 \\ 0.5 \end{bmatrix} \tag{3.118}$$

Substituting the relevant variables and parameters into (3.111), the secondary control references become as given by

$$\begin{bmatrix} \Delta P_{c,\text{sec}\,1}{}^{*} \\ \Delta P_{c,\text{sec}\,2}{}^{*} \end{bmatrix} = \begin{bmatrix} 0.6509 & -0.2906 \\ -0.2586 & 0.6515 \end{bmatrix}^{-1} \begin{bmatrix} 0.5 \\ 0.5 \end{bmatrix} 21.41 = \begin{bmatrix} 28.9 \\ 27.9 \end{bmatrix} \text{MW} \tag{3.119}$$

When the secondary control references computed in (3.119) are applied to the MTDC, the primary-secondary MTDC control response becomes as shown in Fig. 3.25 and Table 3.35.

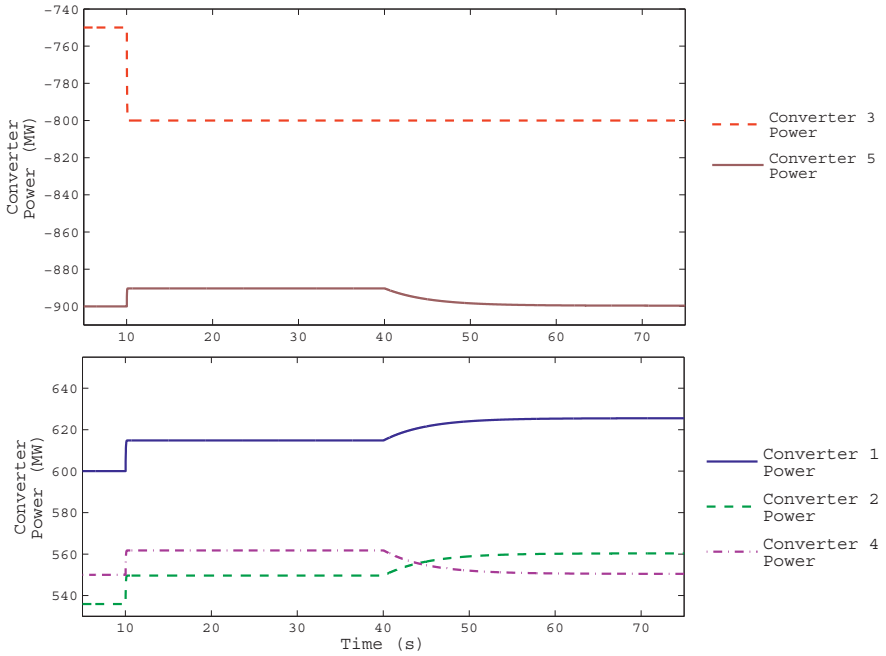


Figure 3.25: MTDC primary and secondary control responses: case 2

The changes in nodal power injection from the initial steady-state levels are shown in Fig. 3.26.

Table 3.35: Steady-state dc-bus voltage and nodal power injections: case 2

Terminal No.		1	2	3	4	5
Initial steady-state	U (kV)	399.550	400.000	396.613	396.928	385.247
	P_c (MW)	600.0	535.9	-750.0	550.0	-900.0
After primary control action	U (kV)	399.287	399.726	396.204	396.667	385.118
	P_c (MW)	614.8	549.7	-800.0	561.7	-890.3
After secondary control action	U (kV)	399.610	400.069	396.507	396.918	385.242
	P_c (MW)	625.5	560.3	-800	550.5	-899.6

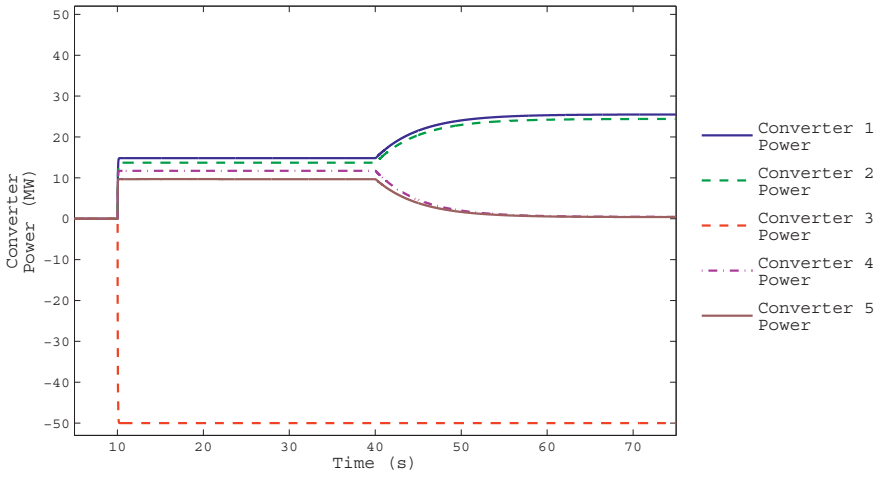


Figure 3.26: Changes in nodal power injections during primary and secondary control: case 2

In the simulation results of both case-1 and case-2 scenarios of secondary control, nodal power injections have been restored at the desired converters.
Secondary control of MTDC may be integrated with secondary control of ac grids, given that both the MTDC and ac grid are commanded by the same transmission system operator (TSO) [44]. In such a case, the hierarchical control of integrated ac/dc system may look like the schematic diagram of Fig. 3.27.
At the highest level of power flow control hierarchy, generation and transmission scheduling in a deregulated power system is governed by power market (specifically the day-ahead market). At this level of control, there is little distinction between ac and dc transmissions. This means that spot electricity market coupled with power flow constraints (in both ac and dc transmissions) will determine the settlement of

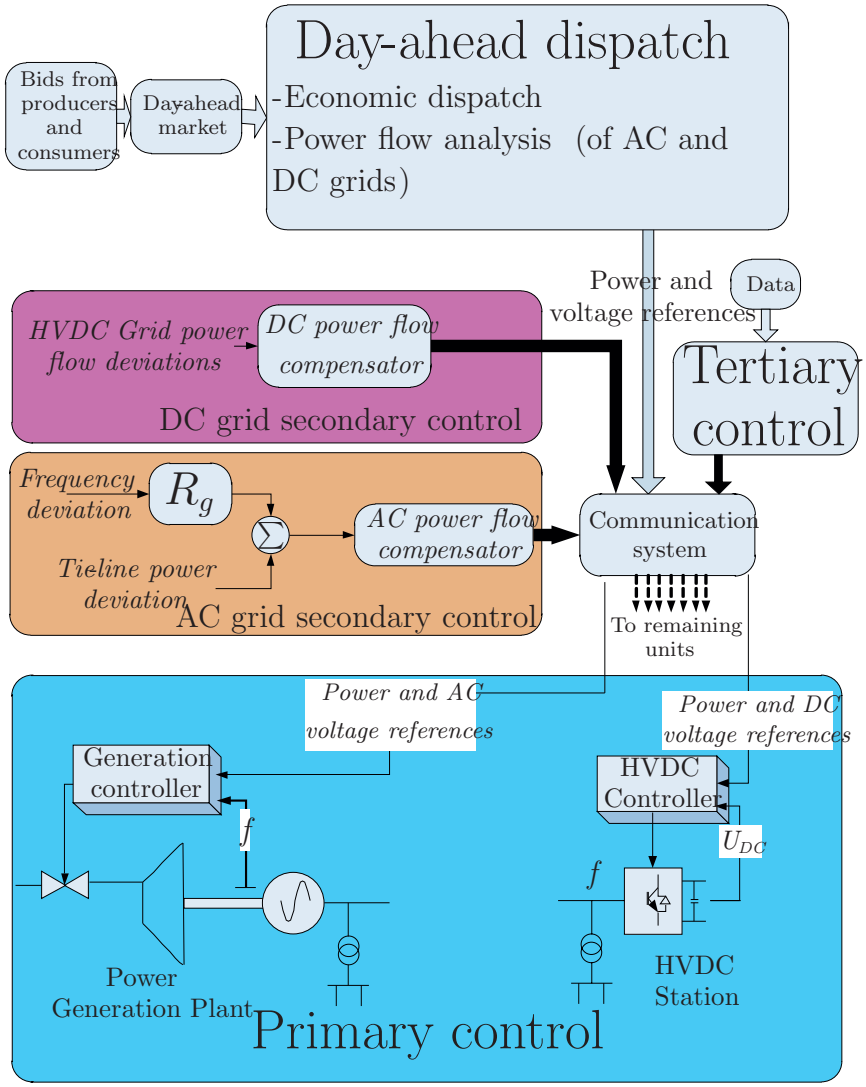


Figure 3.27: Flow chart describing integrated primary, secondary and tertiary controls of ac/dc grids

the final power flow schedule. Similarly, in tertiary control the original power flow

schedule will be modified based upon latest available data about the power system including ac and dc transmission networks.
As one goes down the control hierarchy, the distinction between ac and dc grids becomes larger. In ac grids power flow is controlled by adjusting references to generating units whereas in dc grids power flow is controlled by adjusting references to converter units. In conclusion, MTDC operation can easily be accommodated with the already existing hierarchical control structure of ac grids with some re-adjustment.

3.7 Chapter Summary

Secure operation of MTDC requires that some of the VSC-HVDC terminals be configured as dc voltage droop mode. Precise power flow control in the dc grid is achieved by taking into account the effects of the line resistances as well as converter losses while determining the appropriate control reference values. Moreover, the line resistances also affect the distribution pattern of primary balancing power among converters in dc droop control mode.
Accurate analytical expressions for describing the steady-state power flow interactions in MTDC have been derived. An equivalent-circuit based approach has been proposed to study the impact of dc line resistance and grid topology on primary response of MTDC to power imbalance. Moreover analytical expression for the load-frequency response study of ac/dc systems has been proposed and verified with simulation results of a test MTDC system. Simulation results of a new, proposed secondary control in MTDC, based upon the proposed steady-state analysis, has given satisfactory performances.

4 STABILITY AND DYNAMICS OF MTDC SYSTEMS

This chapter deals with the stability aspects and the dynamics of MTDC systems. In the first section of this chapter large-disturbance stability in MTDC will be studied. In the second part of the chapter small-signal analysis of MTDC will be explored.

4.1 Large-disturbance Stability

4.1.1 P vs U Capability Diagram of VSC

In section 2.3 various control modes of VSC were discussed. It is necessary to keep in mind that the operational characteristics of a VSC, as determined by the inner and outer controllers discussed in section 2.3, will be valid only within a finite/limited domain of operation. Operation of devices beyond the boundary of safe operation will incur the risk of overvoltage and/or overcurrent conditions, thereby exposing the device to damage or destruction. In this regard the components in VSC which are most sensitive to overvoltage and overcurrent are the semiconductor switches. Hence the current, voltage and power limits of the semiconductors will mainly determine the operating limits for the whole VSC unit. The safe operating area of a typical power electronic switch looks like the diagram in Fig. 4.1 [67]. The P vs U (or P

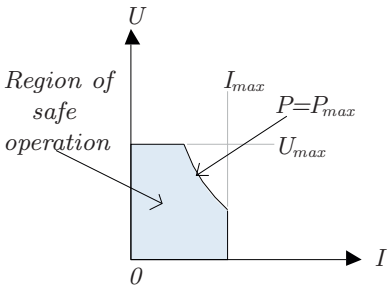


Figure 4.1: Safe operating area of a power electronic switch

vs I) capability diagram defines the normal operating region of VSC where all the operating limits of the converter are respected. Just like the individual electrical/ electronic components, the VSC (including both two level and multilevel types) will have its own domain of normal operation. The domain of operation of a VSC is

characterized by maximum power capacity, maximum dc voltage level, maximum dc current and minimum dc voltage level. The first three constraints come from the need for protection of the converter and dc lines from damage or destruction under excess voltage and/or current levels. The fourth constraint (i.e. minimum dc voltage level) is inherent to the working principle of VSC itself. This is from the fact that while keeping the ac voltage constant at its normal level it will not be possible to discharge (or reduce the dc voltage level) of the VSC beyond a certain level of dc voltage. This minimum dc voltage is approximately 1.28 times the line-to-line ac voltage behind the ac filter and this is reached during square wave modulation of the VSC [67]. In [69] the U vs I diagram of VSC has been described, though some of the limits such as minimum possible dc voltage and maximum dc current are missing.

The dc current limiter makes sure that the dc-bus current is kept below the maximum allowed all the time including during low dc voltage conditions. If the VSC is required to operate below a certain dc voltage level, the power transmission capacity of the VSC station will start to reduce with decreasing dc voltages. This can be observed from the VSC capability diagram shown in Fig 4.5. The maximum possible over-modulation puts the limit on the minimum attainable dc voltage to $1.28V_{LL}$ where V_{LL} is the rms line-to-line voltage at PCC. A high voltage transformer usually provides the inductance needed for filtering the harmonics from entering the ac grid. Such transformers are equipped with tap changers and hence can provide some amount of ac voltage control. The shaded regions in Fig 4.2 (a) and Fig

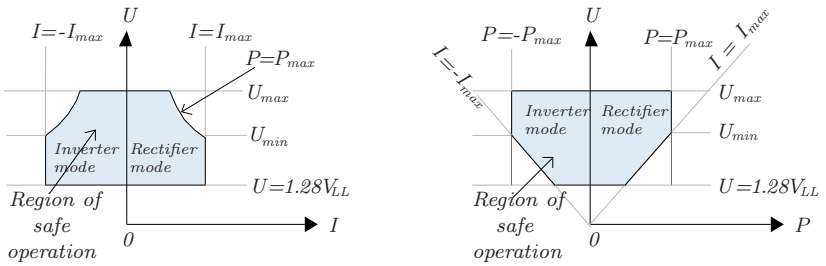


Figure 4.2: Safe operating area of a VSC: (a) U vs I safe operating region (b) U vs P safe operating region

4.2 (b) define the safe operating region of a VSC characterized by maximum power capacity (P_{max}), maximum dc voltage (U_{max}), maximum dc current (I_{max}) and rated line-to-line ac voltage (V_{LL}). The various U vs P characteristics discussed in section 2.3 must always lie within the boundaries of the safe operating region.

In Fig. 4.3, U vs P characteristic line of VSC in constant power control mode is shown. The right side of the safe operating region refers to rectifier mode of operation while the left side refers to inverter mode of operation. The dotted lines show characteristic lines for different values of the power reference (P^*). If for some reason the operating point goes out of the shaded region and the controller is not able to bring it back to the normal operating region, a separate superior protection system may be activated to prevent possible damage due to overvoltages and/or overcurrents. The details of such protection system will not be discussed here. For simplicity, here we assume that the VSC will trip immediately when the the steady-state operating tries to go off the designated normal operating region.

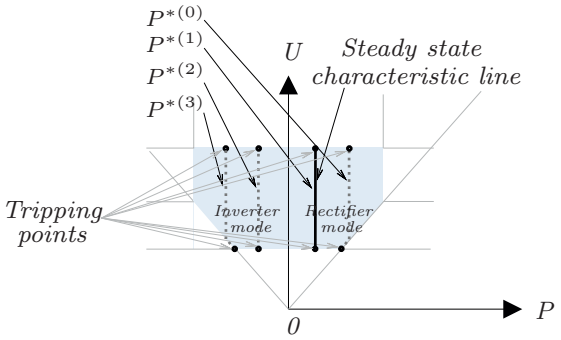


Figure 4.3: U vs P characteristic line of constant power mode bounded within safe operating region

The characteristic line of VSC in constant dc voltage control mode is shown in Fig. 4.4. The tripping points are indicated with dots at the two ends of the characteristic line. By changing the dc voltage reference (U^*) the characteristic line moves up and down along the voltage axis. The dotted lines Fig. 4.4 show characteristic lines for various values of the dc voltage reference. In Fig. 4.5 characteristic U vs P line when dc voltage droop control is applied is shown.
In chapter two it was explained that a dc voltage droop controller has two control parameters; i.e. dc voltage reference (U^*) and power reference (P^*). Increasing/ decreasing either of these two parameters gives the same effect; in both cases the characteristic line moves up/down the voltage axis. (It can also be considered as shifting along the power/horizontal axis. The effect is the same.) The characteristic lines for different dc voltage references are shown with dotted line in Fig. 4.5.

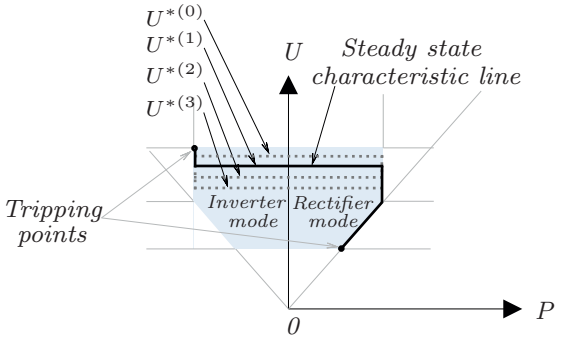


Figure 4.4: U vs P characteristic line of constant dc voltage mode bounded within safe operating region

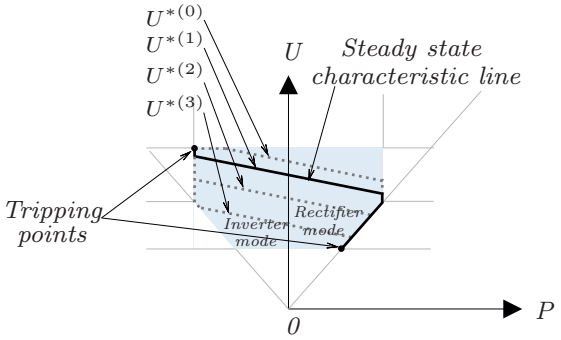


Figure 4.5: U vs P characteristic line of dc voltage droop mode bounded within safe operating region

4.1.2 Determination of the Steady-state Operating Point

In chapter three it was shown that the steady-state operating conditions at a VSC-HVDC terminal (i.e. the nodal power injection and the dc-bus voltage) are determined by the dc grid topology, the employed control mode at various terminals, and the ratings of the converters constituting the dc grid. A quantitative approach was used to analyze the steady-state operation of MTDC in the linear region without considering the boundaries of safe operation. Here in this section, the steady-state operation of MTDC will be discussed qualitatively as introduction to the study of

MTDC stability during large-disturbances. In Fig. 4.6 a two terminal VSC-HVDC, which connects two ac grids, is shown. Let us consider that initial power flow is from left to right (i.e. from terminal-1 to terminal-2). With the specified direction of the

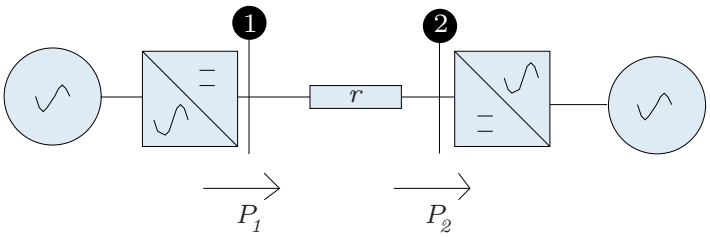


Figure 4.6: Two-terminal VSC-HVDC link

power flow in Fig. 4.6, the U vs P characteristic curves become as in Fig. 4.7. Note that the characteristic curve for terminal-2 is laterally inverted since the power axis for this terminal is opposite to that of terminal-1. This goes in line with the specified direction of power flow in Fig. 4.6. If the dc transmission line losses are ignored, the

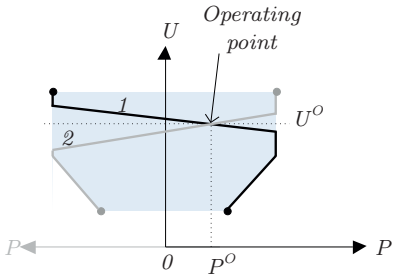


Figure 4.7: Determination of the steady-state operating point from intersection of two characteristic lines

intersection of the two characteristic curves in Fig. 4.7 gives the steady-state operating point of the VSC-HVDC system. Hence the approximate operating dc voltage and the amount of power transfer can be established quickly from the knowledge of the characteristic curves. Another alternative to determine the operating point is to horizontally add up the individual characteristic curves and the zero-power crossing of the aggregate characteristic curve gives the operating dc voltage level. This is because the total of all the nodal power injections gives the aggregate dc line losses,

which in this case has been considered as zero (negligible) for the sake of simplicity. The aggregate characteristic curves, for the example VSC-HVDC system in Fig. 4.6, are shown in Fig. 4.7. Once the operating dc voltage level is determined, the amount of power flow for each individual converter is found by the intersection of the dc line, $U = U^o$, and the characteristic curve for the corresponding terminal.

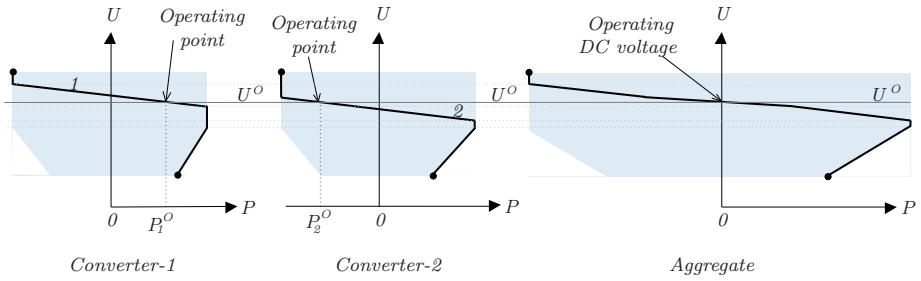


Figure 4.8: Determing the steady-state operating point from the aggregated characteristic line

The two techniques used above for determining the operating points can also be applied to a MTDC system without much difficulty. In the previous chapter it was discussed in detail that the dc line resistances have considerable impact on determining the steady-state operation of MTDC. For simplifying the qualitative analysis, however, we stick to the assumption that the dc line losses are negligible compared to the overall power flow via the dc grid. From Fig. 4.8, we can observe that as the number of terminals increase, the aggregate characteristic curve becomes more elongated horizontally and the slope become flatter. Otherwise, it can be noted that the aggregate of two or more VSC-HVDC terminals has more or less similar shape of U vs P characteristic curve as that of a single VSC-HVDC terminal. Hence large-disturbance stability study based upon two-terminal VSC-HVDC can easily be applied to MTDC systems as well.

4.1.3 Large-disturbance Stability Analysis

Large-disturbance stability in MTDC can be understood by looking at the interaction between all rectifying converter units on one side and all inverting converter units on the other side. A good analogy can be drawn from aggregate generation and aggregate load versus frequency characteristics in ac girds. Fig. 4.9 (a) shows the static frequency versus power (f vs P) characteristic of synchronous generator

and in Fig. 4.9 (b) the static dc voltage versus power (U vs P) characteristic of VSC-HVDC terminal is shown. Several similarities can be drawn from the two diagrams. P_S in Fig. 4.9 (b) refers to the characteristic line of a terminal whose power flow is defined as positive for rectifier operation. This terminal acts as the 'source' node in the dc grid. In the same diagram P_L refers to the characteristic of a converter terminal whose power is defined as positive for inverter mode. Hence this terminal acts as the 'sink' (load) terminal in the dc grid.

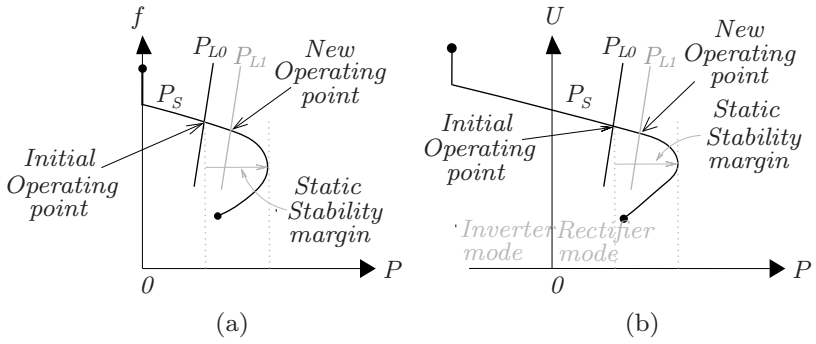


Figure 4.9: Steady-state characteristic points of: (a) Synchronous generator (b) VSC-HVDC terminal

Like synchronous generators in ac grid, in MTDC the aggregate of rectifier terminals resemble the aggregate of generating units in ac grid. Similarly, the aggregate of inverter terminals form the dc grid load line - analogous to the aggregate load line in ac grids. The intersection between the aggregate rectifier characteristics and the aggregate inverter characteristics approximately gives the total amount of power exchanged between ac grids via the MTDC grid. The difference between the amounts of power transferred and the maximum of the aggregated power transfer capacity of the rectifier units gives the *static stability margin*.
The small disturbance stability criterion of a MTDC grid requires that the operating point be above the nose of the aggregate rectifier characteristic curve. An operating point below the nose curve results in dc voltage collapse. Stability of MTDC for larger disturbances is determined, among other factors, by the size of energy storage elements in the dc grid systems. The energy storage elements in MTDC are dc-bus capacitors and dc line capacitances (when cable line is used). The energy stored in the various inductive elements of the VSCs is small in comparison with the energy stored in the capacitances and hence will be neglected here. For simplifying the analysis, a two-terminal HVDC is used to represent a MTDC where the two

converters represent the aggregate of rectifier terminals and aggregate of inverter terminals. It is necessary to have in mind that the aggregation depends on the specific steady-state operational conditions under consideration; since most of the terminals - if not all - are normally expected to operate both in rectifier mode as well as in inverter mode of operation at various times.
Now let us consider that the aggregated two-terminal VSC-HVDC link model shown in Fig. 4.10 represents a hypothetical MTDC grid.

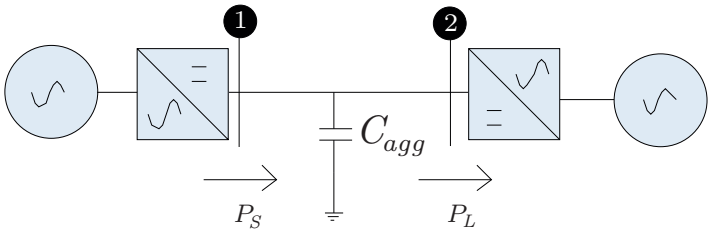


Figure 4.10: Aggregate model representation of MTDC. (Rectifiers and inverters are aggregated separately).

P_S refers to the aggregate power supplied into the dc grid by the rectifiers whereas P_L refers to the aggregate power taken away from the dc grid by inverter units. C_{agg} refers to the sum total of all capacitances in the MTDC. This includes all dc (bus) filter capacitances and all dc cable capacitances. Note that in Fig. 4.10, no dc line resistance is considered. The dc grid line resistances are deliberately ignored so as to make simple use illustration with the aggregate modeling of the rectifiers and inverters. Another advantage of the lossless aggregate modeling is that it enables us to represent all the dc-bus capacitances and the dc line capacitances by a single shunt connected capacitance between the two terminals. The initial steady-state operating point for the aggregate dc grid model is shown by the intersection of the the source line (P_{S0}) and the load line (P_{L0}) (See Fig. 4.11). If the 'load line' goes further to the right beyond the nose of the characteristic line of P_{S0}, instability will follow. Such event is, however, unlikely because power flow schedules always take the available loading capacity of the converters into consideration. (Hence the static stability margin of the aggregate rectifier characteristic line will always be positive during normal operations). Another, more likely, cause of instability is reduction in the aggregate rectifier capacity which makes aggregate characteristic line to move leftwards taking the tip of the nose beyond the dc grid load line (i.e. the transition from P_{S0} characteristic line to P_{S1} characteristic line in Fig. 4.11). This happens during sudden outage of a rectifier terminal, fault occurrence on the ac side of a rectifier terminal or loss of dc line connection to a rectifier unit. If the fault is in

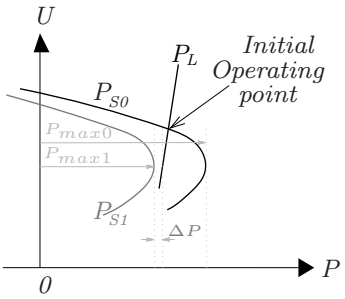


Figure 4.11: Steady-state operating point

the dc grid or within the converter itself, then the problem will most likely persist resulting in dc voltage collapse and then permanent disruption of power flow in the dc grid. ac faults, however, are often temporary and power flow is usually restored after the clearance of the fault depending on the severity and duration of the fault. When the maximum deliverable power of the aggregate rectifier (P_{max}) is lower than the power taken by the aggregate inverter (P_L), the difference (ΔP) will be supplied from the stored energy of the aggregate capacitance. This stored capacitive energy is, however, very small and hence will last only very small duration of time without discharging the capacitors excessively. If the capacitors are discharged further below a critical dc voltage level, dc voltage collapse will be inevitable.
Once the dc voltage gets below a certain minimum value, the dc voltage decrement is accelerated due to decreasing power transfer capabilities of the rectifiers at lower dc voltage levels. On the other hand if the ac fault (which caused the power deficit in the dc grid) is cleared before critical dc voltage is reached, dc voltage will subsequently recover and power flow will continue uninterrupted. Fig. 4.12 and Fig. 4.13 shows stable and unstable dc voltage swings respectively as a result of ac grid fault behind a rectifier unit. Δt in the figures refer to fault clearing time and ΔP refers to power supply gap in the dc grid. The dc voltage stability phenomenon of dc grids has marked similarities with that of first-swing stability of synchronous generators in ac grids. This is evident from comparison of Fig. 4.12 and Fig. 4.14. Note that the horizontal axis for dc voltage stability plot is time while for first-swing stability plot the power angle is used. In both figures the shaded area A_1 represents the amount of energy deficit due to the reduced power injection caused by the ac fault. Since the demanded power is unchanged during the same period, the energy deficit is covered by discharge of the aggregate capacitance in the case of dc grid and from rotational mechanical energy of aggregate inertia in the case of ac grid. For system stability after fault clearance, the inequality $A_2 \geq A_1$ must uphold for

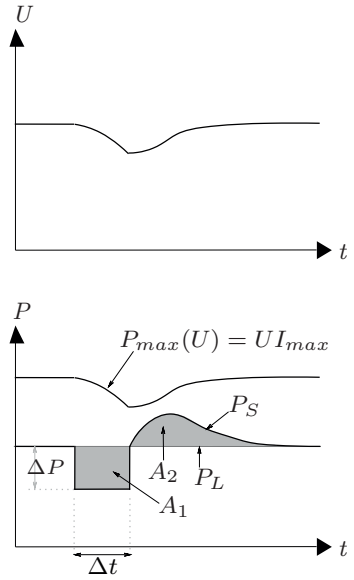


Figure 4.12: Stable case of ac fault impact on dc grid voltage and power flow. Dc voltage is restored after fault clearance

both cases. This will be referred as *equal-area criterion*. This is because A_2 in Fig. 4.12 is not necessarily bounded in time unlike the same area in 4.14 which follows a sine curve. Due to this, the equal-area criterion in dc grid does not tell us the the critical ac fault clearing time beyond which dc voltage collapse will be inevitable. The criterion simply tells us that if the dc voltage recovers from fault, then the aggregate capacitance will be recharged the same amount of energy as it lost during fault duration.

Dc voltage recovery depends on whether or not there will be enough deliverable power right after fault clearance that can meet the power demand. Of course converters may in the mean time trip if low voltage limit is reached before the ac fault is cleared. Moreover some severe ac faults, particularly unbalanced faults, may lead to synchronization problems and lead to earlier tripping of the converter. Here, however, we will focus only on the cases where dc voltage collapse may occur as a result of capacitive energy depletion in the MTDC.

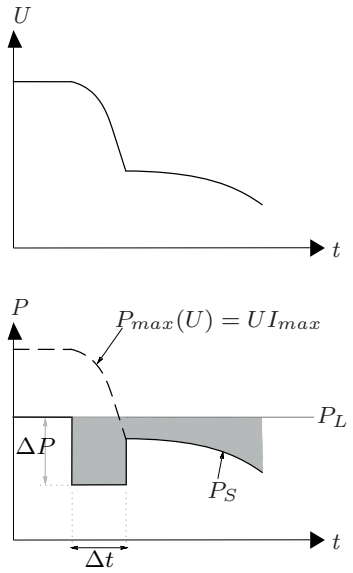


Figure 4.13: Unstable case of ac fault impact on dc grid voltage and power flow. Dc voltage eventually collapses sometime after fault clearance

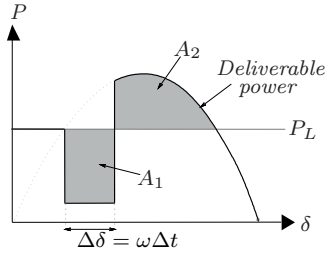


Figure 4.14: Equal-area stability criterion in ac grids

The maximum deliverable power by a converter (P_{max} in Fig. 4.12 and Fig. 4.13) is the product of the dc-bus voltage and maximum dc current capacity of the converter. As can be observed in both figures, the power injection capacity of the aggregated rectifier (P_{max}) reduces with decreasing dc-bus voltage. If the fault is cleared before P_{max} drops below the load demand (P_L), the dc grid will be able to recover from the fault. Hence the dc voltage level at which the aggregate rectifier capacity equals

the load demand defines the *critical dc voltage level ($U_{critical}$)*. The time at which dc voltage reaches the critical dc voltage is defined as *critical clearing time ($\Delta t_{critical}$)*. If the fault is cleared before $\Delta t_{critical}$ is reached, then the MTDC system will recover from the fault and power flow will continue uninterrupted. With larger fault clearing time, the dc voltage will collapse and power flow will be interrupted.
The energy discharged from the capacitor during the fault period is computed as

$$\Delta P \Delta t = \frac{C_{aggr}}{2}\left({U_{initial}}^2 - {U_{final}}^2\right) \tag{4.1}$$

Where $U_{initial}$ refers to the pre-fault dc voltage level and U_{final} refers to the post-fault dc voltage level (or the dc voltage just before the ac fault is cleared). In order to achieve dc grid stability after the fault clearance, the final voltage (U_{final}) should be greater than the critical dc voltage ($U_{critical}$). Hence the maximum amount of capacitive energy ($E_{\max}$) that can be utilized for short term power balancing in the dc grid is given by

$$E_{\max} = \frac{C_{aggr}}{2}\left({U_{initial}}^2 - {U_{critical}}^2\right) \tag{4.2}$$

The stability criterion can be described as

$$\left.\begin{array}{l} U_{critical} < U_{final} \\ \int_{t=0}^{\Delta t} \Delta P dt < E_{\max} = \frac{C_{aggr}}{2}\left({U_{initial}}^2 - {U_{critical}}^2\right) \end{array}\right\} \tag{4.3}$$

In order to explore how the critical dc voltage is determined, we will use the three terminal dc grid shown in Fig. 4.15 as an example. Terminal-C in Fig. 4.15 takes away fixed amount of power (P_C^o) from the dc grid and terminal-B injects fixed amount of power (P_B^o) into the dc grid. Terminal-A regulates the dc voltage by use of dc droop controller. The maximum power transfer capacities of the three VSC-HVDC terminals are given as $P_{A,Rated}$, $P_{B,Rated}$ and $P_{C,Rated}$. Assume that a three phase to ground fault occurs behind terminal-A and as a result the power injected by this terminal into the dc grid is reduced from the pre-fault level of P_A^o to P_A'. The power deficit (ΔP) of the dc grid during the duration of the ac fault becomes as

$$\Delta P = P_A^o - P_A' \tag{4.4}$$

Substituting (4.4) into (4.3) we fined (4.5).

$$\left.\begin{array}{l} \int_{t=0}^{\Delta t_{critical}} \Delta P dt = \frac{C_{agg}}{2}\left({U_{initial}}^2 - {U_{critical}}^2\right) \\ \left(P_A^o - P_A'\right)\Delta t_{critical} = \frac{C_{agg}}{2}\left({U_{initial}}^2 - {U_{critical}}^2\right) \end{array}\right\} \tag{4.5}$$

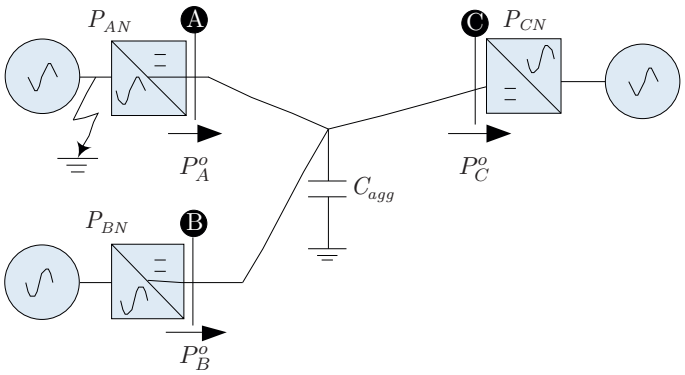


Figure 4.15: Three-terminal VSC-HVDC

From equation (4.5) the critical clearing time is expressed as in (4.6).

$$\Delta t_{critical} = \frac{C_{agg}\left({U_{initial}}^2 - {U_{critical}}^2\right)}{2\left(P_A^o - P_A'\right)} \tag{4.6}$$

The large-disturbance stability criterion of dc grid can be described in terms of power as

$$\left.\begin{array}{l} P_{\max}(U) > P_A^o \\ UI_{max} > P_A^o \end{array}\right\} \tag{4.7}$$

where $P_{\max}(U)$ is maximum deliverable power by converter-A (as a function of dc-bus voltage) and P_A^o refers to power transferred by converter-A into the dc grid prior to the fault occurrence. In order to achieve stability the power transfer capacity of terminal-A just after the fault clearance (i.e. $P_{max}(U_{final})$) must be greater than the power transferred prior to the fault occurrence (P_A^o). (It has been assumed that P_B and P_C remain unaffected by the low dc voltage during the ac fault and hence will remain the same as the pre-fault levels). The critical dc voltage corresponds to the moment when the power transfer capability ($P_{\max}$) equals the power demand (P_A) of the dc grid as seen from terminal-A (i.e. P_A^o). This is mathematically given as

$$U_{critical} = \frac{P_A^o}{I_{max}} = \frac{P_A^o}{kI_N} \tag{4.8}$$

where the factor k describes dc overcurrent capability in terms of the rated dc current for terminal-A. I_{max} is a known fixed value for a converter and P_A has

already been considered as a known value. hence, the critical dc voltage ($U_{critical}$) can be computed right away from (4.8). Once $U_{critical}$ is known, the critical clearing time ($\Delta t_{critical}$) can computed by equation (4.6).

To corroborate the validity of the large-disturbance stability analysis approach promoted so far, we will analyze impact of ac grid fault on a the five-terminal dc grid example case shown in Fig. 4.16. The power rating and the dc-bus capacitances of

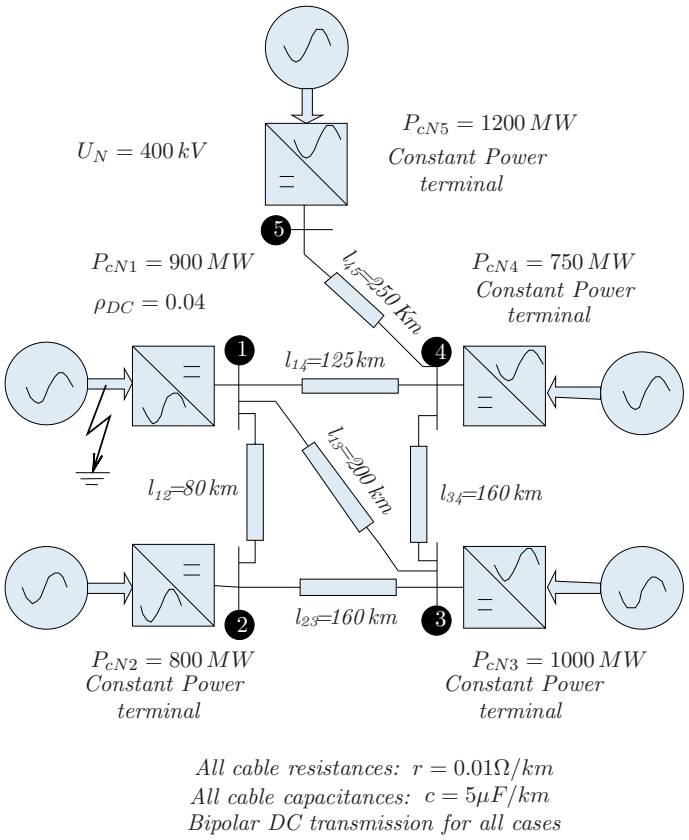


Figure 4.16: Five-terminal VSC-HVDC

each terminal are given in Table 4.1.

Terminal-1 in Fig. 4.16 is equipped with dc over-current controller which will limit the dc current from exceeding 1.1 times the rated dc current (i.e., $I_{max} = 1.1 \times$

Table 4.1: Parameters and initial steady-state of the MTDC simulation in Fig. 4.16

Terminal No.	1	2	3	4	5
P_{cN} (MW)	900	800	1000	750	1200
U_N (kV)	400	400	400	400	400
P_c^o (kV)	838	-400	690	-600	-513
U^o (kV)	401.10	400.12	401.34	397.26	394.14
Control type	dc voltage droop ($\rho_{DC} = 0.04$)	constant power	constant power	constant power	constant power
$C_b\,(\mu F)$	113	100	125	94	80
$\sum C_L\,(\mu F)$	$\frac{1}{2}\,(80 + 200 + 125 + 160 + 160 + 250)$ km $\times$ $5\mu F/\text{km} = 2438\,\mu F$				
$C_{agg}\,(\mu F)$	$\sum C_b + \sum C_L = 2950\,\mu F$				

$(900/400) = 2.475\,\text{kA})$). A three phase to ground fault is applied to the ac grid behind terminal-1 such that the power delivered to the dc grid is reduced from the pre-fault level of 840 MW to just about 120 MW. The critical dc voltage, based on (4.8) becomes

$$U_{critical} = \frac{P_1^o}{I_{max}} = \frac{840}{2.475} \simeq 340\,\text{kV} \tag{4.9}$$

Inserting relevant parameters from Table 4.1 into (4.6), the critical clearing time is computed as

$$\left.\begin{aligned} \Delta t_{critical} &= \frac{C_{agg}\left({U_{initial}}^2 - {U_{critical}}^2\right)}{2\left(P_1^o - P_1'\right)} \\ &= \frac{2950\times10^{-6}\left(400^2 - 340^2\right)}{2(840-120)} \\ &= 0.091\,\text{s} \end{aligned}\right\} \tag{4.10}$$

Now let us compare the critical clearing time computed analytically in (4.10) with simulation results of different ac fault cases (i.e. different fault durations and different fault severities). In order for an ac fault to cause reduction of power flow of converter-A from 840 MW to 120 MW, the ac fault must result in a voltage dip of $(840 - 120)/840 \simeq 86\%$. A fault resistance of $0.1\,\Omega$ was observed to give the required severity of ac fault. (This depends on several factors which includes the MVA ratings and internal reactances of the synchronous generators constituting the ac grid and also on the impedances of the ac line connected to the spot where fault occurs.)

Case 1: MTDC response to a three-phase fault resulting in 86% *voltage dip at terminal-1 and fault duration of* $\Delta t = 70\,ms$

A fault duration of $\Delta t = 70\,\text{ms}$ is applied in this case. Three-phase fault behind converter-1 is applied with a fault resistance of $0.1\,\Omega$ (corresponding to 86% voltage dip). Simulation results are shown in Fig. 4.17. The plots in Fig. 4.17 show that the

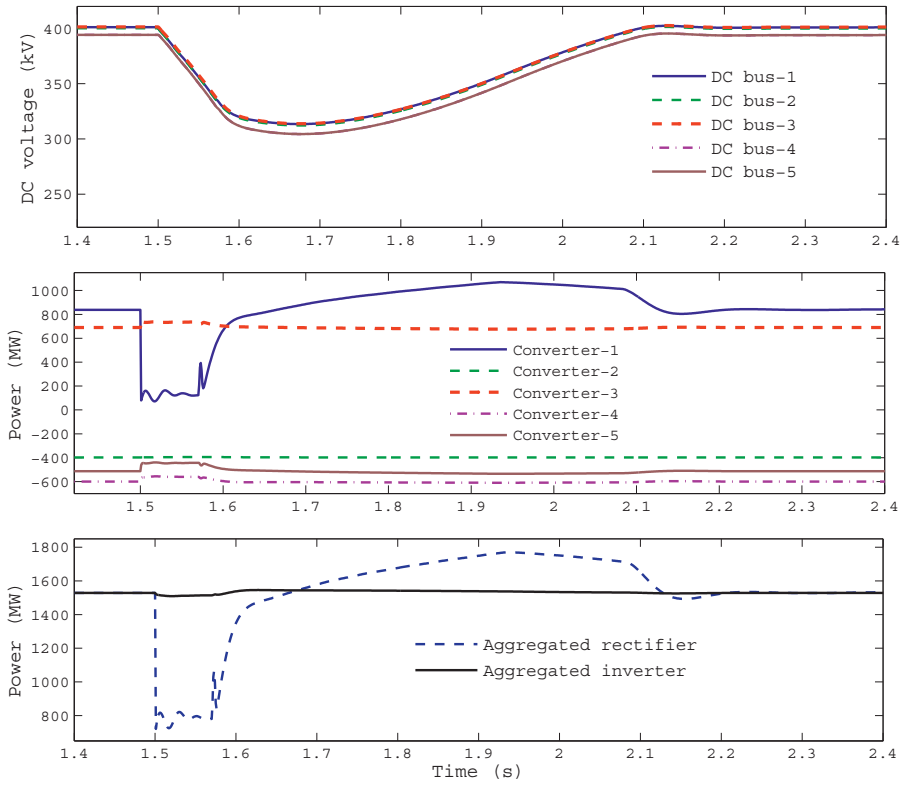


Figure 4.17: MTDC response to a three-phase fault resulting in 86% voltage dip at terminal-1 and fault duration of $\Delta t = 70\,\text{ms}$

dc grid recovers from the fault in about 500 ms to 600 ms duration after clearance of the ac fault. The third/bottom plot in the figure shows the power flow of aggregated rectifiers (converters 1 and 3) and aggregated inverters (converters 2, 4 and 5). Energy discharged from the aggregated capacitances during the fault duration and energy restored to the capacitances latter can be seen in the third plot of same figure. (i.e. the two areas enclosed by the solid and broken lines). The dc grid remains stable after fault clearance.

Case 2: MTDC response to a three-phase fault resulting in 86% *voltage dip at terminal-1 and fault duration of* $\Delta t = 85\,ms$

A fault duration of $\Delta t = 85\,\text{ms}$ is applied in the second case. The fault resistance is kept unchanged (i.e. $0.1\,\Omega$, corresponding to 86% voltage dip). Simulation results are shown in Fig. 4.18. The plots in Fig. 4.17 show that the dc grid needs

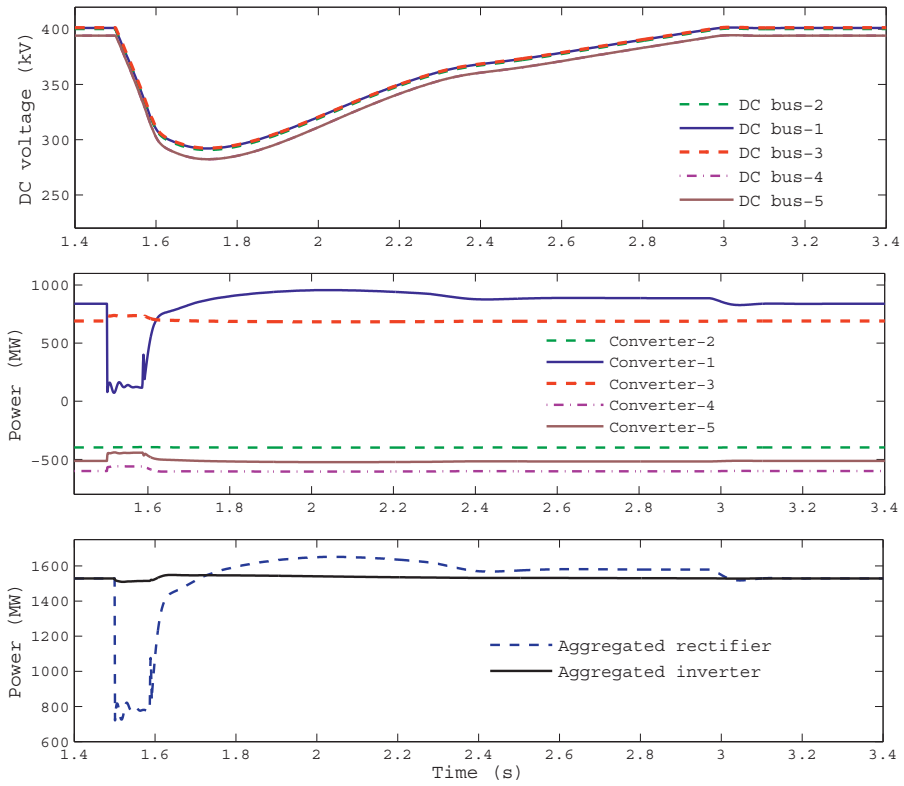


Figure 4.18: MTDC response to a three-phase fault resulting in 86% voltage dip at terminal-1 and fault duration of $\Delta t = 85\,\text{ms}$

considerably longer time to fully recover (i.e. 1.5 s) compared to the previous case (600 ms). This is because the fault clearing time in the second case (i.e. $\Delta t = 85\,\text{ms}$) is considerably closer to the critical clearing time ($\Delta t_{critical} = 91\,\text{ms}$ from (4.10)) in contrast with the fault clearing time in the first case ($\Delta t = 70\,\text{ms}$). The system eventually remains stable though.

Case 3: MTDC response to a three-phase fault resulting in 86% voltage dip at terminal-1 and fault duration of $\Delta t = 90$ ms

The fault duration is now extended to $\Delta t = 90$ ms. The fault resistance remains the same as in the previous two cases. Simulation results are shown in Fig. 4.19. As can be seen from the plots of Fig. 4.19, the ac fault in this case has resulted

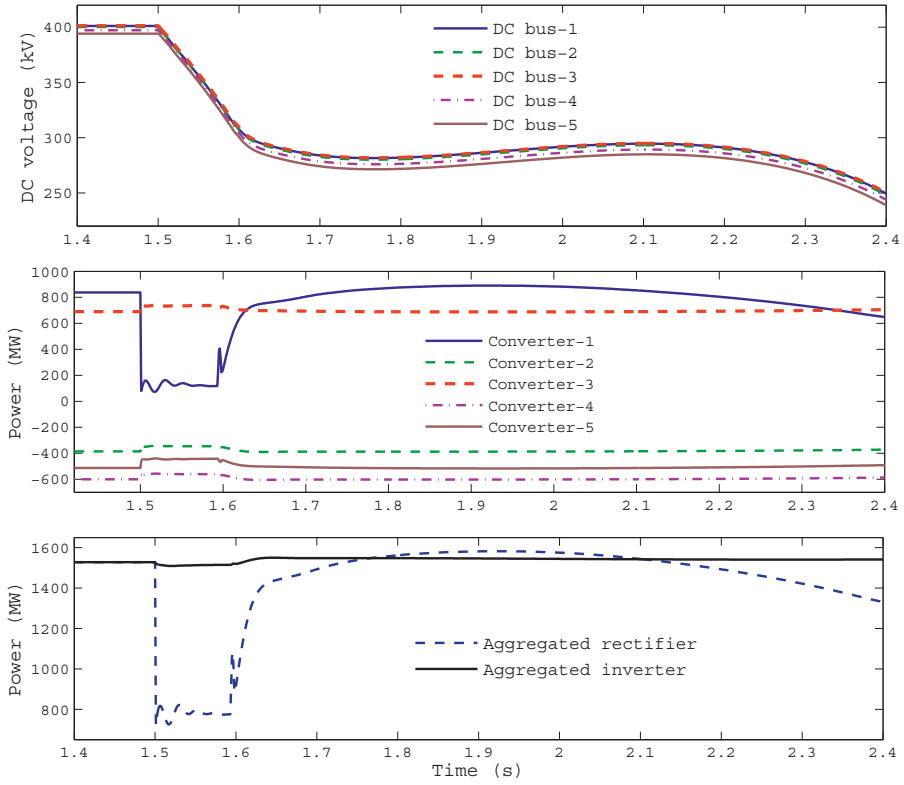


Figure 4.19: MTDC response to a three-phase fault resulting in 86% voltage dip at terminal-1 and fault duration of $\Delta t = 90$ ms

in dc voltage collapse. The third/bottom plot in the same figure shows that the aggregated rectifier barely covers the power demand right after fault clearance. It is well known that fault clearance in ac systems is almost always followed by ac overvoltage for a short period of time. It was observed in the simulation study that this ac overvoltage results in a slight increment of power injected into dc grid via VSC-HVDC terminal. This additional boost, however, damps out rather quickly

and the power supply from the rectifier falls short of meeting the power demand once again, eventually leading to dc voltage instability (collapse).

Case 4: MTDC response to a three-phase fault resulting 43% *voltage dip at terminal-1 and fault duration of* $\Delta t = 90\,ms$

Now the fault duration is kept the same as in the last case (i.e. $\Delta t = 90\,\text{ms}$). The fault resistance, however, is changed to $0.4\,\Omega$ (corresponding to 43% voltage dip). Power flow via converter-1 reduces to from 840 MW to 400 MW. As a result the critical clearing time increases to $\Delta t_{critical} = 150\,\text{ms}$. This means that a fault duration of $\Delta t = 90\,\text{ms}$ (which was calculated in (4.10)) must be tolerated by the MTDC system. Simulation results are shown in Fig. 4.20.

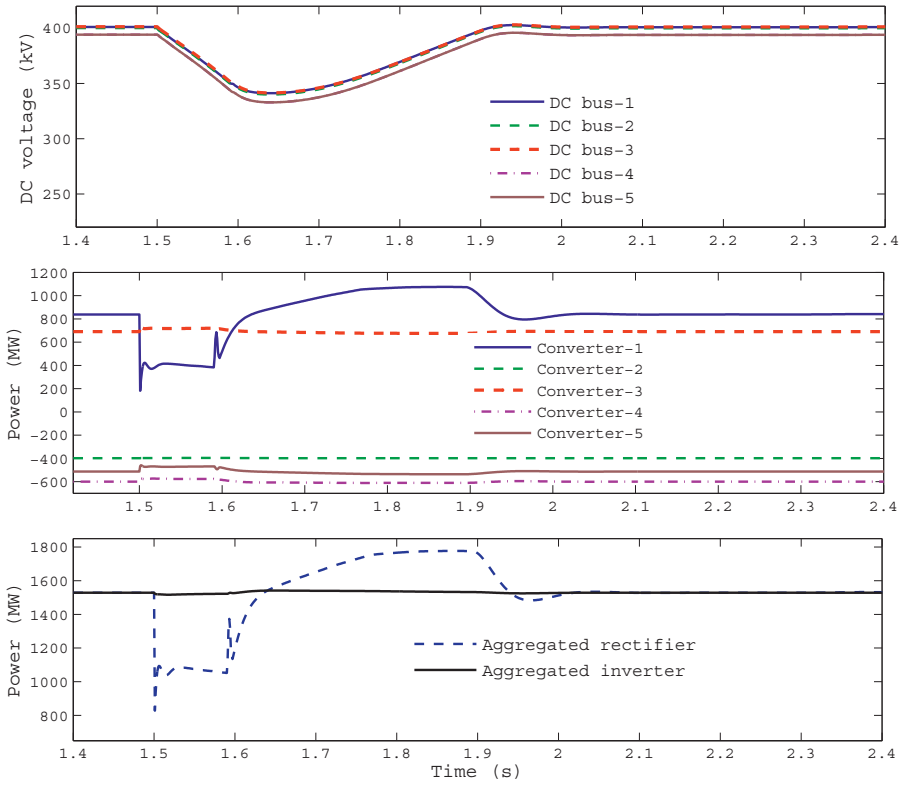


Figure 4.20: MTDC response three-phase fault of 43% voltage dip and fault duration of $\Delta t = 90\,\text{ms}$

As observed from the time plots in Fig. 4.20, the MTDC has managed to recover from the ac fault in approximately 600 ms.

The simulation studies discussed above validate the dc voltage stability analysis approach proposed in this thesis. The critical fault clearing time determines the capacity limit of the MTDC to recover from an ac fault occurring behind a rectifier. Caution should be taken, however, that the converter terminal may trip earlier due to inability of the phase locked loop (PLL) of the converter to synchronize to the ac phase voltages during the fault occurrence. This is of particular concern when the fault is unbalanced, severe and/or the fault causes noises in the voltage measurements of the PLL. In addition to this, the dc voltage collapse and/or the shut down of the entire dc grid will have consequences on the connected ac grids. These secondary effects are out of the scope of the discussion in this section and hence will not be further discussed.

4.2 Small-signal Stability Analysis

The use of the state-space modeling approach facilitates understanding the dynamics of the entire multi-terminal VSC-HVDC system by giving a complete picture of the system dynamics in terms of eigenvalues and transfer functions. This can, for example, be used for tuning of the converter controllers. Small-signal analysis of MTDC has been presented in the literature [32],[68],[26],[14]. In all previous cases, however, the analyses were done based on specific dc grid topologies and by listing down all the of differential equations describing the MTDC system before coming up with the state-matrices. For meshed topologies of more than four terminals this approach becomes very laborious to say the least. The state-space modeling approach that will be presented here attempts to take into account all possible control schemes of individual VSC-HVDC terminals. Moreover, an arbitrary meshed dc grid topology will be considered in the analysis. Some possible topologies of MTDC are discussed in [70],[92].
A schematic representation of VSC-HVDC with bi-polar dc transmission is shown in Fig. 4.21. Two measurement points (A and B shown in Fig. 4.21) are used for ac side and dc side of the converter respectively. Point 'A' refers to the PCC (point of common coupling between converter and ac grid) whereas point 'B' refers to the dc-bus of the converter. The sign convention applied for all power and current measurements of the converter is in such a way that current/power measured at a converter terminal will be positive if it is flowing from the ac grid to the dc grid via the converter station (like in the previous cases of this thesis). This means that positive power (P_c', P_c, P_x, P_y) corresponds to rectifier mode of operation and negative power corresponds to inverter mode of operation.

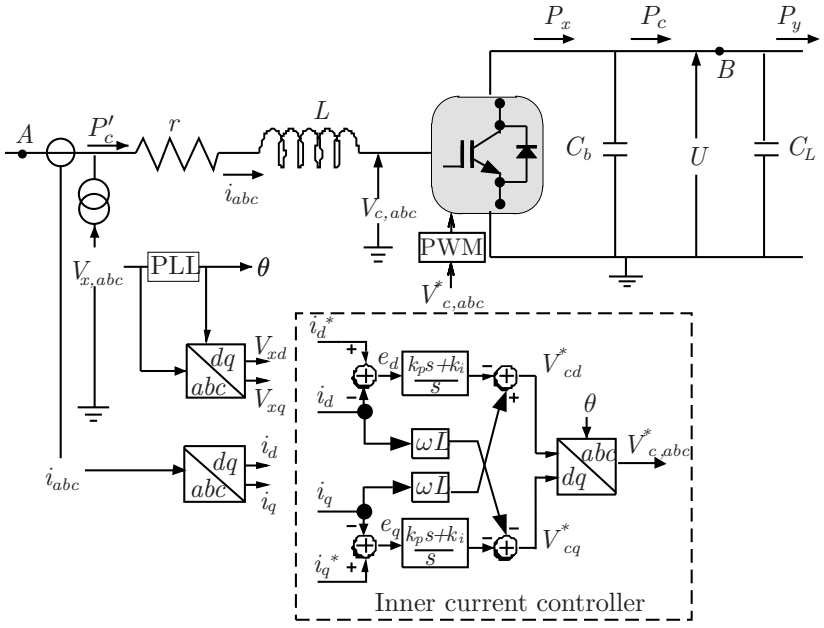


Figure 4.21: Schematic of VSC control

Symbols and parameters used in Fig. 4.21 are listed in Table 4.2.

Table 4.2: List of symbols used in Fig. 4.21

P_c	Power measurement of the converter at the dc-bus (point B);
P_x	Power behind the dc-bus filter capacitance;
P_y	Power beyond the dc line capacitance;
PLL	Phase locked loop;
i_{abc}	3-phase ac current measurement at PCC;
$V_{x,abc}$	3-phase ac voltage measurement at PCC;
$V_{c,abc}$	3-phase ac voltage output of VSC; (internal VSC voltage)
U	dc voltage measurement;
ω	Synchronous frequency in rad/s;
L, r	Series filter inductance and resistance;
C_b	dc filter capacitance;
C_L	DC line aggregate capacitance;

VSC control has already been discussed in depth in chapter two. Hence, here only control aspects which are relevant to small-signal stability study of dc grid will be discussed.
The relation between P_c' and P_x is given by

$$P_c' - P_x = P_{Loss} \tag{4.11}$$

where P_{Loss} refers to the total converter power losses (refer to section 3.2).

Analytical expression of the converter power loss (P_{Loss}) can be established either based on empirical data of the losses of VSC-HVDC in operation or by adding up power losses in individual components of the semiconductors and the ac filters (refer to section 3.2). From such equation relating the two quantities, a linearized expression about a steady-state operating point can be derived:

$$P_x = k_t P_c' \tag{4.12}$$

where the factor k_t is proportionality constant which gives information about the marginal power conversion efficiency of the VSC-HVDC station. Ignoring the decoupling term in Fig. 2.13 (or Fig. 4.21), the active current (i_d) controller can be represented by Fig. 4.22, where K_A and T_A are the proportional gain and integral time-constant of the PI controller whereas s refers to the Laplace transformation parameter.

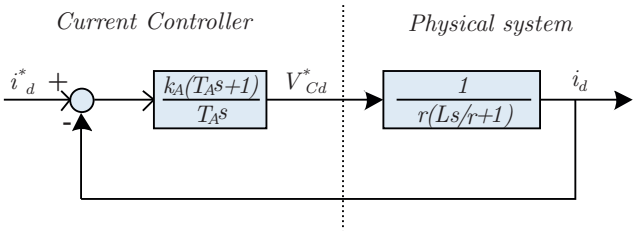


Figure 4.22: Simplified block diagram of active current controller

The pole placement tuning method of the PI controller in Fig. 4.22 gives $K_A T_A = L/r$. This results in the open-loop-gain, $H_{OL}(s)$, given by

$$H_{OL}(s) = \frac{1}{rT_A s} \tag{4.13}$$

Hence, taking (4.13) into consideration, further simplification of Fig. 4.22 gives Fig. 4.23.

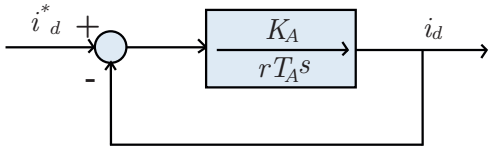


Figure 4.23: Simplified representation of the closed loop current controller

4.2.1 Small-signal Modeling of Outer Controllers

Small-signal Modeling of Constant Power Controller

If the ac voltage at the PCC is does not show large variations under normal circumstances, the active current controller also behaves more or less like constant power controller. In this case there may be no need for an additional power controller. However, if the ac voltage shows variation in magnitude, it necessitates adding an outer controller for active power control. In such a case, there will be two options for the feedback in the controller, i.e. either the ac side power measurement (P'_c) or the dc side power measurement (P_c) can be used as a feedback of power measurement. In Fig. 4.21, P_x is dc power behind the dc filter capacitance and hence is not accessible for measurement. Similarly P_y is dc power to the right of the equivalent dc line capacitance (C_L) and hence is not accessible for measurement. This means that P_x and P_y should be estimated from other measurable dc-bus signals (i.e. P_c and U). Power controller with feedback from ac side is shown in Fig. 4.24.

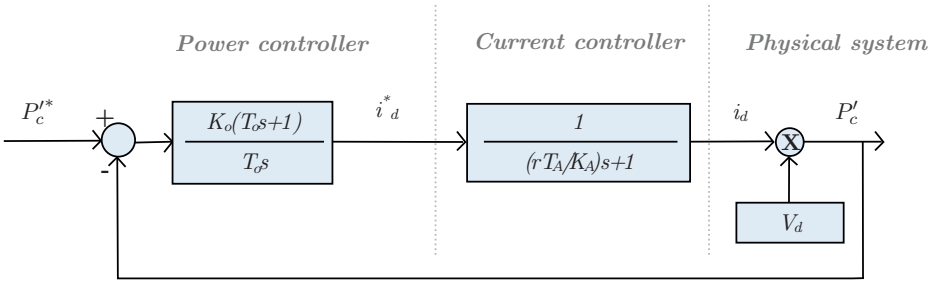


Figure 4.24: Closed loop power controller with feedback power coming from ac side (measurement at PCC)

If the block diagram in Fig. 4.24 is used to control the dc-bus power (P_c), the ac/dc power conversion factor k_t, should be taken into account to compute the dc

side power (P_c) (As discussed in section 3.2 the actual value of k_t depends on the operating point). This can be done by introducing a loss-compensation gain block as in Fig. 4.25. If power measured at the dc-bus (P_c) is used in the controller, the simplified block diagram of the controller will look like Fig. 4.26. Coincidentally

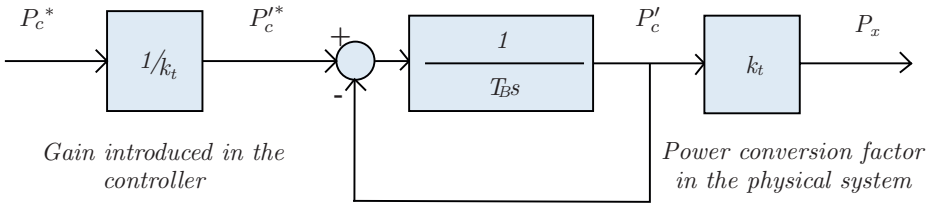


Figure 4.25: Dc-side power control by using ac-side power feedback

further simplification of Fig. 4.25 also gives Fig. 4.26. From Fig. 4.27, the dynamic

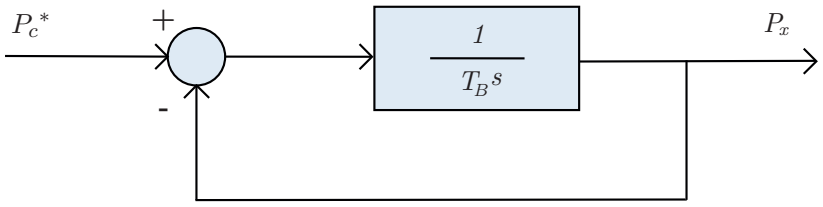


Figure 4.26: Constant power control with dc measurement feedback. This also can be simplified form of the power controller shown in Fig. 4.25

relation between the input (P_c^*) and the output (P_x)is given by (4.14).

$$\frac{dP_x}{dt} = \frac{1}{T_B} P_c^* - \frac{1}{T_B} P_x \tag{4.14}$$

In the case of power controller with feedback from dc-bus measurement (i.e. P_c), the control dynamics will be affected by charging/discharging of the dc filter capacitance (C_b) as well as the equivalent dc line capacitance (C_L). This is shown in Fig. 4.27.

By linearizing the system about a specific operating point (i.e. $U = U^o + \Delta U$), Fig. 4.27 is simplified as in Fig. 4.28. $U = U^o$ refers to the initial steady-state dc-bus voltage at the point of linearization (i.e. the steady-state dc-bus voltage prior to the small-signal perturbation). From Fig. 4.28, the dynamics of the power exchange

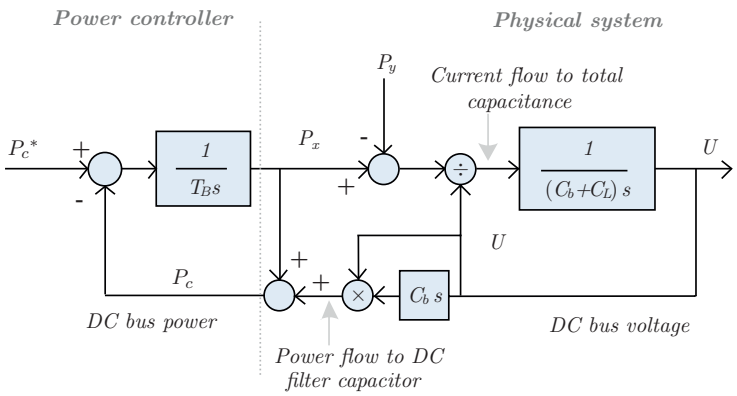


Figure 4.27: Block diagram of VSC-HVDC power control with power feedback from dc-bus measurement

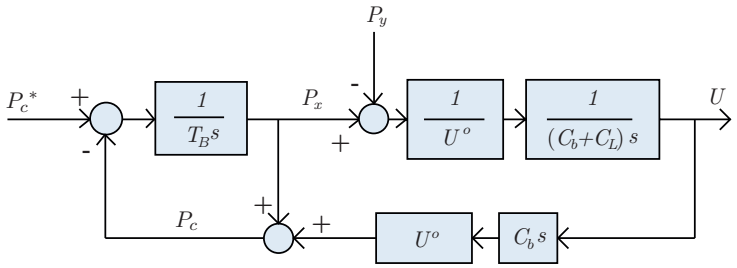


Figure 4.28: Linearization of the constant power controller in Fig. 4.27

with the capacitances C_b and C_L is given by (4.15).

$$\left.\begin{aligned} P_c &= P_x + \tfrac{C_b}{C_b+C_L}\,(P_x - P_y) \\ &= \left(1 + \tfrac{C_b}{C_b+C_L}\right) P_x - \left(\tfrac{C_b}{C_b+C_L}\right) P_y \end{aligned}\right\} \tag{4.15}$$

Furthermore, the control dynamics is given by (4.16).

$$\left.\begin{aligned} \tfrac{dP_x}{dt} &= \tfrac{1}{T_B}\,(P_c^* - P_c) \\ &= -\tfrac{1}{T_B}\left(\tfrac{2C_b+C_L}{C_b+C_L}\right) P_x + \tfrac{1}{T_B}\left(\tfrac{C_b}{C_b+C_L}\right) P_y + \tfrac{1}{T_B} P_c^* \end{aligned}\right\} \tag{4.16}$$

Small-signal Modeling of DC Voltage Droop Controller

The dc voltage droop controller is a modified version of the power controller where a dc-bus voltage droop signal is added to the power reference. Dc voltage droop controller has been discussed in detail in chapter 2 of this thesis. Like in the case of the power controller, the dc voltage droop controller may consist of power feedback either from the ac side or from the dc side. This is shown in Fig. 4.29 where two alternatives are shown for the power feedback; one for dc power feedback, P_c, and the other for ac power feedback, P_x, (compare this with Fig. 4.25, Fig. 4.26 and Fig. 4.27). From Fig. 4.29, the control dynamic equation for the dc droop controller

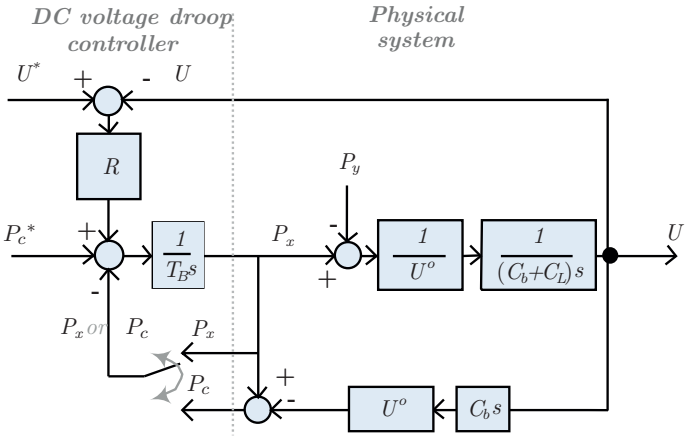


Figure 4.29: Linearized model of dc voltage droop controller

using ac power feedback, is given by (4.17).

$$\frac{dP_x}{dt} = -\frac{1}{T_B}P_x - \frac{R}{T_B}U + \frac{1}{T_B}P_c^* + \frac{R}{T_B}U^* \tag{4.17}$$

Similarly, if the dc power feedback, P_c, is used, the corresponding dynamic equation becomes as in (4.18).

$$\frac{dP_x}{dt} = -\frac{1}{T_B}\left(\frac{C_b}{C_b + C_L}\right)P_x - \frac{R}{T_B}U - \frac{1}{T_B}\left(\frac{C_b}{C_b + C_L}\right)P_y + \frac{1}{T_B}P_c^* + \frac{R}{T_B}U^* \tag{4.18}$$

Small-signal model of constant dc voltage control

In chapter 2 it was discussed that constant dc voltage control involves PI controllers. In the lower frequency range the integral gain is more dominant, compared to the proportional gain (if there is any), in the overall system dynamics and hence the

proportional part will be ignored in the discussion below. A block diagram representation of dc voltage regulator is shown in Fig. 4.30, where T_C refers to the time-constant of the dc voltage regulator. Note that the proportional gain in the controller is neglected in the figure.

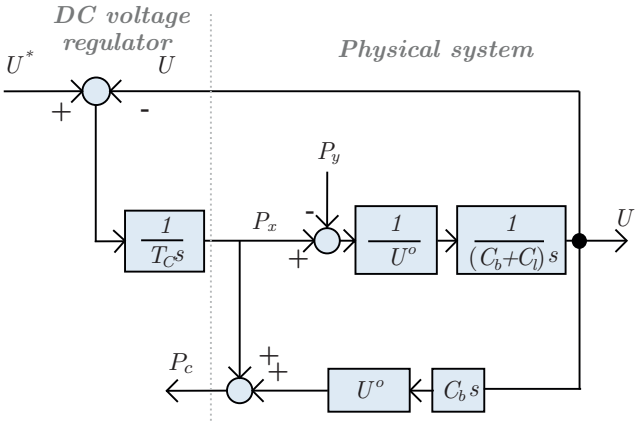


Figure 4.30: Linearized model of constant dc voltage controller

The dynamic equation describing the controller in Fig. 4.30 is given by (4.19).

$$\frac{dP_x}{dt} = -\frac{1}{T_C}U + \frac{1}{T_C}U^* \tag{4.19}$$

4.2.2 Generalized Mathematical Representation of VSC-HVDC Controllers

A VSC-HVDC terminal connected to an active ac grid can have either of the control modes discussed in section 4.2.1. VSC-HVDC terminal connected to a passive grid on the other hand need to control only ac terminal voltage and the power flow is determined by the ac loads connected to the passive ac grid. Hence, although the control method is different, VSC-HVDC connected to passive grid also appears as a constant power controlled terminal (with ac power feedback) when looked from the dc grid side. Therefore, VSC-HVDC terminal connected to a passive grid can be represented as constant power VSC-HVDC connection to an active ac grid, with the load in the ac grid replacing the converter power reference, P_c^*. Hence we can safely consider that the controllers in Fig. 4.26, Fig. 4.28, Fig. 4.29 and Fig. 4.30

can represent all possible cases of VSC-HVDC control modes, including passive grid connection. From (4.14), (4.16), (4.17), (4.18) and (4.19), the control dynamics of all modes of VSC-HVDC control can be described by the generalized expression given by

$$\frac{dP_x}{dt} = aP_x + bU + cP_y + dP_c^* + eU^* \tag{4.20}$$

where the coefficients a, b, c, d and e are given by Table 4.3 for the different types of VSC-HVDC control modes.

Table 4.3: List of coefficients in equation (4.20) for various control modes.

Parameter	Constant power with feedback from		Dc voltage droop with feedback from		Constant dc voltage
	AC side Fig. (4.26) (Type-1)	DC side Fig. (4.28) (Type-2)	AC side Fig. (4.29) (Type-3)	DC side Fig. (4.29) (Type-4)	Fig. (4.30) (Type-5)
a	$-\frac{1}{T_B}$	$-\frac{1}{T_B}\left(\frac{2C_b+C_L}{C_b+C_L}\right)$	$-\frac{1}{T_B}$	$-\frac{1}{T_B}\left(\frac{2C_b+C_L}{C_b+C_L}\right)$	0
b	0	0	$-\frac{R}{T_B}$	$-\frac{R}{T_B}$	0
c	0	$\frac{1}{T_B}\left(\frac{C_b}{C_b+C_L}\right)$	$-\frac{1}{T_C}$	$\frac{1}{T_B}\left(\frac{C_b}{C_b+C_L}\right)$	0
d	$\frac{1}{T_B}$	$\frac{1}{T_B}$	$\frac{1}{T_B}$	$\frac{1}{T_B}$	0
e	0	0	$\frac{R}{T_B}$	$\frac{R}{T_B}$	0

4.2.3 DC Grid Modelling

The continuous line parameters of the dc link are often modeled by single or multiple π-equivalent sections which consist of lumped parameters. With the number of π-sections, the accuracy of the model increases while at the same time computational requirements for analyzing the model also increase tremendously. In the dc grid modeling approach proposed here, we will consider only a single π-section for each dc line (branch). Moreover the line inductances will be ignored here. This takes the assumption that the dc lines consist of cables (and not overhead lines) and hence the line inductances will be very small and the line capacitances will be very large. If overhead lines are used for one or more of the dc transmission lines, the opposite will be true; i.e. there will be large line inductances and small line capacitances. Hence the application of the dc grid modeling promoted here will be restricted to all-cable dc grid system.

In Fig. 4.31, l refers to transmission length in km; r and c refer to line resistance in Ω/km and line capacitance in $\mu F/km$ respectively. The line capacitances of all the dc lines connected to the dc-bus of i^{th} terminal add up to the aggregate dc line capacitance (C_{Li}), as shown in Fig. 4.31. N represents the total number of terminals in the dc grid.

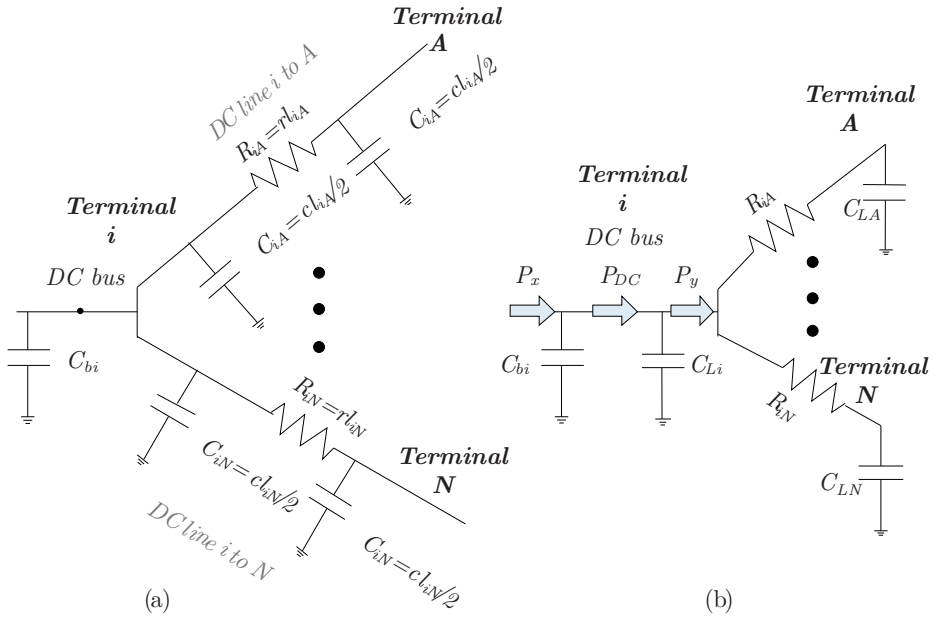


Figure 4.31: Aggregating the dc line capacitances: (a) dc-bus connected to multiple dc lines (b) aggregation of dc line capacitances

The shunt capacitance of the i^{th} terminal (C_i) represents the sum of the dc filter capacitance (C_{bi}) and the aggregate of the line capacitances (C_{Li}), as given by

$$C_i = C_{bi} + C_{Li} \tag{4.21}$$

By applying the π-equivalent model to all dc transmission lines, the dc grid is modeled by a pure resistive network and shunt capacitance connections at each of the dc terminal points, as shown in Fig. 4.32.

In Fig. 4.32 the power P_{yi} refers to the dc power injection from i^{th} dc terminal into the resistive network whereas the power vector P_{xi} refers to power flowing from i^{th}

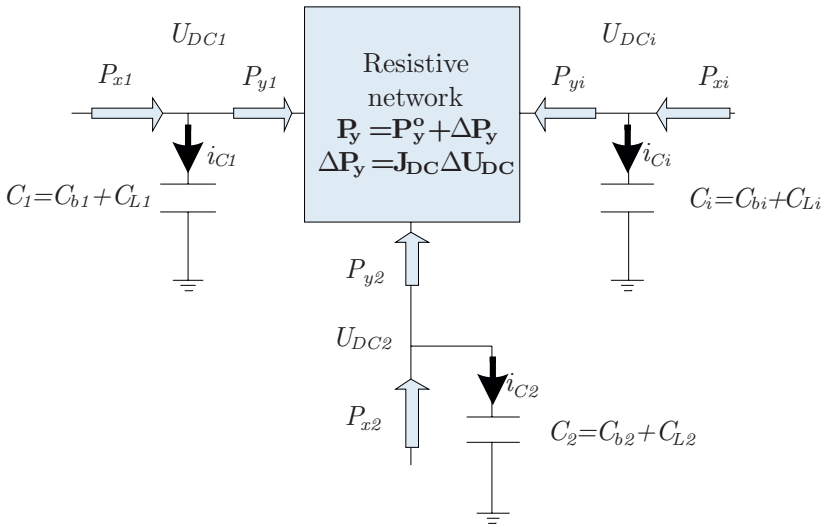


Figure 4.32: DC grid modeling based on π-equivalent model of dc lines

HVDC converter into the dc network plus the shunt equivalent capacitance. The power flow exchange for i^{th} terminal with the capacitance, C_i, is given by

$$P_{xi} - P_{yi} = U_i i_{Ci} = U_i C_i \frac{dU_i}{dt} \tag{4.22}$$

Now let the notations P_{xi}^o, P_{yi}^o and U_i^o represent the initial steady-states of the i^{th} dc terminal. For a small-signal disturbance in the vicinity of the initial steady-state point, these three variables are given by

$$\left.\begin{array}{l} P_x = P_x^o + \Delta P_x \\ P_y = P_y^o + \Delta P_y \\ U = U^o + \Delta U \end{array}\right\} \tag{4.23}$$

where the notation Δ represents the small-signal changes. From (4.22) and (4.23), the power exchange with the shunt capacitances is re-written as

$$P_{xi}^o + \Delta P_{xi} - \left(P_{yi}^o + \Delta P_{yi}\right) = U_i^o C_i \frac{d\left(U_i^o + \Delta U_i\right)}{dt} \tag{4.24}$$

At steady-state there will be no power exchange with the shunt capacitances and hence the relation $P_{xi}^o = P_{yi}^o$. Moreover U_i^o is a fixed value. Hence equation (4.24),

is simplified as

$$\frac{d}{dt}\Delta U_i = \left(\frac{1}{U_i^o C_i}\right)\Delta P_{xi} - \left(\frac{1}{U_i^o C_i}\right)\Delta P_{yi} \tag{4.25}$$

Let the term in the bracket, in equation (4.25), be represented by F_i, as

$$F_i = \frac{1}{U_i^o C_i} \tag{4.26}$$

Substituting (4.26) into (4.25), we get the relation given by

$$\frac{d}{dt}\Delta U_i = F_i \Delta P_{xi} - F_i \Delta P_{yi} \tag{4.27}$$

4.2.4 Generalized State-space Modeling of Multi-terminal VSC-HVDC

So far all the mathematical analysis has been used to describe what happens in a single VSC-HVDC terminal. In order to consolidate the mathematical relations derived in section 4.2.2 and section 4.2.3 into a single state-space representation, the use of vector notation becomes necessary (as was done in section 3.3.2). The vector variables will be represented by bold letters to differentiate from the scalar variables equivalents which are written in italics. For example the vector representing the dc terminal voltages is represented by $\mathbf{U}$. Similarly the vectors $\mathbf{P_x}$ and $\mathbf{P_y}$ refer to the set of dc-bus powers behind shunt capacitances and after shunt capacitances respectively:

$$\mathbf{U} = \begin{bmatrix} U_1 \\ \vdots \\ U_i \\ \vdots \\ U_n \end{bmatrix}, \quad \mathbf{P}_x = \begin{bmatrix} P_{x1} \\ \vdots \\ P_{xi} \\ \vdots \\ P_{xn} \end{bmatrix}, \quad \mathbf{P}_y = \begin{bmatrix} P_{y1} \\ \vdots \\ P_{yi} \\ \vdots \\ P_{yn} \end{bmatrix} \tag{4.28}$$

Similar definitions of vector notation discussed above also apply to other variables ($\Delta\mathbf{P}_x$, $\Delta\mathbf{P}_y$, $\Delta\mathbf{P}_c$, $\Delta\mathbf{U}$, $\Delta\mathbf{U}^*$,...). Now with these vector notations kept in mind, the power flow in the resistive dc network, given by the vector $\mathbf{P}_y$, can described by

$$\mathbf{P}_y = \mathbf{P}_y{}^o + \Delta\mathbf{P}_y \tag{4.29}$$

$$\Delta\mathbf{P}_y = \mathbf{J}_{DC}\Delta\mathbf{U} \tag{4.30}$$

where the matrix $\mathbf{J}_{DC}$ is the dc Jacobian matrix given by

$$\mathbf{J}_{DC} = \frac{\partial\mathbf{P}_y}{\partial\mathbf{U}} \tag{4.31}$$

These relations are also shown in Fig. 4.32. Equation (4.31) is re-written, in vector form, as

$$\frac{d}{dt}\Delta\mathbf{U} = diag\left(\mathbf{F}\right)\Delta\mathbf{P}_x - diag\left(\mathbf{F}\right)\Delta\mathbf{P}_y \tag{4.32}$$

where *diag* refers to the matrix diagonalization operator. Substituting (4.30) in (4.32), the following expression is obtained:

$$\frac{d}{dt}\Delta\mathbf{U} = diag\left(\mathbf{F}\right)\Delta\mathbf{P}_x - diag\left(\mathbf{F}\right)\mathbf{J}_{DC}\Delta\mathbf{U} \tag{4.33}$$

The small-signal equivalent of the generalized control dynamic expression given by (4.20) is written in vector form as

$$\begin{array}{l} \frac{d}{dt}\Delta\mathbf{P}_x = diag\left(\mathbf{a}\right)\Delta\mathbf{P}_x + diag\left(\mathbf{b}\right)\Delta\mathbf{U} \\ \quad + diag\left(\mathbf{c}\right)\Delta\mathbf{P}_y + diag\left(\mathbf{d}\right)\Delta{\mathbf{P}_c}^* + diag\left(\mathbf{e}\right)\Delta\mathbf{U}^* \end{array} \tag{4.34}$$

Substituting (4.30) in (4.34), we get

$$\begin{array}{l} \frac{d}{dt}\Delta\mathbf{P}_x = diag\left(\mathbf{a}\right)\Delta\mathbf{P}_x + \left(diag\left(\mathbf{b}\right) + diag\left(\mathbf{c}\right)\mathbf{J}_{DC}\right)\Delta\mathbf{U} \\ \quad + diag\left(\mathbf{d}\right)\Delta{\mathbf{P}_c}^* + diag\left(\mathbf{e}\right)\Delta\mathbf{U}^* \end{array} \tag{4.35}$$

From (4.33) and (4.35), the state-space representation of the entire multi-terminal VSC-HVDC system becomes

$$\underbrace{\frac{d}{dt}\begin{bmatrix}\Delta\mathbf{P}_x \\ \Delta\mathbf{U}\end{bmatrix}}_{\frac{d}{dt}\mathbf{X}} = \underbrace{\begin{bmatrix}\mathbf{A}_{11} & \mathbf{A}_{12} \\ \mathbf{A}_{21} & \mathbf{A}_{22}\end{bmatrix}}_{\mathbf{A}}\underbrace{\begin{bmatrix}\Delta\mathbf{P}_x \\ \Delta\mathbf{U}\end{bmatrix}}_{x} + \underbrace{\begin{bmatrix}\mathbf{B}_{11} & \mathbf{B}_{12} \\ \mathbf{B}_{21} & \mathbf{B}_{22}\end{bmatrix}}_{\mathbf{B}}\underbrace{\begin{bmatrix}\Delta{\mathbf{P}_c}^* \\ \Delta\mathbf{U}^*\end{bmatrix}}_{\upsilon} \tag{4.36}$$

where the sub-matrices $\mathbf{A}_{11}$ ... $\mathbf{B}_{22}$ are given by

$$\left.\begin{array}{ll} \mathbf{A}_{11} = diag\left(\mathbf{a}\right), & \mathbf{A}_{12} = diag\left(\mathbf{b}\right) + diag\left(\mathbf{c}\right)\mathbf{J_{DC}} \\ \mathbf{A}_{21} = diag\left(\mathbf{F}\right), & \mathbf{A}_{22} = -diag\left(\mathbf{F}\right)\mathbf{J_{DC}} \\ \mathbf{B}_{11} = diag\left(\mathbf{d}\right), & \mathbf{B}_{12} = diag\left(\mathbf{e}\right) \\ \mathbf{B}_{21} = [0]_{n\times n}, & \mathbf{B}_{22} = [0]_{n\ \times n} \end{array}\right\} \tag{4.37}$$

In (4.37) n refers to the number of VSC-HVDC terminals in the dc grid. From (4.36) it can be noticed that the state-variables are the nodal dc voltages (U) and nodal powers behind the shunt capacitances (P_x). Hence n-terminal VSC-HVDC system is represented by $2n$ state-variables. From the state-matrix ($\mathbf{A}$) the eigenvalues of the system can be computed. Applying Laplace transformation, the transfer function between input vector υ and state-variable vector $\mathbf{x}$ is given by

$$\mathbf{H}\left(s\right) = \frac{\mathbf{x}\left(s\right)}{\upsilon\left(s\right)} = \left(s\mathbf{I} - \mathbf{A}\right)^{-1}\mathbf{B} \tag{4.38}$$

where $\mathbf{I}$ refers to identity matrix. From (4.36), the steady-state response (i.e. when $s = 0$) input-output relation becomes

$$\begin{bmatrix} \mathbf{\Delta P_x} \\ \mathbf{\Delta U} \end{bmatrix} = -\begin{bmatrix} \mathbf{A_{11}} & \mathbf{A_{12}} \\ \mathbf{A_{21}} & \mathbf{A_{22}} \end{bmatrix}^{-1} \begin{bmatrix} \mathbf{B_{11}} & \mathbf{B_{12}} \\ \mathbf{B_{21}} & \mathbf{B_{22}} \end{bmatrix} \begin{bmatrix} \mathbf{\Delta P}^* \\ \mathbf{\Delta U}^* \end{bmatrix} \tag{4.39}$$

Thus so far, a generalized small-signal analysis approach has been presented. The proposed small-signal analysis approach provides a quick way of studying both the dynamic characteristic and steady-state interaction of a multi-terminal VSC-HVDC systems. In the next section the validity of the proposed model is demonstrated by comparing time-responses of the state-space model with simulation results of a detailed PSCAD model for a test multi-terminal VSC-HVDC system.

4.2.5 Small-signal Model Validation by Simulation Studies

The small-signal analysis approach proposed in the previous section will be tested for the example case of a five-terminal VSC-HVDC system shown in Fig. 4.33. Time responses of the state-space model will be compared with the time response of the detailed electro transient model of the same system in PSCAD. In the five-terminal VSC-HVDC model of the simulation, two of the VSC-HVDC terminals (i.e. terminal-3 and terminal-5) are set to be operated in fixed power control mode whereas the other three VSC-HVDC terminals participate in the dc voltage droop control with $\rho_{DC} = 0.04$. Initial steady-state of zero power flow in the dc grid is assumed. This is attained by assigning all dc voltage references to the same value (i.e. 400 kV) and all power references to zero. Table 4.4 summarizes important parameters of the VSC-HVDC terminals in the test dc grid system. The descriptions of controllers Type-1 to Type-4 are given in Table 4.3. From the converter parameters

Table 4.4: Converter and dc terminal parameters of the test case

Terminal No.	1	2	3	4	5
P_{cN} (MW)	900	800	1000	750	640
U_{rated} (kV)	400	400	400	400	400
Control type	Type 3	Type 4	Type 2	Type 3	Type 1
ρ_{DC} (pu/pu)	0.04	0.04	∞	0.04	∞
R (MW/kV)	56.25	50	0	46.88	0
T_B (s)	0.05	0.05	0.05	0.05	0.05
C_b (μF)	113	100	125	94	80
C_L (μF)	405	240	520	405	120
$C = C_b + C_L$ (μF)	518	340	645	499	200

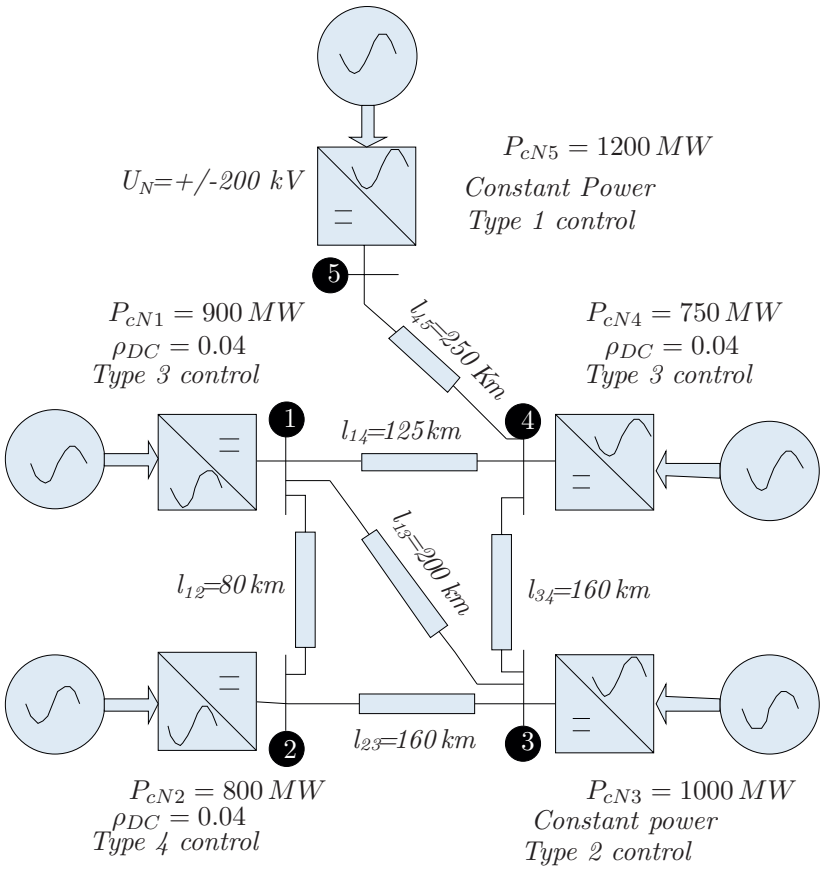


Figure 4.33: A five-terminal VSC-HVDC transmission model used in the simulation study with the employed types of converter controllers

given in Table 4.4, the parameters of equation (4.20) are computed based on Table 4.3, and are given by Table 4.5. Moreover, from (4.26) and the dc voltage response parameters given in Table 4.4, the parameter F is computed for each terminal and is included in the same table.

Table 4.5: Parameters of equation (4.20) for the five-terminal dc grid

Terminal No.	1	2	3	4	5
$a\,(1/\mathrm{s})$	-20.00	-25.88	-23.88	-20.00	-20.00
$b\,(\mathrm{MW/kVs})$	-1125	-1000	0	-938	0
$c\,(1/\mathrm{s})$	0	5.88	3.88	0	0
$d\,(1/\mathrm{s})$	20	20	20	20	20
$e\,(\mathrm{MW/kVs})$	1125	1000	0	938	0
$F\,(\mathrm{kVs/MW})$	4.83	7.35	3.87	5.01	12.5

The next step is to compute the dc Jacobian matrix ($\mathbf{J}_{DC}$). Let the initial steady-state be such that all dc-bus voltages are equal to 400 kV ($U_i^o = U^o = 400\,\mathrm{kV}$ flat voltage profile). (This is chosen in order to make use of the simple expression of the Jacobian matrix for flat voltage profiles.) For flat voltage profile the dc Jacobian becomes $\mathbf{J}_{DC} = U^o\mathbf{Y}$ (Refer to equation (3.33)). This gives

$$\mathbf{J}_{DC} = 400 \begin{bmatrix} 1.2750 & -0.6250 & -0.2500 & -0.4000 & 0.0000 \\ -0.6250 & 0.9375 & -0.3125 & 0.0000 & 0.0000 \\ -0.2500 & -0.3125 & 0.8750 & -0.3125 & 0.0000 \\ -0.4000 & 0.0000 & -0.3125 & 1.1292 & -0.4167 \\ 0.0000 & 0.0000 & 0.0000 & -0.4167 & 0.4167 \end{bmatrix} \tag{4.40}$$

Substituting the relevant variables from Table 4.5 and from (4.40) into (4.37), the state matrix $\mathbf{A}$ and the input matrix $\mathbf{B}$ are computed:

$$\mathbf{A} = \begin{bmatrix} -20.0 & 00.0 & 00.0 & 00.0 & 00.0 & -1125.0 & 0000.0 & 0000.0 & 0000.0 & 0000.0 \\ 00.0 & -25.9 & 00.0 & 00.0 & 00.0 & -1470.6 & 1205.9 & -0735.3 & 0000.0 & 0000.0 \\ 00.0 & 00.0 & -23.9 & 00.0 & 00.0 & -0387.6 & -0484.5 & 1356.6 & -0484.5 & 0000.0 \\ 00.0 & 00.0 & 00.0 & -20.0 & 00.0 & 0000.0 & 0000.0 & 0000.0 & -0937.5 & 0000.0 \\ 00.0 & 00.0 & 00.0 & 00.0 & -20.0 & 0000.0 & 0000.0 & 0000.0 & 0000.0 & 0000.0 \\ 04.8 & 00.0 & 00.0 & 00.0 & 00.0 & -2461.4 & 1206.6 & 0482.6 & 0772.2 & 0000.0 \\ 00.0 & 07.4 & 00.0 & 00.0 & 00.0 & 1838.2 & -2757.4 & 0919.1 & 0000.0 & 0000.0 \\ 00.0 & 00.0 & 03.9 & 00.0 & 00.0 & 0387.6 & 0484.5 & -1356.6 & 0484.5 & 0000.0 \\ 00.0 & 00.0 & 00.0 & 04.0 & 00.0 & 0802.0 & 0000.0 & 0626.6 & -2264.1 & 0835.5 \\ 00.0 & 00.0 & 00.0 & 00.0 & 06.3 & 0000.0 & 0000.0 & 0000.0 & 2083.5 & -2083.8 \end{bmatrix}$$

$$\mathbf{B} = \begin{bmatrix} diag\begin{pmatrix} 20.0 & 20.0 & 20.0 & 20.0 & 20.0 \end{pmatrix} & diag\begin{pmatrix} 1125.0 & 1000.0 & 00.0 & 0937.5 & 00.0 \end{pmatrix} \\ diag\begin{pmatrix} 00.0 & 00.0 & 00.0 & 00.0 & 00.0 \end{pmatrix} & diag\begin{pmatrix} 0000.0 & 0000.0 & 00.0 & 0000.0 & 00.0 \end{pmatrix} \end{bmatrix} \tag{4.41}$$

From the state matrix, $\mathbf{A}$, the eigenvalues of the system are computed:

$$\lambda = \begin{bmatrix} -4383.8 \\ -3386.1 \\ -2003.7 \\ -1153.8 \\ -11.6 + 57.9i \\ -11.6 - 57.9i \\ -43.4 \\ -23.1 \\ -19.9 \\ -20.0 \end{bmatrix} \tag{4.42}$$

From the list of eigenvalues in (4.42), it is observed that all eigenvalues have negative real part and hence are stable. Moreover the system has oscillation mode with a frequency of 9.2 Hz and a damping constant of 19 %.
Given the state matrix ($\mathbf{A}$) and input matrix ($\mathbf{B}$), transfer functions between a specific input element(ΔP_i^* or ΔU_i^*) and a specific output element (ΔP_i or ΔU_i) can be found.

In the detailed PSCAD simulation of the five-terminal VSC-HVDC system, a change in power reference of $\Delta P_5^* = 1$ MW gives the responses shown in Fig. 4.35. Now let us consider a step change of power reference $\Delta P_5^* = 1$ MW. This corresponds to an input vector of $\mathbf{P}^* = [0\ 0\ 0\ 0\ 1]' u(t)$. The nodal power responses and dc-bus voltage changes (from the state-space model) are shown in Fig. 4.34. Comparing this with Fig. 4.34, it is evident that the state-space model responses match very well with the corresponding time-plots from the detailed MTDC model in PSCAD. It can also be noticed that the state-space model responses in Fig. 4.35 depict slightly larger overshoots. This is apparently due to the dc line inductances which were neglected in the state-space modeling. In addition to this, the dc line inductances result in small delays in dc voltage responses as observed in Fig. 4.35. The single time-constant approximation applied for each controller of VSC-HVDC also contributes to the deviations, but in less significant manner. By approximating each VSC-HVDC controller by a single time-constant and by ignoring the dc line inductances, the number of state-variables was kept to a relatively small size (10 in the test case) and yet the the dynamic characteristic of the dc grid has been predicted with reasonable accuracy. In contrast, considering all control time constants and dc line inductances makes the space space modeling very cumbersome and more difficult to manage. Hence, it can be concluded that the proposed approach provides a quick way of studying the dc grid system dynamics analytically with reasonable accuracy.

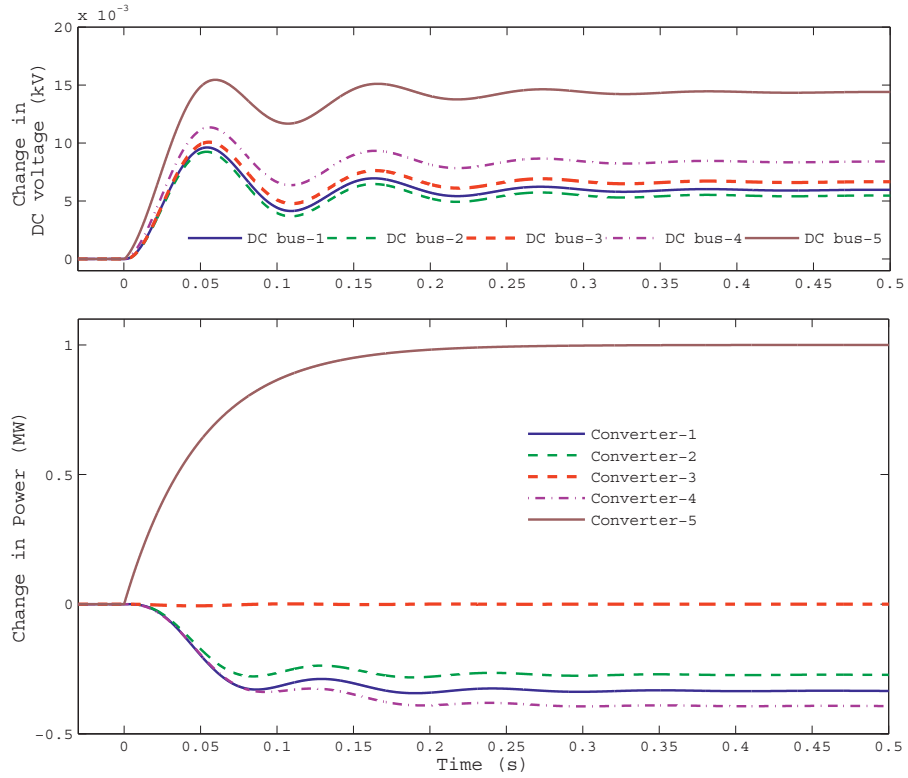


Figure 4.34: State-space model responses: dc-bus voltage and terminal power responses to a step input of $\Delta P_5^* = 1\,\text{MW}$

4.3 Chapter Summary

In this chapter large-disturbance stability and small-signal stability of MTDC have been explored. There are several possible causes of large-disturbance instability in MTDC transmission such as ac fault, dc fault and converter failure. ac faults are usually temporary and clear within short duration of time. In this chapter it was demonstrated that post-fault stability of MTDC depends on pre-fault loading level, aggregate dc capacitance of the dc grid and the duration of the ac fault. An analytical approach has been proposed to compute the critical fault clearing time to have post-fault stability in MTDC systems and the accuracy of the method was corroborated with simulation results. In the small-signal study part of this chapter,

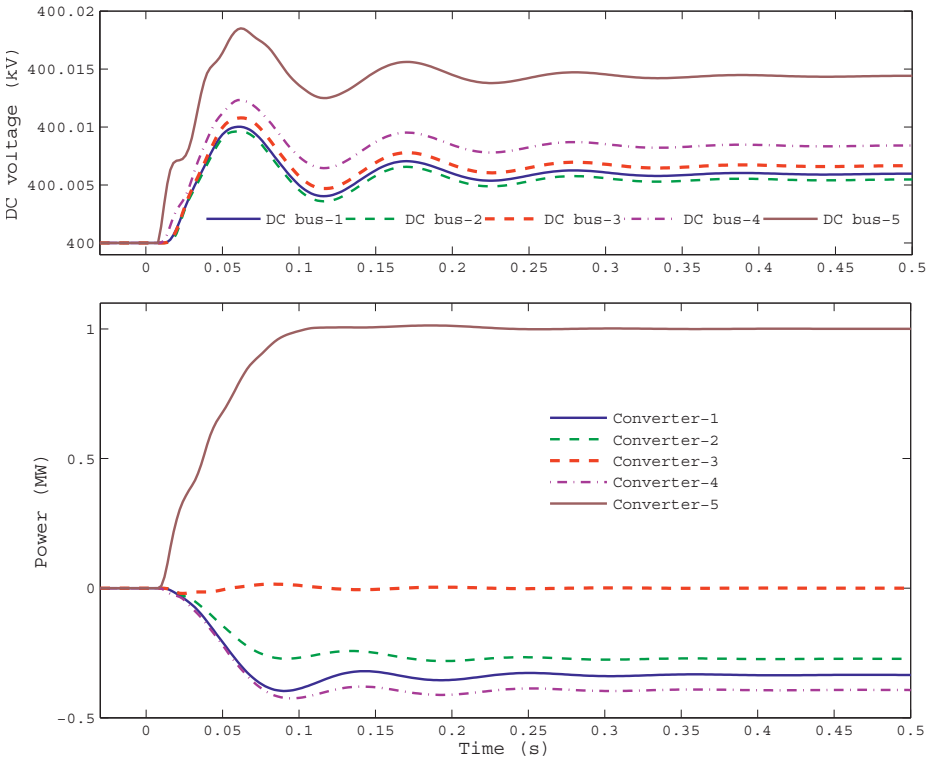


Figure 4.35: Detailed simulation model responses: dc-bus voltage and terminal power responses to a step input of $\Delta P_5^* = 1\,\text{MW}$

a generalized approach of state-space modeling of MTDC has been proposed. Each controller is modeled by a single time constant and each dc line is modeled by a single π-section equivalent consisting of a resistance and two capacitances. Comparison of step responses of the the state-space model (in Matlab) with that of detailed electromagnetic transient model (in PSCAD) has revealed a reasonable degree of agreement between the two. The proposed model is applicable for all five types of VSC control schemes (discussed in this thesis) and for any dc grid topology. Thus the proposed mathematical model can be used for quick analysis of both steady-state and dynamic interactions in the dc grid without requiring detailed time-domain simulations.

5 CASE STUDY OF APPLICATION SCENARIO OF MTDC IN THE NORTH SEA REGION

5.1 Prospects of MTDC Transmission in the North Sea Region

In several references the use of MTDC system has been proposed for integration of wind farms and in particular offshore wind farms [23],[64],[31],[51]. Some have also suggested the use of MTDC as a reinforcement of traditional land-based ac networks [63], [30] [33]. Due to the satisfactory performance of traditional ac networks and lower investment costs (compared to HVDC technology), it will take some time until the use of land-based MTDC systems will be implemented. Offshore based MTDC on the other hand has got a lot of attention in recent years due to increasing development of offshore wind farms. In submarine applications HVDC is the technology of choice for distances of more than 50-60 km due to lower line losses, higher transmission capacity, decoupling of frequencies of ac grids and some other advantages. In this respect, the North Sea region is one of the leading candidate areas which may benefit from the first commercial application of MTDC technology.
The European Network of Transmission System Operators for Electricity (ENTSO-E), an association of Europe's transmission system operators (TSOs) for electricity, is divided into five regional groups (RGs) namely: RG Continental Europe, RG Ireland, RK United Kingdom, RG Nordic and RG Baltic. The North Sea region is surrounded by three of these regional grids, i.e. RG Nordic, RG UK and RG Continental Europe [9]. The North Sea region has several unique features which make MTDC an attractive solution for the grid integration of offshore wind farms. The North Sea region is characterized, among others, by the following features.

1. The area is endowed with vast amounts of wind energy. This provides a lot of potential for developing offshore wind farms. The use of VSC-HVDC for integration of long distance offshore wind farms has become a common trend due to several advantages of such a system (This was discussed partly in chapter 1 of this thesis). The variable generation from wind farms, however, means that there must be more primary and secondary reserves in the ac grids to compensate for the power fluctuations in various time frames.

2. The large hydro power capacity in the Norwegian power system can successfully provide readily available reserves required for compensation of wind power fluctuations. This requires the presence of HVDC connections between the RG UK and RG Nordic. RG Nordic and RG continental are already connected by point-to-point (classic) HVDC link. In the presence of interconnections between the different ac

grids around the North Sea region, wind power producers can easily buy primary and secondary reserves from suitable places (mainly from RG Nordic) and sell wind power production to a much wider regional market.

3. The presence of the three asynchronous ac grids surrounding the North Sea region in a relatively close proximity makes the region suitable for benefiting from interconnection by MTDC. Interconnecting these ac grids by HVDC transmission system enables fast and flexible power flow control in a wider region, while keeping their asynchronous operation unaffected. The benefits mentioned above (in no. 2) for offshore wind power producers also apply to the traditional power producers in the three separate ac grids. Increasing interconnection between regions with compatible physical operations and market mechanisms increases the effective size of the market, which is beneficial both for increased competition and for integrations of large amounts of variable wind power [4].

4. There are some offshore loads in the North Sea (i.e. oil and gas platforms), which mainly use gas fired turbines to meet the power demand. These loads can benefit from clean power supply from onshore grids and/or from offshore wind farms via HVDC connections. In fact in recent years there has already been a trend to supply platforms with VSC-HVDC connections.

All the facts mentioned above reinforce the argument that the use of MTDC in the North Sea region can potentially benefit all the interconnected producers and consumers in a mutual way.

The North Sea HVDC grid will not be developed as a single large project, but in several steps of separate individual projects. Offshore wind farm developments are expected to continue base upon VSC-HVDC interconnections with the three separate ac grids. Once there is substantial number of offshore wind farms in the North Sea, the meshed VSC-HVDC can be formed on the backbone of the already existing subsea power transmission infrastructure. Such scenario is shown by Fig. 5.1 where the blue lines show initial stage developments and the red dashed line shows the formation of meshed North Sea HVDC grid afterwards.

5.2 Meshed North Sea HVDC Grid Scenario: Simulation Results

Different interconnection scenarios have been proposed in the literature for the meshed North Sea HVDC interconnection (sometimes called North Sea Supergrid). Fig. 5.2 shows meshed North Sea HVDC grid scenario proposed by Airtricity [27], Sintef [2], Statnett [7], and EWEA [3].

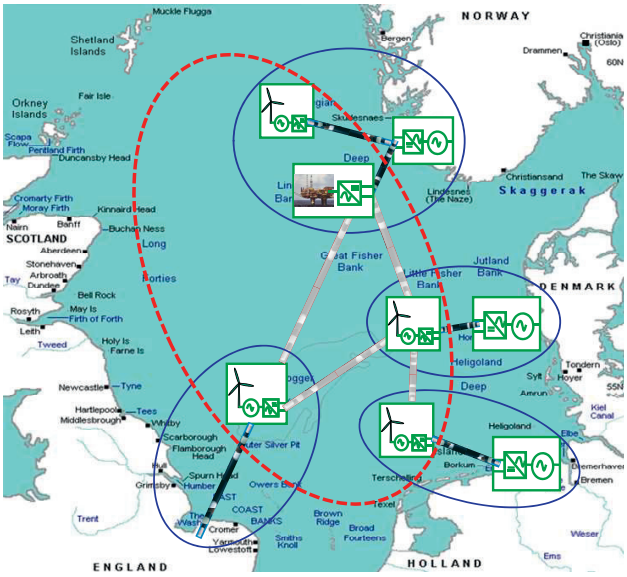


Figure 5.1: Meshed North Sea HVDC grid scenario used for the simulation study

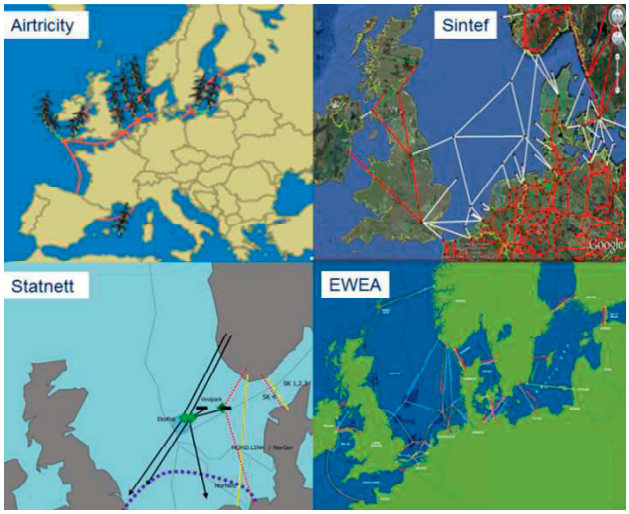


Figure 5.2: North Sea Supergrid proposal by Airtricity (top left, [27]), Sintef (top right, [2]), Statnett (bottom left, [7]) and EWEA (bottom right, [3])

In this chapter a relatively simple scenario of the North Sea super grid has been considered for demonstrating its potentials with the help of simulation studies. As

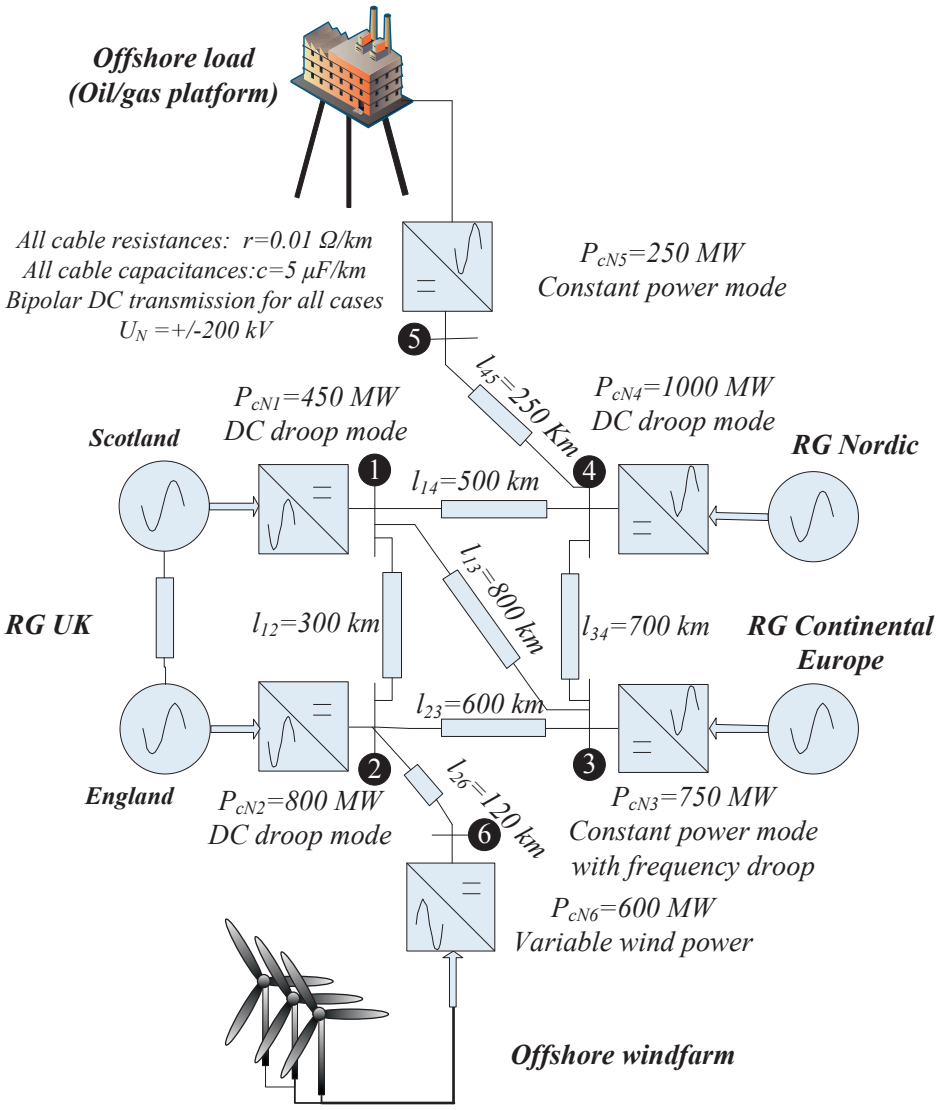


Figure 5.3: North Sea Supergrid scenario chosen for the simulation studies

shown in Fig. 5.3, the chosen test scenario includes two interconnections to RG UK, one interconnection to the RG Nordic, two interconnections to RG Continental Europe, one interconnection to an offshore wind farm and one interconnection to an offshore load (oil and gas platform). Converter power and voltage ratings in Fig. 5.3 are chosen for demonstration purpose only and do not represent any specific future plan for the North Sea super grid. PSCAD simulation software was used for modeling the test scenario. Like in all previous ac grid modeling cases in this thesis, here also each ac grid is represented by a synchronous generator and an equivalent load.

5.2.1 Mitigation of Wind Power Fluctuation by Primary Power Balancing of HVDC Grid

In the test scenario, the offshore wind farm injects variable wind power into the HVDC grid, and as a result the dc-bus voltages also show similar variations. The HVDC terminals with dc voltage droop control (i.e. 1, 2 and 4) respond by varying their power flow accordingly. In contrast, the HVDC terminals with constant power control (i.e. 3 and 5) remain unaffected by the dc-bus voltage variations (see Fig. 5.4). The large power flow variation from the offshore wind farm has effectively been distributed to the HVDC terminals in droop control mode (i.e. terminals 1, 2 and 4), hence demonstrating the capability of the meshed North Sea HVDC grid for mitigating the impact of wind power variation on the ac grid.

5.2.2 Coping with Loss of DC line in the Meshed HVDC Grid

To show the supply security capability of a meshed HVDC grid in the North Sea, outage of a dc line was studied with the simulation model. dc line 1-2 is disconnected abruptly at $t = 90\,s$. This results in increased power flow in some of the dc lines (line 1-3, line 1-4 and line 3-4) such that the power injection at each of the HVDC stations remains nearly unaffected. A closer look at the time plots in Fig. 5.5 shows that the terminals with dc voltage droop control exhibit a small amount of power flow deviation after outage of line 1-2. This is due to the dc line resistances which result in slight variations of the dc-bus voltage changes which in turn affect the droop controllers (quantitative analysis of this effect has been given in chapter 3). Nonetheless, the simulation results show that meshed HVDC grid with dc voltage droop control can ensure supply security even after loss of one of the dc lines constituting the meshed topology.

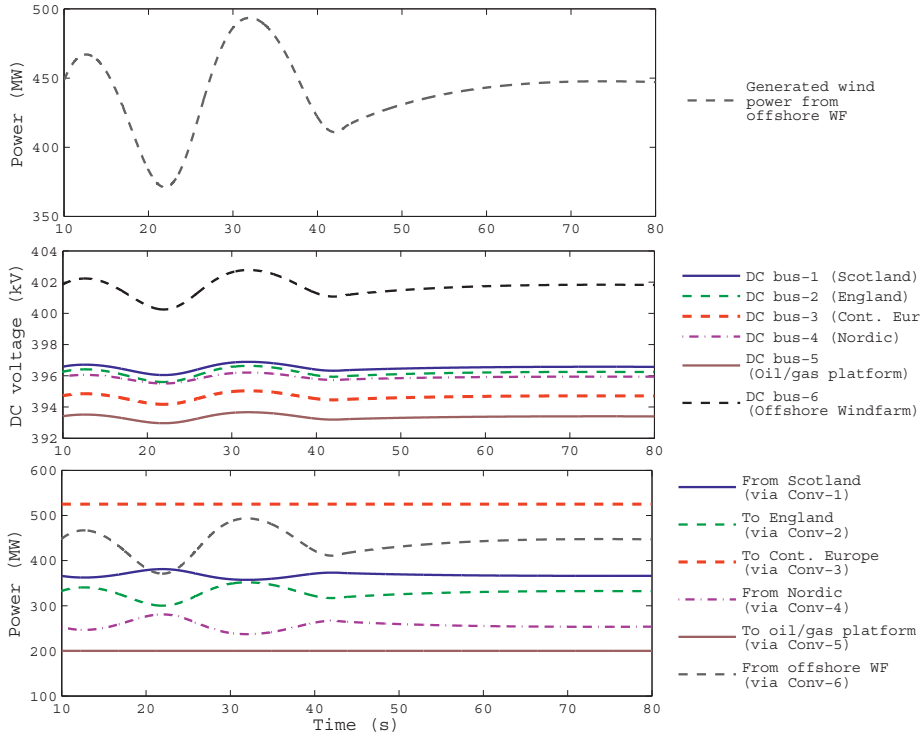


Figure 5.4: Time-variation of wind power and primary balancing by HVDC terminals

5.2.3 Response to Loss of Connection to Offshore Wind Farm

In section 3.1 it was discussed that dc voltage droop control enables the provision of N-1 security in a meshed HVDC grid. This feature can be utilized during loss of connection to offshore wind farm (or loss of power generation from offshore wind farm). This can be seen from the simulation result in Fig. 5.6 where loss of wind power is compensated by the droop controlled terminals (1, 2 and 4). In this particular case, the HVDC terminal connected to RG Continental Europe (i.e. terminal 3) is assigned to constant power mode and hence remains unaffected by the loss of wind power supply in the meshed HVDC grid. Similarly, the power supply to the offshore oil/gas platform remains uninterrupted despite the loss of wind power injection.

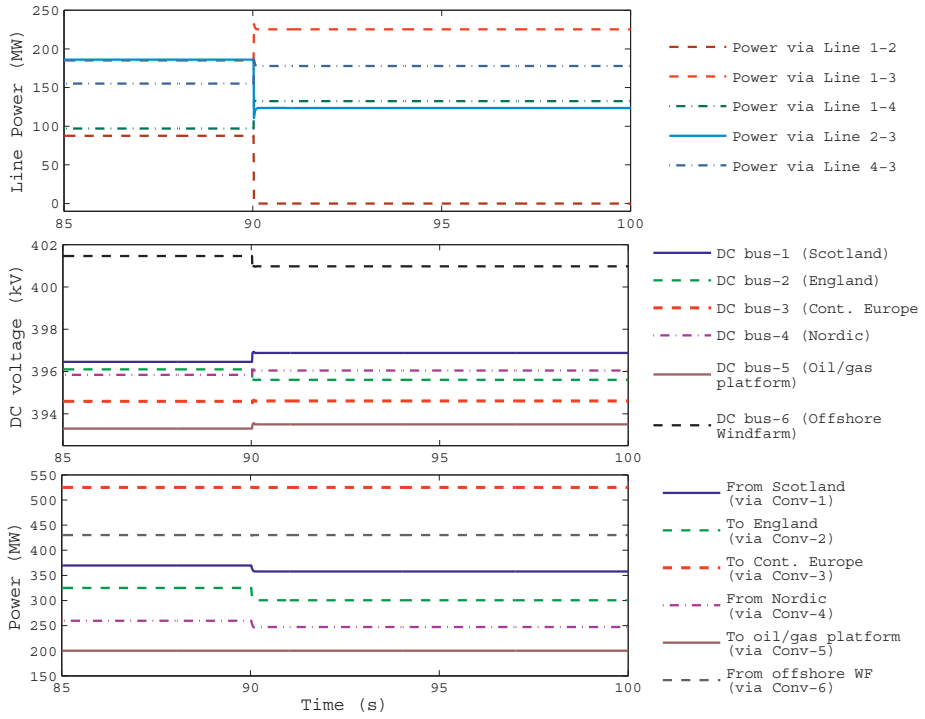


Figure 5.5: Response of meshed HVDC grid to outage of a dc line

5.2.4 Primary Reserve Exchange via HVDC Grid

Exchange of primary and secondary reserves between the three ac grids (RG Nordic, RG UK and RG Continental Europe) is possible by means of meshed North Sea HVDC grid. This requires the use of frequency droop control on the HVDC terminal power flow controller. To demonstrate this, a frequency droop element was added to the power controller of the HVDC terminal connected to RG Continental Europe. An increase of load power inside the RG Continental Europe was simulated and the resulting responses are shown in Fig. 5.7.

Comparison of the frequency responses of the RG Continental Europe in the presence and absence of frequency support by the North Sea HVDC grid is shown in Fig. 5.8. This demonstrates that the North Sea HVDC grid has the potential for enhancing the frequency response of the interconnected ac grids.

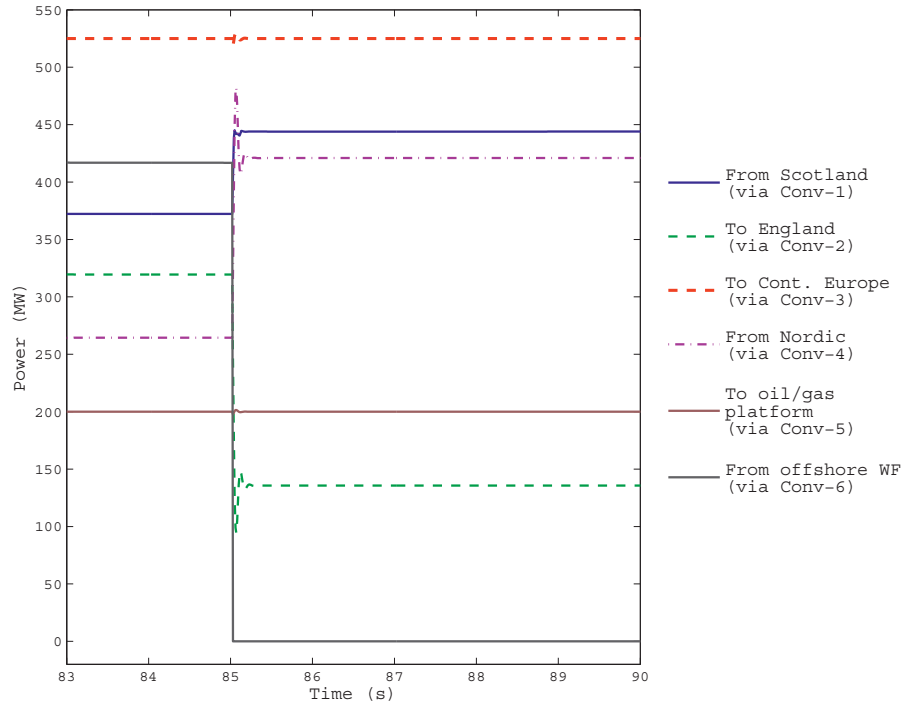


Figure 5.6: Response of dc grid to loss of connection to offshore wind farm

5.2.5 Secondary Control Response of MTDC

Large steady-state power flow deviations in the dc grid may arise from a sudden outage of a converter station. The simulated case of wind power loss in Fig. 5.6 can be a good example of an event which results in steady-state power flow deviations in the VSC-HVDC terminals. In this particular case although converters 1, 2 and 4 are participating in the primary control, there may be a more urgent need to restore power flow in certain HVDC stations than the others. Here we shall consider a scenario where there is a need to restore power flow in converter 1 and 2 (i.e. UK connections) at the expense of more power injection from the RG Nordic via converter-4. This is based on the premise that the huge installed capacity of hydropower in the RG Nordic can be capable of such provision. Based on this scenario, the responses of secondary control in the meshed North Sea HVDC grid simulation dc are shown in Fig. 5.9.

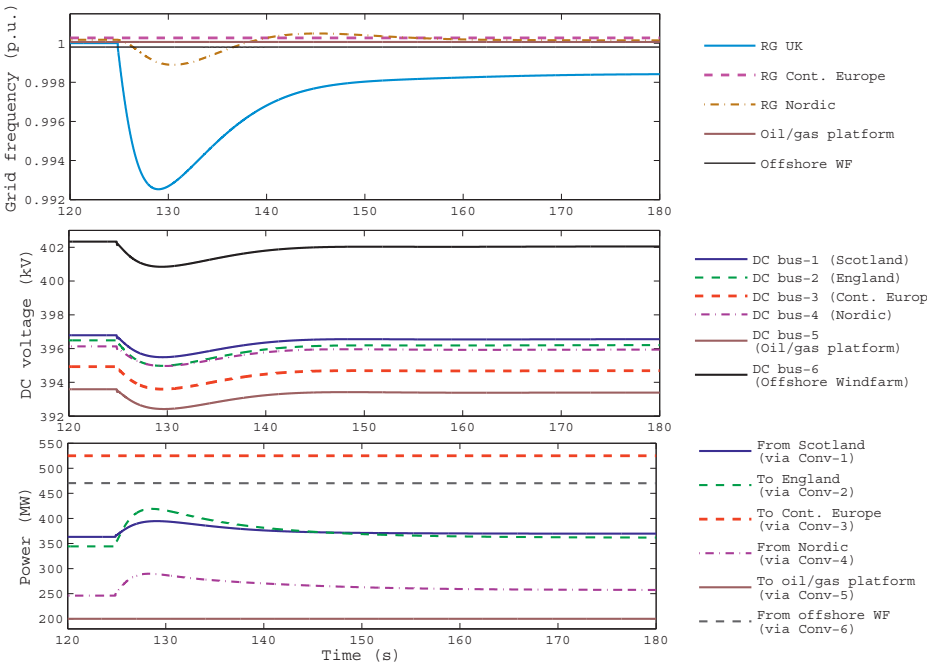


Figure 5.7: Primary reserve exchange via HVDC grid

As shown in Fig. 5.9, the secondary control action is capable of restoring the power flow of converters 1 and 2 to the same level as prior to the loss of connection to offshore wind farm. Power flow via converter terminals 3 and 5 remained intact throughout the primary and secondary control actions.

5.3 Challenges in Developing Meshed North Sea HVDC Grid

While the potentials of meshed HVDC grid in the integration of North Sea producers and consumers appear to be enormous, there are still some challenges in employing the technology in real life [22]. The most salient ones of these challenges are discussed below.

1. Dc fault handing issues: dc fault protection based upon ac-side protection of converters and dc isolators has been proposed in the literature, thereby avoiding

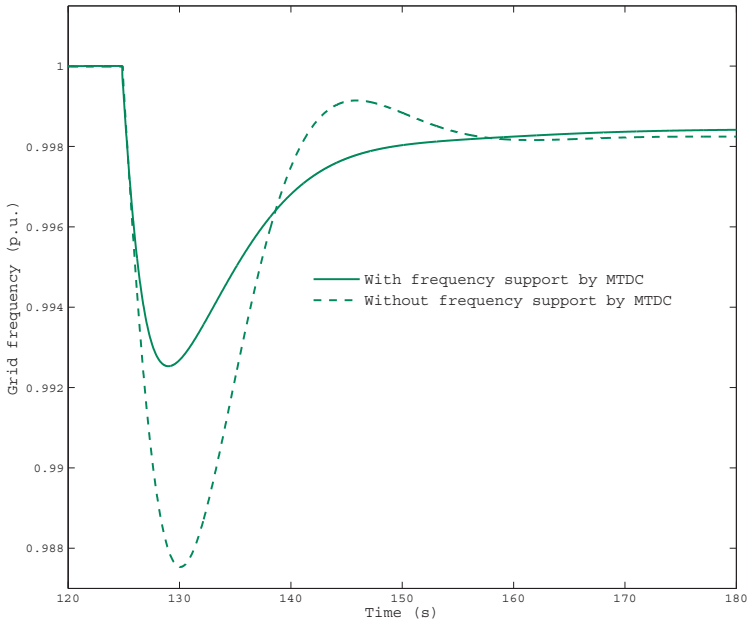


Figure 5.8: Comparison of frequency responses of the RG Continental Europe with and without frequency support by the North Sea HVDC grid

the need for dc circuit breakers [54]. The method involves disconnection of all converters on their respective ac sides, then isolating part of the dc grid with dc fault and reconnects all the healthy converter stations to their respective ac grids. Although the method is capable of disconnecting faulty part and restoring normal operation of the rest of the dc grid, the momentary disconnection of the entire dc grid involved in this process can undermine security of supply unless the restoration time is sufficiently small. Fault localization algorithms for dc cables have been proposed in some references [91],[49]. dc circuit breakers on the other hand can quickly disconnect the faulty part without the need to temporarily disconnect the dc grid from all ac connections. Various solutions of dc circuit breakers based on power electronics have been proposed [53],[47],[41]. However, dc circuit breakers in the high voltage and high current ranges and applicable to such "'supergrids"' have not been made commercially available yet.

2. Standardization of dc transmission voltage level and requirements for dynamic responses: Current suppliers of VSC-HVDC technology use different dc voltage

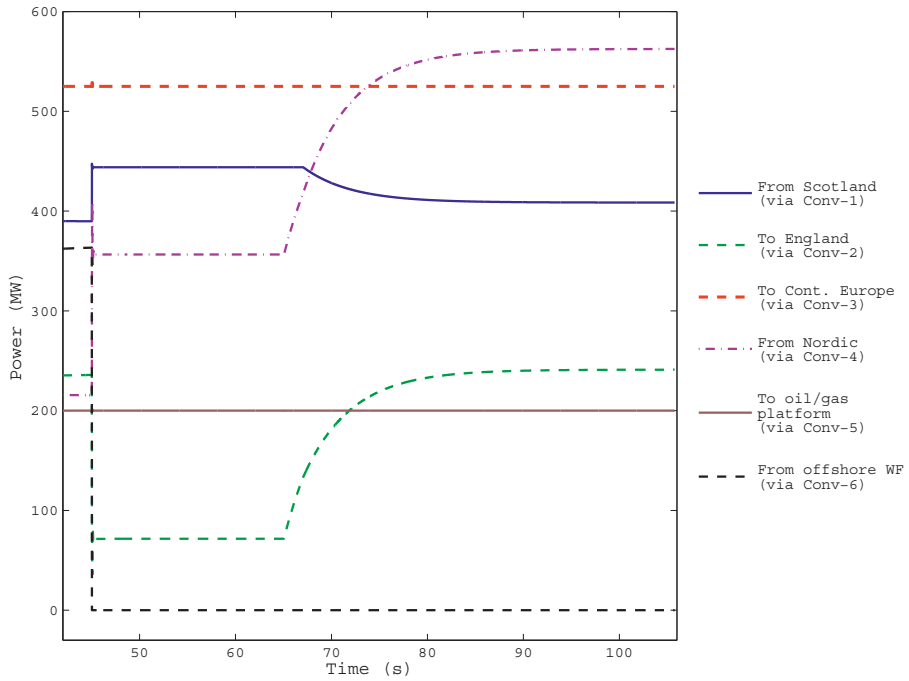


Figure 5.9: Secondary control response of HVDC grid for loss of connection to offshore wind farm

ratings for HVDC solutions, which in many cases are specifically chosen to suit the specific application. Since a meshed HVDC grid would normally be expected to involve various technology suppliers and transmission system operators, there is a clear need for determining a standard dc voltage level as well as dynamic response requirements (such as droop level for dc voltage control, droop level for frequency support by HVDC, fault-ride-though capabilities).

3. Ambiguity surrounding ownership and management of the North Sea Supergrid: Since the North Sea Supergrid would span several transmission system operators; it is not very clear who will own the dc grid and how it will be operated and who will be responsible to the system security. These are crucial questions that should be addresses properly since these directly affect sharing of investment and maintenance costs as well as operation and market integration of the dc grid.

5.4 Chapter Summary

In this chapter a MTDC scenario in the North Sea has been studied with the help of simulation models. It is shown that a meshed MTDC interconnection in the North Sea can increase supply security, and can provide further integration of regional and national electricity markets which in turn encourages competition for both new offshore wind farms as well as for traditional land based power generation. If a meshed HVDC grid in the North Sea is to be realized, some challenges should be first tackled. These include the need for effective dc fault protection, standardization of voltage levels, standardization of controllers of VSC-HVDC terminals and clarification of ownership and management authority of the offshore dc grid.

6 CONCLUSIONS AND FUTURE WORKS

6.1 Conclusions

MTDC transmission system offers several advantages for offshore applications such as wind power integration, interconnection of asynchronous ac grids and supply of power to offshore oil and gas platforms. This is most evident in the case of the North Sea region which has vast potential of wind power, already existing offshore loads (oil and gas platforms) as well as three asynchronous ac grids (RG UK, RG continental and RG Nordic). While there is a growing need for MTDC transmission system, the technology is not yet fully matured for commercial applications. Several research and development efforts have been done in the area of MTDC control and protection systems. According to literature, MTDC must have dc voltage droop control configuration at two or more of the VSC-HVDC terminals in order to provide N-1 security in the dc grid. The research work described in this thesis had the objectives of consolidating the control of MTDC based on existing methods and compare their performances, to propose operational strategy and to increase understanding of the steady-state and dynamic characteristics of MTDC using novel analysis techniques. In line with this objective, operation and analysis of MTDC systems have been thoroughly investigated in the thesis. The research results can be divided into three groups, namely: MTDC control, MTDC operation and MTDC analysis.

i. MTDC Control

In this thesis a control method which enables ac grid frequency support by MTDC has been proposed. The method enables exchange of primary reserves between asynchronous ac grids via a common MTDC system. The control method improves both the dynamic frequency response (i.e. the frequency response in the first few seconds) as well as the steady-state frequency response of ac grids. The most significant advantage of the control method is that does not require any communication between different VSC-HVDC terminals or between the asynchronous ac grids for coordinated actions. Each generator and converter unit acts autonomously based upon local frequency and dc-bus voltage measurements. With the help of various simulation models it was shown that the proposed control method gives satisfactory performance.

ii. MTDC Operation

Dc voltage droop control takes the assumption that dc-bus voltage variations can be taken as a reflection of the loading level of dc grids (just the same way as frequency works in generation-load balancing in ac grids). Unlike frequency of ac grids

however, the bus voltages in a dc grid show slight variations due to line resistances. If these differences in dc-bus voltages are not properly accounted for in determining dc voltage references and power references, there will be large power injection deviations at steady-state and this will pose a challenge to precisely control the power flow at steady-state. From the research work it was found out that if the dc voltage references and power references are assigned the same value as the output from dc power flow analysis of the network, then all the dc voltage error signals in the droop controllers will be eliminated and precise power flow will be achieved. This was corroborated by employing the method on a test model of an MTDC system and simulation results have shown that the method works very well indeed .
Secondary control of dc grid is very much like tie-line control in ac grid. Due to the dc line resistances' impact on the droop controllers, implementation of the secondary control becomes difficult. This, however, has been managed in this thesis by using the results of the steady-state MTDC analysis approach (which itself is one of the main contribution of the research work). The proposed secondary control strategy enables the precise restoration of power flow in selected converter units within the MTDC.

iii. MTDC Analysis

Quantitative approaches for direct analysis of steady-state and dynamic characteristics of MTDC has rarely been used until now in existing research work (even though there are numerous references which used simulation based approaches). In this thesis work various quantitative approaches have been proposed to study the steady-state and dynamic characteristics of MTDCs. In all proposed methods, generalized topology of dc grid and generalized control mode of VSC-HVDC terminals have been considered in order to accommodate all possible topology and control strategy scenarios of MTDC systems. The various quantitative analysis methods proposed and verified in the research work are summarized below.

a. Analytical expression for distribution of primary power flow exchange in MTDC

An analytical expression which correctly estimates the distribution of primary power flow among various VSC-HVDC terminals of a MTDC has been derived via linearization of the power flow equations. This enables to quantify the impact on power flow distribution of (1) dc grid topology (as expressed by the dc Jacobian matrix), (2) use of various dc voltage droop constants and (3) the location where a power excess/deficit has occurred. Hence the expression can be used to accurately estimate changes in nodal power injection after loss of a VSC-HVDC terminal, or loss of a dc line.

b. Analytical expression for steady-state ac/dc interactions in primary response for generalized connection topology

The use of frequency droop control in VSC-HVDC causes load-frequency interaction of asynchronous ac grids via MTDC system. Several factors determine the extent to which a change in load occurring in one ac grid will affect another ac grid connected via MTDC. Frequency responses of the various ac grids, droop constants used in the MTDC (both dc voltage droop and frequency droop constants) as well as the dc grid topology are among the main factors which determine the degree of influences in the ac/dc interactions. Moreover, two or more VSC-HVDC terminals may be connected to the same ac grid. Analytical expression for computing the steady-state ac/dc interactions, which considers all these aforementioned factors, has been derived. With the derived expression, one can for example accurately compute the frequency decrement in an ac grid due to a load increment in an other ac grid connected via the MTDC system. The proposed approach has been verified by simulation results of a test model of MTDC transmission .

c. An approach for state-space modeling in an arbitrary MTDC grid

In some literature small-signal analysis of MTDC grid has been studied. The methodology employed in the existing work has been to analyze some specific MTDC topology and hence generalization of the analysis to an arbitrary MTDC topology was missing. In this research work a universally applicable method for small-signal analysis of any MTDC topology and VSC-HVDC control configuration has been proposed. The method is applicable for small-signal modeling of MTDCs and can give a suitable alternative to detailed time-domain simulation analysis of MTDC grids. The drawback of the method is its limitation to an all-cable dc grid system (i.e. it is not applicable if there is one or more overhead line in the dc grid due to the significantly large line inductances which should be included in the small-signal modeling).

d. Large disturbance stability analysis of MTDC grid

Power flow interruption at a converter in rectifier mode of operation can potentially lead to dc voltage collapse of MTDC system depending on the level of dc grid loading and the amount of static stability margin. A typical cause of power interruption at a rectifier unit is ac fault occurring close to the rectifier terminal. If the ac fault is temporary (which is usually the case) the eventual stability of the dc grid (or alternatively the recovery of the dc grid from the ac fault impact) will depend upon the duration of the ac fault, pre-fault loading of the dc grid and the maximum aggregate power delivery capacity of the rectifier right after the fault clearance. An analytical expression has been derived to compute the *critical clearing time* for the dc grid to avoid eventual dc voltage collapse and power flow interruption thereafter. This critical clearing time is different from the one computed for synchronous generators though there is some analogy between the two. Simulation results have shown that the MTDC fails to recover from the ac fault when the fault duration exceeds the

critical clearing time computed analytically. High severity balanced ac faults and medium severity unbalanced ac faults may result in synchronization failure of the PLL of VSC-HVDC terminals thereby destabilizing the dc grid earlier than the critical clearing time computed by the proposed analytical expression. The proposed approach assumes that the PLL of the converters work properly in the duration of the ac fault and the dc voltage collapse is mainly caused by depletion of energy from the dc capacitances (filter capacitances plus cable capacitances).

6.2 Challenges in Developing MTDC and Suggested Future Works

While MTDC has several potentials advantages and application areas, there are still some challenges which needs to be solved before employing the technology for commercial application. The most important challenges and other suggested future works in the area of MTDC are discussed below.

i. Dc fault handing issues: dc fault protection based upon converters ac side protection and dc isolators has been proposed in the literature, thereby avoiding the need for dc circuit breakers. The method involves disconnection of all converters on their respective ac sides, then isolating part of the dc grid with dc fault and reconnects all the healthy converter stations to their respective ac grids. Although the method is capable of disconnecting faulty part and restoring normal operation of the rest of the dc grid, the momentary disconnection of the entire dc grid involved in this process could undermine security of supply unless the restoration time is sufficiently small. dc circuit breakers on the other hand could instantaneously disconnect the faulty part without the need to temporarily disconnecting the dc grid from all ac connections. However, dc circuit breakers in the high voltage and high current ranges have not been commercially available yet.

ii. Standardization of dc transmission voltage level and requirements for dynamic responses: Current suppliers of VSC-HVDC technology use different dc voltage ratings for HVDC solutions, which in many cases are specifically chosen to suit the specific cases of applications. Since a meshed HVDC grid would normally be expected to involve various technology suppliers and transmission system operators, there is a clear need for determining standard dc voltage level as well as dynamic response requirements (such as droop level for dc voltage control, droop level for frequency support by HVDC, ac and dc fault responses).

iii. Ambiguity surrounding ownership and management of MTDC: MTDC can potentially span several transmission system operators; it is not very clear who would own the dc grid and how it should be managed. These are crucial questions that

should be addresses properly since these directly affect sharing of investment and maintenance costs as well as operation and market integration of the dc grid.

iv. Use of MTDC for damping of oscillations in ac grids: In addition to the challenges listed above, MTDC can potentially be used for damping out disturbances in ac grids [58]. This may be done by using the active power controller or reactive power controller at the VSC-HVDC terminals as power system stabilizers (PSS), i.e. similar to the PSS applied to the excitation control of synchronous generators.

v. Small-signal modeling of generalized ac/dc interconnection including multi-machine ac systems: The generalized small-signal modeling approach proposed in this thesis work only considers the MTDC system excluding the dynamic ac/dc interactions. This should be improved by including detailed multi-machine models in order to get a full picture of the ac/dc dynamic interaction. This becomes even more useful to achieve proper tuning of VSC-HVDC controllers in case they will include supplementary control serving as PSS (as mentioned in no. iv above).

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A Appendix

Control design of VSC-HVDC (and other systems as well) can be done in two ways: (1) based on physical units or (2) based on per-units. Control system based on physical units is more straight forward compared to the later one. Per-unit based control requires the conversion of all input parameters from physical units into per-units. The difference between these two in the case of VSC-HVDC can be understood by looking at Fig. A.1 and Fig. A.2.

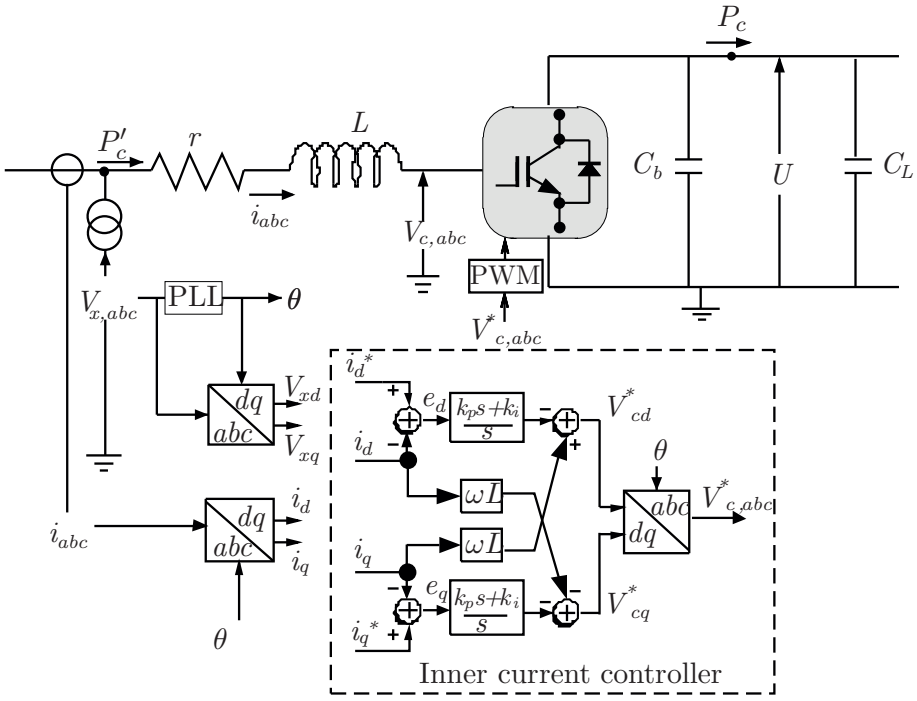

Figure A.1: VSC control structure which uses physical quantities

The main advantage of the per-unit approach of control design is its re-usability for scaled up/down versions of the same system. This means that as long as the systems dynamics remains same, the controller also will remain unchanged for various ratings of the system. Because of this advantage, the per-unit approach has been used for the VSC-HVDC simulation models in this thesis work.
Before proceeding to the VSC-HVDC specification, let us first briefly discuss the

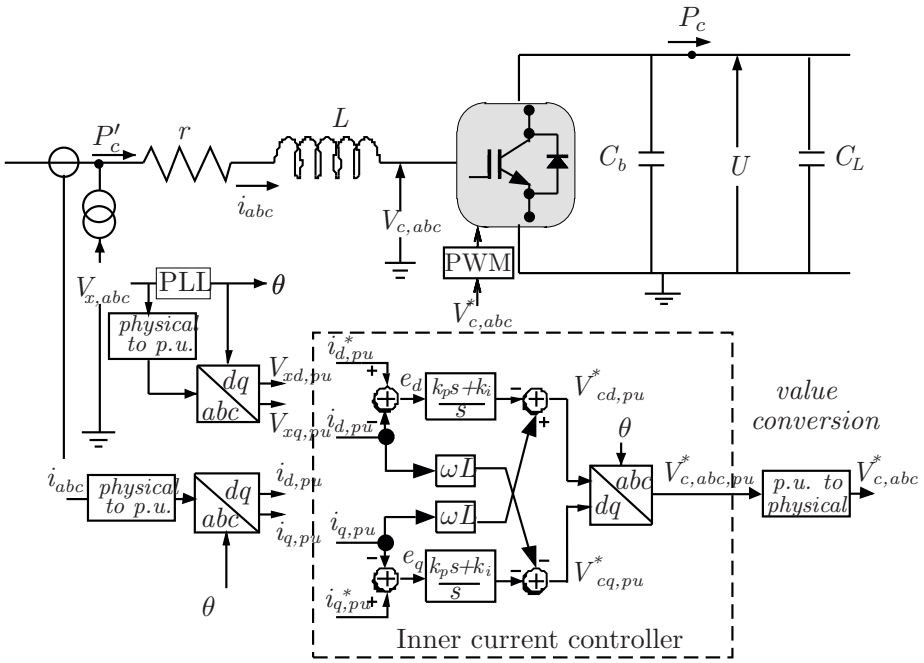

Figure A.2: VSC control structure which uses per-unit quantities

concept of per-unit system. Per-unit system enables us to analyze a system independent from the actual rating of the system in physical units. Per-unit conversion requires a pre-determined set of base-units. The ratio of a physical unit to the corresponding base-unit gives the per-unit equivalent.

In power systems the rated apparent power (or just power), rated voltage and rated current are the most fundamental elements by which electrical equipments or components are specified. In most cases the rated current, rated voltage and rated power/apparent power are taken as the base current, base voltage and base power/apparent power respectively. Base resistance/ impedance Z_{base} is defined as the ratio of base voltage to base current. Base admittance (Y_{base}) is the reciprocal of the base impedance. Hence for an ac system with rated current of I_N, rated voltage

of V_N and rated power/ apparent power of I_N the set of base-units is given by

$$\left.\begin{aligned} V_{base} &= V_N \\ I_{base} &= I_N \\ P_{base} &= S_{base} = S_N \\ r_{base} &= Z_{base}\frac{V_{base}}{I_{base}} \end{aligned}\right\} \tag{A.1}$$

The per-unit conversions are given by

$$\left.\begin{aligned} V_{pu} &= \frac{V}{V_{base}} \\ I_{pu} &= \frac{I}{I_{base}} \\ P_{pu} &= \frac{P}{S_{base}} \\ r_{pu} &= \frac{r}{Z_{base}} \end{aligned}\right\} \tag{A.2}$$

Base inductance and base capacitance are defined in different ways for ac and dc systems. In ac system base inductance and base capacitance are defined in terms of base impedance and base admittance respectively:

$$\left.\begin{aligned} \omega L_{AC,base} &= Z_{AC,base} \\ \omega C_{AC,base} &= Y_{AC,base} \end{aligned}\right\} \tag{A.3}$$

where ω refers to rated ac system frequency in rad/s. The per-unit conversions of inductance and capacitance are given by

$$\left.\begin{aligned} L_{AC,pu} &= \frac{L_{AC}}{\omega Z_{AC,base}} \\ C_{AC,pu} &= \frac{C_{AC}}{\omega Y_{AC,base}} \end{aligned}\right\} \tag{A.4}$$

Like in ac systems, the rated voltage, rated current and rated power in dc systems are also often taken as the base voltage, base current and base power respectively:

$$\left.\begin{aligned} U_{DC,base} &= U_{DC,N} \\ I_{DC,base} &= I_{DC,N} \\ P_{DC,base} &= P_{DC,N} \\ r_{DC,base} &= U_{DC,base}/I_{DC,base} \end{aligned}\right\} \tag{A.5}$$

Inductances and capacitances in dc power system are usually observed from energy storage point of view rather than from the impedance perspective. Hence we introduce the a new quantity termed here as base energy ($E_{DC,base}$) and defined as

$$E_{DC,base} = P_{DC,base} \times 1\,\mathrm{s} \tag{A.6}$$

In dc power system we can define the base inductance and base capacitance in terms of energy accumulation time (occasionally referred as time constant of energy). This is the time required to accumulate the base (rated) energy in to the capacitance/inductance while injecting power into the capacitance/inductance at the rated power of the system (analogous to inertia time constant of synchronous generators). Let us first define the base capacitance and base inductance as

$$\left.\begin{array}{l} \frac{1}{2}C_{DC,base}U^2_{DC,base} = E_{DC,base} = P_{DC,base} \times 1\,\mathrm{s} \\ \frac{1}{2}L_{DC,base}I^2_{DC,base} = E_{DC,base} = P_{DC,base} \times 1\,\mathrm{s} \end{array}\right\} \tag{A.7}$$

Per-unit conversion are given by

$$\left.\begin{array}{l} C_{DC,pu} = \frac{C_{DC}}{C_{DC,base}} = \frac{C_{DC}}{\left(2P_{DC,base}/U^2_{DC,base} \times 1\,s\right)} \\ L_{DC,pu} = \frac{L_{DC}}{L_{DC,base}} = \frac{L_{DC}}{\left(2P_{DC,base}/U^2_{DC,base} \times 1\,\mathrm{S}\right)} \end{array}\right\} \tag{A.8}$$

The per-unit parameters of the VSC model in Fig. A.2 (and also all other VSC models used for simulation studies in this thesis) are shown in Table A.1. Note that

Table A.1: Per-unit parameters of the VSC models used in the thesis

Parameter	value (pu)	Remarks
r	0.01	Rated voltage drop across r is 1 % of rated ac voltage
L	0.06	Rated voltage drop across L is 6 % of rated ac voltage
C_b	0.1	Charging time (at rated power is 100 ms)
k_i	0.0133	Integral gain of inner current controller
k_p	1	Proportional gain of inner current controller

all the parameters in Table A.1 are the same for all VSC-HVDC terminals(control parameters k_i and k_p refer only to active grid connected terminals). The actual (physical) values of the parameters change according to power and voltage ratings:

$$\left.\begin{array}{l} r_{AC} = r_{AC,pu}Z_{AC,base} \\ L_{AC} = L_{AC,pu}L_{AC,base} \\ r_{DC} = r_{DC,pu}Z_{DC,base} \\ C_{DC} = C_{DC,pu}C_{DC,base} \end{array}\right\} \tag{A.9}$$