EVER — CATCHER GROUP

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PART NO. : MS-10-1560S

STANDARD SPECIFICATIONS FOR SED1560 SERIES

FOR MESSRS. :

CONTENTS

90.02.23

ACCEPTED BY :   PROPOSED BY :

RECORD OF REVISION

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3. Precautions for LCM

3-1 Precautions in handling LCD Modules (hereinafter LCM's)

EVERBOUQUET INTERNATIONAL's LCM's have been assembled and accurately calibrated before delivery.
Please observe the following criteria when handling.

A. Do not subject the module to excessive shock.
B. Do not modify the tab on the metal holder.
C. Do not tamper with the printed circuit board.
D. Limit soldering of the printed circuit board to I/O terminals only.
E. Do not touch the zebra strip nor modify its location.

3-2 Static electricity warning:

EVERBOUQUET's LCM uses CMOS LSI technology. Therefore, strict measures to avoid static electricity discharge are followed through all processes from manufacturing through shipping. When handling a LCM, take sufficient care to prevent static electricity discharge as you would and CMOS IC.

A. Do not take the LCM from its anti-static bag until it's to be assembled. LCM's are individually packaged in bags specially treated to resist static electricity. When storing, keep the LCM packed in the original bags, or store them in a container processed to be resistant to static electricity, or in an electric conductive container.

B. Always use a ground strap when handling a LCM.
Always use a ground strap while working with the module, from the time it is taken out of the anti-static bag until it is assembled. When it is necessary to transfer the LCM, once it has been taken out of the bag, always place it in an electric conductive container. Avoid wearing clothes made of chemical fibers, the use of cotton or conductive treated fiber clothing is recommended.

C. Use a no-leak iron for soldering the LCM.
The soldering iron to be used for soldering the I/O terminals to the LCM are to be insulated or grounded at the iron tip.

D. Always ground electrical apparatuses required for assembly.
Electrical apparatuses required to assemble the LCM into a product, i.e. electrical screwdrivers are to be first grounded to avoid transmitting spike noises from the motor.

D. Assure that the workbench is properly grounded.

F. Peel off the LCM protective films slowly. The module is attached with a film to protect the display surface from contamination, damage, adhesion of flux, etc. Peeling off this film abruptly could case static electricity to be generated, so peel the tape slowly.

G. Pay attention to the humidity in the work area.
50~60% RH is recommended.

3-3 Precautions for the soldering of an LCM

The following procedures should be followed when soldering the LCM:

A. Solder only to the I/O terminal.
B. Use a no leakage soldering iron and pay particular attention to the following:
(1) Conditions for soldering I/O terminals

Temperature at iron tip: 280℃ + 10℃

Soldering time: 3-4 sec/terminal

Type of solder : Eutectic solder (rosin flux filled)

Note: Avoid using flux, because it could penetrate the module and the module may get contaminated during cleaning. Peel off protective film after soldering of the I/O terminals is finished. By following this procedure, the surface contamination, caused by the dispersion of flux while soldering, can be avoided.

(2) Removing the wiring

When a lead wire or a connector to the I/O terminal of the module is to be removed, remove it only after the solder at the connection has sufficiently melted since the I/O terminal is a through hole. If it is forcefully removed, it could cause the terminal to break or peel. The recommended procedure is to use a suction-type solder remover. Caution, do not reheat the I/O terminal more than 3 times.

3-4. Long-term storage

If the correct method of storage is not followed, deterioration of the display material polarizer and oxidation of the I/O terminal plating may make the soldering process difficult. Please comply with the following procedure.

A. Store in the shipping container.
B. If the shipping container is not available, place in anti-static bags and seal the opening
C. Store the modules where they are not subjected to direct sunlight or a fluorescent lamp. Sore in a temperature range of 0℃~35℃ with low relative humidity.

3-5. Precautions in use of LCD modules

A. Do not give any external shock.

B. Do not wipe the surface with hard materials.

C. Do not apply excessive force on the surface.

D. Do not expose to direct sunlight or fluorescent light for a long time.

E. Avoid storage in high temperature and high humidity.

F. When storage for a long time at 40℃ or higher is required, R/H shall be less than 60%.

G. Liquid in LCD is hazardous substance. Must not lick, swallow when the liquid is attached to your hands, skin, clothes etc. Wash it out thoroughly.

I T E M	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT	NOTE
VIEWING ANGLE	$\Phi2-\Phi1$	K = 2.0	30	40	------	deg.	1~3
CONTRAST RATIO	K	$\Phi = 10^o$ $\theta = 0^o$	2.5	4.0	------	------	1~3
RESPONSE TIME	tr (rise)	$\Phi = 10^o$ $\theta = 0^{oo}$	------	250	------	ms	1, 4
	tf (fall)	$\Phi = 10^o$ $\theta = 0^o$	------	350	------	ms	1, 4
BRIGHTNESS FOR LED BACKLIGHT	B	(*) $\Phi = 0^o$ $\theta = 0^o$	4.0	------	------	cd/m^2	------

(UNDER NORMAL TEMPERATURE AND HUMIDITY IN A DARK ROOM)

NOTE (1): SEE CUSTOMER ACCEPTANCE STANDARD SPECIFICATION FOR DEFINITION OF OPTICAL CHARACTERISTICS.

4. Optical definitions

4.1 Definition of angle θ and Φ

Z (Normal)
$\Phi2$
eye
Y ($\theta=180^o$)
$\Phi1$
LCD
X' ($\theta=90^o$)
X ($\theta=-90^o$)
Y' ($\theta=0^o$)
θ
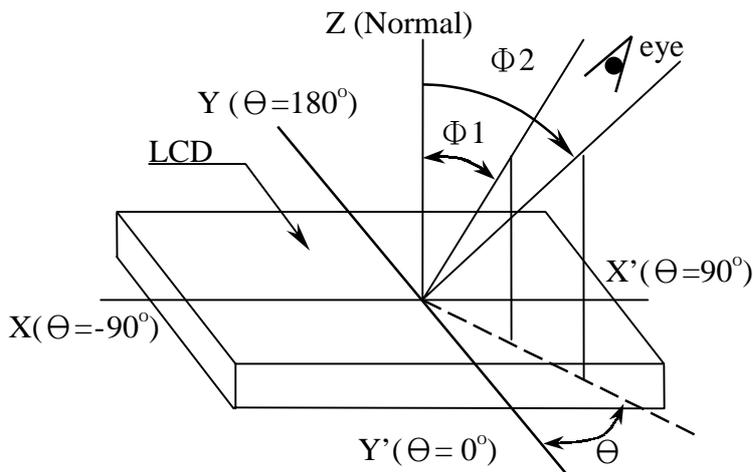
POSITIVE TYPE

4.2 Definition of viewing angle $\Phi1$ and $\Phi2$

K
$\Phi1<10^o<\Phi2$
1.4
$\Phi1$ $\Phi2$
Contrast Ratio K
VS Viewing Angle Φ
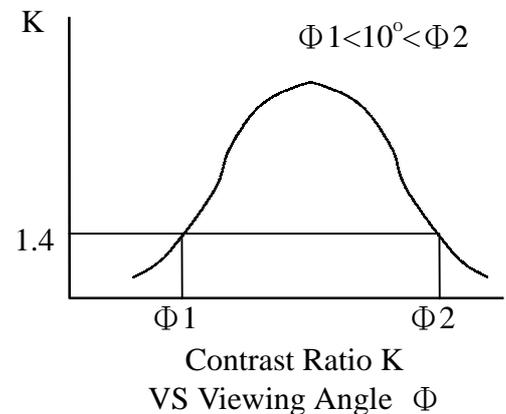
POSITIVE TYPE

4.3 Definition of contrast "K"

$$K= \frac{\text{Brightness of non-selected segment (B2)}}{\text{Brightness of selected segment (B1)}}$$
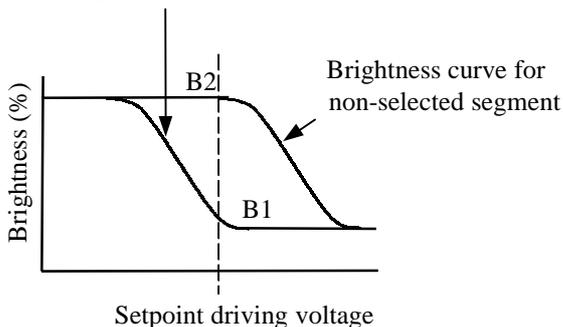
B2
Brightness curve for non-selected segment
Brightness (%)
B1
Setpoint driving voltage

4.4 Definition of optical response

NON Selective State
Selective state
NON Selective State
Brightness
100%
90%
10%
tr (rise time)
tf (fall time)
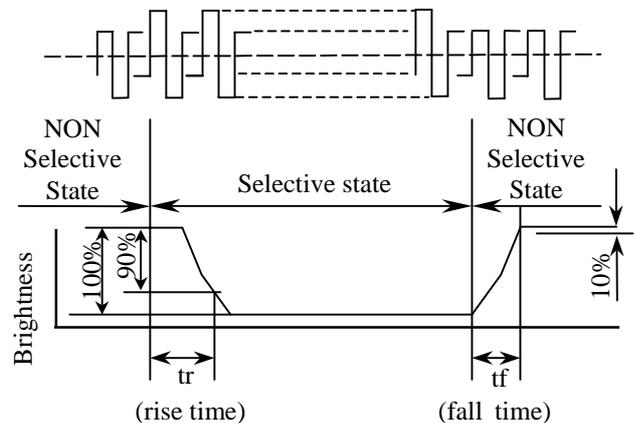
5. Quality and reliability

5-1 Test condition

Test should be conducted under the following conditions:

Ambient temperature　　　: 25 ± 5℃

Humidity　　　　　　　 : 60 ± 20 % RH

5-2 Sampling plan

Sampling method shall be in accordance with MIL-STD-105D, inspection level II, normal inspection, and single sampling plan tables for normal tightened, and reduced inspection.

5-3 Acceptable quality level

A major defect is a defect that could result in failure or materially reduce that the usability of the unit of product for its intended purpose.

A minor defect is one that does not materially reduce the usability of the unit of product for its intended purpose or is a departure from established standards having no significant bearing on the effective use or operation of the unit.

5-4 Appearance

Appearance test is to be conducted by human eyes at approximately 30cm distance from LCD module under the single fluorescent light.

The inspection area of LCD panel shall be within the range. Of following limits.

Zone A Active Area
Zone B Viewing Area
Zone C Frame
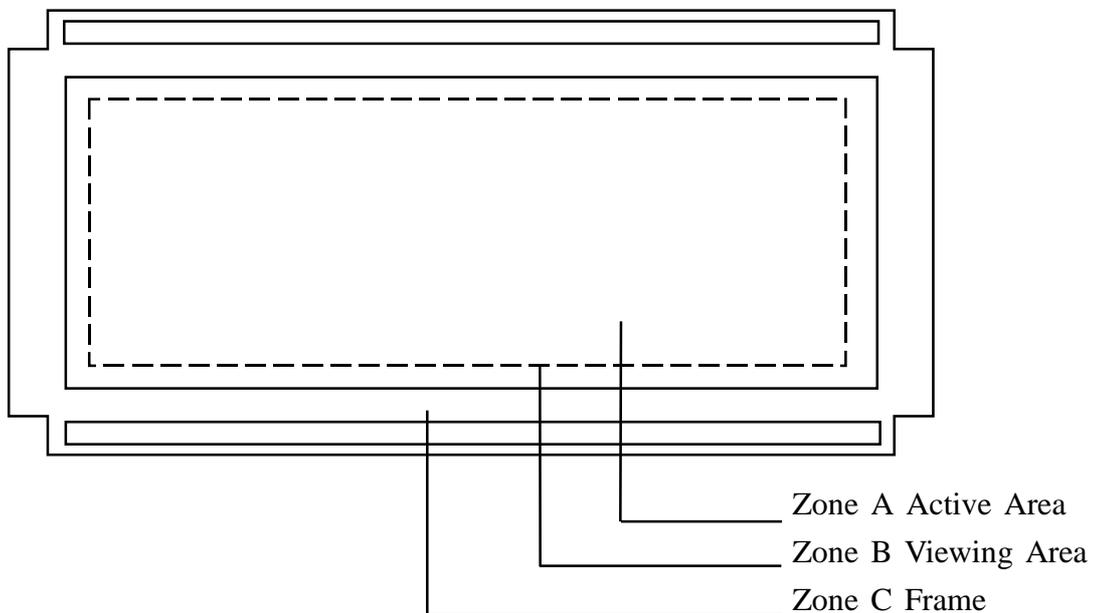
5-5 Inspection quality criteria

ITME	DESCRIPTION OF DEFECTS					Class of defects	Acceptable level (%)
FUNCTION	Short circuit or Pattern cut					Major	0.65
DIMENSION	Refer to individual acceptance specification					Major	2.5
BLACK SPOTS	Ave. dia. D		area A		area B	Minor	2.5
	D $\leqq$ 0.2		disregard				
	0.2 $<$ D $\leqq$ 0.3		3		4		
	0.3 $<$ D $\leqq$ 0.4		2		3		
	0.4 $<$ D		0		1		
BLACK LINES	Width W, Length L			A	B	Minor	2.5
	W $\leqq$ 0.03			disregard			
	0.03 $<$ W $\leqq$ 0.05			3	4		
	0.05 $<$ W $\leqq$ 0.07, L $\leqq$ 3.0			1	1		
BUBBLES IN POLARIZER	Average diameter D 0.2 $<$ D $<$ 0.5 mm for N = 4 , D $<$ 0.5 for N = 1					Minor	2.5
COLOR UNIFORMITY	Rainbow color or Newton ring.					Minor	2.5
GLASS SCRATCHES	Obvious visible damage.					Minor	2.5
VIEWING ANGLE	SEE NOTE 2					Minor	2.5
CONTRAST RATIO	SEE NOTE 3					Minor	2.5
RESPONSE TIME	SEE NOTE 1					Minor	2.5

5-6 Reliability

The LCD module should have no failure in the following reliability test.

TEST ITEM	TEST CONDITIONS	NOTE
HIGH TEMPERATURE OPERATION	60℃ , 200 hr.	NOTE
LOW TEMPERATURE STORAGE	-10℃ , 200 hr.	NOTE
HUMIDITY STORAGE	60℃ , 90%RH , 96hr.	NOTE
HIGH TEMPERATURE OPERATION	40℃, typical operating conditions, 200hr.	NOTE
TEMPERATURE CYCLING	-10℃~70℃ 10min. between each step temp. 50min. at each step temp. 5 cycles.	NOTE
MECHANICAL VIBRATION	10~55Hz sweep, 3G. amp1 =10mm(max) XYZ for 10min. each.	NOTE

NOTE1: The module should not have condensation of water on the module.

NOTE2: The module shelled be inspected after 1 hour storage in normal conditions (15~35°C, 45~65 % RH).

DEFINITIONS OF LIFE END POINT:

(1) Current drain should be smaller than the specified value.

(2) Function of the module should be maintained

(3) Appearance and display quality should not have distinguished degradation.

(4) Contrast ratio should be larger than 50% of initial value.

6. Designation of lot mark

6-1 Lot mark

Lot mark is consisted of 4 digit number.

| 4 | 0 | 5 | 1 |

Week
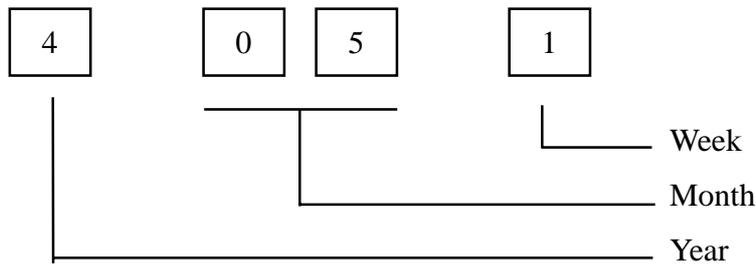
Month

Year

YEAR	FIGURE IN LOT MARK
1999	9
2000	0
2001	1
2002	2
2003	3
2004	4

MONTH	FIGURE IN LOT MARK	MONTH	FIGURE IN LOT MARK
Jan.	01	July	07
Feb.	02	Aug.	08
Mar.	03	Sept.	09
Apr.	04	Oct.	10
May.	05	Nov.	11
Jun.	06	Dec.	12

WEEK (DAY INCALENDAR)	FIGURE IN LOT MARK
1~7	1
8~14	2
15~21	3
22~28	4
29~31	5

7. Timing characteristics

(1) System buses

Read/write characteristics I (80-series MPU)
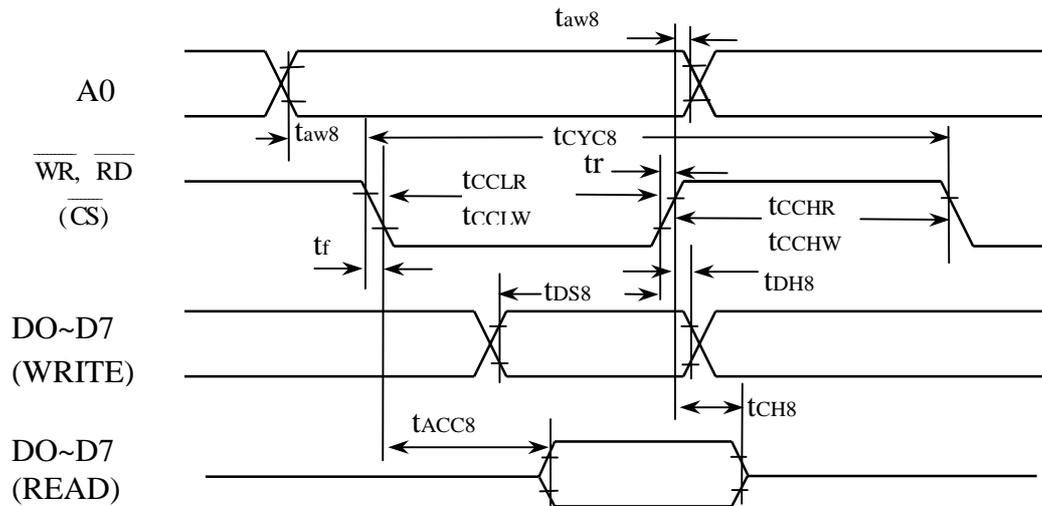
Item	Signal	Symbol	Conditions	VDD=5.0V		VDD2.7~4.5V		Unit
				Min.	Max.	Min.	Max.	
Address hold time	A0,CS	tAH8	-------	10	-----	0	-----	ns
Address setup time		tAW8		10	-----	0	-----	ns
System cycle time	-------	tCYC8	-------	200	-----	450	-----	ns
Control L pulse width (WR)	$\overline{WR}$	tCCLW		22	-----	44	-----	ns
Control H pulse width (RD)	$\overline{RD}$	tCCLR	-------	77	-----	194	-----	ns
Control L pulse width (WR)	$\overline{WR}$	tCCHW		172	-----	394	-----	ns
Control H pulse width (RD)	-------	tCCHR		117	-----	244	-----	ns
Data setup time	-------	tDS8	-------	20	-----	20	-----	ns
Data hold time		tDH8		10	-----	10	-----	ns
$\overline{RD}$ access time	D0 to D7	tACC8	CL=100pF	-----	70	-----	140	ns
Output disable time		tCH8	-------	10	50	10	100	ns
Input signal change time	-------	tr,tf	-------	-----	15	-----	15	ns

Notes: 1. When using the system cycle time in the high-speed mode, it is limited by tr+tf ≤ (tCYC8-tCCLW-tCCHW) or tr+tf ≤ (tCYC8-tCCLR-tCCHR)

2. All signal timings are limited based on the 20% and 80% of Vss voltage.

3. Read/Write operation is performed while CS ($\overline{CS1}$ and CS2) is active and the RD or WR signal is in the low level.

   If read/write operation is performed by the RD or WR signal while CS is active, it is determined by the $\overline{RD}$ or $\overline{WR}$ signal timing.

   If read/write operation is performed by CS while the RD or WR signal is in the low level, it is determined by the CS active timing.

(2) System buses
Read/write characteristics II (68-series MPU)
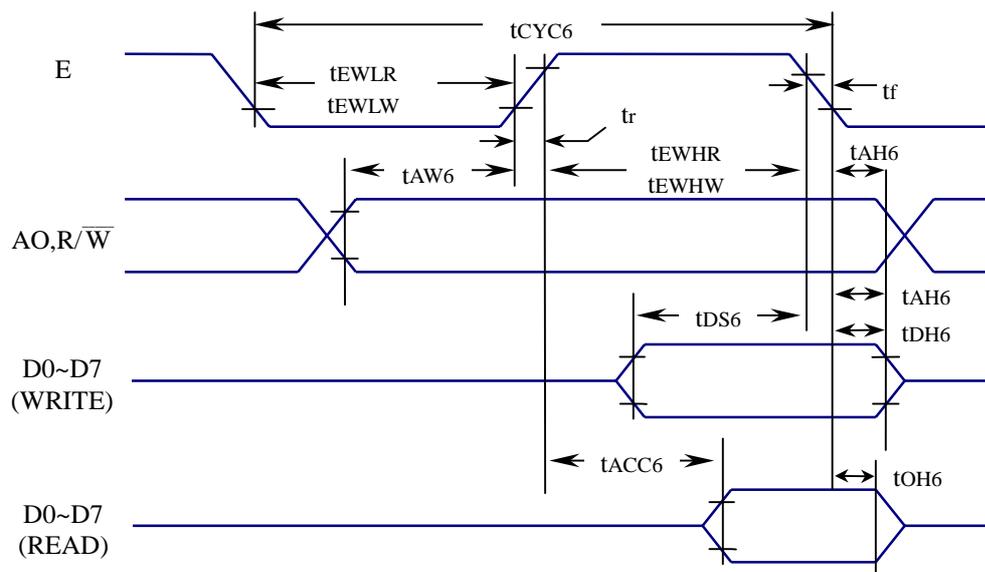
Item		Signal	Symbol	Conditions	V_DD=5.0V Min.	V_DD=5.0V Max.	V_DD=2.7V~4.5V Min.	V_DD=2.7V~4.5V Max.	UNIT
System cycle time		-------	t_{CYC6}	-------	200	-----	450	-------	ns
Address setup time	(A0)	t_{AW6}	-------	10	-----	0	-------	ns
Address hold time	R/$\overline{W}$	t_{AH6}		10	-----	0	-------	ns
Data setup time		t_{DS6}	-------	20	-----	20	-------	ns
Data hold time			t_{DH6}		10	-----	10	-------	ns
Output disable time	D0~D7	t_{OH6}	CL=100pF	10	50	20	100	ns
Access time		t_{ACC5}	-------	-----	70		140	ns
Enable H pulse Width	READ	E	t_{EWHR}	-------	77	-----	194	-------	ns
	WRITE		t_{EWHW}		22	-----	44	-------	ns
Enable L pulse width	READ	E	t_{EWLR}	-------	117	-----	244	-------	ns
	WRITE		t_{EWLW}		172	-----	394	-------	ns
Input signal change time		-------	t_r, t_f	-------	-----	15	-------	15	ns

Notes: 1. When using the system cycle time in the high-speed mode, it is limited by

$t_r + t_f \le (t_{CYC6} - t_{EWLW} - t_{EWHW})$ or $t_r + t_f \le (t_{CYC6} - t_{EWLR} - t_{EWHR})$.

2. All signal timings are limited based on the 20% and 80 % of Vss voltage.

3. Read/write operation is performed while CS (CS1 and CS2) is active and the E signal is in the high level.

If read/write operation is performed by the E signal while CS is active, it is determined by the E signal timing.

If read/write operation is performed by CS while the E signal is in the high level, it is determined by the CS active timing.

(3) Serial interface
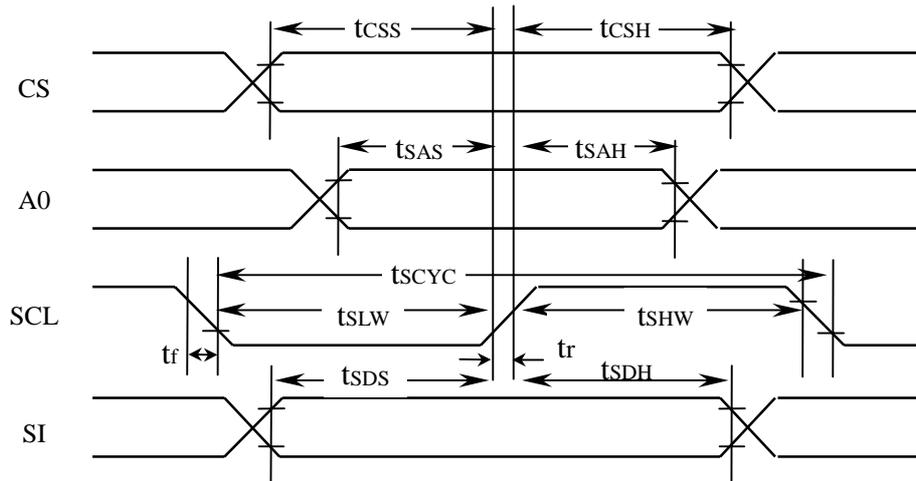
Item	Signal	Symbol	Conditions	VDD=5.0V		VDD=2.7~4.5V		Unit
				Min	Max.	Min	Max.	
Serial clock cycle SCL High pulse width SCL Low pulse width	SCL	tSCYC tSHW tSLW		500 150 150	------- 	1000 300 300	------- 	ns ns ns
Address setup time Address hold time	A0	tSAS tSAH	-------	120 200	-------	250 400	-------	ns ns
Data setup time Data hold time	SI	tSDS tSDH		120 50	-------	250 100	-------	ns ns
CS-SCL time	CS	tCSS tCSH		30 400	-------	60 800	-------	ns
Input signal change time	-------	tr,tf	-------	-------	50	-------	50	ns

*2   All signal timings are limited based on the 20% and 80% of Vss voltage.

8. Functional description

Microprocessor Interface

Parallel/serial interface

Parallel data can be transferred in either direction between the controlling microprocessor and the SED1560 series through the 8-bit I/O buffer (D0 to D7). Serial data can be sent from the microprocessor to the SED1560 series through the serial data input (SI), but not from the SED1560 series to the microprocessor. The parallel or serial interface is selected by P/S as shown in table1.

Table 1. Parallel/serial interface selection

P/S	Input type	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	C86	SI	SCL	D0 to D7
HIGH	Parallel	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	C86	$\times$	$\times$	DO to D7
LOW	Serial	$\overline{CS1}$	CS2	A0	$\times$	$\times$	$\times$	SI	SCL	(Hz)

Note $\times$=don't care

For the parallel interface, the type of microprocessor is selected by C86 as shown in Table 2.

Table 2. Microprocessor selection for parallel interface

C86	MPU bus type	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	D0 to D7
HIGH	6800-series	$\overline{CS1}$	CS2	A0	E	$R/\overline{W}$	D0 to D7
LOW	8080-series	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	D0 to D7

Parallel interface

A0, $\overline{WR}$ (or R/W) and $\overline{RD}$ (or E) identify the type of parallel data transfer to be made as shown in Table 3.

Table 3. Parallel data transfer

Common	6800 series		8080 series		Description
A0	$R/\overline{W}$	E	$\overline{RD}$	$\overline{WR}$	
1	1	1	0	1	Display data read out
1	0	1	1	0	Display data write
0	1	1	0	1	Status read
0	0	1	1	0	Write to internal. Register (command)

Serial interface

The serial interface comprises an 8-bit shift register and a 3-bit counter. These are reset when $\overline{CS1}$ is LOW and CS2 is HIGH. When these states are reversed, serial data and clock pulses can be received from the microprocessor on SI and SCL, respectively.

Serial data is read on the rising edge of SCL and must be input at SI in the sequence D7 to D0. On every eighth clock pulse, the data is transferred from the shift register and processed as 8-bit parallel data.

Input data is display data when A0 is HIGH and control data when A0 is LOW. A0 is read on the rising edge of every eighth clock signal.

The SLC signal is affected by the termination reflection and external noise caused by the line length. The operation check on the actual machine is recommended.
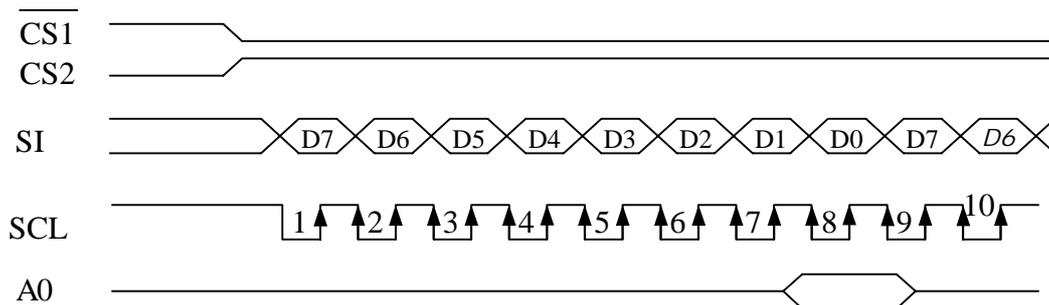

Figure 1. Serial interface timing

Chip select inputs

The SED1560 series has two chip select pins: $\overline{CS1}$ and CS2, and data exchange between the microprocessor and the SED1560 series is enabled when $\overline{CS1}$ is LOW and CS2 is HIGH. When these pins are set to any other combination, D0 to D7 are high impedance. The A0, $\overline{RD}$, $\overline{WR}$, SI and SCI inputs are disabled. If the serial input interface has been selected, the shift register and counter are reset. The Reset signal is entered independent from the $\overline{CS1}$ and CS2 status.

Data Transfer

To match the timing of the display data RAM and registers to that of the controlling microprocessor, the SED1560 series uses an internal data bus and bus buffer. A kind of pipeline processing takes place. When the microprocessor reads the contents of RAM, the data for the initial read cycle is first stored in the bus buffer (dummy read cycle.) On the next read cycle, the data is read from the bus buffer onto the microprocessor bus. At the same time, the next block of data is transferred from RAM to the bus buffer. Likewise, when the microprocessor writes data to display data RAM, the data is first stored in the bus buffer before being written to RAM at the next write cycle.

When writing data from the microprocessor to RAM, there is no delay since data is automatically transferred from the bus buffer to the display data RAM. If the data rate is required to slow down, the microprocessor can insert an NOP instruction which has the same affect as executing a wait procedure.

When a sequence of address sets is executed, a dummy read cycle must be inserted between each pair of address sets. This is necessary because the addressed data from the RAM is delayed one cycle by the bus buffer, before it is sent to the microprocessor. A dummy read cycle is thus necessary after an address set and after a write cycle.
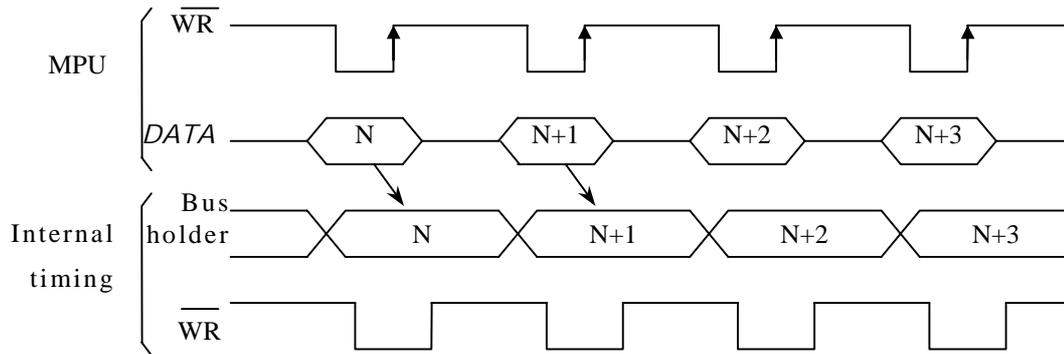
Figure2. Write timing
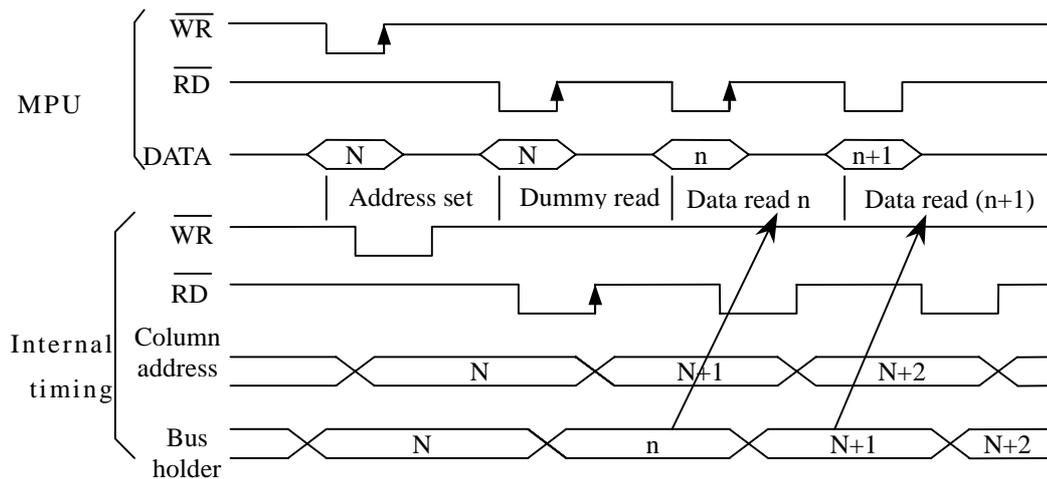
Figure3. Read timing

Status Flag

The SED1560 series has a single bit status flag, D7. When D7 is HIGH, the device is busy and will only accept a Status Read command. If cycle times are monitored   carefully, this flag does not have to be checked before each command, and microprocessor capabilities can be fully utilized.

Display Data RAM

The display data RAM stores pixel data for the LCD. It is a 166-column x 65-row addressable array as shown in figure 4.

(if the display start line is set to 1ch)

Page address	DATA	Column address	Line address		Common address
0 0 0 0	D0–D7	Page 0	00H–07		COM 0 – COM 7
0 0 0 1	D0–D7	Page 1	08–0F		COM 8 – COM15
0 0 1 0	D0–D7	Page 2	10–17		COM16 – COM23
0 0 1 1	D0–D7	Page 3	18–1F		COM24 – COM31
0 1 0 0	D0–D7	Page 4	20–27		COM32 – COM39
0 1 0 1	D0–D7	Page 5	28–2F		COM40 – COM47
0 1 1 0	D0–D7	Page 6	30–37		COM48 – COM55
0 1 1 1	D0–D7	Page 7	38–3F		COM56 – COM63
1 0 0 0	D0	Page 8			COM 1

1/64 Start 1/32

ADC	D0 =1	A5	A4	A3	A2	A1	A0	9F	9E	to	O3	O2	O1	O0	A5
	D0 =0	00	01	02	03	04	05	06	07	to	A2	A3	A4	A5	
LCD OUT		O0	O1	O2	O3	O4	O5	O6	O7	to	O162	O163	O164	O165	

*Figure 4. Display data RAM addressing*

For a 1/65 and 1/33 display duty cycles, page 8 is accessed following 1BH and 3BH, respectively. The 65 rows are divided into 8 pages of 8 lines and a ninth page with a single line (D0 only). Data is read from or written to the 8 lines of each page directly through D0 to D7. The time taken to transfer data is very short, because the microprocessor inputs D0 to D7 correspond to the LCD common lines as shown in figure 5. Large display configurations can thus be created using multiple SED1560s.
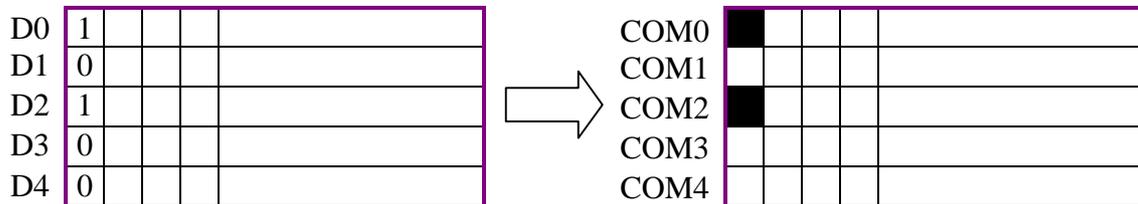

Figure 5. RAM-to-LCD data transfer

The microprocessor reads from and writes to RAM through the I/O buffer. Since the LCD controller operates independently, data can be written to RAM at the same time as data is being displayed, without causing the LCD to flicker.

Column Address Counter

The column address counter is an 8-bit preset table counter that provides the column address to display data RAM. See figure 4. It is incremented by 1 each time a read or write command is received. The counter automatically stops at the highest address A6H. The contents of the column address counter are changed by the Column Address Set command. This counter is independent of the page address register.

When the Select ADC command is used to select inverse display operation, the column address decoder inverts the relationship between the RAM column data and the display segment outputs.

Page Address Register

The 4-bit page address register provides the page address to display data RAM. The contents of the register are changed by the Page Address Set command.

Page address 8 (D3 = H, D2, D1, D0 = L) is a special use RAM area for the indicator.

Initial Display Line Register

The initial display line register stores the address of the RAM line that corresponds to the first (normally the top) line (COM0) of the display. See figure 4. The contents of this 6-bit register are changed by the Initial Display Line command. At the start of each LCD frame, synchronized with SYNC, the initial line is copied to the line counter.

The line counter is then incremented on the CL clock signal once for every display line. This generates the line addresses for the transfer of the 166 bits or RAM data to the LCD drivers.

If a 1/65 or 1/33 display duty cycle is selected by the Duty + 1 command, the line address corresponding to the 65th or 33rd SYNC signal is changed and the indicator special-use line address is selected. If the Duty + 1 command is not used, the indicator special-use line address is not selected.

Output Selection Circuit

The number of common (COM) and segment (SEG) driver outputs can be selected to fit different LCD panel configurations by the output selection circuit.

There are 70 segment-only outputs (O32 to O101) and 96 common or segment dual outputs (O0 to O31 and O102 to O165). A command select the status of the dual common/segment outputs. Figure 6 shows the six different LCD driver arrangements.

Necessary LCD driver voltage is automatically allocated to the COM/SEG dual outputs when their function is determined by the output selection circuit.

The SED1560 selects Case 1,2 or 6 while the SED1561 selects Case3,4,5 or 6. As to the SED1562, COM/SEG output status cannot be selected, being fixed.

| ADC | L | 0 | → | Column address | → | 165 |
| (D0) | H | 165 | ← | | ← | 0 |

Display data RAM

Case1 — 102 segments | 64 commons
Case2 — 32 commons | 102 segments | 32 commons
Case3 — 32 commons | 134 segments
Case4 — 134 segments | 32 commons
Case5 — 16 commons | 134 segments | 16 commons
Case6 — 166 segments

O0   O15   O31   O101   O133   O149   O165
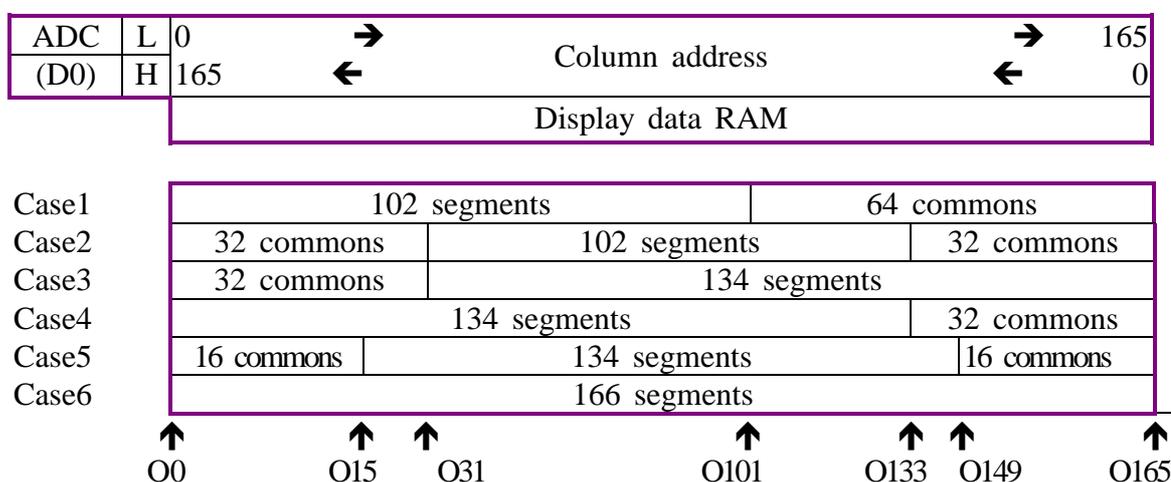
Figure 6. Output configuration selection

When COM outputs are assigned to the output drivers, the unused RAM area is not available. However, all RAM column addresses can still be accessed by the microprocessor.

Since duty setting and output selection are independent, the appropriate duty must be selected for each case. Cases 1 to 6 are determined according to the three lowest bits in the output status register in the output selection circuit. The COM output scanning direction can be selected by setting bit D3 in the output status register to "H" or "L".

Table 4.

	SED1560		SED1561		SED1562
Duty	1/64	1/48	1/32	1/24	1/16
COM I function	COM64	COM48	COM32	COM24	COM16

When the DUTY + 1 command is executed, pin COM1 becomes as shown in Figure 4 irrelevant to output selection.

Since master/slave operation and the output selection circuit are completely independent in the SED1560 series, a chip either on the master or slave side can be allocated to the COM output function in multi-chip configuration.

The LCD driver outputs shown in Table 5 become ineffective when the SED1560 or SED1561 is used with 1/48 OR 1/24 duty, respectively. In this case, ineffective outputs are used in the open state.

Table 5

-------	-------	Output status register				Ineffective output		
		D3	*D2*	*D1*	*D0*			
SED 1560	Case 1	0	1	0	1	O150	to	O165
		1	1	0	1	O102	to	O117
	Case 2	0	1	0	0	O150	to	O165
		1	1	0	0	O16	to	O31
SED 1561	Case 3	0	0	1	1	O0	to	O7
		1	0	1	1	O23	to	O31
	Case 4	0	0	1	0	O158	to	O165
		1	0	1	0	O134	to	O141
	Case 5	0	0	0	1	O158	to	O165
		1	0	0	1	O8	to	O15

SED1560 Output status

The SED1560 selects any output status from Cases 1,2 and 6.

1/64 duty (Display Area 64*102)

Case	Status register				LCD driver output					
	D3	D2	D1	D0	O0 ... O31	O32 ... O101	O102 ... O133	O134 ... O165		
1	0	1	0	1	SEG102		COM0 →			COM63
	1	1	0	1	SEG102		COM63 ←			COM0
2	0	1	0	0	COM31 ←COM0	SEG102		COM32 →		COM63
	1	1	0	0	COM32 →COM63	SEG102		COM31 ←		COM0
6	—	0	0	0	SEG166					

1/48 duty (display Area 48*102)

Case	Status register				LCD driver output					
	D3	D2	D1	D0	O0 ... 031	032 ... O101	O102 ... O133	O134 ... O165		
1	0	1	0	1			COM0 → COM47	■		
	1	1	0	1			■ COM47 ←			COM0
2	0	1	0	0	COM31←COM0	SEG102		COM32 → 47		■
	1	1	0	0	COM32→47 ■	SEG102		COM31 ←		COM0
6	—	0	0	0	SEG166					

SED1561 Output Status

The SED1561 selects any output status from Cases 3,4,5 and 6.

1/32 duty (Display Area 32*134)

Case	D3	D2	D1	D0	O0 O15	O16 O31	O32 O133	O134 149	150 O165
3	0	0	1	1	COM31 ← COM0		SEG134		
3	1	0	1	1	COM0 → COM31		SEG134		
4	0	0	1	0	SEG134			COMO →	M31
4	1	0	1	0	SEG134			COM31 ←	COM0
5	0	0	0	1	15←COMO	SEG134			COM16→31
5	1	0	0	1	COM16→31	SEG134			15←COM0
6	—	0	0	0	SEG166				

1/24 duty (Display Area 24*134)

Case	D3	D2	D1	D0	O0 O15	O16 O31	O32 O133	O134 149	150 O165
3	0	0	1	1	■ COM23 ← COM0		SEG134		
3	1	0	1	1	COM0 → COM23 ■		SEG134		
4	0	0	1	0	SEG134			COMO → COM23	■
4	1	0	1	0	SEG134			■ COM23 ← COM0	
5	0	0	0	1	15 ← COMO	SEG134			16→23 ■
5	1	0	0	1	16 →23 ■	SEG134			15←COM0
6	—	0	0	0	SEG166				

SED1562 Output Status

COM/SEG output status of the SED1562 is fixed.

1/16 duty (16*150)

LCD driver output		
00 0149	150 0165	
SEG150	15 ← COM0	

Reset

When power is turned ON, the SED1560 is initialized on the rising edge of $\overline{RES}$.   Initial settings are as follows.

1. Display	:	OFF
2. Display mode	:	Normal
3. n-line inversion	:	OFF
4. Duty cycle	:	1/64 (SED1560)
	:	1/32 (SED1561)
5. ADC select	:	Normal (D0=L)
6. Read/write modify	:	OFF
7. Internal power supply	:	OFF
8. Serial interface register data	:	Cleared
9. Display initial line register	:	Line 1
10. Column address counter	:	0
11. Page address register	:	Page 0
12. Output selection circuit	:	Case6
13. n-line inversion register	:	16

14. Set the electronic control register to zero (0).

$\overline{RES}$ should be connected to the microprocessor reset terminal so that both devices are reset at the same time $\overline{RES}$ must be LOW for at least $1\mu s$ to correctly reset the SED1560. Normal operation starts $1\mu s$ after the rising edge on $\overline{RES}$.

If the built-in LCD power circuit of the SED156*D*B is not used, the $\overline{RES}$ signal must be low when the external LCD power supply is turned on. When the $\overline{RES}$ goes low, each register is cleared to the above listed initial status. However, the oscillation circuit and output pins (OSC2, FR, SYNC, CLD, DYO, D0 to D7 pins) are not affected. If the SED1560 is not properly initialized when power is turned ON, it can lock itself into a state that cannot be cancelled. When the Reset command is used, only initial settings 9 to 14 are active.

9. Commands

The Command Set

A0, $\overline{RD}$ (E) and $\overline{WR}$ (R/$\overline{W}$) identify the data bus commands. Interpretation and execution of commands are synchronized to the internal clock. Since a busy check is normally not needed, commands can be processed at high speed.

For the 80-series MPU interface, the command is activated when a low pulse is entered in the $\overline{RD}$ Pin during read or when a low pulse is entered in the $\overline{WR}$ pin during write. While the 68-series MPU interface is set to the read status when a high pulse is entered in the R/$\overline{W}$ pin, and it is set to the write status when a low pulse is entered in this pin.

The command is activated when a high pulse is entered in the E pin. (For their timings, see Section 10 "Timing Characteristics") Therefore, the 68-series MPU interface differs from the 80-series MPU interface in the point where the $\overline{RD}$ (or $\overline{E}$) signal is 1 (or high) during status read and during display data read explained in the command description and on the command table. The following command description uses an 80-series MPU interface example.

If the serial interface is selected, data is sequentially entered from D7.

Table 7. SED1560 series command table

Command	Code											Function
	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
Display ON/OF	0	1	0	1	0	1	0	1	1	1	0 / 1	Turns the LCD display ON and OFF 0 :OFF 1: ON
Display START Line set	0	1	0	0	1	Display start address						Determines the RAM display line for COM0
Page address set	0	1	0	1	0	1	1	Page address				Sets the display RAM Pages in the Page Address register.
Column address set; high-order 4 bits	0	1	0	0	0	0	1	High-order Column address				Sets the high-order4 bits of the display RAM Column address in the register.
Column address set; low-order 4 bits.	0	1	0	0	0	0	0	Low-order Column address				Sets the low-order 4 bits of the display RAM column address in the register.
Status read	0	0	1	Status				0	0	0	0	Reads the status information.
Display data write	1	1	0	Write Data								Writes data in the display RAM.
Display data read	1	0	1	Read Data								Reads data from the display RAM.
ADC select	0	1	0	1	0	1	0	0	0	0	0 / 1	Outputs the display RAM address for SEG. 0: Normal 1:Reversed

Command	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function
Normal/reverse display	0	1	0	1	0	1	0	0	1	1	0 1	Displays the LCD image in normal or reverse mode. 0: Normal 1: Reversed
All indicator ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	Lights all indicators. 0: Normal display 1: All ON
Duty select	0	1	0	1	0	1	0	1	0	0	0 1	Sets LCD drive duty (1). 0:1/24, 48 1:1/32, 64
Duty + 1	0	1	0	1	0	1	0	1	0	1	0 1	Sets LCD drive duty(2). 0: Normal 1:Duty+1
n-line reverse register set	0	1	0	0	0	1	1	No. of reversed n-lines				Sets the line reverse driving and No. of reverse lines in the line reverse register.
n-line reverse register release	0	1	0	0	0	1	0	0	0	0	0	Releases the line reverse driving.
Read Modify write	0	1	0	1	1	1	0	0	0	0	0	Increments by 1during write of column address counter, and set to 0 during read.
End	0	1	0	1	1	1	0	1	1	1	0	Releases the Read Modify write mode.
Reset	0	1	0	1	1	1	0	0	0	1	0	Internal reset
Output status register set	0	1	0	1	1	0	0	Output status				Sets the COM and SEG status in registers.
Built-in power Supply ON/OFF	0	1	0	0	0	1	0	0	1	0	0 1	0: Power OFF 1: Power ON
Power-on Completion	0	1	0	1	1	1	0	1	1	0	1	Completes the turn-on sequence of built-in power supply
Electronic control register set	0	1	0	1	0	0	Electronic control value					Sets the V5 output voltage in the electronic control register.
Power save												A complex command to turn off the display and light all indictors.

Commands

Display ON/OFF

Alternatively turns the display ON and OFF.

A0	$\dfrac{E}{RD}$	$\dfrac{R/W}{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	1	1	D

Note

D = 0   Display OFF
D = 1   Display ON

Initial Display Line

Loads the RAM line address of the initial display line, COM0, into the initial display line register. The RAM display data becomes the top line of the LCD screen. It is followed by the higher number lines in ascending order, corresponding to the duty cycle. The screen can be scrolled using this command by incrementing the line address.

A0	$\frac{E}{RD}$	$\frac{R/W}{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	1	A5	A4	A3	A2	A1	A0

A5	A4	A3	A2	A1	A0	Line address
0	0	0	0	0	0	0
0	0	0	0	0	1	1
0	0	0	0	1	0	2
		↓				↓
1	1	1	1	1	0	62
1	1	1	1	1	1	63

Page Address Set

Loads the RAM page address from the microprocessor into the page address register. A page address, along with a column address, defines a RAM location for writing or reading display data. When the page address is changed, the display status is not affected.

Page address 8 is a special use RAM area for the indicator. Only D0 is available for data exchange.

A0	$\frac{E}{RD}$	$\frac{R/W}{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	1	A3	A2	A1	A0

A3	A2	A1	A0	Page
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8

Column Address set

Loads the RAM column address from the microprocessor into the column address register. The column address is divided into two parts-4 high-order bits and 4 low-order bits.

When the microprocessor reads or writes display data to or from RAM, column addresses are automatically incremented, starting with the address stored in the column address register and ending with address 166.

A0	$\dfrac{E}{RD}$	$\dfrac{R/W}{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	0	1	A7	A6	A5	A4

A0	$\dfrac{E}{RD}$	$\dfrac{R/W}{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	0	0	A3	A2	A1	A0

A7	A6	A5	A4	A3	A2	A1	A0	Column address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
↓								↓
1	0	1	0	0	1	0	1	165

Read status

Indicated to the microprocessor the four SED1560 status conditions.

A0	$\dfrac{E}{RD}$	$\dfrac{R/W}{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	Busy	ADC	ON/OFF	RESET	0	0	0	0

BUSY — Indicates whether or not the SED1560 will accept a command. If BUSY is 1, the device is currently executing a command or is resetting, and no new commands can be accepted. If BUSY is 0, a new command can be accepted It is not necessary for the microprocessor to check the status of this bit if enough time is allowed for the last cycle to be completed.

ADC — Indicates the relationship between RAM column addresses and the segment drivers. If ADC is 1, the relationship is normal and column address n corresponds to segment driver n. If ADC is 0, the relationship is inverted and column address (165- n) corresponds to segment driver n.

ON/OFF Indicates whether the display is ON or OFF. If ON/OFF is 1, the display is OFF. If ON/OFF is 0, the display is ON. Note that this is the opposite of the Display ON/OFF command.

RESET Indicates when initialization is in process as the result of RES or the Reset command.

Write Display Data

Writes bytes of display data from the microprocessor to the RAM location specified by the column address and page address registers. The column address is incremented automatically so that the microprocessor can continuously write data to the addressed page.

A0	$\dfrac{E}{RD}$	$\dfrac{R/\overline{W}}{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	Write data							

Read Display Data

Sends bytes of display data to the microprocessor from the RAM location specified by the column address and page address registers. The column address is incremented automatically so that the microprocessor can continuously read data from the addressed page. A dummy read is required after loading an address into the column address register.

Display data cannot be read through the serial interface.

A0	$\dfrac{E}{RD}$	$\dfrac{R/\overline{W}}{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	Read data							

Select ADC

Selects the relationship between the RAM column addresses and the segment drivers. When reading or writing display data. The column address is incremented as shown in figure 4.

A0	$\dfrac{E}{RD}$	$\dfrac{R/\overline{W}}{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	0	0	D

Note

D = 0 Rotate right (normal direction)

D = 1 Rotate left (reverse direction)

The output pin relationship can also be changed by the microprocessor. There are very few restrictions on pin assignments when constructing a LCD module.

Normal/Inverse Display

Determines whether the data in RAM is displayed normally or inverted.

A0	$\dfrac{E}{RD}$	$\dfrac{R/\overline{W}}{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	1	1	D

Note

D = 0 LCD segment is ON when RAM data is 1 (normal).

D = 1 LCD segment is ON when RAM data is 0 (inverse).

Display All Points ON/OFF

Turns all LCD points ON independently of the display data in RAM. The RAM contents are not changed. This command has priority over the normal/inverse display command.

A0	$\dfrac{E}{RD}$	$\dfrac{R/\overline{W}}{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	1	0	D

Note

D = 0   Normal display status

D = 1   All display Segments ON

If this command is received when the display status is OFF, the Power Save command is executed.

Select Duty

Selects the LCD driver duty.

Since this is independent from contents of the output status register, the duty must be selected according to the LCD output status.

In multi-chip configuration, the master and slave devices must have the same duty.

A0	$\dfrac{E}{RD}$	$\dfrac{R/\overline{W}}{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	0	0	D

Model	D	Duty
SED1560	0	1/48
	1	1/64
SED1561	0	1/24
	1	1/32
SED1562	0	1/16
	1	1/16

Duty + 1

Increases the duty by 1. If 1/48 or 1/64 duty is selected in the SED1560 for example, 1/49 or 1/65 is set, respectively and COM1 functions as either the COM48 or COM64 output. The display line always accesses the RAM area corresponding to page address 8, D0. (Refer to Figure 4). In multi-chip configuration, the Duty+1 command must be executed to both the master and slave sides.

A0	$\frac{E}{RD}$	$\frac{R/\overline{W}}{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	0	1	D

Model	D	Duty
SED1560	0 1	1/48 or 1/64 1/49 or 1/65
SED1561	0 1	1/24 or 1/32 1/25 or 1/33
SED1562	0 1	1/16 1/17

Set n-line E inversion

Selects the number of inverse lines for the LCD AC controller. The value of n is set between 2 to 16 and is stored in the n-line inversion register.

A0	$\frac{E}{RD}$	$\frac{R/\overline{W}}{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	1	A3	A2	A1	A0

A3	A2	A1	A0	Number of inverted lines
0	0	0	0	—
0	0	0	1	2
0	0	1	0	3
	↓			↓
1	1	1	0	15
1	1	1	1	16

Cancel n-line Inversion

Cancels n-line inversion and restores the normal 2-frame AC control. The contents of the contents of the n-line inversion register are not changed.

A0	$\frac{E}{RD}$	$\frac{R/\overline{W}}{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	0	0	0	0	0

Modify Read

Following this command, the column address is no longer incremented automatically by a Read Display Data command. The column address is still incremented by the Write Display Data command. This mode is cancelled by the End command. The column address is then returned to its value prior to the Modify Read command. This command makes it easy to manage the duplication of data from a particular display area for features such as cursor blinking.

A0	$\dfrac{E}{RD}$	$\dfrac{R/W}{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0

Note that the Column Address Set command cannot be used in modify-read mode.

Page address set.

↓

Column address set.

↓

Read-modify-write cycle.

↓

Dummy read.

↓

Data read

↓

Data write.

↓

Changes Finished?   No

Yes

↓

END
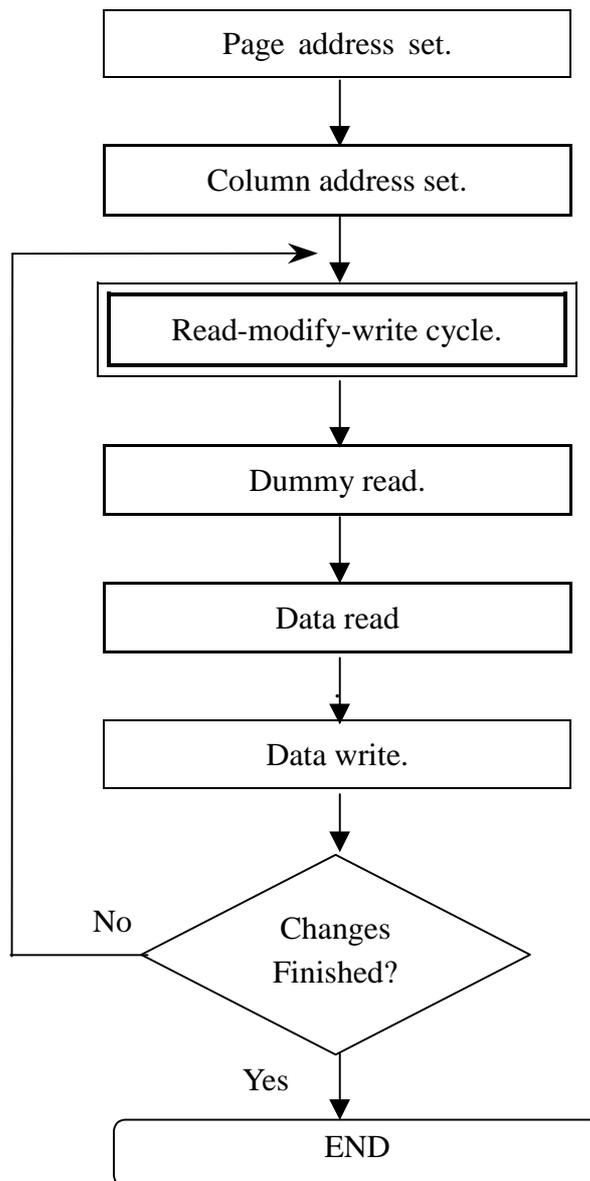
Figure 13. Command sequence for cursor blinking

Column address N N+1 N+2 N+3 -------- N+m N Read-modify-write mode set Return End
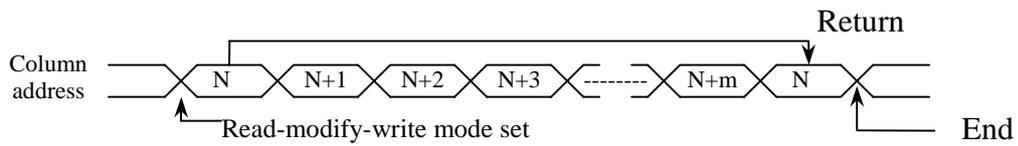
End

Cancels the modify read mode. The column address prior to the Modify Read command is restored.

A0	$\frac{E}{RD}$	$\frac{R/\overline{W}}{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0

Reset

Resets the initial display line, column address, page address, and n-line inversion registers to their initial values. This command does not affect the display data in RAM

A0	$\frac{E}{RD}$	$\frac{R/\overline{W}}{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	0

The reset command does not initialize the LCD power supply. Only RES can be used to initialize the supplies.

Output Status Register

Available only in the SED1560 and SED1561

This command selects the role of the COM/SEG dual pins and determines the LCD driver output status.

The COM output scanning direction can be selected by setting A3 to "H" or "L". For details, refer to the Output Status Circuit in each function description.

A0	$\frac{E}{RD}$	$\frac{R/\overline{W}}{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	0	A3	A2	A1	A0

A3: Selection of the COM output scanning direction.

A_2	A_1	A_0	Output Status	Number of COM/SEG Output pins	Remarks
0	0	0	Case6	SEG 166	Applies to the SED1560/61
0	0	1	Case5	SEG 134,COM32	Applies to the SED1561
0	1	0	Case4	SEG 134,COM32	
0	1	1	Case3	SEG 134,COM32	
1	0	0	Case2	SEG 102,COM64	Applies to the SED1560
1	0	1	Case1	SEG 102,COM64	
1	1	0	Case6	SEG 166	Applies to the SED1560/61
1	1	1	Case6	SEG 166	

LCD Power Supply ON/OFF

Turns the SED156*D*B internal LCD power supply ON or OFF. When the power supply is ON, the voltage converter, the voltage regulator circuit and the voltage followers are operation. For the converter to function, the oscillator must also be operation.

A0	$\frac{E}{RD}$	$\frac{R/\overline{W}}{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	0	0	1	0	0

Note

D = 0 supply OFF

D = 1 supply ON

When an external power supply is used with the SED1560 series, the internal supply must be OFF. If the SED1560 series is used in a multiple-chip configuration, an external power supply that meets the specifications of the LCD panel must be used. An SED1560 operating as a slave must have is internal power supply turned OFF.

Completion of Built-in Power On

This command turns on the built-in power supply.

A0	$\frac{E}{RD}$	$\frac{R/\overline{W}}{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	0	1

The SED1560 series has the built-in, low-power LCD driving voltage generator circuit which can cut almost all currents except those required for LCD display. This is the primary advantage of the SED1560 series product. However, it has the low power and you need perform the following power-on sequence when turning on the built-in power supply.

Sequence in the Built-in Power ON/OFF Status

To turn on internal power supply, execute the above built-in power supply On sequence. To turn OFF internal power supply execute the power save sequence as shown in the following power supply OFF status. Accordingly, to turn on internal power supply again after turn it OFF (power save), execute the "Power Save Clear Sequence" that will be described afterwards.

Internal power supply ON status

Reset by RES signal

*1	Output Status Select	Command	A*(H)
*2	*DUTY+1	Command	AB*(H)*
	Electronic Volume Control	Setup	**(H)
	Internal Power Supply ON	Command	25(H)
*4	(Waiting time)		
*3	Power Supply Startup End	Command	ED(H)

Internal power supply OFF status

	Display OFF	Command	AE(H)
	Output Status case 6	Command	CH(F)
*2	*DUTY+1 Clear	Command	AA(H)
	Display All ON	Command	A5(H)
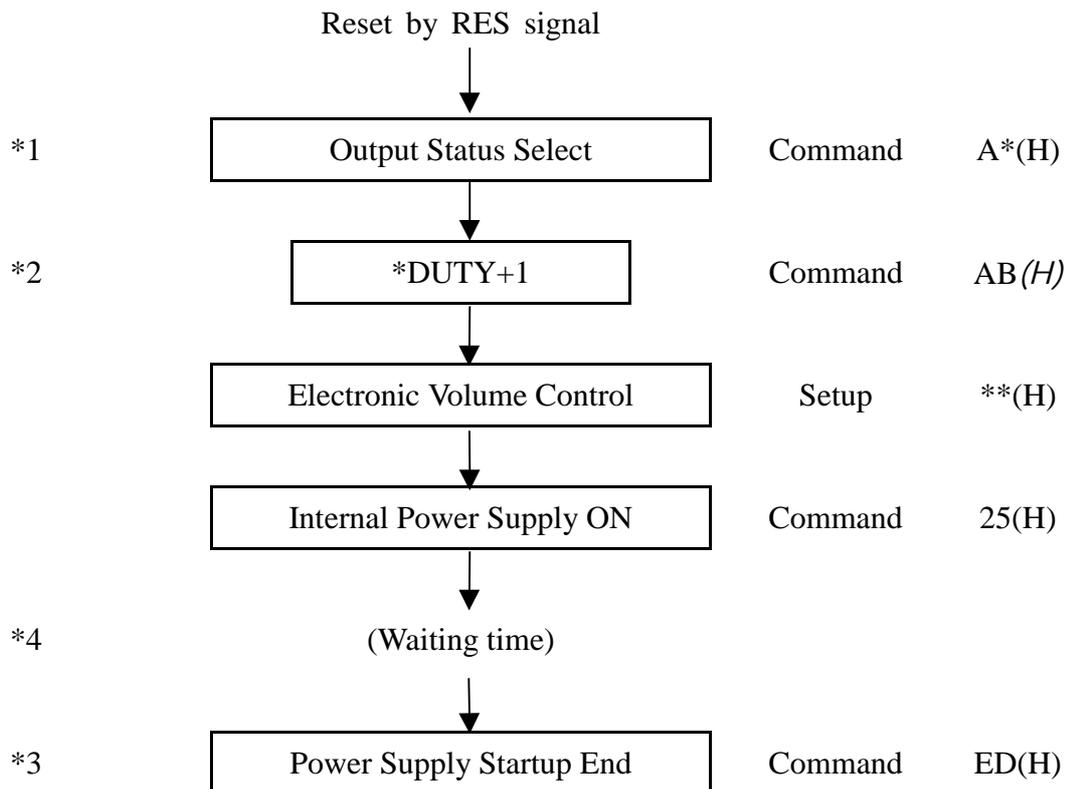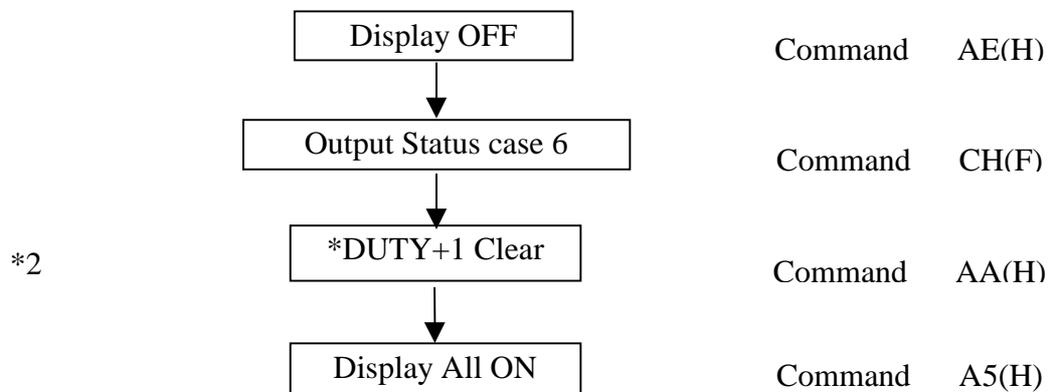
*1: Regarding the SED1562, it is not necessary to execute a command to decide an output status.

*2: When the COMI pin is not used, it is not necessary to enter the DUTY+1 and DUTY+1 Clear commands.

*3: When the built-in power supply startup end command is not executed, current is consumed stationary.

Internal power supply startup end command must always be used in a pair with internal power supply ON command.

*4: Within the waiting time in internal power supply ON status, any command other than internal power supply control commands such as Power Save, and display ON/OFF command, display normal rotation/reverse command, display all ON command, output status select command and DUTY+1 clear command can accept another command without any problem. RAM read and write operations can be freely performed

Electronic Volume control Register

Through these commands, the liquid crystal driving voltage V5 being outputted from the voltage regulation circuit of the built-in liquid crystal power supply, in order to adjust the contrast of the liquid crystal display.

By setting data to the 4bit register, one of the 16 voltage status may be selected for the liquid crystal driving voltage V5. External resistors are used for setting the voltage regulating range of the V5. For details refer to the paragraph of the voltage regulation circuit in the Clause for the explanation of functions.

A0	$\frac{E}{RD}$	$R/\frac{W}{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	A5	A4	A3	A2	A1	A0

A4	A3	A2	A1	A0	IV5I
0	0	0	0	0	Small(as the absolute value)
		:			
		:			
1	1	1	1	1	Large (as the absolute value)

When not using the electronic volume control function, set to (0,0,0,0,0).

Power Save (Complex Command)

If the Display All Points ON command is specified in the display OFF state, the system enters the power save status, reducing the power consumption to approximate the static power consumption value. The internal state in the power save status is as follows.

(a) The oscillator and power supply circuits are stopped.

(b) The LCD driver is stopped and segment and common driver outputs output the VDD level.

(c) An input of an external clock is inhibited and OSC2 enters the high-impedance state.

(d) The display data and operation mode before execution of the power save command are held.

(e) All LCD driver voltages are fixed to the VDD level.

The power save mode is cancelled by entering either the Display ON command or the Display All Points OFF command (display operation state). When external voltage driver resistors are used to supply the LCD driver voltage level, the current through them must be cut off by the power save signal.

If an external power supply is used, it must be turned OFF using the power save signal in the same manner and voltage levels must be fixed to the floating or VDD level.

Sequence in the Power Save Status

Power Save and Power Save Clear must be executed according to the following sequence.

To give a liquid crystal driving voltage level by the externally-installed resistance dividing circuit, the current flowing in this resistance must be cut before or concurrently with putting the SED1560 series into the power save status so that it may be fixed to the floating or VDD level.

When using an external power supply, likewise, its function must be stopped before or concurrently with putting the SED1560 series into the power save status so that it may be fixed to the floating or VDD level. In a configuration in which an exclusive common driver such as SED1630 is combined with the SED1560 series, it is necessary to stop the external power supply function after putting all the common output into non-selection level.

Power save sequence

Display OFF	Command	AE(H)

↓

*3	Output Status case 6	Command	CF(H)

↓

*2	*DUTY+1 Clear	Command	AA(H)

↓

*1	Display All ON	Command	A5(H)
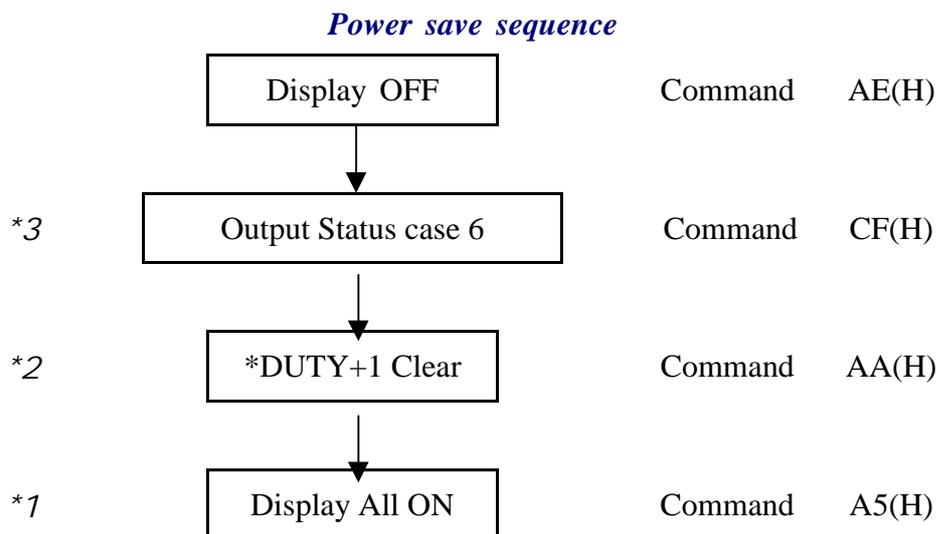
*1: In the power save status is provided after the display all ON command. In the power save clear sequence, the power save status is cleared after the display all ON status OFF command.

*2: When the COMI pin is not used, it is not necessary to enter the DUTY+1 command and DUTY+1 clear command.

*3: In the SED1562, it is not necessary to execute a command to decide an output status.

*4: The display ON command can be executed any where if it is later than the display all ON status OFF command.

*5 When internal power supply startup end command is not executed, current is consumed stationary. Internal power supply startup end command must always be used in a pair with internal power supply ON command.

Power save clear sequence

Reset by RES signal

*3	Output Status Select	Command C*(H)
*2	DUTY + 1	Command AB(H)
	Internal Power Supply ON	Setup 25(H)
	Display All On Status OFF	
*1	(Waiting time)	
*5	Power Supply Startup End	Command ED (H)