REV 2.3

Interface Description

uPatch100 GPS Receiver

This document describes the mechanical and electrical interfaces of the uPatch100 GPS receiver module.

August 10th 2004

Fastrax Ltd.

CHANGE LOG

Rev.	Notes	Date
1.0	Preliminary specification	13-04-2004
1.1	Pin-out change	23-04-2004
1.2	Ordering Information added	04-05-2004
1.3	Changed name from uPatch22-L to uPatch100-L	04-05-2004
1.4	Small changes	07-05-2004
1.5	Added description of valid fix indicator output. Added also supply voltage description.	13-05-2004
1.6	Added 1PPS output description	14-05-2004
1.7	Added antenna tuning information	23-06-2004
2.0	Added application note for power supply alternatives	29-07-2004
2.1	Sensitivity specification added	02-08-2004
2.2	Description of 2D/3D positioning added	10-08-2004
2.3	Changed name from uPatch100-L to uPatch100	16-09-2004

CONTENTS

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COMPLEMENTARY READING

The following reference documents are complementary reading for this document:

Ref. #	File name	Document name

1.   SYSTEM DESCRIPTION

1.1   General Description

A complete GPS receiver with an on-board antenna is implemented on the uPatch100 module. The module includes the following features:

- 28 x 28 mm PCB form factor (antenna included)
- Two external, regulated +3.3V..+5.5V supplies
- 8-pin pad row w/ 1.27mm spacing
- High performance 25x25x4mm patch antenna
- One UART port (RS232 or CMOS levels) for serial data
- GPIO9 output dedicated for valid fix indication
- Pulse per second (PPS) output
- 32768Hz RTC

The basic receiver connection consists of the following external connections:

- Regulated +3.3V...+5.5V supply
- Optional battery backup supply, regulated +3.3V...+5.5V
- Serial data port (RXD0 and TXD0)

1.2   Antenna Considerations

The uPatch100 includes a patch antenna element which is tuned to 1578MHz on the 28x28mm GND plane. It is tuned on purpose 3MHz above L1 center frequency (1575MHz) in order to compensate the detuning effect of typical plastic covers or housings. Usually plastic covers shift the resonance frequency of the antenna downwards when it is placed closed to the antenna element.

Please contact Fastrax for further information about antenna tuning issues if needed.

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1.3   Physical specification

- Size (incl. antenna):   28 x 28 x 7.0mm [W x L x H]
- Weight: 20 g
- Operating Temperature: -30 ºC to +85 ºC
- Operating Humidity: 0% to 95% RH, non condensing
- Vibration   4 G

1.4   Technical specification

- Receiver: L1, C/A code
- Channels: 12
- Update rate: 1 Hz
- Power supply: +3.3..5.5V regulated power supply
- Power Consumption:
      Normal mode: 76 mA (Search Engine On)
                          44 mA (Search Engine Off)
      Battery backup: 150uA typical
- Protocols: NMEA-0183 V3.0

- Sensitivity:
      Acquisition: -139dBm (unaided)
      Navigation: -150dBm
      Tracking: -152dBm

1.5   Block diagram
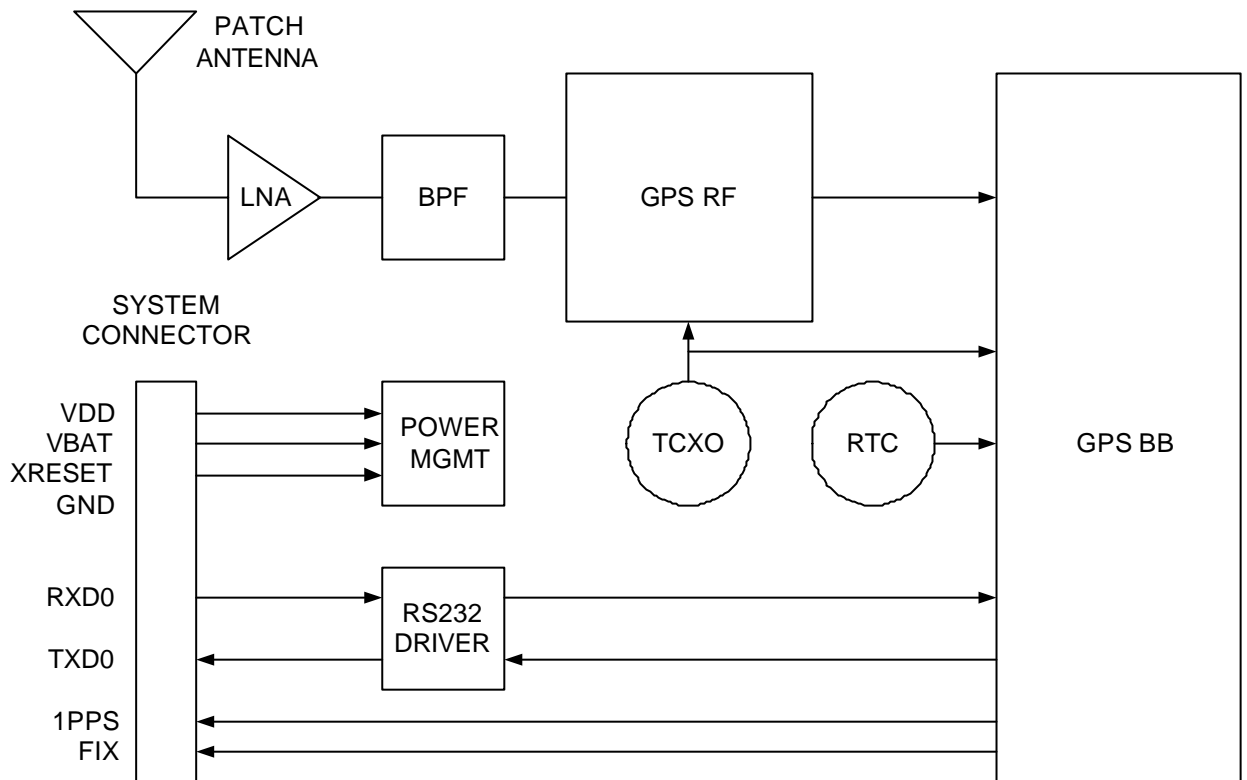
Figure 1   Block diagram of uPatch100 GPS receiver

1.6   Pictures of uPatch100
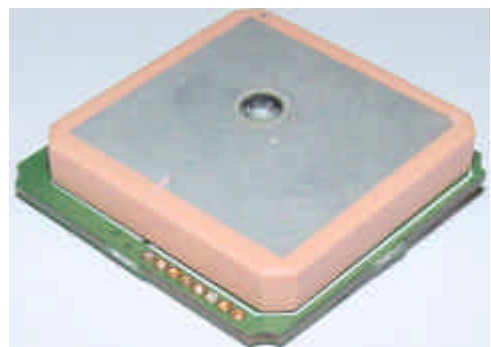
1.7 2D versus 3D positioning

The uPatch100 calculates a 2D fix whenever possible using 3 satellites and a 3D fix using 4 or more satellites. The following DOP limitations apply:

- PDOP <= 8

- HDOP <= 6

Case of 3 satellites

A 2D fix is calculated if the HDOP is <= 6. If HDOP is greater than 6 then a valid fix is not calculated. The following table shows the valid fix mode in case of 3 satellites:

| DOP limits	2D fix w/ 3 satellites
HDOP <= 6	YES
HDOP > 6	NO

Case of 4 or more satellites

A 3D fix is calculated if PDOP is <= 8. If PDOP is greater than 8 then the receiver tries to calculate a 2D fix if HDOP is <=6. If both PDOP > 8 and HDOP > 6 then a 2D fix is not possible.

The following table shows the valid fix mode in case of 4 or more satellites.

DOP limits	2D fix w/ 4 or more satellites	3D fix w/ 4 or more satellites
PDOP <= 8	Not Applicable	YES
PDOP > 8 HDOP <= 6	YES	NO
PDOP > 8 HDOP > 6	NO	NO

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2. MECHANICAL DIMENSIONS
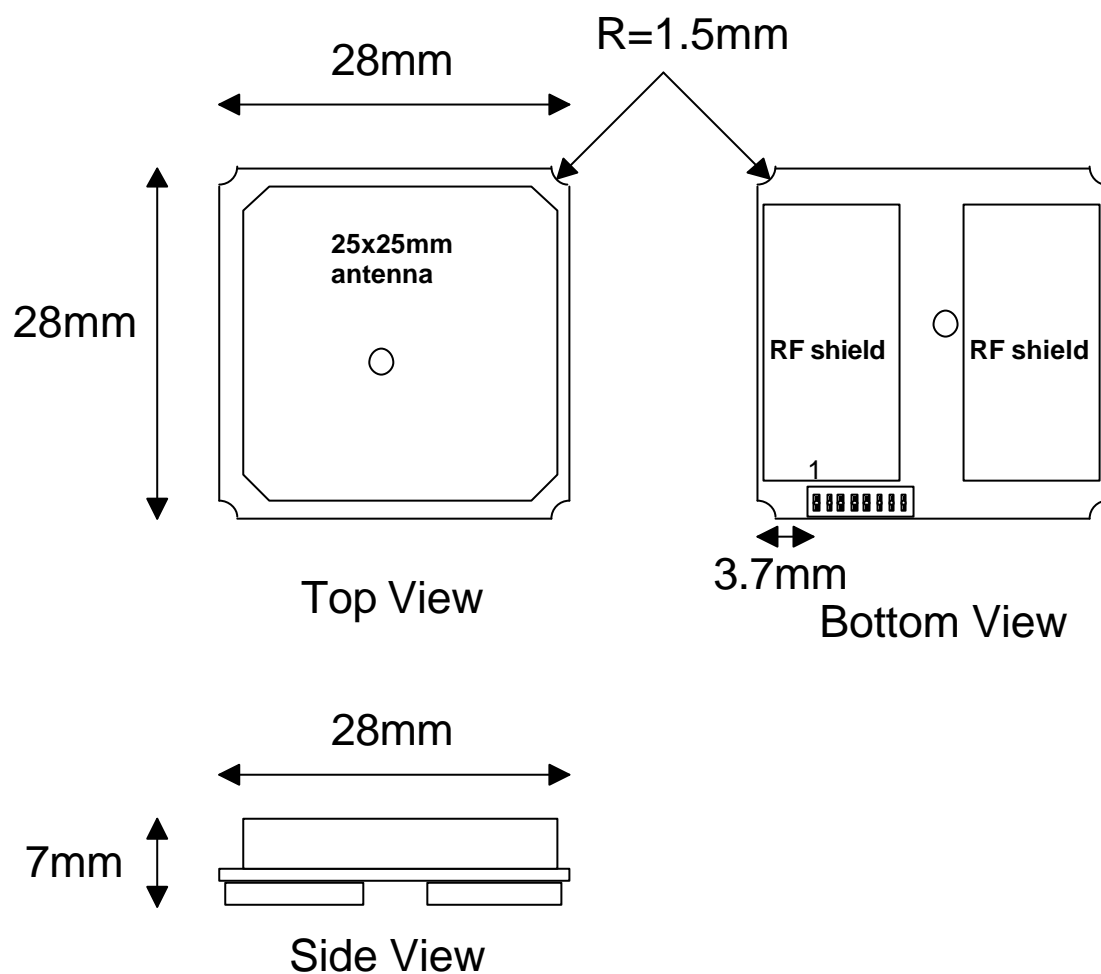
Figure 2 uPatch100 mechanical outlines

3.   EXTERNAL INTERFACES

3.1   System connector

The system connector consists of an 8-pin, through plated, I/O-row on the edge of the uPatch100 module. The user can either solder e.g a Flex-strip cable by hand or use an 8-pin connector. The I/O pad pitch is 1.27 mm.

The following signals are available in the system connector:

Pin	Signal Name	In/Out	Description
1	VDD	Power	+3.3V…+5.5V Main power supply
2	TXD0	Out	UART Port 0, Transmit Data, RS232 or CMOS level 1)
3	RXD0	In	UART Port 0, Receive Data, RS232 or CMOS level 1)
4	GND	Ground	Power and Signal ground
5	XRESET	In	Not connected, Reserved for future use
6	VBAT	Power	+3.3V…+5.5V Battery Backup Power supply
7	1PPS	Out	1 Pulse Per Second Output, CMOS level 2)
8	GPIO9	Out	Satellite Fix indicator output, CMOS level 2)

1) Note that the serial port interface is selectable between RS232 or CMOS levels depending on model.

2) CMOS levels are 3.0V

3.2   UART interface

One asynchronous UART ports is available for serial interfacing. The data format is : xxxx,N,8,1, i.e. 4800/9600 baud, no parity, eight data bits and 1 stop bit (baud rate is selectable with BoM option). No other data formats are supported. LSB is sent first. RS232 or CMOS signal levels are used (depending on BoM option).

Start	D0	D1	D2	D3	D4	D5	D6	D7	Stop

Parity: N
Data Bits: 8
Stop bits: 1

Figure 3   UART Data format (3.0V CMOS levels).

The UART port is named PORT0. PORT0 is used for NMEA 0183 output (TXD0) and system command input (RXD0) in normal operation.
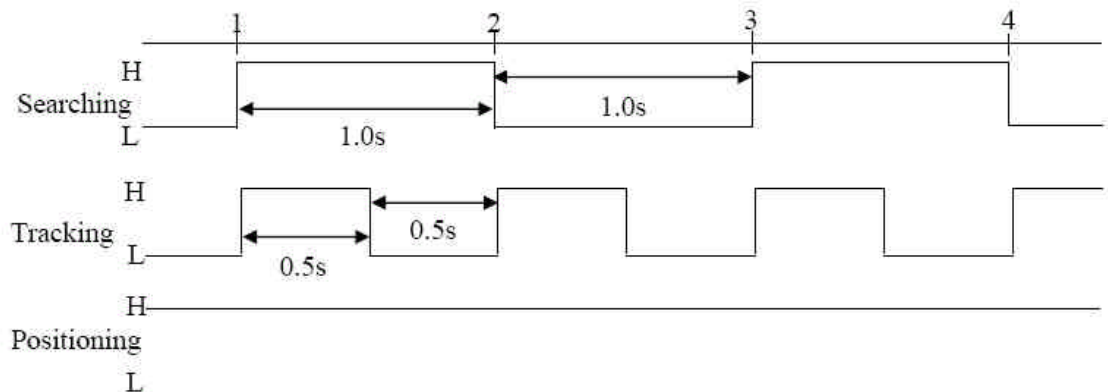
3.3 GPIO9 Output (Valid Fix Indicator Output)

GPIO9 output is dedicated for valid fix indication. See timing diagram below for different modes.

During signal acquisition phase the GPIO9 toggles with a 0.5Hz duty cycle (i.e. 1 second high, 1 second low)

During signal tracking phase (Navigation message decoded from at least one satellite) the GPIO9 toggles with a 1Hz duty cycle (i.e. 0.5 second high, 0.5 second low).

A valid fix is indicated with a high level signal.

Figure 4   Valid fix indicator output in different modes.

Note that the current sourcing capability of GPIO9 is only 4mA. An external buffer is needed for driving e.g. a LED.

3.4 Power supply interfaces

There are two external power supply inputs available (VDD and VBAT).

VDD input is the main power supply input supplying the GPS receiver RF and baseband sections. On board regulators provides the internal supply voltages (1.8V and 3.0V). A internal Power-On-Reset (POR)

circuit is also available that monitors the VDD supply. The POR circuit provides an active low RESET (held 300ms low) signal to the baseband device once the VDD has reached proper voltage level.

VBAT input is dedicated for supplying the receiver in battery backup mode. On board regulators provides the internal battery backup supply voltages (1.8V and 3.0V).

In normal operation both power supplies (VDD and VBAT) should be supplied with a regulated +3.3V...+5.5V voltage.

For low power mode (battery backup mode) the VDD supply can be removed at any time. VBAT provides supply voltages to the battery backup sections of the receiver keeping the RTC running and the battery backed-up section of SRAM alive.
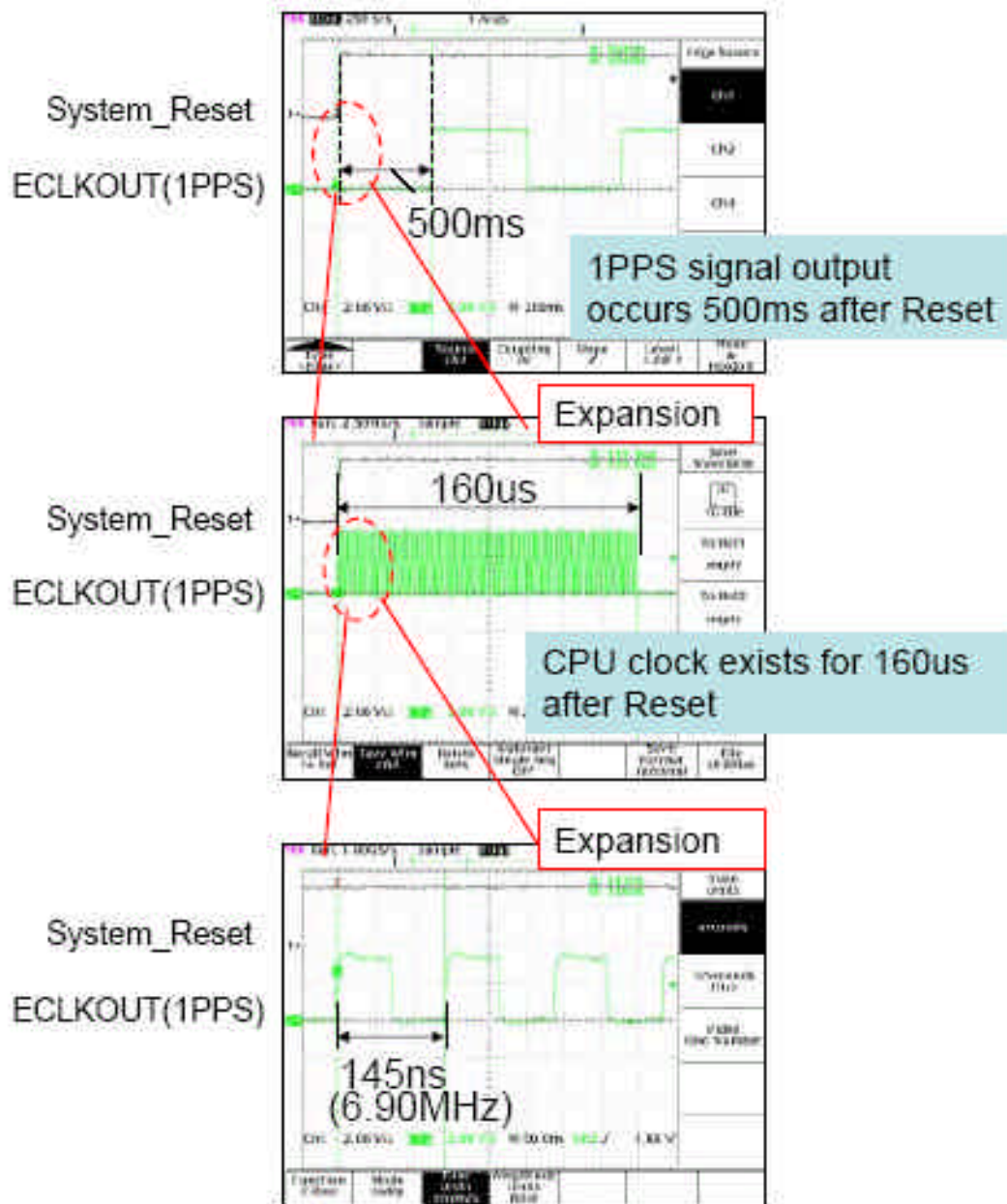

NOTE

The uPatch100 will not operate without the VBAT supply as it supplies power to the RTC section. See section 4 for details.

3.5   1PPS Output

The 1PPS output provides a timing pulse synchronized to GPS time once a valid fix is available.

The figure below shows the behaviour of 1PPS output signal after Power On Reset. For a period of 160us after RESET the 1PPS signal outputs the system clock frequency / 3. 500ms after RESET the actual 1PPS signal is activated.

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Figure 5   1PPS signal output after RESET

4. APPLICATION NOTE FOR POWER SUPPLIES

The uPatch100 has two separate power supply inputs; VDD and VBAT. In normal operating mode power is supplied to both of them. Note that VBAT must be powered in order to keep the RTC running and the receiver in operation.

There are however customer cases where to separate supplies are not available. The following sections shows different power supply possibilities.

4.1 Separate VDD and VBAT supplies available

The best performance combined with low power operating modes are achieved with two separately controlled power supplies; one for VDD and one for VBAT. It is also the most cost efficient solution.

In this mode VDD can be turned off anytime and the receiver then enters sleep mode leaving the RTC and some portion of the internal SRAM powered from VBAT. When VDD is turned on the receiver resumes normal operation and if the ephemerides are still valid it performs a Hot Start. If the ephemerides are old it performs a Warm Start.

If both VDD and VBAT are removed all data is lost and the receiver performs a Cold Start once powered up again. Note that the receiver cannot operate without VBAT.

Min. +3.3V ———————▶ VDD

uPATCH100

Min. +3.3V ———————▶ VBAT
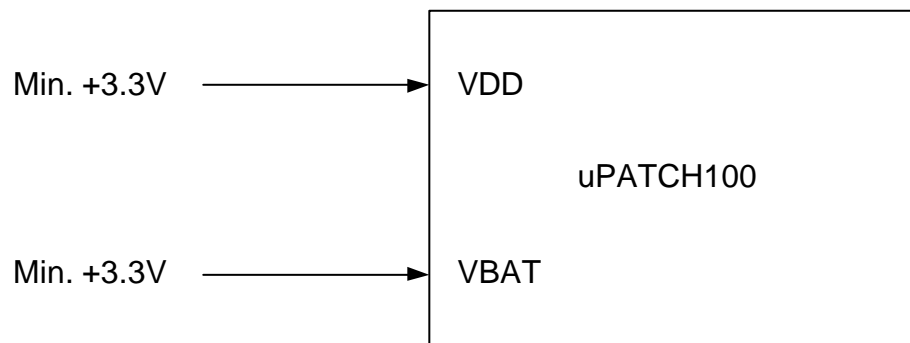
**Figure 6** uPatch100 powered with two separate supplies.

4.2 Single supply available

If only one supply is available then it should be connected to both VDD and VBAT. In this way no low power modes can be achieved as

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the receiver is continuously running. The following figure show the connection.

When the power supply is removed all information is lost (Time, Last Known Good Position, Satellite Ephemerides etc.). Once powered up again the receiver performs a Cold Start.

Note that VBAT must also be connected in order for the receiver RTC operational.
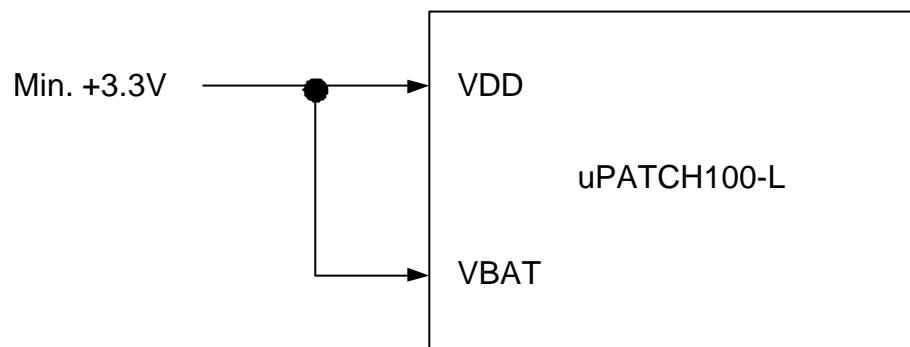
Figure 7   uPatch100 powered with one single external supply.

4.3   Single supply using Super Cap for VBAT

An external high capacity capacitor can also be used for VBAT supply if only one power supply is available. The recommended circuitry is shown in the figure below. The diode should be of Schottky type with a very low drop-out voltage (typically 150mV). The capacitor can be e.g. a 1F 5.5V.

In this way the VDD can be removed at any time. The receiver operates in the same mode as described in section 4.1.

Min. +3.3V   VDD

Schottky Diode

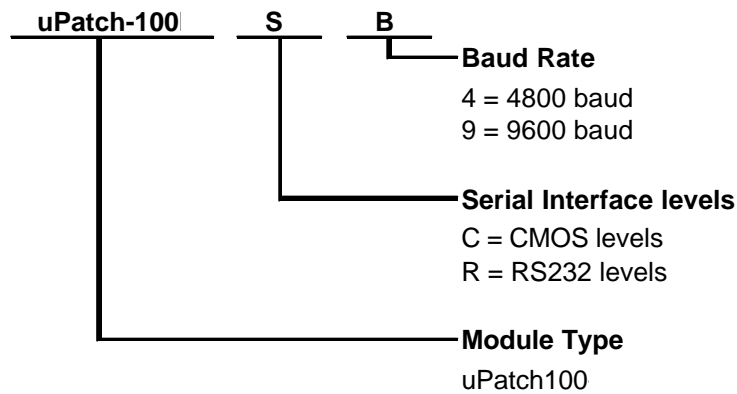uPATCH100-L

VBAT
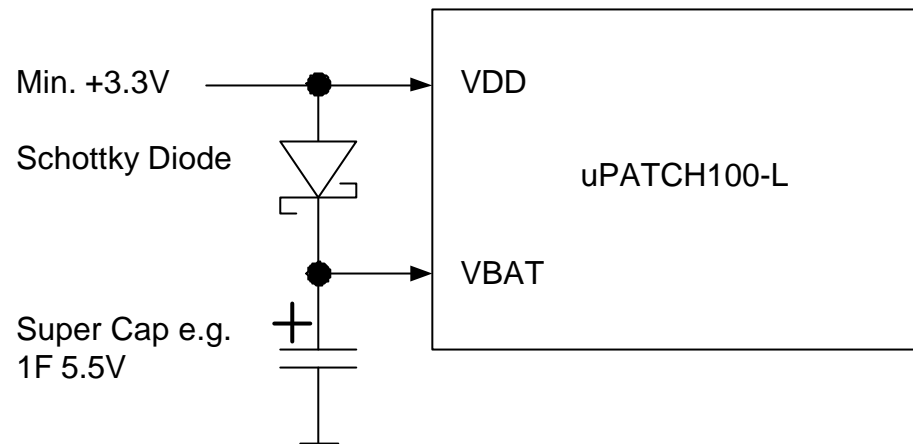
Super Cap e.g.
1F 5.5V

Figure 8   uPatch100 with single supply and Super Cap

5. ORDERING INFORMATION

The uPatch100 can be factory configured for either 4800 baud or 9600 baud serial interface speed. It can also be factory configured for either CMOS or RS232 signal levels for the serial interface.

uPatch-100   S   B

Baud Rate
4 = 4800 baud
9 = 9600 baud

Serial Interface levels
C = CMOS levels
R = RS232 levels

Module Type
uPatch100

Please contact Fastrax Sales for availability and lead-time issues.

Valid combinations are:

uPatch100-R4	RS232 levels @ 4800 baud
uPatch100-R9	RS232 levels @ 9600 baud
uPatch100-C4	CMOS levels @ 4800 baud
uPatch100-C9	CMOS levels @ 9600 baud

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