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Control of Power Electronic Converters in Distributed Power Generation Systems

Evaluation of Current Control Structures for Voltage Source Converters operating under Weak Grid Conditions

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Master of Science in Energy and Environment

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Problem Description

The use of power electronic converters is continuously increasing, and especially the Voltage Source Converter topology is gaining widespread use as a modular topology for many different power system applications. Understanding the limits of stable control and operation for this converter topology is therefore important for interfacing renewable energy sources like wind power and photovoltaic power to the grid. The control performance for such converters is depending on the strategy for synchronization to the grid and is limited by the speed of the inner control loops. For traditional cascaded control systems, this means that the dynamics of the inner loop current controllers and of the grid voltage phase detection is of major importance to the limits for stable operation.

On this background, the objective of this study should be to investigate the dynamic performance and the influence of the inner current control loops on the stability of a Voltage Source Converter operating in a weak grid. The interaction with the synchronization method and the influence of the outer loop controllers should also be investigated from the starting point of the current controllers. The study can be divided into two main parts:

1. Investigation and comparison of the dynamic performance of different current control structures when a converter is operated in a weak grid. This first part of the study should assume balanced grid conditions, and can be based on previous work of the student in the Specialization course project. The operation and stability limits of the converter with the different current control strategies should be investigated by simulation when exposed to changes in active and reactive current references and disturbances in the grid voltage.
2. As a second step, strategies for synchronization to an unbalanced grid voltage should be implemented in the simulation models, and the investigated current control structures should be adapted for control of positive and negative sequence current components. The same investigations of operational characteristics and stability limits as described for balanced conditions should be systematically carried out with control structures adapted for operation under unbalanced grid voltages.

The simulation models should be implemented in the PSCAD/EMTDC simulation software and the description of the models should be supported by theoretical explanations and references to scientific literature. Relevant findings and observations should be illustrated by simulation results and explained with respect to the theoretical and mathematical background.

Assignment given: 09. February 2010
Supervisor: Tore Marvin Undeland, ELKRAFT

Preface

Throughout the work with the master thesis, I have learned a lot. By doing theoretical background studies and then testing my computations by simulations. The study of the simulations has been a good way of understanding the nature of the electrical circuits and controller theory.

During my work with this master thesis there are a number of people I will like to address a great thank to, and who has been of mayor importance for me and my work. First of all I would like to thank Jon Are Suul for always taking the time to help me. He has been irreplaceable in solving my problems with the simulations program PSCAD, guiding me to helpful literature and giving me the inspiration to complete the master thesis. In addition he has been a great contributor for my first academic publication, which gave me the opportunity to travel all the way to China and participate in the IEEE 2nd international Symposium on Power Electronics for Distributed Generation System. Here I will also like to thank the department of Electric Power Engineering at NTNU and Statnett for the contribution that made it possible to participate in the conference.

I would also like to thank my supervisor Prof. Tore Undeland for his enthusiasm, ideas and inspiration and for being so understanding. He has always been quick to respond my emails, even on late Sunday evenings.

At last I would like to thank all the people who have helped me in the finishing of my thesis, both directly by reading and correcting, and for the social contribution during my work. Especially I would like to thank Øyvind Rui, Marie Midtsund, Johanna Roaldset and Martin Fløystad for both critical feedbacks on my work and by moral support during the last weeks, either over the phone or phase to phase.

Tarjei Midtsund

Trondheim, july 2010

Summary

The performance of different current controller structures for Voltage Source Converters (VSC) under weak grid conditions caused by large grid impedance is investigated. The VSC is synchronized to the grid by a Phase Locked Loop (PLL). Current control techniques and PLL techniques for handling both symmetrical and asymmetrical conditions are presented and discussed. The investigated current control structures are; the conventional Proportional Integral (PI)-controller in the synchronous rotating reference frame, dual PI-controllers implemented in positive- and negative-sequence rotating reference frame, the Proportional Resonant (PR)-controller in the stationary reference frame, the phase current hysteresis controller, and a space vector base hysteresis controller in the synchronous rotating reference frame. The PLL-techniques used for synchronization are; a conventional synchronous rotating reference frame PLL, a PLL with notch filter, and a Decoupled Double Synchronous Reference frame PLL (DDSRF-PLL).

The different current control strategies and PLL-techniques are studied by simulations. The results show how large grid impedance can influence the dynamic response of the system and how the interaction between the PLLs, the current controllers and the large grid inductance can even trigger instability when the voltage measurements are highly influenced by the operation of the converter. The PI-controllers in the synchronous rotating reference frames are particularly sensitive to oscillations that can be reinforced when the measured voltage feed-forward terms are used in the control system. The response of the PR-controller is instead slowed down by the interaction with the PLL, while both the hysteresis controllers are quickly tracking the reference value as long as the interaction with the PLL is not leading to instability.

Operation under asymmetrical weak grid conditions are investigated for current controllers that exploit PLL techniques designed to remove the oscillations that occur in the positive sequence reference frame voltage during unbalanced

grid voltage. The simulations show that the DDSRF-PLL has a shorter transient period than the PLL with notch filter, but with a small steady state 100 Hz oscillation under the weak asymmetrical grid conditions.

The results indicate that the tuning of the PLL is of large importance for the stability of the control system, and that a slower PLL can lead to less interaction with the current controllers at the cost of a slower and less accurate dynamic overall control performance.

Sammendrag

Det er undersøkt ulike metoder for strømregulering av en spenningskildeomformer og hvordan disse oppfører seg i et svakt nett, forårsaket av en høy nettimpedans. Spenningskildeomformeren synkroniseres til nettet ved hjelp av en faselåst sløyfe (PLL). Strømregulerings- og PLL- metoder for å håndtere både symmetriske og asymmetriske forhold i nettet er presentert, undersøkt og diskutert. De undersøkte strømregulatorene er: En konvensjonell proporsjonal integrator (PI)-regulator i det synkront roterende referansesystemet, to doble PI-regulatorer implementer i positivt og negativt roterende referansesystem, proporsjonal resonans (PR)-regulator i stasjonært referansesystem, fasestrøm hysterese regulator i stasjonært referansesytem og en spenningsvektorbasert hystereseregulator i synkront roterende referansesystem. PLL-metoden som er brukt for å synkronisere spenningskildeomformeren til nettet er: en konvensjonell synkront roterende referansesystem PLL, en PLL med notch-filter, og en PLL som kobler ut innvirkning mellom positiv og negativ sekvens (DDSRF-PLL).

De ulike strømreguleringsstrategiene og PLL-metodene har blitt studert ved hjelp av simuleringer. Resultatene viser hvordan en høy nettimpedans påvirker systemets dynamiske respons og hvordan interaksjonen mellom PLL, strømregulatorene og en stor nettimpedans fører til ustabilitet når de målte spenningene er sterkt påvirket av driften til omformeren. PI-regulatorene i de roterende referansesystemene er spesielt følsomme for oscillasjonene som vil bli forsterket når reguleringsstrukturene benytter foroverkopling av de målte spenningene. Responsen til PR-regulatoren blir derimot moderert av interaksjonen med den faselåste sløyfen, og hystereseregulatorene følger referansen raskt så lenge interaksjonen med den faselåste sløyfen ikke fører til ustabilitet.

Driften under asymmetriske forhold i et svakt nett er undersøkt for reguleringssystemene som benytter PLL-metoder som er designet til å fjerne oscillasjonene som oppstår i positiv sekvens referansesystem ved ubalansert nettspen-

ning. Simuleringene viser at reguleringssystemene med en DDSRF-PLL har en kortere transient periode enn reguleringssystemet med notch-filter-PLL, men med en liten 100 Hz oscillasjon i stasjonær tilstand i et asymmetrisk svakt nett.

Resultatene indikerer videre at innstillingen til PLL-parametrene spiller en viktig rolle for stabiliteten til reguleringssystemet, og at en tregere PLL kan føre til en mer dempet interaksjon med strømregulatorene på bekostning av et tregere og mindre dynamisk nøyaktig reguleringssystem.

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List of Parameters

Table 1: Subscript and superscipt used in the text

Parameter	*Explanation*
d	Real axis of the Park Transformation
q	Imaginary axis of the Park Transformation
abc	Phases of a three-phase system
pu	pu value
g	Value at the grid
$conv$	Value at the converter
b	Base value
α	Real axis of the Clark transformation
β	Imgainary axis of the Clark transformation
LL	Line to line value
up	Upper value of the band limit
low	Lower value of the band limit
RMS	Root mean square value
ref	Reference value
$+$	Positive Sequence components
$-$	Negative Sequence components
0	Zero Sequence components

Table 2: Parameters used in the text

Parameter	*Explanation*
V_n	Nominal voltage
I_n	Nominal current
S_n	Nominal Power
X	Electric Quantity
φ	Angle between voltage and current
θ	Voltage space vector angle
L	Inductance
R	AC side Resistance
L_g	Grid Inductance
R_g	Grid side Resistance
C_f	Filter capacitance
i	AC side current
V_{DC}	DC bus voltage
f_{sw}	Switching frequency
ω_b	Base angular frequency
τ_i	Regulator Parameter
T_a	VSC time constant
$T_{f,PLL}$	Time constant of PLL filter
K_p	Regulator Parameter
K_i	Regulator Parameter
K_{pv}	Regulator Parameter
T_{iv}	Regulator Parameter
f_n	Nominal frequency
f_{res}	Resonance frequency
T_α	Active damping time constant
v	AC side voltage
A_{low}	Hysteresis band limit
B_{low}	Hysteresis band limit
i	Converter side current
i_o	Grid side current
v_c	Filter capacitor voltage
ω	Angular frequency
M_p	Maximum overshoot
t_p	Instant of maximum overshoot
t_s	Settling time
P	Active Power
Q	Reactive Power

Abrivation

Table 3: Abrivation used in the text

Parameter	*Explanation*
VSC	Voltage source converter
PWM	Pulse width modulator
PLL	Phase locked loop
PI	Proportional integrator
PR	Proportional resonant
SRF	Synchronous Reference Frame
DDSRF	Decoupled Dual Synchronous Reference Frame
IGBT	Insulated-gate bipolar transistor
ASF	Average switching frequency
VCO	Voltage controlled oscillator

Chapter 1

Introduction

Nowadays, there is a common understanding that the global warming is human made, with the energy sector as the main contributor to the green house gas emissions. In Europe, the energy sector alone contributes with 80% of the green house gas emissions [14]. The demand for energy worldwide is at the same time continuously increasing. This has led to a significant attention towards alternative energy resources, and the amount of renewable energy integrated into the power system has grown rapidly during the last years.

Due to the stochastic behavior of the input power from many of the new renewable energy sources and the large intervention of the renewable systems, the implementation of them will have an impact on the operation of the power system. Hence, more stringent grid connection is required. The use of power electronic equipment has then become an essential part for the utilization of the renewable energy generation systems. Especially the Voltage Source Converter (VSC) topology is becoming a standard modular solution due to its capability for reversible flow, DC-voltage control and the implementation of high performance control system [9].

Although many different control structures have been developed for VSC's in various application, the VSC for grid connection is often current controlled. The current controller as the inner control loop of a cascaded control system appears to be the most commonly used control structure [11]. With current control as the inner control loop, the overall operation will depend on the performance of the current controllers. This has led to significant attention in literature towards development and evaluation of different control structures for the VSC.

The control system should be designed for stable operation under every

grid condition, but weak grid conditions, caused by a high value of the grid impedance is one issue that can challenge the control of the VSC. There has so far been given little attention towards control and operation of a VSC in connection with a weak grid, while taking into account the dynamics of the inner current control loop and the interaction between the converter and the grid impedance [25][10].

Remote faults in distribute power systems results in voltage dips through the power system [26]. In areas with high share of decentralized distributed generation, there is grid code requirements for generator "ride-through" where the generator is imposed to stay connected during transient faults. Both balanced and unbalanced changes in the voltage may occur, and affect the operation of the converter in different ways. Hence the current control of the VSC should be able to handle operation under both balanced and unbalanced conditions.

The motivation of this thesis is therefore to investigate, compare and evaluate different current control strategies when a VSC is connected to a weak point in the power system under various grid conditions. The following current control strategies will be presented in investigated: 1) The Decoupled Proportional Integrator (PI) controller in the synchronous rotating reference frame. 2) Two dual PI controller implemented in the separated positive- and negative- sequence rotating reference frame, 3) The PR controller in the stationary reference frame, 4) The two level independent phase current hysteresis controller, and 5) The three level hysteresis controller in the synchronous rotating reference frame.

In addition, the capability of handling both symmetrical and asymmetrical conditions leads the attention towards three different strategies for grid synchronization. 1) A conventional synchronous rotating reference frame Phase Locked Loop (SRF-PLL), designed to handle symmetrical grid conditions, 2) a synchronous rotating reference frame SRF-PLL with notch filter, to filter out the oscillations that occurs during asymmetrical conditions, and 3) a Decoupled Double Synchronous Reference frame-PLL (DDSRF-PLL) that decouples the components of the positive and negative rotating reference frames.

To evaluate and compare the dynamic response and the stability limits for the different current control structures and their respective grid synchronization techniques, simulation studies with the PSCAD/EMTDC simulation software have been carried out. The response to step changes in current reference, operation under various weak grid conditions, and the limits of stable operation of the converter have been investigated by the simulations.

In lack of simple mathematical models with general validity under weak grid conditions, a state space model of the system with a PI controller and a conventional PLL has been tried indentified. This has not been completely fulfilled

and the obtained results are analyzed with reference to physical considerations based on the electrical circuit and on traditional control theory.

Large part of the theoretical background information used in this master thesis is based on the background study preformed in the specialization project. To achieve complete substance of this thesis, the background study in the specialization project that is required to understand the work presented here is repeated.

Chapter 2

Background and Theory

2.1 Three Phase Systems

A symmetrical three phase voltage source can be represented by three voltage vectors with the same length and the phase shifted with 120° with respect to each other, as described in Equation 2.1[2]. The three phases are named *abc* in this thesis.

$$\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = \begin{bmatrix} V\cos(\omega t) \\ V\cos(\omega t - \frac{2\pi}{3}) \\ V\cos(\omega t + \frac{2\pi}{3}) \end{bmatrix} \tag{2.1}$$

If the symmetrical system is connected with a common isolated neutral the currents and the voltage for the three phase system fulfills the conditions of Equation 2.2.

$$\begin{aligned} i_a + i_b + i_c &= 0 \\ v_a + v_b + v_c &= 0 \end{aligned} \tag{2.2}$$

The Thevenin equivalent

A power system can be large and complex with several nodes that connects a number of lines with transformers and generators or loads. During calculation of the performance of one particular node without doing a full scale analysis of the entire network, the network can be represented with its thevenin equivalent

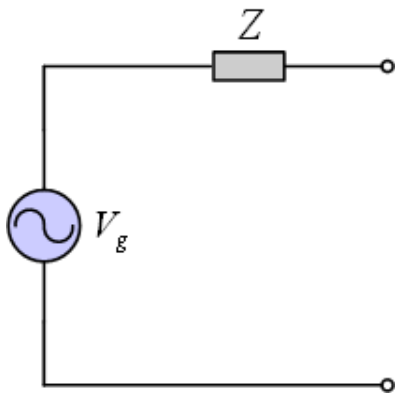


Figure 2.1: The grid Thevenin equivalent

[23]. This thevenin equivalent is shown in Figure 2.1 and the calculation of Z can be found by the fault level S_k at the node by Equation 2.3 [23].

$$|Z| = \frac{V^2}{S_k} \tag{2.3}$$

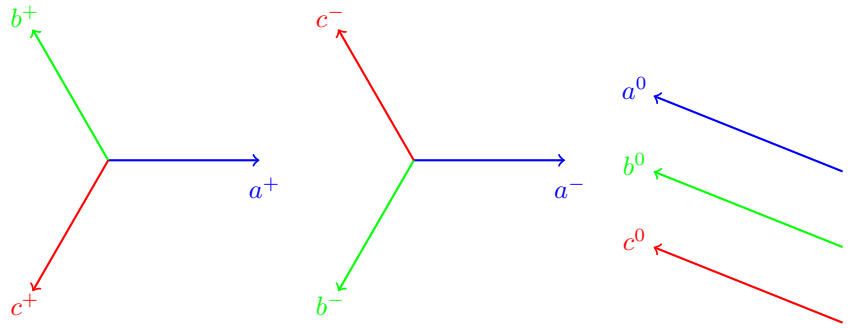
Where S_k is calculated from short circuit analysis of the power system and V is the nominal line-to-line voltage at the node. The thevenin equivalent voltage V_g can be taken as the nominal voltage at the point of interest. The fault level can now be expressed by the X/R ratio in $Z = R + jX$. The fault level is an important parameter, not only during fault conditions, but it is also predicting the performances during normal operation, as it defines the strength of the of the network at the particular point. A weak grid is a network or a part of a network where the fault level is low, that is if Z is high, and indicates that the node voltage is fragile with respect to changes in active and reactive power flow at the node.

2.1.1 Symmetrical Components - The positive-, negative- and zero-sequence

Ideally, the voltages and the currents will be perfectly balanced and symmetrical, which leads to greatly simplified analysis. However, this is not always the case. To analyze the three phase system under unbalanced conditions, the

system can be decomposed by use of symmetrical components which mathematically breaks an unbalanced systems into three balanced sequences. A positive-, negative- and zero-sequence. The theory of symmetrical components comes from a paper written by Fortescue in 1918 [6]. The paper demonstrate that N set of unbalanced phasors could be expressed as the sum of N symmetrical sets of balanced phasors. The unsymmetrical voltage and currents are found by superposition of the three sequences. The voltage can be written as in Equation 2.4 and the phasors of the three phases in the positive- negative- and zero-sequence, with superscript respectively $+$, $-$ and 0, are shown in Figure 2.2a-2.2c.

$$\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = \begin{bmatrix} V_a^- \\ V_b^- \\ V_c^- \end{bmatrix} + \begin{bmatrix} V_a^- \\ V_b^- \\ V_c^- \end{bmatrix} + \begin{bmatrix} V_a^0 \\ V_b^0 \\ V_c^0 \end{bmatrix} \tag{2.4}$$



(a) Positive sequence (b) Negative Sequence (c) Zero sequence

Figure 2.2: Symmetrical components

The steady state vector representation in Figure 2.2a-2.2c, has been derived in [1]and can be written as in Equation 2.5 and becomes as in Equation 2.6 in the time domain [33]. A zero sequence current may be present when there is a path in addition to the three lines, f.ex earth [34].

$$\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 \\ 1 & h & h^2 \\ 1 & h^2 & h \end{bmatrix} \begin{bmatrix} V_a^+ \\ V_a^- \\ V_a^0 \end{bmatrix} \tag{2.5}$$

Where $h = e^{j\frac{2\pi}{3}}$

$$\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = \begin{bmatrix} V^+\cos(\omega t) \\ V^+\cos(\omega t - \frac{2\pi}{3}) \\ V^+\cos(\omega t + \frac{2\pi}{3}) \end{bmatrix} + \begin{bmatrix} V^-\cos(-\omega t + \phi^-) \\ V^-\cos(-\omega t - \frac{2\pi}{3} + \phi^-) \\ V^-\cos(-\omega t + \frac{2\pi}{3} + \phi^-) \end{bmatrix} + \begin{bmatrix} V^0\cos(\omega t + \phi^0) \\ V^0\cos(\omega t + \phi^0) \\ V^0\cos(\omega t + \phi^0) \end{bmatrix} \tag{2.6}$$

Figure 2.3 shows an system that is exposed to an unbalance at a certain instant. The negative- and the zero-sequence are initially set to zero. At the moment the unbalance occurs, the amplitude of the positive sequence voltage is set equal to 0.7 and the amplitude of the negative sequence is set equal to -0.3. The zero sequence is unchanged, equal to zero. As seen from the figure, the unsymmetrical and unbalanced system is decomposed into two symmetrical and balanced systems.

2.1.2 $\alpha\beta$-transformation

The three phases, both voltage and current, can be represented in a two phase representation. The momentarily value of the three phases can be transformed into a voltage vector or a current vector. This vector can then be represented in a orthogonal stationary $\alpha\beta$-reference as shown in Figure 2.4. The transformation from the abc reference to the $\alpha\beta$-reference is shown in Equation 2.7.

$$\begin{bmatrix} X_\alpha \\ X_\beta \\ X_\gamma \end{bmatrix} = \frac{2}{3}\begin{bmatrix} \cos(0) & \cos(\frac{2\pi}{3}) & \cos(-\frac{2\pi}{3}) \\ \sin(0) & \sin(\frac{2\pi}{3}) & \sin(-\frac{2\pi}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix}\begin{bmatrix} X_a \\ X_b \\ X_c \end{bmatrix} \tag{2.7}$$

Introducing the positive- and the negative- sequence and ignoring the zero sequence component, the voltage transformed into in the $\alpha\beta$-reference frame is given by Equation 2.8.

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = V^+\begin{bmatrix} \cos(\omega t) \\ \sin(\omega t) \end{bmatrix} + V^-\begin{bmatrix} \cos(-\omega t + \phi^-) \\ \sin(-\omega t + \phi^-) \end{bmatrix} \tag{2.8}$$

The positive sequence voltage is supposed as the phase origin. The voltage vector consists of two sub vectors. One rotating in the positive direction and one rotating in the negative direction. Nor the magnitude or the rotational frequency of the voltage vector for an unbalanced system is constant [33].

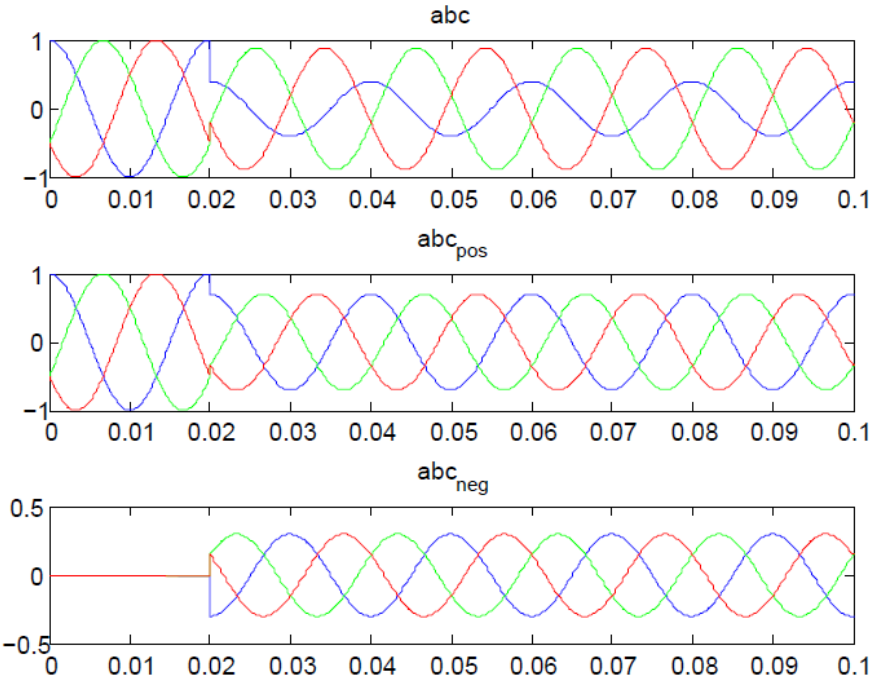


Figure 2.3: Positive and negative sequence in an unbalanced system

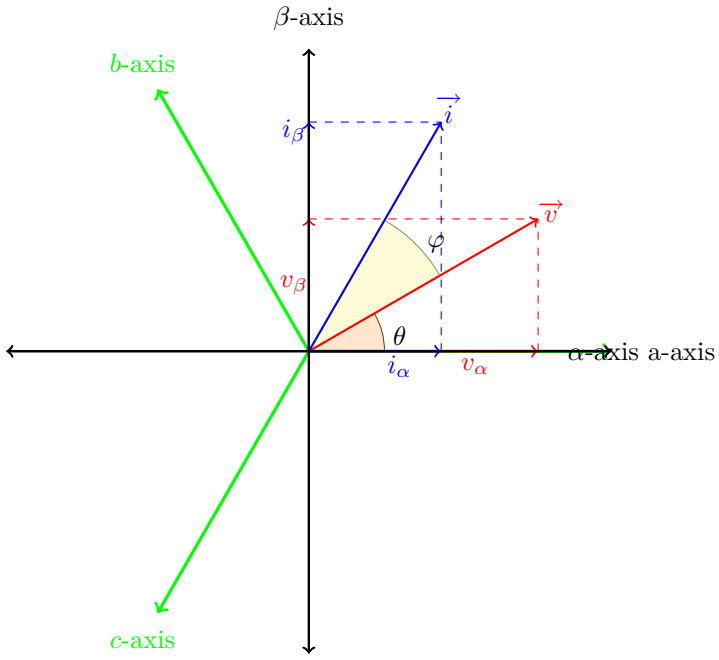


Figure 2.4: Voltage and current vector in $\alpha\beta$-coordinates.

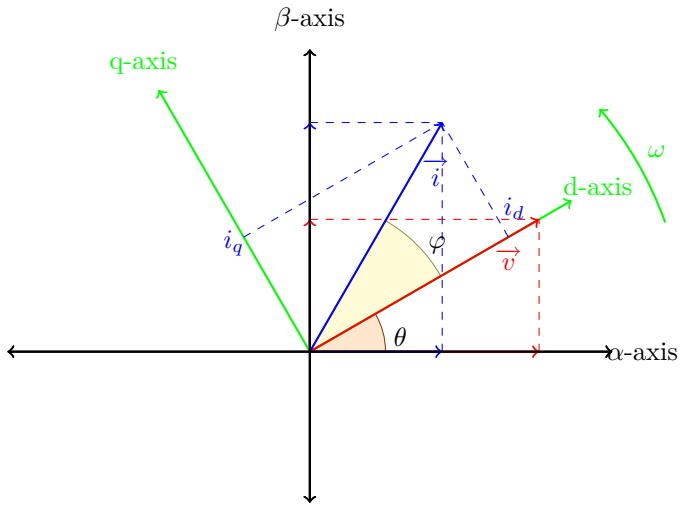


Figure 2.5: Voltage and current vector in dq-coordinates.

2.1.3 dq-transformation

The voltage and current vectors can be represented in any coordinate system. The synchronous rotating reference (SRF)-dq coordinate system is rotating in the same angular speed as the voltage vector. Since the voltage vector and the coordinate system are aligned, the electrical components in this system behaves like DC components. This gives some obvious benefits in control manners. The transformation from $\alpha\beta$-reference to dq-reference is shown in Equation 2.9 and in Figure 2.5 :

$$\begin{bmatrix} X_d \\ X_q \end{bmatrix} = \begin{bmatrix} \cos(\theta) & \sin(\theta) \\ -\sin(\theta) & \cos(\theta) \end{bmatrix} \begin{bmatrix} X_\alpha \\ X_\beta \end{bmatrix} \tag{2.9}$$

Since the voltage vector for the park transformation is aligned with the d-axis, the q component of the voltage vector is zero. The active and reactive power is then reduced to the control of i_d and i_q as shown in Equation 2.10.

$$\begin{aligned} p &= \frac{3}{2} v_d i_d \\ q &= -\frac{3}{2} v_d i_q \end{aligned} \tag{2.10}$$

2.2 pu-transformation

The pu-system is a good and well spread analyzing tool. Since the values are not directly dependent for their ratings, it is useful for comparing different designs of electrical systems. There are different ways of designing the pu-system. For this thesis the base values are chosen to fit with a amplitude invariant park transformation.

$$\begin{aligned} V_{s,b} = V_{d,b} = V_{q,b} = \hat{V}_{abc,n} = \frac{\sqrt{2}}{\sqrt{3}} V_n \\ V_{DC,b} = 2V_{s,b} \qquad (2.11) \\ I_{s,b} = I_{d,b} = I_{q,b} = \hat{I}_{abc,n} = \sqrt{2} I_n \\ S_b = \sqrt{3} \cdot V_n I_n = \frac{3}{2} V_{s,b} I_{s,b} \qquad (2.12) \\ Z_b = \frac{V_{s,b}}{I_{s,b}} \\ \omega_b = 2\pi f \end{aligned}$$

$V_{s,b}$ is the nominal peak phase voltage at the ac side, S_b is the nominal three phase apparent power of the ac side and I_b is the nominal peak phase current. Using the definitions in Equation 2.11 gives the pu-values in Equation 2.13:

$$\begin{aligned} L_{pu} = \frac{\omega_b L}{Z_{base}} \\ C_{pu} = \omega_b C Z_{base} \\ R_{pu} = \frac{R}{Z_{base}} \qquad (2.13) \\ I_{pu} = \frac{I}{I_{base}} \\ V_{pu} = \frac{V}{V_{base}} \end{aligned}$$

2.3 The Voltage Source Converter (VSC)

There are different ways of converting and inverting voltage with power electronic devices. For distributed generation the state of the art is the two level three phase converter. For high power wind turbines a three-level neutral point clamped VSC is an option. Also matrix converters and multilevel converters

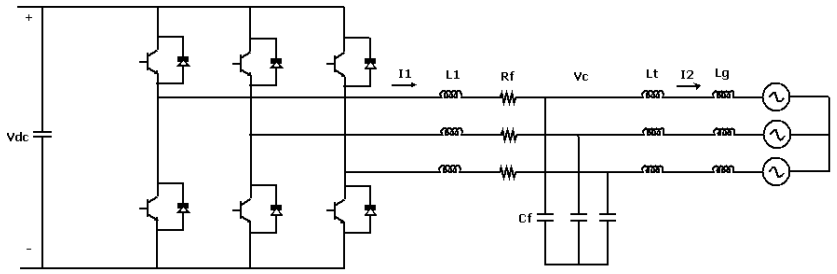


Figure 2.6: Two level - three phase voltage source converter

are developing and been implemented in distribution power generation systems [3]. This thesis will focus on the control of a three-phase two level VSC.

2.3.1 Two level - three phase converter

As seen in figure 2.6 the VSC contains shunted diodes and switches. The diodes are mandatory because bidirectional current flow has to be fulfilled by the semiconductor switches in the VSC. The switches, which usually are IGBTs, are turned on and off by a control trigger signal. Different strategies for triggering the switches are dependent on the control method. By use of a linear controller the switches are triggered by comparing three sinusoidal control signals, phase shifted 120° with respect to each other, with a saw tooth signal as shown in Figure 2.7. The sinusoidal signal has the same frequency as the 1st harmonic of the output voltage, and the saw tooth signal has the same frequency as the switching frequency. This method, called the sinus modulation, can be used when the switching frequency is at least 20 times the 1st harmonic frequency [30].

For nonlinear controllers the switching signals are determined by the choice of voltage vector. The different voltage vector representations are presented in Section 2.3.3. If the switches are seen as ideal and the blanking time of the switches are ignored, the output voltage of the converter is independent of the current, since the switches in one of the legs are always on.

To prevent the PWM from going in to over modulation and to attend a stabile system, the DC side of the voltage must be at least as in Equation 2.14[29]:

$$V_{DC} \geq \frac{2\sqrt{2}}{\sqrt{3}} V_{LL} \tag{2.14}$$

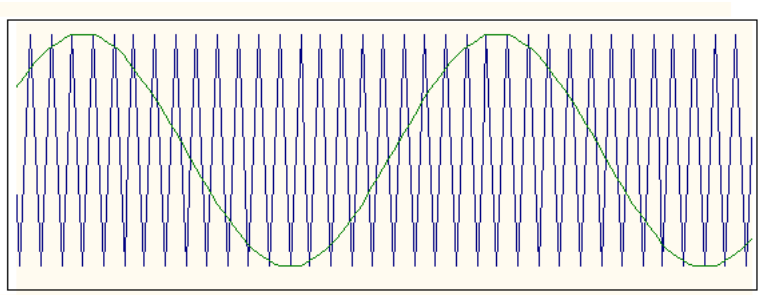


Figure 2.7: PWM in the VSC

2.3.2 3rd Harmonic injection

For operation of the voltage source converter, using a perfect sine wave as modulation reference, do not give the optimum use of the DC-side voltage of the converter for systems with isolated neutral. By decreasing the peak of the phase voltage, and maintaining the peak of the 1st harmonic, the use of the DC voltage can be increased. This can be achieved by injection of the 3rd harmonic, or every 3rd harmonic multiple, in the phase voltage. This harmonics will cancel out in the line-to-line voltage, since it is injected in all three phases. The use of the DC voltage will increase by a factor 1.155 ($\frac{\sqrt{3}}{2}$). From [13] the 3rd harmonic injection for optimal use of the DC-link voltage can be implemented at the modulation reference as:

$$V_a = \sin\omega t + \frac{1}{6}\sin 3\omega t \tag{2.15}$$

$$V_b = \sin(\omega t - \frac{2\pi}{3}) + \frac{1}{6}\sin 3(\omega t - \frac{2\pi}{3}) \tag{2.16}$$

$$V_c = \sin(\omega t - \frac{4\pi}{3}) + \frac{1}{6}\sin 3(\omega t - \frac{4\pi}{3}) \tag{2.17}$$

To maximize the use of the DC voltage, the PWM can also operate in the over modulation range. The line-to-line voltage will then not be a sine wave and contain a high harmonic distortion.

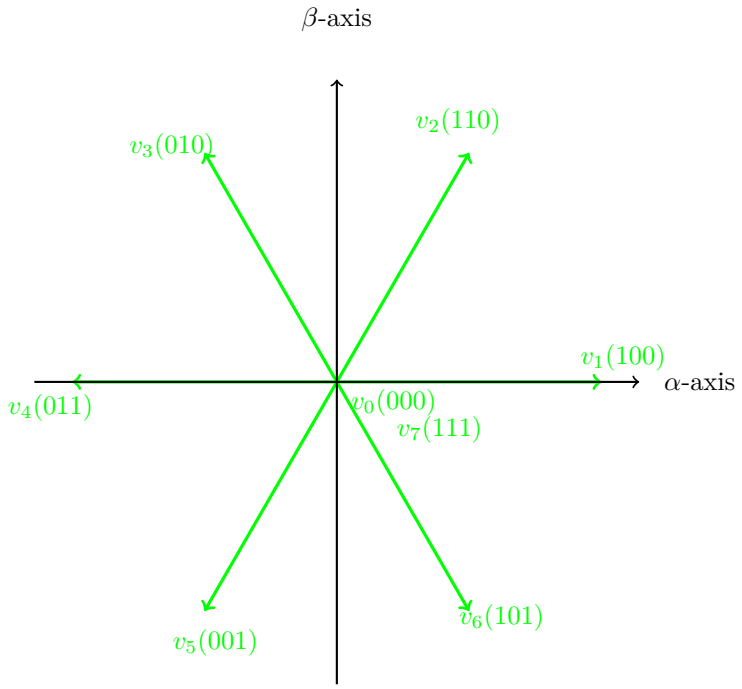


Figure 2.8: Switching States of the VSC voltage

2.3.3 Switching in the VSC

By use of different combinations of the switches in the converter the voltage vector can be represented by eight space vectors. Since the three phases are shifted 120 degrees with respect to each other, combination of the the six switches on the three legs and phases will give the the following voltage vector representations:

$$\overrightarrow{v_k} = \begin{cases} (\frac{2}{3})V_{DC}e^{j\pi(k-1)/3} & \text{for} \quad k = 1, ...6 \\ 0 & \text{for} \quad k = 0, 7 \end{cases} \tag{2.18}$$

This give six nonzero voltage vectors and two zero voltage vectors. Figure 2.8 shows the voltage vector in the $\alpha\beta$-reference frame.

2.3.4 LCL-filter

The high frequency harmonics in voltage and current, generated by the high frequency switching in the VSC, can be suppressed by the use of a LCL filter. The LCL filter consists of two inductors in series and a capacitor shunted between them. Compared to a filter with the use of a single inductor, the damping of the switching harmonics, at lower switching frequency, improve by using a LCL filter. In many application, when there is a transformer in the interface between the VSC and the grid, the leakage inductance in the transformer can be used as the second filter inductance. In [24] a method for designing the LCL filter is proposed. The total inductance of the filter should be as small as possible to realize fast tracking and high dynamics, and still handel the ripple in the current.

$$\Delta i_{L1,max} = \frac{V_{DC}}{8 L_1 f_{SW}} \tag{2.19}$$

The selection of current ripple is a trade off between the size of L_1, switching losses and inductor coil and core losses [40]. The choice of the capacitor is done based on the evaluation of the reactive power in the capacitor and in the inductance.

The resonance frequency of the system, ignoring the resistance for simplifications, is given by Equation 2.20.

$$f_{res} = \frac{1}{2\pi}\sqrt{\frac{L_1 + L_2 + L_g}{L_1(L_2 + L_g)C_f}} \tag{2.20}$$

In pu representation this becomes as in Equation 2.21.

$$\omega_{res} = \omega_b\sqrt{\frac{(L_{1,pu} + L_{g,pu})}{L_{g,pu}L_{1,pu}C_{f,pu}}} \tag{2.21}$$

The LCL filter itself is independent of the power level and the switching frequency as seen in Equation 2.20,but the LCL-filter resonance should be lower for lower switching frequencies to achieve better filtering. The switching in the VSC should be lower for higher power levels [25].

If the grid voltage is balanced the ripple in the current, for the use of a L-filter is described in [29] and given by Equation 2.22.

$$i_{ripple}(t) = \frac{1}{L}\int_0^t v_{ripple}(\tau)d\tau \tag{2.22}$$

2.3.5 Mathematical Model

When designing the control structure for the current, it is useful to have a model of the converter to design the controller properly. In [4], a mathematical model for a three phase voltage source converter, is presented. The system is assumed balanced. This model includes the effect of the switches, and the switching function. The dq representation in a synchronous reference frame is shown in Equation 2.23

$$\begin{aligned} u_{DC} &= (\frac{3}{2}(i_q d_q + i_d d_d) - i_{DC})\frac{1}{sC} \\ i_d &= (u_{DC} d_d - v_d + \omega L i_q)\frac{1}{R + sL} \\ i_q &= (u_{DC} d_q - v_q - \omega L i_d)\frac{1}{R + sL} \end{aligned} \tag{2.23}$$

This model can be simplified by merging the DC-voltage v_{dc} and the switching function d to an average v_{conv}. The VSC will then have a vector representation as shown in Equation 2.24, the current is defined positive in direction from the VSC towards the grid as shown in Figure 2.6.

$$\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & \omega \\ -\omega & -\frac{R}{L} \end{bmatrix}\begin{bmatrix} i_d \\ i_q \end{bmatrix} + \begin{bmatrix} v_{d,conv} - v_d \\ v_{q,conv} - v_q \end{bmatrix} \tag{2.24}$$

By using the pu transformation introduced in Section 2.2 the mathematical model in Equation 2.24 becomes as in Equation 2.25.

$$\begin{aligned} \frac{d}{dt}\begin{bmatrix} i_{d,pu} \\ i_{q,pu} \end{bmatrix} = \begin{bmatrix} -\frac{\omega_b R_{pu}}{L_{pu}} & \omega \\ -\omega & -\frac{\omega_b R_{pu}}{L_{pu}} \end{bmatrix}\begin{bmatrix} i_{d,pu} \\ i_{q,pu} \end{bmatrix} + \\ \frac{\omega_b}{L}\begin{bmatrix} v_{d,conv,pu} - v_{d,pu} \\ v_{q,conv,pu} - v_{q,pu} \end{bmatrix} \end{aligned} \tag{2.25}$$

This gives the block diagram of the VSC as shown in the Figure 2.9

The switching in the PWM can be mathematical modeled as a time delay for control manners. The 1.order transfer function approximation for the time delay is as in Equation 2.26 [30].

$$\frac{1}{1 + sT_a} \tag{2.26}$$

Where T_a is half the switching period.

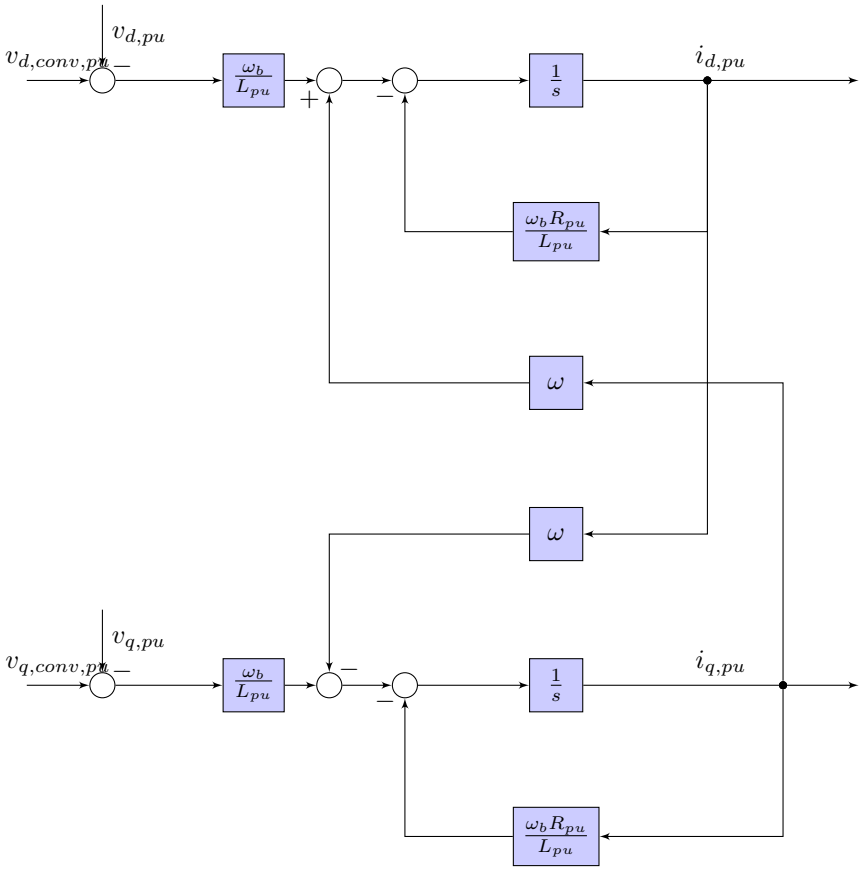


Figure 2.9: Block diagram of VSC

State-space model of the LCL circuit

The state space model presented in this thesis is largely based on the work done in [22], and modified to describe the system under investigation. The LC-circuit is described in Equation 2.23 and shown with pu-values in Figure 2.9. To include the capacitor in the filter and the weak grid thevenin equivalent inductance, that influences the point of synchronization, Equation 2.27 and Equation 2.28 are added to the mathematical model.

$$\begin{aligned} i_{od} &= (v_{cd} - v_{od} + \omega L_g i_{oq}) \frac{1}{R_g + sL_g} \\ i_{oq} &= (v_{cq} - v_{oq} - \omega L_g i_{od}) \frac{1}{R_g + sL_g} \end{aligned} \tag{2.27}$$

$$\begin{aligned} v_{cd} &= (i_d - i_{od} + \omega C v_{cq}) \frac{1}{sC} \\ v_{cq} &= (i_q - i_{oq} - \omega C v_{cd}) \frac{1}{sC} \end{aligned} \tag{2.28}$$

Where L_g and R_g are the grid side inductance and resistance in the weak grid thevenin equivalent. The state vector, the input vector and the output vector for this LCL-circuit subsystem is shown in Equation 2.29, Equation 2.30 and Equation 2.31 respectively.

$$\mathbf{x_{LCL}} = [i_{d,pu}\ i_{q,pu}\ i_{0,pu}\ v_{cd,pu}\ v_{cq,pu}\ v_{c0,pu}\ i_{od,pu}\ i_{oq,pu}\ i_{o0,pu}]^T \tag{2.29}$$

$$\mathbf{u_{LCL}} = [v_{d,conv,pu}\ v_{q,conv,pu}\ v_{0,conv,pu}\ v_{od,pu}\ v_{oq,pu}\ v_{o0,pu}\ \omega]^T \tag{2.30}$$

$$\mathbf{y_{LCL}} = [i_{d,pu}\ i_{q,pu}\ i_{0,pu}\ v_{cd,pu}\ v_{cq,pu}\ v_{c0,pu}\ i_{od,pu}\ i_{oq,pu}\ i_{o0,pu}]^T \tag{2.31}$$

The zero sequence components is added in the state space model here, but not given any attention since it is not considered in this work and removed from the total state-space model. The matrixes of the state space model for the LCL circuit in a pu-representation is written as in Equation 2.32.

$$\dot{\mathbf{x}}_{\mathbf{LCL}} = \mathbf{A}_{\mathbf{LCL}}\mathbf{x}_{\mathbf{LCL}} + \mathbf{B}_{\mathbf{LCL}}\mathbf{u}_{\mathbf{LCL}} + \mathbf{R}_{\mathbf{LCL}}(\mathbf{x}_{\mathbf{LCL}}, \mathbf{u}_{\mathbf{LCL}}) \tag{2.32}$$

Where:

$$\mathbf{A}_{\mathbf{LCL}} = \begin{bmatrix} -\frac{\omega_b R_{pu}}{L_{pu}} & 0 & 0 & -\frac{\omega_b}{L_{pu}} & 0 & 0 & 0 & 0 & 0 \\ 0 & -\frac{\omega_b R_{pu}}{L_{pu}} & 0 & 0 & -\frac{\omega_b}{L_{pu}} & -\frac{\omega_b}{L_{pu}} & 0 & 0 & 0 \\ 0 & 0 & -\frac{\omega_b R_{pu}}{L_{pu}} & 0 & 0 & 0 & -\frac{\omega_b}{C_{pu}} & 0 & 0 \\ \frac{\omega_b}{C_{pu}} & 0 & 0 & 0 & 0 & 0 & 0 & -\frac{\omega_b}{C_{pu}} & 0 \\ 0 & \frac{\omega_b}{C_{pu}} & 0 & 0 & 0 & 0 & 0 & 0 & -\frac{\omega_b}{C_{pu}} \\ 0 & 0 & \frac{\omega_b}{C_{pu}} & 0 & 0 & 0 & -\frac{\omega_b R_{g,pu}}{L_{g,pu}} & 0 & 0 \\ 0 & 0 & 0 & \frac{\omega_b}{L_{g,pu}} & 0 & 0 & 0 & -\frac{\omega_b R_{g,pu}}{L_{g,pu}} & 0 \\ 0 & 0 & 0 & 0 & \frac{\omega_b}{L_{g,pu}} & 0 & 0 & 0 & -\frac{\omega_b R_{g,pu}}{L_{g,pu}} \\ 0 & 0 & 0 & 0 & 0 & & & & \end{bmatrix} \tag{2.33}$$

$$\mathbf{B}_{\mathbf{LCL}} = \begin{bmatrix} \frac{\omega_b}{L_{pu}} & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{\omega_b}{L_{pu}} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{\omega_b}{L_{pu}} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{\omega_b}{L_{g,pu}} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{\omega_b}{L_{g,pu}} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{\omega_b}{L_{g,pu}} & 0 \end{bmatrix} \tag{2.34}$$

$$\mathbf{R}_{\mathbf{LCL}} = \begin{bmatrix} \omega i_{q,pu} \\ -\omega i_{d,pu} \\ 0 \\ \omega v_{cq,pu} \\ -\omega v_{cd,pu} \\ 0 \\ \omega i_{oq,pu} \\ -\omega i_{0d,pu} \\ 0 \end{bmatrix} \tag{2.35}$$

Since the output is equal to the state, the output matrix ($\mathbf{C}$) becomes the identity matrix ($\mathbf{I}$).

$$\mathbf{C} = \mathbf{I} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix} \tag{2.36}$$

State space model of the VSC

The state space model is a simplification of the system, and do not include the switches and the physical consequences of the voltage on the converter side of the filter being turned on and off. In the state space representation of the system, the converter is represented as a 1.order time delay approximation as in Equation 2.26. The state space model of the converter then becomes as in Equation 2.37

$$\mathbf{x_{VSC}} = \frac{d}{dt} \begin{bmatrix} v^*_{d,conv,pu} \\ v^*_{q,conv,pu} \end{bmatrix} = \begin{bmatrix} -\frac{1}{T_a} & 0 \\ 0 & -\frac{1}{T_a} \end{bmatrix} \begin{bmatrix} v^*_{d,conv,pu} \\ v^*_{q,conv,pu} \end{bmatrix} + \frac{1}{T_a} \begin{bmatrix} v_{d,conv,pu} \\ v_{q,conv,pu} \end{bmatrix} \tag{2.37}$$

Where $v^*_{dq,conv,pu}$ is the delayed converter voltage.

2.3.6 Mathematical model for unbalanced system

In unbalanced systems the mathematical model can be divided into the positive and negative sequence. The mathematical model for an unbalanced system has been derived in [21] and [35]. Based on the transformation of the unbalanced system into the two synchronous rotating reference frames, given in Equation 2.47 and 2.48, and the current and voltage in the positive and negative sequence, given in Equation 2.6. Since the simplification of the mathematical expression is already explained in Section 2.3.5, the derivation is skipped here, and the simplified pu-representation of the mathematical expression is shown in Equation 2.38.

$$
\begin{aligned}
i_d^+ &= (v_{d,conv}^+ - v_d^+ + \omega L i_q^+)\frac{1}{R+sL} \\
i_q^+ &= (v_{q,conv}^+ - v_q^+ - \omega L i_d^+)\frac{1}{R+sL} \\
i_d^- &= (v_{d,conv}^- - v_d^- - \omega L i_q^-)\frac{1}{R+sL} \\
i_q^- &= (v_{q,conv}^- - v_q^- + \omega L i_d^-)\frac{1}{R+sL}
\end{aligned}
\tag{2.38}
$$

The impedance of the negative sequence is the same as for the positive sequence for lines, transformers and reactors [34].

2.4 Grid Synchronization

The phase angle of the voltage vector is important and basic information for the VSC and injection of current needs to be synchronized with the grid voltages [3]. The Phase Locked Loop is the most extendedly used technique for grid synchronization, and will be given most attention and used for grid synchronization in this thesis. A number of different techniques for grid synchronization exist, and in [41] and [3] they were divided into the following main categories: Zero crossing method, filtering techniques, phase locked loop based- and adoptive notch filter- based techniques. The zero crossing method provides simplicity, but with low dynamic performance [3]. The filtering techniques consist of both $\alpha\beta$- and dq-filter algorithms. The adoptive notch filter-based techniques are frequency based and don't have a voltage controlled oscillator in their structures [41]. A good synchronization technique must track the phase and frequency variation of the utility signals and reject harmonics, disturbances and other types of pollution that exists in the grid signals [41]. The following section describes the Phase Locked Loop.

2.4.1 The Synchronous Reference Frame Phase Locked Loop (SRF-PLL)

Control of power factor is a common goal for several different applications of the VSC and detecting the phase angle is a critical part of achieving this. In the most common control structure, the PI controller in dq-reference frame (Section 2.6), the transformation of the current into DC-quantities is dependent on the

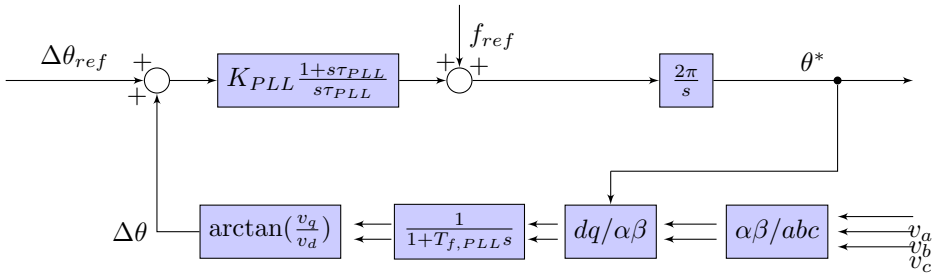


Figure 2.10: PLL Control Loop

angle of the dq-axis, which should be synchronized with the voltage vector. The PLL should therefore be designed to detect the correct angle of the voltage vector and lock the dq-axis to this angle so that the current and voltage are synchronized to the grid. The PLL should be able to phase-lock the utility voltages as quickly as possible and provide low distortion output under different operating conditions such as line notching, voltage unbalance, line dips and frequency variations [17].

2.4.2 Phase Locked Loop for a Balanced System

The structure of the PLL is shown in Figure 2.10. The voltage vector is transformed into $\alpha\beta$-reference frame and then into the dq-reference frame.

The $\Delta\theta$ is calculated by equation 2.39.

$$\Delta\theta = \arctan(\frac{V_q}{V_d}) \tag{2.39}$$

As long as the values of V_q are small, the term $\arctan(\frac{V_q}{V_d}) \approx \frac{V_q}{V_d}$ behaves linearly and $\arctan(\frac{V_q}{V_d}) \approx \Delta\theta$. Thus the PLL can be treated as a linear control for design purpose. Since the voltage vector and the d-axis should be aligned, $\Delta\theta_{ref}$ is equal to zero. If the voltage vector phase angle is greater than the phase angle of the d-axis, the angular speed of the dq-axis should be increased. The phase diagram in Figure 2.11 shows the different variables [16]. The PLL uses a PI-controller tuned after the symmetrical optimum as in Equation 2.40 and Equation 2.41

$$T_{i,PLL} = a^2 T_{f,PLL} \tag{2.40}$$

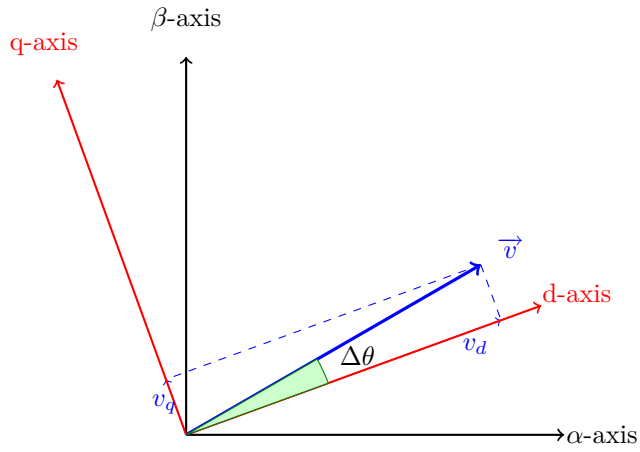


Figure 2.11: Phase diagram, showing the $\Delta\theta$

$$K_{p,PLL} = \frac{1}{aK_{VCO}T_{f,PLL}} \tag{2.41}$$

The filter time constant $T_{f,PLL}$ is chosen to attenuate the noise and harmonics and a should be in the range 2-4 [16].

A feed forward frequency of 50 Hz is used to reduce the pull-in time of the PLL.

State-space model of the PLL

Since the value of V_q is small, the linearization of the model, ($V_q = \Delta\theta$) is used for the state-space model of the PLL. The input variables to the PLL is the three-phase voltages over the capacitor, which the control system synchronizes to: $\mathbf{u_{PLL}} = [v_{ca}\ v_{cb}\ v_{cc}]^T$. This voltage is transformed by the clark transformation (Equation 2.7) and the park transformation (Equation 2.9). The measured voltage over the capacitors may contain harmonics and noise due to the distortion of the current at the point of measurements. Thus a low pass filter is added to remove the noise, and this filter should be added in the state-space model.

$$v'_{cq} = \frac{1}{1 + T_{f,PLL}s} v_{qc} \tag{2.42}$$

Re-arranging Equation 2.42 into integro-differential form as in Equation 2.43 with the filtered voltage as a state-variable in the state space model.

$$v'_{cq}s = \frac{1}{T_{f,PLL}}(v_{cq} - v'_{cq}) \tag{2.43}$$

The closed loop PI controller acts on the alignment error to set the rotation frequency, and the integral of the frequency gives the angle, as given in Equation 2.44 and 2.45 respectively.

$$\omega = 2\pi(K_{p,PLL}v'_{cq} + K_{i,PLL}\int v'_{cq}dt) \tag{2.44}$$

$$\theta = \int \omega dt \tag{2.45}$$

A virtual flux $\psi_{PLL} = \int v'_{cq}dt$ is defined to express 2.44 in a purely differential form, and is a state variable together with θ and v'_{cq}. $\mathbf{x_{PLL}} = [v'_{cq}\ \theta\ \psi_{PLL}]^T$. The output of the PLL is: $\mathbf{y_{PLL}} = [\theta\ v_{cd}\ v_{cq}]^T$. The state space model of the PLL can then be written in the form given in Equation 2.46.

$$\dot{\mathbf{x}}_{\mathbf{PLL}} = \mathbf{A_{PLL}}\mathbf{x_{PLL}} + \mathbf{R_{PLL}}(\mathbf{x_{PLL}}, \mathbf{u_{PLL}})$$

$$\dot{\mathbf{x}}_{\mathbf{PLL}} = \begin{bmatrix} -\frac{1}{T_{f,PLL}} & 0 & 0 \\ 2\pi K_{p,PLL} & 0 & 2\pi K_{i,PLL} \\ 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} v'_{cq} \\ \theta \\ \psi_{PLL} \end{bmatrix} + \begin{bmatrix} \frac{1}{T_{f,PLL}}v_{cq} \\ 0 \\ 0 \end{bmatrix} \tag{2.46}$$

2.4.3 Phase Locked Loop for Unbalanced Systems

Under unbalance conditions, there exists both and positive and negative rotating voltage vector. A fast and precise detection of both the positive and the negative sequence angle and magnitude of the voltage component is a vital issue during transient faults in the grid [32]. To control the components in both sequences, two rotating reference frame can be introduced. The PLL for an unbalanced system is controlled, as for the PLL in the balanced system, to synchronize with, and to be locked to, the positive sequence voltage vector. The position of the negative sequence reference frame has the negative angle of the positive sequence reference frame.

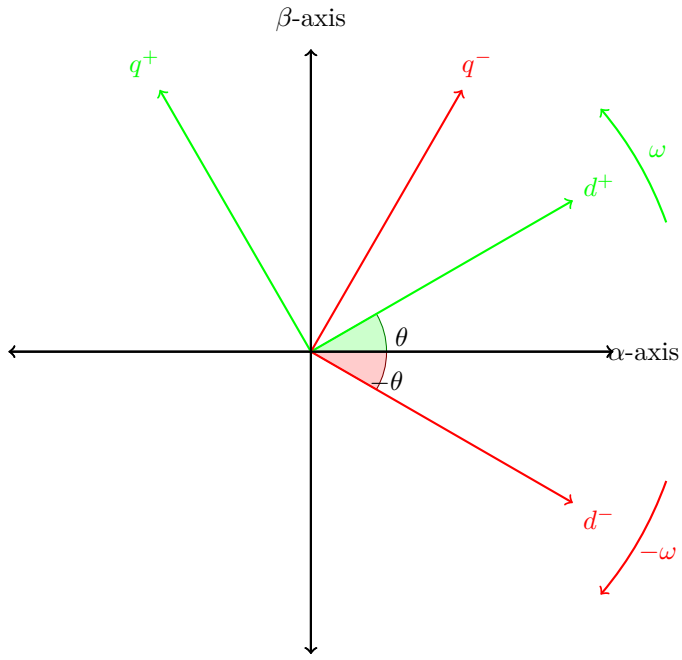


Figure 2.12: Positive and negative synchronous rotating reference frame

dq-transformation for unbalanced and unsymmetrical system

The synchronous rotating reference frame of the positive and negative sequence is chosen to be respectively as the green, and the red reference frames as shown in Figure 2.12. The transformation of the electrical component vectors is shown in Equation 2.47 and in 2.48 for respectively the positive rotating reference frame dq^+ and the negative rotating reference frame dq^-. As shown in Figure 2.12, the positive reference frame is rotating in a counterclockwise direction and the negative reference frame is rotating in a clockwise direction.

$$\begin{bmatrix} X_{d^+} \\ X_{q^+} \end{bmatrix} = \begin{bmatrix} \cos(\theta) & \sin(\theta) \\ -\sin(\theta) & \cos(\theta) \end{bmatrix} \begin{bmatrix} X_\alpha \\ X_\beta \end{bmatrix} \tag{2.47}$$

$$\begin{bmatrix} X_{d^-} \\ X_{q^-} \end{bmatrix} = \begin{bmatrix} \cos(\theta) & -\sin(\theta) \\ \sin(\theta) & \cos(\theta) \end{bmatrix} \begin{bmatrix} X_\alpha \\ X_\beta \end{bmatrix} \tag{2.48}$$

The the voltage vector can be expressed as in Equation 2.49 for the positive dq-reference frame and as in Equation 2.50 for the negative dq-reference frame.

$$\begin{bmatrix} v_{d^+} \\ v_{q^+} \end{bmatrix} = V^+ \begin{bmatrix} \cos(\phi^+) \\ \sin(\phi^+) \end{bmatrix} + V^- \cos(\phi^-) \begin{bmatrix} \cos(2\omega t) \\ -\sin(2\omega t) \end{bmatrix} + V^- \sin(\phi^-) \begin{bmatrix} \sin(2\omega t) \\ \cos(2\omega t) \end{bmatrix} \tag{2.49}$$

$$\begin{bmatrix} v_{d^-} \\ v_{q^-} \end{bmatrix} = V^- \begin{bmatrix} \cos(\phi^-) \\ \sin(\phi^-) \end{bmatrix} + V^+ \cos(\phi^+) \begin{bmatrix} \cos(2\omega t) \\ \sin(2\omega t) \end{bmatrix} + V^+ \sin(\phi^+) \begin{bmatrix} -\sin(2\omega t) \\ \cos(2\omega t) \end{bmatrix} \tag{2.50}$$

The constants in Equation 2.50 and 2.49, $V^+ \cos(\phi^+)$, $V^+ \sin(\phi^+)$, $V^- \cos(\phi^-)$ and $V^- \sin(\phi^-)$, represents the average value of the voltage in respectively the d and q axis in the positive sequence and the d and q axis in the negative synchronous reference frame. As seen from the equations the transformation into positive and negative rotating reference frame gives an oscillation two times the fundamental frequency caused by the negative reference frame in the positive reference frame, and vice versa for the negative reference frame. This addresses the problem of synchronization in an unbalanced grid, and the following next two subsections reviews methods for removing these oscillations.

PLL with Notch Filter

To suppress the oscillation from the opposite reference frame, the two synchronous rotating reference frame voltage measurements can be filtered in the grid synchronization. A low-pass filter of 100 Hz will reduce the band width of the control system, and may cause stability problems. Therefor a notch filter is introduced in [35]. A notch filter is a band-stop filter with a narrow stop band as given in Equation 2.51. Since it is reducing the gain only at twice the fundamental frequency signals it is not effecting the band width of the control system.

$$T(s) = \frac{s^2 + 2\omega}{s^2 + \frac{2\omega s}{Q} + (2\omega)^2} \tag{2.51}$$

The size of Q determines the bandwidth of the filter. A high Q gives a smaller band. Figure 2.13 shows the bode plot of the filter with $Q = 10$.

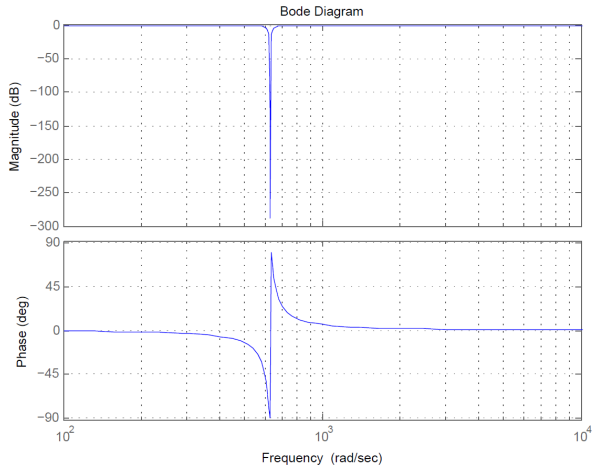


Figure 2.13: Bode plot of notch filter

The notch filter removes by time the oscillations from the negative sequence seen in the positive rotating reference frame and vice versa, and the angular position of the positive sequence voltage vector can be detected without influence of the negative sequence.

Decoupled Double Synchronous Reference frame PLL (DDSRF-PLL)

[33] proposes a method for removing the oscillations in the two reference frame, by a decoupling of the positive and negative sequence. The decoupling is based on Equation 2.49 and 2.50 and shown in Equation 2.52 and in Figure 2.14. By adding the decoupling algorithm in Equation 2.52 to Equation 2.49 the voltages that are used for synchronization are independent of the opposite sequence. The figure and mathematical expression is shown only for the positive sequence. The same operation is performed for the negative sequence, and the block diagram, and the Equation is shown in Appendix,Figure A.1 and Equation A.1 .

$$\begin{aligned}\begin{bmatrix} v^*_{d+} \\ v^*_{q+} \end{bmatrix} &= \begin{bmatrix} v_{d+} \\ v_{q+} \end{bmatrix} - v^-_{d-} \begin{bmatrix} \cos(2\omega t) \\ -\sin(2\omega t) \end{bmatrix} - v^-_{q-} \begin{bmatrix} \sin(2\omega t) \\ \cos(2\omega t) \end{bmatrix} \\ &\approx V^+ \begin{bmatrix} \cos(\phi^+) \\ \sin(\phi^+) \end{bmatrix}\end{aligned} \tag{2.52}$$

To determine the average value used for the cross feedback decoupling a low pass filter is used designed as in Equation:

$$LPF(s) = \frac{\omega_f}{s + \omega_f} \tag{2.53}$$

The PI controller in the PLL synchronize the positive rotating reference frame with the voltage. The negative rotating reference frame is set to be the negative value of the angle of the positive sequence. The block diagram of the PLL is shown in Figure 2.15. The same procedure as for the PLL described in Figure 2.10 is used for the decoupled positive sequence voltages to calculate/control the positive sequence synchronous reference frame instantaneous angle and frequency.

2.5 Active Damping (AD)

To damp the high frequency harmonics from the switches, usually in the range of 2-15kHz, in the VSC, a passive LCL filter is used on the grid side, introduced in Section 2.3.4. To overcome the problem of resonance and the oscillation of the filters, damping is necessary. A resistor in series with the capacitor in the filter, will cause a loss in power. Thus an active damper is used to avoid the problem of power losses.

2.5.1 AD - Using a High Pass Filter

To cancel out the ripples caused by the resonance frequency, the voltage of the capacitor is measured and then filtered through a high pass filter, so that the oscillating component is extracted from the voltage [31]. The high pass filter should be tuned to only include the harmonics of frequency of order higher than the bandwidth of the control loop. Then the high frequency components are amplified by a proportional amplifier and subtracted from the current reference. This can be placed before or after the PI controller (when using a PI-controller), since the signals of the ripples are to fast for the integrator and will therefore only go through the proportional gain. The principle of the AD is shown in Figure 2.16.

State space model of Active Damping

The active damping high pass filter can be arranged in a differential form for the d-axis and the q-axis as shown in Equation 2.54.

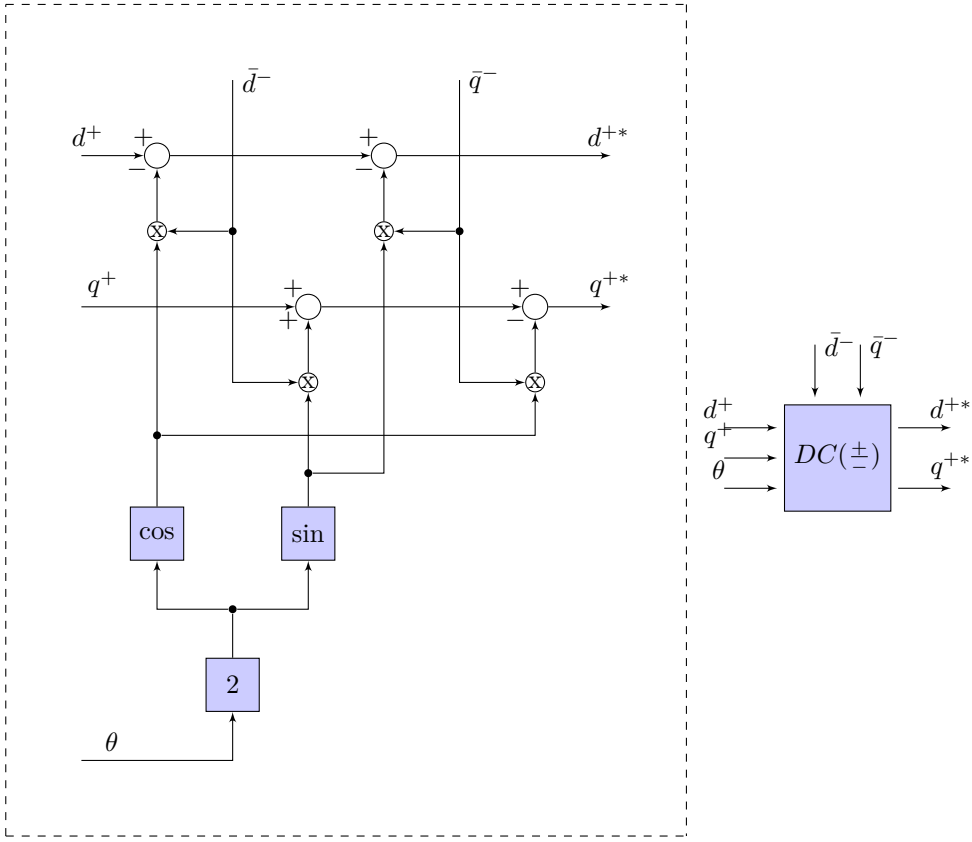


Figure 2.14: Decoupling of the positive and negative sequence

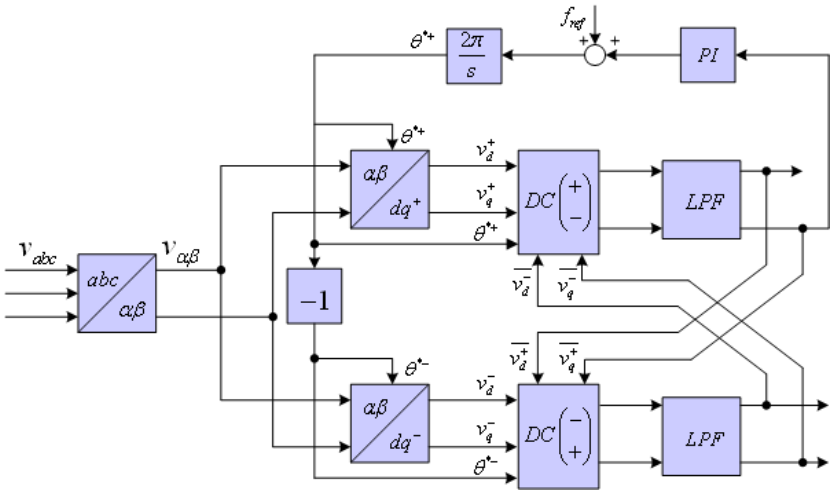


Figure 2.15: The DDSRF-PLL

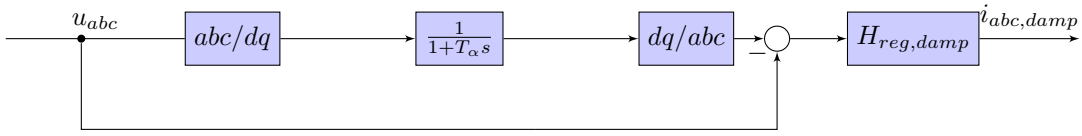


Figure 2.16: The Active damping

$$i_{ad,d} = -\frac{1}{sT_\alpha} i_{ad,d} - K_\alpha v_{cd}$$
$$i_{ad,q} = -\frac{1}{sT_\alpha} i_{ad,q} - K_\alpha v_{cq} \tag{2.54}$$

To obtain the state-space model, new variables from Equation 2.54 are introduced. $q_{ad} = \int i_{ad} dt$. Equation 2.54, then becomes as in Equation 2.55.

$$sq_{ad,d} = -\frac{1}{T_\alpha} q_{ad,d} - K_\alpha v_{cd}$$
$$sq_{ad,q} = -\frac{1}{T_\alpha} q_{ad,q} - K_\alpha v_{cq} \tag{2.55}$$

Where the input vector $\mathbf{u} = [v_{cd}\ v_{cq}]^T$. The output vector becomes $\mathbf{y} = [i_{ad,d}\ i_{ad,q}]^T$. And the state vector is given by the new state variables, $\mathbf{x} = [q_{ad,d}\ q_{ad,q}]^T$ This gives the following **A**-matrix 2.56 and **B**-matrix 2.57

$$\mathbf{A_{AD}} = \begin{bmatrix} -\frac{1}{T_\alpha} & 0 \\ 0 & -\frac{1}{T_\alpha} \end{bmatrix} \tag{2.56}$$

$$\mathbf{B_{AD}} = \begin{bmatrix} -K_\alpha & 0 \\ 0 & -K_\alpha \end{bmatrix} \tag{2.57}$$

Since the active damping is added in the current controller, it will seen by the derivation of the assembled state space model shown in Appendix D, that the voltage feed forward loop and the active damping can be simplified by adding them together and substituting $q_{ad,d}\ q_{ad,q}$ with the state variables $v_{cd} *\ v_{vq} *$.

2.6 SRF- Proportional Integrator (SRF-PI) Controller

The PI controller is a widely used control structure. It contains a proportional gain and an integrator, as shown in Equation 2.58.

$$G_{PI}(s) = K_p(\frac{1 + \tau_i s}{\tau_i s}) \tag{2.58}$$

Since the electric quantities in the synchronous reference frame acts as DC quantities, it is common to transform the mathematical model of the VSC into

the synchronous dq-reference frame and use a PI-controller to obtain zero steady state error. The integrator in the PI controller gives infinite gain at zero frequency, which results in zero steady state error.

2.6.1 Decoupling of the d and q axis

Using the simplified pu-represented mathematical model of the VSC and the filter inductance found in Equation 2.25, the proportional gain and the integrator time constant can be found. In this control structure it is desirable to control the d- and q- current independently. To avoid the cross coupling between i_d and i_q and the capacitor voltage from the filter, Equation 2.25 should be written in the canonic form, as in Equation 2.60[28]

$$\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} -\frac{\omega_b R_{pu}}{L_{pu}} & 0 \\ 0 & -\frac{\omega_b R_{pu}}{L_{pu}} \end{bmatrix} \begin{bmatrix} i_{d,pu} \\ i_{q,pu} \end{bmatrix} + \frac{\omega_b}{L} \begin{bmatrix} v`_{d,conv,pu} \\ v`_{q,conv,pu} \end{bmatrix} \tag{2.59}$$

To obtain this the controller should be added a feed forward loop for the capacitor voltage and a decoupling of the currents, as shown in Equation 2.60.

$$\begin{bmatrix} v_{d,conv,pu} \\ v_{q,conv,pu} \end{bmatrix} = \begin{bmatrix} 0 & -\omega \\ \omega & 0 \end{bmatrix} \begin{bmatrix} i_{d,pu} \\ i_{q,pu} \end{bmatrix} + \begin{bmatrix} v'_{d,conv,pu} + v_{d,pu} \\ v'_{q,conv,pu} + v_{q,pu} \end{bmatrix} \tag{2.60}$$

Then the voltage and the coupled current is removed from the system and the transfer function between the current and the converter voltage is given by Equation 2.61. The use of subscript is skipped, since the transfer function is the same for both the d- and q-axis current.

$$\frac{i_{pu}}{v_{con,pu}} = \frac{1}{R_{pu}} \frac{1}{1 + \frac{L_{pu}}{\omega_b R pu} s} \tag{2.61}$$

The block diagram of the current controller for the d-axis and q-axis current becomes as in Figure 2.17.

2.6.2 Tuning of the PI Controller for the Current Loop

By combining Equation 2.61 and Equation 2.26, and using the modulus optimum criteria the PI controller is tuned. For the derivation of the modulus optimum see the Appendix B.

$$K_{p,pu} = \frac{\tau_{pu} R_{pu}}{2T_a} \tag{2.62}$$

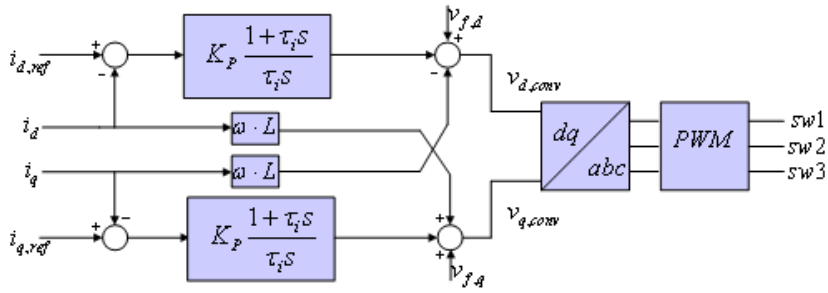


Figure 2.17: PI current controller with decoupling between the d-axis and the q-axis

and

$$\tau_i = \tau_{pu} \tag{2.63}$$

Where

$$\tau_{pu} = \frac{L_{pu}}{\omega_b R_{pu}} \tag{2.64}$$

Sine $\tau_i = \tau_{pu}$, the terms, $1+\tau_i s$ and $1+\tau_{pu} s$ cancel each other out, the open loop transfer function of the current loop becomes as i Equation 2.65 and the closed loop transfer function as in Equation 2.66.

$$H_{OL} = \frac{K_{p,pu}}{\tau_{pu} R_{pu}} \frac{1}{s(1+T_a s)} \tag{2.65}$$

$$H_{CL}(s) = \frac{\frac{K_{p,pu}}{R_{pu}\tau_i T_a}}{s^2 + \frac{1}{Ta}s + \frac{K_{p,pu}}{R_{pu}\tau_i T_a}} \tag{2.66}$$

The bandwidth of the system is defined, by the Nyquist criteria, as the frequency where the gain of the open loop transfer function crosses -3dB line or the phase delay becomes greater than 45 degrees. Since this do not always occur at the same time, the definition that gives the smallest bandwidth should be chosen [12].

The damping factor and the undamped natural frequency is given by equation 2.67 and 2.68 [15].

$$\omega_n = \sqrt{\frac{K_{p,pu}}{\tau_{pu} R_{pu} T_a}} = \frac{1}{\sqrt{2} T_a} \tag{2.67}$$

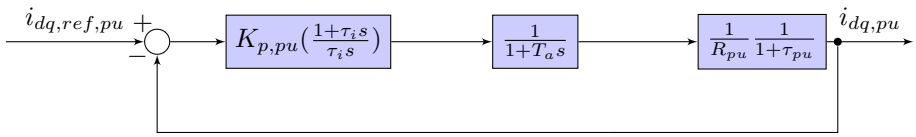


Figure 2.18: Current Loop for the PI controller

$$\xi = \frac{1}{2}\sqrt{\frac{\tau_{pu} R_{pu}}{K_{p,pu} T_a}} = \frac{1}{\sqrt{2}} \tag{2.68}$$

State-space model of the current controller

The state space of the PI controller with decoupling of the d and q axis is shown in the Equation 2.73. To obtain the state space model new variables are introduced: $q_{ld}^{err} = \int i_{ld}^{err} dt$ and $q_{lq}^{err} = \int i_{lq}^{err} dt$. These state variables can be obtained as a charge, since its the integral of the current. The state vector is given in 2.69, the input vector is given in 2.71 and the output vector as in 2.70.

$$\mathbf{x_{cc}} = [q_{ld}^{err}\ q_{lq}^{err}]^T \tag{2.69}$$

$$\mathbf{y_{cc}} = [v_{d,conv,pu}\ v_{q,conv,pu}]^T \tag{2.70}$$

$$\mathbf{u_{cc}} = [i_{d,ref,pu}\ i_{q,ref,pu}\ i_{d,pu}\ i_{q,pu}\ v_{cd,pu}\ v_{cq,pu}\ \omega]^T \tag{2.71}$$

The state space model of the current controller has a standard linear form, but the A-matrix is zero because of the new variables which do not include internal feedback.

$$\dot{\mathbf{x}}_{\mathbf{cc}} = \mathbf{A_{cc}}\mathbf{x_{cc}} + \mathbf{B_{cc}}\mathbf{u_{cc}}$$

$$\dot{\mathbf{x}}_{\mathbf{cc}} = \begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} q_{ld}^{err} \\ q_{lq}^{err} \end{bmatrix} + \begin{bmatrix} 1 & 0 & -1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & -1 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_{d,ref} \\ i_{q,ref} \\ i_d \\ i_q \\ v_{cd} \\ v_{cq} \\ \omega \end{bmatrix} \tag{2.72}$$

$$\mathbf{y_{cc}} = (\mathbf{C}\mathbf{x_{cc}} + \mathbf{D}\mathbf{u} + \mathbf{S}(\mathbf{u}))$$

$$\mathbf{y_{cc}} = \begin{bmatrix} K_i & 0 \\ 0 & K_i \end{bmatrix} \begin{bmatrix} q_{ld}^{err} \\ q_{lq}^{err} \end{bmatrix} + \begin{bmatrix} K_{p,pu} & 0 & -K_{p,pu} & 0 & 1 & 0 & 0 & 1 & 0 \\ 0 & K_{p,pu} & 0 & -K_{p,pu} & 0 & 1 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_{d,ref} \\ i_{q,ref} \\ i_d \\ i_q \\ v_{cd} \\ v_{cq} \\ \omega \\ i_{ad,d} \\ i_{ad,q} \end{bmatrix} + \begin{bmatrix} -\omega i_{q,pu} \\ \omega i_{d,pu} \end{bmatrix} \tag{2.73}$$

2.6.3 Dual Current PI controller

Separately measured currents of the positive and negative sequences can be used for separate control of the two sequences currents. This can be implemented by a dual PI controller, which consists of a PI controller structure that regulates the positive sequence currents in the positive synchronous rotating reference frame, and another PI controller structure that regulates the negative sequence currents in the negative synchronous rotating reference frame [35]. As for the voltage there is a 100 Hz oscillation in the components in the two rotational reference frame caused by the reversal of rotating direction between them. As shown in Equation 2.74.

$$I_{dq^+} = I_{dq^+} + e^{-j\omega t} I_{dq^-}$$

$$I_{dq^-} = I_{dq^-} + e^{j\omega t} I_{dq^+} \tag{2.74}$$

Hence for control purpose of the the two sequences, the measured current needs to be separated into the positive sequence and the negative sequence. This is can be achieved in the same way as separation of the two sequences in the PLL. Hence in this thesis the measured current in the dual PI controllers are separated in two ways, by a notch filter, as presented in Section 2.4.3 and by the decoupling algorithm as for the DDSRF-PLL, presented in Section 2.4.3.

With proper separation of the two sequences they can be controlled as DC-signals in their corresponding rotational reference frame. The control system of the positive sequence currents will be as for the synchronous rotating reference frame currents as described in Section 2.6, while the negative sequence control system will have opposite polarity in the decoupling of the d- and q-axis currents, since the rotational induced voltages are of opposite polarity, given by the clockwise rotational direction of the negative sequence synchronous rotating reference frame. This can be seen in the mathematical model of the system in Equation 2.38.

It can also be added here that the control of the negative sequence currents will be important with respect to the DC-link voltage and the quality of the power delivered from the converter under unbalanced voltage conditions. Unbalanced voltage conditions will cause 100 Hz oscillations in the DC-link voltage and in the power that can be removed with proper selection of the negative sequence current reference [35]. The control of negative sequence current to remove these oscillations in the DC-link will however not be implemented in this thesis, but control structures that are able to control both the positive and the negative sequence currents will be investigated.

2.7 State Space Model including the PI Current Controller

The VSC is a complex dynamic system that interacts with the grid. The model of the integration of VSC in DG systems must include all the dynamics of the converter in the frequency range of interest. This model should then include both the LCL filter in the interface between the converter and the grid, and the control system associated with the converter circuit. A single state-space model which includes the physical model and the transformation, current control and the PLL is derived in [22] and modified in this thesis. The state-space model will be in the form given by Equation 2.75.

$$\begin{aligned} \dot{x} &= Ax + R(x,u) \\ y &= S(x,u) \end{aligned} \tag{2.75}$$

Complete State-space Model

The state-variables for the different subsystems (PLL, VSC, Current Controller and the LCL-filter) are added together in one state-variable array as in 2.76.

$$\mathbf{x_{tot}} = [v'_{cq}\ \theta\ \psi_{PLL}\ q_{ld}^{err}\ q_{lq}^{err}\ v_{cd}^{*}\ v_{cq}^{*}\ v_{d,conv} *\ v_{q,conv} *\ v_{d,conv}\ v_{q,conv}\ i_d\ i_q\ v_{cd}\ v_{cq}\ i_{od}\ i_{oq}]^T \tag{2.76}$$

The same is done for the total $\mathbf{A_{tot}}$-matrix as shown in Equation 2.77.

$$\mathbf{A_{tot}} = \begin{bmatrix} \mathbf{A_{PLL}} & 0 & 0 & 0 \\ 0 & \mathbf{A_{cc}} & 0 & 0 \\ 0 & 0 & \mathbf{A_{VSC}} & 0 \\ 0 & 0 & 0 & \mathbf{A_{LCL}} \end{bmatrix} \tag{2.77}$$

Since the input for some of the subsystem is a state-variable in the total system, the sub $\mathbf{A}$-matrixes of the total $\mathbf{A_{tot}}$-matrix must be adjusted to include these variables. The total A-matrix becomes then as shown in Appendix D. The state values of the active damping has been changed in the final state space model. They are based on the sub state space models, but when some mathematical expression has been added together to give fewer stat variables the two new state variables v_{cd}^{*} and v_{cq}^{*} will appear as a combination of the voltage feed-forward loop in the current controller and the active damping. This is explained in the Appendix D. Also the zero sequence components has been removed, since this is not considered in the analysis.

2.8 Proportional Resonant (PR) Controller

The PI control structure described in Section 2.6 is designed for variables transformed into a synchronous rotating reference frame, which gives DC behavior in the control manner. Due to the simplicity and the zero steady state error this is the most common current control structure for the VSC. Since this gives a complex transformation, which may lead to an error if the dq reference frame is not synchronized with the voltage vector, a method for controlling the current directly in the stationary abc- reference frame is presented in [43]. A frequency

domain transfer function transformed from the dq- reference frame to the $\alpha\beta$-reference frame will be as in Equation 2.78 [42].

$$H_{AC}(s) = \frac{1}{2}[H_{DC}(s + j\omega) + H_{DC}(s - j\omega)] \tag{2.78}$$

Where ω is the angular speed of the rotating dq-reference system. Equation 2.78 gives the stationary $\alpha\beta$-reference transfer function as in Equation 2.79.

$$H_{\alpha\beta}(s) = K_p + \frac{2K_i s}{s^2 + \omega^2} \tag{2.79}$$

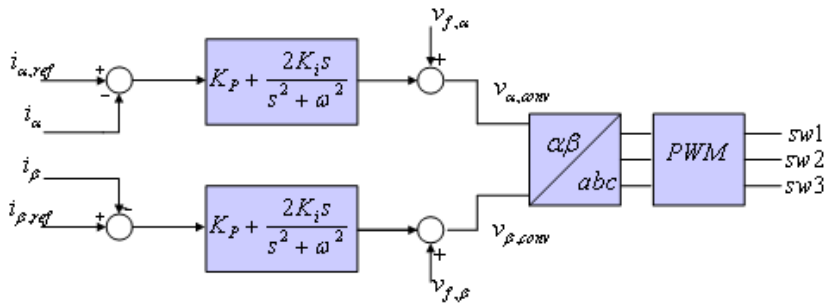


Figure 2.19: The PR current controller

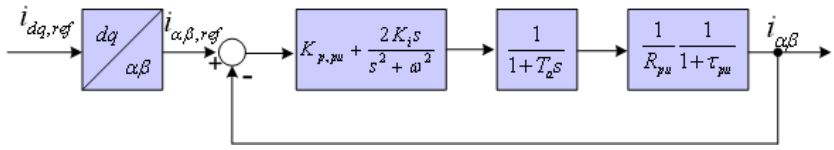


Figure 2.20: Current Loop for the PR controller

The transfer function of the resonant controller has a infinite gain at the frequency of operation, and will have a zero steady state error. The bode plot of the resonant controller is shown as the black plot in Figure 2.21.

Since the controller has the infinite gain at, or close to, the frequency of the grid, it is extremely weak for changes in the frequency. A possible method to solve this is to insert a damping factor and choose a band width of the controller system, as shown in Equation 2.80. The bode plot of this controller is shown

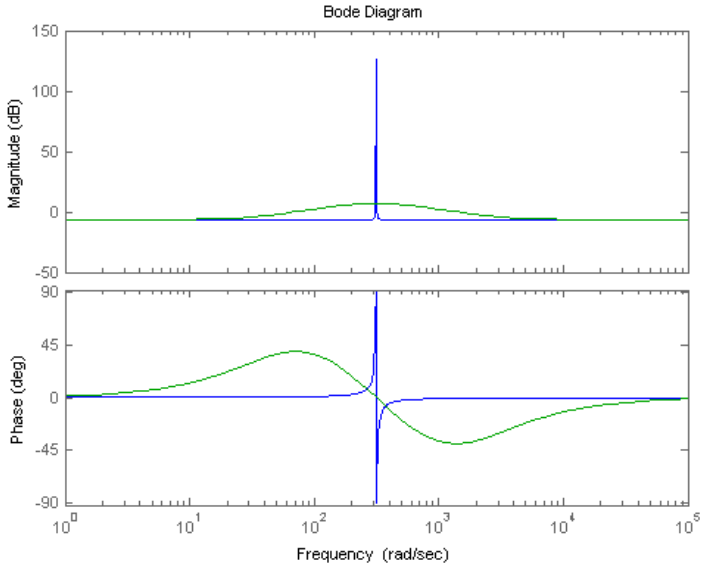


Figure 2.21: Frequency response of PR controller. The blue plot shows the bode plot for Equation 2.79 and the green plot shows for Equation 2.80

as the green plot in Figure 2.21. As seen from the plot the band width has increased, but the gain is reduced. ω_c is chosen so; $\omega_c << \omega$

$$H_{\alpha\beta}(s) = K_p + \frac{K_i \omega_c s}{s^2 + 2\omega_c s + \omega^2} \tag{2.80}$$

2.8.1 PR-controller in unbalanced grid

The PR-controller controls the current in the stationary $\alpha\beta$-reference frame. Hence the control under unbalanced conditions and the control of the positive and negative sequence current is performed in one and the same control loop. The transformation of the PI current control into the stationary reference frame is as shown in Equation 2.81 [37].

$$H_{\alpha\beta}(s) = \frac{1}{2} \begin{bmatrix} H_{dq^+} + H_{dq^-} & jH_{dq^+} - jH_{dq^-} \\ jH_{dq^+} + jH_{dq^-} & H_{dq^+} + H_{dq^-} \end{bmatrix} \tag{2.81}$$

Where $H_{dq^+} = H_{dq}(s + j\omega)$ and $H_{dq^-} = H_{dq}(s - j\omega)$. The equivalent controllers for compensating the positive sequence feedback error signals when $H_{dq} = \frac{Ki}{s}$ becomes then as in Equation 2.82

$$H^+_{\alpha\beta}(s) = \frac{1}{2}\begin{bmatrix} \frac{2K_i s}{s^2+\omega^2} & \frac{2K_i s}{s^2+\omega^2} \\ -\frac{2K_i s}{s^2+\omega^2} & \frac{2K_i s}{s^2+\omega^2} \end{bmatrix} \tag{2.82}$$

Similarly for compensating the negative sequence becomes as in Equation 2.83

$$H^-_{\alpha\beta}(s) = \frac{1}{2}\begin{bmatrix} \frac{2K_i s}{s^2+\omega^2} & -\frac{2K_i s}{s^2+\omega^2} \\ \frac{2K_i s}{s^2+\omega^2} & \frac{2K_i s}{s^2+\omega^2} \end{bmatrix} \tag{2.83}$$

The opposite polarities in the diagonal terms can be seen as the reversal of the rotational direction of the two rotating reference frame. Combing Equation 2.82 and Equation 2.83 gives Equation 2.84 that compensate both the positive and the negative sequence feedback error. Also the decoupling term of the d- and q-axis currents are now removed from the control system.

$$H_{\alpha\beta}(s) = \frac{1}{2}\begin{bmatrix} \frac{2K_i s}{s^2+\omega^2} & 0 \\ 0 & \frac{2K_i s}{s^2+\omega^2} \end{bmatrix} \tag{2.84}$$

2.9 Non Linear Control - Hysteresis controller

The hysteresis controller is a non-linear controller loop with hysteresis comparators. Switches are turned on and off, and forms the voltage vectors presented in Section 2.3.3, depending on where the error of the current is compared to a reference band. Among advantages using a hysteresis control is predominantly the simplicity, robustness, independence of load parameters and good dynamics [19]. There are two main disadvantages by using the hysteresis controller. It does not have any fixed switching frequency and therefore a wide frequency spectrum, and current ripple is relatively high and can theoretically reach twice the size of the band limit for the phase current hysteresis controller.

2.9.1 Hysteresis controller in abc-reference frame

The simplest of the hysteresis controllers is the hysteresis controller for the *abc*-reference frame with a fixed two level hysteresis band. The three phases are controlled separately. If the current exceeds the band limit, the switch connected to the phase which exceeds the band limit is turned off and the voltage at the

converter terminal is equal to 0 (or $-\frac{1}{2}V_{DC}$), if the current founders the band limit, the switch will be turned on and the voltage at the converter terminal is equal to V_{DC} (or $\frac{1}{2}V_{DC}$). This forces the current to follow the reference as given in Equation 2.85 [38].

$$\begin{aligned} i_{ref} &= i_{max}\sin(\omega t) \\ i_{up} &= i_{ref} + \Delta i \\ i_{lo} &= i_{ref} - \Delta i \end{aligned} \tag{2.85}$$

A problem concerning this control method is the interaction between the three phase currents when they have a common neutral. The control of one phase will influence the two other phases. This leads to a miss-match with the bandlimits and possibly high ripple in the current. The block diagram of the two level hysteresis controller is shown in Figure 2.22.

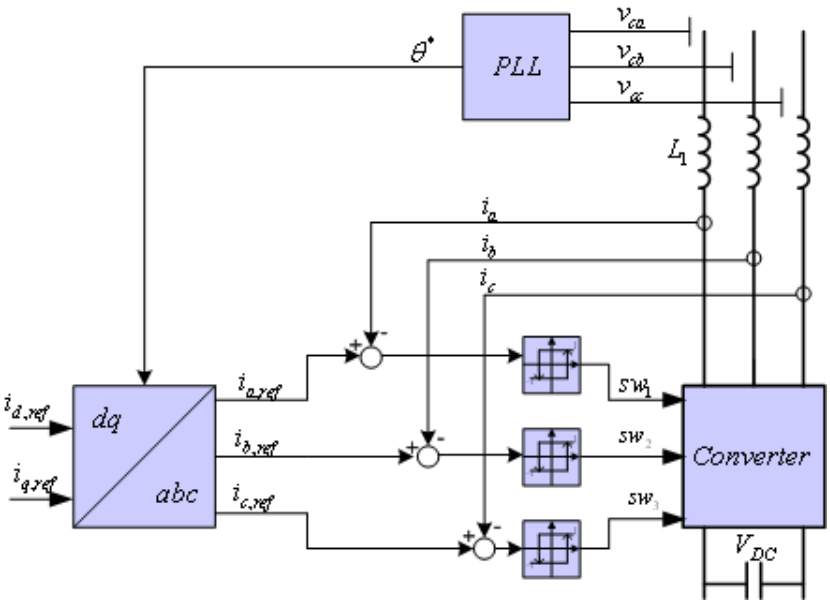


Figure 2.22: *abc*-hysteresis controller with three two level hysteresis comparators

2.9.2 Hysteresis controller based on Space Vector Approach

In [18] and [20], an approach for controlling the current in an induction machine is proposed. This control structure can also be applied in converters for grid connection, and is given attention in the paper added in Appendix I. The method uses separate three level hysteresis band for the d and q axes. By transforming the three phase currents into a current vector, the control is performed on the three phases simultaneously. This prevents, or take into account, the problem of the interaction of the three phases. The control loop is shown in Figure 2.23. The method uses a switching table based on the appropriate voltage vector that can be represented from the VSC as shown in Figure 2.8. The three level hysteresis band makes the controller include the use of the zero voltage vectors, this may reduce the switching frequency compared to the hysteresis *abc*-reference controller if the voltage in drops.

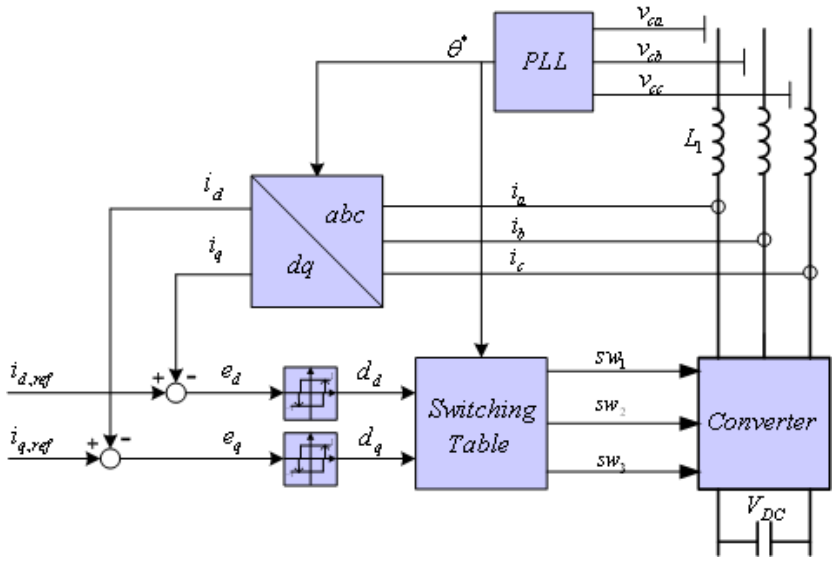


Figure 2.23: *dq*-hysteresis controller with two three level hysteresis comparators

Three level hysteresis band

The three level hysteresis band is shown in figure 2.24. It consist of outer band limits, negative A_{low} and positive A_{up} and inner band limits, a negative B_{low} and positive B_{up}.

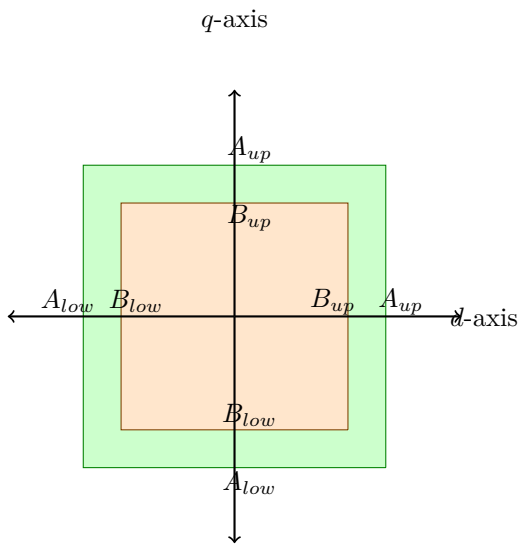


Figure 2.24: Three level hysteresis band.

First the error of the current is compared with the band limits, the positive and negative for both the outer band limit and the inner band limit, as shown in Figure 2.25. The output of the comparators continues into the flip flops. For the inner band the output of the positive band limit comparator goes to the "set input" (S) and the output of the negative band limit comparator to the "reset input" (R). For the outer band it's the opposite. The output of the negative band limit comparator goes to R and the output of the positive band limit comparator to S, as shown in Figure 2.25 and Equation 2.86.

$$S_1 = \begin{cases} 1 & \text{if} i_e > B_{up} \\ 0 & \text{if} i_e < B_{up} \end{cases}$$

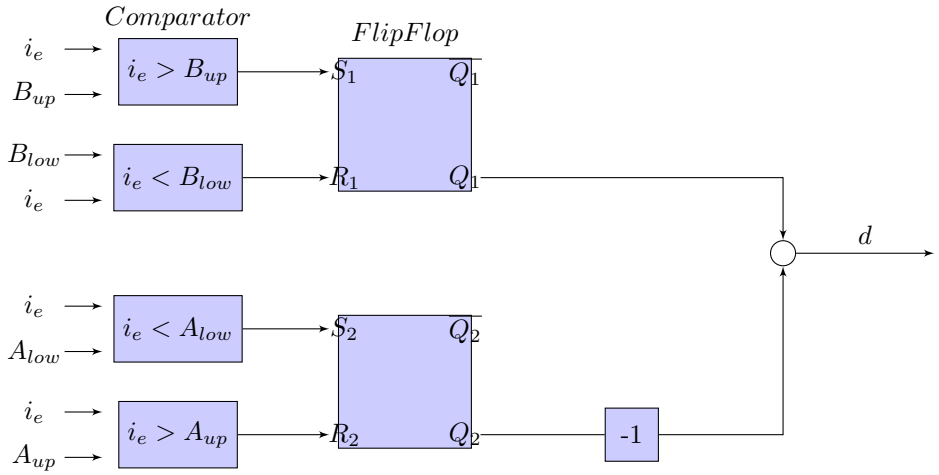


Figure 2.25: The three level hysteresis comparator

$$R_1 = \begin{cases} 1 & \text{if} i_e < B_{low} \\ 0 & \text{if} i_e > B_{low} \end{cases} \tag{2.86}$$

$$S_2 = \begin{cases} 1 & \text{if} i_e < A_{low} \\ 0 & \text{if} i_e > A_{low} \end{cases}$$

$$R_2 = \begin{cases} 1 & \text{if} i_e > A_{up} \\ 0 & \text{if} i_e < A_{up} \end{cases}$$

The flip flop is made up of AND and NOR logics and gives the output described in Table 2.1, where $\overline{Q}$ is the complement of Q. When the flip flop is in storage mode, that is when both S and R are low, Q and $\overline{Q}$ stays unchanged. If S becomes high while R stays low, Q becomes high and stays there even if S is going back to low. If R becomes high while S stays low, Q becomes low and stays there even if R is going back to low.

The output of the three level hysteresis is described by Table 2.2:

Table 2.1: Flip Flop

S	R	*Action*
0	0	Keep State
1	0	$Q = 1\overline{Q} = 0$
0	1	$Q = 0\overline{Q} = 0$
1	1	Not possible

Table 2.2: Output of three level hysteresis comparator

S_1	R_1	Q_1	S_2	R_2	Q_2	d
1	0	1	0	1	0	1
1	0	1	0	0	0	1
0	0	1	0	0	0	1
0	1	0	0	0	0	0
0	0	0	0	0	0	0
0	1	0	1	0	1	−1
0	1	0	0	0	1	−1
0	0	0	0	0	1	−1
1	0	1	0	0	1	0
0	0	1	0	0	1	0

The voltage Vector look up table

In the look up table the voltage space vector plane is divided into, not only 6 but, 24 sectors (Figure 2.26). This gives better accuracy and an improved choice of voltage vector. The choice of voltage vector is dependent on the angle of the dq-axis and the value of d_d and d_q as shown in Table 2.3. The switching frequency of this controller can further be reduced by choosing the zero voltage vector that is closets to the last switching vector used. This can be obtained by adding a memory of the last vector used in the look up table, and then a choice of the closest zero voltage vector. Hence only one of the switches has to change its state when choosing a zero voltage vector. This is described in Table 2.4.

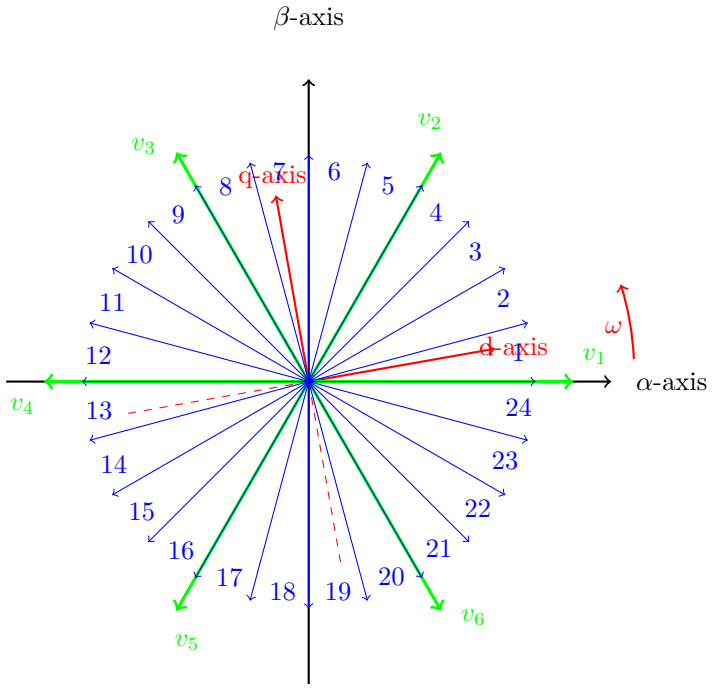


Figure 2.26: The Voltage Vector plane divided into 24 sectors

Table 2.3: Switching table for the *dq*-hysteresis controller

d		Sector																							
d_d	d_q	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
1	-1	v_2	v_2	v_2	v_3	v_3	v_3	v_3	v_4	v_4	v_4	v_4	v_5	v_5	v_5	v_5	v_6	v_6	v_6	v_6	v_1	v_1	v_1	v_1	v_2
1	0	v_1	v_1	v_2	v_2	v_2	v_2	v_3	v_3	v_3	v_3	v_4	v_4	v_4	v_4	v_5	v_5	v_5	v_5	v_6	v_6	v_6	v_6	v_1	v_1
1	-1	v_6	v_1	v_1	v_1	v_1	v_2	v_2	v_2	v_2	v_3	v_3	v_3	v_3	v_4	v_4	v_4	v_4	v_5	v_5	v_5	v_5	v_6	v_6	v_6
0	1	v_3	v_3	v_3	v_3	v_4	v_4	v_4	v_4	v_5	v_5	v_5	v_5	v_6	v_6	v_6	v_6	v_1	v_1	v_1	v_1	v_2	v_2	v_2	v_2
0	0	v_0	v_0	v_0	v_0	v_0	v_0	v_0	v_0	v_0	v_0	v_0	v_0	v_0	v_0	v_0	v_0	v_0	v_0	v_0	v_0	v_0	v_0	v_0	v_0
0	-1	v_6	v_6	v_6	v_6	v_1	v_1	v_1	v_1	v_2	v_2	v_2	v_2	v_3	v_3	v_3	v_3	v_4	v_4	v_4	v_4	v_5	v_5	v_5	v_5
-1	1	v_3	v_4	v_4	v_4	v_4	v_5	v_5	v_5	v_5	v_6	v_6	v_6	v_6	v_1	v_1	v_1	v_1	v_2	v_2	v_2	v_2	v_3	v_3	v_3
-1	0	v_4	v_4	v_5	v_5	v_5	v_5	v_6	v_6	v_6	v_6	v_1	v_1	v_1	v_1	v_2	v_2	v_2	v_2	v_3	v_3	v_3	v_3	v_4	v_4
-1	-1	v_5	v_5	v_5	v_6	v_6	v_6	v_6	v_1	v_1	v_1	v_1	v_2	v_2	v_2	v_2	v_3	v_3	v_3	v_3	v_4	v_4	v_4	v_4	v_5

Table 2.4: Selection of closest zero voltage vector

Previous vector	v_1	v_2	v_3	v_4	v_5	v_6
Switching state	001	011	010	110	100	101
Zero vector	v_0	v_7	v_0	v_7	v_0	v_7
Switching state	000	111	000	111	000	111

2.10 DC-link Voltage Controller

The focus for the project is on different current control structures. Even so, a VSC converter contains an outer DC voltage control loop that influences the stability of the system and should be included in the simulations. The outer voltage control loop is shown in Figure 2.27. The purpose of the DC-link is to act as a filter for the time-variant Power Supply e.g. a Wind Turbine, to give a time invariant power supply to the grid [8]. The switches in the converter are assumed lossless. By the use of equation 2.10 and assuming the voltage vector to be synchronized with the *dq*-reference frame, the DC-current can be written as in Equation 2.87.

$$I_{DC} = \frac{3}{2}\frac{v_d}{V_{DC}} i_d \tag{2.87}$$

$$C\frac{dV_{DC}}{dt} = \frac{3}{2}\frac{V_d}{V_{DC}} i_d - i_L \tag{2.88}$$

Since this equation is non-linear it is linearized around the operation point of

steady state conditions by use of the first segment in a Taylor series expansion for non-linear functions. Equation 2.87 is then reduced to:

$$C\frac{d\Delta V_{DC}}{dt} = \frac{3}{2}\frac{v_{d,0}}{v_{DC,ref}}\Delta i_d \tag{2.89}$$

Applying Laplace transform on Equation 2.89

$$\frac{\Delta V_{DC}(s)}{\Delta i_d(s)} = \frac{3}{2}\frac{v_{d,0}}{v_{d,ref}}\frac{1}{sC} \tag{2.90}$$

By using the equations for the pu-system described in chapter 2.2, the DC current can be written:

$$i_{DC,pu} = \frac{vd,pu}{v_{DC,pu}} i_{d,pu} \tag{2.91}$$

During dynamic behavior will the dc link voltage in pu-representation be:

$$v_{DC,pu}(s) = \frac{\omega_b C_{pu}}{s}[i_{dc,pu} - i_{L,pu}] \tag{2.92}$$

For design of the voltage controller the inner closed current control loop is represented as a 1. order time delay function [30]. Where $T_{eq} = 2T_a$.

To compensate for the current disturbance i_L the controller is added a feed forward loop of this current. The block diagram of the outer voltage control loop is shown in Figure 2.27, and the open loop transfer function becomes as in equation 2.93.

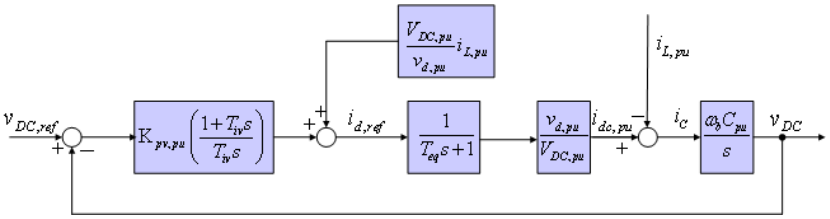


Figure 2.27: Block diagram of the dc-link voltage control loop

$$G_{v,ol} = K_{pv,pu}(\frac{1+T_{iv}s}{T_{iv}s})\frac{1}{1+T_{eq}s}[\frac{v_{d,pu}}{V_{DC,pu}}\frac{\omega_b C_{pu}}{s}] \tag{2.93}$$

2.10.1 Tuning the DC-link voltage controller

By using the symmetrical optimum criteria the parameters of the controller can be determined, as in equation 2.94 and 2.95. The derivation of the symmetrical optimum is shown in the Appendix C.

$$T_{iv} = a^2 T_{eq} \tag{2.94}$$

$$K_{pv,pu} = \frac{T_C}{aKT_{eq}} \tag{2.95}$$

Where

$$T_C = \frac{1}{\omega_b C_{pu}} \tag{2.96}$$

and

$$K = \frac{v_{d,pu}}{v_{dc,pu}} \tag{2.97}$$

As seen from the derivation in the appendix the constant a define the placement of the poles of the closed transfer function of the system. Thus the choice of a define the behavior of the control loop.

Chapter 3

System Design

3.1 System component design

3.1.1 LCL-filter parameters

The system parameters are chosen to be as in Table 3.1, which could represent a typical wind-generation configuration.. The switching frequency (f_{sw}) of the converter is set to 3 kHz for the linear controllers (PI-controller and PR-controller). For the nonlinear control structures (Hysteresis controllers) the switching frequency of the converter is not constant, but the band is chosen to give an average switching frequency close to 3 kHz.

Since the PI-current regulator tuning is based on the parameters of the LCL

Table 3.1: System parameters

Parameter	*Value*
S_n	2.5 MVA
$V_{n1,RMS}$	690 V
I_{n1}	2.091 kA
f_n	50 Hz
V_{DC}	1.2 kV
f_{sw}	3000 Hz

Table 3.2: Filter parameters

Parameter	*PU-Value*	*Value*
L_1	0.05 pu	30.309 μH
C_f	0.10 pu	1671.4 μF
R_f	0.00109 pu	0.2 mΩ

Table 3.3: Filter Characteristics

Parameter	*PU-Value*	*Value*
f_{res}	15.78	$789Hz$

filter, the parameters of the filter should first be found. In Section 2.3.4 a method for designing the filter is proposed. Since the objective of this project is to compare different current control structures the filter could be designed for ease of analyzing rather than designing the optimum filter.

The inductor in the filter is chosen, so that the voltage drop over the inductor is 5%. This is the same as choosing a $0.05pu$ inductor. The inductor on the grid side of the filter is included in the transformer and the line inductance. For comparing the different control strategies the load inductance will be changed and therefor also the resonance frequency of the filter. The capacitor in the filter is chosen so the reactive current is reduced by 10%, this gives a 0.1 pu capacitor. Table 3.2 shows the chosen values of the filter.

Operating under the circumstances described in Table 3.1 and Table 3.2, gives the resonance frequency of the filter shown in Table 3.3.

3.2 Controllers Design

If nothing else is mentioned, the controllers are designed as described in this section, for the simulations performed in this survey.

Table 3.4: PI Control Parameters

Parameter	*Value*
$K_{p,pu}$	0.475783934
τ_i	0.1457185 sec
ω_b	576 Hz
ξ	0.70763
ω_n	$4239.45 \frac{rad}{sec}$

3.2.1 PI Current Controller Parameters

Based on the LCL-filter parameters, the parameters in the PI current controller is determined, as shown in Table 3.4 based on the description of tuning of the PI controller presented in Section 2.6.2.

The open loop transfer function for the VSC, if not including the inductance in the grid, becomes as shown in Equation 2.65. By using the parameter presented, the bode plot becomes as in Figure 3.1.

This gives a stable system with a phase margin of $65.6 degrees$ at $2.72 \cdot 10^3 \frac{rad}{sec}$.

The design parameters of the PI controller are verified by Figure 3.2, that shows the time response when the converter is connected to a stiff grid. To remove the ripple given by the switches in the converter, this figure is simulated by use of a average PWM model. Figure 3.2 shows: Maximum overshoot, $M_p = 1.035$ pu, the time at maximum overshoot, $t_p = 0.00152$ s, and settling time, using the 2% criteria, $t_s = 0.0019$ s. The 2% criteria is defined as when the deviation for the response becomes smaller than 2%.

Dual PI controller Parameters

Since the inductance and the resistance are equal for the positive and negative sequence [34], the PI controller parameters for the negative sequence is the same as for the positive sequence and given in Table 3.4. The only different in the negative sequence controller is the change in polarity for the feed forward loop of the rotational induced voltages. Given from the negative rotational direction of the negative sequence reference frame. To obtain separate synchronous frame currents, the measured current must be separated into the two sequences. The dual PI controller that uses the PLL with notch-filter uses a notch filter to

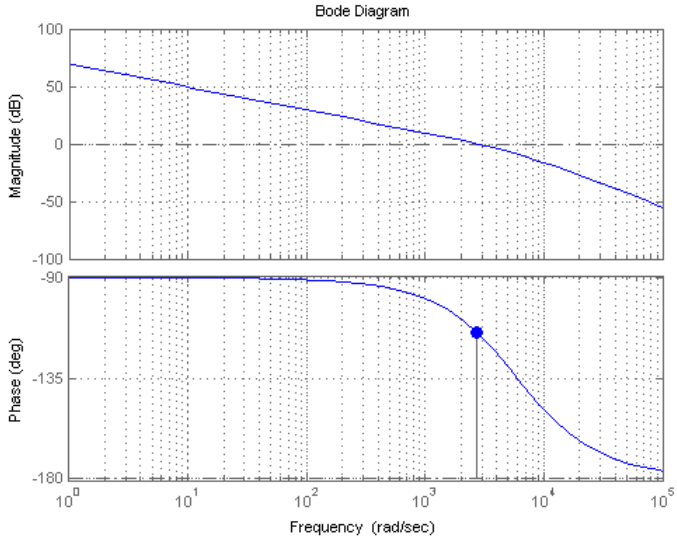


Figure 3.1: Bode plot of the open loop transfer function, Equation 2.65

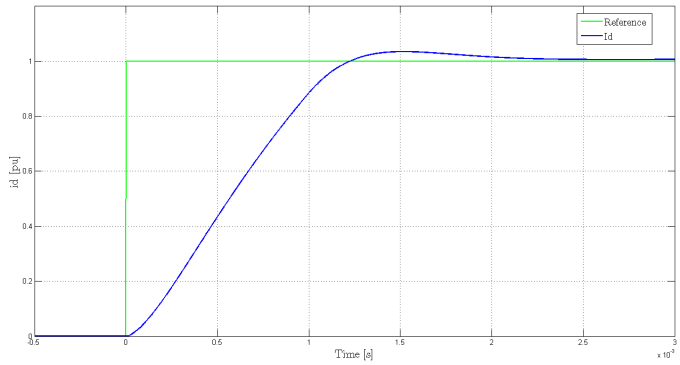


Figure 3.2: PI controller, step response in i_d when connected to a stiff grid

Table 3.5: PR-Control parameters

Parameter	*Value*
$K_{p,pu}$	0.475783934
K_i	3.27
ω_0	314.159 $\frac{\text{rad}}{\text{sec}}$

separate the currents. The dual PI controller that uses the DDSRF-PLL uses the DDSRF-algorithm to separate the currents in the simulations.

3.2.2 PR Current Control Parameters

The PR controller is as described in Section 2.8 based on the PI-controller in the dq-reference frame. Since this control structures parameters are designed based on the PI-controller for the synchronous reference frame, and transformed into stationary $\alpha\beta$- reference frame, the values of the PR-controller should be the same as the PI-controller. The parameters are shown in Table 3.5.

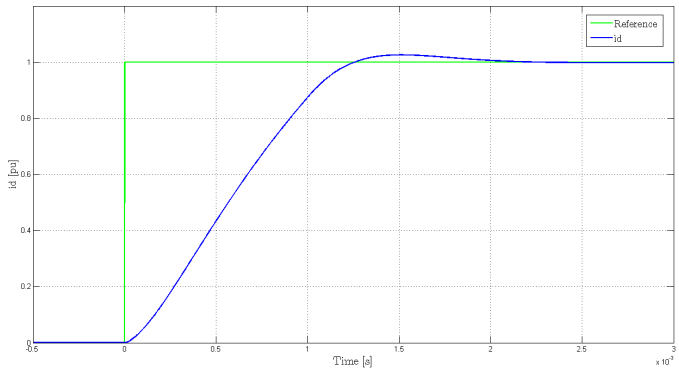


Figure 3.3: PR controller, step response in i_d when connected to a stiff grid

As the same reason as for the PI time response, Figure 3.3 shows the step response when the PR controller is simulated with a average PWM model.

The figure shows: Maximum overshoot, $M_p = 1.0255$, the time at maximum overshoot, $t_p = 0.00151$ s, and settling time, using the 2% criteria, $t_s = 0.0017$.

Under unbalanced conditions, the PR controller uses the double decoupled synchronous rotating reference frame PLL that is described in Section 2.4.3.

3.2.3 Hysteresis Current Control Parameters

Since the hysteresis controller is a non linear controller, the switching frequency is not constant. The aim is to compare different control structures and it should be aspired to have the same working conditions for the VSC. This means to achieve approximately the same switching frequency of the transistors. Since the switching frequency for the linear controllers is 3 kHz the width of the hysteresis band is chosen so that the average switching frequency is approximately the same, given by Equation 3.1 [38].

$$ASF = \frac{N_s}{T} \tag{3.1}$$

Where N_s is the number of switchings in one fundamental period and T is the time of one fundamental period. The width of the hysteresis band is by trial and error and Equation 3.1 calculated to $+/-16\%$. Since the switching states are generated directly from the current divagation it is not possible to simulate the hysteresis controller by use of a average PWM model. Figure 3.4 show the time response when the controller is connected to a stiff grid.

As seen in the figure the current ripple exceeds the hysteresis band. This comes from the interaction between the three phases. The dq-response is added in Appendix F.1.1 in Figure F.1 together with the response in the three phases current in Figure F.2 to visualize this interaction.

Hysteresis Controller for Control under Unbalanced Conditions

The two level phase current hysteresis controller is more or less the same for additional control of the negative sequence current. The difference will be in the PLL, which is the PLL that decouples the positive and negative sequence, to separate the angles of the two sequence voltage vectors. The negative sequence current reference is then added to the positive sequence current reference according to Figure 3.5.

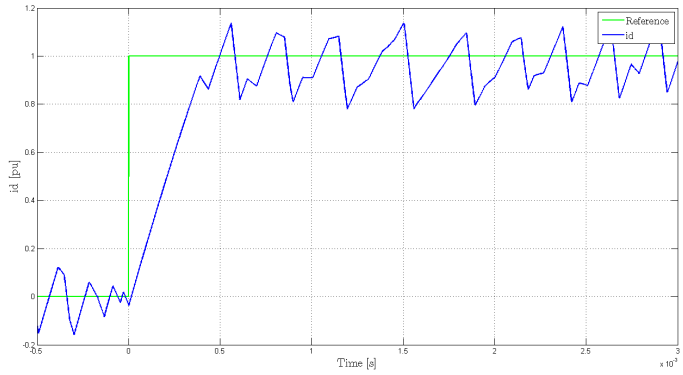


Figure 3.4: Phase current hysteresis controller, step response in i_d when connected to a stiff grid

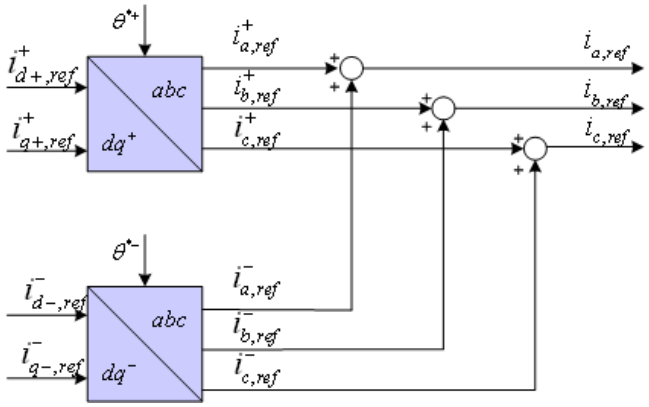


Figure 3.5: Positive and negative current reference in phase current hysteresis controller

3.2.4 Three level dq-Hysteresis controller

The design of the band at the hysteresis controller is based upon the band in the phase current hysteresis controller and to give approximately the same current ripple. Thus the inner band is chosen equal to the phase current hysteresis

band 16%. The maximum peak of the current that may occur in a phase current hysteresis controller is two times the size of the band caused by the interaction between the three phases [7]. Hence the outer band of the dq-Hysteresis controller is designed to give a maximum peak that is two times the inner band. Since the current error in the dq-hysteresis controller is kept within a square as shown in Figure 2.24, the outer band limit will consequently be $\sqrt{2}$ times the inner band, 22.62%. Figure 3.6 shows the step response of the three level dq-hysteresis controller when the VSC is connected to a stiff grid. Where the red plot shows the dq-hysteresis controller with fixed zero-voltage vector and the blue plot shows the dq-hysteresis controller with selection of zero-voltage vector. The slightly difference are mainly caused by that the results plotted does not reflect the exactly same non-zero switching actions, since the hysteresis controllers are extremely sensitive to the initial conditions due its chaotic nature.

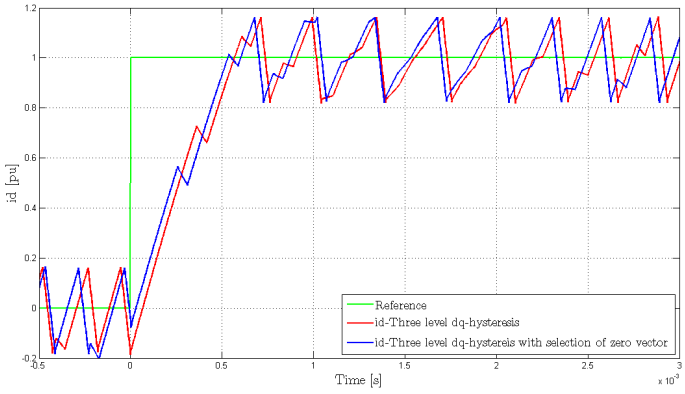


Figure 3.6: dq-Hysteresis controller, step response in i_d when connected to a stiff grid

Three level dq-Hysteresis Controller under Unbalanced Conditions

Since the three level hysteresis controller is controlled by choosing the appropriate voltage vector, based upon the position of the dq-reference frame, the negative sequence current reference is then seen as a rotational vector of two times the fundamental frequency by the hysteresis controller. The negative se-

quence reference must therefor be transformed into the positive sequence, which is done according to Figure 3.7.

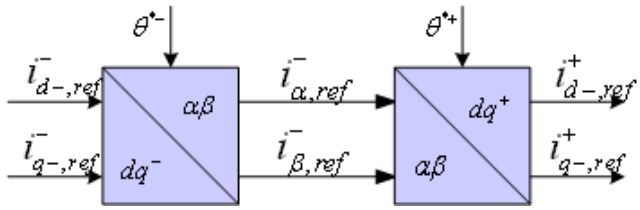


Figure 3.7: Negative sequence reference

3.2.5 DC-link Voltage Controller Parameters

The DC-link controller is designed according to the symmetrical optimum criteria as described in Section 2.10.1. In addition to this there exists some constrains to the gain of the DC-link controller. One is that the cross frequency of the DC-link control loop should be 10 times lower than the cross frequency of the current control loop [30]. By choosing the time delay of the inner control loop to be represented by a time delay of $2T_a$ and tuned according to the symmetrical optimum, the cross frequency of the outer control loop becomes as in Equation 3.2, 2121 $\frac{\text{rad}}{\text{sec}}$. An additional time delay is therefore added into the representation of the inner control loop, chosen to give the cross frequency of the DC-link voltage controller to be 1 decade lower than the cross frequency of the inner current control loop. Hence T_{eq} is chosen equal to 1.179245 ms.

$$\omega_{n,DC} = \frac{1}{2T_{eq}} \tag{3.2}$$

Another limitation of the DC-link controller is that it can not have much overshoot in its response. Since the lower value of the DC-link voltage can not be below $\frac{2\sqrt{2}}{\sqrt{3}}V_{LL}$ 2.14, and a upper voltage limit with respect to the maximum voltage for secure operation to prevent breakdown. Hence the value of a is chosen to be 3. Based on the DC-link capacitor given in Table 3.6, the parameters of the DC-link controller is given in Table 3.6. This give the open loop transfer function bode plot as shown in Figure 3.8, and the step response in a stiff grid as shown in Figure 3.9.

Table 3.6: DC-link controller parameters

Parameter	*Value*
C_{DC}	50000 μF(0.124 pu)
a	3
T_{iv}	10.6 ms
K_{pv}	7.2758
$\omega_{n,DC}$	420 $\frac{\text{rad}}{\text{sec}}$

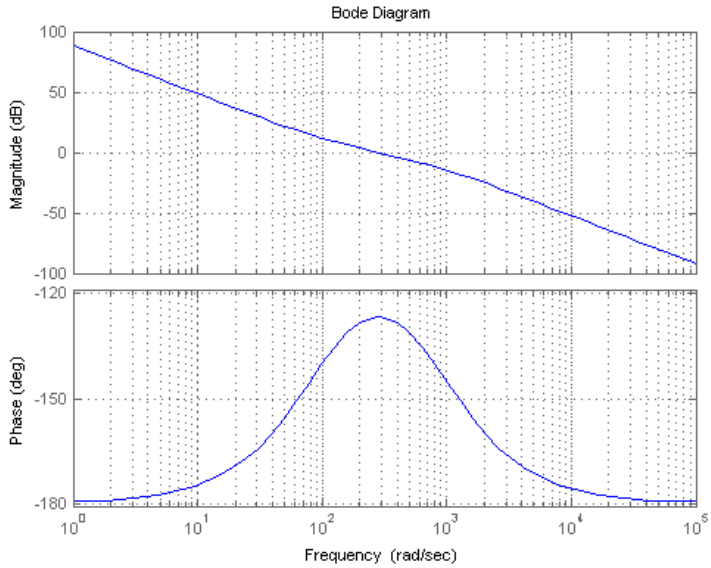


Figure 3.8: Bode plot of DC-link open loop transfer function

3.2.6 Tuning of the Phase Locked Loop

As described in Section 2.4.2 the PI controller in the PLL is tuned after the symmetrical optimum criteria, based on the filter time constant that attenuates the noise and harmonics in the measured voltage. The filter time constant is

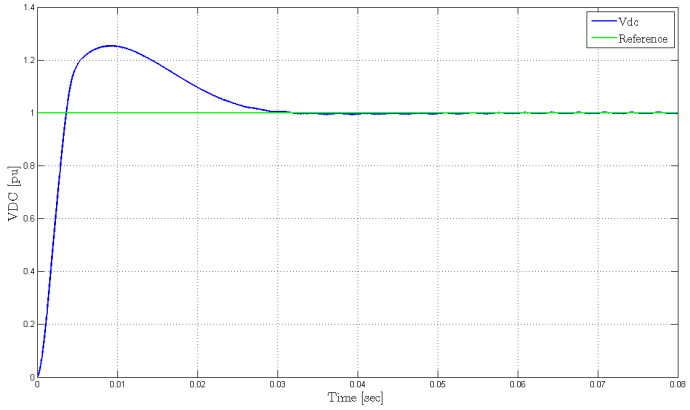


Figure 3.9: Step response in V_{DC} when connected to a stiff grid

Table 3.7: PLL PI control parameters

Parameter	*Value*
$T_{f,PLL}$	1 ms
$K_{p,PLL}$	50.3
$T_{i,PLL}$	10 ms

chosen as described in [16], and the design parameters are shown in Table 3.7. The value of a is chosen to be $\sqrt{10}$.

The simulations shows that the tuning of the PLL is of great importance for how the current controller acts in a weak grid. Therefore an additional PLL tuning is used in several simulations. The parameters of the PLL are then changed by having a stronger filtering effect on the measured voltage that will limit the influence of the converter operation to the synchronization with the filter time constant equal to 5 ms. The controller parameters are then tuned with the same value of $a = \sqrt{10}$. When ever the PLL is tuned slower, it will be noticed. The default is hence a PLL tuned with parameters shown in Table 3.7.

Notch Filter Parameters

The notch filter is designed with a $Q = 10$ which gives the bode plot stop band shown in Figure 2.13, and removes signals at a frequency of twice the line voltage fundamental frequency. In addition, a low pass filter, with same filter time constant as the conventional PLL, to filter out the noise and harmonic in the measured current is added, giving the same tuning of the PLL as described in Table 3.7.

Decoupled Dual Synchronous rotating reference PLL frame parameters

The low pass filter that is used to calculate the average value of the positive and negative synchronous rotating reference frame voltages for decoupling, is for the case of comparison with the other PLL used in this thesis chosen to be equal to the filter in Table 3.7, which again gives the same tuning of the PLL as described in Table 3.7. As it will be shown by the simulation, this tuning of the PLL will be unstable for the decoupled dual synchronous rotating reference frame PLL, and the parameters and the filter are then tuned five times slower, which is named the slow PLL in this thesis. Hence $\omega_f = 200$ Hz in Equation 2.53.

3.3 Active Damping

The active damping algorithm is damping the resonant frequency of the grid. As seen from Equation 2.20 the resonance frequency is dependent of the impedance in the grid. The High Pass filter should also be outside the band width of the system. Based on these two constrains the time constant of the active damping is determined to be: T_α 0.00143 sec (700 Hz). Figure 3.10 show the relationship between the grid impedance and the resonance frequency of the LCL filter. It doesn't exists much theoretical work on how the active damping should be implemented in a control system for unbalanced grid. But it should be noticed that the voltages used for active damping should be the positive sequence with the influence of the negative sequence removed, unless it can influence the control system to behave poorly. This is found out by trial and error and is not theoretically proven.

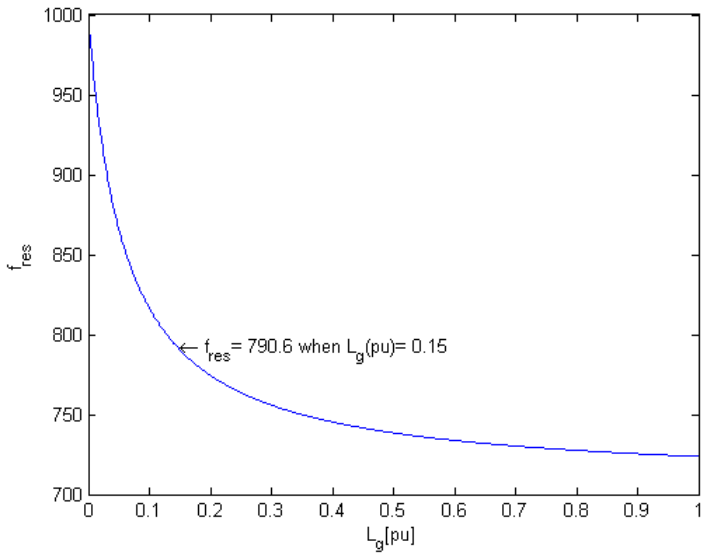


Figure 3.10: The resonance frequency as a function of the grid impedance

3.4 The Overall Control System

Figure 3.11 shows the overall control system. The current control and modulation block is an assembly block of the control structures presented in this thesis. The control system is in this figure shown with the outer DC-link voltage controller, but for the major part of the simulations this control loop is not added into the system. During these simulations the DC-link is represented with a constant DC-voltage source. The figure also includes the simple grid thevenin equivalent.

3.5 The Simulink Model

The mathematical expressions of the state space model are analyzed by a Simulink model. The presented sub-state-space models are linked together as shown in Appendix, Figure D.1. It is a pu model, and all the components, and inputs are given in pu values. The tuning of the components in the control struc-

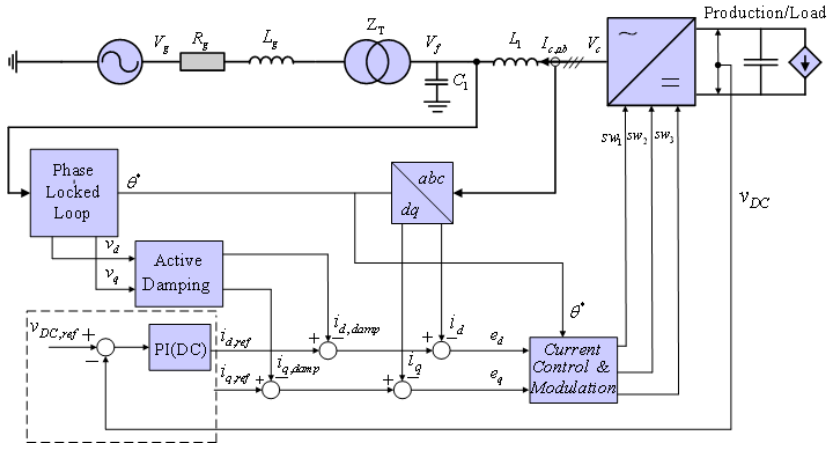


Figure 3.11: The overall control system

ture will be the same as for the PSCAD simulation model. The whole system operates in the dq-reference frame, except the PLL which uses the transformation from the stationary reference frame into the synchronous reference frame as a part of the feed back in the control loop, and the grid voltage input which transforms its inputs from the stationary reference frame to the synchronous reference frame. That the system includes these transformation is the main drawback for stability and dynamic analysis, since it becomes a highly non-linear time variant system. It should be noticed that the DC-link voltage in the state-space model is a constant value. In the real system there will be a limit for this value when the converter goes into over modulation. The DC-link voltage limitation is therefore in the simulink-model represented as a constant that will go into saturation at a given voltage. Since the clark and park transformation is a part of the PLL, and not included in the state space model, this linearized model will be an extreme simplification that will not give a sufficient behavior. In the simulations of the state space model performed in simulink, the park transformation is added to give correct information of the estimated angle from the PLL.

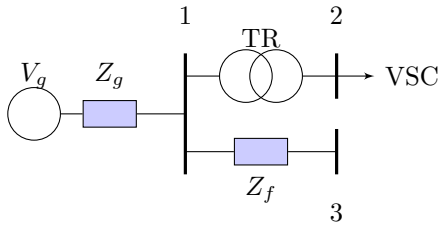


Figure 3.12: Single-line model for dip analysis

Table 3.8: Type of transformers

Type	*Transformer Connection*	*Description*
Type 1	Grounded $Y(gr.)Y(gr.)$	Does not change anything
Type 2	Y/Y(at least one side not gr.), Δ/Z	Removes zero sequence
Type 3	Δ/Y, Y/Δ, Y/Z	Swaps line and phase voltages

3.6 Simulation Cases

To give a good basis for the evaluation and comparison between the control structures and their performance in a weak grid, the system should be analyzed under different conditions. This sections describe some situations that occurs in a power system.

3.6.1 Classification of Voltage Dips

A voltage dip is the voltage experienced at the the terminal of the VSC due to a short circuit fault at a point in the electrical network. The single-line diagram in Figure 3.12 describes the network. Depending on the type of transformer, the fault at bus 1 may change at the terminal of the VSC (bus 2). The classification of the transformers type, and a short description of what they do with the voltage is shown in Table 3.8.

There exists seven types of unbalanced voltage dips [5]. The classification of

Table 3.9: Transformation of voltage dip, through transformer

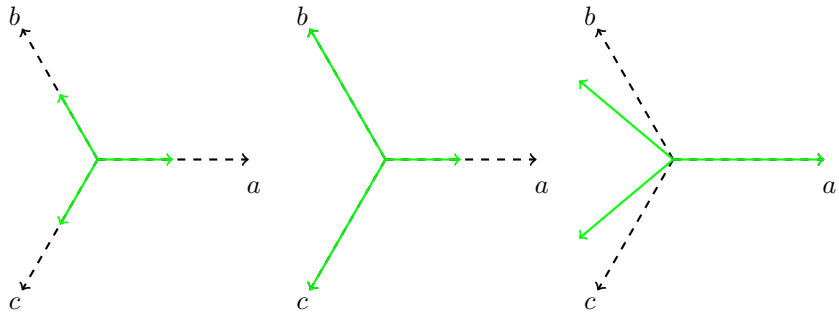
TRF Type	Dip on primary side						
Dip Type	A	B	C	D	E	F	G
Type 1	A	B	C	D	E	F	G
Type 2	A	D*	C	D	G	F	G
Type 3	A	C*	D	C	F	G	F

the three phase voltage dips are based on the following assumptions:

- Positive- and negative-sequence impedances are identical
- The zero-sequence component of the voltage does not propagate down to the terminal of the VSC, so we can consider phase to neutral voltages
- Load current, before, during and after the fault can be neglected

The seven faults and how they appear at the secondary side of the transformer, depending on the transformer and the fault, is shown in Table [27].

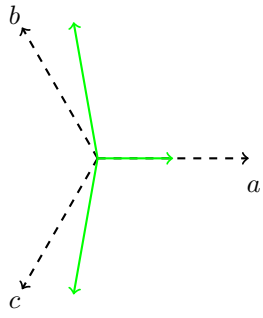
The short circuit faults that gives the seven types of fault is either three-phase fault, single phase to ground fault, phase to phase faults, or double phase to ground faults. The transformer in this project is a Δ/Y transformer, and we normally find five types of faults at the VSC terminal. Type A faults, due to three phase faults, type C and D due to single-phase and double-phase faults, and type F and G due to double-phase to ground faults. However can faults of type B and E occur if the fault is at the same side of the transformer as the VSC. [27].



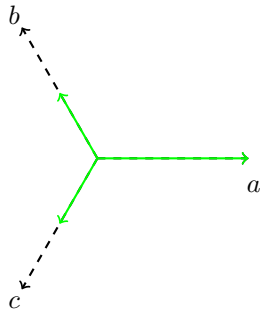
(a) Type A

(b) Type B

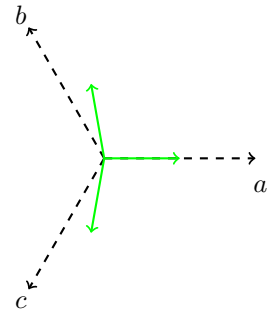
(c) Type C



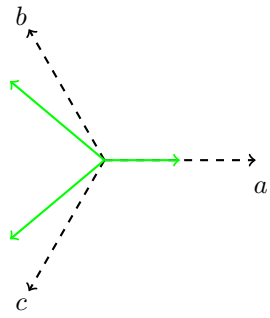
(d) Type D



(e) Type E



(f) Type F



(g) Type G

Figure 3.13: Classification of voltage dips

Chapter 4

Simulation and Discussion

The simulations are performed in the simulation tool PSCAD/EMTDC from Manitoba HVDC Research Center. PSCAD is the graphical user interface of the EMTDC simulation engine which solves differential equations using fixed time step calculations.

The simulations are performed with a fixed DC-link voltage to isolate the response of the current controllers from the outer controller loops dynamics. Some simulations are performed with a DC-link controller, and will be notified whenever this is the case.

To limit the visual disturbance from the current ripple, the current at the grid side of the filter is plotted. The LCL filter contains a capacitor of 0.1 pu, and will extract a reactive current of 10% of the value of the filter capacitor voltages. To represent the behavior of the current at the converter side of the filter, the extraction of the reactive current is compensated in the plotted figures in this report.

4.1 Operation of the Voltage Source Converter

4.1.1 Step Response when Connected to a Stiff Grid

The step response of the current controllers that are designed for a balanced grid is shown in Figure 3.2, 3.3, 3.4 and 3.6 in Section 3.2 for the PI-controller, the PR-controller, the phase current hysteresis controller and the three-level dq-hysteresis controller respectively.

Dual PI current Controllers

The dual current controllers control the positive and negative sequence separately, even though these sequences are only separated for the control perspective and not in the real circuit. Figure 4.1 and 4.2 shows the step response of the dual PI controller for respectively use of a notch filter and decoupling to separate the positive and negative sequence SRF components when the VSC is connected to a stiff balanced grid. The notch-filter controller uses notch filter for separation of the two SRF in both the measured current and in the PLL, and the dual PI controller with decoupling between positive- and negative sequence uses the decoupling algorithm for both the measured current and in the PLL.

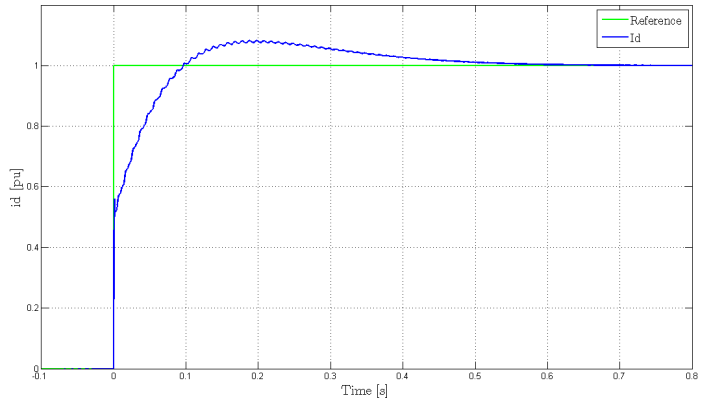


Figure 4.1: Step response in i_d^+ when connected to a stiff grid with dual PI controller with notch filter

Figure 4.1 shows: Maximum overshoot, $M_p = 1.0825$ pu, the time at maximum overshoot, $t_p = 0.1879283$ s, and settling time, using the 2% criteria, $t_s = 0.43313$ s. Figure 4.2 shows, $M_p = 1.149$ pu, the time at maximum overshoot, $t_p = 0.010247$ s, and settling time, using the 2% criteria, $t_s = 0.0166$ s. The dual PI controller that uses a notch-filter to remove the oscillations is significantly slower than all the other control structures. Also the dual controller that uses decoupling to remove the oscillations is slower than the control structures that are designed for balanced systems, but it tracks its reference faster than the notch-filter controller. Although there exists no negative sequence in

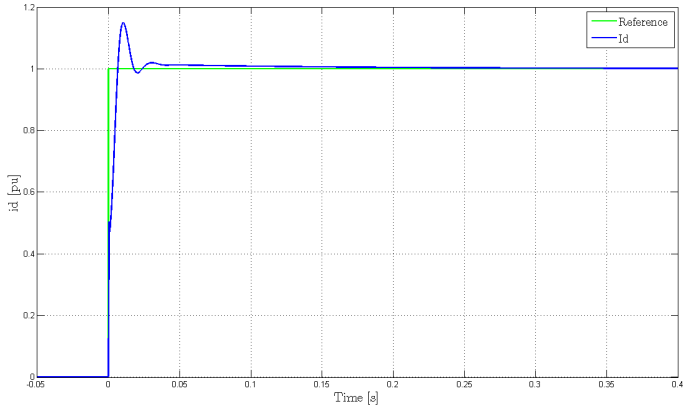


Figure 4.2: Step response in i_d^+ when connected to a stiff grid with dual PI controller with decoupling

the system when it is balanced, the dual current controllers controls the two separate sequences SRF currents. When the current in the positive sequence SRF has a step change to 1.0 pu the negative sequence SRF controller experience a 100 Hz oscillations that by time is removed from the notch-filter or the decoupling sequence. The negative sequence controller controls this oscillation to become zero, which in the real system will influence the positive sequence in the transient period giving a slower response. It should also be noticed that the PLL that decouples the positive and the negative sequence SRF becomes unstable when using the parameters used for conventional synchronous reference frame PLL. And hence in all the simulations with decoupled negative and positive sequence dual PI controller, the PLL is tuned five times slower than the parameters determined in Section 3.2.6.

4.1.2 Stability Limits at Zero Current Injection in Weak Grid

The inductance in the weak grid thevenin equivalent is increased until the system becomes unstable, while there is no current floating in the system. The results are shown in Table 4.1. The PLL is tuned according to Table 3.7

The controllers that decouples the positive and negative sequence, are also

Table 4.1: Stability limits with zero current injection

Controller	$L_g + L_t$ *(pu)*
PI	0.60 pu
PR	0.68 pu
Hyst-abc	< 1 pu
Hyst-dq	< 1 pu
Dual PI-notch	0.29 pu
Dual PI-dec.	–
PR PLL-dec	–
Hyst-dq, PLL-dec	–
Hyst-abc, PLL-dec	–

simulated with the PLL parameters as in Table 3.7 in this case. The table shows that even with no current in the grid, the system becomes unstable even if the grid is stiff. Hence Table 4.1 shows no stability limits for these controller systems.

4.1.3 Step response, when step change in $i^+_{d,ref}$ in a weak grid

To analyze the dynamic behavior of the current controllers in a symmetrical and balanced weak grid, the control structures are simulated with a step change in positive sequence d-axis current reference $i_{d,ref}$, while $i_{q,ref}$ is kept equal to zero. This is the same as a generator mode operation of the VSC. The weak grid is represented by an inductance, including the transformer inductance, of 0.2 pu and a resistance of 0.025 pu in the weak grid thevenin equivalent. All the parameters in the controllers are tuned as described in Section 3.2 and the response in d-axis current and the angle deviation from the synchronization for the different control structures are shown in Figure 4.3-4.11. The blue plots shows the response when the PLL is tuned as described in Section 3.2.6, while the red plots shows the case when the PLL is tuned five times slower.

The inductance in the grid is four times higher than the filter inductance. Hence the voltage over the filter capacitors are highly influenced by the operation of the converter itself. Since the filter capacitor voltage is the voltage that the converter uses to synchronize to the grid, also the synchronization signals is

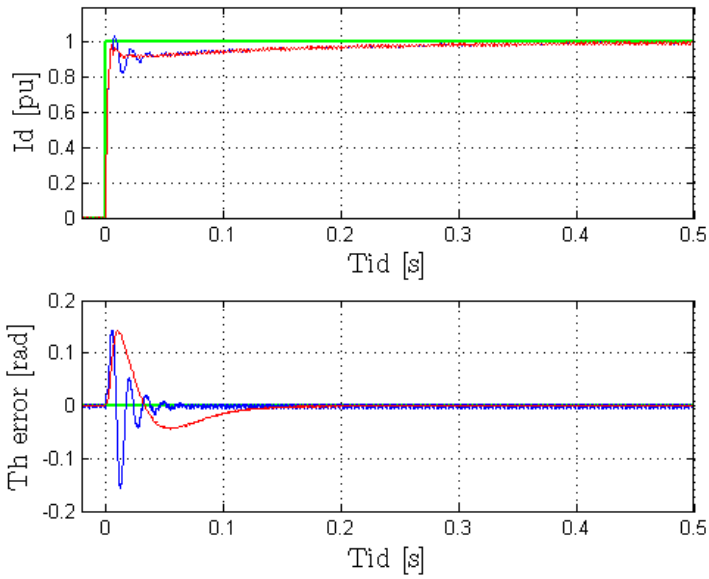


Figure 4.3: PI controller, step response in i_d^+ when connected to a weak grid

influenced by the operation of the converter. Therefore the information of the synchronization to the grid is of great importance to understand the dynamic behavior of the control structures. Table 4.2 is describing the maximum overshoot (M_p), the instant of maximum overshoot, (t_p) and the setting time using the 2% criteria (t_s) read from the figures.

The poorly damped oscillations in the PI controller, can also be seen in the phase angle deviation. The change in d-axis current is causing a change (Figure 4.12a and 4.12b) and oscillation in the filter voltage, used for synchronization and therefore also in the internal phase angle deviation. The d- and q- axis voltage components measured at the filter capacitors are used in the feed-forward loop and introduces a further disturbance to the current controller when the voltage is oscillating. The interaction between the PLL, the current controller and the voltage feed-forward loop is hence the main reason for the oscillatory response for the PI controller seen in the Figure 4.3. The feed forward loop and its influence on the current response is more thoroughly discussed in Appendix Section F.2.1

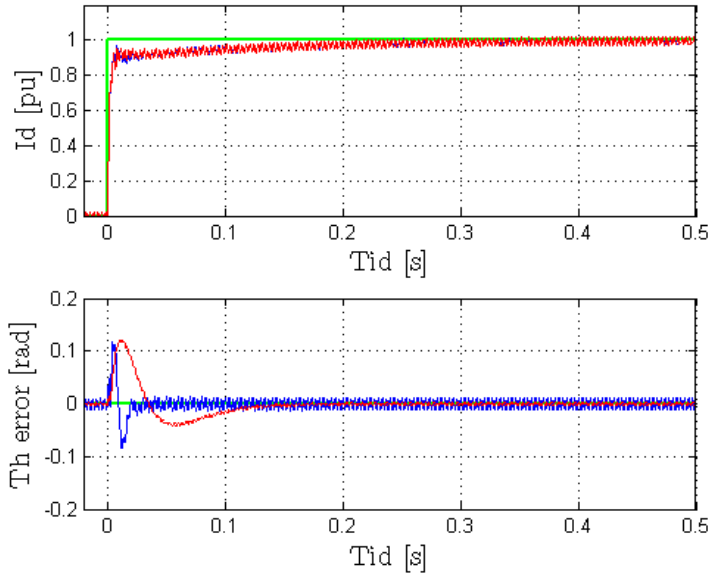


Figure 4.4: PR controller, step response in i_d^+ when connected to a weak grid

The PI controller and the PR controller are under ideal conditions analytically the same. This can be verified by the stiff grid response shown in Section 3.2. Hence the difference in the current response of the two controller shown in Figure 4.3 and 4.4 is not obvious. But the PR controller is only expected to give the same response as the PI controller for fundamental frequency signals. The angle estimated from the PLL is used to transform the reference values for the PR controller from the synchronous rotating reference frame into the stationary reference frame. The weak grid will therefore make the PR controller to transiently be operating outside the resonant frequency, which leads to a reduced gain and a more damped response. Since the PR controller has a reduced gain at frequencies that differs from the fundamental frequency, the interaction between the PLL and the PR controller is reduced, compared to when the current is controlled by the PI controller. After the transient period, there is a slow response for both the PR controller and the PI controller. This can possibly be explained by that the RL(τ)-time constant of the system has increased in the simplified transfer function in Equation 4.1 compared to the connection to a stiff

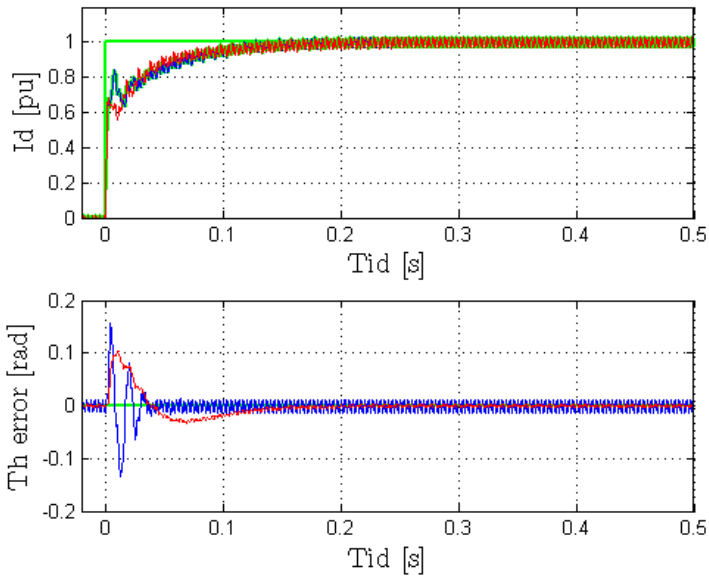


Figure 4.5: Dual PI controller with notch filter, step response in i_d^+ when connected to a weak grid

grid. The transfer function is simulated with a step response for the SRF-PI controller and added in Appendix, Figure F.6. It shows approximately the same settling-time.

$$H_{OL} = K_{p,pu}(\frac{1+s\tau_i}{s\tau_i})(\frac{1}{1+sT_a})(\frac{1}{r_{pu}})(\frac{1}{1+s\tau}) \tag{4.1}$$

This equation is an extreme simplification, since its point of synchronization now is addressed at the stiff grid, and it neglects the capacitor in the filter and the influence of the PLL. So there can also possibly be other reasons for the slow response of the current in the weak grid.

As the red plot shows, the interaction between the PLL and the current controllers is reduced when the PLL is tuned slower. The oscillations in the response when using the PI controller is as good as removed, and under these conditions the PI and PR controller gives close to the same result. Under this condition the influence of the PLL is reduced, and the PLL is having a strong

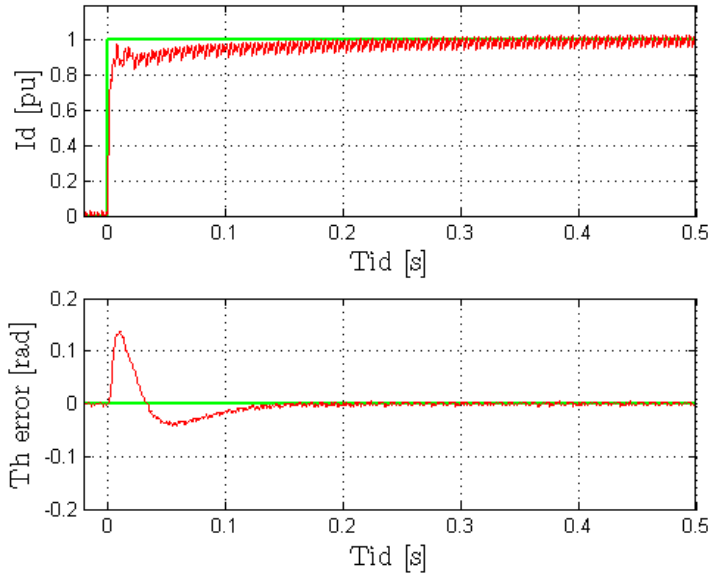


Figure 4.6: Dual PI controller, sequence decoupled, step response in i_d^+ when connected to a weak grid

filtering effect that limits the influence from the converter operation on the synchronization to the weak grid, and it will not see fast changes in the voltage phase angle.

The dual PI controller, that suppress the second order harmonics by using the notch filter, gives a significantly slower response than the other control structures in this survey. The negative and the positive sequence currents are separated with a notch filter. The step response of a notch filter is shown in the Appendix Figure F.3, and the influence of the negative sequence is first removed after 0.1 sec, which gives a slower response in the current as seen in Figure 4.5. Even so, the oscillations are the same as for the PI controller designed for balanced systems, and hence also the internal angle deviation in the PLL response corresponds to when the current is controlled by the single PI controller.

The Dual PI controller that decouples the negative and positive sequence, gives a much faster separation of the two sequences, leading to a more rapid current response than the dual PI controller with notch filter. The stability

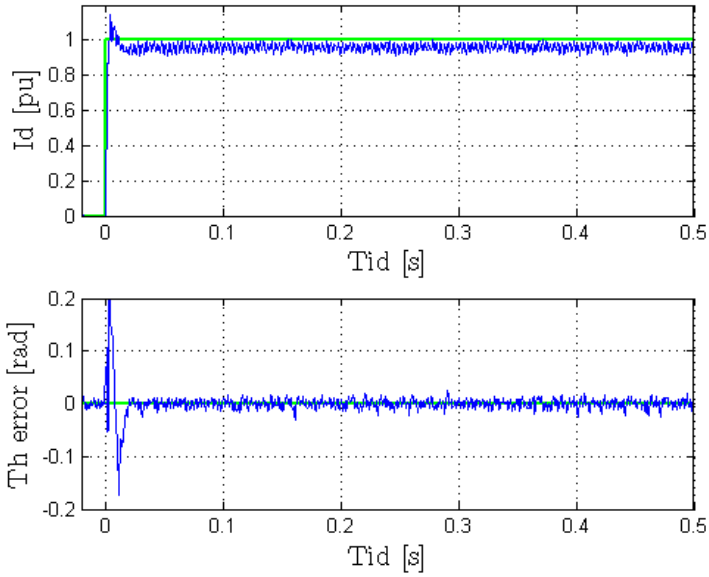


Figure 4.7: Phase current hysteresis controller, step response in i_d^+ when connected to a weak grid

limit of this control structure is lower than the inductance given in this section, as seen in Table 4.3. Hence the plot in Figure 4.6 shows only the case of the PLL to be tuned five times slower than described in Table 3.7.

As observed in Figure 4.9- Figure 4.11, the response of the PR controller and the hysteresis controller with a DDSRF-PLL give close to the same performance as the same current controllers with conventional PLL. A difference will however be shown if the voltage conditions should contain an unbalance. The control structures with the DDSRF-PLL would give almost the same result for a small unbalance in the grid, while the control structures with the conventional PLL would then contain a 100 Hz oscillation. This is shown with a comparison between the PR controller with a DDSRF-PLL and with a conventional PLL for a step change in the positive sequence d-axis current during a small grid unbalance in Appendix, Figure F.7.

The Hysteresis controllers gives a quick response with low oscillations and a small overshoot. There is a small steady state error that comes from the fact

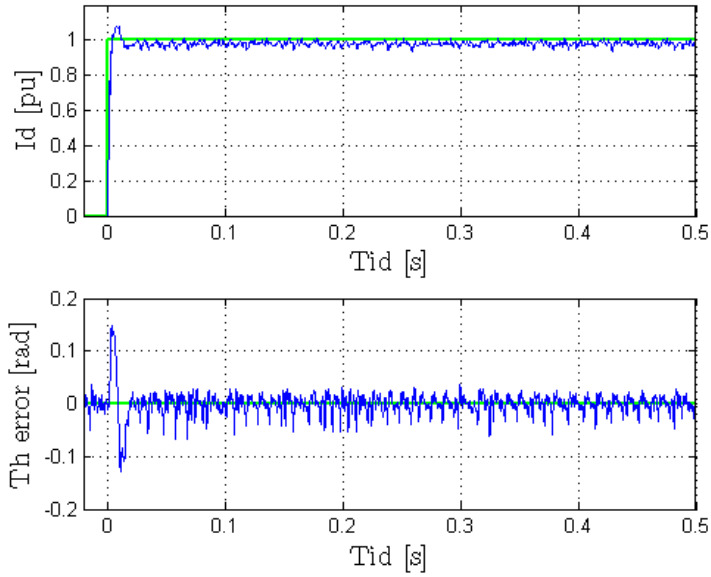


Figure 4.8: Three level hysteresis-dq controller, step response in i_d^+ when connected to a weak grid

that the hysteresis controller is not controlling the average value of the current, but the maximum deviation from its reference value.

The state space model

Equation 4.1 assumes ideal performance of the PLL, and does not take into account the interaction between the current controller and the PLL. And hence the response will give no oscillations. To describe the system fully also the PLL must be included.

The state spaced model presented in [22] and modified in this thesis, includes the influence of the PLL. The state space model is used as basis in a Simulink model. This model is also a simplification of the real system, since it uses the estimated frequency in the modulation of the LCL-circuit. Even so, it is to a certain extent including the interaction between the PLL and the current controller. Figure 4.13 shows the step response of a step change in the d-axis

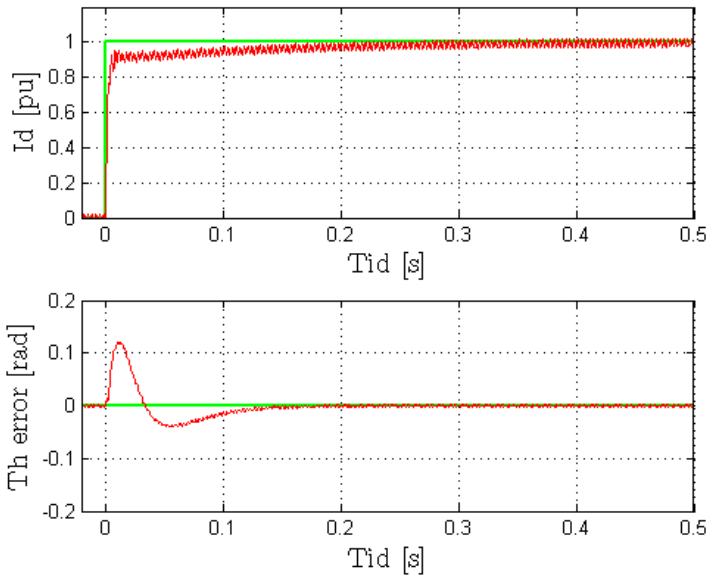


Figure 4.9: PR controller, PLL sequence decoupled, step response in i_d^+ when connected to a weak grid

current reference under the same conditions as in the PSCAD-simulations, where the blue graph shows the response when the PLL is tuned as described in Table 3.7 and the red graph shows the response when the filter and the tuning of the PLL is five time slower.

Since the state space model is taking into account the transient behavior of the control system, this can be used as a basis for the pole placement of the current control system in a weak grid. But the overall system is nonlinear and needs to be linearized around an operation point. The PLL itself is also a nonlinear time variant system where the control structure itself is used for the transformation from the stationary reference frame into the synchronous reference frame. If the PLL is to be linearized, some critical information will be lost, and the system description will not be sufficient. Hence, to get analytical results for the current control of the voltage source converter in connection with a weak grid where the point of synchronization is influenced by the operation of the converter itself, a method for solving this phenomena is necessary. This

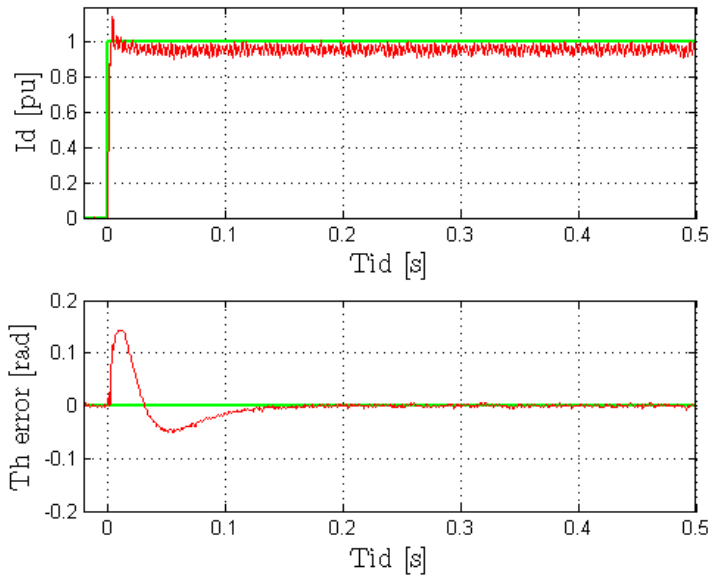


Figure 4.10: Phase current hysteresis controller, PLL sequence decoupled, step response in i_d^+ when connected to a weak grid

is not done in this thesis, but it can possibly be achieved by a state space representation in the dq-reference frame only. Since the analytical expression is not sufficient to describe the dynamic behavior of the system, the discussion in this thesis is based upon observation from the time-domain simulations.

Stability limits for the control structures

To further analyze the influence of a weak grid, the control structures are simulated with the step change in $i_{d,ref}^+$ as for the simulations in section 4.1.3, and the inductance in the grid is increased until a point of instability occurs. The stability limits are shown in Table 4.3.

To describe the stability limits, a starting point can be the dynamics observed in Section 4.1.3, and the interaction between the PLL and the current controller in the transient period of the response. The PR controller has the highest stability limits of the controllers. This can be described by comparing

Table 4.2: Results from simulations

Controller	M_p	t_p	t_s
PI	1.033 pu	8.3 ms	0.2016 s
PR	0.970 pu	8.3 ms	0.1317 s
Phase Current Hysteresis	1.076 pu	8.1 ms	0.025 s
Three level dq-Hysteresis	1.063 pu	7.9 ms	0.02427 s
Dual PI with notch filter	0.843 pu	82.9 ms	0.127 s
Dual PI with sequence decoupling	0.975 pu	8.8 ms	0.115 s

Table 4.3: Stability limits when step change in $i_{d,ref}$

Controller	$L_g + L_t$ *(pu)*	*Slow PLL*
PI	0.31 pu	0.72 pu
PR	0.46 pu	0.84 pu
Hyst-abc	0.41 pu	0.81 pu
Hyst-dq	0.42 pu	0.80 pu
Dual PI-notch	0.29 pu	0.41 pu
DDSRF-PI.	–	0.43 pu
PR, DDSRF-PLL	–	0.86 pu
Hyst-abc, DDSRF-PLL	–	0.85 pu
Hyst-dq, DDSRF-PLL	–	0.84 pu

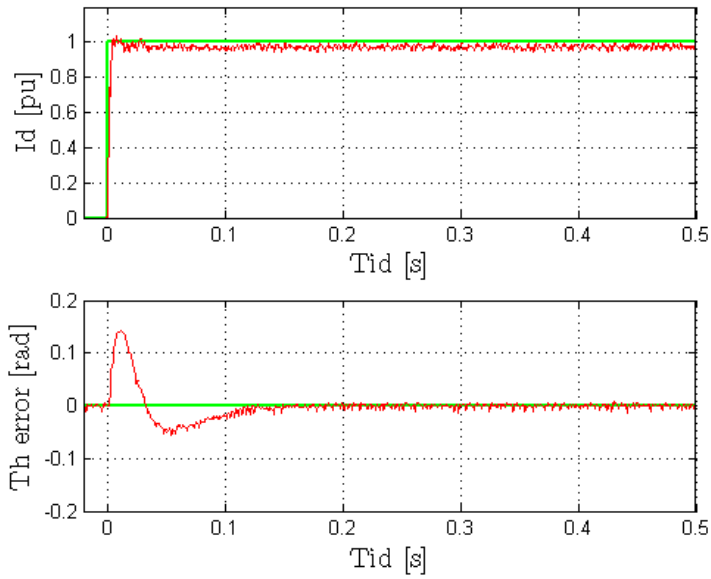
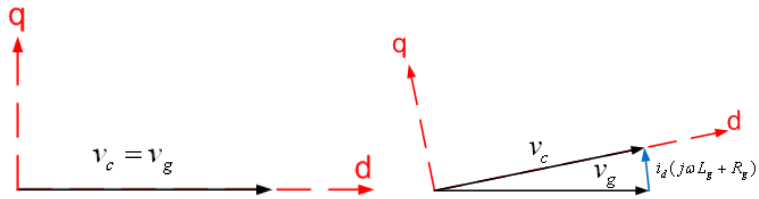


Figure 4.11: Three level hysteresis-dq controller, PLL sequence decoupled, step response in i_d^+ when connected to a weak grid

the PI controller and the PR controller. As observed in Figure 4.3 the use of the PI controller results in an oscillatory response with relatively poor damping. As described in 4.1.3 this comes from the interaction between the PLL and PI controller. As the inductor in the weak grid increases, a change in current gives a larger change in measured voltage and the oscillation in the instantaneous angle estimate and in the current response becomes more prevailing. At the stability limits the interaction between the PLL and the current controller results in an undamped oscillation. The PR controller has, as described, a reduced gain at frequencies that differs from the line voltage fundamental frequency. This reduces the interaction between the PLL and the current controller. Hence the stability limit is higher for the PR controller compared to the PI controller. As Table 4.3 shows, the PR controller also has a higher stability limit than the Hysteresis controllers. As for the PR controller, the Phase current Hysteresis controllers are only indirectly influenced by the the PLL, as it uses the angle estimate from the PLL to transform the current reference from the synchronous



(a) Steady state voltage at $t < 0$ (b) Steady state voltage at $t > 0$

Figure 4.12: Change in voltage at change in current

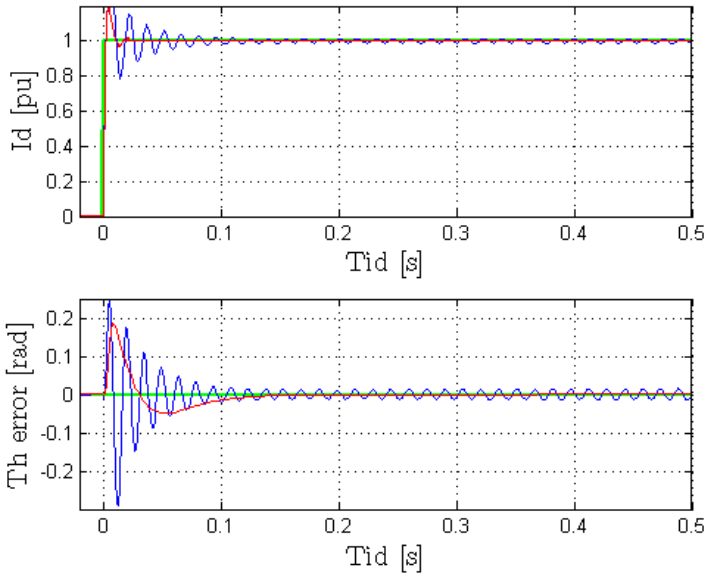


Figure 4.13: State space model with step change in $i_{d,ref}$

rotating reference frame into the stationary reference frame. But unlike the PR controller, the phase current hysteresis controllers response time is not influenced by the transient state of the PLL. This will give a high overshoot in the transient response of the internal angle deviation of the PLL. If the angular error of the PLL becomes significant, the reference in the stationary reference

frame becomes distorted and the system gets unstable. The three level hysteresis controller in the dq-reference frame uses the estimated angle from the PLL in the switching table to select the appropriate voltage vector given from the current error and the position of the dq-reference frame. If the PLL estimates an angle of the voltage vector that differs significantly from the real angle of the voltage vector, the switching table select an improper switching state and the system will then get unstable.

Another observation from Table 4.3 is that the stability limits of the PR controller and the hysteresis controllers has a small growth when it uses a DDSRF-PLL compared to when it uses a conventional PLL for synchronization, both PLL-controllers tuned five times slower than described in Table 3.7. This is some what unexpected since the DDSRF-PLL doesn't contain any extra delay that would slow down the interaction between the PLL and the current controller. However, the DDSRF-PLL calculation of the positive sequence SRF- d- and q- axis voltage vectors are influenced by the negative sequence SRF-voltage vectors. A possible explanation could then be that if the negative sequence is in anti phase with respect to the positive sequence, the decoupling would then actually slow down the changes in the positive sequence SRF voltages and consequently in the internal phase angle deviation in the PLL. Hence the interaction between the PLL and the current controller would be slower giving a higher stability limit.

4.1.4 Step response, when step change in $i^+_{q,ref}$ in a weak grid

In many applications the VSC is injecting reactive power into the grid, which is the same as a negative q-axis current from the VSC. Hence the control structures are evaluated for a step change in $i^+_{q,ref}$ from 0 pu to -1 pu. The weak grid is represented by a inductance of 0.2 pu including the transformer inductance. The grid resistance is 0.025 pu. Since the injection of reactive power in a weak grid makes the voltage over the filter capacitors increase and the DC-link voltage is not controlled but fixed, the system goes into over modulation for relatively small values of the grid inductance during injection of reactive power. To shield the analysis from this phenomena the grid voltage is reduced to 480 V which is equal to 0.7 pu.

The difference between the step response in this case and the case analyzed in Section 4.1.3 can be explained by the same argumentation for the different control structures presented in this thesis, and will be most evident shown in the response of the PI controller. At the same time will the differences between

the response of the different control structures in this specific case correspond to the explanation given in Section 4.1.3. Hence the response of the PI controller is shown in this section in Figure 4.14, while the response of the remaining control structures are added in the Appendix, Section F.2.3, Figure F.9-F.15.

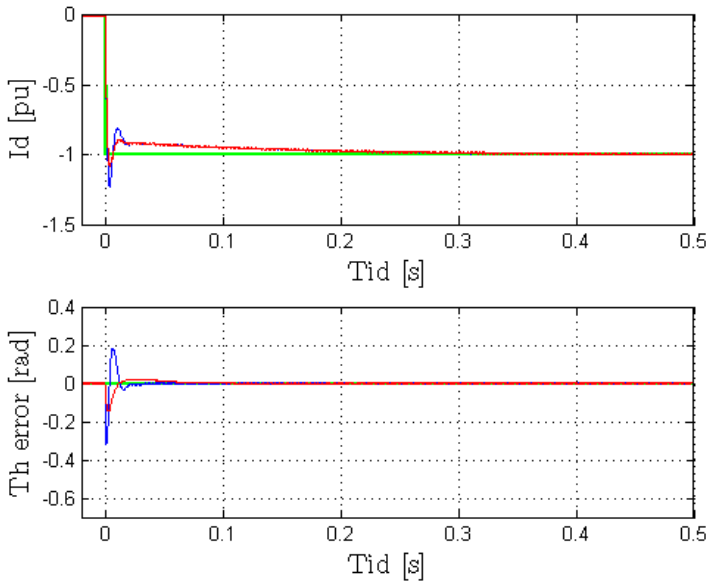
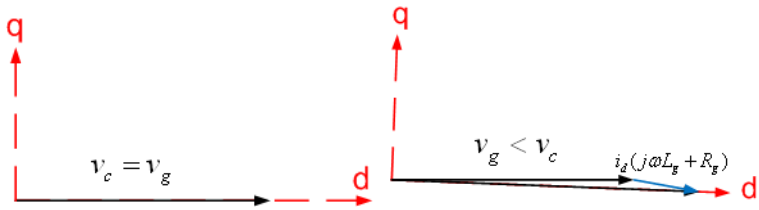


Figure 4.14: PI controller, step response in i_q^+ when connected to a weak grid

The change in q-axis current in the weak grid will give a change in the filter voltage. But contrary to the step change in d-axis current, the change in angular position of the voltage vector is small, and the change will mostly be seen in the voltage vector magnitude, as shown in Figure 4.15. Since the step change in the q-axis current causes a smaller change in the internal phase angle deviation of the PLL the oscillations in the response of both current and filter voltage becomes smaller. In addition will the PLL be more robust with respect to the synchronization as the voltage magnitude increase. A change in the q-axis component will be seen as smaller relative to the magnitude of the voltage vector, and hence also the change in angle deviation in the PLL, resulting in a more damped transient response. The same case is run for the state-space model, in the Simulink model. The result of this simulation is shown in the Appendix,

Figure F.16, which shows relatively correspondence to the simulation in PSCAD, and confirms the indication of the correctness of the state space model.



(a) Steady state voltage at $t < 0$ (b) Steady state voltage at $t > 0$

Figure 4.15: Change in voltage at change in q-axis current

Stability for Current Control Structures with injection of reactive current

Since the weak grid thevenin equivalent is close to purely inductive will the injection of reactive power increases the voltage at the filter capacitors, proportional to the grid inductance. The increased voltage makes the system more robust with respect to the synchronization, since the transients in the angle estimation error, which is equivalent to a transient in the q-axis voltage, will be reduced. This can be seen by Equation 2.39, where a change in v_q will give less change in $\Delta\theta$ if v_d is large. Hence the injection reactive power increases the stability limits, even compared to when zero current is injected.

4.1.5 Operation with a DC-link controller

To show the influence that the outer DC-link controller has on the control system, two chosen inner current controllers, the PI controller and the phase current hysteresis controller structure, are simulated for a weak grid represented by an inductance, including the transformer impedance, of 0.20 pu and resistance of 0.025 pu in the weak grid thevenin equivalent. The system is exposed to a step change in the input active power from 0 to 1.0 pu. This corresponds to a step change in the d-axis current reference for the converter with a fixed DC-link voltage. The DC-link voltage reference is kept at 1.0 pu before and after the step change. The results are shown in Figure 4.16.

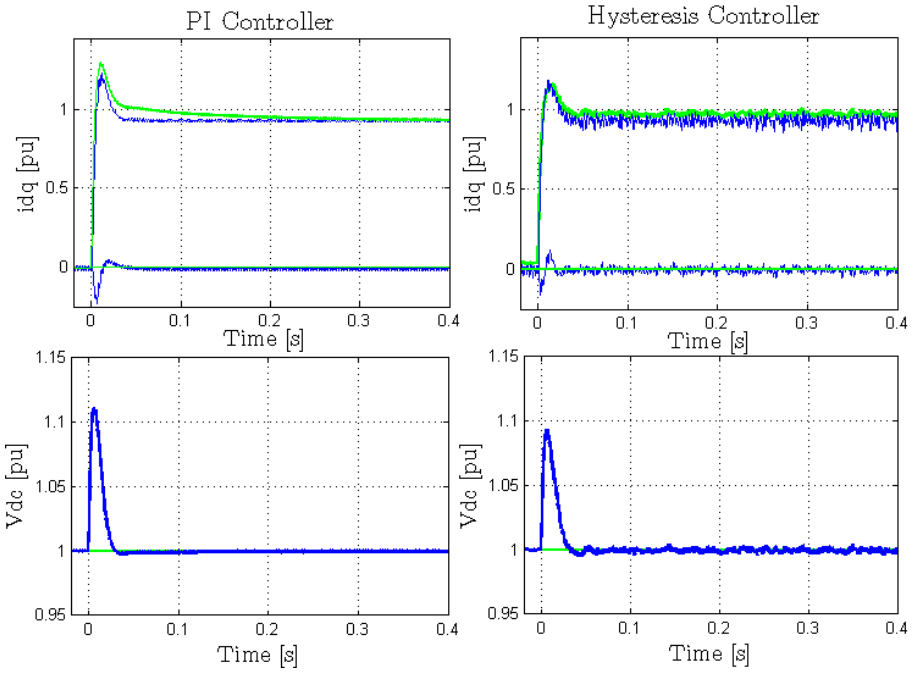


Figure 4.16: Current response, and response i the DC-link voltage for a step change in input power for a PI current controller structure, and a Phase current hysteresis controller as the inner control loop

The overshoot in the DC-link controller leads to an overshoot in the current reference and hence in the current response. Since the phase current hysteresis controller tracks the current reference faster than the PI controller the overshoot in both the DC-link voltage response and in the current response is smaller for the hysteresis controller.

To compare the stability limits of the system with and without an outer DC-link voltage controller, the inductance in the weak grid thevinin equivalent is increased until the system reaches instability. This is performed on the controller structures with a conventional PLL and shown in Table 4.4.

The high transient overshoot in the current reference which is observed in Figure 4.16 will be further increased with the grid inductance. The current will transiently follow the current reference into higher values than in the case

Table 4.4: Stability limits when step change in power input, with dc-link controller

Controller	$L_g + L_t$ *(pu)*
PI	0.29 pu
PR	0.40 pu
Hyst-abc	0.39 pu
Hyst-dq	0.36 pu

of a step change in the d-axis current reference, with a fixed DC-link voltage. Consequently the stability limits are decreased. At the same time will the delay in the DC-link voltage controller give a slope in the current reference with finite value, and not a step change. This slows down the interaction between the PLL and the current controller. Hence the stability limits is not that drastically decreased compared to the step change in the d-axis current reference with a fixed DC-link voltage.

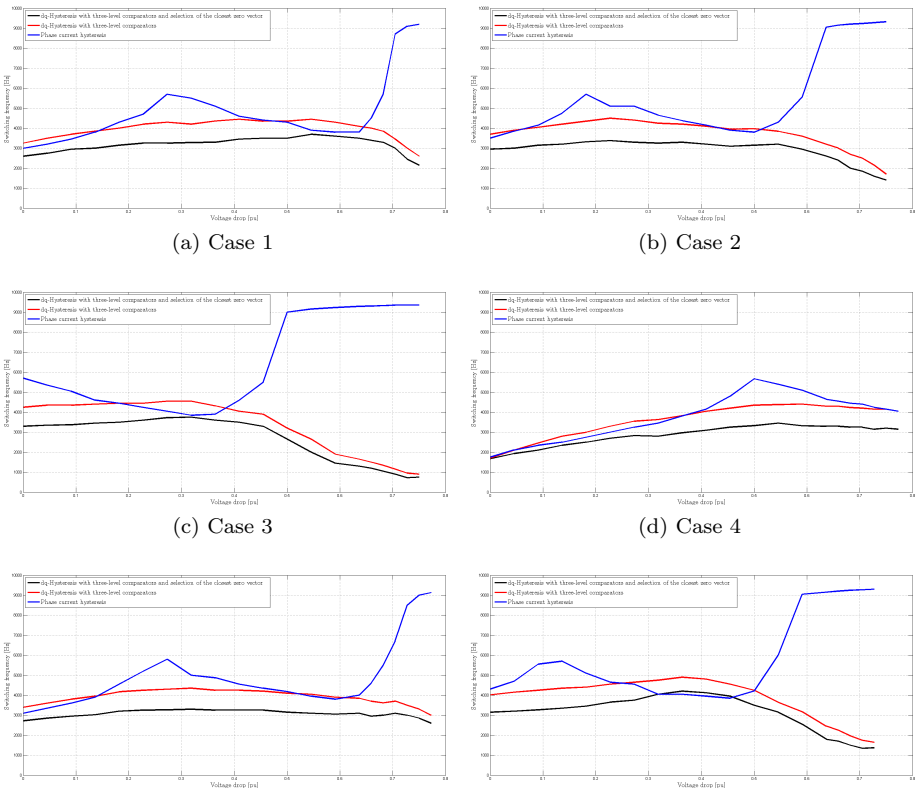
4.2 Voltage Drop in the Grid

The grid is operating around its nominal value most of the time. However it can happen that the voltage in the grid experience drop in it value for a short period of time, and the converter must be able to handle such conditions. This is especially the case in renewable energy applications, where there are grid code requirements for 'low voltage ride through' capabilities [32]. Hence this section is investigating the operation of the converter under different types of drop in the grid voltage.

4.2.1 Switching Frequency in Hysteresis Current Controllers in a Three Phase Voltage drop

A drop in the grid voltage is a case that will influence the average switching frequency of the hysteresis controllers. Limit cycle in the phase current hysteresis current controller is likely to occur under such conditions. The hysteresis controllers has therefore been compared with simulations based on the average switching frequency as a function of the grid voltage drop. The comparison is

done between the following three hysteresis controllers:



(a) Case 1 (b) Case 2

(c) Case 3 (d) Case 4

(e) Case 5 (f) Case 6

Figure 4.17: Switching frequency in hysteresis controllers

- Hysteresis controller in the abc-reference frame with fixed two level hysteresis band (Section 2.9.1, blue graph in Figure 4.17a-4.17f)
- Hysteresis controller in the dq-reference frame with three-level comparators (Section 2.9.2, red graph in Figure 4.17a-4.17f)
- Hysteresis controller in the dq-reference frame with three-level comparators and selection of zero-voltage vector (Section 2.9.2, black graph in

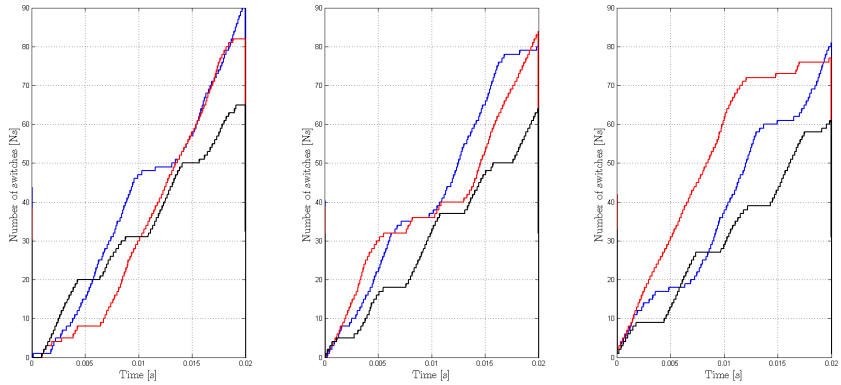
Figure4.17a-4.17f)

The simulations in Figure 4.17a-4.17f are carried out for the operation of the converter as a generator (Case 1), as a load (case 2), for consumption of reactive current (case 3), for injection of reactive current (case 4), for no load conditions (case 5) and both in generator mode while consuming reactive current (case 6). In addition, SINTEF Energy has carried out a laboratory set up for verification of the simulations, and shown in Appendix I, which shows good correspondence to the simulations.

From Figure 4.17a-4.17f it can be observed that the phase current hysteresis controller has an increasing switching frequency until it reaches a local peak around a voltage drop to 20-40 % depending on the current reference. The reduced grid voltage increases the slope of the current giving a shorter period of time between when the error goes from the upper tolerance band to the lower tolerance band. Around the local peak of the switching frequency the interaction between the three phases makes the error in one phase to be drifting within its tolerance band, while the two other phases are switching rapidly, as shown in the Appendix Figure F.24. As the voltage is further reduced in the grid these periods becomes shorter and the switching frequency drop. When the voltage has a drop to extreme low values the limit cycle phenomena and the interaction between the three phases gives a extremely high switching frequencies.

The two versions of the three level dq-hysteresis controller shows also an increase in switching frequency that has a global peak placed at a voltage drop from 20-70% depending on the current reference. This increase comes also from the increased slope of the current. The dq-hysteresis controller with selection of zero-voltage vector has a lower switching frequency than the two other hysteresis controllers for all the cases and under every condition. When the grid voltage has a drop to low values, the switching frequency of the dq-hysteresis controllers goes down, on the basis of that it is now utilizing the zero voltage vector, that decreases the slope of the current error.

Figure 4.18a-4.18c shows the number of switching action in each leg during one period for the three hysteresis controllers. It shows a different switching pattern between the phase current hysteresis controller, that has a more random distribution of switching action, and the dq-hysteresis controller with fixed zero-vectors, that has periods with almost no switching action from around the period when the sine wave of the grid voltages crosses zero, and the zero-voltage vectors are utilized. The total number of switching actions is significantly reduced when utilizing the dq-hysteresis controller with selection of zero-voltage vector. This corresponds to a lower switching frequency.



(a) Phase A (b) Phase B (c) Phase C

Figure 4.18: Number of switches during one period

4.2.2 Evaluation of Current Control Structures with conventional PLL in a Three Phase Voltage Drop in a Weak Grid

The system is exposed to a perturbation of a three phase voltage drop in the grid from 1.0 pu to 0.7 pu. This type of fault is classified as a Type A fault, and shown in Figure 3.13a. According to Table 3.9 this type of fault will not be transformed by the transformer, and appear as a type A fault at the primary side of the converter. During the fault, the VSC is operating in generator mode, with d-axis current reference at 1.0 pu and the q-axis current reference is kept at 0 pu. The grid inductance, including the transformer impedance, is 0.2 pu and the grid resistance is 0.025 pu in the weak grid thevenin equivalent. The system is simulated for the PI controller, the PR controller, the phase current hysteresis controller, and the hysteresis controller in the dq-reference frame, all with a conventional SRF-PLL. The resulting response of the current is shown in Figure 4.19. The blue plot shows the response when the PLL is tuned according to Table 3.7, and the red plot shows the response when the PLL is tuned five times slower.

During a voltage drop in a weak grid, there are two factors that influence the point of synchronization. The three phase drop in the grid gives a change in the d-axis voltage. Additionally will the change in voltage lead to a transient in the

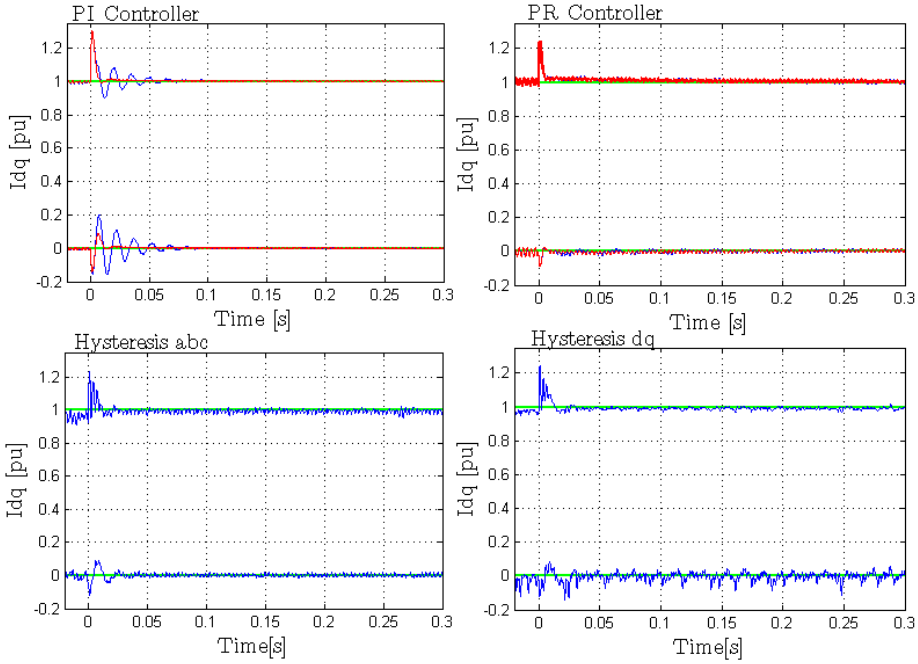


Figure 4.19: Current controllers, voltage drop type A when connected to a weak grid

current. The current transient that goes through the weak grid inductance is consequently introducing a change in q-axis component of the measured voltage. This leads to, as described earlier, change in the internal angle deviation of the PLL, that interact with the current controller giving oscillations in the current response. By comparing the red and the blue plot in Figure 4.19 it can be observed that a slower tuning of the PLL will reduce these oscillations in the PI control structure. The PR controller is transiently operating outside the line voltage fundamental frequency which gives a reduced interaction between the PLL and the current controller which results in a more damped response, where the difference in the tuning of the PLL cannot easily be seen. The current also experience a short transient when it is controlled by the hysteresis controllers. Even if the current is kept within its hysteresis bands, a short current transient will lead to a transient in the internal angle deviation of the PLL, and in the

estimated angle used for transformation of the current reference from SRF into the stationary reference frame. This result in a distorted current hysteresis band for a short period of time, and the current in the SRF experience a small deviation from its reference during the same period. The reduction of the d-axis voltage will give a smaller ratio between the d-axis and the q-axis voltage components. Hence the PLL becomes less robust with respect to changes in the voltage q-axis component. This is the opposite of the explanation given for the increased stability of injection of reactive power given in Section 4.1.4, and is giving rise to even more pronounced oscillations in the current response.

Three Phase Voltage Drop response with DC-link Controller

The three phase voltage drop is simulated with a voltage DC-link controller for the PI current controller and the phase current hysteresis controller under the same conditions as described above, with a DC-link voltage reference at 1.0 pu. The resulting DC-link voltage response and the current response are shown as the blue plot in Figure 4.20. In addition the same case is simulated with an injection of reactive power at the instant of the voltage drop.

To provide a constant DC-link voltage and injected active power, the current reference increases during a three phase voltage drop in the grid. The injection of reactive power will restore the level of the measured voltage. Hence the d-axis current reference is not increasing during the fault which lower the transient in the DC-link voltage response, and consequently in the injected active power. Injection of reactive power can be an option for better dynamic behavior during a three phase voltage drop in the grid.

4.2.3 Voltage Drop in a Stiff Grid

The rest of Section 4.2 is dedicated to the current control structures that are designed to handle an asymmetrical voltage drop. The dual PI controller with notch filter, the DDSRF PI controller, the PR controller with a DDSRF-PLL, the phase current hysteresis controller with a DDSRF-PLL and the dq-hysteresis controller with a DDSRF-PLL, will hence be further investigated. During a voltage drop in a weak grid there are, as said, two factors that influence the measured voltage used for synchronization: The change in the grid voltage and the operation of the converter. To give a base for understanding the dynamics and stability-limits for the current controllers in a weak grid, the current response to a voltage drop in a stiff grid is analyzed. This will isolate the influence the change in the grid voltage plays for the synchronization from the

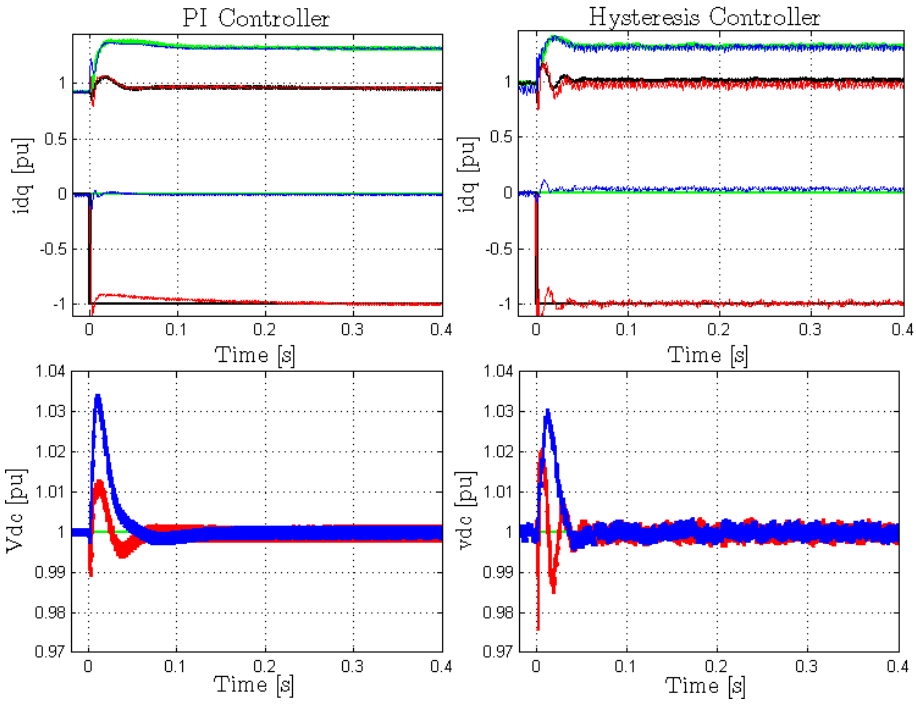


Figure 4.20: Current controllers, voltage drop type A when connected to a weak grid

operation of the converter, since the operation of the converter is not affecting the measured voltage in the stiff grid. The system is simulated, and analyzed for three types of grid faults:

- A three phase fault in the grid, classified as a type A fault, and shown in Figure 3.13a. This fault is represented as a change in the positive sequence grid voltage amplitude from 1.0 pu to 0.7 pu.

- A single phase fault in the grid, classified as a type B fault, and shown in Figure 3.13b. This fault is represented as a change in the positive sequence grid voltage amplitude from 1.0 pu to 0.7 pu and a change in the negative sequence grid voltage amplitude from 0 to -0.3 pu.

- A two phase fault in the grid, classified as a type C fault, and shown in Figure 3.13c. This fault is represented as a change in the positive sequence grid voltage amplitude from 1 pu to 0.7 pu and a change in the negative sequence grid voltage amplitude from 0 to 0.3 pu.

The linear controller in the stiff grid is simulated with an average PWM to avoid the current ripples caused by the transistor switches in the converter. Since it is not possible to simulate the hysteresis controllers with an average PWM model, they are omitted from the investigation of the current response in a stiff grid, and their resulting response is added in Appendix F.3.

The converter is operating in generator mode during the fault, with the d-axis current component reference at 1.0 pu and the q-axis current component reference at 0 . Also the negative sequence current references are kept at zero during the fault. Since the DDSRF-PLL experience instability with the PLL parameters given in Table 3.7, the PLL filter and its associated parameters are tuned five times slower for all the simulations, also for the Notch filter dual PI current controller PLL, (that also uses a notch filter in its PLL). The resulting current response for the stiff grid simulations are sown in Figure 4.21. The first row shows the response from the Dual PI controller with a notch filter, the second row shows the response for the DDSRF-PI controller and the third row shows the response for a PR controller with a DDSRF-PLL.

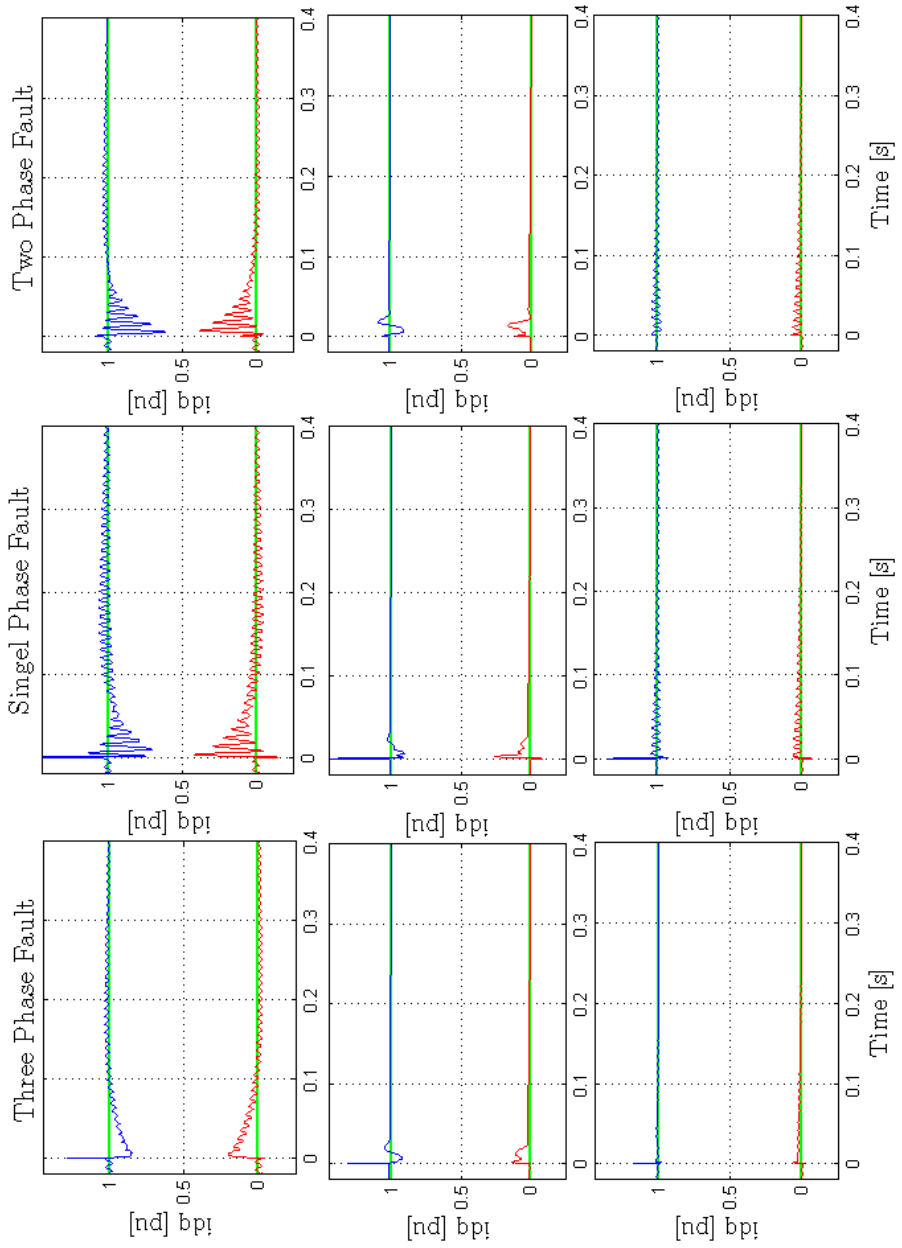


Figure 4.21: Current response to voltage drop in stiff grid. The first row show the Dual PI controller with notch filter, the second row shows the Dual PI controller with DDSRF, and the third row shows the PR controller with DDSRF-PLL

The asymmetrical faults will be transformed through the step up transformer, according to Table 3.9. The single phase fault, type B, will appear as a two phase fault, type C at the measured voltages, since the transformer is of type 3. The two phase fault, type C will appear as type D at the measured voltages.

Since the system is simulated with a stiff grid during the fault, the transient response observed in Figure 4.21 comes from the change in the grid alone. The measured voltages for both the positive SRF and the negative SRF during the fault is shown in Figure 4.22, for the DDSRF PI controller. The steady state values will be the same for all three controller structures, but the transient behavior will be different. The corresponding figure for the dual pi controller with notch filter is shown in Appendix Figure F.18.

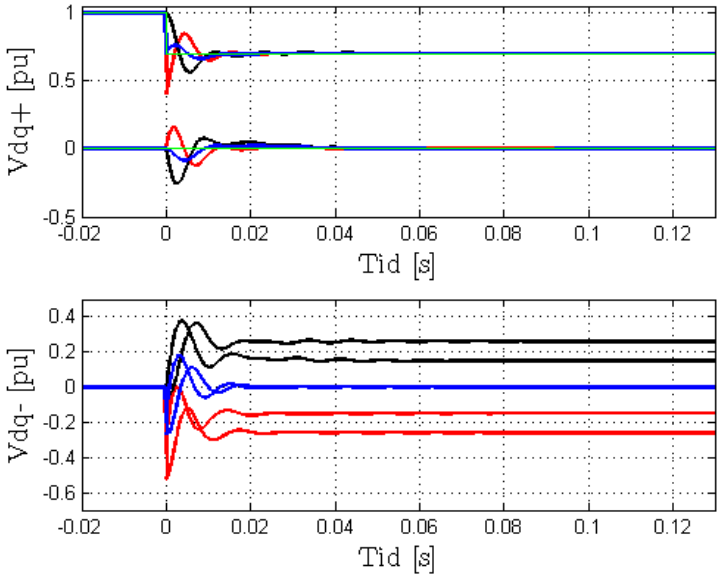


Figure 4.22: Positive and negative sequence voltage at voltage drop in the grid

The measured voltages at a three phase fault in the grid is shown as the blue plot, the single phase fault in the grid is shown as the red plot and the two phase fault in the grid is shown as the black plot. For comparison, the positive sequence SRF voltages for the PI controller with the conventional PLL at a

three phase voltage drop in a stiff grid is plotted as the green graph in Figure 4.22.

Even in the stiff grid, a three phase fault results in a transient in the q-axis voltage for the DDSRF-PI controller. This transient is not present for the PI controller with conventional PLL, in the green plot in Figure 4.22. The system is in steady state at the instance the fault occurs. In steady state the positive and negative sequences are fully separated by the decoupling algorithm. Therefore, the sudden drop in the positive sequence SRF d-axis voltage will be experienced as a 100 Hz oscillation with amplitude 0.3 pu in the negative sequence SRF. The decoupling algorithm is now tracking a new steady state, and it is consequently decoupling the positive and negative SRF sequences. The cross coupling between these two sequences results in oscillations in the positive sequence q-axis component, and hence in the internal angle deviation in the PLL.

When the fault in the grid is of asymmetrical nature, the measured voltage will experience a step change in both its positive and negative sequence SRF components. This leads to a more pronounced change in the negative sequence SRF components, since permanent changes in the negative sequence comes in addition to oscillations commented above. Consequently will the transient influence on the positive sequence SRF voltage from the negative sequence be even greater in these situations compared to the three phase fault in the grid.

All three current controllers contains a feed forward loop of the measured voltages in its control structures. As it can be seen from Figure 4.22 , the positive sequence d-axis voltage has a reduced derivative at the two phase voltage drop in the grid compared to the three phase voltage drop and the single phase fault. This comes from the decoupling of the negative sequence voltage that is in anti-phase. Hence the feed-forward loop will give reduced overshoot for a two phase fault, than the three phase fault and the single phase fault, which can be observed in the current response in Figure 4.21.

Finally it can be concluded that these control structures are able to handle an unbalance in the stiff grid, giving zero steady state error.

4.2.4 Voltage Drop in a Weak Grid

To investigate the influence a weak grid plays for control of current during a voltage drop, the same cases as simulated for the stiff grid in Section 4.2.3 is simulated for a situation of a weak grid. The weak grid is represented with an inductance, including the transformer inductance, of 0.2 pu, and a resistance of 0.025 pu in the thvenin equivalent. The current response for the investigated

control structures are shown in Figure 4.23 and Figure 4.24. The first row in Figure 4.23 shows the result of the Dual PI controller with a notch filter and notch filter PLL and the second row shows the response of the DDSRF-PI controller and DDSRF-PLL. The first row in Figure 4.24 shows the response for the PR controller with a DDSRF-PLL and the second row shows the Hysteresis controllers with a DDSRF-PLL where the black plot shows the response for the dq-hysteresis controller with a DDSRF-PLL.

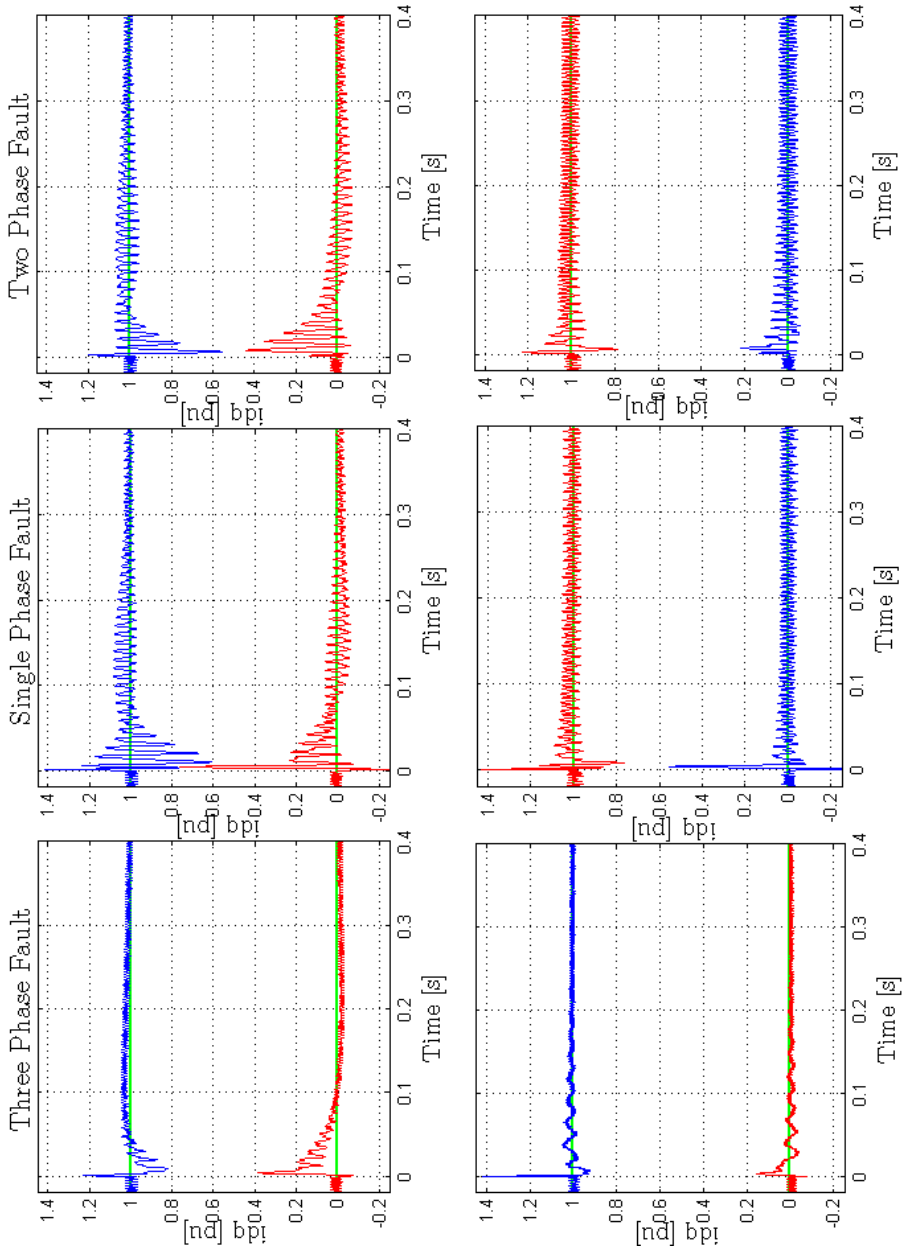


Figure 4.23: Current response to voltage drop. The first row shows the Dual PI controller with notch filter and the second row shows the Dual PI DDSRF controller

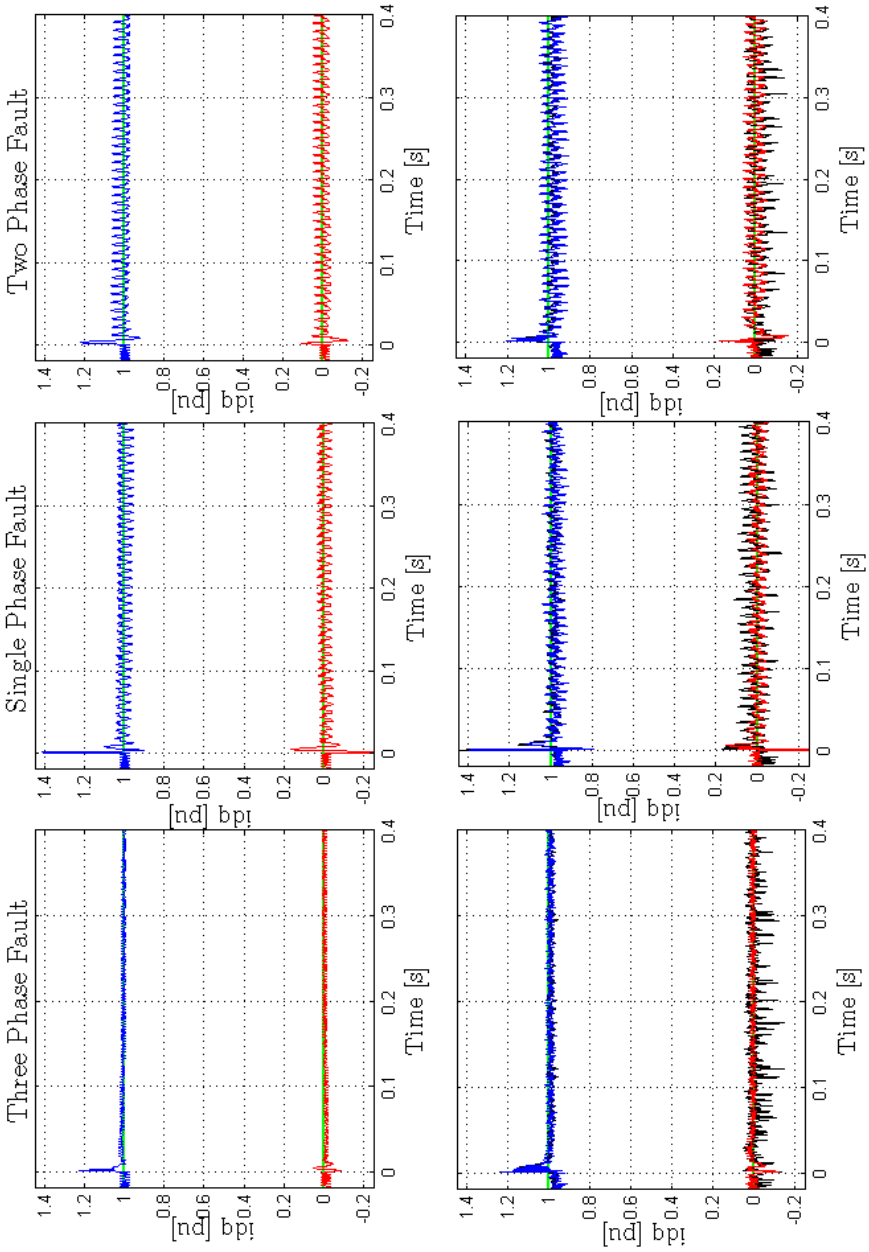


Figure 4.24: Current response to voltage drop. The first row shows the PR controller with DDSRF-PLL and the second row shows the Phase Current hysteresis controller (red and blue plot) and the dq-Hysteresis controller (black plot) both with DDSRF-PLL

During a voltage drop in a weak grid, the operation of the converter itself will in addition to the change in the grid voltage influence the voltage at the point of synchronization. The weak grid inductance and resistance, and the current reference will now phase shift the measured voltages in steady state to obtain a positive sequence current of 1.0 pu for asymmetrical faults. This phase shift will be greater as the grid inductance gets higher. The transient response of the current from the two dual PI controllers contains oscillations in addition to what was observed in the stiff grid. The argumentation for this corresponds to the explanation given in Section 4.1.3 for the PI controller with a conventional PLL, where it is argued that the interaction between the PLL and the current controller results in oscillations in the current response. The current controller with notch filter shows as in the case of a stiff grid, bad dynamic behavior compared to the controllers with the DDSRF-PLL, but by time the influence of the negative sequence is as good as removed. On the other hand will the control structures with the DDSRF-PLL have a short transient period, but in steady state it is not capable of removing the influence of the negative sequence and the response contains oscillations of 100 Hz which is not present in the stiff grid response of the same control-structures.

There exists different control objectives and control strategies for the converter controller system during a grid fault. In the simulations, which is shown to illustrate the dynamic behavior during a grid fault, where the positive sequence current are controlled to a constant value, and the negative sequence currents are controlled to zero is not necessarily the preferred operation. For the situation where the generator is a wind turbine, there is no specific demand of the current injection during a fault [32]. As seen in Section 4.2.2 will the DC-link controller increase the current reference during a three phase grid fault to maintain the DC-link voltage magnitude, and the power delivered to the grid. This can be achieved if the voltage drop is relatively small, but the current from a converter has a limit and consequently also the delivered power from the converter. During an unbalanced voltage the real power P and the reactive power Q can be written as in Equation 4.2 4.3 [35].

$$P(t) = P_0 + P_{c2}cos(2\omega t) + P_{s2}sin(2\omega t) \tag{4.2}$$

$$Q(t) = Q_0 + Q_{c2}cos(2\omega t) + Q_{s2}sin(2\omega t) \tag{4.3}$$

As seen from the equation will the delivered power contain a second order harmonic if not P_{c2}, P_{s2}, Q_{c2} and Q_{s2} are controlled to become zero. These fluctuations in the power can be canceled with currents that compensates for the

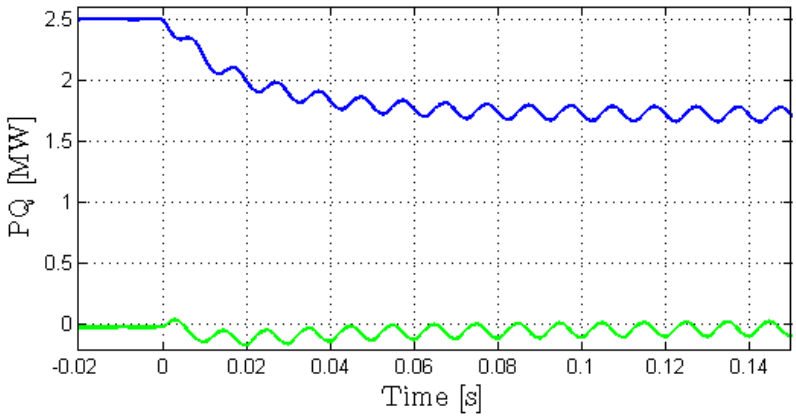


Figure 4.25: Power during an asymmetrical fault

negative sequence voltage. Figure 4.25 shows the presence of these oscillations in the power during an unbalanced voltage, where the positive sequence d-axis current reference is set to one, and the q-axis current reference and the negative sequence current references are zero. It should be considered what the goal of the control of current is. It is desired to deliver a symmetrical current to the grid, at the same time as it is desired to obtain a power without oscillations. These two goals are not achievable at the same time during an asymmetrical grid fault [39].

There is no control of the current references to cancel out these oscillations in this thesis and should be considered as a scope for further work.

4.2.5 Stability Limits for Voltage Drop in the Grid

To further analyze the influence of the weak grid has on the operation of the converter during a voltage drop in the grid, the inductance in the weak grid thevenin equivalent is increased until the system gets unstable. The stability limits are found for the same three types of voltage drop that has been investigated in this section, and the resulting stability limits is given in Table 4.5, Table 4.6 and Table 4.7 for a three phase voltage drop, a single phase voltage drop and a two phase voltage drop respectively.

The stability limits for the current controllers that utilize the conventional

Table 4.5: Stability limits at three phase fault

Controller	$L_g + L_t$ *(pu)*	*Slow PLL*
PI	0.25 pu	0.59 pu
PR	0.36 pu	0.64 pu
Hyst-abc	0.32 pu	0.59 pu
Hyst-dq	0.33 pu	0.58 pu
Dual PI-notch	0.29 pu	0.38 pu
Dual PI-dec.	–	0.40 pu
PR, PLL-dec	–	0.64 pu
Hyst-abc, PLL-dec	–	0.61 pu
Hyst-dq, PLL-dec	–	0.61 pu

Table 4.6: Stability limits at Single Phase Fault

Controller	$L_g + L_t$ *(pu)*
PR-dec	0.64 pu
Hyst-abc-dec	0.61 pu
Hyst-dq-dec	0.61 pu
Dual PI-notch	0.37 pu
Dual PI-dec.	0.4 pu

Table 4.7: Stability limits at Two Phase Fault

Controller	$L_g + L_t$ *(pu)*
PR-dec	0.64 pu
Hyst-abc-dec	0.63 pu
Hyst-dq-dec	0.61 pu
Dual PI-notch	0.37 pu
Dual PI-dec.	0.4 pu

PLL to synchronize with the grid can be given by the same argumentation as the stability limits at the step change in the d-axis current reference that comes from the interaction between the PLL and the current controller. It can be observed that the stability limits in a three phase voltage drop is decreased compared to the stability limits of the step change in the d-axis current reference. This can mainly be explained by the decreased magnitude of the measured voltage. The ratio between the d- and q-axis voltages becomes smaller, leading to a less robust PLL. The changes in the q-axis component will then result in a larger oscillation in the internal angle deviation in the PLL, as described earlier, which corresponds to reduction of the stability limits. Injection of reactive power will increase the measured voltage, and the PLL will hence be more robust with respect to changes in the q-axis voltage. This can possibly be a solution for both better dynamic behavior and increasing stability limit during a three phase voltage drop in a weak grid.

Further it can be observed that the stability limits of the current controllers that are designed to handle asymmetrical conditions has unchanged stability limits for the three phase fault in the grid and the asymmetrical voltage faults in the grid. First of all it should be noted that the positive sequence voltage drop is the same in all situations. The positive sequence voltage is used for synchronization, and the result can to some extend be explained by this fact. Even so, it is unexpected with respect to the argumentation of the interaction between the PLL and the current controller, according to the observations from the stiff grid response. In the stiff grid simulations it was observed that the unbalanced grid fault was affecting the internal angle deviation in the PLL more than a balanced grid fault. This was truly the case for the single phase fault where the negative sequence component lead to greater change in the positive sequence q-axis component and a higher overshoot in the current response. This was discussed thoroughly in Section 4.2.3.

This indicates that there possibly is another reason for the instability observed. Based on this assumption, the system controlling the current and the PLL with the DDSRF-algorithm is simulated with a fairly faster PLL, that is two times slower than the PLL described in Table 3.7. The observation from these simulations confirm the assumption of that there is another phenomena that is now triggering the instability. The stability limits is actually increased under these conditions. For a three phase fault from 0.40 pu to 0.44 pu grid inductance, and for a single phase fault from 0.40 pu to 0.44 pu grid inductance. To give an explanation to this, the response of the decoupling algorithm with respect to the filter time constant must be addressed. The relationship between the filter time constant and the response of the decoupling algorithm in the time

domain is a complex analysis, performed in [33], and shown in Equation 4.4 for the positive SRF d-axis voltage.

$$\begin{aligned}\overline{v}_d^+ = V^+ - (V^+ cos(\omega t) cos(\omega t\sqrt{1-k^2}) - \\ \frac{1}{\sqrt{1-k^2}}(V^+ sin(\omega t) - kV^- cos(\omega t)) \\ \times sin(\omega t\sqrt{1-k^2}))e^{-k\omega t}\end{aligned} \tag{4.4}$$

Where $k = \frac{\omega_f}{\omega}$. As the grid inductance increases, the PLL experience more oscillations in its internal phase angle deviation that is caused by the feed forward loop and the interaction between the PLL and the current controller, as described in Section 4.1.3. This leads to oscillations in both the positive and the negative sequence SRF voltages. If the grid inductance is high and the low pass filter time constant in the PLL is high, the slow decoupling of the negative sequence SRF voltage and its oscillations will give additional oscillations in the positive sequence q-axis voltage vector, and also in the internal angle deviation in the PLL. When the low pass filter time constant is smaller, the decoupling of the positive and negative sequence will be faster according to Equation 4.4, and the negative sequence influence on the positive sequence voltage vector is reduced, and consequently the transients in both the internal angle deviation in the PLL and in the current response becomes more damped. Therefore will also the stability limit be increased with the PLL tuned faster for the current controller that detects the angle with the DDSRF-PLL. This can be verified by simulations shown in Figure 4.26 and 4.27, that shows the response of the positive sequence SRF d- and q- axis voltages to a voltage drop for a PLL with a low pass filter time constant five times slower (Figure 4.26) and two times slower (Figure 4.27) and its associated PLL controller tuned with a value of $a = \sqrt{10}$, when the inductance in the weak grid is 0.35 pu. In addition, to show that this phenomena is not so clearly present in the weak grid representation in Section 4.2.4, the same plot is added in Appendix, Figure F.22 and Figure F.23 where the weak grid inductance is 0.20 pu.

At the same time will a too fast design of the PLL trigger instability according to the argumentation of the interaction between the PLL and the current controller without the influence of the negative sequence SRF components.

To sum up; a too high filter time constant in the DDSRF-PLL will delay the decoupling between the positive and negative sequence SRF components, and the high oscillations in the angle deviation caused by a high grid inductance will then be increased by the additional oscillations form the negative sequence

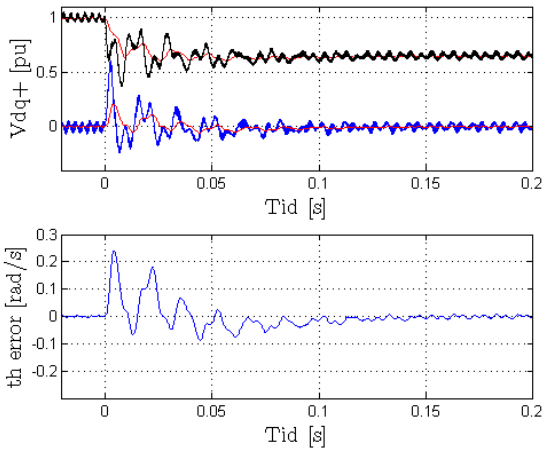


Figure 4.26: Positive sequence voltage and angle deviation at grid inductance 0.35 pu and PLL tuned five time slower than Table 3.7

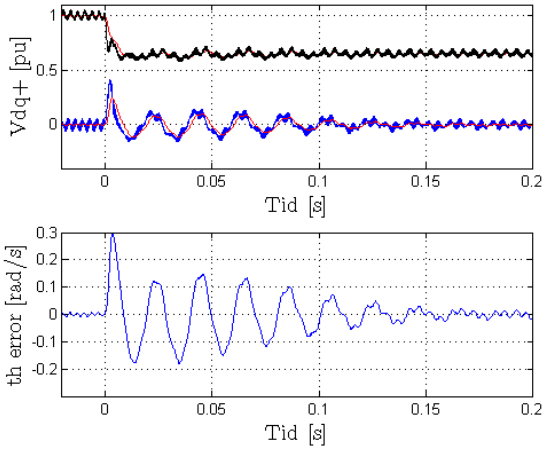


Figure 4.27: Positive sequence voltage and angle deviation at grid inductance 0.35 pu and PLL tuned two time slower than Table 3.7

SRF voltages. A too low filter time constant in the DDSRF-PLL will give high oscillations caused by the interaction between the current controller and the fast PLL, according to the discussion in Section 4.1.3.

The dual PI controller with a notch filter is also experiencing close to no change in the stability limits between the different types of voltage drop. Since this system is much more linear than the control system that separates the positive and the negative sequence with the DDSRF-PLL, the explanation can possibly be fairly easier. The power flow for all three situation will be the same since it is given by the positive sequence voltages and currents when the negative sequence currents are controlled to zero. A suggestion can therefore be that the system parameters, and its corresponding eigenvalues at the given inductance, tuning of the PLL, etc. is at its stability limit. Hence the type of perturbation is not influencing the stability limit of the control system, and the stability limits is the same for all three types of voltage drop. At the same time, the argumentation for the instability comes from the interaction between the PLL and the current controller.

4.3 General Discussion

All the simulations shown give attention towards the voltage at the point of synchronization, and the influence of the synchronization technique. Here performed by different PLL-methods. During weak grid conditions the operation of the converter is influencing the measured voltages, and the influence will be stronger as the the inductance of the grid increases. This is the case for both changes in the operation of the converter and for changes in the grid voltage. During asymmetrical grid voltage conditions, there is an additional concern regarding the choice of current references and the quality of the delivered power, as the weak grid inductance phase shifts the voltage between the point of synchronization and the stiff grid. If the 100 Hz oscillations are controlled to be canceled out where the voltage is measured, the weak grid will shift the unbalance in the voltage and the stiff grid power will still experience 100 Hz oscillations. Lately there has been given attention towards voltage-sensor-less control of the VSC [12] [36]. The voltage in this strategy is estimated by a virtual flux model, based on the current and the grid impedance. This method makes it possible to chose an arbitrary point for the voltage reference for the synchronization. If the grid impedance is known, this point can be chosen at the stiff grid. This will to some extent reduce the influence of the weak grid on the operation of the converter. At the same time, when the reference point is at the stiff grid, the problem

of choice of current reference during asymmetrical conditions will be reduced since the voltage reference point is at the stiff gird. The great drawback of this method is that the impedance in the weak grid thevenin equivalent should be known, which it rarely is.

Since the synchronization-method plays such a significant role, also other techniques than the PLL should be considered and tested under weak grid conditions. Most probably will other synchronization techniques experience the same problems regarding weak grid conditions, since they will be using the same point in the circuit for voltage measurements.

Chapter 5

Conclusion

The work presented in this thesis is an initial study of the influence that a weak grid has on the response and stability of current controllers for a Voltage Source Converter. Different control structures have been evaluated by comparison based on different simulation cases. The operation of the converter for the simulated cases does not necessarily represent the preferred performance, but it show trends that indicate a general behavior during different type of converter-operation under various grid conditions.

It is verified that a weak grid, represented by a large grid inductance, can make the system become unstable and that the interaction between the PLL and the current controllers plays a significant role in provoking such instability mechanisms. This is particularly the case for the PI controller in the synchronous reference frame. This interaction will be even more evident for the dual PI controllers where the PLL interacts with the PI controller in both the negative sequence and the positive sequence rotating reference frames. The dual PI controllers will at the same time have a slower current response, since it is controlling the current in the two reference frames that transiently interact with each other. The interaction between the PLL and the current controllers implemented in the stationary reference frame is appearing indirectly thorough the transformation of the current references into the stationary coordinates. Also the three level hysteresis controller implemented in the synchronous rotating reference frame will be influenced indirectly through its switching table. These controllers act more robust with the respect to the behavior of the PLL. However, the PR controllers and the hysteresis controllers will experience instability when the grid inductance is high and the operation of the PLL is highly

influenced by the converter itself.

Unbalanced conditions give extra concerns regarding both synchronization to the grid and control of the current. The decomposition of the electrical components into a positive and a negative sequence leads to two rotational synchronous reference frames that will influence each other with oscillations of two times the fundamental frequency. These oscillations have to be removed, and the simulations show that this can be achieved by both a decoupling algorithm and a notch-filter under stiff symmetrical and asymmetrical grid conditions. The current controllers with a DDSRF-PLL has a short transient period compared to the current controller with a notch filter, but the weak and asymmetrical grid conditions results in an oscillating steady state where the interaction between the two reference frame are not totally removed by the DDSRF-PLL.

Reduced amplitude in voltages used for synchronization makes the PLL less robust whit respect to changes in the q-axis voltage. The injection of reactive power from the converter, which increases the measured voltages, can be used to re-allocate the robustness of the PLL during voltage drop, giving better dynamic behavior and increased stability limits.

During a voltage drop in the grid with a high inductance between the converter and the stiff grid voltage source, both the change in the grid itself and the operation of the converter will challenge the point of synchronization. Hence the operation of the converter during a voltage drop in the grid leads to a less robust PLL with high transient in its estimated angle, and consequently in the current response.

It is shown that the stability limits of the system are increased by using a slower PLL and allowing for a larger transient phase angle deviation between the PLL and the voltage at the filter capacitor. At the same time will this not be equally evident for the current controller with a DDSRF-PLL, as slow filtering will lead to more pronounced influence from the negative sequence into the positive sequence synchronous reference frame voltages, and consequently in the phase angle deviation. A slow PLL will also lead to a slower and less accurate dynamic control performance of the overall control system.

The three level hysteresis controller implemented in the synchronous rotating reference frame allows the use of zero-voltage vectors which prevents high switching frequency caused by the interaction between the three phases, which can be seen in the phase current hysteresis controller during a voltage drop. The switching frequency will be even further reduced if the three level hysteresis controller allow selection of the most appropriate zero-voltage vector.

Chapter 6

Scope for Further Work

It has been shown little attention towards current controllers and the PLL under weak grid conditions in the literature, and generally is the point of synchronization placed at the stiff grid. The simulations in this work shows that the weak grid plays a significant role in both dynamic behavior and stability for the current controllers. This has not been verified mathematically. Hence the state space model representing a weak grid and with synchronization at a point where the operation of the converter itself is influencing the measured voltages used for the synchronization should be further developed. This model includes the interaction between the PLL and the current controller, but is highly non-linear. A suggestion to the focus of further work could then be to represent the PLL in the synchronous rotating reference frame only, and in some way try to express the estimated frequency by linear mathematical expressions.

Since it is shown that the PLL plays a significant role for the response of the current controller in a weak grid, other techniques for synchronization should also be investigated.

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Appendix A

Negative sequence decoupling

$$\begin{bmatrix} v^*_{d^-} \\ v^*_{q^-} \end{bmatrix} = \begin{bmatrix} v_{d^-} \\ v_{q^-} \end{bmatrix} - \bar{v_{d^+}} \begin{bmatrix} \cos(2\omega t) \\ \sin(2\omega t) \end{bmatrix} - \bar{v_{q^+}} \begin{bmatrix} -\sin(2\omega t) \\ \cos(2\omega t) \end{bmatrix} \approx V^+ \begin{bmatrix} \cos(\phi^-) \\ \sin(\phi^-) \end{bmatrix} \tag{A.1}$$

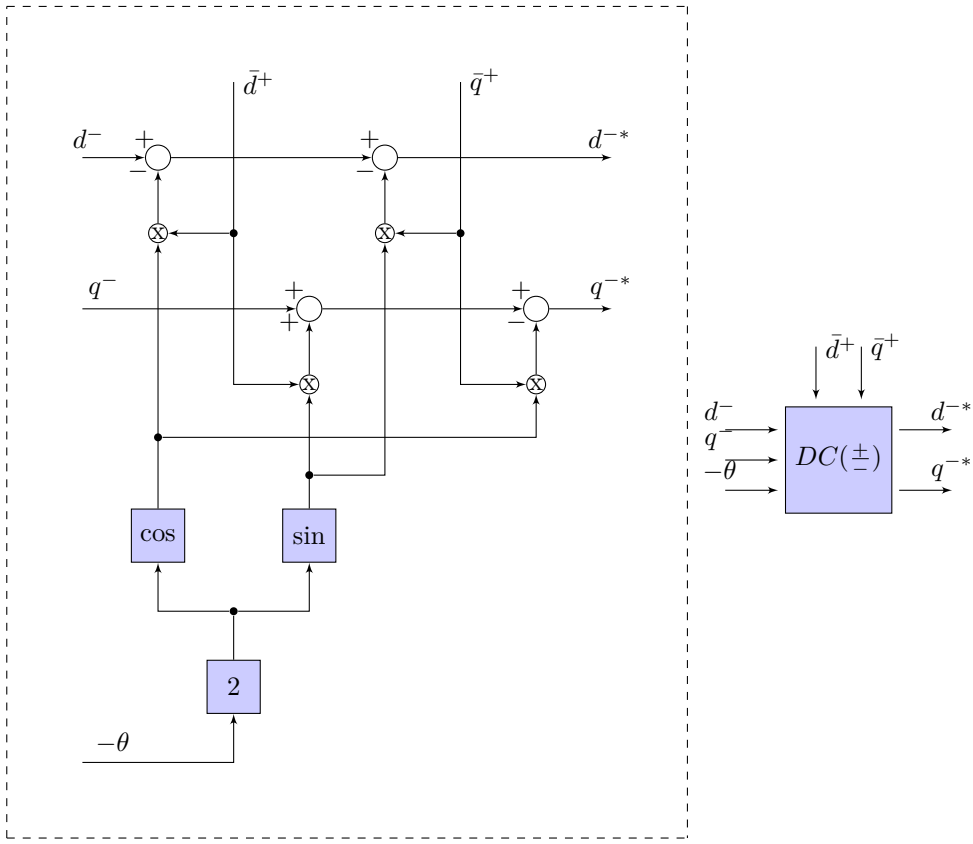


Figure A.1: Decoupling of the positive and negative sequence

Appendix B

Modulus Optimum

The current control in chapter 2.6.2 uses the modulus optimum for the tuning of the current PI-controller. The integral time constant τ_i is design so that it cancel out the time constant in the filter of the VSC. This gives the open loop transfer function for the current loop as shown in equation B.1

$$H_{OL}(s) = \frac{K_{p,pu}}{\tau_{pu} R_{pu} T_a s^2 + \tau_{pu} R_{pu} s + K_{p,pu}} \tag{B.1}$$

The goal of applying the modulus optimum in the control design is to archive a gain from the open loop transfer function from zero frequency and to a as high bandwidth as possible. This give the open loop as follows in equation B.2

$$|H_{OL}(s)| = 1 \tag{B.2}$$

By the combining equation B.1 and B.2 the result becomes as shown in

$$\begin{aligned} |H_{OL}(s)| &= |\frac{K_{p,pu}}{\tau_{pu} R_{pu} T_a (j\omega)^2 + \tau_{pu} R_{pu} j\omega + K_{p,pu}}| = 1 \\ |H_{OL}(s)|^2 &= \frac{K_{p,pu}^2}{(K_{p,pu} - \tau_{pu} R_{pu} T_a \omega^2)^2 + (\tau_{pu} R_{pu} \omega)^2} = 1 \\ K_{p,pu}^2 &= (K_{p,pu} - \tau_{pu} R_{pu} T_a \omega^2)^2 + (\tau_{pu} R_{pu} \omega)^2 \\ K_{p,pu}^2 &= K_{p,pu}^2 - 2K_{p,pu} \tau_{pu} R_{pu} T_a \omega^2 + \tau_{pu} R_{pu} T_a \omega^4 + \tau_{pu}^2 R_{pu}^2 \omega^2 \end{aligned} \tag{B.3}$$

For lower frequencies the term $\tau_{pu} R_{pu} T_a \omega^4 \simeq 0$ Deriving equation B.3 for $K_{p,pu}$ gives the modulus optimum as shown in equation B.4

$$K_{p,pu} = \frac{\tau_{pu} R_{pu}}{2T_a} \tag{B.4}$$

Appendix C

Symmetrical Optimum

Both the PLL and the DC-link voltage controller is tuned by the symmetrical optimum criteria. The explanation given in this section comes from [8]. When the system has a dominant time constant, and other small time constants, the controller can be tuned using the modulus optimum criteria. When there is a pole close to the origin or at the origin the modulus optimum is not appropriate. The open loop transfer function for both the PLL (Equation C.1) and the voltage controller (Equation 2.93) has two poles at the origin. The general case for this is given by Equation C.3

$$G_{PLL,ol} = (K_{p,PLL}\frac{1+\tau_{i,PLL}}{\tau_{i,PLL}})(\frac{2\pi}{s})(\frac{1}{T_{f,PLL}}) \tag{C.1}$$

$$G_{v,ol} = K_{pv,pu}(\frac{1+T_{iv}s}{T_{iv}s})\frac{1}{1+T_{eq}s}[\frac{v_{d,pu}}{V_{DC,pu}}\frac{\omega_b C_{pu}}{s}] \tag{C.2}$$

$$G_{SO,ol} = (K_p\frac{1+\tau_i s}{\tau_i s})(\frac{1}{Ts})(\frac{K}{1+T_{eq}s}) \tag{C.3}$$

The Nyquist criteria for stability is given by Equation C.4 [15].

$$\begin{aligned} |G_{ol}(j\omega)| &= 1 \\ \angle G_{ol}(j\omega) &= -180^o + \phi_M \end{aligned} \tag{C.4}$$

Differentiation of the angle criteria with respect to ω give the condition of maximum value of phase margin is then given by Equation C.5

$$\omega_d = \frac{1}{\sqrt{\tau_i T_{eq}}} \tag{C.5}$$

This gives the tuning criteria for the integral time constant as in Equation C.6.

$$\tau_i = T_{eq}\frac{1+\sin(\phi_M)}{1-\sin(\phi_M)} \tag{C.6}$$

The maximum phase margin will occur at the cross over frequency, symmetrical around $\frac{1}{\tau_i}$ and $\frac{1}{T_{eq}}$. This can be written by using a as the symmetrical distance between the cross over frequency and $\frac{1}{\tau_i}$ and the cross over frequency and $\frac{1}{T_{eq}}$.

$$\tau_i = a^2 T_{eq} \tag{C.7}$$

From the magnitude condition of the Nyquist criteria, the controller gain can be found as in Equation C.8.

$$K_p = \frac{T}{K\sqrt{\tau_i T_{eq}}} = \frac{T}{aKT_{eq}} \tag{C.8}$$

This results in the following closed loop transfer function as given in Equation

$$G_{SO,cl} = \frac{1+a^2 T_{eq}s}{1+a^2 T_{eq}s + a^3 T_{eq}^2 s^2 a^3 T_{eq}^3 s^3} \tag{C.9}$$

This gives the following bode plot shown in Figure C.1. Where the green plot shows the bode plot with $a = 3$ and the blue plot shows when $a = 2$.

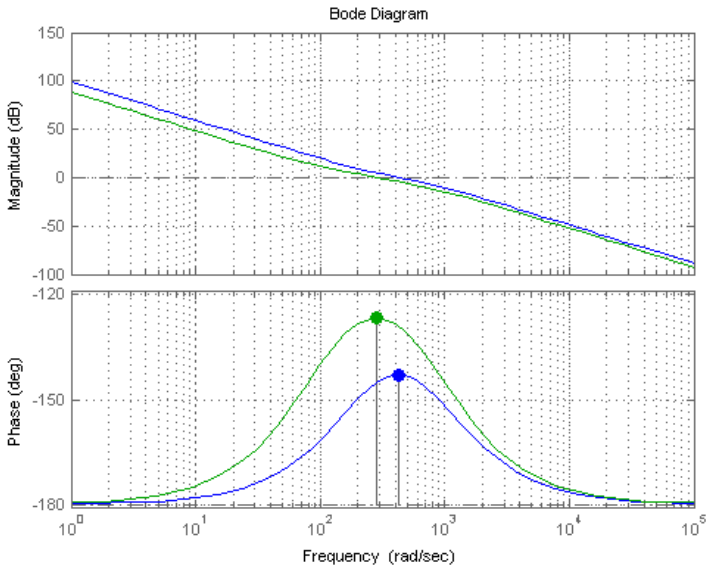


Figure C.1: Symmetrical optimum bode plot

Appendix D

State-space model

This chapter shows the derivation of the total state space model, and the differential equations used in the total A-matrix:

PLL differential equations:

$$sv'_{cq,pu} = \frac{1}{T_{f,PLL}}(v_{cq} - v'_{cq}) \tag{D.1}$$

$$s\theta = 2\pi K_{p,PLL} v'_{cq} + K_{i,PLL}\psi \tag{D.2}$$

$$s\psi = v'_{cq} \tag{D.3}$$

The simplification of adding the active damping and the feed-forward loop together in the final state space model. Together they becomes like a low pass filter of the capacitor voltage.

$$i_{ad,d} = (v_{cd,pu}\frac{1}{1+sT_\alpha} - v_{cd,pu})K_\alpha \tag{D.4}$$

$$i_{ad,q} = (v_{cq,pu}\frac{1}{1+sT_\alpha} - v_{cq,pu})K_\alpha \tag{D.5}$$

Adding them together and introduce the new state variables $v_{cd}*$ and $v_{cq}*$ simplified by choosing $K_\alpha = 1$

$$v_{cd,pu}* = v_{vd,pu} + i_{ad,d} = \frac{1}{1+T_\alpha} \tag{D.6}$$

$$v_{cd,pu}* = v_{vd,pu} + i_{ad,d} = \frac{1}{1+T_\alpha} \tag{D.7}$$

Which gives:

$$sv_{cd,pu}* = \frac{1}{T_\alpha}(v_{cd,pu} - v_{cd,pu}*) \tag{D.8}$$

$$sv_{cq,pu}* = \frac{1}{T_\alpha}(v_{cq} - v_{cq,pu}*) \tag{D.9}$$

The current controller:

$$sq_{ld}^{err} = \frac{1}{K_{p,pu}}v_{d,conv,pu} - \frac{K_i}{K_{p,pu}}q_{ld}^{err} - \frac{\omega}{K_{p,pu}}i_{d,pu} + v_{cd}* \tag{D.10}$$

$$sq_{lq}^{err} = \frac{1}{K_{p,pu}}v_{q,conv,pu} - \frac{K_i}{K_{p,pu}}q_{ld}^{err} - \frac{\omega}{K_{p,pu}}i_{d,pu} + v_{cq}* \tag{D.11}$$

The Voltage Source Converter:

$$sv_{d,conv,pu}* = \frac{1}{T_a}(-v_{d,conv,pu}* + v_{d,conv,pu}) \tag{D.12}$$

$$sv_{q,conv,pu}* = \frac{1}{T_a}(-v_{q,conv,pu}* + v_{q,conv,pu}) \tag{D.13}$$

The LCL circuit:

$$si_{d,pu} = -\frac{R_{pu}\omega_b}{L_{pu}}i_{d,pu} + \frac{\omega_b}{L_{pu}}v_{d,conv,pu}* - \frac{\omega_b}{L_{pu}}v_{cd,pu} + \omega i_{q,pu} \tag{D.14}$$

$$si_{q,pu} = -\frac{R_{pu}\omega_b}{L_{pu}}i_{q,pu} + \frac{\omega_b}{L_{pu}}v_{q,conv,pu}* - \frac{\omega_b}{L_{pu}}v_{cq,pu} - \omega i_{d,pu} \tag{D.15}$$

$$si_{od,pu} = -\frac{R_{g,pu}\omega_b}{L_{pu}}i_{od,pu} + \frac{\omega_b}{L_{g,pu}}v_{cd,pu} - \frac{\omega_b}{L_{g,pu}}v_{od,pu} + \omega i_{oq,pu} \tag{D.16}$$

$$si_{oq,pu} = -\frac{R_{g,pu}\omega_b}{L_{pu}}i_{oq,pu} + \frac{\omega_b}{L_{g,pu}}v_{cq,pu} - \frac{\omega_b}{L_{g,pu}}v_{oq,pu} - \omega i_{od,pu} \tag{D.17}$$

$$sv_{cd,pu} = \frac{\omega_b}{C_{pu}} i_{d,pu} - \frac{\omega_b}{C_{pu}} i_{od,pu} + \omega v_{cq,pu} \tag{D.18}$$

$$sv_{cq,pu} = \frac{\omega_b}{C_{pu}} i_{q,pu} - \frac{\omega_b}{C_{pu}} i_{oq,pu} - \omega v_{cd,pu} \tag{D.19}$$

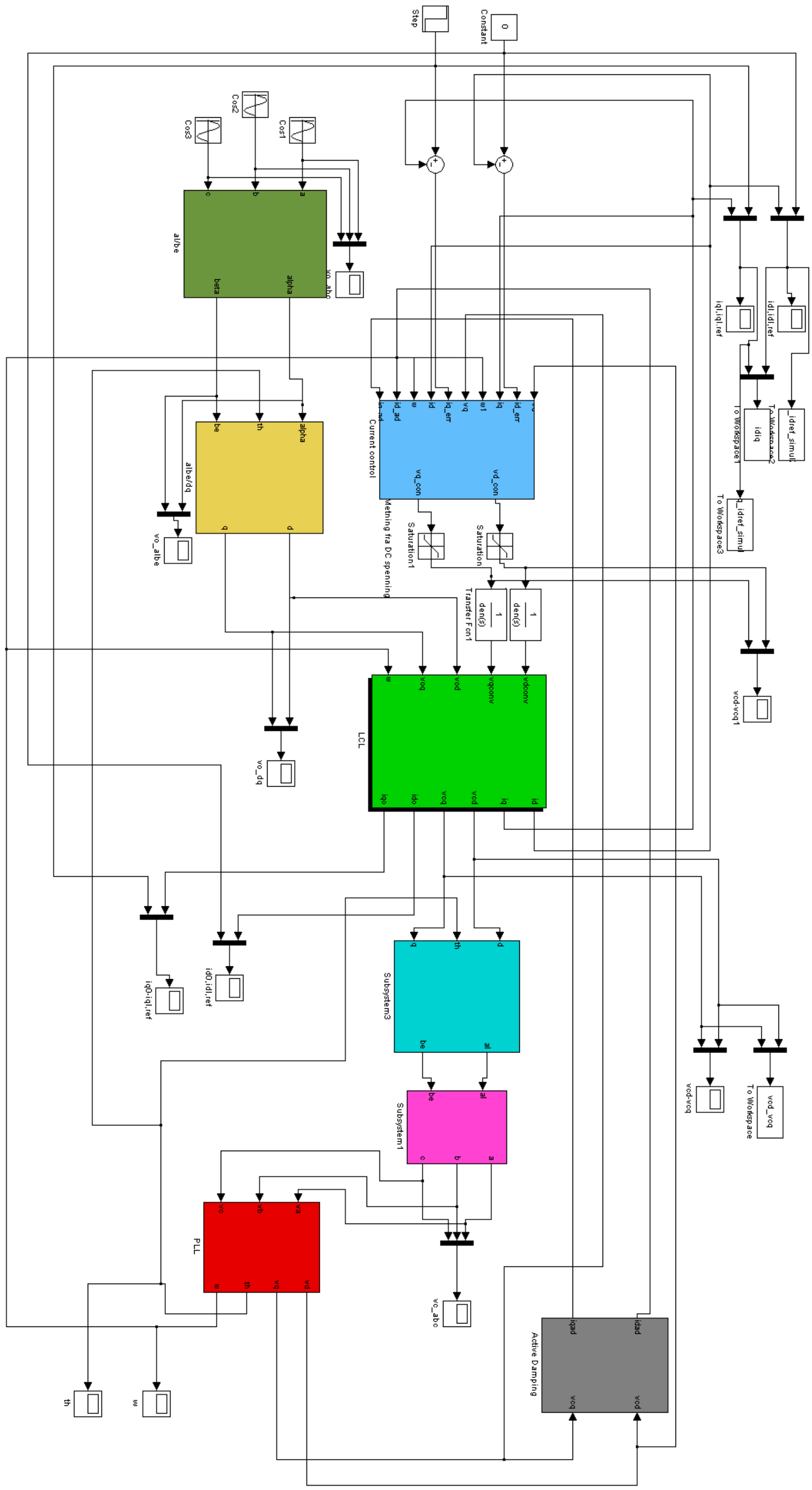
$$\mathbf{x_{tot}} = [v'_{cq}\ \theta\ \psi_{PLL}\ q_{ld}^{err}\ q_{lq}^{err}\ v_{cd}^{*}\ v_{cq}^{*}\ v_{d,conv}*\ v_{q,conv}*\ v_{d,conv}\ v_{q,conv}\ i_d\ i_q\ v_{cd}\ v_{cq}\ i_{od}\ i_{oq}]^T \tag{D.20}$$

$$\mathbf{u_{tot}} = [v_{oa}\ v_{ob}\ v_{oc}\ i_{d,ref}\ i_{q,ref}]^T \tag{D.21}$$

$$
\mathbf{A_{tot}} = \begin{bmatrix}
-\frac{1}{T_{f,PLL}} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{T_{f,PLL}} & 0 & 0 \\
2\pi K_{p,PLL} & 0 & K_{i,PLL} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & -\frac{K_i}{K_{p,pu}} & 0 & 1 & 0 & 0 & \frac{1}{K_{p,pu}} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & -\frac{K_i}{K_{p,pu}} & 0 & 1 & 0 & 0 & \frac{1}{K_{p,pu}} & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & -\frac{1}{T_\alpha} & 0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{T_\alpha} & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & -\frac{1}{T_a} & 0 & \frac{1}{T_a} & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -\frac{1}{T_a} & 0 & \frac{1}{T_a} & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & \frac{\omega_b}{L_{pu}} & 0 & 0 & 0 & -\frac{\omega_b}{L_{pu}} & 0 & -\frac{\omega_b}{L_{pu}} & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & \frac{\omega_b}{L_{pu}} & 0 & 0 & 0 & -\frac{\omega_b}{L_{pu}} & 0 & -\frac{\omega_b}{L_{pu}} & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & \frac{\omega_b}{C_{pu}} & 0 & 0 & 0 & -\frac{\omega_b}{C_{pu}} & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & \frac{\omega_b}{C_{pu}} & 0 & 0 & 0 & -\frac{\omega_b}{C_{pu}} \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & \frac{\omega_b}{L_{g,pu}} & 0 & -\frac{R_{g,pu}\omega_b}{L_{g,pu}} & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & \frac{\omega_b}{L_{g,pu}} & 0 & -\frac{R_{g,pu}\omega_b}{L_{g,pu}}
\end{bmatrix}
$$

$$\mathbf{R_{tot}}(\mathbf{x},\mathbf{u}) = \begin{bmatrix} 0 \\ 0 \\ 0 \\ -\frac{\omega}{K_{p,pu}} i_{q,pu} \\ \frac{\omega}{K_{p,pu}} i_{d,pu} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ \omega i_{q,pu} - \omega i_{d,pu} \omega v_{cq,pu} \\ -\omega v_{cd,pu} \\ -\frac{\omega_b}{L_{g,pu}} v_{od,pu} + \omega i_{oq,pu} \\ -\frac{\omega_b}{L_{g,pu}} v_{oq,pu} - \omega o_{od,pu} \end{bmatrix} \tag{D.22}$$

The obvious weakness of this state space model is that the input is given in abc, but the rest of the system is in dq. This should then include a transformation from abc to dq which is not present in this state space model.


Step
Constant
Cos1
Cos2
Cos3
al/be
albe/dq
Current control
Saturation
Saturation1
LCL
Subsystem3
Subsystem1
PLL
Active Damping
vo_abc
vo_albe
vo_dq
th
w

Appendix E

The PSCAD-model

The average model used for the stiff grid simulations is shown in Figure E.1.

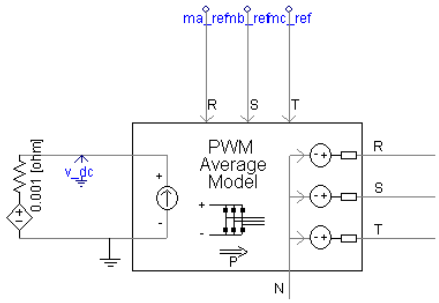


Figure E.1: The PSCAD average PWM-model

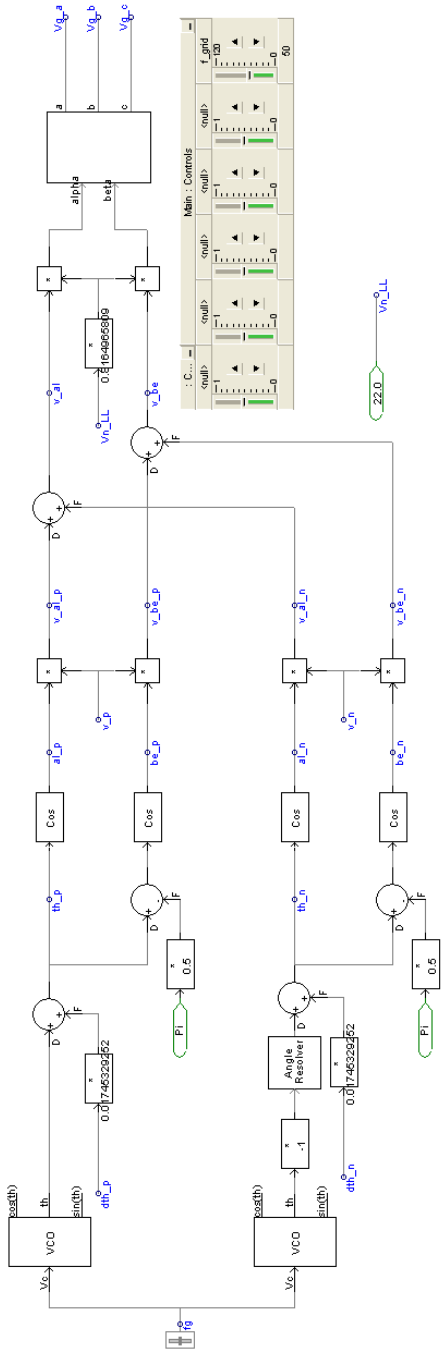


Figure E.2: The PSCAD-model stiff grid voltage source

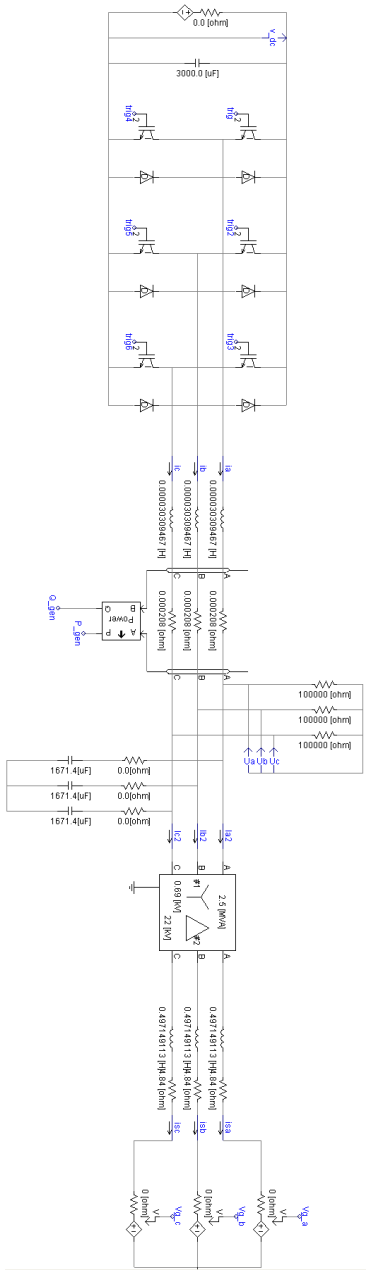


Figure E.3: The PSCAD-model electric circuit

Appendix F

Additional Simulation Figures

F.1 Stiff grid step response

The following figures, shows some additional plots for the simulations performed in Section 4.1.1.

F.1.1 Hysteresis current response

The following Figure F.1 and F.2, shows that due to the interaction between the three phases, the phase current hysteresis controller has instants where it exceeds its bandlimits.

F.1.2 Notch filter time response

Figure F.3 shows the step response for a notch filter by using the step function in Matlab at the notch filter transfer function. This filter is used to remove the negative sequence 100 Hz oscillations that is seen in the positive sequence for the dual PI controller that uses a notch filter to separate the two sequences. The notch filter step response show that the two rotating reference frames are independent from each other first after 0.1 sec.

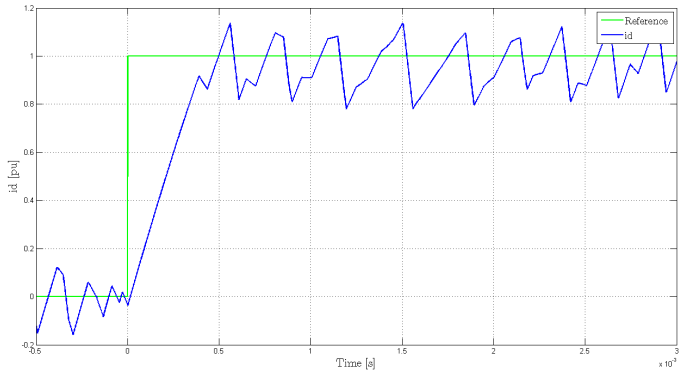


Figure F.1: Phase current hysteresis controller, step response in i_d when connected to a stiff grid

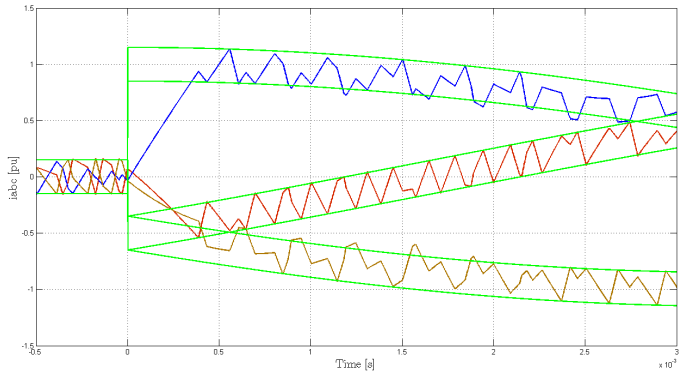


Figure F.2: Phase current hysteresis controller, step response in i_{abc} when connected to a stiff grid

F.1.3 Negative Sequence for dual PI controller in stiff grid

Figure F.4 show the negative sequence response to the step change in the d-axis current reference, for the dual PI controllers. As it can be seen will the DDSRF-controller separate the two sequences much faster than the notch filter.

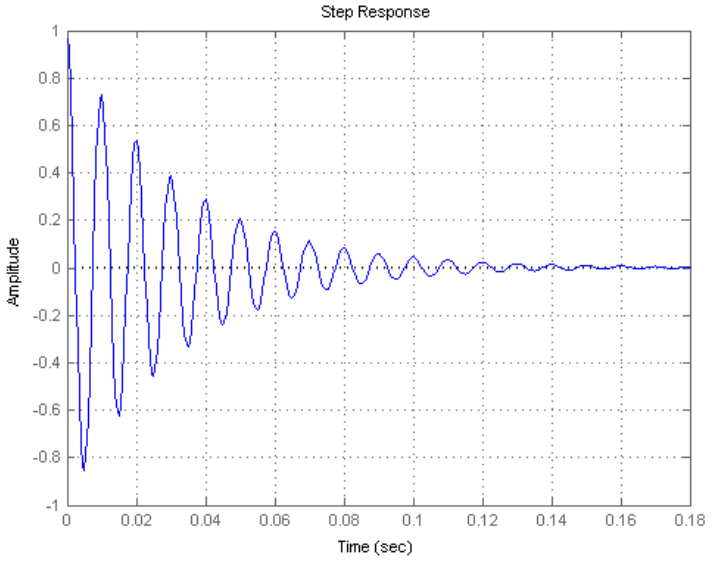


Figure F.3: Step response, notch filter

This gives a faster response in the positive sequence d-axis current.

F.2 Weak Grid Step Response

F.2.1 Feed forward loop

The feed forward loop in the PI controller is further investigated. The weak grid is represented by an inductor of 0.2 pu and a resistance of 0.025 pu. The stability limit of the system is shown in Table F.1a for stability limit of step response to a step change in $i_{d,ref}$ from 0 to 1.0 pu and Table F.1b for a step change in $i_{q,ref}$ from 0 to 1.0 pu.

To analyze how the voltage feed forward loop influence the response to a change in the grid voltage, the grid voltage is exposed to a step change from 1 pu to 0.8 pu. The current response is shown

It can be seen from the figure and the stability limits that the feed-forward

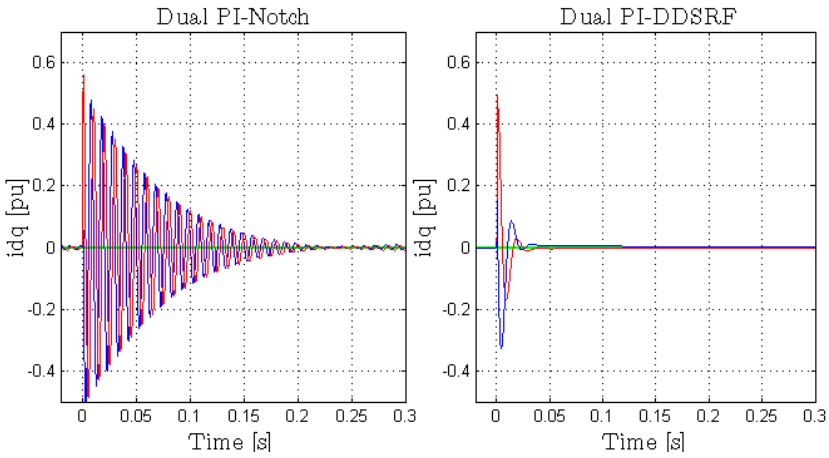


Figure F.4: Step response, notch filter

Feed forward	*PLL(fast)*	*PLL(slow)*
$vd = vd$ and $vq = vq$	0.260 pu	0.665 pu
$vd = 1$ and $vq = 0$	0.3926 pu	0.403 pu
$vd = vd$ and $vq = 0$	0.222 pu	0.590 pu
$vd = 1$ and $vq = vq$	0.399 pu	0.420 pu

(a) Step change in $i_{d,ref}$ from 0 pu to 1 pu

Feed forward	*PLL(fast)*	*PLL(slow)*
$vd = vd$ and $vq = vq$	0.233 pu	0.560 pu
$vd = 1$ and $vq = 0$	0.374 pu	0.449 pu
$vd = vd$ and $vq = 0$	0.275 pu	0.604 pu
$vd = 1$ and $vq = vq$	0.330 pu	0.426 pu

(b) Step change in $i_{q,ref}$ from 0 pu to 1 pu

Table F.1: Stability limits for different situation of the voltage feed-forward loop in the PI controller

loop of the capacitor voltage, is influencing both the dynamic behavior and the stability of the current control of the VSC in a weak grid. When the current is oscillating, this bring oscillations in the voltage, than again brings more os-

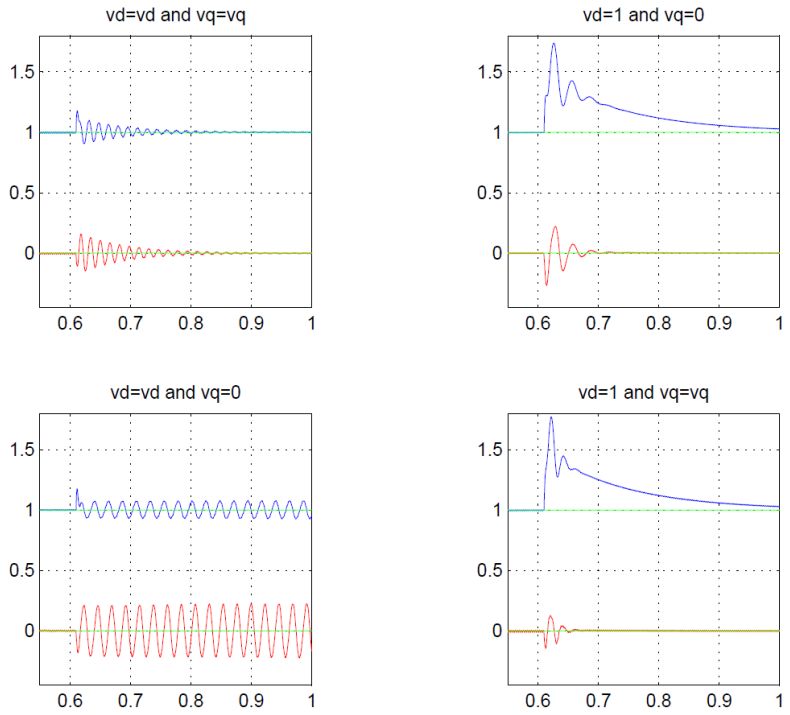


Figure F.5: Current response with and without the voltage feed-forward loop

cillations in the current controller. And the current controller will have more oscillations to control and to damp out. The influence of the feed forward voltage loop will be reduced when the PLL is tuned to act slower, since the synchronization now will be slower, but more stable.

F.2.2 Step change in $i_{d,ref}$

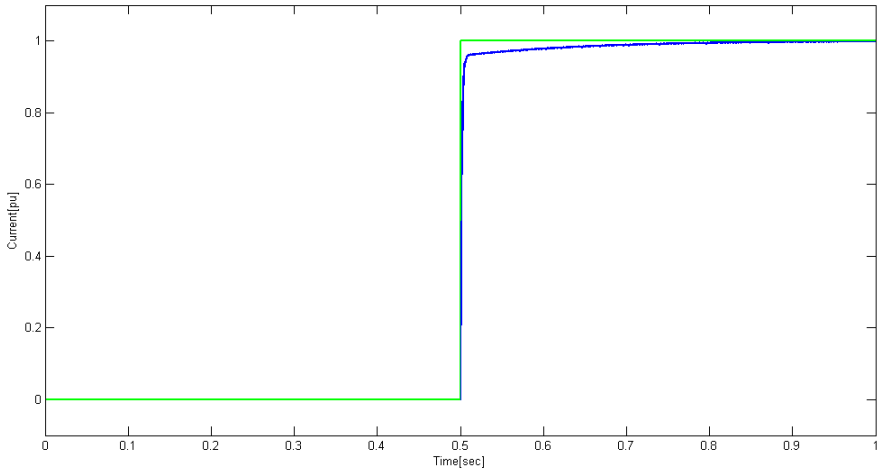


Figure F.6: Step response for i_d when step change in $i_{d,ref}$, using open loop transfer function in Equation 4.1, $L_g = 0.2pu$ and $R_g = 0.025pu$.

The PR controller with an conventional PLL and the PR controller with a DDSRF-PLL compared to show that the transient response to a step change in the d-axis current reference under a small unbalance condition will give close to the same response to the same case during a balanced voltage. The PR controller with conventional PLL will experience a difference between the response under balanced conditions compared to a small unbalance, seen in the 100 Hz in the transient response.

F.2.3 Step change in q-axis current

Figure F.16, shows the step response when the q-axis current reference has a step change from 0 to -1 pu, for the state space model of the PI controller. It shows both with the PLL tuned according to Table and when it is tuned five times slower. The result corresponds to the PSCAD simulation in Figure 4.14.

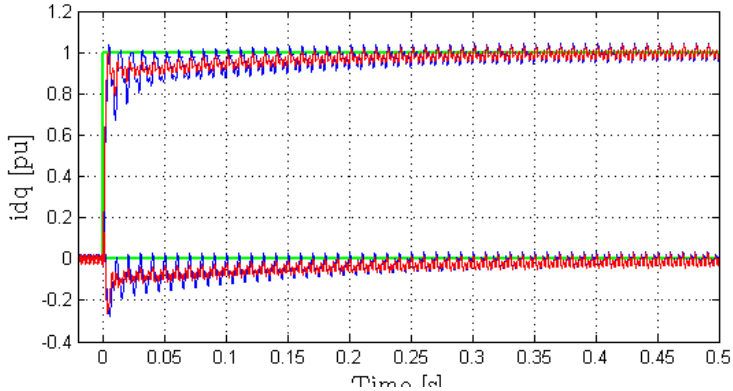


Figure F.7: PR controller with conventional PLL in blue and with DDSRF-PLL in red

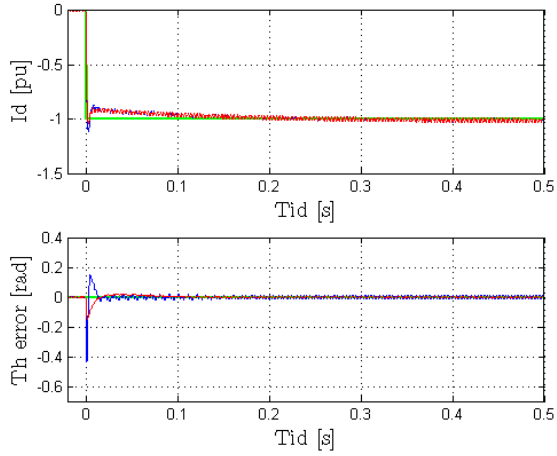


Figure F.8: PR controller, step response in i_q when connected to a weak grid

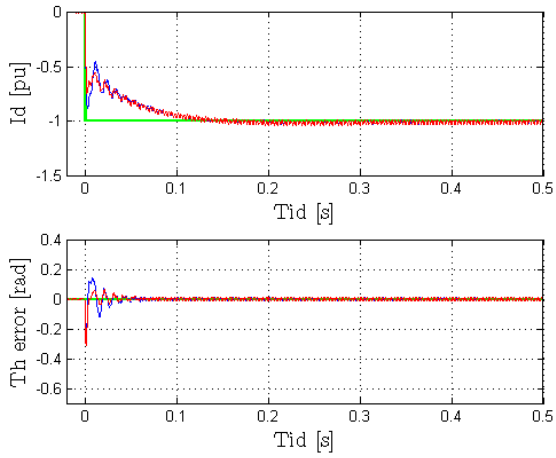


Figure F.9: Dual PI controller with notch filter, step response in i_q when connected to a weak grid

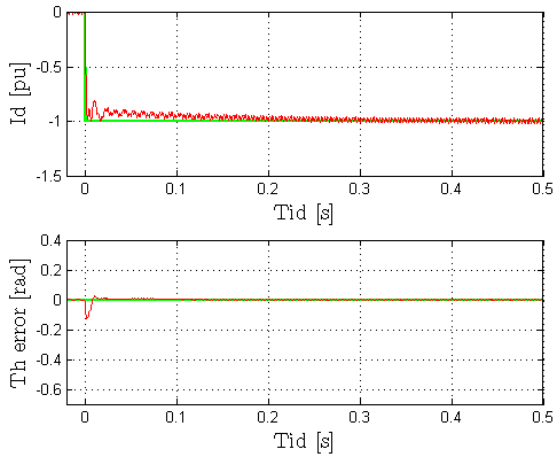


Figure F.10: Dual PI controller, sequence decoupled, step response in i_q when connected to a weak grid

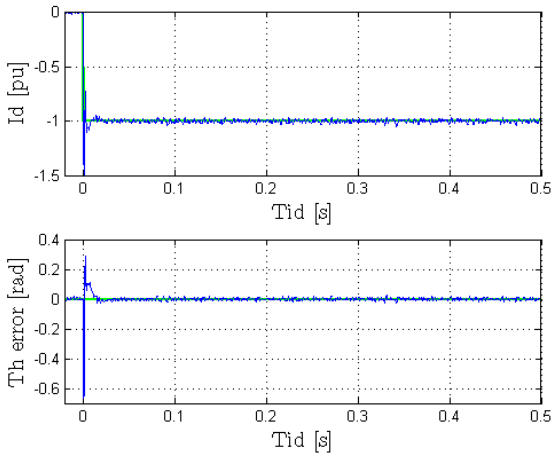


Figure F.11: Phase current hysteresis controller, step response in i_q when connected to a weak grid

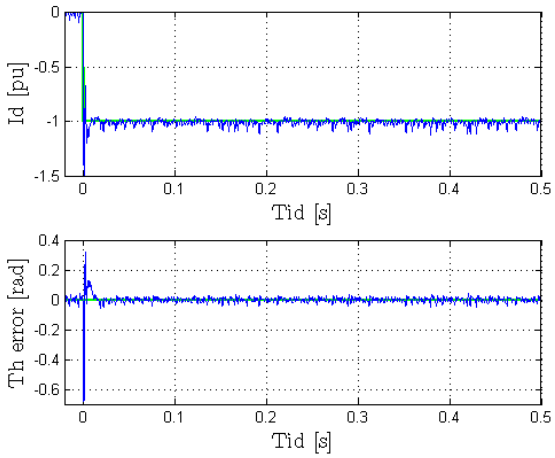


Figure F.12: Three level hysteresis-dq controller, step response in i_q when connected to a weak grid

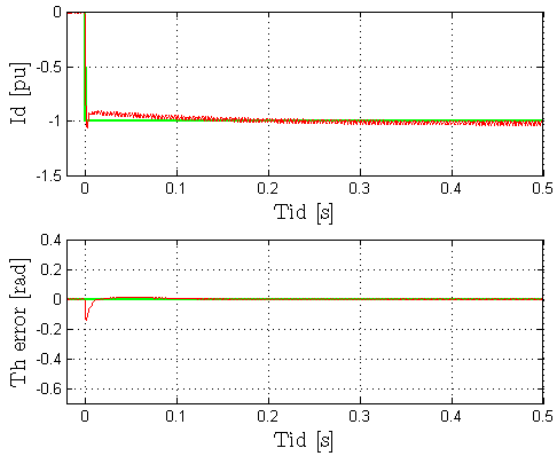


Figure F.13: PR controller,PLL decoupled, step response in i_q when connected to a weak grid

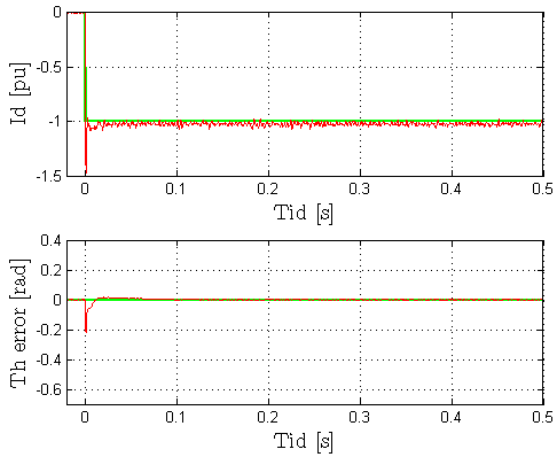


Figure F.14: Phase current hysteresis controller, PLL decoupled, step response in i_q when connected to a weak grid

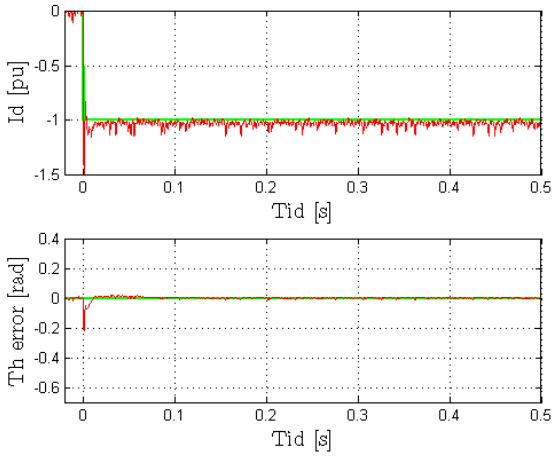


Figure F.15: Three level hysteresis-dq controller, PLL decoupled, step response in i_q when connected to a weak grid

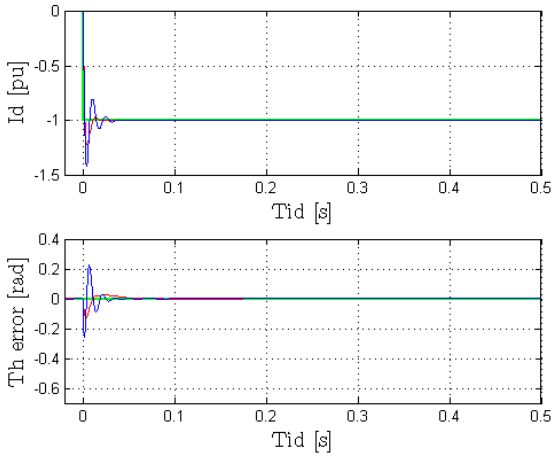


Figure F.16: Step response in i_q when connected to a weak grid

F.3 Voltage Drop

F.3.1 Stiff grid current response

Figure F.17 shows the negative sequence current response to the change into unbalanced conditions in the grid when the grid is stiff.

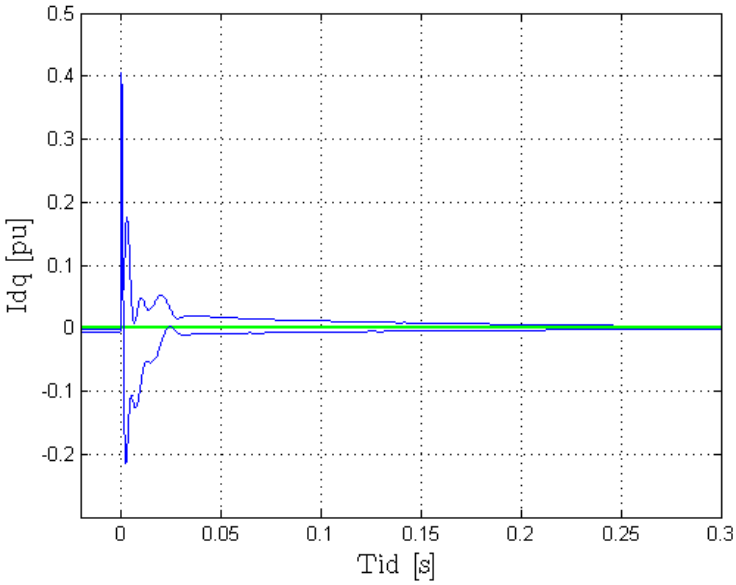


Figure F.17: Negative sequence,Dual PI decoupled sequences, current response to voltage unbalance

Figure F.18 shows the positive and negative rotating reference frame voltages at voltage change for a three phase drop (blue graph), a two phase voltage drop (black graph) and a single phase voltage drop (red graph) in a stiff grid, where the PLL uses a notch filter to decouple the two sequences. As seen in the figure, the positive sequence appears as oscillations in the negative sequence, and the negative sequence appears as oscillations in the positive sequence. The notch filter removes these oscillations by time.

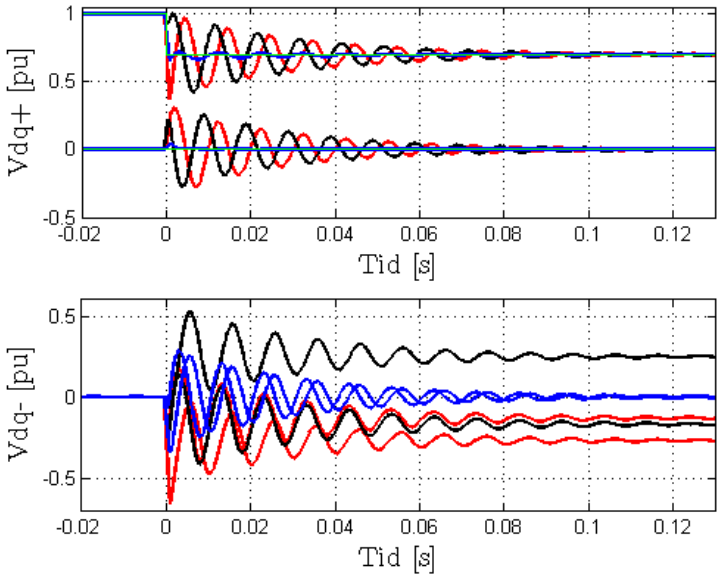


Figure F.18: Positive and negative sequence voltage at voltage drop in the grid

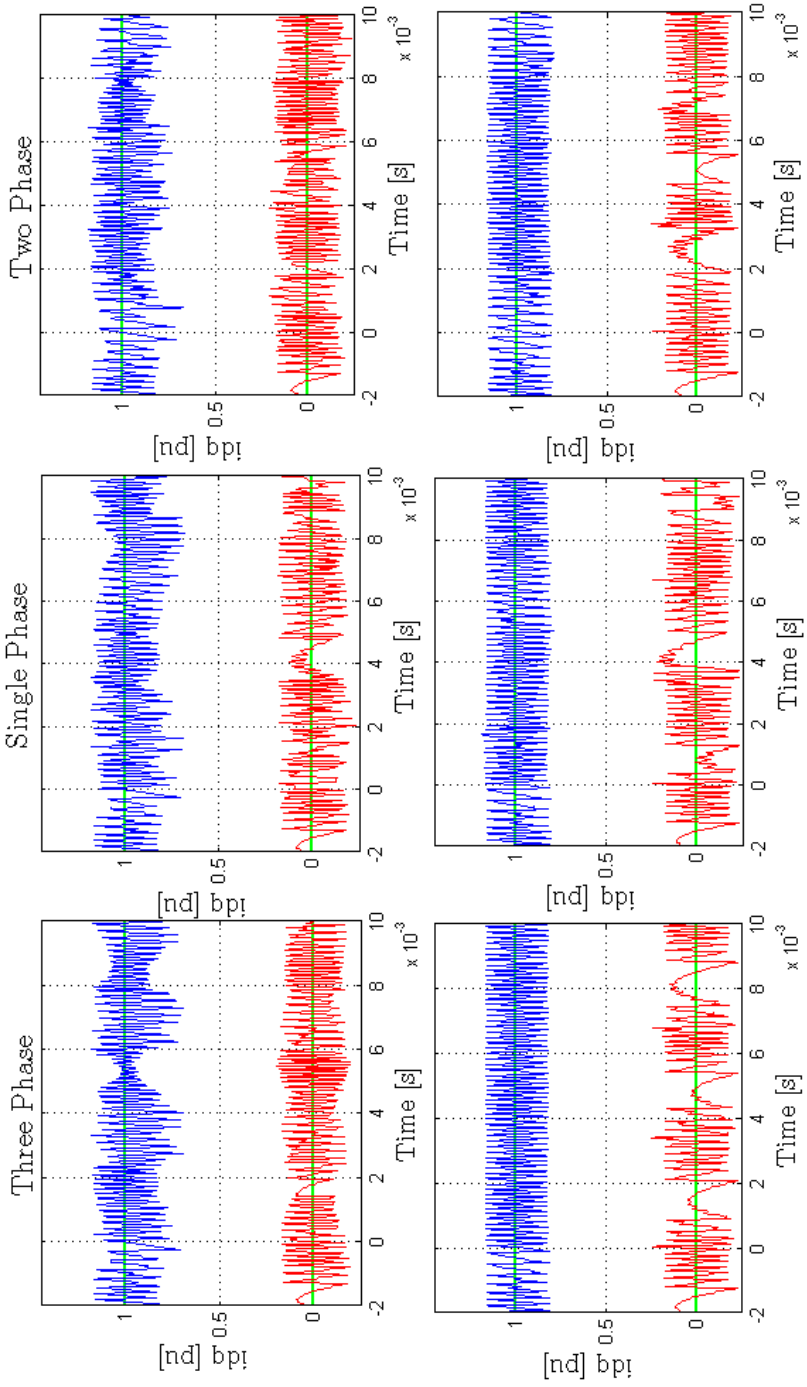


Figure F.19: Hysteresis controller in stiff grid during voltage drop. The first row shows the phase current hysteresis controller and the second row shows the dq-hysteresis controller.

F.3.2 Weak grid current response

Figure F.20 and F.21 shows the response in the negative sequence currents when the weak grid is exposed to a unbalanced condition. The red plot show the negative sequence q-axis current and the blue plot shows the negative sequence d-axis current.

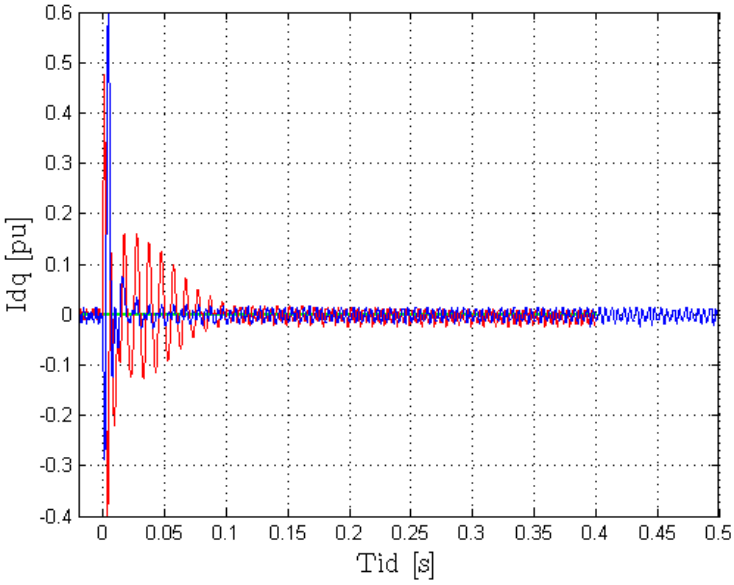


Figure F.20: Negative sequence,Dual PI decoupled sequences, current response to voltage unbalance

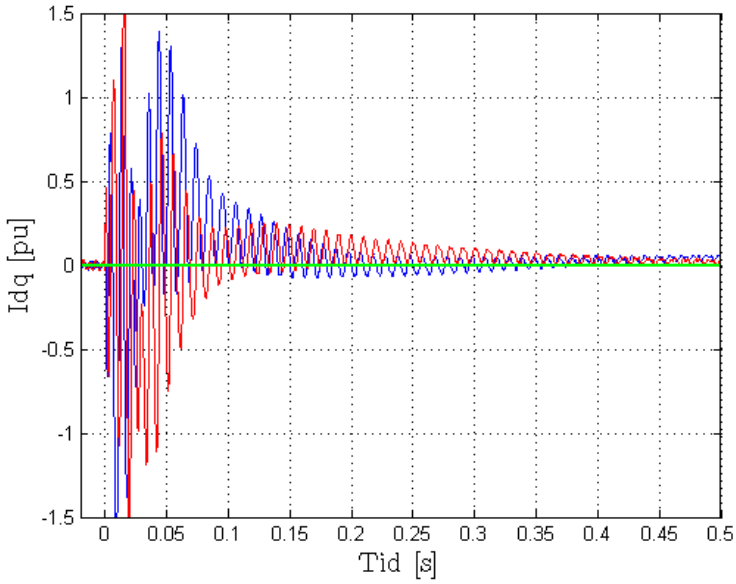


Figure F.21: Negative sequence,Dual PI notch filter, current response to voltage unbalance

Three phase voltage drop DDSRF dual PI controller

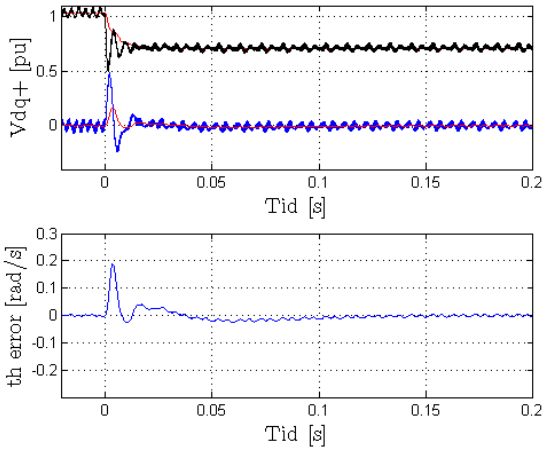


Figure F.22: Positive sequence voltage and angle deviation at grid inductance 0.2 pu and PLL tuned five time slower than Table 3.7

Figure F.22 and Figure F.23 shows the response of the positive sequence SRF d- and q- axis voltages to a voltage drop for a PLL with a low pass filter time constant five times slower (Figure F.22) and two times slower (Figure F.23) and its associated PLL controller tuned with a value of $a = \sqrt{10}$, when the inductance in the weak grid is 0.20 pu. This figure shows that the influence of the negative sequence SRF is not that pronounced under the conditions simulated in Section 4.2.4 for the slow tuned PLL, as it will be at a weak grid inductance of 0.35 pu and at the stability limit as discussed in Section 4.2.5.

F.3.3 Switching Frequency

Figure F.24 show the current for a phase current hysteresis controller during a three phase voltage drop. Because of the interaction between the three phases the current error in one phase is drifting within its tolerance band while the two other phases are switching rapidly, giving a high switching frequency, and the local peak for the three phase hysteresis controller observed in Figure 4.17a-4.17f.

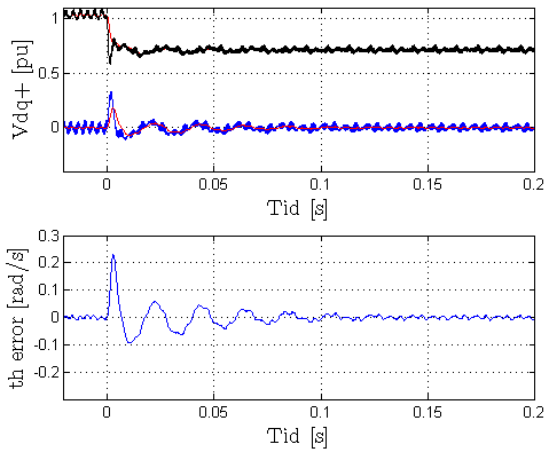


Figure F.23: Positive sequence voltage and angle deviation at grid inductance 0.2 pu and PLL tuned two time slower than Table 3.7

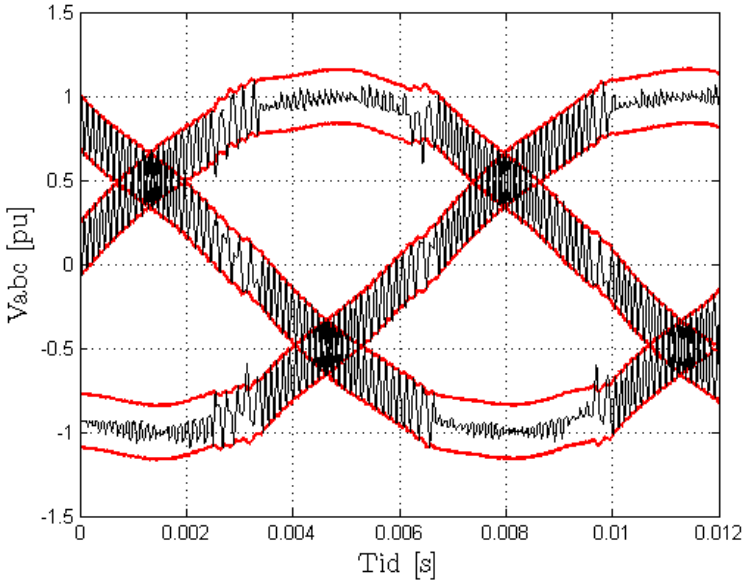


Figure F.24: Current from Hysteresis controller, at voltage drop to 0.72 pu

Appendix G

Digital Appendix

Table G.1: Digital appendix

File name	*Explanation*
Dual-PI-notch-average	Average PWM model with Dual PI notch filter controller
DDSRF-PI-DDSRF-PLL-average	Average PWM model with DDSRF-PI controller
PI-average	Average PWM model with SRF-PI controller
PR-average	Average PWM model with PR controller
PI-DC-average	Average PWM model with SRF-PI controller and DC-link controller
PR-DDSRF-PLL-average	Average PWM model with PR controller and DDSRF-PLL
PR-controller	PSCAD Model with PR-controller
PI-controller	PSCAD Model with SRF-PI-controller
PI-controller-DC	PSCAD Model with SRF-PI-controller and DC-link controller
PR-controller-DC	PSCAD Model with PR-controller and DC-link controller
Hysteresis-controller	PSCAD Model with abc-hysteresis and dq-hysteresis controller
Hysteresis-controller-DC	PSCAD Model with abc-hysteresis and dq-hysteresis controller and DC-link controller
Hysteresis-controller-DDSRF	PSCAD Model with abc-hysteresis and dq-hysteresis with DDSRF-PLL
PR-controller-DDSRF	PSCAD Model with PR-controller with DDSRF-PLL
Dual-PI-Notch	PSCAD Model with Dual PI notch filter controller
DDSRF-PI-DDSRF-PLL	PSCAD Model with DDSRF-PI controller
PR-controller-average	Average PWM Model with with PR controller
statespace	Simulink Model of PI controller state space model

Appendix H

Paper presented at IEEE PEDG2010 in Hefei China, June 2010

Evaluation of Current Controller Performance and Stability for Voltage Source Converters Connected to a Weak Grid

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Abstract-- **This paper investigates the operation of a current controlled Voltage Source Converter (VSC) under weak grid conditions caused by large grid impedance. Three different current controller structures are investigated; the conventional decoupled PI-controller in the synchronously rotating reference frame, Proportional Resonant (PR) controllers in the stationary reference frame, and the phase current hysteresis controllers. The different control strategies are studied by simulation, and the results show how large grid impedances can influence the dynamic response of the system. It is further discussed how the interaction between the current controllers, the Phase Locked Loop (PLL) and the grid inductance can trigger instability when the voltage measurements are highly influenced by the operation of the converter. The results indicate that the tuning of the PLL and the way of utilizing the phase information is of large importance for the stability and dynamic response of the control system.**

Index Terms--**Current Control, Stability, Voltage Source Converter, Weak grid**

I. Introduction

The amount of renewable energy sources integrated into the power system has grown rapidly during the last years, and significantly increased utilization of renewable energy is considered a necessity for the future electricity supply system. Different types of energy sources have different characteristics with respect to the operation of the power system, and power electronic equipment is continuously becoming a more important part of renewable generation systems because of more stringent requirements for grid interconnection. Especially the Voltage Source Converter (VSC) topology is becoming a standard, modular, solution for many applications due to its capacity for reversible power flow, for DC-voltage control and for implementation of high performance control systems [1].

Although many different control structures have been developed for VSC's in various applications, cascaded control systems based on an inner current control loop appears to be most commonly used [2]-[3]. With current control as the inner loop of the control system, the overall operation will however depend on the performance of the current controllers. This has led to a significant attention in literature towards development and evaluation of different current control structures for the VSC [3]-[5].

The control system of a VSC should be designed for stable operation under every grid condition, but weak grid conditions caused by a high value of the grid impedance is one issue that can challenge the control of the VSC. Still, there only exist a few studies considering VSCs connected to a weak grid while taking into account the dynamics of the inner current control loop and the interaction between the converter and the grid impedance [6]-[7].

The motivation of this paper is therefore to investigate, compare and evaluate the operation of different current control strategies when a VSC is connected to a weak point in the power system where there is high impedance between the converter and a stiff grid voltage. The following three control structures are chosen for the investigation: 1) Decoupled PI Current Controllers implemented in the synchronously rotating dq-reference frame[2], [9], [12]; 2) Proportional-Resonant (PR) Current Controllers in the stationary reference frame [3], [15]-[18]; 3) independent phase current hysteresis controllers [7], [19].

To examine the dynamic response and the stability limits of the VSC with different current control structures, simulation studies with the PSCAD/EMTDC simulation software have been carried out. The responses to steps in the reference values and in the grid voltage have been compared under weak grid conditions, and the limits of stable operation of the converter have been investigated by trial and error simulations. In lack of simple mathematical models with general validity under weak grid conditions, the obtained results are analyzed with reference to physical considerations based on the electric circuit and on traditional control theory.

This paper, and the presented results, should be considered as an introductory study of how the operation of a VSC can be influenced by high impedance in the grid. The results will also indicate how the nonlinearities caused by reference frame transformations and the orientation of the PLL make it challenging to establish accurate mathematical models that can be used for linearization and systematic analysis of stability and parameter sensitivity by tools from traditional control theory. Further efforts in refining mathematical models with general validity as a starting point for stability investigations under weak grid conditions will be a natural line for future continuation of the presented work.

II. System under investigation

The configuration used as basis for the investigations is shown in Fig. 1. The model includes a two-level VSC with a DC-capacitor, an LCL-filter in the grid side, a

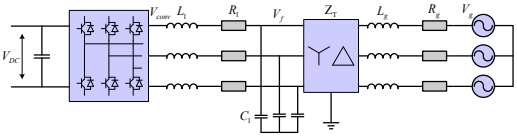


Fig. 1. Configuration of investigated system

step-up transformer and a simple grid model consisting of a series-impedance and an ideal voltage source. Since the current sensors are assumed to be located at the converter terminals, the controlled current will be the current in the filter inductor, and the mathematical model of this inductor can easily be transformed into the synchronously rotating dq-reference frame [8], [12]. The mathematical model of the VSC and the filter inductor as derived and described in [9], is given by (1).

$$I_d = (V_{DC} d_d - V_{f,d} + \omega \cdot L \cdot I_q) \frac{1}{R + s \cdot L} \qquad (1)$$

$$I_q = (V_{DC} d_q - V_{f,q} - \omega \cdot L \cdot I_d) \frac{1}{R + s \cdot L}$$

By merging the dc-voltage v_{DC} and the switching function d into an average voltage, v_{conv} at the terminals of the VSC and referring the equations to per unit values, the mathematical model of the VSC and the filter inductor can be expressed by (2).

$$\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} -\frac{\omega_b \cdot r}{l} & \omega \\ -\omega & -\frac{\omega_b \cdot r}{l} \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} + \frac{\omega_b}{l} \begin{bmatrix} v_{d,conv} - v_{f,d} \\ v_{q,conv} - v_{f,q} \end{bmatrix} \qquad (2)$$

The rotating reference frame used for orientation of the dq-coordinates is synchronized with the voltage vector $\boldsymbol{V_f}$ at the terminals of the filter inductor by the use of a phase locked loop (PLL) as shown in Fig. 2. The PLL is based on a PI-controller eliminating the steady-state error of the estimated phase angle, and the controller parameters are selected on basis of the Symmetrical Optimum criteria [11].

III. Overview of Investigated Current Control Strategies

An overview of the basic structure used for all the evaluated current controllers is shown in Fig. 3. For the linear controllers, the output voltages are used for generating PWM signals, while the modulation is inherent to hysteresis current controller. The current control and modulation is thus indicated by a common block in the figure. In addition to the current controller, the modulation and the PLL, the system also includes an active damping algorithm to damp oscillations in the LCL-filter. The active damping is based on high-pass filtering of the voltage measurements at the filter capacitors, and the output signals are subtracted from the current reference, as shown in Fig. 3.[10]

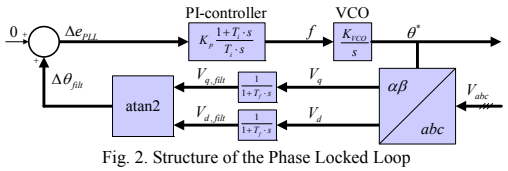


Fig. 2. Structure of the Phase Locked Loop

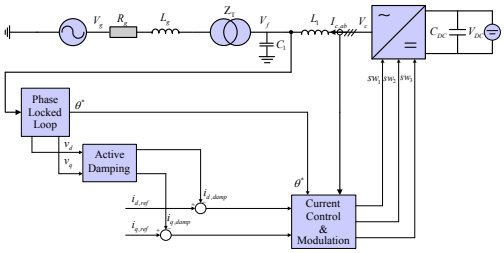


Fig. 3. Grid connected converter with LCL filter, PLL, active damping and current controller

As a basis for description and tuning of the different current controllers, the configuration from Fig. 1 and Fig. 3 will be investigated with the main parameters as given in Table I. The converter used as an example is rated for 2.5 MVA and operated at 690 V_{RMS} nominal line voltage, and a desired switching frequency of 3 kHz is assumed. The LCL-filter is designed with relatively small inductance and large capacitance. This is usually a desired characteristic with respect to cost in industrial applications, but a small inductance can also be a disadvantage with respect to stable operation in a weak grid as will be discussed later.

The basic requirements and performance criteria for the current controller of a VSC are listed in [4], [13]. Ideal reference tracking with zero steady state error and high dynamic response should be achieved at the same time as the switching frequency should be limited. The parameterization of the different current controllers will be discussed in the following subsections.

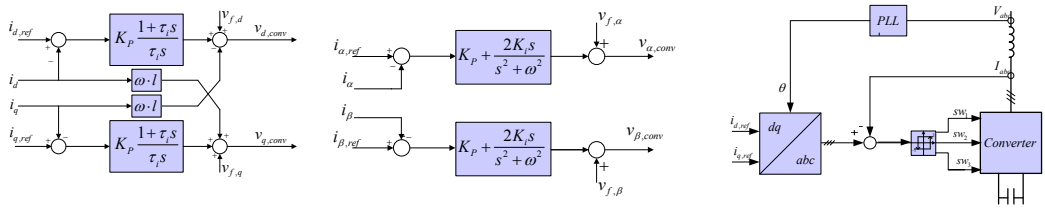
A. Proportional Integral (PI) Controllers in the Synchronous Reference Frame

In steady state, the dq-reference frame is rotating in the same angular speed as the voltage vector. Hence, the electrical components in the synchronous rotating reference frame behave as DC-quantities, and a PI controller is capable of obtaining zero steady state error. The PI current controllers in the dq-reference frame can usually be tuned by the Modulus Optimum criteria applied to the open loop transfer function of the current control loop as given by (3) [9], [14]. The d- and q-axis controllers are decoupled by the use of a forward term as seen in Fig. 4 a), to remove the coupling term in (2) and achieve independent control of the d- and q-axis currents. The controller also includes a feed-forward of the measured voltage at the filter capacitor. The open loop

TABLE I

ELECTRICAL PARAMETERS OF INVESTIGATED SYSTEM

Parameter	Value
S_n	2.5MVA
V_g	22kV
N_1:N_2	0.69:22
V_{DC}	1.2kV
f_g	50Hz
f_{sw}	3000 Hz
L_1	30μH = 0.05 pu
R_1	0.2 mΩ = 0.001 pu
C_1	1671μF = 0.10 pu



a) b) c)

Fig. 4 a) PI current controller in the dq-reference frame with decoupling of the d and q axis and feed-forward of filter voltages, b) PR current controller with feed-forward of the measured voltages in the stationary reference frame, and c) Independent phase current hysteresis controller

transfer function of (3) is therefore representing (2) with ideal decoupling and feed-forward of the filter voltage.

The controller parameters resulting from the Modulus Optimum are given by (4), where τ is the RL-time constant of the filter inductor, r is the per unit resistance of the inductor and T_a is a time constant representing a first order approximation to the PWM operation and the filtering effects in the control system. By Modulus Optimum, the integral time constant is designed to cancel out the RL-time constant of the filter, and the proportional gain is designed to achieve a gain equal to 1 of the system closed loop transfer function for as high frequency as possible. This corresponds to designing the system for a damping coefficient of $1/\sqrt{2}$.

$$H_{dq,OL}(s) = \underbrace{K_{P,pu}\left(\frac{1+s\tau_i}{s\tau_i}\right)}_{H_{CCdq}} \cdot \underbrace{\left(\frac{1}{1+sT_A}\right)}_{H_{VSC}} \cdot \underbrace{\left(\frac{1}{r}\cdot\frac{1}{1+s\tau}\right)}_{H_{lr}} \quad (3)$$

$$K_{P,pu} = \frac{\tau \cdot r}{2T_a} \qquad (4)$$

$$\tau_i = \tau$$

Fig. 5 a) shows the response to a unity step in the d-axis current reference for a controller with parameters given by (4). For this simulation, the converter is operated with a fixed DC-link voltage and the filter inductor of the converter is connected directly to an ideal, strong grid. The simulation is carried out with an average model of the VSC, to show the response of the current controller without the influence of the switching ripple [20]. This current response can be used as a reference when considering the simulations that will later be presented for a converter connected to a weak grid with high total impedance.

B. *Proportional Resonant (PR) Controller in the stationary reference frame*

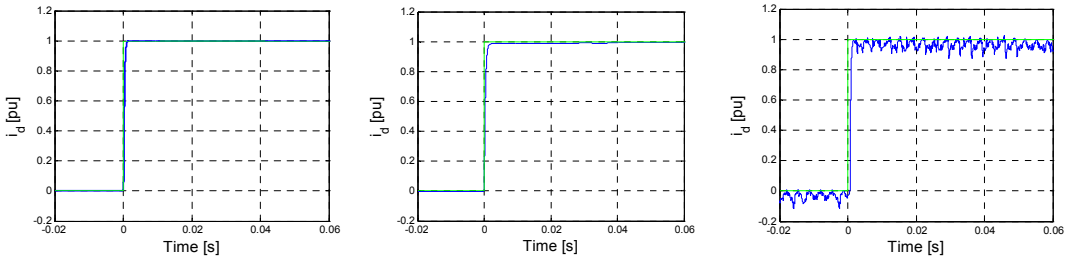
The PR controller is equivalent to the PI controller in the synchronous reference frame, but with the controller transfer function transformed into the stationary αβ-reference frame. The transformation results in the transfer function, given as $H_{cc,\alpha\beta}$ in (5), describing a resonant structure that will operate as an amplitude integrator for signals at the resonant frequency. This corresponds to a transfer function with infinite gain at the line voltage fundamental frequency. Since the PR-controller is a transformation of the PI-controller transfer function in synchronous rotating reference frame into the stationary frame, the parameters in the PR controller is kept the same as for the PI-controller although the integral gain K_i is used to express the integral time constant. The PR-controller as shown in Fig. 4 b) is therefore able to provide zero steady state error for fundamental frequency sinusoidal current references [15]-[17]. As seen in the figure, the operation of the PR-controllers is also relieved by using the measured voltages in the stationary reference frame as feed-forward terms added to the output of the controllers.

$$H_{\alpha\beta,OL}(s) = \underbrace{\left(K_P + \frac{2K_i s}{s^2+\omega_0^2}\right)}_{Hcc,\alpha\beta} \cdot \underbrace{\left(\frac{1}{1+sT_A}\right)}_{H_{VSC}} \cdot \underbrace{\left(\frac{1}{r}\cdot\frac{1}{1+s\tau}\right)}_{H_{lr}} \quad (5)$$

By using the same parameters as designed for the PI-controllers in the dq-reference frame, the PR-controller should also be expected to have the same dynamic response. This is verified with the step-response shown in Fig. 5 b), under the same conditions as explained for the PI-controllers.

C. *Independent Hysteresis Current Control of phase currents*

The hysteresis controller in the stationary abc-reference frame is shown in Fig. 4 c). Since the modulation is embedded into the current controller for this control strategy, the whole system is included in the figure. The three phase currents are controlled separately



a) PI-controller b) PR-controller c) Hysteresis control

Fig. 5. Step response of current controllers when the filter inductor is connected directly to a strong grid:

by using the error between the reference value and the measured value. The upper switch in one leg is turned on when the corresponding error exceeds the upper tolerance band, and is kept on until the current error reaches the lower tolerance band. Because the three-phase system has isolated neutral point, there is however an interaction between the three phases that can lead to current deviations larger than the tolerance band specified for the phase currents [4]. In general, the hysteresis control provides robustness with a relative independence of load parameters, but do not have constant switching frequency.

To give a good base for comparison between the three control structures the tolerance band of the hysteresis controller is selected so that the average switching frequency will be the same as the switching frequency for the linear current controllers.

The response to a step in the d-axis current reference for the hysteresis controller is given in Fig. 5 c) for the case with direct connection to a strong grid. For simulating the hysteresis controller, it is however not possible to use an average model of the converter, since the switching signals are generated directly from the current deviation. The simulation is therefore carried out with a switching model of the converter, but the measured currents are averaged over the period between the last two switching instants before transforming the measurements into the dq-reference frame. Therefore, some remaining ripple caused by the switching actions and current variations du to the random and chaotic nature of the hysteresis controllers can be seen in the figure.

IV. Comparison of the Control Structures

To investigate the performance of the different current controllers under weak grid conditions, further simulations are carried out. The simulated system is still characterized by the parameters from Table I, but the converter will now be connected to a weak grid. The controller parameters resulting from the discussion in the previous section are summarized in Table II.

To isolate the response of the current controllers from the control of the power flow in the converter, the simulations are still run with a fixed DC-link voltage.

A. Response to Step Change in Current

To observe the dynamic response, the system is first exposed to a step change in $i_{d,ref}$ from 0 to 1.0 pu while $i_{q,ref}$ remains at 0. The weak grid is represented by an inductance of 0.2 pu and a resistance of 0.025 pu, and the grid inductance is thus 4 times larger than the filter resistance. This makes the voltages at the filter capacitors, and by that the signals used for synchronization to the grid, to be highly influenced by the operation of the converter itself. The main results are shown in Fig. 6, and to limit the visual disturbance caused by the ripple currents, only the current at the grid side of the filter is plotted.

The PI controller is simulated for three different cases. The blue graph is showing the PI controller with the parameters shown in Table II, while the red graph showing the response when the feed-forward of the measured d- and q-axis voltage components is replaced by a constant d-axis voltage of 1 pu and the q-axis voltage of 0 pu. The black graph is showing the response when the PLL is tuned 5 times slower than described in Table II. It can be seen by the blue graph that the PI-controller results in an oscillatory response with relatively poor damping, which is significantly different from to the results in a strong grid.

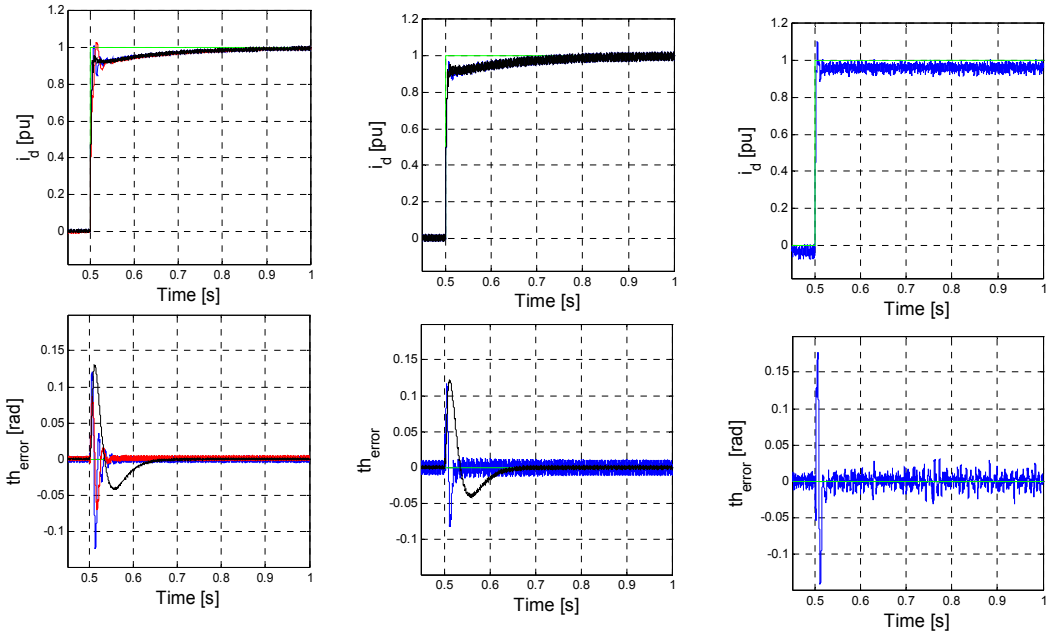
TABLE II
CONTROLLER PARAMETERS

Parameter	Value
$K_{PI,P}$	0.47578
τ_{PI}	0.1457 s
$K_{PR,P}$	0.47578
$K_{i,PR}$	3.27
$K_{P,PLL}$	50.3
τ_{PLL}	0.01 s
Hyst. Lim.	15%

Fig. 6 is also showing the internal phase error signal of the PLL, and it can be seen that for the PI-controller this angle has similar oscillations as the response in the current. This is mainly because the current response following the step in the reference value is causing an oscillation in the filter voltage, and therefore also in the phase angle deviation of the PLL. Additionally, the use of the d- and q-axis voltage components measured at the capacitors as feed-forward terms introduces a further disturbance to the current controller when the voltage is oscillating. The interaction of the current controller with the PLL and the influence of the feed-forward terms is therefore the main cause of the oscillating current response seen in Fig. 6 a). It can also be seen from the same curves that the oscillation frequency is reduced and the damping of the oscillations are increased when tuning the PLL slower.

The PR controller is simulated for two different cases, and the curves in Fig. 6 b) are representing the parameters used in Table II while the black curves are representing the case when the PLL tuned 5 times slower. It can be seen from the blue curves that the PR-controller is giving a more damped response under the conditions of Table II than the PI controller. This difference in response is not obvious since similar results should be expected from these two controllers. However, a change of current in a weak grid is implying a transient change of phase angle and therefore also a transient in the local frequency that can be estimated at the terminals of the converter. The PR-controller is however only expected to give similar results as the dq-oriented PI-controllers for fundamental frequency signals. The change of phase angle caused by the weak grid conditions will therefore make the PR-controller to transiently operate outside the resonant frequency, leading to a reduced gain and a more damped response.

When the PLL is tuned to respond slower, the PR controller and the PI controller acts more or less similar, since the transient response of the phase angle at the filter



a) PI-controller b) PR-controller c) Hysteresis controller

Fig. 6 Current step response and corresponding phase angle deviation in the PLL for the voltage source converter connected to a weak grid represented by a grid inductance of 0.2 pu and a resistance of 0.025 pu

capacitors and the influence on the PLL is reduced for both the two controller structures. The PLL is then also having a stronger filtering effect that limits the influence from the converter operation on the synchronization to the weak grid at the cost of a slower response.

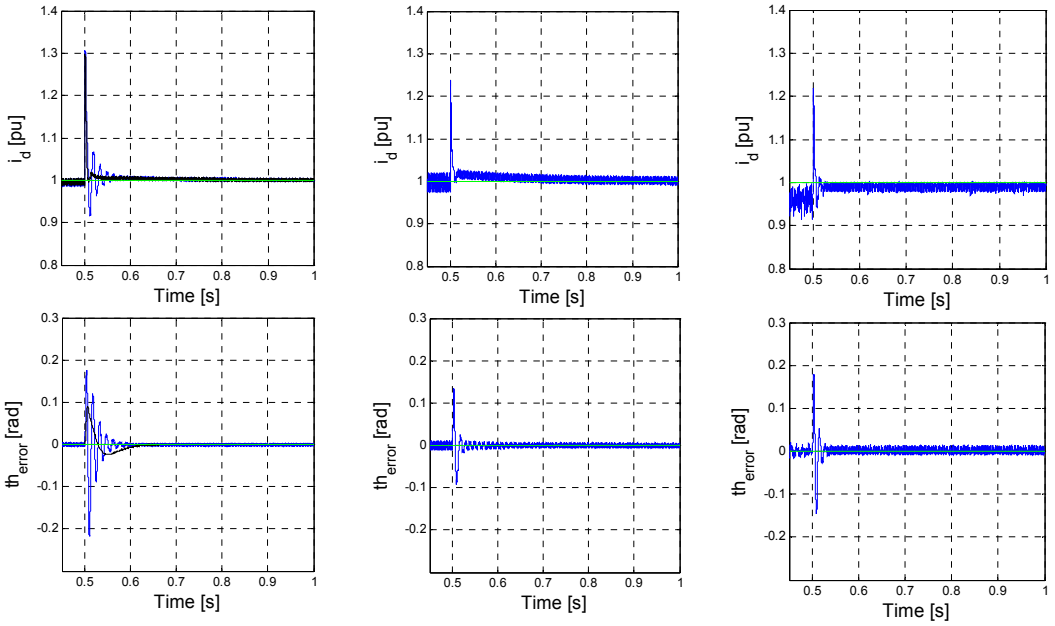
From the results of the linear current controllers in Fig. 6, it can also be noted that there is a slow response in the current after the main oscillatory transient caused by the current controllers. This slow elimination of the steady-state error is similar for both the dq-reference frame PI-controller and for the PR-controller, and becomes more pronounced when the grid becomes weaker.

The hysteresis controller is simulated only under the conditions of the PLL described in Table II and the results are shown in Fig. 6 c). As expected, the hysteresis controller has a quick response with low oscillation and a short overshoot. However, there is a small steady state error in the response originating from the fact that the hysteresis controllers is not controlling the average value of the current but only the maximum deviation from the reference value. The control of current in the hysteresis controller is however almost independent of the phase angle, that is only used for transformation of the current reference into the stationary reference frame. As long as there is sufficient voltage margin between the DC-link voltage and the grid voltage, the hysteresis controller will not be significantly influenced by the rest of the control system. The hysteresis controller can therefore be used as a point of reference for discussing the interaction between the PLL and the rest of the control system.

The different interaction between the current controller and the PLL can be further commented by considering how the phase angle information is used. The PI controllers are based on using the angle from the PLL to transform the measured current into the synchronous rotating reference frame and then transform the voltage reference output of the current controller back to the stationary reference frame for generating the switching states. The PR controller and the hysteresis controller are however using the same angle only to transform the current reference from the synchronous reference frame into the stationary reference frame. Although the PI- and PR controller should be equivalent, the results show to be quite different. These differences in the simulation results give an indication on how the nonlinear interaction between the current controller and the PLL through the phase angle used for the reference frame transformations influence the stability of the system. This explanation is supported by the observation in Fig. 6, where the response of the PI and PR controller are close to identical, when the influence of the PLL is reduced for both controller structures. However, a slower tuning of the PLL will result in slower overall response of the control system, and reduced accuracy in transient control of active and reactive power flow.

B. Response to a Voltage Drop

To give a wider base of observations, the system is also exposed to a voltage drop in the stiff grid from 1.0 pu to 0.7 pu, while $i_{d,ref}$ and $i_{q,ref}$ are kept constant at respectively 1.0 pu and 0 during the simulation. The result for the different control structures is shown in Fig. 7. At the instant when the voltage drop occurs, it can be seen from Fig. 7, that the current has a significant overshoot before it is controlled back to 1.0 pu. This



a) PI-controller b) PR-controller c) Hysteresis controller

Fig. 7.Response in current and corresponding phase angle deviation in the PLL when the system is exposed to a drop in grid voltage from 1.0 pu to 0.7 pu, for the voltage source converter connected to a weak grid represented by a grid inductance of 0.2 pu and a resistance of 0.025 pu.

current is going through the weak grid, influencing v_f and the internal phase angle deviation of the PLL. This interaction can be most clearly seen in the oscillating response in the PI controller. The PR controller and the hysteresis controller are also experiencing the peak in the current, but as explained earlier the interaction between the current controller and the PLL is weaker for these controllers, leading to a less oscillatory response than the PI controller. To show the influence of the PLL on the PI controller, the system is further simulated with the PLL tuned 5 times slower than the parameters given in Table II, and shown as the black graph in Fig. 7a). As expected the current response acts more similar to the PR controller, confirming that the controller responses become more equal with a limited influence from the PLL.

C. *Investigation of Stability Limits*

To further investigate the influence of the grid inductance, the inductance value in the simulation model is increased until the system reaches a point of instability. The first investigation is based on a step in $i_{d,ref}$ from 0 to 1.0 pu. The results are shown in Table 3, where it can be seen that the PR-controller is stable for a larger range than the PI-controller. The hysteresis controller is not as dependent on the angular position from the PLL as the linear control structures, but the reference is transformed from dq-reference frame to abc-reference frame by use of the angle from the PLL. If the grid inductance is so large that the angular error in the PLL becomes significant during the transient response, the references will be distorted, and the controller becomes unstable because of this effect. Due to its non-linear operation, the hysteresis current controllers are therefore making the system to reach instability caused by distortions for a lower value of the grid inductance than the PR-controller.

The same investigation is performed on the current controllers with PLL tuned 5 times slower, showing an increased stability limit for both the PI controller (L_g=0.72pu), the PR controller (L_g=0.82 pu) and the hysteresis controller (L_g=0.84 pu). This further verifies that a control system with reduced dynamic performance will be more stable in a weak grid.

Table III also shows the stability limit, when the VSC is controlled to consume reactive power, simulated as a step change in $i_{q,ref}$ from 0 til 1 pu. The stability limit for this step change is lower for all three controllers investigated compared to when the system is exposed to a step change in id. The weak grid is represented by a line which is significant more inductive than resistive. A change in i_q will give a higher voltage drop than a change in i_d, and as described in the previous sections, a voltage drop results in an overshoot in the d-axis current and then consequently in the angle divagation, which again gives a more unstable system caused by the PLL being unable to detect this change.

The stability limit is also investigated for a voltage drop in the grid from 1pu to 0.7 pu with a constant $i_{d,ref}$=1.0 pu and shown in Table III. It can be seen from

TABLE III
GRID INDUCTANCE AT THE STABILITY LIMIT FOR THE THREE DIFFERENT CONTROL STRUCTURES

Method	Step in i_d	Step in i_q	Step in v_g
PI-controller	0.32 pu	0.29 pu	0.255 pu
PR-controller	0.46 pu	0.365 pu	0.36 pu
Hysteresis abc	0.38 pu	0.30 pu	0.29 pu

the table that the grid inductance at the stability limit is slightly lower than for the step change in iq. It can be seen in Fig. 6 and Fig. 7, that the overshoot in the current and in the angular deviation is higher for a step change in the grid voltage than in a step change in $i_{d,ref}$, The overshoot in the current and the internal angel deviation increase with increasing inductance in the grid. At the value given in Table III the overshoot gets so high that the PLL and the current controller is unable to detect its reference, and the system becomes unstable.

V. Conclusion

This paper presents an initial investigation on the influence that large grid inductance values has on the response and stability of current controllers for Voltage Source Converters. It is verified that a large grid inductance can make the control system to become unstable, and that the interaction between the PLL and the current controller plays a significant role in provoking such instability mechanisms. This is particularly the case for the PI-controllers in the synchronous reference frame. The interaction between the PLL and the controllers implemented in the stationary reference frame is however appearing indirectly through the transformation of the current references into the stationary coordinates, and these control strategies are therefore more robust with respect to a large grid inductance. However, also the PR- and the hysteresis current controllers can become unstable with a high grid inductance when the operation of the PLL is highly influenced by the converter itself. It is shown that the stability limits of the system are increased by using a slower PLL and allowing for a larger transient phase angle deviation between the PLL and the voltage at the filter capacitors. This will however lead to a slower and less accurate dynamic control performance of the control structures. For stability studies of converters operating in weak grids, correct representation of nonlinearities interactions between the PLL and the current controllers will therefore be critical. This stresses the importance of establishing mathematical models that consider these phenomena, when attempting to carry out a complete analysis VSCs operating in weak grids.

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Appendix I

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Synchronous Reference Frame Hysteresis Current Control for Grid Converter Applications

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***Abstract* — This paper presents the application of space-vector based hysteresis current control in the synchronous reference frame for grid connected voltage source converters. The space-vector based approach allows for systematic application of zero-voltage vectors and prevents high switching frequencies caused by phase interaction. The average switching frequency can be minimized by always selecting the zero-voltage vector that is closest to the previous switching state. For operation in a grid connected converter with LCL-filter, the current references to the hysteresis controllers are given by a DC-link voltage controller and an Active Damping strategy for preventing filter oscillations. Results from simulations and laboratory experiments are presented to discuss the features of the investigated approach compared to traditional phase-current hysteresis controllers.**

***Keywords* — Voltage Source Converter, Converter control, Non-linear control, Active damping**

I. Introduction

The overall performance of current controlled Voltage Source Converters (VSC's) is limited by the response of the inner current control loop. As the utilization of power electronic converters have been increasing during the last decades, current controllers for three-phase VSC's has therefore received significant attention in the literature, and many different control concepts have been developed and analyzed [1], [2].

Hysteresis based control schemes have been known for a long time as a simple and effective way of implementing current control of switching converters. Variable switching frequency, strong load dependency of the average switching frequency, and the possibilities for limit cycle operation with high frequency switching, are well known disadvantages of basic hysteresis controllers. Still, hysteresis current control schemes can be relevant for many applications, due to the fast dynamic performance that is highly robust with respect to changes in systems parameters and operating conditions [1]-[3].

In this paper, a strategy for space vector based hysteresis current control in the Synchronous Reference Frame is applied to a grid connected VSC. The space vector based approach ensures that zero voltage vectors are systematically applied, resulting in lower average switching frequency than for basic hysteresis current controllers. The investigated strategy was originally presented for application to induction motor drives in [4] and it will be shown that the same approach can be applied to a grid connected Voltage Source Converter. This paper will also show how the switching frequency of the investigated controller can be minimized by selecting zero-voltage vectors that requires switching of only one converter leg. In case of an LCL-filter, the current control strategy must also be combined with an active damping algorithm.

The laboratory experiments presented in this paper have been obtained within the project "Power Electronic for Reliable and Energy Efficient Renewable Energy Systems" at SINTEF Energy, supported by The Norwegian Research Council, Wärtsilä, Statkraft and GE.
http://www.sintef.no/OPE

II. Brief Review of Hysteresis Current Control

The most basic implementation of hysteresis control for three-phase VSC's is independent phase-current control by hysteresis comparators generating the gate signals to the converter directly from the current error, as shown in Fig. 1 [1], [3]. In such a control strategy, sinusoidal current references are compared to measured currents and the upper switch in one leg is turned on when the error exceeds the upper tolerance band, and kept on until the current error reaches the lower tolerance band. One of the main problems with this simple control structure is that limit cycle operation can occur at low voltages in systems with isolated neutral, when current error is switched between two phases at very high instantaneous switching frequency. This problem occurs because the current in each phase is influenced by the current in the other phases, and because zero-voltage vectors are not systematically applied [3]. Due to the interaction between the phases, the current error can also reach twice the hysteresis band.

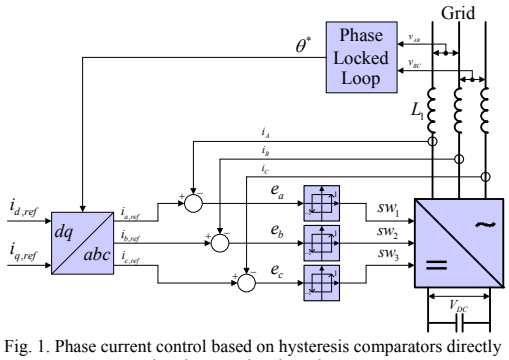


Fig. 1. Phase current control based on hysteresis comparators directly generating the gate signals to the converter

The simple hysteresis control strategy shown in Fig. 1 is still in common use, and simple schemes for suppressing limit cycle oscillations have been suggested as for instance discussed in [5]. However, significant efforts have been made to suggest improved strategies for hysteresis current control. One common strategy is to utilize space-vector based approaches for systematically applying zero-voltage vectors to reduce the switching frequency and avoid the possibility for limit cycle operation. In [6] and [7], this is achieved by using the phase current errors together with a region detector and a switching table for selection of the proper voltage vectors including the zero-voltage vector. Other approaches have been designed for operating in the two phase stationary reference frame and are based on several sets of hysteresis comparators, three-level hysteresis comparators, or comparison of different current error magnitudes [8]-[11]. Utilization of the sign of the current error derivatives as an additional input to switching table-based hysteresis control in the stationary reference frame has also been proposed [12]-[14].

A conceptually different implementation of space-vector based hysteresis current control was proposed by [4] and [11]. This concept, as adapted to a grid connected converter in Fig. 2, is based on three-level hysteresis comparators operating on the current error components in the synchronously rotating dq-reference frame. The gate signals to the converter are then given by a switching table according to the state of the comparators and the angular position of the grid voltage vector.

The principles of the control structure shown in Fig. 2, was discussed for application to induction motor drives in [4], [11] and [15]. A modified version of the same approach has also been presented for application to a STATCOM in [16]. This paper is however discussing the application of the same control strategy for a general purpose grid connected Voltage Source Converter with an LCL-filter. The hysteresis current controller is then the inner loop in a control system where the active current reference is given by a DC-link voltage controller, and the grid voltage phase angle is detected by a Phase Locked Loop (PLL). A strategy for Active Damping of LC-oscillations caused by the wide-spectrum harmonics generated by the hysteresis controller must also be included in the control system.

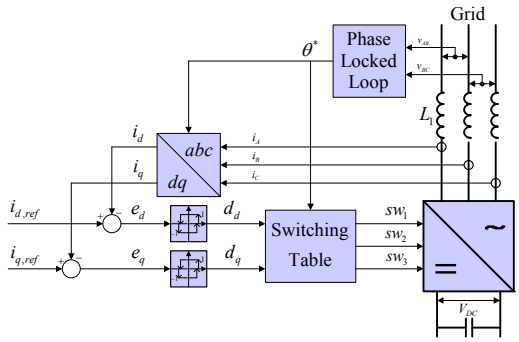


Fig. 2. Space vector based hysteresis current control in the synchronous dq-reference frame with three-level comparators and switching table for generating gate signals to the converter

III. Converter and Control System Configuration

For application to a general purpose grid connected converter, the space-vector based hysteresis current control in the synchronously rotating dq-reference frame from Fig. 2 is used as part of the configuration shown in Fig. 3. The Voltage Source Converter could for instance be the grid interface of a wind turbine or a photovoltaic system, or it could be used as an active rectifier, a reactive power compensator and even as an active filter.

A. System Overview

Fig. 3 shows an overview of the system including both the electrical circuit and the main parts of the control structure. As seen from the figure, the three-phase VSC is connected to a grid through an LCL-filter, where the leakage inductance of a transformer constitutes the grid side inductance of the filter.

For grid synchronization, the voltages at the filter capacitors are measured and a Phase Locked Loop (PLL)

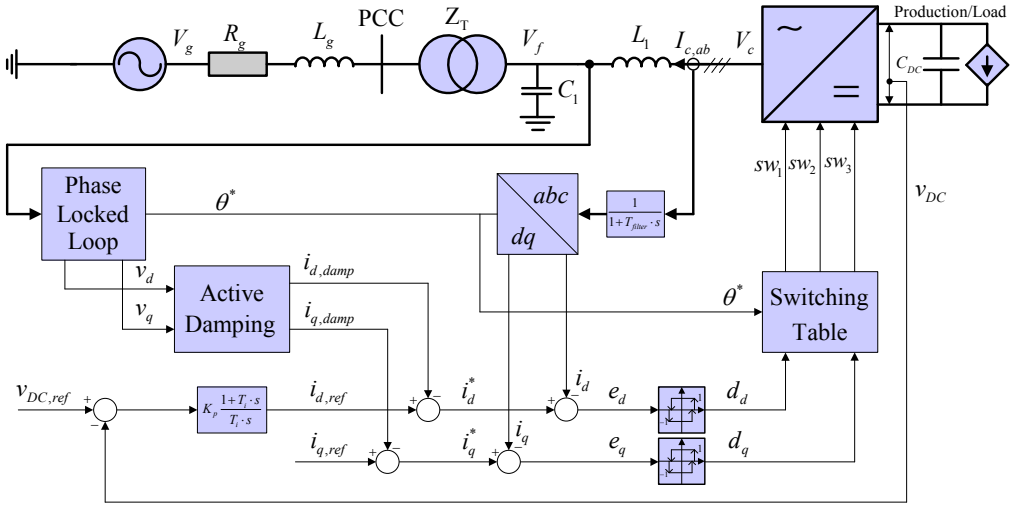


Fig. 3. Grid connected converter with LCL-filter and control system with space-vector based hysteresis current control in the synchronously rotating dq-reference frame, Active Damping of LC-oscillations, DC-link voltage controller and Phase Locked Loop for grid synchronization

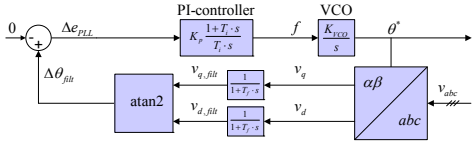


Fig. 4. Phase Locked Loop for detection of grid voltage angular position

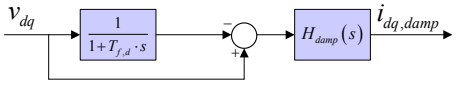


Fig. 5. Active damping of LC-resonances

is used to detect the angular position of the grid voltage vector. The d-axis of the synchronous reference frame is aligned with the grid voltage vector, and the structure of the PLL is shown in Fig. 4, [17], [18].

The DC-link voltage of the converter is controlled by a simple PI-controller that gives the active current reference $i_{d,ref}$. In this case, the reactive current reference is kept at a constant value, but it should be given by a separate control loop if voltage control or reactive power control is required.

In order to suppress LC-resonances in the LCL-filter, an Active Damping mechanism is included in the control system [19], [20]. The applied approach is based on high-pass filtering of the d-and q-axis components of the voltage measured at the filter capacitors as show in Fig. 5. The filtering time constant $T_{f,d}$ determines the frequency range of the damping effect, and the transfer function H_{damp} can be selected to get suitable suppression of the high frequency resonances [20]. For simplicity, only a proportional gain is used for $H_{damp}(s)$. The output signal from the damping mechanism is subtracted from the current references as shown in Fig. 3, giving modified reference values that will suppress the LC-oscillations.

The current error signals used for the hysteresis current control are calculated in the dq-reference frame. The measured phase currents are therefore transformed into the synchronous reference frame by using the grid voltage phase angle, θ*, from the PLL.

B. Details of the applied hysteresis current controller

To generate the switching signals to the converter gate-drives, the output of two three-level hysteresis comparators based on the d- and q-axis current error signals are used as input to a switching table. The synthesis of the three-level comparators and the switching table will be briefly explained in the following subsections.

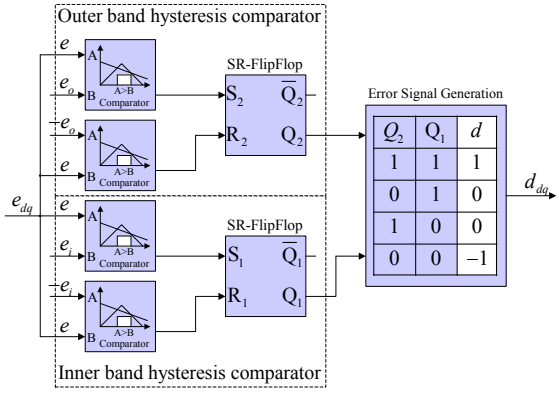
1) Three-level hysteresis comparators

The use of the three-level hysteresis comparators on the current errors is what enables the systematic application of zero voltage vectors in the presented control system [4], [11]. A three-level hysteresis comparator can be constructed from two traditional hysteresis comparators as shown in Fig. 6a). Each hysteresis element consists of two separate comparators and a SR Flip-Flop that is set when the error signal is above the upper threshold and reset when the error signal is below the lower threshold. The three-level hysteresis effect is obtained when the outputs of two sets of hysteresis comparators with different hysteresis bands are combined to give three possible error signals as seen from the table given in the figure. For the investigated control strategy, the hysteresis comparators are configured with a set of inner and outer bands centered with respect to zero, and the values of the resulting error signals can be given the following simple interpretation:

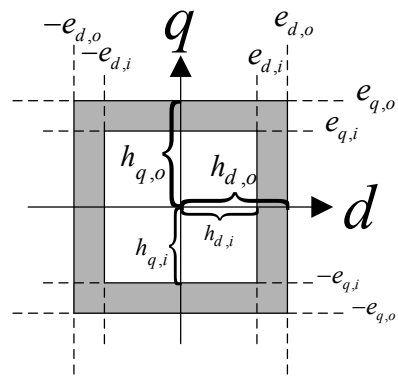
- If the error signal is equal to 1, a positive voltage should be applied in the corresponding axis to increase the current and thus reduce the current error.
- If the error signal is 0, zero voltage can be applied in the corresponding axis.
- If the error signal is equal to -1, a negative voltage should be applied in the corresponding axis to reduce the current.

The operation of the three-level hysteresis comparator will result in an error signal that will be changing between 0 and a value depending on the state of the hysteresis comparator representing the outer band. The state of the outer comparator will change when the switching actions caused by the inner hysteresis band are not enough to control the current, so that the current error reaches the outer hysteresis band.

The inner and outer hysteresis bands of the d- and q-axis current components can be represented in the dq-plane as shown in Fig. 6c), where the buffer zone between the inner and outer hysteresis bands is shown in grey. This representation of the hysteresis bands gives an inner and outer area for the current error trajectory in the dq-reference frame. When the hysteresis bands are equal in the d- and q-axis, this area will be square, while different bands in the d- and q-axis result in a rectangular area.



a) Implementation of three-level hysteresis comparators



b) Tolerance area in the dq-reference frame

Fig. 6. Three-level comparators for generating error signals and resulting tolerance area in the dq-reference frame

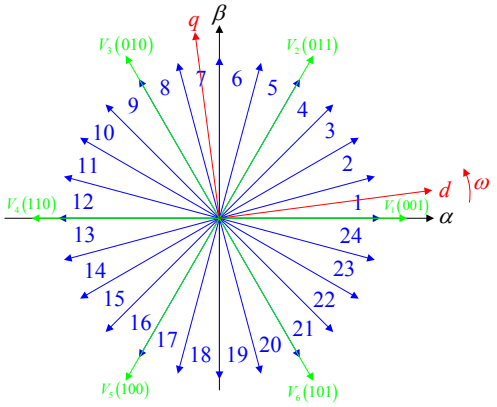


Fig. 7. Two-dimensional voltage vector plane divided into 24 sectors

2) Switching table

The error signals from the three-level hysteresis comparators operating on the d- and q-axis current errors are used as input to a switching table for generating the converter gate signals. This switching table is therefore of main importance to the operation of the hysteresis current controller. The synthesis of the switching table is explained in detail in [4] where this hysteresis current control strategy was first introduced for field oriented control of induction motor drives. The approach will however be reviewed here for application to a grid connected converter.

In the system shown in Fig. 3, the proposed hysteresis controller will operate on the d- and q-axis current components in the filter inductor. With an inductance value of L_1 and an internal resistance of R_{L1}, the per unit mathematical model of the inductor in the synchronous reference frame is given by (1). This equation is similar to the model of an induction machine with a counter-induced voltage behind the leakage inductance, and the same switching table as developed for induction machine drives can therefore be used.

$$i_d = \frac{1}{r_{L_1}} \frac{1}{1+T_{L_1}\cdot s}\left[v_{c,d} - v_{f,d} + \omega \cdot l_1 \cdot i_q\right]$$
$$i_q = \frac{1}{r_{L_1}} \frac{1}{1+T_{L_1}\cdot s}\left[v_{c,q} - v_{f,q} - \omega \cdot l_1 \cdot i_d\right] \quad (1)$$

The switching table can be synthesized by dividing the stationary frame vector plane into 24 sectors, as shown in Fig. 7. Then, the most suitable voltage vector for each of the possible combinations of output signals from the d- and q-axis three-level hysteresis comparators must be identified for every sector. Since there are 9 different combinations of d- and q-axis error signals for each sector of the vector plane, the switching table will have 9x24 elements. The complete switching table is reproduced in TABLE I [4], [11]. The non-zero voltage vectors are labeled from V_1 to V_6 as given by Fig. 7.

The division of the vector plane into 24 sectors originates from the 6 non-zero voltage vectors from a two-level three-phase voltage source converter, and the 4 different directions of current deviation in the synchronously rotating dq-reference frame. By using Fig. 7, it can also be verified that the most suitable voltage vector for at least one combination of error signals from the d- and q-axis hysteresis comparators will change for each sector of 15°.

TABLE II. CHOICE OF ZERO VOLTAGE VECTORS

Previous vector	V_1 (001)	V_2 (011)	V_3 (010)	V_4 (110)	V_5 (100)	V_6 (101)
Zero-vector	V_0 (000)	V_7 (111)	V_0 (000)	V_7 (111)	V_0 (000)	V_7 (111)

C. Selection of zero-voltage vectors

The switching table from [4] and [11] allows for systematically applying a zero-voltage vector when the output from both three-level comparators is 0. Using the table to set the gate signals directly will switch the converter to a fixed zero-voltage vector, even if both the switching states (000) and (111) are zero-voltage vectors. This will result in unnecessary switching actions. These unnecessary switching actions can be avoided by storing the previous voltage vector, and choosing the zero-voltage vector that requires only one of the switches to change its state. This resulting selection of zero-voltage vectors is shown in TABLE II.

D. Parameterization of three-level comparators

The parameterization of the three-level comparators was not thoroughly discussed in the first descriptions of hysteresis control in the synchronous reference frame from [4] and [11]. It was however noted that selection of different bands in the d-and q-axis could be beneficial for reducing torque ripples in induction motor drives. The same freedom to select different tolerance bands in the d- and q-axis also apply to a grid connected converter, but this will be of minor importance unless theoretical details of instantaneous power components are studied. Selection of the values for the inner and outer hysteresis bands, and especially the difference between these bands, is however important for practical utilization of this control concept.

One important restriction on the parameterization of the three-level comparators is related to the total time-delay of the system from the time when a change in the output voltage vector is given until the effect is seen at the current errors used as input to the three-level comparators. This total time-delay will be influenced by the bandwidth of the current sensors, any input signal conditioning, the delay in the internal processing pipeline of the control

TABLE I. SWITCHING TABLE FOR IMPLEMENTATION OF dq-HYSTERESIS CURRENT CONTROL BASED ON THREE-LEVEL COMPARATORS

d		Sector																							
d_d	d_q	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
1	1	V_2	V_2	V_2	V_3	V_3	V_3	V_3	V_4	V_4	V_4	V_4	V_5	V_5	V_5	V_5	V_6	V_6	V_6	V_6	V_1	V_1	V_1	V_1	V_2
1	0	V_1	V_1	V_2	V_2	V_2	V_2	V_3	V_3	V_3	V_3	V_4	V_4	V_4	V_4	V_5	V_5	V_5	V_5	V_6	V_6	V_6	V_6	V_1	V_1
1	-1	V_6	V_1	V_1	V_1	V_1	V_2	V_2	V_2	V_2	V_3	V_3	V_3	V_3	V_4	V_4	V_4	V_4	V_5	V_5	V_5	V_5	V_6	V_6	V_6
0	1	V_3	V_3	V_3	V_4	V_4	V_4	V_4	V_5	V_5	V_5	V_5	V_6	V_6	V_6	V_6	V_1	V_1	V_1	V_1	V_2	V_2	V_2	V_2	V_2
0	0	V_0	V_0	V_0	V_0	V_0	V_0	V_0	V_0	V_0	V_0	V_0	V_0	V_0	V_0	V_0	V_0	V_0	V_0	V_0	V_0	V_0	V_0	V_0	V_0
0	-1	V_6	V_6	V_6	V_6	V_1	V_1	V_1	V_1	V_2	V_2	V_2	V_2	V_3	V_3	V_3	V_3	V_4	V_4	V_4	V_4	V_5	V_5	V_5	V_5
-1	1	V_3	V_4	V_4	V_4	V_4	V_5	V_5	V_5	V_5	V_6	V_6	V_6	V_6	V_1	V_1	V_1	V_1	V_2	V_2	V_2	V_2	V_3	V_3	V_3
-1	0	V_4	V_4	V_5	V_5	V_5	V_5	V_6	V_6	V_6	V_6	V_1	V_1	V_1	V_1	V_2	V_2	V_2	V_2	V_3	V_3	V_3	V_3	V_4	V_4
-1	-1	V_5	V_5	V_5	V_6	V_6	V_6	V_6	V_1	V_1	V_1	V_1	V_2	V_2	V_2	V_2	V_3	V_3	V_3	V_3	V_4	V_4	V_4	V_4	V_5

system and the turn-on and turn-off delays of the power semiconductors. In cases where the total delay is significant, and the maximum current derivative is large, the detected current error may pass from the inner hysteresis band to the outer hysteresis band before the influence of a new switching vector is seen on the current error. In such a case, non-optimal switching sequences will occur, and the switching table will not be utilized according to the intention. An idealized situation where the system is on the limit of such a problem is shown in Fig. 8. To avoid this condition, the difference between the outer and the inner hysteresis bands should fulfill the criteria specified by (2).

$$\left(e_o - e_i\right) > \left|\frac{di_{dq}}{dt}\right|_{\max} \cdot \left(T_{filter} + T_{delay} + T_{dead-time}\right) \tag{2}$$

This discussion, and the criteria specified by (2), shows that the delay of the system will be critical if a small difference between the inner and outer hysteresis bands is selected. For simulating a system under such conditions, representation of system delays will then be of significant importance for the validity of the obtained results.

It can also be noted that conflictive situations can occur if both the d- and q-axis deviations reach their bands at the same time. Since it will be easier to correct the current deviation in the q-axis where there is no counter-voltage from the grid, such a situation might cause the d-axis current to pass outside its outer band while the current in the q-axis is forced to the other side of its tolerance region. To avoid such situations, the outer hysteresis bands of the q-axis current can be relatively wide, so that the converter can correct the d-axis current while the q-axis current is within the buffer zone between the inner and the outer hysteresis band. A set of conditions for the ratio between inner and outer hysteresis bands, that have resulted in reasonable results for both simulations and laboratory experiments presented in this paper is given by (3). Here, the inner hysteresis bands $e_{d,i}$ and $e_{q,i}$ are set equal so that the inner tolerance area is square.

$$e_{d,o} \approx \sqrt{2} \cdot e_{d,i} \qquad \sqrt{2} \cdot e_{q,i} \le e_{q,o} < 2 \cdot e_{q,i} \tag{3}$$

IV. Investigation of Operaitonal Characteristics

To verify the operability of the space-vector based dq - hysteresis control system, and to discuss its operational characteristics, the proposed control system has first been simulated with the PSCAD/EMTDC software and then implemented for control of a reduced scale laboratory converter setup. The basic phase current hysteresis control from Fig. 1 has also been simulated and implemented in the laboratory setup as a reference-case.

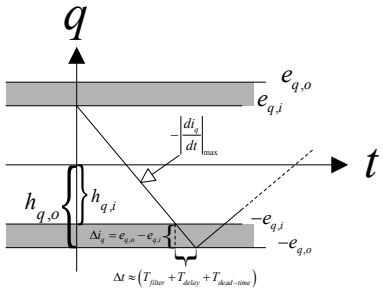


Fig. 8. Current error in q-axis passing through the buffer zone between the inner and outer hysteresis bands with maximum rate of change

A. Simulation results during normal operation

The system for investigations by simulation studies is based on a converter rated for 2.5 MVA at 690 V_{RMS} line voltage with 5% filter inductance L_1 and 10% filter capacitance C_1. A total grid inductance of 0.20 pu including the leakage inductance of the grid side transformer is included in the model, and the system is connected to a stiff voltage source at 22 kV_{RMS} line voltage. An average switching frequency of about 3 kHz is assumed as the starting point and three different cases have been simulated; 1) phase current hysteresis, 2) dq-hysteresis control based on three-level comparators with fixed zero-vector, 3) dq-hysteresis control based on three-level comparators with zero-vector selection.

Fig. 9 shows the simulated phase-currents and the current error trajectories when the converter is operated as a generator with about 0.8 pu power being fed to the DC-link. The DC-link voltage is controlled to 1.0 pu voltage, corresponding to about 1.1 kV. The tolerance band of the phase current hysteresis controllers are selected by trial and error to obtain an average switching frequency close to 3 kHz under these operating conditions. The inner tolerance bands of the dq-hysteresis are then set to the same values. The outer tolerance band in the d-axis is set to √2 times the inner value, while the outer band in the q-axis is set to 2 times the inner value. This result in approximately the same average switching frequency for the phase current hysteresis and the dq-hysteresis with fixed zero-vector.

In the first column of Fig. 9, the well known characteristics of the phase current hysteresis is seen. The second column shows that the phase currents with dq-hysteresis are almost the same as for the phase current hysteresis, but the distribution of the current ripple is slightly different. This is more clearly seen from the plots of the current error trajectories, where the characteristic star-shape of the current error for the phase current hysteresis is replaced by a more circular area in the stationary reference frame. In the rotating reference frame, the borders of inner current error area for the dq-hysteresis controllers can be clearly seen, and the limits of the outer band for the q-axis comparators can also be identified. The d-axis current error is mainly operating within the inner hysteresis band, with some deviations in the direction of positive errors. This is due to the grid voltage that is acting in the d-axis, forcing the error in the positive direction. If the grid voltage is low, the d-axis current deviation can also reach the lower, outer, hysteresis band and the switching table elements corresponding to a negative d-axis current error signal will be utilized.

The third column in Fig. 9 shows the result when zero-voltage vectors are selected according to the information in TABLE II. As expected, there is no significant difference in the currents between this case and the case with fixed zero-vector. The slight differences in current error trajectories that can be observed are mainly because the captured results are not reflecting exactly the same sequence of non-zero switching actions because of extreme sensitivity to initial conditions due to the chaotic nature of hysteresis controllers.

The number of switching actions in each leg of the converter is compared for the three simulated cases in Fig. 10. These curves shows that the distribution of switching actions over one fundamental frequency period is quite

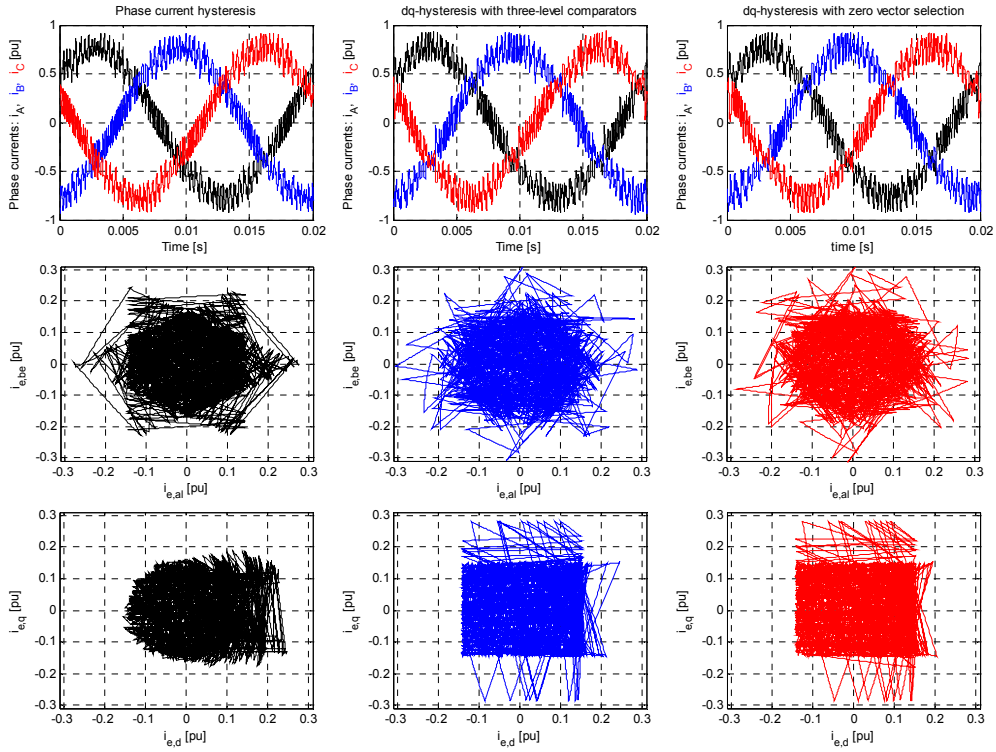


Fig. 9. Simulation results showing phase currents together with current error trajectory in the stationary reference frame and in the synchronous dq-reference frame when 0.8 pu power is being fed to the DC-link

different for the phase current hysteresis and the dq-hysteresis with fixed zero vector, even if total number of switching actions is almost the same. In case of the dq-hysteresis with fixed zero-vector, the switches in each phase have significant periods with almost no switching actions, while the distribution is more random for the phase-current hysteresis controller.

When applying the strategy for selection of zero vectors, it is seen that the total number of switching actions is significantly reduced. In this case, the average switching frequency is reduced from about 3000 Hz to about 2500Hz with exactly the same hysteresis bands, and no significant difference in the current waveform. It is also seen that the distribution of switching actions becomes much more regular with 4 short periods without switching actions during each fundamental frequency cycle.

It can however be noted that the simulations with dq-hysteresis results in slightly higher THD and RMS ripple in the filter currents under the simulated conditions.

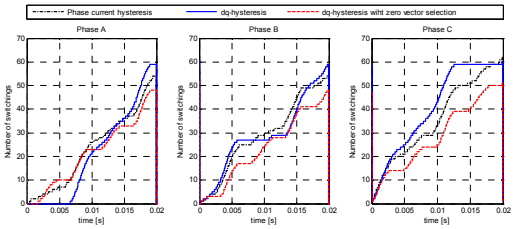


Fig. 10. Simulation results showing number of switching actions in each phase-leg of the converter for one fundamental frequency period

However, if the strategy for zero vector selection is applied, and the bands are adjusted so that the average switching frequency is kept at 3 kHz, the dq-hysteresis will obtain similar or lower distortion than the phase current hysteresis. When operating at lower voltages, the situation will however be different, and the benefit of systematically applying zero vectors will be larger.

It can also be noted that the long periods without switching actions when using the dq-hysteresis with fixed zero-voltage vector can be disadvantageous with respect to thermal cycling of the semiconductors. The regular distribution of switching actions for the dq-hysteresis with zero vector selection can however be beneficial compared to the random distribution of switching actions resulting from the phase current hysteresis. This could be further investigated by evaluating the total semiconductor losses with the different control strategies.

B. Experimental testing

The investigated hysteresis controllers are also tested in a laboratory setup to verify the simulation results and to further investigate the operational characteristics of the different control strategies.

1) Experimental setup and controller implementation

The basis for the laboratory experiments is a 20 kW IGBT converter module developed specifically for laboratory setups. The IGBT driver circuits have a turn-on delay of 3 us and a turn-off delay specified to 1 us. The converter is connected to the grid through a LC-filter with inductance of 0.5 mH and Y-connected capacitors of 50

µF. This system is connected to the grid via a transformer with variable turns ratio, and is operated with 230 V_{RMS} and 40A_{RMS} as base values.

The control systems are implemented on a processor board based on a Xilinx Virtex FX30T FPGA, shown in Fig. 11 [21], [22]. The FPGA fabric runs at 100 MHz clock frequency, while the PowerPC processor core that is embedded on the FPGA chip runs at 300 MHz. Voltage and current signals are fed into the FPGA by a fast Analog-Digital converter (8 channels, 12 bit, 40 MSPS). Total signal delay in the AD converter and buffer amplifier stages is about 300 ns. The FPGA is configured by using the Xilinx Embedded Development Kit (EDK).

The functions needed for the hysteresis controllers are programmed as modules in VHDL and connected to a signal processing pipeline that is able to work at the same sampling rate as the AD converter. The additional delay caused by the control system implementation is therefore insignificant. Less time critical parts of the control system, as the PI-controller of the PLL and the DC-link controller, are handled by processor routines that are running at 0.2 ms update rate.

Internal signals from the control system are made available for external measurements through a set of Digital-Analog converters. The experimental results presented in the following subsections are thus obtained by an oscilloscope and processed in Matlab for plotting the results.

2) Steady-state operation of the different controllers

To verify the validity of the simulation models, the same three cases as simulated in section IV.A were tested in the laboratory setup. For convenience, the converter was operated as load with about 40A_{RMS} constant active current while a voltage controlled brake chopper with a load resistor was used to keep the DC-link voltage at 375 V. The hysteresis bands were adjusted to obtain about 3 kHz average switching frequency for the phase current controllers and for the dq-hysteresis control with fixed zero-vector, according to the same criteria as used for the simulations.

The main results from these experiments are shown in Fig. 12, and the curves are corresponding very well with the results from the simulations studies. The slight differences between the simulation results and the experimental results are mainly due to the delay caused by the signal processing in the control system and the signal delay and dead time of the gate drivers.

The number of switching actions in phase A for two fundamental frequency periods, as obtained from the laboratory experiments with the different control

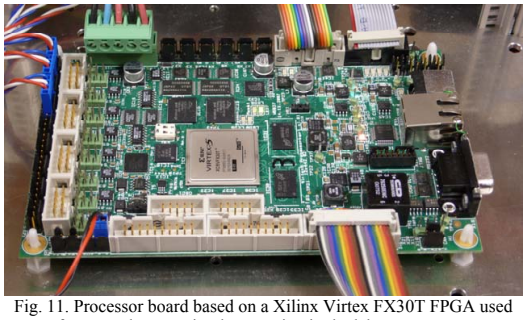


Fig. 11. Processor board based on a Xilinx Virtex FX30T FPGA used for control system implementation in the laboratory setup

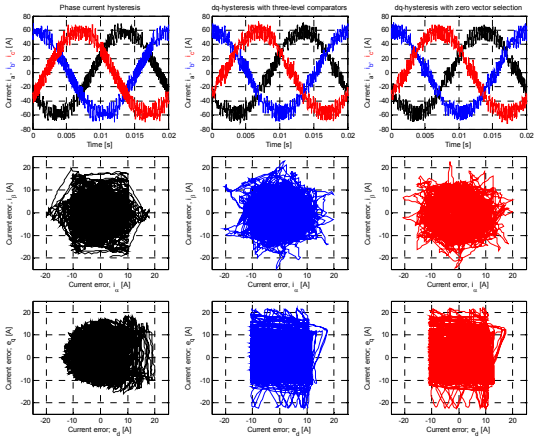


Fig. 12. Laboratory measurements obtained at 230V_{RMS} grid voltage with DC-voltage of 375V and 40A_{RMS} active current. The curves are showing the phase currents and the current error trajectories in the stationary reference frame and in the synchronously rotating dq-reference

strategies, is shown in Fig. 13. These results are also corresponding closely to the simulation results from Fig. 10, and show the same characteristics as already discussed. The operability of the space-vector based dq-hysteresis current control for a grid connected converter is thus verified by both simulations and experiments.

3) Influence of measurement filtering

A low pass filter in the current measurements was included in the control system for smoothing of switching transients. For the laboratory testing, the filter time-constant could be varied from 0.1 to 10 µs, and this was tested to investigate the influence of filtering delays on the performance of the control system. It was easily verified that a time constants of 1 µs or less had minor influence on the results. However, the sensitivity to signal delay was verified by increasing this filter time constant and changing the ratio between the inner and outer hysteresis bands. The results showed how significant filtering effects or too small buffer zone between the inner and outer hysteresis band is reducing the performance of the dq-hysteresis controller and will cause transient currents outside the tolerance area, as discussed in section III.D.

4) Verification of Active Damping

The operation of the Active Damping strategy has also been tested by laboratory experiments, but only results from the dq-hysteresis with zero vector selection will be shown here. In order to obtain a clear case with little direct influence of current ripple on the voltage, the tolerance

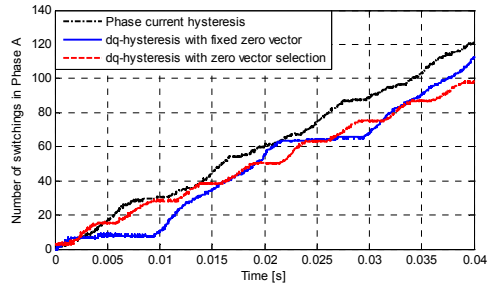
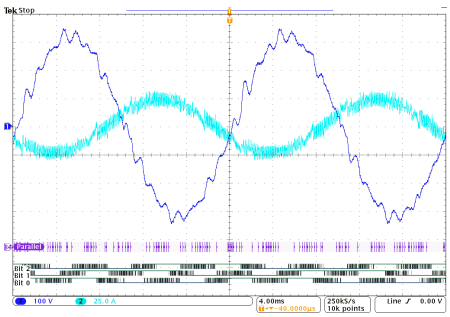
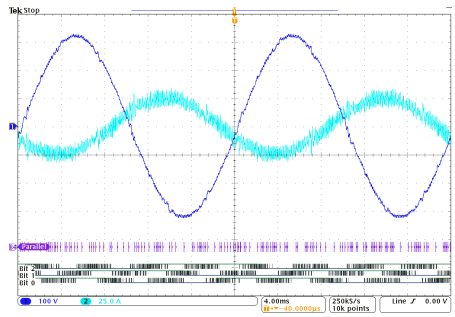


Fig. 13. Number of switching actions in phase A the during two fundamental frequency periods obtained from laboratory experiments



a) Voltage and current measurements with Active Damping disabled



b) Voltage and current measurements with Active Damping enabled

Fig. 14. Measured voltage and current in laboratory setup controlled by dq-hysteresis with and without Active Damping

band was reduced so that the switching frequency increased to about 4.8 kHz. The outer bands of both the d- and q-axis current errors were set to 2 times the inner bands.

A set of results without Active Damping are shown in Fig. 14 a) as an oscilloscope screenshot with one line-voltage measured at the filter capacitors and one phase-current. The gate-signals from the switching table are also shown in the lowest part of the figure. Some LC-oscillations can be seen in the voltage curve, but they are in this case well damped, mainly due to a relatively high resistance in the power supply. A case with a high power converter in a real grid with less passive damping will give more pronounced and less damped oscillations.

The effect of the Active Damping function is clearly seen in Fig. 14 b), where the converter is running at the same operating point as before but with Active Damping enabled. In this case, the voltage is nearly sinusoidal and any LC-oscillations caused by the switching actions of the converter are quickly forced to zero.

C. Switching frequency as function of grid voltage

As mentioned, one of the main drawbacks of the simple phase current hysteresis control is the possibility for limit cycle operation with intervals of very high switching frequency. This is less likely to occur under normal operating conditions in a grid connected converter than for a motor drive system, since the grid voltage will stay around its nominal value most of the time. However, in case of grid faults, the converter may be required to operate for a short time with very low grid voltage. This will especially be the case for renewable energy applications where there are requirements for Low Voltage Ride Through capability. In such cases the possibility for limit cycles can be a limitation for continuous operation of the converter.

In Fig. 15, the average switching frequency of the three-phase converter is mapped as a function of the grid voltage for the different hysteresis current controllers discussed in this paper. The switching frequency is mapped for operation as generator, as load, for injection of reactive current, for consumption of reactive current and for no-load conditions [23]. These simulations are carried out with the model from section IV.A, but with fixed DC-link voltage and fixed current references that are independent of the grid voltage. The lower right plot of Fig. 15 is obtained from the laboratory setup, and is provided as a verification of the trends obtained from the simulations.

The results in Fig. 15, show that the switching frequency of the phase current hysteresis controller increases as the voltage drops, until a certain point around 50-70 % of rated voltage, depending on the current references. One reason for this is that reduced grid voltage increases the current derivative when the converter is applying voltage to increase the current. Around this local peak of the switching frequency, the interaction between the phases also causes the phase current controllers to enter a state where the current in one phase is drifting within the tolerance band, while the other two phases are switching rapidly. This is similar to limit cycle operation, but without causing excessively high instantaneous switching frequencies. As the grid voltage is further reduced, the length of these periods is reduced while the possibilities for applying zero-voltage vectors increases.

The space-vector based hysteresis controllers also show a trend of increasing switching frequency as the grid voltage is reduced. Since the phase interaction is implicitly handled by this approach, the average switching frequency is only increasing due to the higher average current derivative. As expected, selection of the nearest zero vector always results in less switching actions.

When the voltage is further reduced, the switching

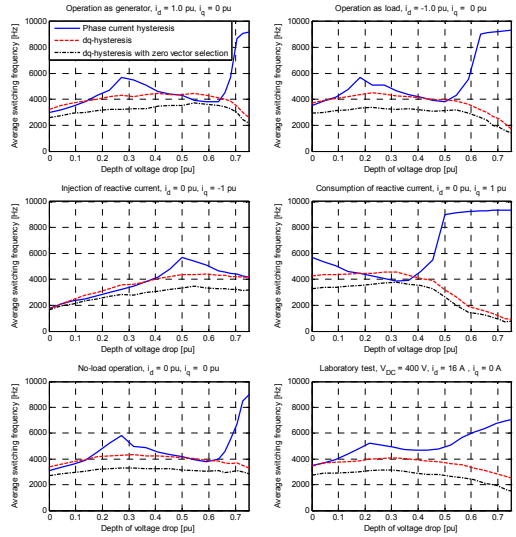


Fig. 15. Average switching frequency as function of grid voltage for different operating conditions obtained from simulation studies and laboratory testing

frequency of the phase current controllers is decreasing again, and in the simulations it can reach down to the same level as for the space-vector based control. For very low voltages, the limit cycle operation and phase interaction of the phase-current hysteresis is however resulting in very high switching frequencies. This problem is completely avoided with the space-vector based approach, as zero vectors can be applied for longer time, resulting in low switching frequencies at low grid voltages.

Considering the results in Fig. 15, it should be remembered that the currents of the converter will influence the voltage at the filter capacitors. The local maximum of switching frequency for the different operating conditions is therefore mainly depending on the voltage at the grid side of the filter inductors. This can be seen from the curves since they all have similar profiles, only shifted to different values of the grid voltage.

In the measurements from the laboratory setup, the average switching frequency for the phase current controller is increasing less when the voltage is reduced compared to the results from simulations. The minimum switching frequency and the maximum switching frequency at low voltages also have less extreme values. This smoother switching frequency profile might be caused by the delays, the current filtering and the blanking time of the real converter, since these effects are not included in the simulation models. The main shape of the switching frequency profile as function of the grid voltage is however verified, and demonstrates the beneficial properties of the space vector-based dq-hysteresis control with respect to zero-vector utilization.

V. Conclusion

This paper has investigated space-vector based hysteresis current control in the synchronously rotating reference frame for grid connected voltage source converters. The presented approach was originally proposed for induction motor drives, and in this paper the control structure is expanded to include DC-link voltage control and active damping of LC-resonances. The implementation of the control system is explained, and the operation is verified by simulations and laboratory experiments. This paper also shows how the average switching frequency of the converter can be minimized by selecting the zero-voltage vectors according to the previous switching state of the converter.

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