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Isolated Full-Bridge DC-DC Converter Configurations for Photovoltaic Applications using Modular Multilevel Converter

Guro Watten Furu

Master of Energy and Environmental Engineering
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Supervisor: Lars Einar Norum, IEL

Norwegian University of Science and Technology
Department of Electric Power Engineering

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Abstract

Traditionally, photovoltaic (PV) systems have used two- or three-level converters in conjunction with a step-up transformer in the connection to the grid. The transformer provides isolation at the point of common coupling to protect the PV system from the grid, however, this necessarily increases the total cost of the plant.

Recently, the Modular Multilevel Converter (MMC) inverter got introduced as an attractive topology for PV plants due to a high scalability that facilitates a direct connection to medium voltage grid without the use of a step-up transformer. The required voltage level is achieved by designing the MMC with the correct number of submodules. It also provides high MPPT tracking, which gives the MMC several advantages over conventional PV inverters. The isolation in such a configuration can be provided between the PV strings and the submodules of the MMC by utilizing isolated DC-DC converters.

In this study, different isolated full-bridge DC-DC converter configurations with high efficiency rate are presented. The single-unit configuration provides a simple structure, but requires high voltage and current ratings on equipment due to the high power transfer. By utilizing a parallel- or series-connection of converters, the bulk transmission of power to the submodules is distributed, which increases the overall reliability of the system. If the PV string operating voltage is not equal to the submodule capacitor voltage, then a step-up in voltage is necessary. However, the PV strings are in this study designed such that the HF transformer turns ratio is 1:1 in all configurations.

The parallel-arrangement avoids the parallel-connection of switching devices in the DC-DC converter in order to handle the high currents. In case of the series-arrangement, the voltage stress on the switching device is reduced considerably. Due to the reduced voltage, an utilization of GaN devices is possible, resulting in a higher switching frequency range of operation. Simulations are performed in order to find the efficiency of the different isolated DC-DC converter configurations.

Furthermore, the obtained efficiency curves are utilized in a simulation model in order to find the overall energy efficiency and the levelized cost of energy (LCOE) of the MMC PV plant configurations. These configurations are also compared to a central inverter (CI) PV configuration and a multi-string central inverter (MSCI) PV configuration in order to state the benefits of utilizing the MMC as inverter in medium voltage PV plants.

The simulations verifies the improved energy efficiency and the lowered LCOE when utilizing MMC over the CI and the MSCI configurations in medium voltage PV plant applications. They also presents the high efficiency of the isolated DC-DC converter configurations. When utilizing the GaN HEMTs in the series-arrangement, high efficiency is obtained at high-switching frequency. However, these simulations and calculations do not address losses in the HF transformer.

Summary

As a result of the continuously increasing carbon emissions, the global demand for cleaner energy is rising. Grid-connected photovoltaic (PV) systems is an attractive solution to provide green energy, and PV technology has therefore gained increased attention which has resulted in higher efficiency PV panels. PV plants have benefited with increased annual energy yield, and the never before has solar energy contributed with more new power capacity to the power grid. However, variable power production due to unpredictable weather conditions pose a challenge for optimal planning, grid operation, and grid stability.

A replacement of the classic inverter with Modular Multilevel Converter (MMC) got introduced as an attractive topology for PV plants due to a high scalability that facilitates a direct connection to medium voltage grid without the use of a step-up transformer. The required voltage level is achieved by designing the MMC with the correct number of submodules. It also provides high MPPT tracking, which gives the MMC several advantages over conventional PV inverters. The isolation in such a configuration can be provided between the PV strings and the submodules of the MMC by utilizing isolated DC-DC converters.

Different isolated full-bridge DC-DC converter configurations with high efficiency are investigated in this study. The single-unit full-bridge configuration provides a simple structure, but requires high voltage and current ratings due to the high power transfer. By utilizing a parallel- or series-connection of converters, the bulk transmission of power to the submodules is distributed, which increases the overall reliability of the system. If the PV string operating voltage is not equal to the submodule capacitor voltage, then a step-up in voltage is necessary. However, the PV strings are in this study designed such that the HF transformer turns ratio is 1:1 in all configurations.

The parallel-arrangement avoids the parallel-connection of switching devices in the DC-DC converter in order to handle the high currents. SiC MOSFETs have been utilized in the full-bridge due to the high voltage rating. Simulations have been performed at different DC-link voltages, at many different switching frequencies and for the entire operating range of 0.1-1 per unit power in order to find the efficiency. A 50% reduction in the current through each full-bridge results in a 50% reduction in the total copper losses. The copper losses are proportional to the square current, and by reducing the current by 50%, the total copper losses is reduced by 50%. However, the voltage rating is the same when assuming an unity voltage transformer ratio.

In case of the series-arrangement, the voltage stress on the switching device is reduced considerably. Due to the reduced voltage, an utilization of GaN devices is possible. GaN switching devices have a lower voltage rating than SiC. However, they have shown a superior performance, especially at high-frequency operation. High-frequency operation is beneficial due to reduced size of the HF transformer. The efficiency of the GaN-based series-connected full-bridge DC-DC converter was obtained by calculations of the switching and conduction losses by assuming a worst-case duty ratio of 0.5. The results gave a high efficiency of 98% for a operating range up to 200 kHz switching.

The obtained efficiency curves were utilized in a simulation model in order to find the overall energy efficiency and the levelized cost of energy (LCOE) of the MMC PV plant configurations. These configurations were also compared to a central inverter (CI) PV configuration and a multi-string central inverter (MSCI) PV configuration in order to state the benefits of utilizing the MMC as inverter in medium voltage PV plants. The MMC topologies, as well as the MSCI topology, provides lower MPPT losses due to the distributed MPPT in comparison with the CI configuration. The MMC configurations had a better energy efficiency for all the different DC-DC converter configurations compared to both the CI and the MSCI configuration.

For the MMC utilizing the single-unit DC-DC configuration, the energy efficiency was obtained to be 95.28% for the best-case switching frequency at 1 kHz, and 94.40% for the worst-case switching frequency at 20 kHz. The CI and MSCI efficiency was in comparison 89.63% and 90.11% respectively. However, the MMC configurations did not account for losses in the HF transformer in the DC-DC configurations. It was assumed that these losses do not account for a great part of the total losses in the PV plant, and the results would have been almost the same when accounting for them.

For the MMC utilizing a parallel-connection of DC-DC converters, the energy efficiency was obtained to be 95.25% at 10 kHz switching. In the MMC utilizing the GaN-based series-connection of DC-DC converters, the energy efficiency was calculated to be 95.01% at 20 kHz switching, and 94.39% at 200 kHz switching.

The levelized cost of energy (LCOE) was also found for all the different PV configurations. The LCOE was shown to be 6.25% lower for the MMC utilizing the single-unit DC-DC converter compared to the CI configuration, and 6.21% and 5.76% lower for the MMC utilizing the parallel- and series-connection of DC-DC converters respectively. This shows the great benefits of utilizing the MMC instead of the conventional PV inverters.

Another important aspect is that partial shading is not considered in these simulations. The MMC configurations will increase the MPPT substantially, resulting in a even higher extracted energy compared to the CI configuration during partially shaded and non-equalized irradiance conditions in the PV plant. The parallel- and series-connection of DC-DC converters increases the MPPT more than the single-unit DC-DC converter configuration. This will result in a substantially decrease in the LCOE of the MMC PV configurations compared to the CI configuration.

A higher number of series- or parallel-connected DC-DC converter may result in higher efficiency and lower losses, but at the cost of a more complex system and a higher price due to more components. The number of series- and parallel-connected devices must therefore be selected with care.

The simulations on the proposed MMC PV plant configurations verified the improved energy efficiency and the lowered LCOE when utilizing MMC over the CI and the MSCI configurations in medium voltage PV plant applications.

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A specialization project, completed by the author in the autumn of 2017, gave a preliminary analysis for this thesis. The assignment was initially proposed by ABB, and the scope was later redefined to propose different topologies for isolated full-bridge DC-DC converters to interface Photovoltaics to the Modular Multilevel Converter in order to increase the efficiency of the DC to AC power conversion. Basic topics that are not directly relevant for the specific topic of the thesis are either left out or only given in short sections instead of reproducing text from the specialization project.

This year has been challenging, but also full of learning experiences. I have thoroughly enjoyed working on this topic for my thesis. I have been fortunate enough to have had several people support me this year, both personally and in my academic endeavors.

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Table of Contents

Abstract i

Summary iii

Preface v

Table of Contents ix

List of Tables xii

List of Figures xv

Nomenclature xvi

I Introduction 1

1 Background 3
- 1.1 Grid-connected Photovoltaic Applications 3
  - 1.1.1 Trends 3
  - 1.1.2 PV Penetration Challenges and Issues 4
  - 1.1.3 PV Inverter Topologies 5
- 1.2 Motivation and Objectives 7
- 1.3 Problem Description 8
- 1.4 Implementation Tools 8
- 1.5 Thesis Outline 9

II Theory 11

2 Medium Voltage Grid-Connected MMC for PV Applications 13
- 2.1 Modular Multilevel Coverter 13

2.1.1 Configurations . . . 13
2.1.2 Circuit Topology . . . 16
2.1.3 Operation . . . 16
2.2 PV MMC Plant Description . . . 18

3 Isolated DC-DC Converters 21
3.1 Introduction . . . 21
3.1.1 Classification . . . 22
3.2 Full-Bridge Isolated DC-DC Converters . . . 23
3.2.1 Efficiency and Power Losses . . . 24
3.2.2 Control and Modulation . . . 24
3.3 The High-Frequency Transformer Network . . . 25
3.3.1 Isolation Transformer Representation . . . 26
3.3.2 HF Transformer Designs . . . 27
3.3.3 Magnetic Behavior and Effects . . . 29
3.3.4 Power Losses and Heating Effects . . . 37
3.3.5 Ferrite Core Losses . . . 37
3.3.6 Copper Winding Losses . . . 39
3.3.7 Thermal Considerations . . . 40
3.3.8 HF Transformer Construction . . . 41
3.4 Power Switching Devices . . . 45
3.4.1 Real Switches . . . 46
3.4.2 Diodes . . . 47
3.4.3 Metal-Oxide-Semiconductor Field Effect Transistors . . . 49
3.4.4 Semiconductor Materials and Manufacturers . . . 53

III Method 55

4 Full-Bridge Converter Configurations for Interfacing PV to MMC 57
4.1 Introduction . . . 57
4.2 Single DC-DC Converter Configuration . . . 58
4.2.1 Power Switches . . . 58
4.2.2 The HR Transformer . . . 58
4.2.3 Efficiency and Total losses . . . 59
4.3 Series-Configuration of the High Frequency Isolated Full Bridge DC-DC Converter . . . 59
4.3.1 Power switches . . . 60
4.3.2 The HF Transformer . . . 60
4.3.3 Efficiency and Total losses . . . 60
4.3.4 Optimal choice of $\mathbf{k_s}$ series connected DC-DC converters . . . 61
4.4 Parallel-Configuration of the High Frequency Isolated Full Bridge DC-DC Converter . . . 62
4.4.1 Power switches and the HF Transformer . . . 62
4.4.2 Efficiency . . . 63
4.4.3 Optimal choice of $\mathbf{k_p}$ parallel-connected DC-DC converters . . . 63

4.5 Comparison 63
4.6 Configurations chosen for a further analysis 63

5 PV Plant Configuration **65**
5.1 Introduction 65
5.2 The PV Module 65
5.3 PV Array Design for the different converter topologies 66

IV Results, Discussion and Conclusion 71

6 Annual Energy Yield and Efficiency Comparison **73**
6.1 Description of the Evaluation Models 73
    6.1.1 PV Array Performance Model 74
    6.1.2 Central Inverter and Multi-String Inverter Configurations 75
    6.1.3 MMC Performance Model 75
6.2 Isolated DC-DC Converter Performance Models 76
    6.2.1 PV Array 76
    6.2.2 MMC Model 77
    6.2.3 Switching Devices Performance Models 78
    6.2.4 HF Transformer Performance model 80
    6.2.5 Single DC-DC Converter Configuration 82
    6.2.6 Parallel-Connected SiC-Based DC-DC Converter Configuration . 82
    6.2.7 Series-Connected GaN-Based DC-DC Converter Configuration . 83
6.3 Annual Energy Yield and Efficiency Comparison 84

7 Economic Benefits **87**
7.1 Levelized Cost of Energy 87
7.2 Lifetime Cost 88
    7.2.1 PV Plant Fixed Cost 88
    7.2.2 Converter and Transformer Cost 89
    7.2.3 Total Lifetime Cost 91
7.3 Extracted energy, Total Cost and LCOE 92

8 Conclusion and Further Work **95**
8.1 Conclusion 95
8.2 Further Work 97

Bibliography **99**

Appendix **105**
A Power Switching Devices 105
    A.1 SiC MOSFETs 105
    A.2 GaN HEMTs 116
    A.3 SiC Schotty Diodes 131
B Skin depth of copper wires 138

List of Tables

1.1 PV Plant Technical Data [1]. 8

2.1 Comparison of the MMC configurations [2] 15
2.2 Operation of the chopper cell SM. 17
2.3 MMC Technical Data. 19

4.1 Comparison of the different DC-DC converter configurations. 64

5.1 PV module Titan S6-60 series electrical characteristics [3]. 66
5.2 Required PV array ratings for the different DC-DC converter configurations. 67
5.3 PV array configuration for the different MMC DC-DC converter configurations 68
5.4 Power, voltage, and current for the different PV array configurations at peak power. 68

6.1 Coefficients of the polynomial in equation 6.1 for P_{mp} and V_{mp} respectively [2]. 74
6.2 Coefficients of the core and copper loss equations given in equation 6.4 [4]. 75
6.3 Parameters for Transformer Design. 81
6.4 Annual energy obtained from the different PV onfigurations. 86

7.1 Extracted energy over a lifetime for all the configurations. 88
7.2 Fixed cost for all the PV plant configurations [1, 5]. 88
7.3 Converter and transformer costs for the different PV plant configurations [6, 2]. 89
7.4 Cost per inverter [6]. 89
7.5 Cost per DC-DC converter for the MSCI configuration [2]. 90
7.6 Cost per SM for the MMC PV configuration [2]. 90
7.7 Cost for single-unit full-bridge DC-DC converter. 91
7.8 Cost for two SiC based full-bridge DC-DC converters in parallel. 91
7.9 Cost for two GaN-based full-bridge DC-DC converters in series. 92
7.10 92

7.11 Extracted energy, total cost, and LCOE for all the configurations in per unit. 92

A1 Comparison of different manufacturers SiC MOSFETs at 25 °C. 105
A2 Comparison of different manufacturers GaN Enchancement Mode HEMTs at 25 °C. 116
A3 Comparison of different manufacturers SiC Schottky diodes at 25 °C. . . 131
A4 Skin depth of copper wire at different frequencies. 138

List of Figures

1.1 Levelized cost of electricity (LCOE) for PV technology [7] 4
1.2 The principle of MPPT with DC-DC converter. 6
1.3 (a) Centralized arrangement, (b) decentralized multi-string arrangement, (c) decentralized string arrangement, and (d) module distributed arrangement. 6

2.1 Modular Multilevel Converter Configurations (a) Single-Star Bridge Cell (SSBC), (b) Single-Delta Bridge Cell (SDBC), (c) Double-Star Chopper Cell (DSCC) or Double-Star Bridge Cell (DSBC), depending on the submodule configuration [2]. 14
2.2 Submodule configuration (a) Chopper Cell (half-bridge), (b) Bridge Cell (full-bridge). 15
2.3 Three-phase MMC circuit topology. 16
2.4 (a) State 1, (b) State 2, (c) State 3, (d) AC terminal voltage v_{ac} 18
2.5 MMC with PV multi-string connected to an isolated DC-DC converter. . 19

3.1 The required components for an isolated DC-DC converter. 21
3.2 Unidirectional full-bridge DC-DC converter. 22
3.3 Bidirectional full-bridge DC-DC converter. 23
3.4 DC-AC converter, (a) voltage-fed, (b) current-fed. 23
3.5 Pulse-width modulation with (a) bipolar switching, and (b) unipolar switching. 25
3.6 25
3.7 Transformer representation, (a) two-winding transformer, (b) equivalent circuit. 27
3.8 Transformer cores, (a) double-E core, (b) double-U core, (c) toroidal core. 28
3.9 Round wires fitting, (a) square fitting, and (b) hexagonal fitting. 28
3.10 Simple transformer 30
3.11 (a) Magnetic domains orientated randomly, (b) Magnetic domains lined up in the presence of an external magnetic field. 32

3.12 Transformer magnetization, (a) The applied current $i(t)$, (b) The resulting hysteresis loop [8]. 33
3.13 Eddy currents in the magnetic transformer core. 34
3.14 Approximation of the fringing effect from [9], (a) the fringing flux, (b) the effective cross-sectional area of the air gap, and (c) the equivalent representation of the air gap. 35
3.15 Mutual and leakage fluxes in the transformer core. 36
3.16 Eddy currents generated by the proximity effect in the magnetic transformer core [9]. 37
3.17 A simple toroidal transformer. 42
3.18 Toroidal core dimensions. 43
3.19 Ideal switch, (a) off-state, (b) on-state. 45
3.20 Diode (a) circuit symbol, (b) i-v characteristics, (c) idealized switching. . 47
3.21 Diode reverse-recovery time t_{rr}. 48
3.22 N-channel MOSFET (a) circuit symbol with body diode, (b) i-v characteristics, (c) idealized switching. 49
3.23 Switching characteristics of MOSFET, (a) turn-on, (b) turn-off [9]. 51
3.24 MOSFET circuit equivalent, (a) in the ohmic region, (b) in the cut-off and active region. 51
3.25 Comparison of Si, SiC, and GaN material properties [10]. 53

4.1 Single DC-DC converter configuration. 58
4.2 Topology of the proposed series-connection of isolated full bridge DC-DC converters. 59
4.3 Iterative selection of the number of series connected DC-DC converters. . 61
4.4 Topology of the proposed parallel connection of isolated full bridge DC-DC converters. 62

5.1 I-V curve, available power and maximum power point for the Titan S6-60 series PV module at different irradiance levels at 25 °C. 66
5.2 I-V curve and the available power at different irradiance levels at 25 °C for the PV array design for (a) the single-unit DC-DC converter configuration, (b) the series-connected DC-DC converter configuration, and (c) the parallel-connected DC-DC converter configuration. 69

6.1 Block representation of performance model with temperature estimation of PV cells [2]. 74
6.2 Simple control structure of DC-DC converter. 76
6.3 MMC SM voltage with 10%ripple from simulations. 77
6.4 Conduction losses provided by the manufacturer. 79
6.5 SiC MOSFET from Cree Wolfspeed (C2M0025120D), (a) turn-on losses, (b) turn-off losses, and (c) conduction losses. 79
6.6 Switching losses for the GaN HEMT GS66504B from GaN Systems [11]. 80
6.7 GaN HEMT GS66504B from GaN Systems, (a) turn-on losses, (b) turn-off losses, and (c) conduction losses. 81

6.8 Efficiency of the single-unit DC-DC converter configuration at different DC link voltage at (a) 1 kHz switching, and (b) 20 kHz switching. 82
6.9 Efficiency curves for the single-unit DC-DC converter configuration at 1 kHz, 10 kHz, and 20 kHz switching frequency. 83
6.10 Efficiency of the parallel-connected DC-DC converter configuration at different DC link voltage and (a) 1 kHz switching, and (b) 10 kHz switching. . . . 83
6.11 Estimated efficiency of the two series-connected GaN-based DC-DC converter configuration at different DC link voltage and (a) 20 kHz switching, (b) 200 kHz switching, and (c) 500 kHz switching. 85

Nomenclature

Abbreviations

BESS	Battery energy storage systems
CI	Central inverter
DBR	Diode Bridge Rectifier
GaN	Gallium-Nitride
HEMT	High Electron Mobility Transistor
HF	High-frequency
IGBT	Insulated-Gate Bipolar Transistor
LCOE	Levelized Cost of Electricity
MLT	Mean length turn
MMC	Modular Multilevel Converter
MMF	Magnetomotive Force
MOSFETs	Metal-oxide-semiconductor field effect transistors
MPP	Maximum Power Point
MPPT	Maximum Power Point Tracking
MSCI	Multi-string inverter
MV	Medium voltage
PV	Photovoltaics
RES	Renewable Energy Sources
RMS	Root Mean Square
Si	Silicon
SiC	Silicon-carbide
SM	Submodule
STC	Standard Test Conditions
WBG	Wide-bandgap

Constants

$k = 1.3806485210^{-23}$	Boltzman constant	$[m^2kgs^{-2}K^{-1}]$
$\sigma = 5.67 * 10^{-8}$	Stefan-Boltzmann constant	$[W/m^2 * K^4]$
$\mu_0 = 4\pi 10^{-7}$	Permeability of free space	$[H/m]$
$\mu_{cu} = 1.257 * 10^{-6}$	Permeability of copper	$[H/m]$
$\pi = 3.14159$	Pi	
$\rho_{cu} = 1.72 * 10^{-8}$	Resistivity of copper	$[\Omega m]$
q	electron charge	

Variables

A_c	Cross-sectional area of core	$[m^2]$
A_s	Surface area	$[m^2]$
A_w	Window area	$[m^2]$
A	Transformer core coefficient	–
a_{ch}	Largest diameter of a toroidal core	$[m]$
a_{cu}	Cross-sectional copper wire area	$[mm^2]$
B	Flux density	$[T]$
D	Duty ratio	–
d	Wire diameter	$[m]$
$\mathbf{E}$	Electrical field	$[V/m]$
f_{sw}	Switching frequency	$[Hz]$
G	irradiance	$[W/m^2]$
H	Magnetic field intensity	$[A/m]$
h	Height	$[m]$
h_{conv}	Convection heat transfer coefficient	$[W/m^2 * {}^\circ\mathrm{C}]$
I_p	Primary side current	$[A]$
I_s	Secondary side current	$[A]$
J_{cu}	Copper current density	$[A/mm^2]$
k_t	Thermal conductivity	$[W/m{}^\circ\mathrm{C}]$
k_e	Dimensionless loss coefficient	–
k_s	Series connected DC-DC converters	–
k_p	Parallel connected DC-DC converters	–
l_{cu}	Copper conductor length	$[m]$
N	Number of submodules	
N_s	Number of winding on secondary side, or Series connections of PV modules	
N_p	Number of windings on primary side, or Parallel connections of PV arrays	
P_c	Conductive heat transfer	$[W]$
P_{cond}	Conduction loss	$[W]$
P_{conv}	Convective heat transfer	$[W]$
P_{cu}	Copper losses	$[W]$
P_{fe}	Core losses	$[W]$
$P_{fe,h}$	Hysteresis loss in the core	$[W]$
P_{rad}	Radiative heat transfer	$[W]$
P_{sw}	Switching loss	$[W]$
P_{tr}	Transformer loss	$[W]$
T	Temperature	$[K]$
T_a	Ambient temperature	$[K]$
T_s	Surface temperature	$[K]$
t_{rr}	Reverse recovery time	$[s]$
t_r	Forward recovery time	$[s]$
R	Resistance	$[\Omega]$
R_s	series power losses	$[\Omega]$
R_p	parallel power losses	$[\Omega]$

Variables, cont.

a	diode quality factor	
μ_r	Relative permeability of magnetic material	
μ	Magnetic permeability	
V_s	String voltage	$[V]$
V_{sm}	Submodule voltage	$[V]$
l	Length	$[m]$
l_{cu}	Average length of winding turn	$[m]$
α_{cu}	Copper fill factor	
ϵ	Electric field intensity	$[V/m]$
ϵ	Permittivity	
ϵ_s	Emissivity of surface	
$[\Omega^{-1}m^{-1}]$		
ρ_{fe}	Resistivity of core	$[\Omega m]$
σ	Conductivity	

Part I

Introduction

Chapter 1

Background

This chapter presents as a basic introduction to the topic of this master thesis.

1.1 Grid-connected Photovoltaic Applications

As a result of the continuously increasing carbon emissions, the global demand for cleaner energy is rising. Grid-connected photovoltaic (PV) systems is an attractive solution to provide green energy. However, variable power production due to unpredictable weather conditions pose a challenge for optimal planning, grid operation, and grid stability.

1.1.1 Trends

In the 2015 Paris Agreement, one hundred and ninety-four nations agreed to long-term actions to reduce carbon emissions and limit the increase in the global average temperature to well below 2 °C. It is the first legally-binding climate agreement ever [12].

The use of renewable energy has experienced a rapid growth in the last few years. According to the most recent U.N. environmental-backed report [7], a record 98 GW of new power capacity from solar power was installed globally in 2017. Solar energy dominated global investing in the new power generation with more added capacity than coal, gas, and nuclear plans combined. China alone contributed with more than half (53 GW) of the installed solar power capacity, leading the way from fossil fuel to a climate neutral power generation. The total capacity added from renewable energy sources (RES) was 157 GW in 2017. By comparison, the installed power capacity from fossil fuel was 70 GW over the same period. However, fossil fuels still dominate the existing power capacity counting for 87.9 per cent of the market.

According to U.N. Environment, the Frankfurt School - UNEP Collaborating Centre, and Bloomberg New Energy Finance, the increased investment in solar power is driven by the decreasing cost of production. In 2017, the cost of large-scale PV technology fell by

15 per cent to \$86 per MWh. Despite the lower capital cost, the global investment rose by 18 per cent to \$160.8 billion, where China alone counted for 45 per cent. The total investment in renewables increased by two per cent globally, with sharp increase in the amount of money deployed in new markets such as Mexico, the United Arab Emirates, and Egypt. However, in some major and mature markets such as the United States, United Kingdom, Germany, and Japan, a decrease in investments occurred due to changes in international governments.

Over the years, manufacturers have demonstrated huge improvements in PV panels efficiency, resulting in an increased annual yield for PV systems. Figure 1.1 shows that the levelized cost of electricity (LCOE) has decreased significantly over the years for PV technology [7]. This has boosted the competitiveness of solar technology against established technologies such as coal and gas.

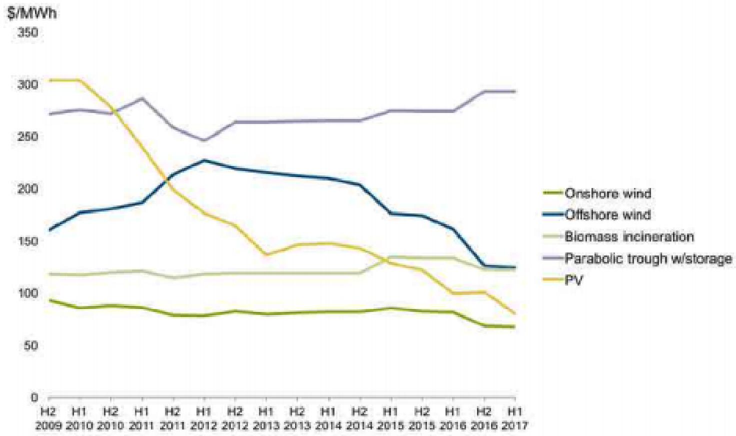


Figure 1.1: Levelized cost of electricity (LCOE) for PV technology [7]

1.1.2 PV Penetration Challenges and Issues

The shift from the predominant use of fossil fuels for power generation to using a significant share of RES is changing the power grid. The stability of the power system relies on the balance between generation and consumption of energy. The movement of the sun is now well understood and solar energy can therefore be predicted with great accuracy. However, due to the variability caused by moving clouds, solar power production is subjected to second-to-second changes [13]. Today's power system cannot handle the intermittent nature of solar power production. A detailed discussion of the control of the power system, however, is beyond the scope of this thesis.

A fixed voltage and frequency in the power system isnecessary. When the power is generated by synchronous generators, the active and reactive power flow is controlled by the power angle and voltage relationships, which again is directly controlled by the governor and field current [14]. Active power flows from a higher power angle to a lower power angle, as well as the reactive power, is controlled by the system voltage. The bus voltages are normally fixed, but the induced voltage in the generators can be varied. This enables control of the reactive power. This control is essential for maintaining the stability and power quality in the power system today.

Solar power is a non-dispatchable energy resource, due to the inability to dispatch power when demanded and the lack of capability to provide active and reactive power controls. A significant share of PV systems can therefore affect volt/var control, power quality, and system operation. Issues related to high PV penetration appear in both the steady-state and in the dynamic time frame, and can be local or system-wide. The severity of these issues is determined by the penetration level of PV systems. The most pertinent of these issues are [13]:

- Voltage rise and unbalance in feeder.
- Feeder, equipment and component overloading.
- Malfunction of voltage regulation equipment, such as on load tap changer, line voltage regulators and capacitor banks.
- Fluctuations in reactive power flow due to operation of capacitor banks.
- Power quality issues and voltage fluctuations.
- Over-current and over-voltage, and misoperation of protection devices.
- Reverse power flow.
- Variation in power factor in feeder.
- Issues with reliable and secure operation of the power system.

The key problem, especially with a high PV penetration level, is the variation of the produced power in the PV plant due to variable weather conditions. This can impact the power quality in the grid negatively. Power electronics play a vital role in the interface of PV to the grid, especially when considering the operation of the power system with high PV penetration levels [15].

1.1.3 PV Inverter Topologies

When connecting PV to the AC power grid, DC to AC power conversion is clearly required. PV systems generally suffer from poor conversion efficiency due to the variable power production. Inverter arrangements with Maximum Power Point Tracking (MPPT) algorithms are therefore essential to ensure that maximum power is extracted from the PV plant at all times [16]. Several MPPT techniques have been presented in the literature [17, 18, 19, 20], and the principle is depicted in figure 1.2.

The existing central inverter arrangement, shown in figure 1.3 (a), is based on two- or three-level inverters with one MPPT [2]. The PV strings are connected in parallel and the generated power is fed into the grid through one central inverter. During partial shading and unequal distribution of irradiance in the PV plant, this inverter topology is not capable of harvesting available power from the PV panels, resulting in lower energy yield. In

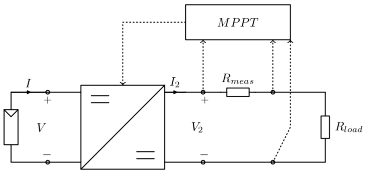


Figure 1.2: The principle of MPPT with DC-DC converter.

the decentralized multi-string inverter arrangement, depicted in figure 1.3 (b), a parallel connection of a few PV strings are connected to one string inverter. This increases the Maximum Power Point (MPP) control, but MPPT is only obtainable after it is clear that the strings have the same structure and will not be shaded.

The decentralized string arrangement, depicted in 1.3 (c), has only one PV string connected to each DC-DC converter, which provides MPP control on each PV string. In the module distributed arrangement, shown in 1.3 (d), one DC-DC converter is connected to each PV module providing individual module MPP control. However, both the decentralized string arrangement and the module distributed arrangement require a large number of DC-DC converters, resulting in a high cost, reduced efficiency, and a decreased annual yield [2]. They are therefore not suitable for utility scale PV plants. The central inverter arrangement and the decentralized multi-string inverter arrangement result in a lower number of converters, and are therefore cheaper solutions compared to (c) and (d), but the energy yield is susceptible to panel mismatch and partial shading [2]. A step-up transformer facilitates the connection from the low voltage grid to the high voltage grid and isolates the PV arrangement from the MV utility grid. This is a high-volume, high-cost solution yielding increased power losses.

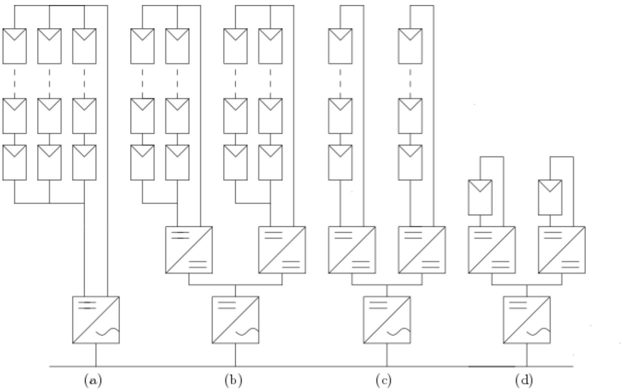


Figure 1.3: (a) Centralized arrangement, (b) decentralized multi-string arrangement, (c) decentralized string arrangement, and (d) module distributed arrangement.

1.2 Motivation and Objectives

Efficient power converters are an enabling technology for integration of renewables, and the total system efficiency is strongly dependent on the converter efficiency. The existing central inverter topology for PV plants is based on two- or three-level inverters with one MPPT, resulting in lower energy yield due to lost power production in times with partial shading and unequal distribution of irradiance. The efficiency of the inverter is strongly load dependent, which is critical for PV inverters as the power generation changes throughout the day.

Recently, new topologies as the Cascaded H-Bridge (CHB) and Modular Multilevel Converter (MMC) have been proposed as an alternative solution to the two- or three-level inverters [21, 22, 23, 24, 25]. The MMC has the last couple of years emerged as an attractive solution for grid connected PV applications due to higher reliability, inherent modularity and scalability [2].

The MMC is built up of a number of series connected converters referred to as submodules (SMs), which can be independently controlled. Redundancy is often added by installing extra SMs, which increases the reliability, makes maintenance easier, and ensures normal operation in case of failure in one SM [26]. It is also a cost effective converter due to the economies of scale [27]. The MMC can simply be scaled for direct connection to Medium Voltage (MV) grid by adding more SMs, thereby avoiding the need for a step-up transformer [28]. Isolation must be provided for safety of the operator, as per IEEE Std 1547 for Interconnecting Distributed Resources with Electric Power Systems [29]. However, it does not need to be at the point of common coupling to the grid. Because of the MMC modularity, a realization of a decentralized PV plant with high MPPT granularity is possible.

The isolation in a MMC PV plant can be provided by using isolated DC-DC converters. In this master thesis, cascaded full-bridge solutions will be investigated as topologies to interface PV to MMC. Since the PV inverter operates at rated conditions only for a few hours a day, it is important that the isolated DC-DC converter has a high efficiency from no-load to full-load.

By utilizing series- or parallel- connections of full-bridge converters, the bulk power transmission to the SM is distributed. This increases the overall reliability of the system. Such cascaded topologies also changes the ratings of the switching devices in the DC-DC converter.

SiC- and GaN-based power conversion devices have the last years been introduced to the market as a promising topologies. Utilizing these devices can improves the switching characteristics due to superior material properties giving a high efficiency power conversion.

The objective of this thesis is to analyze different high-frequency full-bridge DC-DC converter configurations for the MMC PV plant and compare them in terms of efficiency, energy yield, and levelized cost of energy (LCOE). Two classical PV plant arrangements, the central inverter (CI) configuration and the multi-string central inverter (MSCI) configuration, are also considered for performance comparison to the different MMC PV plant configurations.

The design of the converter in terms of inductive paramenters such as the HF transformer, filter network, inductors, and capacitors is beyond the scope of this thesis and therefore not addressed in detail. Simulation models are made in order to look at the efficiency and the energy yield of different PV inverter topologies.

1.3 Problem Description

A 3 MW grid-connected solar PV plant at Kolar, Karnataka, India is considered for the study of this master thesis. The technical data for this PV plant is provided in [1] and shown here in table 1.1. The PV modules in this plant are Titan S6-60 series, mono-crystalline PV modules from Titan Energy Systems Ltd.

This PV plant has four central inverter outputs connected together as the input to a 1.25 MVA step-up transformer. Three of these step-up transformers are used to connect similar units to the medium voltage (MV) grid.

Table 1.1: PV Plant Technical Data [1].

Parameter	*Symbol*	*Values*
Medium voltage (nominal)	$V_{g,MV}$	11 kV
Low voltage (nominal)	$V_{g,MV}$	230 V
Apparent power (nominal)	S_N	3 MVA
Grid frequency	f_g	50 Hz
Central inverter capacity (nominal)	S_{CI}	250 kVA
No. of central inverters	N_{CI}	12
Medium voltage transformer apparent power	S_T	1.25 MVA
PV panel maximum power	P_{mp}	235 Wp

This PV plant is compared with MMC PV plant configurations. The MMC PV plant has the same ratings as the one presented above. The high scalability of the MMC facilitates a direct connection to MV grid without the use of a step up transformer. The required voltage level is achieved by designing the MMC with the correct number of SMs in order to directly connect the MMC to MV grid [28]. The isolation in such a configuration can be provided between the PV strings and the SM of the MMC by utilizing DC-DC converters.

1.4 Implementation Tools

Simulations with DC-DC converters utilizing different switching topologies have been performed in PLECS®simulation software in order to capture switching and conduction losses in the switching devices. The thermal models for the different switching devices are provided by the manufacturer, or the models are made by utilizing the data provided in the datasheets from manufacturers.

When considering the PV plant as a whole, the results from the PLECS simulations of the DC-DC configurations have been implemented in Simulink®to obtain the annual energy extracted and the LCOE.

1.5 Thesis Outline

This thesis is divided into four parts:

- Part I: Introduction
- Part II: Theory
- Part III: Method
- Part IV: Results, discussion and conclusion

Part I is a general introduction of the master thesis. Chapter 1 is about implementation of RES into the power grid. It looks at the increasing trends in investing in PV technology, and briefly looks at the challenges associated with the increased share of PV in the power grid. The different PV inverter topologies are presented, and this outlines the background for this master thesis, which is presented at the end of chapter 1.

Part II provides a literature study of relevant topics. Chapter 2 presents the Modular Multilevel Converter (MMC) as an attractive solution to the conventional inverters in PV plants due to several advantages, while chapter 3 looks at isolated DC-DC converters. It introduces the isolated full-bridge converter and addresses magnetic effects in HF transformer. At the end of chapter 3, different power switching devices are presented and an introduction of SiC and GaN switching technology is given.

Part III presents the method of the simulations performed. Chapter 4 presents the three different isolated full-bridge converter configurations considered to interface PV to MMC in the MMC PV plant. Chapter 5 describes the modelling of PV arrays used in the simulations for each isolated DC-DC converter topology.

Part IV concerns the evaluation models used in order to find the annual energy yield and LCOE, and presents the results from simulations. Chapter 6 addressed the anual energy yield and the efficiency of the different isolated DC-DC converter configurations, while chapter 7 calculates the LCOE and states the benefits of chosing a MMC PV plant. Chapter 8 gives the conclusion and rounds up this thesis by presenting some ideas for further work.

Part II

Theory

Chapter 2

Medium Voltage Grid-Connected MMC for PV Applications

The MMC has the last couple of years emerged as an attractive solution for grid connected PV applications due to higher reliability, inherent modularity and scalability [2]. An introduction of the fundamental operation and dynamics of the Modular Multilevel Converter (MMC) is presented in this chapter.

2.1 Modular Multilevel Coverter

The Modular Multilevel Converter (MMC), also known as M2C, was first introduced in [30]. Based on a cascaded multilevel topology with series connections of submodules (SMs) instead of semi conductors, the MMC power rating can be scaled with the number of SMs and easily achieve high power ratings compared to other multilevel topologies. By installing more submodules, redundancy can be implemented [27], providing high reliability. With high scalability the MMC offers superior harmonic performance in the conversion from DC to AC voltage.

2.1.1 Configurations

The MMC branches can be configured for any number of phases and for DC-AC, AC-AC or DC-DC. [31] has presented the different three phase DC-AC circuit configurations in the MMC family: the Single-Star Bridge Cell (SSBC); the Single-Delta Bridge Cell (SDBC); the Double-Star Chopper Cell (DSCC); and the Double-Star Bridge Cell (DSBC), here presented in figure 2.1.

Each phase arm is obtained by a series connection of power converters referred to as submodules (SM) and one arm inductor. Each SM is made up of a half-bridge (HB) (chopper cell) or a full-bridge (FB) (bridge cell) configuration, both with a floating capacitor.

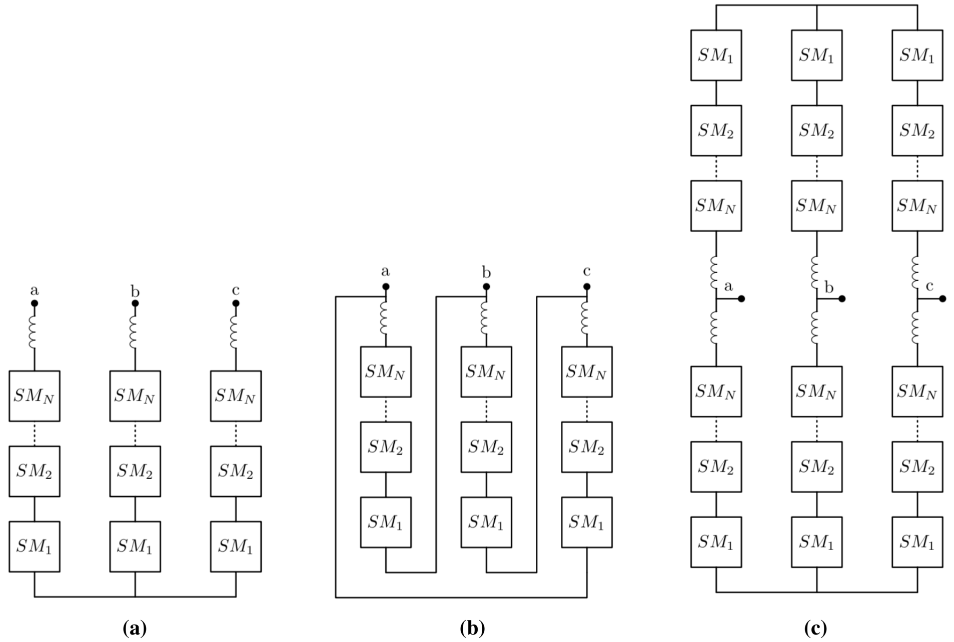


Figure 2.1: Modular Multilevel Converter Configurations (a) Single-Star Bridge Cell (SSBC), (b) Single-Delta Bridge Cell (SDBC), (c) Double-Star Chopper Cell (DSCC) or Double-Star Bridge Cell (DSBC), depending on the submodule configuration [2].

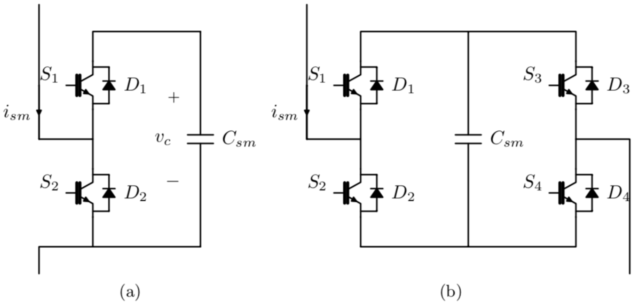


Figure 2.2: Submodule configuration (a) Chopper Cell (half-bridge), (b) Bridge Cell (full-bridge).

Table 2.1: Comparison of the MMC configurations [2]

MMC Configuration	*Submodules*	*Switches*	*MPPT Modularity*
SSBC	$3N$	$12N$	$3N$
SDBC	$3N$	$12N$	$3N$
DSBC	$6N$	$24N$	$6N$
DSCC	$6N$	$12N$	$6N$

Figure 2.2 depicts the two different SM topologies. The DSCC is realized using the HB configuration, while the DSBC uses a FB configuration.

Figure 2.2 shows that the bridge cell topology requires two extra switches compared to the chopper cell topology for the same power rating. However, the SM capacitor requirement is doubled [2]. In table 2.1 the different configurations are compared in terms of number of SMs and switches assuming N SMs per phase arm. Since each SM consists of one SM capacitor, the number of SMs equals the number of capacitors. In the SSBC and the SDBC configuration, the number of SMs is half of the DSBC and the DSCC. However, since the DSCC is realized using the chopper cell configuration, the number of switches is the same. The DSBC requires twice as many switches as the other configurations, resulting in higher switching losses and lower energy yield. For the same power rating, the MPPT modularity is twice as high in DSBC and DSCC compared to SSBC and SDBC since is has twice as many SMs.

The MMC configurations presented in figure 2.1 presents different variants of the MMC applicable in the connection of PV to the utility grid. The DSCC-MMC, referred to as MMC hereafter, is chosen for this study due to the lowest number of switching devices for the same power rating. It also has twice as high MPPT granularity compared to the other topologies for the same number of switches [2]. It requires twice as many SM capacitors as the SSBC and SDBC, but according to [2], this is not a disadvantage when considering energy savings per year. The chopper cell is consequentially the most discussed topology in the literature and is often referred to as the standard SM topology [32].

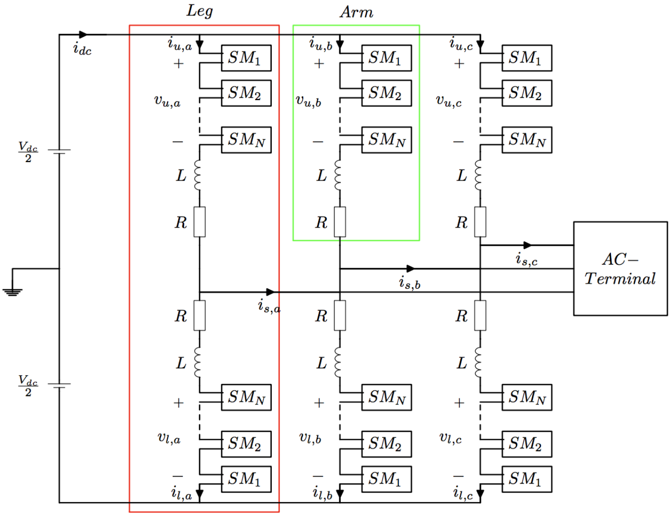


Figure 2.3: Three-phase MMC circuit topology.

2.1.2 Circuit Topology

The three-phase MMC is depicted in figure 2.3 and consists of three phase legs connected in parallel. The series resistor R represents the switching losses in the SMs and the ohmic losses in the inductor. The two terminals over the phase legs make up the DC terminal of the converter, while the midpoint connections between the upper and lower arms form the three-phase AC terminal. A balanced three-phase system is made by phase shifting the AC reference of each leg with 120°.

The series connected arm inductors limit the circulating arm current that arise from voltage differences in the upper and lower legs by limiting the rate of change of current during switching [33]. Without these inductors, potentially high transient currents could occur between the phase legs and subsequently damage the equipment. They also limit the AC fault current when a short circuit occurs on the DC side. However, these inductors do not need to be large since the arm voltage can be controlled with high precision [32].

2.1.3 Operation

The SMs are identical modules and provides the modular characteristics of the MMC. The floating capacitor functions as an energy storage device, which maintains a direct voltage. It can either be inserted or bypassed in the MMC circuit. By defining a SM insertion index n, which takes on the value 1 if the SM capacitor is inserted and 0 if the SM capacitor is bypassed, the SM terminal voltage can be defined as:

$$v_{sm} = n * v_c \tag{2.1}$$

Table 2.2 summarize the different states of operation of the chopper cell SM.

Table 2.2: Operation of the chopper cell SM.

State	**S1**	**S2**	v_{sm}	i_{sm}	**Capacitor**
Inserted	ON	OFF	v_c	> 0 < 0	Charging via D1 Discharging via S1
Bypassed	OFF	ON	0	> 0 < 0	Bypassed via S2 Bypassed via D2
Blocked	OFF	OFF	v_c 0 -	$i_{sm} > 0$ and $v_{sm} \geq v_c$ $i_{sm} < 0$ and $v_{sm} \leq 0$ Else	Charging via D1 Bypassed via D2 None and $i_{sm} = 0$

This means that the voltage across each SM can be controlled separately, and each SM can therefore be considered as a controllable, unipolar voltage source. The highest voltage across the SM terminals equals the capacitor voltage, and the switches and the diodes must be able to block this voltage for the SMs to function properly [32].

The required voltage level of the converter is achieved by designing the MMC with the correct number of SMs. A series connection of SMs, called SM strings, can produce an output voltage with values between zero and $N * v_c$, which gives a total of $(N + 1)$ or $(2N + 1)$ voltage levels, depending on the modulation method [34]. The number of voltage levels can therefore be easily increased by adding more SMs in each arm, thus permitting the MMC to take on any number of levels in the voltage. The upper and lower arm voltages can be expressed as:

$$v_{u,l} = \sum_{i=1}^{N} n_{u,l}^{i} v_{cu,l}^{i} \tag{2.2}$$

Utilizing KVL in figure 2.3, it is seen that the sum of the SM voltages in one phase leg equals the DC terminal voltage. Therefore, to obtain a constant DC terminal voltage, the number of inserted SMs in one leg is constant. However, the AC voltage will change accordingly to the relationship between the number of inserted SMs in the upper and lower leg:

$$v_{ac} = -v_{upper} + v_{lower} \tag{2.3}$$

Figure 2.4 shows how one phase leg with 2 SMs in each phase arm can be operated to achieve different output voltage levels while the DC terminal voltage stays constant. This is the same for a three-phase system, where operation of the converter is based on controlling the SMs in the six phase arms in order to achieve the desired AC output voltage. As a result, the converter can behave as a controllable voltage source with great precision, both with respect to the AC and DC sides.

Half of the SMs in one leg will be on and the other half will be off at all times - thus the number N represents the number of inserted SMs at every moment. The SM capacitors are therefore all being charged to the MMC DC link voltage divided by the number of SMs:

$$v_c = \frac{V_{dc}}{N} \tag{2.4}$$

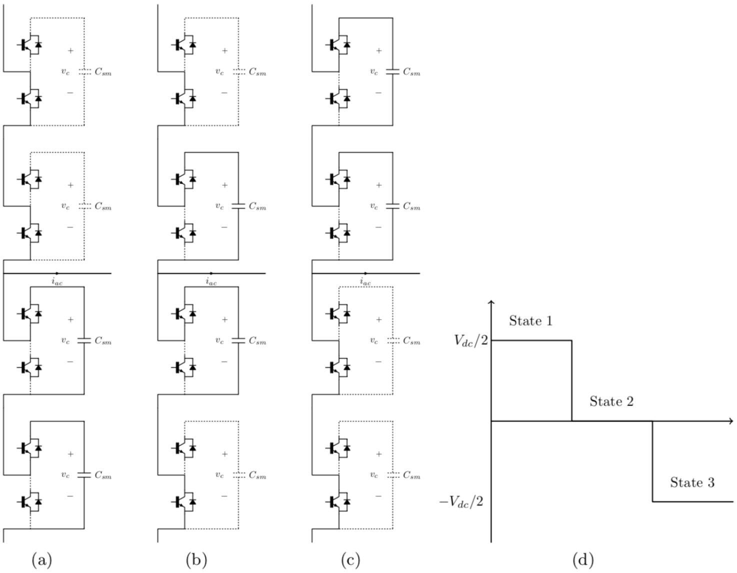


Figure 2.4: (a) State 1, (b) State 2, (c) State 3, (d) AC terminal voltage v_{ac}

A standard MMC is also typically built with redundant SMs in each phase arm, in order to increase reliability and ensure standard operation in case of a failure in one SM [26].

2.2 PV MMC Plant Description

The high scalability of the MMC facilitates a direct connection of the PV system to medium voltage (MV) grid without the use of a step up transformer. However, as per IEEE Std 1547 guidelines [35], isolation must be provided for safety of the operator, but it does not need be at the point of common coupling (PCC) to grid. By connecting one PV string or PV array to the MMC SM through an isolated DC-DC converter, as depicted in figure 2.5, the required isolation is provided and a realization of a decentralized PV MMC plant connected directly to MV grid without the use of a step-up transformer is possible. This solution also provides high MPPT granularity.

The overall efficiency for the inverter arrangement is the product of the MMC efficiency and the isolated DC-DC converter efficiency:

$$\eta_{inv} = \eta_{mmc}\eta_{dc-dc} \tag{2.5}$$

The required voltage level is achieved by designing the MMC with the correct number of SMs in order to directly connect the MMC to MV grid [28]. The three-phase MMC consists of six phase arms, resulting in a total number of SMs equal to:

$$SMs = N * 6 \tag{2.6}$$

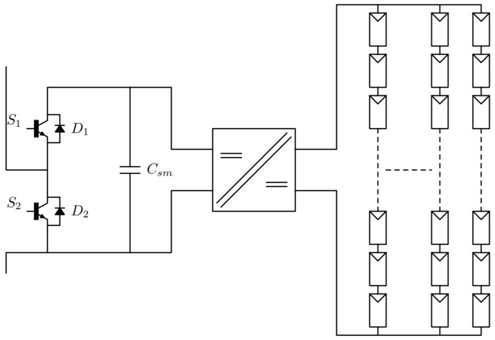


Figure 2.5: MMC with PV multi-string connected to an isolated DC-DC converter.

where N is the number of MMC SMs in each phase arm. The rated power of the MMC is then given by:

$$P_t = N * P_{sm} \tag{2.7}$$

where P_{sm} is the rated power of each SM. The total power produced from the MMC PV plant is obtained from:

$$P_{pv} = NP_{sm} \tag{2.8}$$

where N is the number of MMC SMs, and P_{sm} is the power at each SM.

The PV plant chosen for this study is a 3 MW scale grid-connected PV plant. With 6 phase arms in the three-phase MMC, each phase arm must be rated for 0.5 MW. For a rating on 100 kW for each MMC SM, this configuration requires 5 SMs in each phase arm to obtain the power ratings. Table 2.3 presents the parameters of the MMC used for the PV plant described in table 1.1.

Table 2.3: MMC Technical Data.

Parameter	*Symbol*	*Values*
Rated apparent power	S_R	3 MVA
Grid frequency	f_g	50 Hz
DC-link voltage	V_{dc}	5 kV
Number of submodules	N	5
SM voltage	V_{SM}	1000 V
Maximum SM voltage	$V_{SM,max}$	1100 V
SM rated power	P_{SM}	100 kW

Chapter 3

Isolated DC-DC Converters

This chapter is an introduction to DC-DC converters with electrical isolation to interface PV to MMC. As mentioned in earlier chapters, isolation can be provided in the PV MMC system using a transformer. However, line-frequency transformers are large and bulky, and utilization of high-frequency (HF) transformers with lower weight and lower volume have therefore become popular. Isolated DC-DC converters utilize the HF transformer in the DC to DC conversion stage, providing isolation and safety in the system.

3.1 Introduction

The required components for DC-DC converters with galvanic isolation is seen in figure 3.1. The electrical isolation is provided by a high-frequency (HF) isolation transformer. The filter networks, consisting of capacitors, and inductors, provide smooth terminal voltages and currents. The DC-AC converter consists of a controllable switch network that alternates the DC input voltage and provides AC voltage to the HF transformer. The semiconductor switches are typically Insulated-Gate Bipolar Transistors (IGBTs) or Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs). The AC-DC converter rectifies the AC voltage from the HF transformer and provides DC voltage to the output terminal.

The reactive HF network consists of a series connected inductor and the HF transformer. It provides energy storage capability which is used to modify the shapes of the switch current waveforms in order to achieve low switching losses. This will in practice always

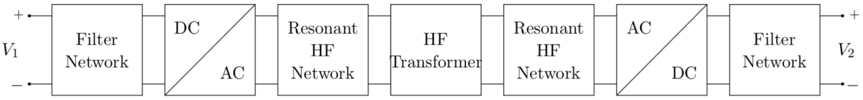


Figure 3.1: The required components for an isolated DC-DC converter.

be the case due to parasitic components in the HF transformer [36].

The network on the left side of the HF transformer is referred to as the primary side, while the network on the right side of the HF transformer is referred to as the secondary side.

3.1.1 Classification

Various types of inverter and rectifier units can be utilized in DC-DC converters, depending on the type of application. For high power application, half-bridge, full-bridge or push-pull topologies can be used to obtain effective DC to AC power conversion [36]. The full-bridge topology holds important advantages over the other topologies, as generating zero output voltage to the HF transformer. The advantages of the half-bridge converter is the lower amount of switches. However, the current rating of the switches is twice the rating as for the full-bridge topology. The magnitude of the half-bridge AC voltage is half of the one of the full-bridge topology, resulting in lower RMS currents in the HF transformer when utilizing the full-bridge topology instead of the half-bridge.

The push-pull topology has drawbacks as lower transformer utilization, need for additional snubber circuitry for transistor blocking voltage limitation, and challenges related to the requirement of a center tap on the transformer for high-power applications [37, 36, 38]. A higher voltage rating on switches results in higher conduction losses due to a higher on-resistance. The full-bridge converter is therefore the most commonly used topology, and is the topology that is considered in this thesis.

Unidirectional and Bidirectional Converters

Figure 3.2 shows an unidirectional full-bridge DC-DC converter. It is unidirectional due to the presence of diodes in the AC to DC conversion stage on the secondary side of the HF transformer, allowing for one direction of power flow only. A replacement of the diode bridge rectifier (DBR) with controllable switches will enable power transfer in both directions, and the converter becomes bidirectional. The bidirectional full-bridge converter is depicted in figure 3.3.

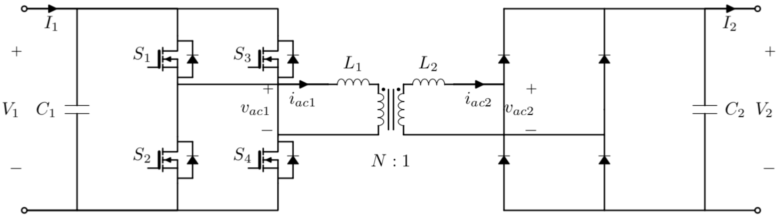


Figure 3.2: Unidirectional full-bridge DC-DC converter.

However, utilizing controllable switches instead of diodes, will increase the complexity of the control system and increase the cost of the converter.

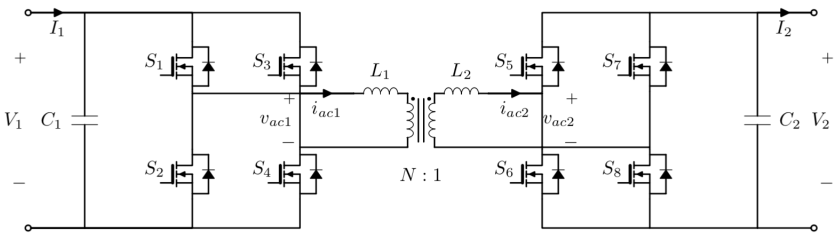
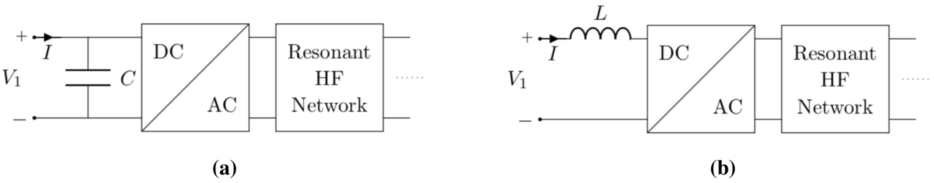


Figure 3.3: Bidirectional full-bridge DC-DC converter.

Voltage-fed and Current-fed Converters

Depending on their input circuit, DC-DC converters can be classified as either *voltage-fed* or *current-fed* converters. The voltage-fed converter is shown in 3.4 (a) and has a capacitor in parallel with its input terminal, acting like a voltage source. The current-fed converter is shown in 3.4 (b) and has an inductor in series with its input terminal, acting like a current source.



(a) **(b)**

Figure 3.4: DC-AC converter, (a) voltage-fed, (b) current-fed.

The type of converter to utilize depends on the system application, and it can affect the current and voltage waveforms of the converter to a large extend.

3.2 Full-Bridge Isolated DC-DC Converters

The isolated full-bridge converter is one of the most promising topologies for unidirectional power conversion application [39, 40]. By connecting the PV array to the MMC SM through an isolated full-bridge DC-DC converter, a realization of a high efficiency, decentralized PV MMC plant connected directly to MV grid is possible. without the use of a step-up transformer is possible. This configuration provides high MPPT granularity and does not require a step-up transformer.

The full-bridge converter has high power efficiency for a wide variable input voltage range, which is essential in providing a PV MMC Plant with high efficiency. It holds advantages due to its low numbers of components, high power capabilities, evenly shared currents in the switches and soft switching properties [36].

The full-bridge converter consists of four controllable semiconductor switches S_{1-4} on the primary side of the HF transformer, and four switches S_{5-8} (controlled or uncontrolled) on the secondary side. These are switched with a switching frequency f_{sw} to provide a time varying, square wave voltage $v_s(t)$ to the HF network in order to transfer power.

3.2.1 Efficiency and Power Losses

The power losses in the DC-DC converter can be classified in four loss components: switching loss P_{sw}, conduction loss P_{cond}, copper loss P_{cu}, and core loss P_{fe}:

$$P_{loss} = P_{sw} + P_{cond} + P_{cu} + P_{fe} \tag{3.1}$$

The switching and conduction losses are caused by the switching devices, and the copper and core losses are caused by magnetic devices in the circuit. Ohmic loss is a description of the losses that are proportional with the square of the rms value of the AC current. Both the conduction loss and the copper loss are ohmic losses.

The total efficiency of the converter is given as the relationship between the power at the output terminals at the power at the input terminals:

$$\eta = \frac{P_{out}}{P_{in}} = \frac{P_{in} - P_{loss}}{P_{in}} \tag{3.2}$$

The efficiency is therefore a function of switching frequency f_{sw}, operating power P_{dc} and the output voltage V_{dc}.

3.2.2 Control and Modulation

The input and output load of the DC-DC converter often fluctuates. In order to obtain the desired output voltage level, the average DC output voltage of the DC-DC converter must be controlled [9].

The average value of the output voltage depends on the on- and off-durations, t_{on} and t_{off}, of the controllable switches.

Pulse-Width Modulation switching

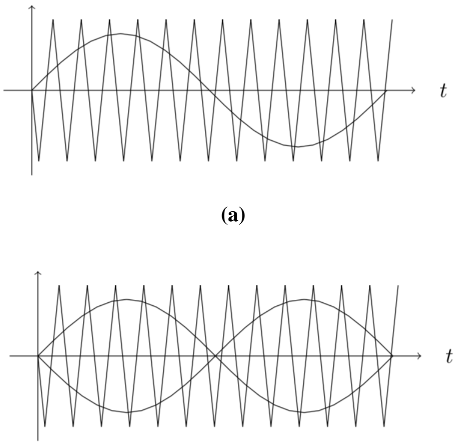
In the *pulse-width modulation* (PWM) method, the switching instances in the converter are determined by comparing the reference voltage wave - often a sinusoidal one - with a higher frequency repetitive triangular carrier. The repetitive triangular carrier frequency is kept constant in the PWM method, and is normally in a few kilohertz to a few hundred kilohertz range.

The switch is turned on when the reference voltage exceeds the magnitude of the carrier, and turned off when the carrier exceeds the reference voltage. The frequency of the repetitive triangular carrier decides the switching frequency.

The constant switching frequency results in a constant switching time period. The switch duty ratio D is therefore varied. D is defined as the ratio of the on-duration to the switching time period:

$$D = \frac{t_{on}}{T_s} \tag{3.3}$$

where $T_s = t_{on} + t_{off}$.



(a)

(b)

Figure 3.5: Pulse-width modulation with (a) bipolar switching, and (b) unipolar switching.

Figure 3.6

Unipolar and bipolar PWM

PWM with bipolar switching treats the switches in the full-bridge as pairs; the diagonal switches are connected to the same switching pulse, synchronizing the switching instances for the diagonal pairs. Switches in each pair are turned on and on simultaneously. This is depicted in figure 3.5 (a).

In PWM with unipolar switching, the switches in each leg are controlled independently. The switching instances are determined by comparing the carrier with the positive sinusoidal reference voltage for one leg and with the negative of the sinusoidal reference voltage for the other leg. The upper switch in the first leg is turned on when the sinusoidal reference voltage exceeds the carrier, and the lower switch is off. When the carrier exceeds the reference voltage, the lower switch turns on, and the upper turns off. For the second leg, the upper switch turns on when the negative of the sinusoidal reference voltage exceeds the carrier, and the lower switch is then off. When the carrier exceeds the reference voltage, the lower switch turns on and the upper turns off. Unipolar PWM switching is depicted in figure 3.5 (b).

The duty ratio Figure 3.6 (cond. ark) depicts how the inductor current varies with the duty ratio.

3.3 The High-Frequency Transformer Network

The HF transformer is required to provide electrical isolation in the circuit and protect the PV strings from the power grid. The motivation for using high switching frequency is to reduce the size of the transformer. However, increasing the switching frequency will increase the skin and proximity effect in the transformer core. It is therefore a critical component when designing the DC-DC converter.

Losses in the HF transformer has a significant impact on the efficiency and reliability of the converter, and the transformer design is therefore important towards achieving high efficiency in the converter. Power transformers that are small in weight and size and have low power losses. Using a high switching frequency will reduce the size of the transformer [9], but will increase the skin and proximity effects in the core [36].

This section first presents the transformer basics and presents different transformer and wire designs. Then the basics of magnetic behavior and effects are addressed, before losses in the transformer and the windings looked at. At the end of this section, a method for designing the HF transformer and wire is presented.

3.3.1 Isolation Transformer Representation

The transformer has N_p turns in the primary side winding and N_s turns in the secondary side winding. The turns ratio is given by N_p/N_s. In the ideal transformer, the relationship between the turns ratio and the primary and secondary side voltage is:

$$\frac{v_p(t)}{v_s(t)} = \frac{N_p}{N_s} \tag{3.4}$$

And the relationship between the turns ratio and the primary side and secondary side current is:

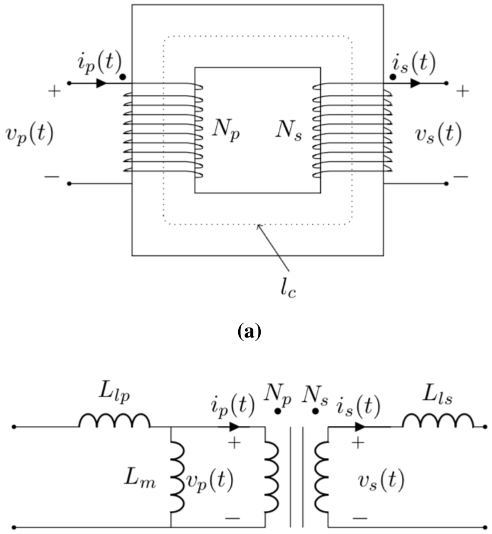
$$N_p i_p(t) = N_s i_s(t) \tag{3.5}$$

The HF transformer alters the AC voltage amplitude provided by the primary side according to its turns ratio, and applies $v_s(t) = v_p(t)\frac{N_s}{N_p}$ to the secondary side of the converter. Figure 3.7 (a) depicts a two-winding transformer. When neglecting the losses, the equivalent circuit for the transformer can be drawn as in figure 3.7 (b). L_m is the magnetizing inductance referred to the primary side of the transformer, and L_{lp} and L_{ls} are the primary and secondary side leakage inductances respectively.

It is desirable to reduce the magnetizing inductances that will be present in the real transformer by obtaining a close coupling between the primary and secondary side windings. This is because the energy from the leakage inductances has to be absorbed by the switches and their snubber circuits. It is also desirable to have a large magnetizing inductance to reduce the magnetizing current i_m. This is because the magnetizing current flows through the switches of the DC-DC converter, which increases their current ratings [9]. However, the leakage inductances have only a small effect on the converter voltage transfer characteristics.

Transformer Dot Convention

For real transformers, it would only be possible to tell the secondary side's polarity if the transformer was opened and examined [41]. Transformers therefore utilize the *dot convention*. The dots at the upper end of both the windings on the transformer seen in figure 3.7 tell the polarity of the voltage and current on the secondary side of the transformer, when the primary side voltage and current polarity is given. If the primary



(a)

(b)

Figure 3.7: Transformer representation, (a) two-winding transformer, (b) equivalent circuit.

side voltage is positive at the dotted end of the winding with respect to the undotted end, then the secondary side voltage will be positive at the dotted end also. If the primary side current of the transformer flows into the dotted end of the primary side winding, the secondary side current will flow out of the dotted end of the secondary winding. The use of the dot convention is depicted in figure 3.7.

3.3.2 HF Transformer Designs

Figure 3.8 shows different types of transformer cores.

Magnetic Core Materials

According to [9], materials used for magnetic cores can be classified in two broad classes depending on their magnetic properties: alloys and ferrites.

Alloys have a large flux density saturation limit, up to 1.8 T. These materials have high eddy current losses and must therefore be laminated even at low frequencies. Cores can also be made of powdered iron and powdered iron alloys. They feature electronically isolated iron particles, thus having significantly larger resistivity than a laminated core resulting in lower eddy currents. However, this results in a low permeability.

Ferrites have a large resistivity and a low flux density saturation limit (typically 0.3-0.4 T). This results in low eddy current losses, and they are therefore suited for high frequency operations. Ferrites are the best core material for high frequency applications due to their high resistivity [42], and is therefore chosen as the core material in this thesis.

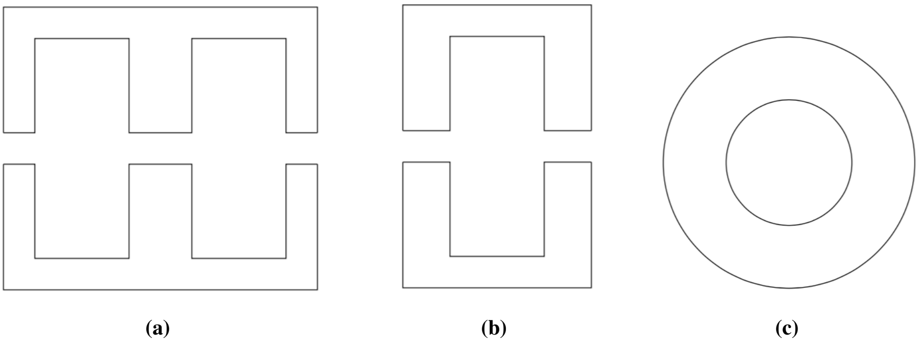


Figure 3.8: Transformer cores, (a) double-E core, (b) double-U core, (c) toroidal core.

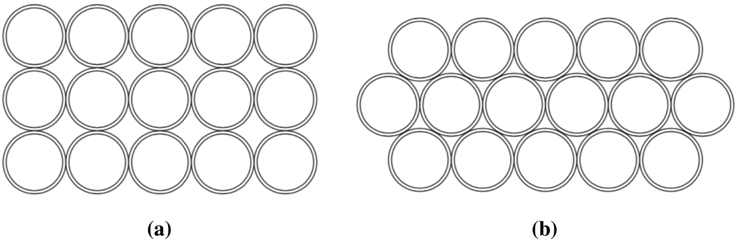


Figure 3.9: Round wires fitting, (a) square fitting, and (b) hexagonal fitting.

Coil Windings and Fill Factor

The conductors used in transformer windings are normally made from copper due to its high conductivity and ductility which makes it easy to bend into tight windings. This minimizes the use of copper, and therefore the size and weight of the transformer windings [9].

The copper fill factor α_{cu} defines the ratio between the total area of the copper windings and the area of the core window A_w [9], where the area of the copper windings equals the product of the number of windings N and the wire cross-sectional area a_{cu}:

$$\alpha_{cu} = \frac{N a_{cu}}{A_w} \tag{3.6}$$

The fill factor depends on several aspects: the type of coil former used; the insulation thickness compared to the wire diameter; the creepage distance and insulation sheets; and the accuracy of the winding equipment.

For round wires, the copper fill factor is typically 0.5-0.7. There are two types of fitting for round wires: square fitting and hexagonal fitting [42]. For square fitting, the wire fit in a square grid as shown in figure 3.9 (a). The theoretical filling factor is then determined by:

$$\alpha_{cu} = \frac{\pi}{4}\left(\frac{d_{cu}}{d_0}\right)^2 \tag{3.7}$$

where d_{cu} is the effective diameter of the copper wire, and d_0 is the outer diameter of the enameled copper wire. Hexagonal fitting is shown in figure 3.9 (b), and the theoretical filling factor is [42]:

$$\alpha_{cu} = \frac{\pi}{2\sqrt{3}}\Big(\frac{d_{cu}}{d_0}\Big)^2 \tag{3.8}$$

In the ideal case $d_{cu} = d_0$.

Foil wires are suited for high frequency and high current applications [8]. This is due to low eddy current losses for fields parallel to the foil. The filling factor depends on the copper foil thickness t_{cu}, and the foil insulation thickness d_i:

$$\alpha_{cu} = \frac{t_{cu}}{t_{cu} + d_i} \tag{3.9}$$

It is possible to obtain a high filling factor if $t_{cu} >> d_i$.

Rectangular cross-section wires are often the preferred solution in large transformers handling high current at 50 Hz.

Litz wires are multistranded conductors used to reduce eddy currents at high frequencies [42]. The strands are isolated from each other and assembled in groups that again are isolated from the other groups. This results in lower high-frequency losses, but the Litz wire has a low copper fill factor, normally around 0.3-0.4. This is due to that the isolation takes more space around the windings compared to the topologies.

3.3.3 Magnetic Behavior and Effects

Electromagentics

If an electric field is set up across a conducting material, an electrical charge is flowing across the material. This average flow is the current density J, and is given by [43]:

$$J = \sigma\epsilon \tag{3.10}$$

where σ is the conductivity of the material and ϵ is the electric field intensity. This is equivalent with Ohm's law when expressed in terms of element voltage and current:

$$I = \frac{V}{R} \tag{3.11}$$

The resistance R of a material is given by the material's properties:

$$R = \frac{l}{\sigma A_c} \tag{3.12}$$

l is here the length of the material and A_c is the cross sectional area. In comparison, if a magnetic field H is set up across a magnetic material, a magnetic flux density B is set up in the material:

$$B = \mu H \tag{3.13}$$

where μ is the magnetic permeability of the material and B is measured in Tesla $[T]$.

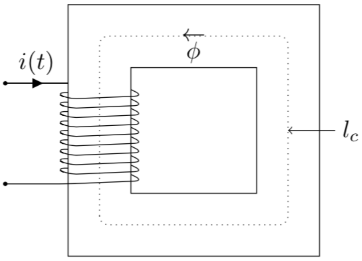


Figure 3.10: Simple transformer

Figure 3.10 shows a cross section of a simple transformer with one coil. When applying an alternating current $i(t)$ to one side of a transformer, the current produces an alternating magnetic field in the area around it, which again produces a flux in the core. This induces a voltage in coils of wires that the magnetic field passes through [41]. This is the principle of transformer action and is briefly explained here.

This magnetic field is governed by Ampere's law. When the current is carried by wires in a coil with N turns this becomes:

$$\oint \mathbf{H} * d\mathbf{l} = \int_S \mathbf{J} * d\mathbf{S} = Ni \tag{3.14}$$

where $\mathbf{H}$ is the magnetic field intensity produced by the effective current Ni, and $d\mathbf{l}$ defines the length along the integration path. $\mathbf{J}$ is the current density. Maxwell completed this law by adding a term on the right-hand side, called the displacement current:

$$\oint \mathbf{H} * d\mathbf{l} = \int_S \mathbf{J} * d\mathbf{S} + \frac{\delta}{\delta t}\int_S \epsilon\mathbf{E} * d\mathbf{S} \tag{3.15}$$

ϵ is here the permittivity of the material and $\mathbf{E}$ is the electrical field. For power electronics, the displacement current can often be neglected since the current density is dominating [42]. This is called quasi-static approach. But for currents in capacitors caused by parasitic capacitances, and applications with high frequency and low current density, the displacement current is of great importance.

For a transformer with N turns and a core with mean path length equal to l_c, equation 3.14 simplifies to:

$$H * l_c = N * i \tag{3.16}$$

The effective current flow applied to the core is equivalent to the magnetomotive force (MMF), normally measured in Ampere-turns:

$$\mathcal{F} = Ni \tag{3.17}$$

The magnetic field intensity $\mathbf{H}$ leads to a resulting magnetic surface flux density $\mathbf{B}$ produced in the material, given by:

$$\mathbf{B} = \mu\mathbf{H} \tag{3.18}$$

where μ is the magnetic permeability of the core material and is equal to the product of the permeability of free space, $\mu_0 = 4\pi 10^{-7}$, and the relative permeability of the magnetic material of the transformer core, μ_r. For ferromagnetic materials, μ_r varies from several hundred to tens of thousands resulting in a magnetic permeability much greater than for free space [42, 41]. If μ_r is equal to 6000, 6000 times more flux is established in an area of ferromagnetic material than in the same area of free space for a given current. The total value of flux ϕ passing through a cross-sectional area A_c in the core is equal to $\mathbf{B}$ integrated over the area:

$$\phi = \int_A \mathbf{B} * d\mathbf{A} \tag{3.19}$$

If the flux density vector is uniform and perpendicular to the whole cross-sectional area A_c of the transformer core, equation 3.19 simplifies to:

$$\phi = BA_c \tag{3.20}$$

Which, by rearranging equation 3.16 and inserting in 3.20, knowing that $B = \mu H$, can be written as:

$$\phi = \frac{\mu NiA}{l_c} \tag{3.21}$$

If the flux is time-changing and passing through a winding, it induces a voltage given by Faraday's law:

$$v_{ind}(t) = -N\frac{d\phi(t)}{dt} \tag{3.22}$$

The minus sign in equation 3.22 comes from Lenz' law which states that the voltage $v_{ind}(t)$ generated by a time-changing magnetic flux $\phi(t)$ has the direction to drive a current in the closed loop that induces a flux opposing the change in the original flux [42]. This determines the polarity of the voltages induced in transformer windings.

The MMF drives the flux in a magnetic core, which is analogue to the voltage that drives the current in an electric circuit. The counterpart of electrical resistance is reluctance $\mathcal{R}$, and the relationship between the MMF, flux and reluctance is given by:

$$\mathcal{F} = \phi\mathcal{R} \tag{3.23}$$

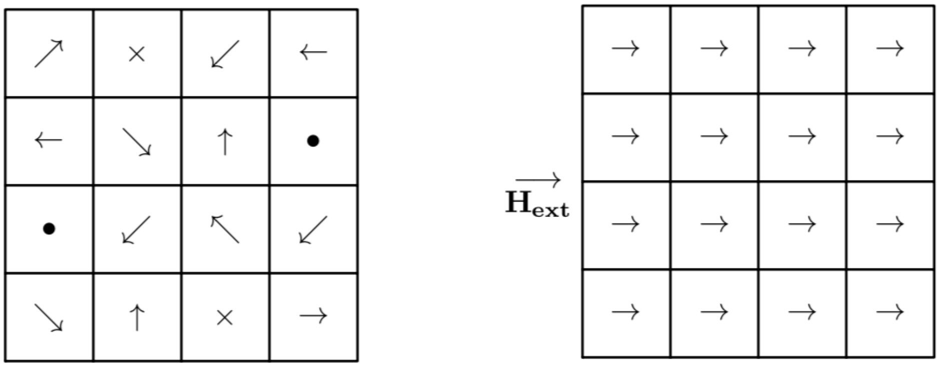
By inserting 3.21 in 3.23, and knowing that $\mathcal{F} = Ni$, it is seen that the reluctance is equal to:

$$\mathcal{R} = \frac{l_c}{\mu A} \tag{3.24}$$

However, calculations of flux in a magnetic core is not very accurate due to: leakage flux, flux escaping in the surrounding air; a varying permeability; and the fringing effect [41].

The Magnetizing Process

In a ferromagnetic material, the inter-atomic forces tend to align the small magnetic moment of all atoms in the same direction within certain regions containing a large number of atoms. These regions are called ferromagnetic domains or Weiss domains [42]. However,



(a) **(b)**

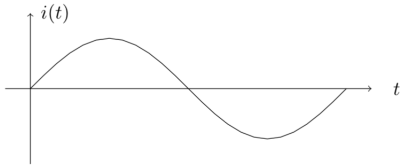
Figure 3.11: (a) Magnetic domains orientated randomly, (b) Magnetic domains lined up in the presence of an external magnetic field.

the direction of the domain magnetic moment vary from domain to domain, as depicted in figure 3.11 (a).

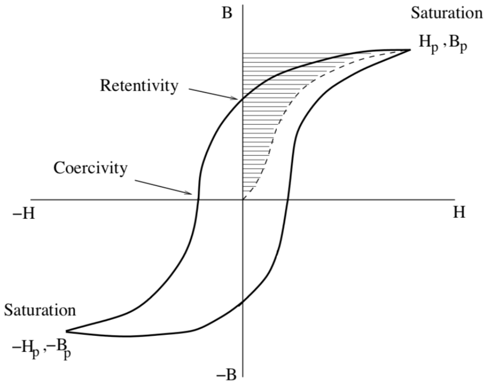
When a ferromagnetic material is subjected to an external magnetic field $\mathbf{H_{ext}}$, a torque is tending to rotate the domain magnetic moments in the same direction as $\mathbf{H_{ext}}$. Domains with a magnetic moment in the same direction as $\mathbf{H_{ext}}$, do not experience this torque. When the applied magnetic field is small, the torque moves the domain walls by increasing the magnetic moment in domains aligned in the same direction as $\mathbf{H_{ext}}$ and decreasing magnetic moment in domains aligned in the opposite direction. This process is first slowly and the displacement of the domain walls are reversible, but this process increases the magnetization, which is the average value per unit volume of all atomic magnets [42]. When the external magnetic field is strong enough, sudden jumps of the magnetic domain walls, called Barkhausen jumps, occurs. These are non-reversible domain wall displacements, which induces very intense and brief eddy current pulses near the domain walls. These eddy currents dissipate a finite amount of energy, causing hysteresis in the B-H relation and the sum of these accounts for the hysteresis loss.

When the magnetization is increased even more, domain rotation occurs in the direction of $\mathbf{H_{ext}}$. This process is called the magnetizing process and is showed in figure 3.11 (b).

Assume that the flux and magnetic field initially are zero in the transformer in figure 3.10. When an alternating current $i(t)$, as in figure 3.12 (a), is applied to the transformer, a magnetic field intensity H is produced in the core, according to Amperes law in equation 3.14. As the current increases for the first time, reversible domain walls displacements occurs and the magnetic field is slowly rising. This corresponds to the path a-b in figure 3.12 (b). When the magnetization has reached a certain level, Barkhausen jumps of the magnetic domain walls starts to occur, and the magnetic flux density $\mathbf{B}$ increases rapidly with an increase in $\mathbf{H}$, resulting in a steep curve from b-c. When all domains are aligned in the direction of the applied magnetic field $\mathbf{H_{ext}}$, a further increase in the magnetic flux $\mathbf{B}$ is not possible and the magnetization curve flats out. The core material has then reached



(a)



(b)

Figure 3.12: Transformer magnetization, (a) The applied current $i(t)$, (b) The resulting hysteresis loop [8].

saturation in d, which gives the maximum value of the magnetic flux density B_p. A further increase in $\mathbf{H}$ does not result in a significant increase in $\mathbf{B}$.

When the current $i(t)$ falls, the domains are rotating back to their initial direction and some of the domain walls jumps back to their initial position. But most of the domain walls remains in the displacement position. The flux will therefore trace out a different path then a-d. When H falls, B lags behind, resulting in a residual magnetic flux B_r in the core when H has dropped to zero. To reduce the magnetic flux to zero, a negative field is required. When the alternating current goes negative, B drops to zero at $-H_c$. This value of the magnetic field is called coercivity and is sufficient to restore the initial positions of the domain walls. A further decrease in the current leads to a magnetization in the opposite direction until saturation is reached ($|-B_p| = B_p$). The alternating current will trace out the hysteresis loop, as depicted in figure 3.12 (b), which gives the relation between the flux density $\mathbf{B}$ and the magnetic field intensity $\mathbf{H}$. The hysteresis loop shows that the flux in the core depends on both the current applied to the windings and the previous history of flux in the core. The area of the surface of the loop equals the hysteresis loss per volume for one complete magnetization cycle [42].

To avoid saturation in the HF transformer core in steady state operation, the average values of the AC terminal voltages, $v_p(t)$ and $v_s(t)$, have to be zero when evaluated over one switching period.

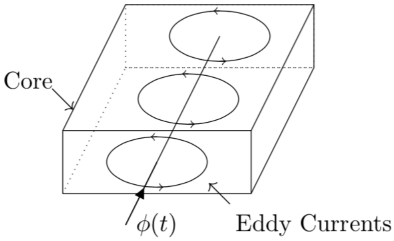


Figure 3.13: Eddy currents in the magnetic transformer core.

Eddy Current Effects and Skin Depth

Due to the relatively high conductivity of the magnetic core, the time-changing magnetic flux induces an internal voltage $d\Phi/dt$ within the core, in the same manner as it is inducing voltages in windings, described by equation 3.22. These voltages causes swirls of currents around the flux path, termed eddy currents. They are flowing in the resistive material of the transformer core, dissipating energy and causing heating losses [41].

Eddy currents flow in a direction such that new magnetic fields are produced opposing the applied magnetic field, as showed in figure 3.13. These opposing magnetic fields results in an exponential decreasing magnetic field in the core. This results in a current density largest near the surface of the core, decreasing with the depth of the core until a level called *skin depth*. No current is flowing interior this level, and this is determined as the *skin effect*. The skin depth is dependent on the frequency of the applied magnetic field $f = \omega/2\pi$, and the permeability μ and the conductivity σ of the magnetic core material:

$$\delta = \sqrt{\frac{2}{\omega\mu\sigma}} = \sqrt{\frac{2\rho}{\omega\mu}} \tag{3.25}$$

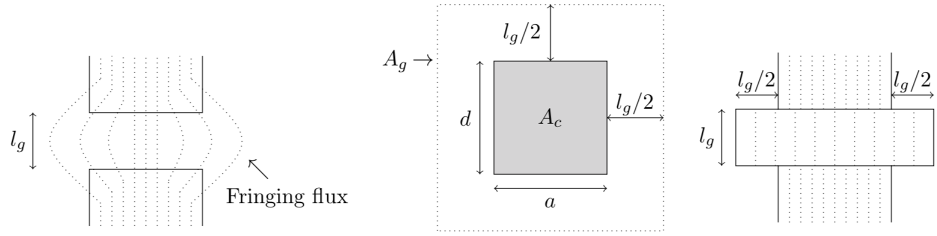
where ρ is the resistivity of the material. If the cross-sectional dimension of the core is much larger than the skin depth, the current is mostly flowing on the surface. The effective AC reluctance of the core is then increased for the given frequency.

Fringing Effect

If an air gap is present in the magnetic core, the flux will be fringing as showed in figure 3.14. This is called the fringing effect and it has two effects: increased cross section area of the air gap; and increased length of the magnetic path at the air gap. The flux will spread over an area greater than the cross section, resulting in a reduced theoretical reluctance at the air gap, which makes errors in estimated values from calculations. The flux density in the air gap is then significantly lower than the flux density in the core [42].

The fringing effect increases with an increased air gap and makes the reluctance more difficult to estimate.

A simple analysis of the fringing effect is presented in [9]. Assuming a transformer with an air gap of length l_g and a cross-sectional area of $A_c = d * a$, as showed in figure 3.14. The flux lines form closed loops, called the continuity of flux, meaning that the flux



(a) **(b)** **(c)**

Figure 3.14: Approximation of the fringing effect from [9], (a) the fringing flux, (b) the effective cross-sectional area of the air gap, and (c) the equivalent representation of the air gap.

lines entering a closed surface area must equal those leaving it. This is expressed as:

$$\phi = \int \int_A \mathbf{B} * d\mathbf{A} = 0 \tag{3.26}$$

where A is a closed surface. For the transformer in figure 3.14, this means:

$$B_c A_c + B_g A_g = 0 \tag{3.27}$$

From figure 3.14 (c), it is seen that the cross-sectional area of the air gap A_g is given by:

$$A_g = (a + l_g)(d + l_g) = A_c + (a + d)l_g + l_g^2 \tag{3.28}$$

Resulting in a core flux density B_c:

$$B_c = B_g \frac{A_g}{A_c} \tag{3.29}$$

Since $A_g > A_c$, the flux density in the core is greater than the flux density in the air gap.

The reluctance of the air gap $\mathcal{R}_g$ can be written as, using equation 3.24, an air gap of length l_g and a cross-sectional area A_g given by equation 3.28:

$$\mathcal{R}_g = \frac{l_g}{\mu_0 [A_c + (a + d)l_g + l_g^2]} \tag{3.30}$$

[8] has modified this expression by including fringing flux at the corners:

$$\mathcal{R}_g = \frac{l_g}{\mu_0 [A_c + 2(a + d)l_g + \pi l_g^2]} \tag{3.31}$$

The total reluctance of the transformer then becomes:

$$\mathcal{R}_t = \mathcal{R}_c + \mathcal{R}_g \tag{3.32}$$

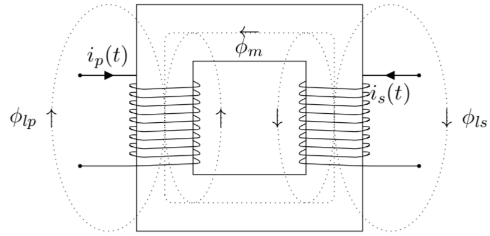


Figure 3.15: Mutual and leakage fluxes in the transformer core.

Mutual Flux and Leakage Flux

The average flux that is present in the transformers primary winding is proportional to the integral of the applied voltage, where the proportionality constant is the reciprocal of the number of turns in the primary side winding [41]:

$$\overline{\phi}_p = \frac{1}{N_p} \int v_p(t)dt \tag{3.33}$$

$\overline{\phi}_p$ is the average flux in the primary side, N_p is the number of turns in the primary side winding, and $v_p(t)$ is the applied voltage to the primary side.

Most of this flux will stay in the transformer core and also pass through the secondary side winding. This flux links the primary and secondary side winding and is named *mutual flux*. However, as seen in figure 3.15, some of the flux will pass through the air instead. This flux is called *leakage flux* and is much smaller than the mutual flux. The primary side flux therefore consists of both leakage flux and mutual flux:

$$\overline{\phi}_p = \phi_m + \phi_{lp} \tag{3.34}$$

where ϕ_m is the mutual flux and ϕ_{lp} is the primary side leakage flux. This is equal for the average flux from the secondary side winding $\overline{\phi}_s$:

$$\overline{\phi}_s = \phi_m + \phi_{ls} \tag{3.35}$$

ϕ_{ls} is here the secondary side leakage flux that returns through the air and bypasses the primary side winding.

Proximity Effect

In the same manner as skin effect occurs in transformer cores, it occurs in the copper conductors used in transformer windings [9]. The applied time-varying current $i(t)$ generates a magnetic field which again generates eddy currents flowing in the conductor. At high frequencies, the major part of the current is flowing in the outer layer if the conductor, resulting in a small skin depth. The magnetic flux is perpendicular to the direction of the applied current. The generated eddy currents will therefore flow either in parallel or in anti-parallel to the applied current as showed in figure 3.16. This results in that the eddy

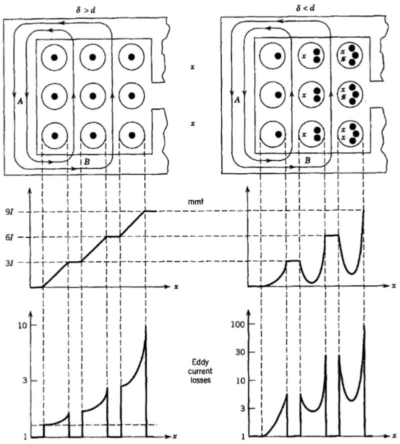


Figure 3.16: Eddy currents generated by the proximity effect in the magnetic transformer core [9].

current losses in wires close to each other are much larger than in a free wire. This is due to the transverse field made by the adjacent conductors and is called the proximity effect. Both the skin effect and the proximity effect will occur simultaneously in a conductor carrying an alternating current when it is exposed to an external alternating field, which is the case for a conductor used in a transformer winding. These eddy currents have three major effects: heat due to ohmic losses; opposite magnetic reaction field; and additional forced due to interaction of induces and inducing fields.

3.3.4 Power Losses and Heating Effects

The total losses in the HF transformer can be divided into core losses P_{fe} and winding losses P_{cu}:

$$P_{tr} = P_{fe} + P_{cu} \tag{3.36}$$

They are in this section expressed in terms of geometry, material, winding and excitation parameters.

3.3.5 Ferrite Core Losses

Core losses in ferrites consists of a sum of hysteresis, eddy current, and residual loss components [42]. They can be treated separately assuming independence of each other. This is important since the different losses exhibits a different power law depending on frequency and the flux density.

Hysteresis Core Losses

The hysteresis loss caused by the dissipated energy due to eddy currents and hysteresis in the B-H relation described earlier accounts for the hysteresis loss $P_{fe,h}$. These hysteresis ferrites losses is given by the Steinmetz equation [42]:

$$P_{fe,h} = k_h f^{\alpha} B_m^{\beta} \tag{3.37}$$

where k_h is a hysteresis loss coefficient, β is the core loss exponent depending on the core material, α is the frequency loss component, f is the magnetization frequency, and B_m is the peak flux density. For commonly used ferrites, $\alpha = 1.2 - 2$ and $\beta = 2.4 - 3$ [42].

Eddy Current Effects in the Core

The eddy current losses depends on the size of the current swirls and the resistivity of the transformer core material. For a given core material and thickness, the eddy current losses $P_{fe,ec}$ per volume is given by [42]:

$$P_{fe,ec} = k_e \frac{f_s^2 B_m^2}{\rho_{fe}} \tag{3.38}$$

where k_e is a dimensionless loss coefficient and ρ_{fe} is the internal resistivity of the core and equals $1/\sigma$. The peak flux density B_m for a full-bridge DC-DC converter is given by [9]:

$$B_m = \frac{V_p D}{2 N_p A_c f_s} \tag{3.39}$$

With a duty D of 0.5, the eddy current losses can be written as:

$$P_{fe,ec} = \frac{k_e}{\rho_{fe}} \left(\frac{V_p}{4 N_p A_c} \right)^2 \tag{3.40}$$

However, this is just an approximation of the actual eddy current losses, due to a frequency and temperature dependency of the resistivity.

Residual Loss

A third loss component is required to obtain more accurate core losses. This loss is called residual loss $P_{fe,r}$ and is due to magnetic relaxation and resonances in the ferrite core material. Residual losses are strongly dependent on the frequency, and can be reduces by using fine-grained ferrites [42].

Total Core Losses

The total losses in the core is given by the sum of the three losses described above:

$$P_{fe} = P_{fe,h} + P_{fe,ec} + P_{fe,r} = k_h f^{\alpha} B_m^{\beta} + k_e \frac{f_s^2 B_m^2}{\rho_{fe}} + P_r \tag{3.41}$$

However, the losses in the core are small compared to the copper winding losses.

3.3.6 Copper Winding Losses

Ohmic loss

Ohmic loss occurs in copper conductors as a result of the DC resistance. For one winding, the ohmic power dissipation is:

$$P_{cu,dc} = I_{rms}^2 R_{dc} \tag{3.42}$$

where R_{dc} can be found directly from the transformer characteristics. For a two winding transformer the total power dissipation from ohmic losses becomes [44]:

$$P_{cu,dc} = I_p^2 R_p + I_s^2 R_s \tag{3.43}$$

where I_p and R_p are the primary side rms current and DC resistance respectively, and I_s and R_s are the secondary side rms current and DC resistance respectively.

The DC winding resistances can be expressed as:

$$\begin{aligned} R_p &= \rho_{cu} \frac{l_{cu} N_p^2}{A_{cu,p}} \\ R_s &= \rho_{cu} \frac{l_{cu} N_s^2}{A_{cu,s}} \end{aligned} \tag{3.44}$$

where ρ_{cu} is the copper resistivity; l_{cu} is the average length of winding turn; $A_{cu,p}$ and $A_{cu,s}$ are the total area of the primary and secondary windings respectively; and N_p and N_s are the number of turns on the primary and secondary windings respectively. Inserting 3.44 equation 3.43 can be rewritten as:

$$P_{cu,dc} = I_p^2 \rho_{cu} \frac{l_{cu} N_p^2}{A_{cu,p}} + I_s^2 \rho_{cu} \frac{l_{cu} N_s^2}{A_{cu,s}} \tag{3.45}$$

Eddy Current losses

In the same manner as skin effect occurs in transformer cores, it occurs in the copper conductors used in transformer windings [9]. The resulting dissipate power P_{ec} will contribute to the winding losses, and can be given as:

$$P_{cu,ec} = I_{rms}^2 R_{ec} \tag{3.46}$$

where R_{ec} is the effective eddy current resistance.

Total Copper Winding Losses

Total power dissipated in a winding then becomes [9]:

$$P_{cu} = P_{cu,dc} + P_{cu,ec} = I_{rms}^2 R_{dc} + I_{rms}^2 R_{ec} = I_{rms}^2 R_{ac} \tag{3.47}$$

The effective resistance of the conductor windings is increasing with frequency due to the skin and proximity effects. Dowell considered this by deriving values for the AC resistance versus frequency [45]. Ferreira gave an exact solution for round wires [44]:

$$R_{ac} = R_{dc}\frac{\Delta}{2}\Big[\frac{sinh\Delta + sin\Delta}{cosh\Delta - cos\Delta} + (2m-1)^2\frac{sinh\Delta - sin\Delta}{cosh\Delta + cos\Delta}\Big] \tag{3.48}$$

where m is the number of layers in the winding section, R_{dc} is the DC resistance, and Δ is given by:

$$\Delta = \frac{\sqrt{\pi}}{2}\frac{d}{\delta} \tag{3.49}$$

d is here the wire diameter and δ is the skin depth given by equation 3.25. A similar treatment could have been done for the magnetizing current [44], but these losses are neglected in this thesis. Table A4 in appendix B gives the skin depth of copper wires at different frequencies.

3.3.7 Thermal Considerations

Heat transfer occurs as a result of temperature difference between regions. Heat is the rate of the energy transferred from a region with high temperature to a region with a lower temperature. This process continues until the regions have the same temperature. There are three heat transfer mechanisms – conduction, convection, and radiation [42].

The power losses get converted to heat, which increases the temperature in the core and the windings. The temperature increase reduces their performance and increase the losses even more. Thermal considerations are therefore important when designing the transformer. The resistivity of the copper windings increases with temperature, which gives higher ohmic losses. For ferrites, the minimum core loss occurs at around 100 °C, but increases with a further increase in the temperature [9]. The heat transfer mechanisms result in a equal steady-state temperature of the components. And the maximum allowable steady-state temperature of the system is defined by the lowest temperature rated component.

Conduction

Conduction heat transfer occurs in a substance due to energy differences in the particles of the substance. These energy differences are due to lattice vibrations and free flow of electrons in solids, and collision and diffusion in liquid and gases [8]. Energy is transferred from a high temperature region in the substance to a low temperature region along a temperature gradient. The conductive heat transfer capacity P_c is proportional to the cross-sectional area A_c and to the temperature gradient $\partial T/\partial x$ [42], and is given by Fourier's law:

$$P_c = k_t A_c \frac{\partial T}{\partial x} \tag{3.50}$$

where k_t is the thermal conductivity of the material. It is often a negative sign in this equation indicating that the heat flows downhill on the temperature slope $\partial T/\partial x$.

Convection

Convection is energy transfer between a solid surface and an adjacent fluid in motion. It also includes conduction to the boundary level of the fluid [8]. The heat transfer due to convection is proportional to the temperature difference of the surface of the heated body T_s and the adjacent fluid T_a, both measured in Kelvin $[K]$, and is given by Newton's law of cooling [42]:

$$P_{conv} = h_{conv} A_s (T_s - T_a) \tag{3.51}$$

where A_s is the surface area of the heated body where the convection heat transfer takes place and h_{conv} is the convection heat transfer coefficient. h_{conv} is not a property of the fluid, but an experimental determined parameter. This parameter is difficult to estimate, but for vertical plates h_{conv} is given by [42]:

$$h_{conv} = 1.42 \Big(\frac{T_s - T_a}{h} \Big)^{1/4} \tag{3.52}$$

where h is the height of the plate. This is in the case of natural convection.

Natural (or free) convection is when the fluid motion only occurs due to the density difference between the hot and cold air without any external source of movement. Forced convection is when there is an external source of movement to the fluid motion, for example a fan.

Radiation

Radiation is energy transfer in form of electromagnetic energy. This is the fastest type of heat transfer and does not require a material medium like conduction and convection. Radiation can therefore occur in vacuum. The heat transfer from radiation that can be emitted by a surface area A_s with absolute temperature T_s, is given by Stefan-Boltzmann law of thermal radiation:

$$P_{rad} = \epsilon_s \sigma A_s (T_s^4) \tag{3.53}$$

where ϵ_s is the emissivity of the surface, and σ is the Stefan-Boltzmann constant equal to $5.67 * 10^{-8}\ W/m^2 * K^4$.

Heat transfer from radiation between two surfaces is proportional to the difference in the absolute temperatures to the fourth:

$$P_{rad} = \epsilon_s \sigma A_s (T_s^4 - T_a^4) \tag{3.54}$$

3.3.8 HF Transformer Construction

The HF transformer needs to be designed for safe operation and to meet the circuit ratings. In order to keep the magnetization current low, the HF transformer does not consist of an air gap. For the transformer design, the following is required to be designed:

- Size of wire and number of turns to be used for primary and secondary windings.
- Core to be used.
- Resistance of the winding.

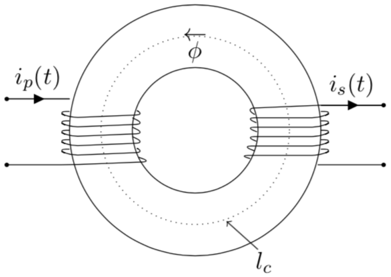


Figure 3.17: A simple toroidal transformer.

- Magnetizing inductance of the transformer.

However, the design of the transformer is beyond the scope of this thesis and is therefore not addressed in detail. It is left to the reader to choose a real core for the required specifications when designing the isolated DC-DC converter.

Specifications and assumptions

The specifications of a two winding transformer are listed below:

- Primary side rms voltage, V_p V
- Primary side rms current, I_p A
- Number of turns on primary side, N_p
- Secondary side rms voltage, V_s V
- Secondary side rms current, I_s A
- Number of turns on secondary side, N_s
- VA rating, $V_pI_p = V_sI_s$
- Frequency, f Hz

The ferrite toroidal core is depicted in 3.17. The toroidal core has a continuous magnetic path and yields the highest effective permeability and the lowest flux leakage of any transformer shape. The dimensions of the toroidal core are depicted in figure 3.18.

The window area A_w of the toroidal core accommodates both the primary and the secondary side of the transformer. The two windings are overlapping each other. It is assumed that the window is filled with conductors to a fraction of α_{cu}:

$$\alpha_{cu}A_w = N_pI_p + N_sI_s \tag{3.55}$$

α_{cu} is assumed to be 0.4 for the toroidal core [46].

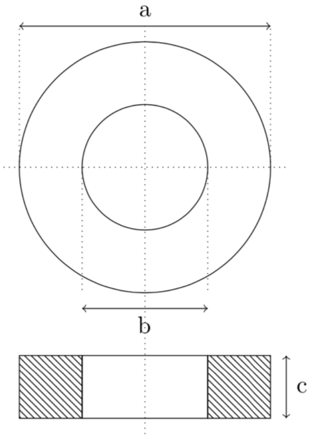


Figure 3.18: Toroidal core dimensions.

A magnetic material can only carry a certain maximum amount of flux density without saturating. If the core saturates, the relative permeability drops substantially, and saturation needs therefore to be avoided. The maximum allowable flux density is denoted B_m and is about 0.4 T for ferrites.

The choice of the transformer is an iterative process and the steps are shown below. These design steps are the same as described in [43].

Step 1 - Core Material and Size

The product of the core cross-sectional area A_c and the window area A_w is a measurement of the energy handling capability of the transformer, and relates the area product to the required VA rating of the transformer [43]. This determines the first selection of the cross sectional area of the transformer core and the window area. The area product is given by:

$$A_c A_w = \frac{VA}{2fB_m J_{cu} \alpha_{cu}} \tag{3.56}$$

The smallest core with an area product higher then the calculated one from equation 3.56 can be chosen from core tables. The core area A_c and the window area A_w can then be found from the core table for the selected core.

Step 2 - Select the number of turns

The number of turns on the primary and secondary side are calculated as follows:

$$\begin{aligned} N_p &= \frac{V_p}{4fB_m A_c} \\ N_s &= \frac{V_s}{4fB_m A_c} \end{aligned} \tag{3.57}$$

These numbers of N_p and N_s are rounded up to the nearest whole number and chosen as the primary and secondary side number of turns respectively.

Step 3 - Select the size of the wire for the secondary and primary side windings

The conductor can only carry a certain maximum amount of current per unit cross sectional area. This is equal to the current density capability given by:

$$J_{cu} = \frac{I_{rms}}{a_{cu}} \tag{3.58}$$

If this limit is exceeded, the wire will overheat due to the DC resistance. For a copper conductor, the current capacity is between 2 A/mm^2 and 5 A/mm^2 [43]. Rearranging equation 3.58, gives the minimum cross-sectional area of the primary and secondary side wire respectively:

$$\begin{aligned} a_{cu,p} &= \frac{I_p}{J_{cu}} \\ a_{cu,s} &= \frac{I_s}{J_{cu}} \end{aligned} \tag{3.59}$$

The primary and secondary side wires can be chosen from wire tables.

Step 4 - Check if A_w is big enough

It is then important to figure out if the required number of turn windings will fit in the selected core window in step 1.

The total area of the wires equals:

$$A_{cu} = N_p a_{cu,p} + N_s a_{cu,s} \tag{3.60}$$

This must be less or equal to the window area times the copper fill factor:

$$A_{cu} = N_p a_{cu,p} + N_s a_{cu,s} \leq \alpha_{cu} A_w \tag{3.61}$$

If this is not true, then a new size of the transformer core must be chosen.

Step 5 - Calculate the length of the wires

The length of the turns are calculated from the chosen core dimensions.

For a toroidal core, the mean length is difficult to calculate due to the many ways of winding. [46] has given an approximation for the mean length turn (MLT) to be:

$$MLT = 0.8(a + 2c) \tag{3.62}$$

where a is the diameter of the toroidal core, and c is the height of the core as depicted in figure 3.18. The total length of the wires then becomes:

$$\begin{aligned} l_{cu,p} &= MLT * N_p \\ l_{cu,s} &= MLT * N_s \end{aligned} \tag{3.63}$$

Step 6 - Resistance of copper wires

The copper DC resistance of the primary and secondary side windings can be found when knowing the total length l_{cu} of the wire, the cross-sectional area a_{cu}, and the resistivity ρ of the material:

$$R_{dc} = \frac{\rho l_{cu}}{a_{cu}} \tag{3.64}$$

Step 7 - Core Reluctance

The core reluctance is calculated from equation 3.24, reproduced here:

$$\mathcal{R} = \frac{l_c}{A_c \mu_0 \mu_r} \tag{3.65}$$

where l_c is the mean length of the transformer core, A_c is the cross-sectional core area, μ_0 is the permeability of free space, and μ_r is the relative permeability of the transformer core material.

Step 7 - Magnetizing Inductance

The magnetizing inductance can be found from:

$$L_m = \frac{N^2}{R} \tag{3.66}$$

3.4 Power Switching Devices

Power switching devices controls the power flow in power electronic systems by conducting current in the on-state and blocking the current in the off-state [43]. The ideal switch has two states, on and off, as depicted in figure 3.19. In the off-state, no current is conducted through the switch, and the switch can block any voltage:

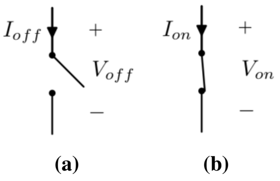


Figure 3.19: Ideal switch, (a) off-state, (b) on-state.

$$\begin{aligned} I_{off} &= 0 \\ -\infty < V_{off} &< \infty \end{aligned} \tag{3.67}$$

When the ideal switch is turned on, it can conduct any current with no voltage drop:

$$\begin{aligned} -\infty < I_{on} &< \infty \\ V_{on} &= 0 \end{aligned} \tag{3.68}$$

This implies that no power is dissipated in the ideal switch in either the on- or the off-state, and it therefore features zero conduction and blocking losses:

$$\begin{aligned} P_{on} &= 0 \\ P_{off} &= 0 \end{aligned} \tag{3.69}$$

The ideal switch also features instantaneous turn-on and turn-off, and does not need energy to switch between the two states or to maintain in either the on-state or the off-state. This results in zero switching losses and zero control effort:

$$\begin{aligned} t_{on} &= 0 \\ t_{off} &= 0 \\ P_{sw} &= 0 \end{aligned} \tag{3.70}$$

3.4.1 Real Switches

Real switches does not have the same features as ideal switches. In the off-state, real switches conduct a small current, termed *leakage current*. This current causes blocking losses greater than zero. Real switches also have limitations on the blocking voltage capacity.

$$\begin{aligned} I_{off} &\neq 0 \\ V_{-} < V_{off} &< V_{+} \\ P_{off} &\neq 0 \end{aligned} \tag{3.71}$$

where V_{+} and V_{-} are the upper and lower blocking voltage limits respectively.

In the on-state, the voltage across real switches are nonzero causing conduction losses. The conducting current capacity is also limited by the switches physics.

$$\begin{aligned} I_{-} < I_{on} &< I_{+} \\ V_{on} &\neq 0 \\ P_{on} &\neq 0 \end{aligned} \tag{3.72}$$

where I_{+} and I_{-} are the upper and lower conducting current limits respectively.

Real switches does not feature instantaneous switching, it takes some time to switch from one state to another:

$$\begin{aligned} t_{on} &\neq 0 \\ t_{off} &\neq 0 \end{aligned} \tag{3.73}$$

This limits the maximum operating frequency of the switch. The switching transition requires external energy to turn the switches on and off. This energy appears as turn-on and turn-off losses: ($E_{on} \neq 0$, $E_{off} \neq 0$). This is provided by an additional drive circuit.

Real switches are also thermally limited since the power dissipation is nonzero. The power dissipation appears at heat with rises the temperature of the switching device. Heat can increase the losses even further and result in component failure. It is therefore important to avoid unlimited temperature rise.

There are three types of switches:

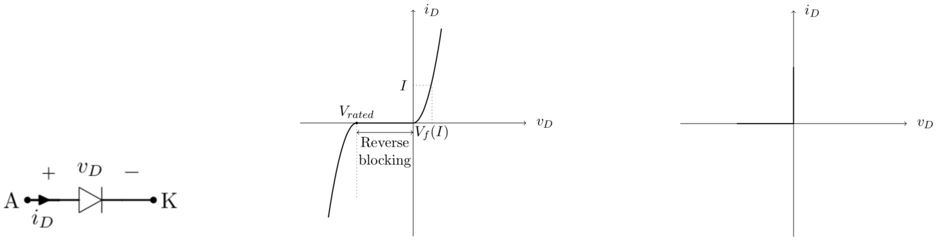
- Uncontrolled switches
- Semi-controlled switches
- Controlled switches

Uncontrolled switches are devices where the state is determined by the state of the power circuit. Diodes are uncontrolled switches where the current direction decides whether it is in on- or off-state. These devices does not have any external control. In semi-controlled switches, one of the states (on or off) can be controlled by external control. However, the other state is only reachable by intervention from the power circuit. An example on a semi-controlled switch is a thyristor. It is turned on by a current injected into its gate terminal, but can only be turned off by reducing the main current through the device to zero. Controllable switches are turned both on and off by control signals provided by external control. Examples of controlled switches are bipolar junction transistors (BJTs), metal-oxide-semiconductor field effect transistors (MOSFETs), gate turn off (GTO) thyristors, and insulated gate bipolar transistors (IGBTs) [9].

In this thesis, MOSFETs and diodes are utilized and are therefor the switches that are further looked at.

3.4.2 Diodes

The diode is a two terminal device with an anode (A) and a cathode (K) [43]. The circuit symbol and the i-v characteristics are showed in figure 3.20 (a) and (b) respectively. The idealized switching characteristics are showed in figure 3.20 (c).



(a) **(b)** **(c)**

Figure 3.20: Diode (a) circuit symbol, (b) i-v characteristics, (c) idealized switching.

When the diode is forward biased ($v_D > 0$), it is in the on-state and conducts current with a small forward voltage V_f across it. When the diode is reverse biased ($v_D < 0$), it is in the off-state and a small leakage current i_{rev} flows through it. This current is often neglectable.

At turn-on, the diode reaches the on-state with a small time delay called the forward-recovery time t_r. Due to a rapid turn-on compared to the transients in the power circuit, the diode can be considered as ideal [9] at turn-on. At turn-off, however, the diode current reverses for a time called reverse-recovery time t_{rr}, before falling to zero. This is depicted in figure 3.21. This negative (reverse-recovery) current is required to supply the reverse charge required in the diode to block the negative voltage across the junction. t_{rr} limits the switching frequency of the diode.

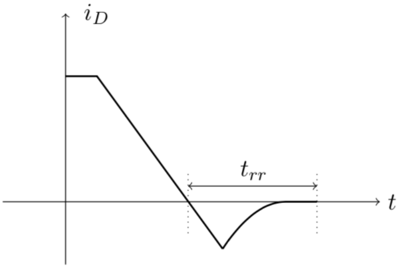


Figure 3.21: Diode reverse-recovery time t_{rr}.

The diode is an uncontrolled, unidirectional switch and does not have explicit control inputs. It reaches the on-state with a small delay t_r and conducts positive current when the device is forward biased. When the forward current goes to zero, it blocks the negative voltage and goes to off-state after a small time delay t_r.

Power Losses

When the diode is forward biased, it dissipates power due to the forward voltage drop V_f across the diode. These losses are conduction losses and are equal to:

$$P_{on} = V_f I_{on} \tag{3.74}$$

I_{on} is decided by the power circuit.

When the diode is reverse biased, it dissipated power due to the leakage current I_{rev}. These are blocking losses equal to:

$$P_{off} = V_{off} I_{rev} \tag{3.75}$$

Diode types

There are three different types of diodes available:

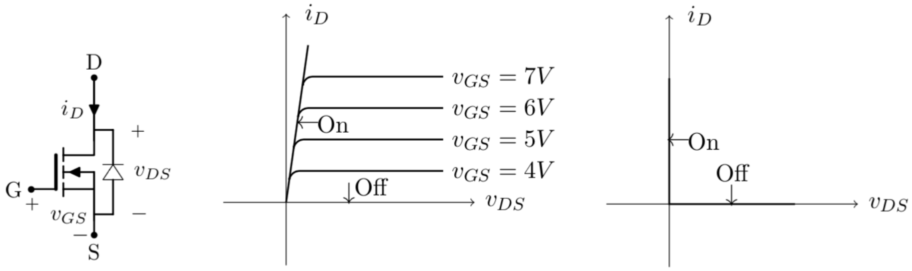
- Schottky diodes
- Fast-recovery diodes
- Line-frequency diodes

The chose of diodes depends on the application requirements. Schottky diodes have a low forward voltage drop, but has limited blocking voltage capabilities, typically 50-100 V. This diode is preferred in circuits where low conduction loss is desired. Fast-recovery diodes are designed to be used in high-frequency switching applications where a small reverse-recovery time is needed. they are often used in combination with controllable switches. Line-frequency diodes are suitable as rectifier diodes due to a very low forward voltage drop in the on-state. The voltage and current rating can be up to several kV and kA respectively, but they have a large reverse-recovery time. This is, however, acceptable for line-frequency applications.

3.4.3 Metal-Oxide-Semiconductor Field Effect Transistors

MOSFETs are voltage-controlled switches that consists of three terminals - drain (D), source (S), and gate (G) [9], as depicted in figure 3.22 (a). These devices have been available since the early 1980s [9], but research on new materials with substantial performance improvements is bringing new devices into the market. They have become popular in high frequency switching applications due to a fast switching speed and low switching losses. MOSFETs are available with voltage ratings up to 1700 V and current ratings at 73 A [1]. Data sheets for the MOSFETs utilized in this thesis are found in Appendix A.1. Both N-channel and P-channel MOSFETs are available, but N-channel is most common [43], and is the only one considered here.

v_{DS} is the drain-to-source voltage and form the power terminal pair, while v_{GS} is the gate-to-source voltage and form the control terminal pair. The gate is insulated from the circuit, and draws therefore no current at steady state. However, during the transient from on to off-state (or vice versa), the gate capacitance is being charged/discharged and a small current is flowing.



(a) **(b)** **(c)**

Figure 3.22: N-channel MOSFET (a) circuit symbol with body diode, (b) i-v characteristics, (c) idealized switching.

The current flow between the MOSFET's output terminals (D and S) is externally controlled by the gate. When v_{GS} is charged to a suitable potential by an external control circuit, a conducting path from the drain to the source is established and the MOSFET is on. In the on-state, the MOSFET is equivalent to a resistance $R_{ds,on}$. This region of operation is therefore called the resistance (or ohmic) region, and occurs when v_{DS} is equal to or less than $v_{GS} - V_{GS,th}$:

$$v_{GS} - V_{GS,th} > v_{DS} > 0 \tag{3.76}$$

---

[1] SiC MOSFET C2M0045170D from Cree Wolfspeed.

The MOSFET is then driven by a large gate-to-source voltage, and in power applications is normally $v_{GS} >> V_{GS,th}$. This results in that the criteria for being in the ohmic region can be simplified to $v_{DS} < v_{GS}$. v_{DS} is equal to the voltage in the on-state, given by:

$$V_{on} = R_{ds,on} I_{on} \tag{3.77}$$

I_{on} is the on-current and is decided by the circuit. The peak and continuous drain current is limited by the MOSFETs physics:

$$-I_{SD} \leq I_{on} \leq I_D \tag{3.78}$$

The body diode conducts the reverse current, and the negative current capability is therefore decided by the body diode.

MOSFETs are enhancement type, meaning that it requires a continuous v_{GS} of appropriate magnitude to conduct current and maintain in the on-state [43]. When v_{GS} falls below the threshold voltage $V_{GS,th}$, the MOSFET blocks the voltage and goes to the off-state, also called the cut-off region. The MOSFET is then an open circuit and must block the applied voltage. The MOSFETs blocking voltage capability is limited by its physics:

$$0 \leq V_{DSS} \leq BV_{DSS} \tag{3.79}$$

where BV_{DSS} is the drain-to-source breakdown voltage. BV_{DSS} must be larger than the applied drain-to-source voltage at all times to avoid avalanche breakdown of the drain-body junction in the MOSFET [9].

In the cut-off operation region, the MOSFET passes a small leakage current:

$$I_{off} = I_{DSS} \neq 0 \tag{3.80}$$

The i-v output characteristics with respect to v_{GS} are shown in figure 3.22 (b), and the respective idealized switching characteristics are shown in (c). The MOSFET with body diode therefore blocks positive voltage and passes both positive and negative current.

Due to a positive temperature coefficient in the on-state, MOSFETs are easily parallel coupled [43]. This is because the device carrying the higher current heats up and get forces to share its current with the parallel MOSFET(s).

Switching characteristics

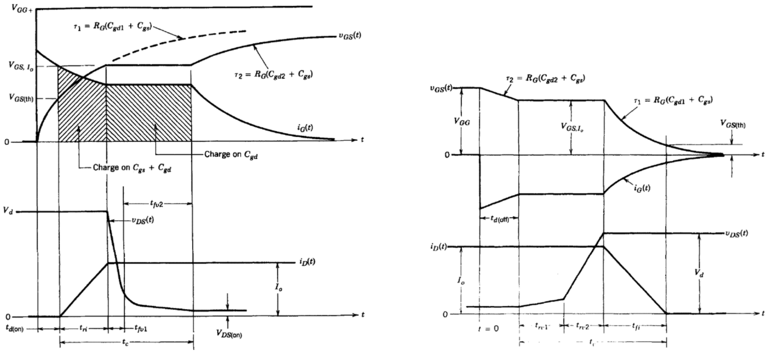
MOSFETs have a fast switching characteristics compared to other switching devices. This is due to that no excess carriers needs to be moved into or out of the device at turn-on and turn-off [9]. It is only the gate capacitances that needs to be charged/discharged at turn-on/turn-off.

The switching performance of the MOSFET is shown in figure 3.25. This is a simplified linearized model of the switching characteristics described in [9]. $t_{d,on}$ is the turn-on delay time where the gate-to-source voltage v_{GS} rises from zero and up to the threshold value $V_{GS,th}$ to obtain conduction through the MOSFET. This rise is exponential. This increase in v_{GS} is due to currents flowing through and charging C_{GS} and C_{GD}. Beyond $V_{GS,th}$, v_{GS} keeps rising and the drain current i_D begins to increase linearly. The drain-to-source voltage v_{DS} is constant equal to the blocking voltage V_{DS} as long as the diode is conducting

($i_D < I_0$). When i_D has built up to carry the full load current I_{on} after the time t_r, v_{DS} starts to decreases to the on-state voltage V_{on}. This decrease in v_{DS} takes a time t_{fv}. v_{GS} is here temporarily clamped at a level to maintain $i_D = I_{on}$. The entire gate current i_G flows through the capacitor C_{GD} in this case. At the beginning of t_{fv}, the MOSFET is still in the active region of operation, but it moves into the ohmic region. At the end of t_{fv}, v_{DS} has obtained a value equal to $V_{on} = R_{ds,on}I_{on}$ and v_{GS} continues to rise to the applied gate voltage while the gate current i_G falls to zero. The MOSFET is fully on.

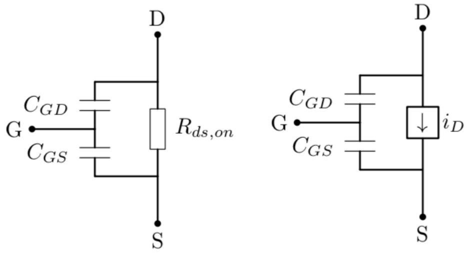
The rise time t_r is the gate charging time to drive the gate through the control range of the gate voltage required for full condition of the device.

This process is reversed at turn-off. $t_{d,off}$ is the turn-off delay time required for the gate to discharge from its overdriven voltage to the threshold voltage. This is called the active region. t_f is the fall time required for the gate voltage to move through the active region before entering cut-off region. The MOSFETs equivalent circuits in the ohmic and in the active and cut-off region shown in figure 3.24 (a) and (b) respectively.



(a) **(b)**

Figure 3.23: Switching characteristics of MOSFET, (a) turn-on, (b) turn-off [9].



(a) **(b)**

Figure 3.24: MOSFET circuit equivalent, (a) in the ohmic region, (b) in the cut-off and active region.

The important specifications of the MOSFET to assess suitability with the power circuit, calculate power losses, and for proper design of the drive circuit are [43]:

- Average and peak current I_D and I_M
- Peak blocking voltage BV_{DSS}
- On-state resistance $R_{ds,on}$
- Off-state current I_{DSS}
- Thermal impedance
- Switching times $t_{d,on}$, t_r, $t_{d,off}$, and t_f
- Threshold voltage $V_{GS,th}$
- Body diode current I_{SD}
- Body diode recovery time t_{rr}
- Input capacitances C_{iss}, C_{oss}, and C_{rss}

Power Losses

In the on-state region, the power dissipation can be kept low by minimizing the voltage drop $V_{DS,on}$, even with a large drain current i_D. The on-state resistance $R_{ds,on}$ increases rapidly with the blocking voltage capability of the MOSFET. However, the technology is developing quickly, and new technologies and materials have significantly improved the efficiency of the device by lowering the on-state resistance over the last years [47]. The power dissipation (conduction loss) in the on-state is given by:

$$P_{cond} = I_{on}^2 R_{ds,on} \tag{3.81}$$

In the off-state, the blocking losses are given by:

$$P_{blocking} = V_{DS} I_{DSS} \tag{3.82}$$

Switching losses are given by:

$$P_{sw} = P_{on} + P_{off} \tag{3.83}$$

where:

$$P_{on} = E_{on}(I) f_{sw} \tag{3.84}$$

$$P_{off} = E_{off}(I) f_{sw} \tag{3.85}$$

The switching takes a time t_{on} and t_{off} for turn-on and turn-off respectively. These switching times are given by [43]:

$$t_{on} = t_{d,on} + t_r \tag{3.86}$$

$$t_{off} = t_{d,off} + t_f \tag{3.87}$$

where $t_{d,on}$ and $t_{d,off}$ are the on and off delay time respectively, t_r is the rise time, and t_f is the fall time.

These losses raise the junction temperature in the MOSFET, and makes the thermal design important in order to limit the operating junction temperature.

3.4.4 Semiconductor Materials and Manufacturers

Silicon (Si) have been the dominant choice of material in power devices. However, the requirements are rising and Si-based power devices are approaching their performance limit due to material characteristics [47].

Recently, research on wide-bandgap (WBG) materials as silicon-carbide (SiC) and gallium-nitride (GaN) has lead to an introduction of new switching devices with reduced losses and higher power density [10]. In WBG materials, the energy required for an electron to go from the valence band to the conduction band is larger than in the conventional Si MOSFET. These materials are therefore superior to its Si based counterpart for switching power devices, offering several key characteristics as: high dielectric strength; high-speed switching; excellent thermal stability; high current density; and low on-resistance [47, 48, 49]. A lower on-resistance improves the efficiency of power switching devices due to reduced conduction and switching losses. Utilizing these materials also decreases the size of the module due to increased power density [49]. The thermal stability enables operation in environments with high temperature.

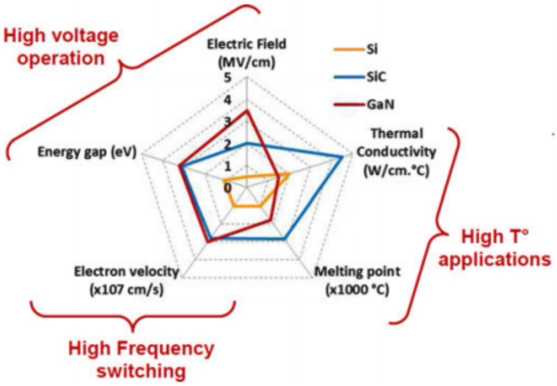


Figure 3.25: Comparison of Si, SiC, and GaN material properties [10].

The market of SiC devices have grown much faster than the market for GaN devices. SiC technology has reached a mature stage, and SiC power devices as the Schottky diode, MOSFETs, JFETs, and BJTs are provided by several manufacturers and in a wide range of blocking voltages. Both the SiC Schottky diode and the SiC MOSFET have already ousted their Si counterparts in high voltage applications. They can also handle higher currents because they can be easily parallel connected due to positive thermal coefficients.

GaN High Electron Mobility Transistors (HEMTs) have shown superior material properties, especially for high frequency applications. The high electron mobility allows operations at higher switching frequencies than SiC. This also decreases the module size because of smaller passive components [49]. Another significant advantage of the GaN HEMT is the absence of a parasitic body diode common to SiC MOSFETs. They have a reverse conduction mechanism similar to the conventional Si MOSFET without any reverse recovery losses. Due to low parasitic capacitances, fast switching, low driving losses, and zero reverse recovery charge, GaN power semiconductors tends to replace Si and SiC devices, especially at higher frequencies [50].

The GaN market is less mature than the SiC market. However, it is rising and several manufacturers are now offering GaN HEMTs. GaN devices for high voltage have become commercially available just recently. Some manufacturers that are offering SiC and GaN devices are discussed here.

Manufacturers

Efficient Power Conversion (EPC) was founded in 2007 with the foresight that GaN would be the inevitable successor to silicon in the advancement of power because of its incomparable speed, efficiency, and low cost. EPC delivered the first commercial enhancement-mode GaN transistor in 2009. Today, they deliver a broad range of GaN transistors in a blocking voltage range of 15-350 V, and they provide single transistors, half-bridges, and drivers. EPC has plans to go to 900V in the future. SiC has better thermal conductivity than GaN at that voltage range, however, GaN has a cost advantage at all voltage levels, and EPC predicts the battle between SiC and GaN to begin at 900 V and move upwards [51].

GaN Systems provides award-winning GaN HEMTs and is the only company with a product portfolio encompassing products in both the 100 V and 650 V range. GaN Systems also provides an enhancement mode GaN on silicon power transistor (GS-065-120-1-D) with a very low on-state resistance (12mΩ) and high voltage and current ratings on 650 V and 120 A respectively.

Cree have an unique position providing both SiC and GaN devices. Having an in-depth knowledge for both processes, they utilize SiC for higher voltages devices, while using GaN for its RF devices. They provide SiC MOSFETS, SiC Schottky diodes, SiC power modules, gate driver boards, different and GaN RF products. Cree provides SiC MOSFETs in the range of 900 V to 1700 V, and SiC Schottky diodes in the range of 600 V to 1700 V.

Rohm Semiconductor provides Si and SiC power devices as Schottky diodes, MOSFETs, and power modules. Their SiC MOSFETs are in the voltage range of 650V to 1700V, while the SiC Schottky diodes comes in the voltage range of 650 V to 1200 V.

Microsemi provides SiC MOSFETs and SiC Schottky diodes in the voltage range of 700 V, 1200 V, and 1700 V. They also provide GaN transistors for RF amplifiers. Infineon provides SiC MOSFETs, SiC Schottky diodes, and different hybrid modules. The SiC MOSFETs comes with a blocking voltage of 1200 V, while the SiC Schottky diodes are provided in the voltage range of 600 V, 650 V, and 1200 V.

UnitedSiC provides different SiC devices as Schottky diodes, JFETs, and cascodes. Their SiC Schottky diodes comes with a blocking voltage of 650 V.

Table A1 and table A2 in Appendix A compares SiC MOSFETs and GaN HEMTs from different manufacturers in terms of voltage and current ratings, and on-state resistance respectively. Table A3 in Appendix A compares SiC Schottky diodes from different manufacturers in terms of voltage and current ratings.

Part III

Method

Chapter 4

Full-Bridge Converter Configurations for Interfacing PV to MMC

This chapter proposes three different isolated full-bridge DC-DC converter configurations for interfacing PV to MMC. The single-unit DC-DC converter configuration must handle high power transfer. By utilizing a series-connection of isolated full-bridge DC-DC converters, the power rating on each full-bridge and the voltage ratings on equipment is reduced. A parallel-connection of isolated full-bridge DC-DC converters lowers the current stress on the switches and reduces the ohmic losses. This chapter examines these different configurations and addresses the power losses and efficiency calculations for the proposed DC-DC converter configurations.

4.1 Introduction

The PV inverter operates at rated conditions only for a few hours per day. Therefore, it's pivotal that the isolated DC-DC converter has a high efficiency from no-load to full-load. High power full-bridge DC-DC converters are suitable topologies for up to a few hundreds of kilo-watts for medium voltage MMC PV Plants [27, 52, 53].

In the MMC PV plant configuration proposed in [2], and shown in figure 2.5, the DC-DC converter must provide isolation and address MPPT. In this study, only unidirectional power transfer from the PV plant to the MMC is considered, and it is therefore not required to have a full-bridge with controllable switches on the secondary side of the HF transformer. A diode bridge rectifier (DBR) is thus chosen on the secondary side of the HR transformer due to lower cost and control requirements when utilizing diodes instead of controllable switches. According to [39, 40], the isolated full-bridge converter is one of the most promising topologies for unidirectional power conversion application with a high power efficiency for a wide input voltage range.

Since the overall efficiency for the PV inverter arrangement is the product of the MMC efficiency and the DC-DC converter efficiency, the choice of converter topology, switching devices, switching frequency, and HF transformer design for the DC-DC converter is essential in order to obtain high efficiency in the MMC PV plant.

4.2 Single DC-DC Converter Configuration

The single-unit DC-DC converter configuration is a straightforward and simple configuration. The power transfer from the PV array to the MMC SM occurs through one isolated full-bridge DC-DC converter. Clearly, this isolated full-bridge DC-DC converter must also be rated for the whole power transfer. This configuration is depicted in figure 4.1.

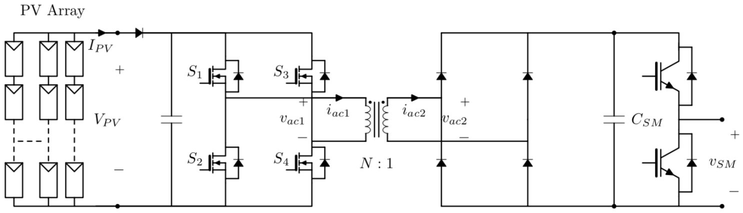


Figure 4.1: Single DC-DC converter configuration.

The most obvious benefit of this configuration is that it only requires one DC-DC converter with one HF transformer, which offers a simple structure. However, the high power transfer requires high current and voltage ratings on the equipment, resulting in high stress and losses in the converter.

4.2.1 Power Switches

Si and SiC power MOSFETs handle high-power and high-voltage transfer, and are suitable switches for this topology. SiC MOSFETs are available with voltage ratings of up to 1700 V, have a much lower on-state resistance, and allow a higher switching frequency than Si MOSFETs, resulting in a higher converter efficiency. However, a parallel-connection of switching devices in the DC-DC converter is necessary in order to handle the high currents. The SiC based isolated DC-DC converter is studied in [54], and the efficiency is shown to be as high as 98.7% when operated at 10 kHz.

4.2.2 The HR Transformer

The HR transformer must handle AC peak-to-peak voltage when assuming a unity transformer voltage ratio (1:1). This limits the switching frequency due to the high-power transfer with a high-sending current. A high-switching frequency and a high-sending current will result in spikes in the energy in the transformer because of the leaking inductance.

When changing the polarity of the current at a high frequency, the stored energy will result in a back EMF increasing the potential substantially, which may also then lead to an isolation failure in the transformer. This configuration must therefore operate at maximum medium-switching frequency in order to reduce losses.

4.2.3 Efficiency and Total losses

The full-bridge converter carries all the power from the PV plant to the MMC SM. The efficiency of this configuration depends on the switching and conduction losses in the switching devices, and on the copper and core losses in the HF transformer. [31] has found that for a 100 kW SiC based full-bridge converter operating at 20 kHz, the switching devices contributes with around 60% of the overall losses.

4.3 Series-Configuration of the High Frequency Isolated Full Bridge DC-DC Converter

Figure 4.2 shows a series-configuration of the high-frequency isolated full-bridge DC-DC converter. The series arrangement consists of a series-connection of k_s full-bridge DC-DC converters connected to each MMC SM. Each full-bridge is interfaced with segmented PV arrays, which are designed assuming an unity voltage ratio in the HF transformer. With this configuration, the voltage stress on the switching device is reduced considerably. A series connection of DC-DC converters results in a lower required voltage rating of each full-bridge. The voltage will be divided over the full-bridges, resulting in a voltage rating equal to:

$$V_{dc-dc} = V_{sm}/k_s \tag{4.1}$$

However, the current handled by each full-bridge will be the same as in the one-unit configuration.

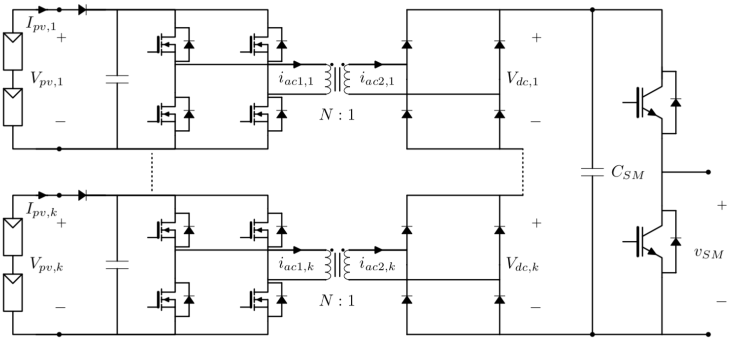


Figure 4.2: Topology of the proposed series-connection of isolated full bridge DC-DC converters.

The PV arrays are designed such that the power carried by each full-bridge P_{dc-dc} is equal to the rated SM power $P_{sm,r}$ divided by the number of series-connected DC-DC converters k_s:

$$P_{dc-dc} = P_{sm,r}/k_s \tag{4.2}$$

This increases also the MPPT with the number of k_s compared to the single converter arrangement.

The main advantage of this configuration is that the bulk transmission of power to the SM is distributed, which increase the overall reliability of the converter.

4.3.1 Power switches

The lower voltage rating of each full-bridge in this configuration allows for use of lower rated switching devices. Since the power transfer in each DC-DC converter is lower, the switching frequency can also be higher. This configuration can therefore utilize the benefits of GaN devices. GaN switching technology has shown superior material properties compared to Si devices, especially for high frequency applications, and are available with voltage rating up to 650 V. The properties of GaN allow for higher switching frequency then what SiC devices do. Due to a higher critical electric field strength, GaN devices are smaller for a given on-state resistance and breakdown voltage [48]. This results in reduced parasitic parameters and a higher possible operating switching frequency. A higher switching frequency results in a lower flux density and reduces the size of the required HF transformer core and the use of copper significantly. However, due to the high currents, a parallel-connection of GaN devices is necessary in order to handle the high currents.

4.3.2 The HF Transformer

For each series-connected full-bridge, one HF transformer is required. The power transfer and voltage rating is in this configuration reduced by k_s. The current however, remains the same as in the one-unit configuration when assuming a unity transformer voltage ratio. The copper windings therefore needs the same design as in the one-unit configurations, but the core can be design for less power transfer.

4.3.3 Efficiency and Total losses

The power transfer from the PV arrays to the MMC SM is divided by k_s full-bridge converters. The efficiency of the whole isolated DC-DC converter configuration is given by the average of the series-connected full-bridges:

$$\eta_{dc-dc} = \frac{1}{k_s} \sum_{i=1}^{k_s} \eta_{dc-dc_i} \tag{4.3}$$

The efficiency is a function of switching frequency f_{sw}, operating power P_{dc} and the output voltage V_{dc}.

4.3.4 Optimal choice of k_s series connected DC-DC converters

The number of series-connected isolated DC-DC converters k_s has to be selected so that the overall efficiency of the system does not decrease significantly. To optimally choose the number of series-connected DC-DC converters, an algorithm can be made. It is based on that the efficiency for the series configuration of k_s DC-DC converters must be higher for the chosen value of k_s than the efficiency for one DC-DC converter carrying all the power at rated conditions:

$$\eta_{dc-dc,k_s} > \eta_{dc-dc} \tag{4.4}$$

where η_{dc-dc,k_s} is the total efficiency of the series configuration, while η_{dc-dc} is the efficiency of the one-unit configuration. This iterative selection is shown in figure 4.3.

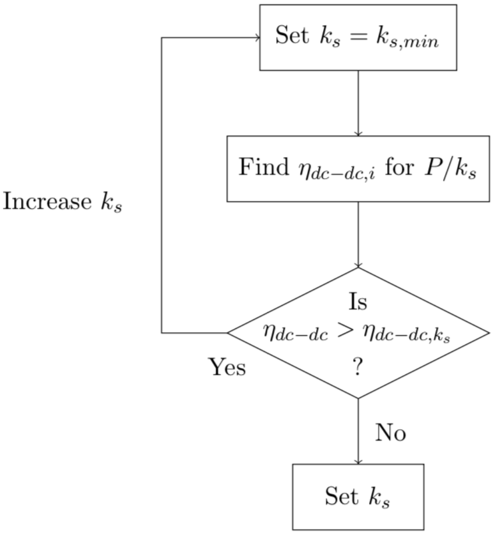

Set $k_s = k_{s,min}$
Find $\eta_{dc-dc,i}$ for P/k_s
Increase k_s
Is $\eta_{dc-dc} > \eta_{dc-dc,k_s}$?
Yes
No
Set k_s

Figure 4.3: Iterative selection of the number of series connected DC-DC converters.

The number k_s also depends on the voltage ratings of the switching devices. GaN devices comes with voltage ratings of 100 V or 650 V. If choosing switches with voltage ratings on 100 V, assuming that only one device is used in series for each switch, and a rated power and voltage at the MMC SM at 100 kW and 1000 V respectively, the minimum number of k_s is 13. This is when assuming that each switch carries 80% of the rated voltage at rated conditions. If utilizing GaN switches with a voltage rating of 650V, the minimum number of k_s is 2.

In this thesis, the number of k_s is set to the minimum value $k_{s,min}$, knowing that a smaller number of series-connected converters is beneficial due to a lower number of switching devices, HF transformers, and a more simple control structure. However, the number needs to be big enough to increase the efficiency of the whole converter arrangement.

4.4 Parallel-Configuration of the High Frequency Isolated Full Bridge DC-DC Converter

Figure 4.4 shows the parallel-configuration of the high-frequency isolated full-bridge DC-DC converter. It consist of a parallel-connection of k_p DC-DC converters connected to the MMC SM. Each DC-DC converter is interfaced with segmented PV arrays. If the PV string operating voltage is not equal to the SM capacitor voltage, then a step-up in voltage is necessary in the HF transformer.

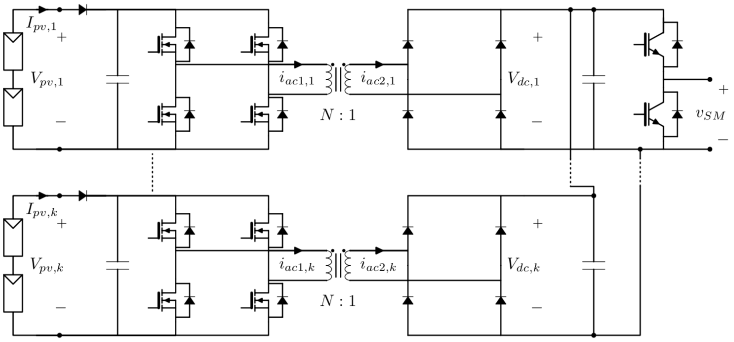


Figure 4.4: Topology of the proposed parallel connection of isolated full bridge DC-DC converters.

The PV arrays are designed so that the power carried by each DC-DC converter unit is equal to the rated power at the SM divided by the number of DC-DC converters in parallel k_p:

$$P_{dc-dc} = P_{sm,r}/k_p \tag{4.5}$$

This increases also the MPPT with the number of k_p compared to the single converter arrangement. Also for this configuration is the main advantage that the bulk transmission of power to the SM is distributed, which increase the overall reliability of the converter.

A unity voltage ratio in the HF transformer results in the same voltage ratings in each full-bridge as in the single DC-DC converter configuration. However, the current is divided by the number of parallel-connected full-bridges:

$$I_{dc-dc} = I_{sm,r}/k_p \tag{4.6}$$

This reduces the ohmic loss in the isolated converter. The ohmic loss is dependent on the square of the current, and a reduction in the current in each full-bridge will therefore reduce the overall ohmic loss. Lets say if the current in each full-bridge is halved compared to the one-unit configuration, the total ohmic loss is also halved for the whole isolated DC-DC converter due to the square relationship.

4.4.1 Power switches and the HF Transformer

Due to the reduced sending current in each full-bridge, the parallel-arrangement of converters avoids the parallel-connection of switching devices in each full-bridge in order to handle the high currents. The total number of switching devices are therefore reduced in this configuration compared to the series-connected converter configuration.

At a unity voltage ratio, the power switches must be rated for the SM voltage, and SiC MOSFETs are therefore the natural choice for this configuration. If utilizing a 1:2 voltage ratio however, the voltage rating on the full-bridge switches only needs to be half, and GaN devices can be utilized.

4.4.2 Efficiency

The efficiency of the parallel-connected DC-DC arrangement is calculated in the same manner as the series-connected arrangement:

$$\eta_{dc-dc} = \frac{1}{k_p}\sum_{i=1}^{k_p} \eta_{dc-dc_i} \tag{4.7}$$

Where k_p is the number of DC-DC converters connected in parallel.

4.4.3 Optimal choice of $\mathrm{k_p}$ parallel-connected DC-DC converters

In the same manner as for the series connected configuration, the number of parallel connected isolated DC-DC converters k_p has to be selected so that the overall efficiency of the system does not decrease significantly. k_p can therefore be selected as depicted in figure 4.3.

The number of k_p is in this thesis set to the same value as k_s in order to compare the different DC-DC converter configurations in terms of component and ratings.

4.5 Comparison

Table 4.1 compares the one-unit arrangement, the series-arrangement, and the parallel-arrangement in terms of MPPT, and power, voltage, and current ratings. The one-unit arrangement is chosen as the base value. This depicts that with a distributed arrangement of the power from the PV to the MMC SM, the MPPT efficiency increases significantly. For the series and parallel configuration the MPPT increases with k_s and k_p respectively. However, the MPPT is already significantly increased compared to the CI arrangement presented in figure 1.3 (a) by utilizing MMC as the inverter.

The number of switching devices in each configuration depends on the choice of k_s and k_p, and the choice of switching technology. However, reducing the current rating as in the parallel configuration, requires less switching devices and also results in lower ohmic losses. With a lower voltage rating for each full-bridge, as in the series configuration, new switching technology as GaN devices with improved switching characteristics for high frequency applications can be utilized.

4.6 Configurations chosen for a further analysis

For the single DC-DC converter configuration, 1200V SiC MOSFETs are utilized.

Table 4.1: Comparison of the different DC-DC converter configurations.

DC-DC configuration	*MPPT*	*Power rating*	*Voltage rating*	*Current rating*
Single-unit converter	1	1 p.u.	1 p.u.	1 p.u.
Series-connected converters	k_s	1/k_s p.u.	1/k_s p.u.	1 p.u.
Parallel-connected converters	k_p	1/1/k_p p.u.	1 p.u.	1/k_p p.u.

For the series-configuration, the chosen power switch is a 650 V GaN HEMT. The minimum number of series connected devices is chosen out from this voltage rating. Since the SM is rated for 1000 V, the number of series-connected isolated DC-DC converters k_s is chosen to be two.

To compare the series-arrangement and the parallel-arrangement, this is also the number chosen for k_p.

Chapter 5

PV Plant Configuration

The PV arrays making up the 3 MW scale grid-connected PV MMC power plant considered in this thesis are in this chapter modelled for the three different converter configurations presented in chapter 4. The PV arrays need to meet the power and voltage requirements for each of the configuration.

5.1 Introduction

Each DC-DC converter is connected to one MMC SM, which is rated for 100 kW. The PV arrays are either designed for 100 kW or 50 kW depending on the isolated DC-DC converter configuration. The required string voltage is also different for the different configurations.

By an appropriate interconnection between the PV modules in the PV array, the energy yield of the PV plant can be improved [2].

5.2 The PV Module

The PV modules used in the evaluated PV plant are Titan S6-60 series, mono-crystalline panels from Titan Energy Systems Ltd with a maximum power of 235 Wp. Table 5.1 tabulates the PV module electrical characteristics at Standard Test Conditions (STC), which is at a irradiation level of $G = 1000W/m^2$ with an AM1.5 spectrum at 25 °C [55].

Figure 5.1 depicts the I-V curve and the power available from the PV module at different irradiance levels. This figure is obtained from simulations in SIMULINK. It also shows the maximum power point (MPP) of the PV module, which is the operating point where the maximum power is provided at a given irradiance and temperature. This

Table 5.1: PV module Titan S6-60 series electrical characteristics [3].

Parameter	*Symbol*	*Values*
Maximum power	P_{mp}	235 W
Maximum power voltage	V_{mp}	29.43 V
Maximum power current	I_{mp}	8 V
Cells per module	N_{cell}	60
Open Circuit Voltage	V_{oc}	37.5 V
Short Circuit Current	I_{sc}	8.52 A
Operating Temperature	T_{module}	$-40\,°\mathrm{C} \sim 85\,°\mathrm{C}$
Maximum System Voltage	$V_{s,max}$	1000 V

occurs at:

$$P_{mp} = V_{mp} * I_{mp} \tag{5.1}$$

The maximum power is also termed the nominal power of the PV module and given with the unit watt-peak (Wp).

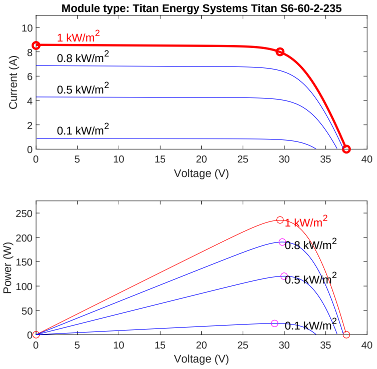


Figure 5.1: I-V curve, available power and maximum power point for the Titan S6-60 series PV module at different irradiance levels at 25 °C.

5.3 PV Array Design for the different converter topologies

The different DC-DC converter configurations requires different ratings for the PV array. The MMC SM is rated for 100 kW and 1000 V. The PV arrays are modelled with PV panels in series to obtain the rated voltage and strings are added in parallel in order to reach the required power rating. The PV arrays are designed for a unity voltage ratio in the HF transformer.

Table 5.2 tabulates the required power and voltage ratings for each PV array in the different DC-DC converter configurations. The required number of PV panels in each

Table 5.2: Required PV array ratings for the different DC-DC converter configurations.

MMC DC-DC configuration	*Required power P_r*	*Required voltage V_r*
Single-unit converter	100 kW	1000 V
Two series-connected converters	50 kW	500 V
Two parallel-connected converters	50 kW	1000 V

array to meet the required power rating is found by:

$$N_{total} = \frac{P_r}{P_{mp}} \tag{5.2}$$

This number is rounded up to the nearest whole number. The number of required series-connected PV panels in order to obtain the required string voltage can be found from:

$$N_s = \frac{V_r}{V_{mp}} \tag{5.3}$$

This number is rounded up and selected as the number of series-connected PV panels. The actual string voltage at rated conditions can then be found from:

$$V_{s,r} = N_s * V_{mp} \tag{5.4}$$

The actual power produced by one string P_s of N_s PV modules is equal to the number of series connected modules multiplied with the maximum power:

$$P_s = N_s * P_{mp} \tag{5.5}$$

N_s The number of required parallel-connected PV strings required to meet the power rating is then found from:

$$N_p = \frac{P_r}{P_s} \tag{5.6}$$

where P_r is the required PV array power, and P_s is the power produced by one string. The number of N_p is rounded up and chosen as the number of parallel connected PV strings with N_s modules in series. The peak power from the PV array is obtained by multiplying the PV module peak power with the total number of PV modules in the PV array:

$$P_{pv,peak} = P_{mp} * N_s * N_p \tag{5.7}$$

The current produced by the PV array is found from:

$$I_{pv} = N_p * I_{mp} \tag{5.8}$$

Table 5.3 summarizes the configuration of the PV array for the different DC-DC converter configurations, while table 5.4 gives the resulting power, voltage, and current for the different PV array configurations at peak power. According to [56], the performance is generally increased by reducing the number of modules in series and by increasing the number of those in parallel. It is seen from table 5.3 that the series-connected converter

Table 5.3: PV array configuration for the different MMC DC-DC converter configurations

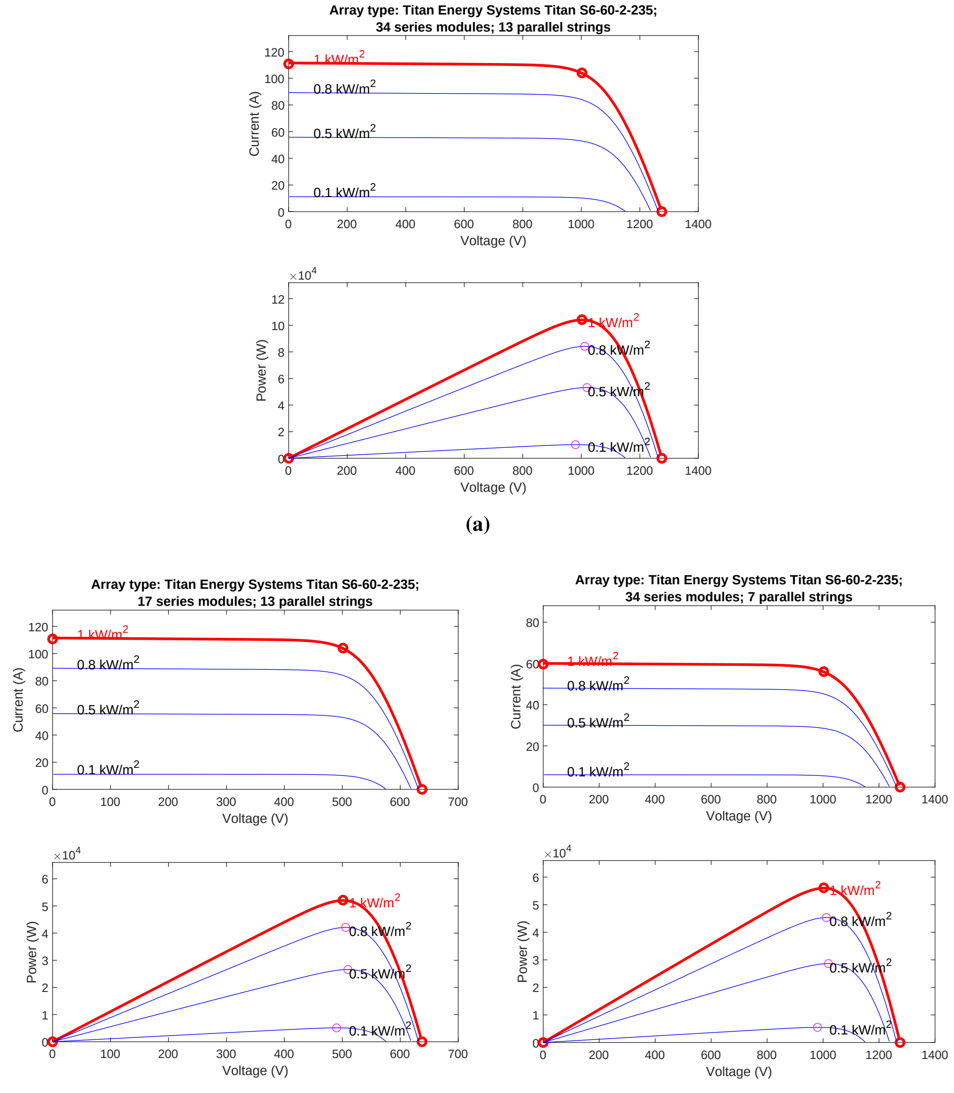
MMC DC-DC configuration	*Parameter*	*Value*
Single-unit converter	Number of PV modules in series	34
	Number of PV modules in parallel	13
Two series-connected converters	Number of PV modules in series	17
	Number of PV modules in parallel	13
Two parallel-connected converters	Number of PV modules in series	34
	Number of PV modules in parallel	7

Table 5.4: Power, voltage, and current for the different PV array configurations at peak power.

MMC DC-DC configuration	*Power* P_{pv}	*Voltage* V_{pv}	*Current* I_{pv}
Single-unit converter	103 870 W	1000.62 V	104 A
Two series-connected converters	51 935 W	500.31 V	104 A
Two parallel-connected converters	55 930 W	1000.62 V	56 A

configuration has the lowest number of series-connected PV modules, and the highest number of parallel-connected PV modules.

Figure 5.2 shows the I-V curves and the available power at the different PV arrays at different irradiance levels. These are found by simulations in SIMULINK for the chosen PV module.



(a)

(b)

(c)

Figure 5.2: I-V curve and the available power at different irradiance levels at 25 °C for the PV array design for (a) the single-unit DC-DC converter configuration, (b) the series-connected DC-DC converter configuration, and (c) the parallel-connected DC-DC converter configuration.

Part IV

Results, Discussion and Conclusion

Chapter 6

Annual Energy Yield and Efficiency Comparison

This chapter presents the annual energy yield and annual losses for different PV inverter topologies. Simulations are performed in order to find the efficiency of the different isolated DC-DC configurations for the MMC PV plant discussed in chapter 4. The results are presented in this chapter.

The different isolated full-bridge DC-DC configurations for the MMC PV plant discussed in chapter 4 are considered for further evaluation. Two classical PV plant arrangements, the central inverter (CI) configuration and the multi-string central inverter (MSCI) configuration, shown in figure 1.3 (a) and (b) respectively, are also considered for performance comparison to the different MMC PV plant configurations.

This chapter first presents the performance models of the different components in the PV plant configurations in order to find the annual energy yield. Section 6.2.7 presents the simulation model made in PLECS®in order to find the efficiency of the different DC-DC converter configurations presented in chapter 4. The results are also discussed. The last section compares the annual energy yield and the efficiency of all the different PV plant configurations considered.

6.1 Description of the Evaluation Models

The performance model regarding the annual energy yield for the PV plant is set up as shown in figure 6.1. It is the same model as used in [2] for the CI and MSCI configurations, while it is modified for the MMC configuration in order to capture the annual energy yield for the different isolated full-bridge DC-DC converter configurations presented in 4. This evaluation model is built using Simulink®.

The cable losses are not more than 1% of the total power capacity of the PV plant [4],

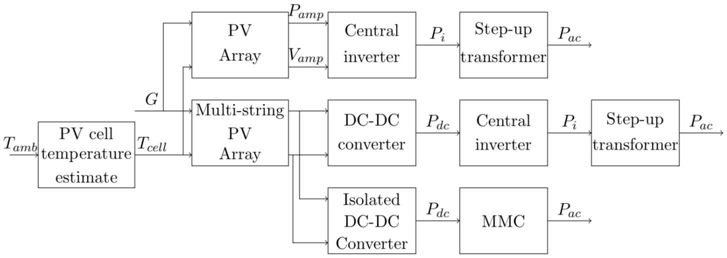

P_{amp}
V_{amp}
PV Array
Central inverter
P_i
Step-up transformer
P_{ac}
G
T_{amb}
PV cell temperature estimate
T_{cell}
Multi-string PV Array
DC-DC converter
P_{dc}
Central inverter
P_i
Step-up transformer
P_{ac}
Isolated DC-DC Converter
P_{dc}
MMC
P_{ac}

Figure 6.1: Block representation of performance model with temperature estimation of PV cells [2].

and they are therefore neglected and not considered in this performance model.

6.1.1 PV Array Performance Model

The power production at the PV plant varies with irradiance, temperature and wind speed. These are stochastic data with strong function to the geographic location and season. The weather data is obtained from [57] for the location of the PV plant and is the same as used in [2]. The same set of weather data for the PV plant is used to evaluate the annual energy production for all the different PV plant inverter topologies. The PV module temperature is estimated as per [58] based on the ambient temperature data, irradiance profile, and the average wind speed.

In order to find the maximum power obtained from the PV array, [2] has used a look-up table approach. The PV module operating point at maximum power, as a function of irradiance G and temperature T, is found as a surface fitted second order polynomial:

$$f(G,T) = a_0 + a_1 G + a_2 G^2 + a_3 T + a_4 T^2 + a_5 GT \tag{6.1}$$

with coefficients as listed in table 6.1. This guarantees that the same data accuracy is used in all the different PV plant configurations for variation in irradiance and temperature.

Table 6.1: Coefficients of the polynomial in equation 6.1 for P_{mp} and V_{mp} respectively [2].

f(G,T)	a_0	a_1	a_2	a_3	a_4	a_5
P_{mp}	98.08	56.27	-0.9347	-12.91	-0.0142	-7.256
P_{mp}	24.66	0.3922	-0.4573	-3.142	-0.0232	-0.00960

The output from this performance model is then the net maximum power of the PV array P_{amp} and the respective voltage V_{amp}:

$$\begin{aligned} P_{amp} &= \sum_{j=1}^{N_p} \sum_{i=1}^{N_s} P_{mp,ij}(G,T) \\ V_{amp} &= \sum_{i=1}^{N_s} V_{mp,ij}(G,T) \end{aligned} \tag{6.2}$$

This gives an accurate prediction of the PV output data for various configurations of PV arrays, since they are directly obtained from look-up tables. However, it only regards non-partial shaded conditions.

6.1.2 Central Inverter and Multi-String Inverter Configurations

The central inverter performance model is identical for the CI and MSCI configuration. The additional DC-DC converters in the MSCI is the only difference.

The PV array output fed to the central inverter configuration is a 250 kW PV array configuration with 24 PV modules in series and 45 PV strings in parallel [1]. Four 250 kW central inverters are connected to one 1.25 MVA step-up transformer, and three such configurations makes up the 3 MW scale PV power plant.

The MSCI configuration is designed with the same power ratings. The PV array is designed with 27 PV modules in series obtaining a 12.5 kW PV array that is connected to each DC-DC converter. These DC-DC converters are assumed to have an efficiency in the range of 99% even at low partial loads [2].The MSCI consists of 240 such arrangements in order to produce 3 MVA.

The inverter and MPPT efficiencies are modelled using two-dimensional look-up tables. The central inverter from Advanced Energy Industries (AE 250NX), which has a CEC efficiency of 97.5%, is used in this evaluation model [2].

Transformer efficiency

Both the CI and the MSCI configuration utilizes step-up transformers in the connection the the power grid. [4] has defined a non-linear function for transformer power losses as a function of total apparent power loading S at a time t and nominal apparent power S_N:

$$P_{tr,loss} = k_{tr} P_{fe} + \frac{P_{cu}}{k_t r}\left(\frac{S(t)}{S_N}\right)^2 \tag{6.3}$$

where:

$$\begin{aligned} P_{fe} &= n * S_N + p \\ P_{cu} &= a * S_N^2 + b * S_N \end{aligned} \tag{6.4}$$

Coefficients for equation 6.4 are given in table 6.2 for two different transformers.

Table 6.2: Coefficients of the core and copper loss equations given in equation 6.4 [4].

f(G,T)	n	p	a	b
Class A	$1.14 * 10^{-3}$	0.3014	$-11.31 * 10^{-7}$	$1.044 * 10^{-2}$
Class B	$1.285 * 10^{-3}$	0.3811	$-9.893 * 10^{-7}$	$1.176 * 10^{-2}$

6.1.3 MMC Performance Model

The MMC operates at a fixed DC link voltage and has a flat efficiency cure. [2] has found the lowest efficiency of the MMC to be 95%. In these simulations however, it is assumed a 99% efficiency of the MMC when operating as an inverter.

The next section describes the performance models for the different full-bridge isolated DC-DC converter configurations for the MMC PV plant.

6.2 Isolated DC-DC Converter Performance Models

In order to model the efficiency for the different isolated full-bridge DC-DC converter configurations presented in chapter 4, performance models are built in PLECS®simulation software.

Efficiency is obtained at different DC link voltages, evaluated over a wide frequency range, and performed both with and without ripple from the MMC. In order to obtain the worst-case and best-case energy yield, simulations are performed for the entire operation range of 0.1 to 1 per unit power.

The conversion efficiency is found by measuring the power at the DC input and DC output terminals:

$$\eta = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{out} + P_{loss}} \tag{6.5}$$

The results obtained from these simulations are then extrapolated to obtain the efficiency at all power points, put in two-dimensional look-up tables, and used in the evaluation model to obtain the annual extracted energy and the annual energy yield for the different DC-DC converter configurations for the MMC PV plant topology.

A simple control system is used to control the output voltage of the DC-DC converter. Unipolar PWM is utilized to control the switches, and the sinusoidal reference voltage is obtained from comparing the actual output voltage with the desired value. One subtracted by the per unit value of this error is then multiplied with the sinusoidal reference wave in order to control the output voltage waveform. Figure 6.2 depicts this simple control structure.

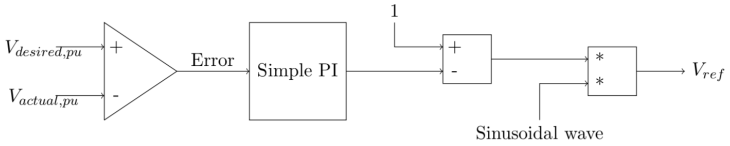


Figure 6.2: Simple control structure of DC-DC converter.

To get the best loss evaluation from this model, the sampling time during transition is high. This results in a high running time for each simulation, especially when increasing the switching frequency.

6.2.1 PV Array

The PV array is modelled as a controlled current source. The current is determined from the voltage produced at the PV array at different irradiance levels and the power output as follows:

$$I_{pv} = \frac{P_{pv}}{V_{pv}} \tag{6.6}$$

where V_{pv} is the voltage produced at the PV array, and varies with irradiation. Three different irradiance profiles are looked at; 800 W/m^2 which is at NMOT, 1000 W/m^2 which is at STC, and 100 W/m^2. This gives voltage values of 1 per unit (p.u.), 1.1 p.u., and 0.8 p.u. respectively. P_{pv} depends on the different configurations as stated earlier. The power, voltage and current ratings of the different DC-DC converter configurations were tabulates in 5.4.

6.2.2 MMC Model

The MMC operates at fixed DC link voltage and fixed SM voltage. As mentioned in chapter 2, the MMC SM can be modelled as a controllable voltage source. In this performance model, it is both modelled as a constant voltage source, and as a controlled voltage source from a look-up table with 10% ripple. It is assumed that each SM can handle 100 kW and has a fixed voltage of 1000 V. This results in a maximum SM voltage at 1100 V in the simulations where it is modelled with ripple, this voltage curve is shown in figure 6.3.

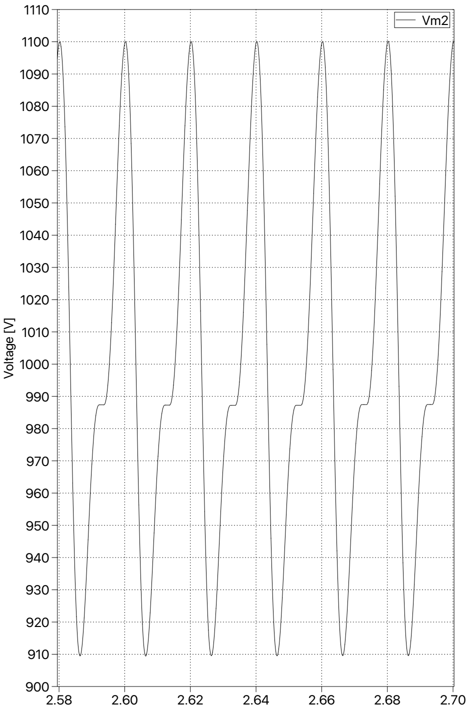


Figure 6.3: MMC SM voltage with 10%ripple from simulations.

However, the efficiency of the DC-DC converters did not vary much when applying ripple on the MMC SM voltage compared to when it was modelled as a the constant voltage source. Due to the longer simulation time when utilizing the controllable voltage MMC source with ripple, the results presented later in this chapter is considering the MMC as a constant voltage source equal to 1000 V.

6.2.3 Switching Devices Performance Models

The switching devices utilized in the performance model for the full-bridge DC-DC converter configurations are the same for the one unit DC-DC converter configuration and the configuration with a parallel-connection of DC-DC converters with an unity transformer ratio. This is due to the same voltage ratings. It is only the number of devices connected in parallel that varies due to different current requirements.

For the series-connection of full-bridge DC-DC converters, the GaN HEMT is utilized due to the lower voltage ratings and better performance at higher switching frequency.

As stated in chapter 4, a diode bridge rectifier (DBR) is chosen on the secondary side of the HF transformer due to the unidirectional power transfer. However, the number of diodes connected in parallel varies for the different configurations due to different current ratings.

Diode Bridge Rectifier Performance Model

The device chosen is a 1200 V, 30 A SiC Schottky diode from Cree Wolfspeed (C4D30120D). It is chosen due to a high voltage rating and a low on-state resistance $R_{dc,on}$. This is found from the provided datasheet and calculated as follows at 25 °C:

$$R_{dc,on} = \frac{V_2 - V_1}{I_2 - I_1} = \frac{2.25 - 1.5}{30 - 12.5}\Omega = 0.043\,\Omega \tag{6.7}$$

The datasheet can be found in appendix A.3, together with a comparison of different diodes A.3.

A PLECS model for this diode is given by the manufacturer, and figure 6.4 depicts the conduction losses in terms of the on-state voltage and on-state current. These diodes are used in DBR for all the different full-bridge DC-DC configurations considered.

SiC MOSFET Performance Model

A comparison of different MOSFET devices can be found in appendix A.1. The switching device considered is a 1200 V, 90 A SiC MOSFET from Cree Wolfspeed (C2M0025120D). The on-resistance at 25 °C is 25 mΩ. A PLECS model is given by the manufacturer, and the turn-on, turn-off, and conduction losses are provided in figure 6.5 (a), (b), and (c), respectively. The datasheet for this MOSFET is also provided in appendix A.1.

This MOSFET is chosen due to the lowest R_{on} value, which gives the lowest conduction losses. This MOSFET comes with an anti-parallel body diode, like most MOSFETs, and this diode is included in the model even though no current flows through it in these simulations.

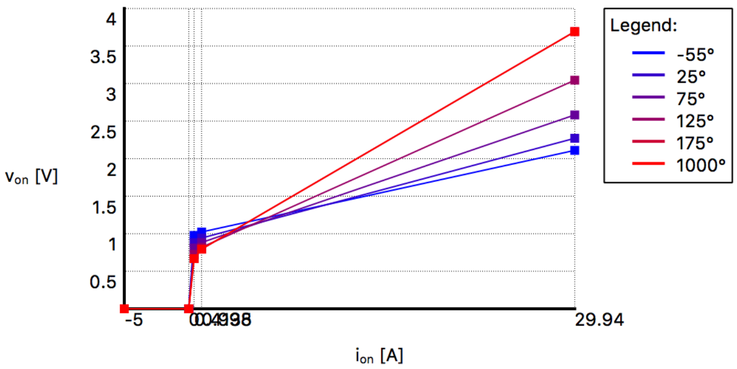
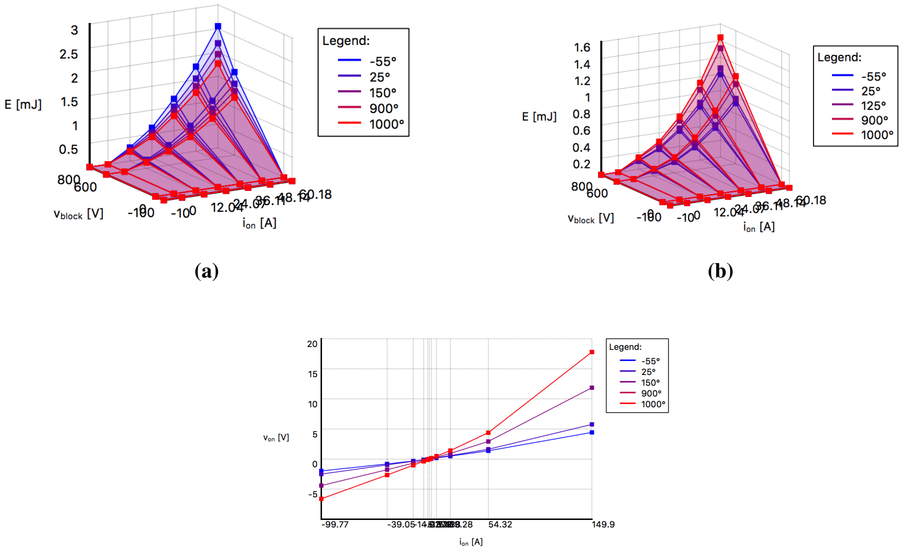


Figure 6.4: Conduction losses provided by the manufacturer.



(a)

(b)

(c)

Figure 6.5: SiC MOSFET from Cree Wolfspeed (C2M0025120D), (a) turn-on losses, (b) turn-off losses, and (c) conduction losses.

GaN HEMT Performance Model

A comparison of different GaN devices can be found in appendix A.2. The 650 V/15 A GaN HEMT (GS66504B) from GaN Systems is chosen as the switching device for the series-connected DC-DC configuration. It has a $R_{dc,on}$ equal to $100\,\mathrm{m}\Omega$. The performance model is built in PLECS from the obtained datasheet, provided here in appendix A.2. However, the turn-on and turn-off losses are not given in the datasheet and are obtained from [11]. Figure 6.6 depicts the turn-on and turn-off losses for this device given by [11].

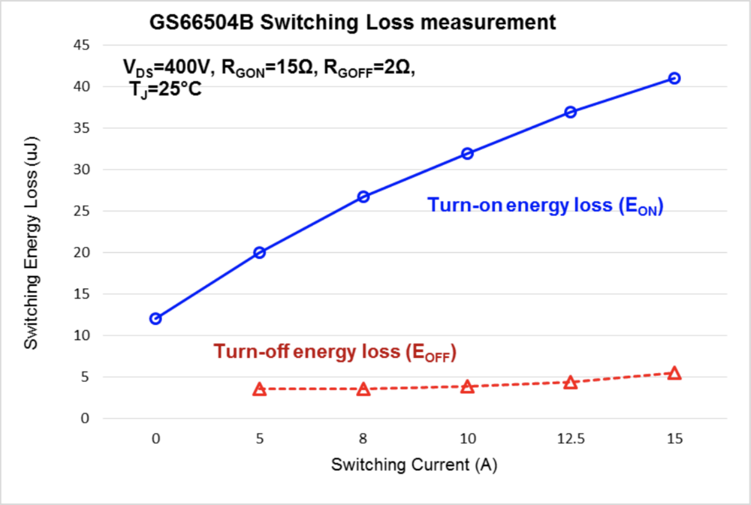


Figure 6.6: Switching losses for the GaN HEMT GS66504B from GaN Systems [11].

The resulting thermal model of the turn-on, turn-off, and conduction losses is depicted in figure 6.7 (a)-(c), respectively.

6.2.4 HF Transformer Performance model

The design of the transformer is beyond the scope of this thesis, and losses in the HF transformer are not included in this simulation model. The transformer is therefore assumed ideal in these simulations. However, when comparing the different topologies in terms of efficiency, extracted energy and LCOE, the losses in the HF transformer are discussed as well. Higher frequency is beneficial in terms of reduced size of the transformer core and reduced use of copper. However, a higher frequency also results in higher magnetic effects, as the proximity effect and the skin-effect explained in chapter 3.

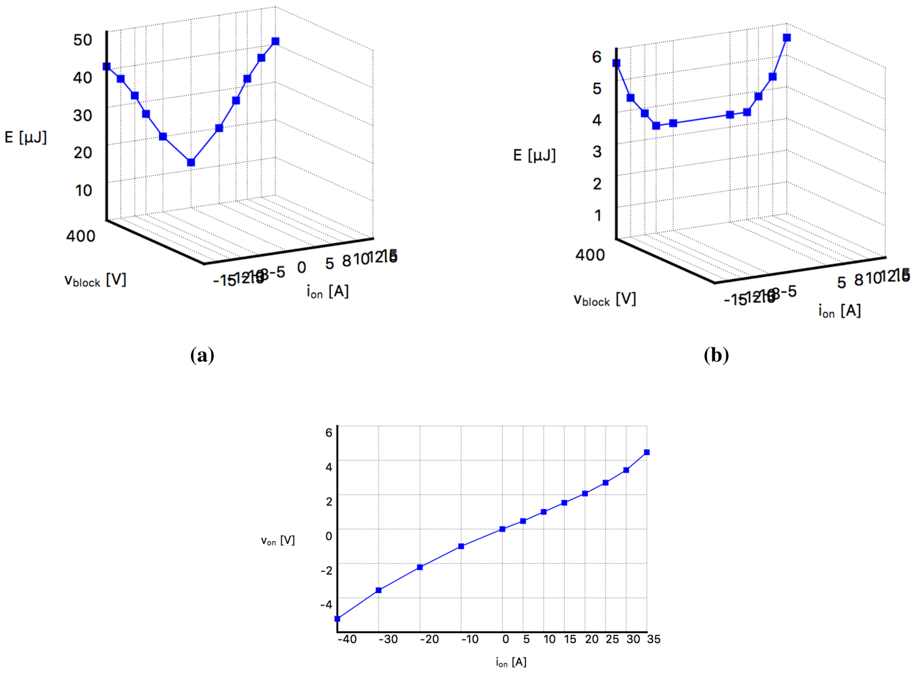
A configuration with lower AC current through the HF transformer is beneficial due to lower ohmic losses. The copper loss contributes to the biggest part of the losses in the HF transformer, and they are proportional with the square of the AC RMS current:

$$P_{dc} = I_{rms}^2 R_{dc} \tag{6.8}$$

R_{dc} can directly be calculated from equation 3.44 when knowing the transformer core and winding geometry. R_{ac} can be obtained from equation 3.48 to account for proximity and skin effects in the HF transformer.

[54] has found that the losses in the magnetic devices contributes with around 30% of the total losses in a 100 kW isolated full-bridge DC-DC converter when operating 20 kHz.

It is left to the reader to add the HF transformer losses when choosing and designing a proper HF transformer for the isolated DC-DC converter. The core loss is normally provided by the manufacturer and can be easily added.



(a)

(b)

(c)

Figure 6.7: GaN HEMT GS66504B from GaN Systems, (a) turn-on losses, (b) turn-off losses, and (c) conduction losses.

A method to design the HF transformer is given in section 3.3.8 and the parameters are given in table 6.3. The skin depth at different frequencies is shown in appendix B in order to obtain the R_{ac} resistance in equation 3.48.

The choice of copper windings are decided from the RMS current through the windings and the maximum allowable current density. The copper cross-sectional area can be found from equation 3.59. However, simulations shows a RMS current up to 200 A for the single-unit DC-DC converter configuration. This means that a 80 mm^2 copper wire is needed to carry the current. This is a huge dimension for a copper wire, and it might then be a better solution to chose a smaller copper wire that only conducts parts of the current, and utilize multiple wires. This also makes it easier to wind the wires around the

Table 6.3: Parameters for Transformer Design.

Parameter	*Symbol*	*Value*
Maximum peak flux density	B_m	0.4 T
Maximum current density in copper wires	J_{cu}	2.5 A/mm^2
Copper fill factor	α_{cu}	0.4

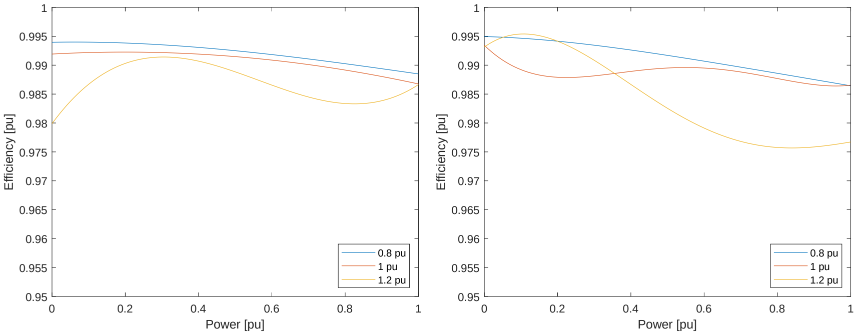
transformer core. The selected copper wires must fit in the selected core area window.

6.2.5 Single DC-DC Converter Configuration

The single-unit DC-DC converter configuration in rated for 100 kW, 1000 V and consists of eight 1.2 kV/400 A SiC MOSFETs. Two and two MOSFETs are connected in parallel in order to handle the high sending current from the PV array. On the secondary side of the HF transformer four diodes are connected in parallel for each switch, resulting in a total number of 16 diodes in the DBR.

The one unit DC-DC converter is simulated over a wide range of frequencies. SiC MOSFETs can operate up to 50 kHz in switching frequency, but the losses increases due to capacitive elements in the converter and a high sending current.

For a switching frequency of 1 kHz, the single-unit configuration has high power efficiency in the 99% range for different voltage profiles over the whole operation range, as shown in figure 6.8 (a). However, at 1.2 p.u. volts, the efficiency goes slightly down. It varies more in the figure due to the extrapolating. Increasing the switching frequency, results in increased losses. This is depicted in figure 6.9 where efficiency curves for a switching frequency of 1 kHz, 10 kHz, and 20 kHz is presented at 1 p.u. voltage, and in figure 6.8 (b) where the efficiency at a switching of 20 kHz is presented.



(a) (b)

Figure 6.8: Efficiency of the single-unit DC-DC converter configuration at different DC link voltage at (a) 1 kHz switching, and (b) 20 kHz switching.

6.2.6 Parallel-Connected SiC-Based DC-DC Converter Configuration

When utilizing a parallel-connection of two SiC based DC-DC converters, the power rating on each full-bridge is half of the single-unit DC-DC converter configuration. With an unity transformer ratio, the voltage rating is the same. The current, however, is halved compared to the one-unit configuration. This configuration therefore avoids the parallel connection of MOSFETs due to the lower current rating.

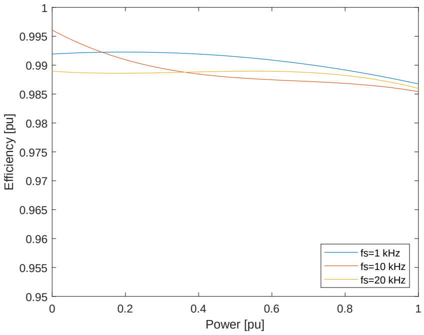
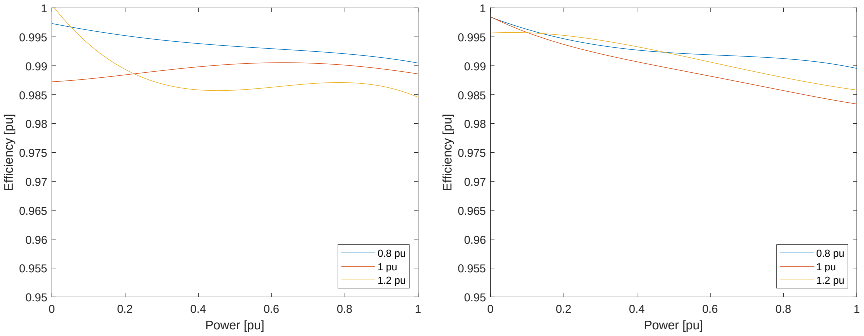


Figure 6.9: Efficiency curves for the single-unit DC-DC converter configuration at 1 kHz, 10 kHz, and 20 kHz switching frequency.

Figure 6.10 depicts the efficiency curves at different DC link voltage for a switching frequency of 1 kHz and 10 kHz. It is seen that the efficiency is above 98% for the whole operating range.



(a) **(b)**

Figure 6.10: Efficiency of the parallel-connected DC-DC converter configuration at different DC link voltage and (a) 1 kHz switching, and (b) 10 kHz switching.

When utilizing a parallel connection of two DC-DC converters rated for only half the power transfer, the current through each HF transformer goes down. A 50% reduction in the current though each HF transformer results in a 50% reduction in the total copper losses. The copper losses are proportional to the square current, and by reducing the current by 50%, the total copper losses is reduced by 50%. This solution also increases the MPPT compared to the single-unit DC-DC configuration.

6.2.7 Series-Connected GaN-Based DC-DC Converter Configuration

In series-connected GaN-based DC-DC converter configuration is each full-bridge rated for 50 kW and 500 V. Utilizing GaN HEMTs instead of SiC devices increases the switching frequency range of the converter. GaN Systems enhancement mode HEMTs do not need an intrinsic body diode and there is therefore zero reverse recovery charge. The devices are naturally capable of reverse conduction and exhibit different characteristics depending on the gate voltage. This converter arrangement requires the same current ratings as in the single-unit configuration, and a parallel connection of eight 650 V/15 A GaN HEMTs is necessary in order to obtain the high current rating. Four diodes are connected in parallel in each of the DBRs, resulting in a total number of 32 diodes in total.

Due to a very long simulation time for high frequency, the losses for this configuration is estimated based on the information given in the datasheet and from figure 6.6 for the GaN HEMT. The conduction losses from the DBR utilizing SiC diodes are also estimated from the datasheet. The turn-on and turn-off losses are given by:

$$P_{on} = E_{on}(I_{ds})f_{sw} \tag{6.9}$$

$$P_{off} = E_{off}(I_{ds})f_{sw} \tag{6.10}$$

The estimated switching loss is then equal to:

$$P_{sw,est} = P_{on} + P_{off} = E_{on}(I_{ds})f_{sw} + E_{off}(I_{ds})f_{sw} \tag{6.11}$$

The conduction loss is dependent on the on-current, on-voltage and the duty ratio and can be found from:

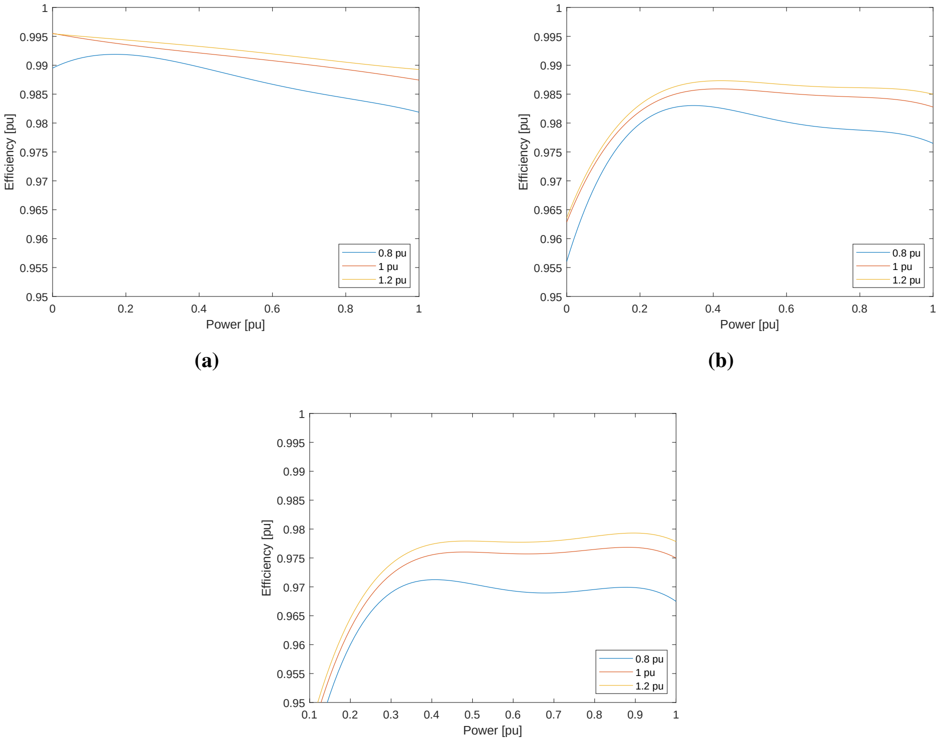
$$P_{cond,est} = I_{ds}V_{ds} * d \tag{6.12}$$

Where d is the duty ratio. Since the switches will not conduct all the time, the duty ratio plays an important role regarding conduction losses. The duty ratio will vary from 0.1 to 0.9 with PWM switching, but on an average it can be assumed to be 0.5. For a duty ratio of 0.5, the inductor current will go up to maximum and fall down to zero for each switching cycle. This is assumed to be the worst case duty ratio and gives the maximum loss anticipated from conduction.

Figure 6.11 (a)-(c) presents the estimated efficiency curves for the whole operating range at different voltages at a switching frequency of 20 kHz, 200 kHz, and 500 kHz, respectively. From these results, it is seen that when utilizing a series connection of two GaN based DC-DC converters rated for only half the power transfer and half the voltage, the operating switching frequency can be increased up to 200 kHz without increasing the losses in the DC-DC converter significantly. At 200 kHz, the converter efficiency is still in a 98% range, not regarding the losses in the HF transformer. At 500 kHz switching however, the losses have increased and the efficiency has fallen below 98%. This is due to the superior GaN characteristics at high frequency. This is beneficial due to a reduced size of the transformer core. The main contribution to the losses at 20 kHz switching is the loss in the DBR.

6.3 Annual Energy Yield and Efficiency Comparison

The efficiency of the isolated DC-DC converter configurations found from the PLECS models are multiplied with the MPPT efficiency to get to total efficiency of the isolated DC-DC converter. This efficiency is again multiplied with the MMC efficiency to get the



(a) (b)

(c)

Figure 6.11: Estimated efficiency of the two series-connected GaN-based DC-DC converter configuration at different DC link voltage and (a) 20 kHz switching, (b) 200 kHz switching, and (c) 500 kHz switching.

total inverter efficiency of the PV plant. The net efficiency of the inverter is multiplied with the maximum power available at the PV plant to get the extracted power. To obtain the annual energy yield, this power is integrated over one year:

$$P_{annual} = \int_{0}^{1year} P_{extracted} \tag{6.13}$$

PV inverters are normally underrated due to that the maximum power extracted from the PV plant only occurs at few hours a day. The maximum and minimum voltage for MPPT are set to 0.8-1.2 p.u. in these simulations. If the voltage exceeds these limits, the efficiency of the inverter configuration is set to zero. When the voltage is between 0.8-1.2 p.u., MPPT is assumed in all the configurations. This means that the irradiance is assumed to be equal in the whole PV plant and that there are no shadowing.

Table 6.4 tabulates the annual energy extracted by the different PV plants for different isolated DC-DC converter configurations. k_p and k_s refers here to the parallel- and series-connected configurations respectively, while MMC SiC refers to the single-unit DC-DC converter configuration.

The energy efficiency is measured as the ratio of the power output at the MV terminal to the maximum power generated by the PV array. The maximum annual energy differs a bit from the CI and MSCI configuration to the MMC configuration. This is due to a different configuration of the PV arrays in the CI and the MSCI configuration. However, all the configurations are designed as 3 MVA PV power plants. It is seen that the energy efficiency from the single-unit DC-DC converter MMC PV plant configuration at the best-case (1 kHz switching) efficiency profile is 5.65% higher than the CI configuration, and 5.17% higher than the MSCI configuration. For the worst-cast (10 kHz swithcing), this is reduced to 4.77% and 4.29% respectively.

For the MMC with parallel-connected isolated DC-DC converter configuration, the energy efficiency is almost the same at 10 kHz switching as the single-unit configuration is for 1 kHz switching.

For the series-configuration utilizing GaN HEMTs, the efficiency at 20 kHz switching is improved by 5.38% compared to the CI configuration, but reduced by 0.27% compared to the best-case MMC with single-unit DC-DC converter configurations. At a switching of 200 kHz, the efficiency is 0.89% lower for the series-connection. However, a higher switching frequency has a lot of benefits in terms of flux density in the transformer core and the transformer size. This shows that utilizing GaN switches, it is possible to increase the switching frequency without significantly reduce the efficiency of the converter. Even at a switching frequency of 500 kHz, the efficiency of the of MMC PV plant utilizing the series-connected DC-DC converter configuration is not much lower than the single-unit or the parallel-connected configuration.

The MMC PV plant configurations provide higher annual energy yield than the CI and the MSCI configurations. Even at the lowest efficiency of the DC-DC converter arrangements, the yields are higher for the MMC PV plant configurations. This shows that the MMC PV configurations has superior performance compared to the CI and the MSCI PV plant configurations.

Table 6.4: Annual energy obtained from the different PV onfigurations.

PV plant configuration	*Maximum annual energy*	*Annual energy extracted*	*Energy efficiency*
CI	5796 MW_ph	5195 MWh	89.63%
MSCI	5796 MW_ph	5223 MWh	90.11%
MMC SiC at 1 kHz	5930 MW_ph	5650 MWh	95.28%
MMC SiC at 10 kHz	5930 MW_ph	5598 MWh	94.40%
MMC SiC k_p at 10 kHz	5930MW_ph	5648 MWh	95.25%
MMC GaN k_s at 20 kHz	5930 MW_ph	5634MWh	95.01%
MMC GaN k_s at 200 kHz	5930 MW_ph	5597 MWh	94.39%
MMC GaN k_s at 500 kHz	5930 MW_ph	5538 MWh	93.39%

Chapter 7

Economic Benefits

This chapter discusses the possible economic benefits for a MMC PV plant. The different configurations outlined in chapter 4 are juxtapose them with the traditional central inverter configuration and the multi-string inverter configuration for PV plants from an economic perspective.

In order to properly the different topologies that have been analyzed in this study effectively, the levelized cost of energy (LCOE) is considered. The different PV MMC configurations are also compared to the CI and the MSCI configurations introduced at the beginning of this analysis in order to highlight the benefits of a MMC distributed PV plant.

7.1 Levelized Cost of Energy

The LCOE measures the costs divided by the total energy extracted over a lifetime:

$$LCOE = \frac{\text{Total lifetime cost}}{\text{Energy produced over lifetime}} \left[\frac{€}{MWh}\right] \tag{7.1}$$

LCOE makes the comparison between different configurations and technologies possible, since it takes both the total, lifetime extracted energy and the lifetime costs into account. LCOE is an important measurement for prospective projects that intend to make money. LCOE calculates the present value of the total cost of building and operating the PV plant. In this study, however, the total lifetime cost only considers capital investment cost (i.e. initial cost) of the PV plant and does not account for operating costs. It is assumed that the operating costs will be the same for the different PV plant configurations, and thus the difference in LCOE for the different converter configurations is still a viable measuring tool.

The lifetime for a PV Plant is assumed to be 25 years, limited by the PV module life time. The energy produced over the lifetime is found by multiplying the annual extracted energy found in chapter 6 by 25 years. The result is presented in table 7.1. Only the best-case efficiency for the different MMC PV plant configurations are shown.

Table 7.1: Extracted energy over a lifetime for all the configurations.

Inverter Configuration	*Extracted energy*
Central inverter	129 875 MWh
Multi-string inverter	130 575 MWh
MMC single-unit DC-DC converter	141 250 MWh
MMC parallel-connected DC-DC converters	141 200 MWh
MMC series-connected DC-DC converters	140 850 MWh

7.2 Lifetime Cost

In order to calculated the LCOE, the lifetime cost of the different configurations are found. The lifetime cost can mainly be divided into four parts: cost of PV, cost of converters, cost of transformer, and the fixed cost for a power plant [2]. The cost of the PV arrays for the 3 MVA PV plant is €6,000,000.00 [1].

7.2.1 PV Plant Fixed Cost

The fixed cost for the PV plant is assumed to be the same for all the different inverter configurations. This includes the total cost for cables and hardware, pipes, SCADA systems, etc. All the fixed costs that has been taken into account in this thesis are summarized in table 7.2.

Table 7.2: Fixed cost for all the PV plant configurations [1, 5].

Equipment	*Cost*
Mounting structures	€415,688.00
Cables and hardware	€69,281.00
Junction box and distribution boxes	€12,471.00
Lightning arrester, earthing kit	€16,628.00
PVC pipes and accessories	€4,157.00
Spares for 3 years	€6,928.00
SCADA system	€27,713.00
Taxes, CST/KVAT, etc.	€146,572.00
Design, engineering, quality surveillance, testing, transportation, insurance converage, etc.	€250,790.00
Total cost	**€950,228.00**

7.2.2 Converter and Transformer Cost

The cost of the converter and transformer depends on the PV plant configuration. This cost is found for all the inverter configurations, and the result is summarized in table 7.3

Table 7.3: Converter and transformer costs for the different PV plant configurations [6, 2].

Component	*CI*	*MSCI*	*MMC*	*MMC k_p*	*MMC k_s*
Inverter	€154,584.00	€154,584.00	—	—	—
DC-DC converter	—	€109,440.00	€178,440.00	€178,800.00	€195,465.60
Submodule	—	—	€5,730.00	€5,730.00	€5,730.00
Transformer	€53,178.00	€53,178.00	—	—	—
Filter	€1,418.00	1,418.00 €	€620.00	620.00	€620.00
Total cost	**€209,180.00**	**€318,620.00**	**€184,790.00**	**€185,230.00**	**€201,815.60**

Central Inverter and Multi-String Inverter Configurations

The excising CI configuration consists of twelve inverters, three transformers and one filter [1]. Table 7.4 depicts the total cost of one inverter. Each inverter consists of six 6500 V/600 A IGBTs with an unit price of 1,595.00 € and 12x69 electrolytic capacitors with an unit price of 4 €. The resulting total cost of one inverter then becomes 12,882.00 €, which equals 154,584.00 € for 12 inverters. The three transformers have an unit price of 17,726.00 € and the filter costs 1,418.00 € [6]. The total price for the converter, transformer and filter for the CI configuration then becomes 209,180.00 €.

Table 7.4: Cost per inverter [6].

Component	*Unit price*	*Quantity*	*Total price*
6500 V/600 A IGBT	1,595.00 €	6	9,570.00 €
820μF/400V electrolytic capacitor	4.00 €	12x69	3,312.00 €
Total cost			**12,882.00 €**

For the MSCI configuration, the cost is the same as for the CI configuration plus the additional cost of the DC-DC converters. There are assumed 240 DC-DC converters in total for this configuration. Table 7.5 depicts the cost for one DC-DC converter used in the MSCI configuration. Each converter consists of 4 IGBTs, each with an unit price of 89.00 €, and an output filter with the price of 100.00 €. The resulting total cost of one DC-DC converter then becomes 456.00 €, which gives a total cost of 109,440.00 € for all 240 converters. The total cost for the converter, transformer, and filter then becomes 318,620.00 € for the MSCI configuration.

MMC Configurations

The MMC consists of five SMs per phase arm, which gives 30 SMs in total. Each SM consists of two 1700 V/120 A IGBTs with an unit price of 89.00 €, and one capacitor of

Table 7.5: Cost per DC-DC converter for the MSCI configuration [2].

Component	*Unit price*	*Quantity*	*Total price*
1700 V/120 A IGBT	89.00 €	4	356.00 €
Output filter	100.00 €	1	100.00 €
Total cost			**456.00 €**

1 mF with a price of 13.00 €. The cost per SM is 191.00 €, as depicted in table 7.6. The total price for 30 SMs becomes 5,730.00 €.

Table 7.6: Cost per SM for the MMC PV configuration [2].

Component	*Unit price*	*Quantity*	*Total price*
1700 V/120 A IGBT	89.00 €	2	178.00 €
1 mF capacitor	13.00 €	1	13.00 €
Total cost			**191.00 €**

Since the MMC configuration is a transformer-less topology, the main transformer cost is avoided. However, the filter is still used, giving an additional cost of 620.00 € [6]. The required isolation is provided by the HF transformer in the DC-DC converter. The price for the DC-DC converter in the MMC PV plant depends on the DC-DC converter configuration. The prices for the devices utilized in the DC-DC converter configurations for the MMC PV plant is found at farnell.com or at mouser.com, and the price for the highest possible quantity is chosen. The 1200 V/90 A SiC MOSFET C2M0025120D from Wolfspeed has an unit price of 62.00 € when buying 100+ units including the body diode, while the 1200 V/30 A SiC Schottky diode C4D30120D from Wolfspeed has an unit price of 26.00 € when buying 100+ units. The unit price for the GaN HEMT GS66504B is found to be 10.18 € when purchasing 1000 units.

The single-unit DC-DC configuration only requires one unidirectional full-bridge DC-DC converter. It utilizes four controllable switches consisting of two MOSFETs in parallel in order to handle the current, which gives a total price of 496.00 € for the MOSFETs. On the secondary side, it utilizes four diode rectifiers, each consisting of four diodes in parallel. This gives a price of 416.00 € for the diodes. The DC-link capacitor consists of three 820 μF/400 V capacitors in series in order to handle the 1 kV rating, and three of these connected in parallel to obtain the required capacitance in the circuit. Each capacitor costs 4.00 €, and the price for nine comes to 36.00 €.

The cost of the HF transformer is assumed to be 50.00 € per kW. This is just an assumption based on earlier knowledge, and is assumed to be a high cost estimate. The cost for an actual transformer is therefore assumed to be lower, and this estimate can later be replaced with the actual cost of the HF transformer to obtain a more accurate LCOE calculation. The required 100 kW HF transformer is therefore assumed to cost around 5,000.00 €. The total cost of the single-unit DC-DC converter then becomes 5,948.00 € and is tabulated in table 7.7. In the MMC configuration, one DC-DC converter is connected to each SM. With 30 SMs, this results in a total cost of 178,440.00 € for the DC-DC converters in this MMC configuration.

Table 7.7: Cost for single-unit full-bridge DC-DC converter.

Component	*Unit price*	*Quantity*	*Total price*
1200 V/90 A SiC MOSFET	62.00 €	2x4	496.00 €
1200 V/88 A SiC Schottky diodes	26.00 €	4x4	416.00 €
80 μF/400 V electrolytic capacitor	4.00 €	3x3	36.00 €
100 kW HF Transformer	5,000.00 €	1	5,000.00 €
Total cost			**5,948.00 €**

For the parallel configuration of two full-bridge DC-DC converters, here referred to as MMC k_p, only one MOSFETs is required for each switch due to the lower current rating. A total number of eight MOSFETs gives a price of 496.00 €. Each DBR utilizes 2 diodes in parallel, resulting in a total number of 16 diodes. The DC-link capacitor in each full-bridge still consists of three 820 μF/400 V capacitors in series in order to handle the 1 kV rating, but two of these connected in parallel are enough to obtain the required capacitance in the circuit. The 50 kW HF transformers are also here assumed to cost 50.00 € per kW, resulting in a price of 2,500.00 € each. The total cost of the two parallel-connected full-bridge DC-DC converter then becomes 5,960.00 €, which is tabulated in table 7.9.

Table 7.8: Cost for two SiC based full-bridge DC-DC converters in parallel.

Component	*Unit price*	*Quantity*	*Total price*
1200 V/90 A SiC MOSFET	62.00 €	2x4	496.00 €
1200 V/88 A SiC Schottky diodes	26.00 €	2x2x4	416.00 €
80 μF/400 V electrolytic capacitor	4.00 €	2x3x2	48.00 €
50 kW HF Transformer	2,500.00 €	2	5,000.00 €
Total cost			**5,960.00 €**

For the series-connection of two full-bridge converters utilizing GaN HEMTs, the number of switching devices connected in parallel is 8 due to the current rating of 15 A per device. The total price for the GaN HEMTs becomes 652.00 €. The DBR utilizes a parallel-connection of four SiC Schottky diodes in each switch due to the high current, resulting in a total cost of 832.00 €. The required number of capacitors in series in order to handle the voltage rating is assumed to be 2. And 2 of these series-connected capacitors are connected in parallel in order to obtain the required capacitance in the circuit. It is assumed that it utilizes the same HF transformer as in the series-connection of two converters. This gives a total cost of one isolated GaN-based parallel-connected DC-DC converter to be 6,516.00 €, resulting in a total cost of 195,480.00 € for the isolated DC-DC converters.

7.2.3 Total Lifetime Cost

The total lifetime cost of the different configurations are summarized in table 7.10. It shows that the total cost is least for the MMC PV plant utilizing a single-unit DC-DC converter. This is due to the choice of a lower number of DC-DC converter in the MMC

Table 7.9: Cost for two GaN-based full-bridge DC-DC converters in series.

Component	*Unit price*	*Quantity*	*Total price*
650 V/15 A GaN HEMTs	10.18 €	2x8x4	651.52 €
1200 V/88 A SiC Schottky diodes	26.00 €	2x4x4	832.00 €
80 μF/400 V electrolytic capacitor	4.00 €	2x2x2	32.00 €
50 kW HF Transformer	2,500.00 €	2	5,000.00 €
Total cost			**6,515.52 €**

compared to the MSCI configuration, due to a high rating of the SMs. These results are used in the next section to calculate the LCOE of the PV plant configurations.

Table 7.10

Cost	*CI*	*MSCI*	*MMC*	*MMC k_p*	*MMC k_s*
PV array	6,000,000.00 €	6,000,000.00 €	6,000,000.00 €	6,000,000.00 €	6,000,000.00 €
Fixed cost	950,228.00 €	950,228.00 €	950,228.00 €	950,228.00€	950,228.00€
Converter, transformer, and filter	209,180.00 €	318,620.00 €	184,790.00 €	185,230.00€	201,830.00 €
Total cost	**7,159,408.00 €**	**7,268,848.00€**	**7,135,018.00 €**	**7,135,458.00 €**	**7,152,058.00€**

7.3 Extracted energy, Total Cost and LCOE

The annual energy extracted from the different PV plant configurations were found in chapter 6, and presented in 6.3. The LCOE can now be evaluated with respect to the total lifetime cost presented in table 7.10 for the different configurations. The CI configuration is chosen as the base unit quantity. The extracted energy in p.u. values is calculated with the energy efficiency is calculated in order to account for the difference in the maximum annual energy available at the different PV plant configurations. This means that the energy efficiency and the total cost of the other configurations are given in p.u. values with respect to the CI energy efficiency (89.63%) and the CI total cost (7,159,408.00 €).

Table 7.11 shows the LCOE for all the structures in p.u. considering the central inverter as the base unit quantity.

Table 7.11: Extracted energy, total cost, and LCOE for all the configurations in per unit.

Configuration	*Extracted energy (p.u.)*	*Total cost (p.u.)*	*LCOE (p.u.)*
Central inverter	1.000	1.000	1.000
Multi-string inverter	1.0054	1.0153	1.0098
MMC single-unit	1.0630	0.9966	0.9375
MMC k_p	1.0627	0.9967	0.9379
MMC k_s	1.0600	0.9990	0.9424

From table 7.11, it is seen that the LCOE is better for all the MMC PV plant configurations compared to the CI and the MSCI PV plant configurations. The LCOE is best for the MMC PV plant utilizing the single-unit DC-DC configuration, with a 6.25% and 7.23% lower LCOE than the CI and MSCI respectively. The MMC PV plants utilizing the parallel-configuration of DC-DC converters have 6.21% and 7.19% lower LCOE than the CI and MSCI respectively. The MMC PV plants utilizing the series-configuration of DC-DC converters have 5.76% and 6.74% lower LCOE than the CI and MSCI respectively. This results in only 0.49% lower LCOE in the MMC PV plant utilizing the single-unit DC-DC converter at a switching frequency of 1 kHz compared to the MMC PV plant utilizing the series-connection of DC-DC converter at a switching frequency of 20 kHz. Even at a switching frequency of 200 kHz for the MMC PV plant utilizing the series-connection of DC-DC converter, the LCOE becomes as high as 0.9486.

These simulations and calculations have been done assuming no partial shading in the PV plant. The MMC configuration will increase the MPPT substantially, resulting in higher extracted energy (p.u.) compared to the CI configuration then what is shown here for partially shaded and non-equalized irradiance conditions in the PV plant. This results in a substantially decrease in the LCOE (p.u.) of the MMC PV configuration compared to the CI configuration in non-idealized conditions. The series- and parallel-configurations of the isolated DC-DC converters will increase the MPPT even more due to the distribution of the bulk transmission of power to the MMC SM and the increased number of DC-DC converters with MPPT.

Chapter 8

Conclusion and Further Work

The conclusion based on the results obtained from simulations, both regarding the efficiency of the different isolated DC-DC converters configurations and the energy yield and LCOE for the whole PV plant configurations, are presented in this chapter. This summarizes the discussions provided in the earlier chapters to get an overview of what is done. To get the full aspect and overview of the assumptions and analyses, it is therefore recommended to read those chapters first. The last section briefly presents some proposed topics for future work, reflecting the possibilities with utilizing the MMC inverter in PV plants.

8.1 Conclusion

This study has investigated different isolated DC-DC converter topologies to interface PV arrays to the SMs in a MMC PV plant. The isolated DC-DC converter configurations have been compared in terms of efficiency, MPPT, and switching frequency range. The benefits and drawbacks of each configuration have been discussed.

The benefits of the single-unit isolated DC-DC converter configuration is the straightforward and simple structure. However, the full-bridge must be rated for the whole power transfer from the PV array to the SM. This results in a high current rating, which requires several switching devices operating in parallel.

By utilizing a parallel-connection of two full-bridge DC-DC converters rated for only half the power transfer, the current through each full-bridge decreases. A 50% reduction in the current through each full-bridge results in a 50% reduction in the total copper losses. The copper losses are proportional to the square current, and by reducing the current by 50%, the total copper losses is reduced by 50%. However, the voltage rating is the same when assuming an unity voltage transformer ratio.

SiC MOSFETs have been utilized in the full-bridge due to the high voltage rating. Simulations have been performed at different DC-link voltages, at many different switching frequencies and for the entire operating range of 0.1-1 per unit power in order to find the efficiency. The results was an efficiency in the 98%-99% range for both the configurations. However, these simulations did not account for losses in the HF transformer.

A series-connection of DC-DC converters results in a lowered voltage rating for each full-bridge, reducing the voltage stress on the switching devices considerably. This makes an utilization of GaN switching devices possible. GaN switching devices have a lower voltage rating than SiC. However, they have shown a superior performance, especially at high-frequency operation. High-frequency operation is beneficial due to reduced size of the HF transformer. The efficiency of the GaN-based series-connected full-bridge DC-DC converter was obtained by calculations of the switching and conduction losses by assuming a worst-case duty ratio of 0.5. The results gave a high efficiency of 98% for a operating range up to 200 kHz switching.

The main advantage for the series- and the parallel-connection of converters is that the bulk transmission of power to the SM is distributed. This results in an increase in the overall reliability of the PV plant inverter configuration.

The annual energy losses for different efficiency curves for the DC-DC converter configurations were used to obtain the overall efficiency of the different MMC PV plant configurations, and to state the benefits of utilizing MMC instead of the excising CI and MSCI topology in medium voltage PV plants. The extracted energy was compared with the maximum energy available at the PV plant. The MMC topology, as well as the MSCI topology, provides lower MPPT losses due to the distributed MPPT in comparison with the CI configuration. The MMC configurations had a better energy efficiency for all the different DC-DC converter configurations compared to both the CI and the MSCI configuration. For the MMC utilizing the single-unit DC-DC configuration, the energy efficiency was obtained to be 95.28% for the best-case switching frequency at 1 kHz, and 94.40% for the worst-case switching frequency at 20 kHz. The CI and MSCI efficiency was in comparison 89.63% and 90.11% respectively. However, the MMC configurations did not account for losses in the HF transformer in the DC-DC configurations. It is assumed that these losses do not account for a great part of the total losses in the PV plant, and the results would have been almost the same when accounting for them.

For the MMC utilizing a parallel-connection of DC-DC converters, the energy efficiency was obtained to be 95.25% at 10 kHz switching. The MMC utilizing the GaN-based series-connection of DC-DC converters, the energy efficiency was calculated to be 95.01% at 20 kHz switching, and 94.39% at 200 kHz switching.

The LCOE was shown to be 6.25% lower for the MMC utilizing the single-unit DC-DC converter compared to the CI configuration, and 6.21% and 5.76% lower for the MMC utilizing the parallel- and series-connection of DC-DC converters respectively. This shows the great benefits of utilizing the MMC instead of the conventional PV inverters.

Another important aspect is that partial shading is not considered in these simulations. The MMC configurations will increase the MPPT substantially, resulting in a even higher extracted energy compared to the CI configuration during partially shaded and non-equalized irradiance conditions in the PV plant. The parallel- and series-connection of DC-DC converters increases the MPPT more than the single-unit DC-DC converter configuration. This will result in a substantially decrease in the LCOE of the MMC PV configurations compared to the CI configuration.

A higher number of series- or parallel-connected DC-DC converter may result in higher efficiency and lower losses, but at the cost of a more complex system and a higher price due to more components. The number of series- and parallel-connected devices must therefore be selected with care.

The proposed MMC PV plant configurations seems from the results presented in this thesis to be an attractive solution for medium voltage PV plants. But further work on simulations and finally hardware tests on prototypes should be carried out to completely verify and provide an even clearer picture on the pros and cons of this solution.

8.2 Further Work

Isolated full-bridge DC-DC converters were chosen for investigation in this thesis. In these configurations, it was assumed a unity voltage ratio in the HF transformer. Another configuration that would have been of interest to analyze is a 1:N transformer ratio in the parallel-connection of DC-DC converters. This would have resulted in a lower voltage ration on the full-bridge, and an utilization of GaN HEMTs would have been possible in this configuration too. The parallel-connection reduces the current rating of the full-bridge, avoiding the need to parallel-connect as many devices for each switch in order to handle the current from the PV array. This solution would therefore might be more cost-effective, and result in a lowered LCOE for the PV plant.

The losses in the GaN HEMTs were difficult to estimate from simulations due to very long simulation times at high frequencies. The turn-on and turn-off losses for this device were therefore only estimated from values given from the manufacturer. Experiments with GaN HEMTs would therefore have been beneficial in order to find the actual turn-on and turn-off losses. [50] has found from experiments that a relatively high on-state voltage drops occurs during reverse conduction in GaN devices. An interesting solution would then have been to utilize anti-parallel SiC Schottky diodes with the GaN HEMT.

It would also have been interesting to also analyze other DC-DC converters in order to evaluate their performance in a similar medium voltage MMC PV plants. It would especially have been of interest to utilize the half-bridge converter in the series- and parallel-configurations presented in this thesis. These configurations provide distribution of the bulk power transfer, which makes an utilization of the half-bridge possible. The half-bridge converter utilities two half-bridges instead of one full-bridge and one DBR, resulting in a total number of four active switches. This results in a lower cost due to the absence of the DBR, which may result in a decreased LCOE.

Another interesting aspect would have been to look at the use of battery energy storage systems (BESS) in the MMC PV plant. Battery storage can either be concentrated or distributed. By utilizing a tertiary winding in the HF transformer in the isolated DC-DC converter configurations in the MMC PV plant, a realization of a distributed BESS would have been possible. This tertiary winding could have made it possible to deliver power from the BESS in periods with low irradiance and low power production at the PV plant. However, with a BESS in the HF transformer, it would have been necessary to replace the DBR with a full-bridge on the secondary side, in order to obtain bidirectional power flow. This will require more control, which results in a higher cost.

Bibliography

[1] H. Mitavachan, A. Gokhale, and J. Srinivasan, "3-mw scale grid-connected solar photovoltaic power plant at kolar, karnataka."

[2] A. B. Acharya, M. Ricco, D. Sera, R. Teodorescu, and L. E. Norum, "Performance analysis of medium voltage grid integration of pv plant using modular multilevel converter," In process of publication.

[3] T. E. S. Ltd. Pv module titan s6-60. [Online]. Available: https://cdn.enfsolar.com/Product/pdf/Crystalline/5029cfb7bd1c8.pdf

[4] K.-N. D. Malamaki and C. S. Demoulias, "Analytical calculation of the electrical energy losses on fixed-mounted pv plants," *IEEE Transactions on Sustainable Energy*, vol. 5, no. 4, pp. 1080–1089, 2014.

[5] Y. Xue, K. C. Divya, G. Griepentrog, M. Liviu, S. Suresh, and M. Manjrekar, "Towards next generation photovoltaic inverters," in *Energy Conversion Congress and Exposition (ECCE), 2011 IEEE.* IEEE, 2011, pp. 2467–2474.

[6] Y. Xue, B. Ge, and F. Z. Peng, "Reliability, efficiency, and cost comparisons of mw-scale photovoltaic inverters," in *Energy Conversion Congress and Exposition (ECCE), 2012 IEEE.* IEEE, 2012, pp. 1627–1634.

[7] "Global trends in renewable energy investment 2018," 2018.

[8] B. Parikshith, "Integrated approach to filter design for grid connected power converters," *MSc (Engg.) thesis, Indian Institute of Science, Bangalore, India*, 2009.

[9] N. Mohan and T. M. Undeland, *Power electronics: converters, applications, and design.* John Wiley & Sons, 2007.

[10] J. Millan, P. Godignon, X. Perpina, A. Pérez-Tomás, and J. Rebollo, "A survey of wide bandgap power semiconductor devices," *IEEE transactions on Power Electronics*, vol. 29, no. 5, pp. 2155–2163, 2014.

[11] Gs66504b-evbdb gan e-hemt daughter board and gs665mb-evb evaluation platform. [Online]. Available: https://gansystems.com/wp-content/uploads/2018/01/GS66504B-EVBDB_UserGuide_rev_20161117.pdf

[12] U. N. F. C. on Climate Change, "Historic paris agreement on climate change: 195 nations set path to keep temperature rise well below 2 degrees celsius," 2015. [Online]. Available: https://unfccc.int/news/finale-cop21

[13] F. Katiraei and J. R. Aguero, "Solar pv integration challenges," *IEEE Power and Energy Magazine*, vol. 9, no. 3, pp. 62–71, 2011.

[14] S. C. Smith, P. Sen, B. Kroposki, and K. Malmedal, "Renewable energy and energy storage systems in rural electrical power systems: Issues, challenges and application guidelines," in *Rural Electric Power Conference (REPC), 2010 IEEE.* IEEE, 2010, pp. B4–B4.

[15] V. Kumar, A. Pandey, and S. Sinha, "Grid integration and power quality issues of wind and solar energy system: A review," in *Emerging Trends in Electrical Electronics & Sustainable Energy Systems (ICETEESES), International Conference on.* IEEE, 2016, pp. 71–80.

[16] M. Hossain, N. Rahim *et al.*, "Recent progress and development on power dc-dc converter topology, control, design and applications: A review," *Renewable and Sustainable Energy Reviews*, vol. 81, pp. 205–230, 2018.

[17] T. Esram and P. L. Chapman, "Comparison of photovoltaic array maximum power point tracking techniques," *IEEE Transactions on energy conversion*, vol. 22, no. 2, pp. 439–449, 2007.

[18] N. Femia, G. Petrone, G. Spagnuolo, and M. Vitelli, "Optimization of perturb and observe maximum power point tracking method," *IEEE transactions on power electronics*, vol. 20, no. 4, pp. 963–973, 2005.

[19] E. Koutroulis, K. Kalaitzakis, and N. C. Voulgaris, "Development of a microcontroller-based, photovoltaic maximum power point tracking control system," *IEEE Transactions on power electronics*, vol. 16, no. 1, pp. 46–54, 2001.

[20] J. Ahmed and Z. Salam, "An improved perturb and observe (p&o) maximum power point tracking (mppt) algorithm for higher efficiency," *Applied Energy*, vol. 150, pp. 97–108, 2015.

[21] A. Cabrera-Tobar, E. Bullich-Massagué, M. Aragüés-Peñalba, and O. Gomis-Bellmunt, "Topologies for large scale photovoltaic power plants," *Renewable and Sustainable Energy Reviews*, vol. 59, pp. 309–319, Jun. 2016.

[22] Y. Xue, K. C. Divya, G. Griepentrog, M. Liviu, S. Suresh, and M. Manjrekar, "Towards next generation photovoltaic inverters," in *2011 IEEE Energy Conversion Congress and Exposition*, Sep. 2011, pp. 2467–2474.

[23] M. R. Islam, Y. Guo, and J. Zhu, “Multiple-input multiple-output medium frequency-link based medium voltage inverter for direct grid connection of photovoltaic arrays,” in *2013 International Conference on Electrical Machines and Systems (ICEMS)*, Oct. 2013, pp. 202–207.

[24] B. Xiao, L. Hang, J. Mei, C. Riley, L. M. Tolbert, and B. Ozpineci, “Modular Cascaded H-Bridge Multilevel PV Inverter With Distributed MPPT for Grid-Connected Applications,” *IEEE Transactions on Industry Applications*, vol. 51, no. 2, pp. 1722–1731, Mar. 2015.

[25] S. Rivera, B. Wu, R. Lizana, S. Kouro, M. Perez, and J. Rodriguez, “Modular multilevel converter for large-scale multistring photovoltaic energy conversion system,” in *2013 IEEE Energy Conversion Congress and Exposition*, Sep. 2013, pp. 1941–1946.

[26] T. Soong and P. W. Lehn, “Assessment of fault tolerance in modular multilevel converters with integrated energy storage,” *IEEE Transactions on Power Electronics*, vol. 31, no. 6, pp. 4085–4095, 2016.

[27] S. P. Engel, M. Stieneker, N. Soltau, S. Rabiee, H. Stagge, and R. W. D. Doncker, “Comparison of the Modular Multilevel DC Converter and the Dual-Active Bridge Converter for Power Conversion in HVDC and MVDC Grids,” *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 124–137, Jan. 2015.

[28] A. Hillers and J. Biela, “Optimal design of the modular multilevel converter for an energy storage system based on split batteries,” in *2013 15th European Conference on Power Electronics and Applications (EPE)*, Sep. 2013, pp. 1–11.

[29] “Ieee standard for interconnecting distributed resources with electric power systems,” *IEEE Std 1547-2003*, pp. 1–28, July 2003.

[30] A. Lesnicar and R. Marquardt, “An innovative modular multilevel converter topology suitable for a wide power range,” in *Power Tech Conference Proceedings, 2003 IEEE Bologna*, vol. 3. IEEE, 2003, pp. 6–pp.

[31] H. Akagi, “Classification, terminology, and application of the modular multilevel cascade converter (mmcc),” *IEEE Transactions on Power Electronics*, vol. 26, no. 11, pp. 3119–3130, 2011.

[32] H. Nademi, *Advanced control of power converters: Modular multilevel converter*. NTNU, 2014.

[33] K. Sharifabadi, L. Harnefors, H.-P. Nee, S. Norrga, and R. Teodorescu, *Design, Control, and Application of Modular Multilevel Converters for HVDC Transmission Systems*. John Wiley & Sons, 2016.

[34] A. The, J. Böcker, and S. Dieckerhoff, “Energy storage and circulating currents in the modular multilevel converter,” in *Energy Conversion Congress and Exposition (ECCE), 2012 IEEE*. IEEE, 2012, pp. 4788–4793.

[35] "IEEE Application Guide for IEEE Std 1547(TM), IEEE Standard for Interconnecting Distributed Resources with Electric Power Systems," *IEEE Std 1547.2-2008*, pp. 1–217, Apr. 2009.

[36] F. Krismer, "Modeling and optimization of bidirectional dual active bridge dc-dc converter topologies," 2010.

[37] F. Krismer, J. Biela, and J. W. Kolar, "A comparative evaluation of isolated bi-directional dc/dc converters with wide input and output voltage range," in *Industry Applications Conference, 2005. Fourtieth IAS Annual Meeting. Conference Record of the 2005*, vol. 1. IEEE, 2005, pp. 599–606.

[38] J.-S. Lai and D. J. Nelson, "Energy management power converters in hybrid electric and fuel cell vehicles," *Proceedings of the IEEE*, vol. 95, no. 4, pp. 766–777, 2007.

[39] C. P. Dick, K. Rigbers, H. Radermacher, and R. W. De Doncker, "Investigations on the controllability and the design of dc/dc convertors connected to pv-generators," *Electrical Power Quality and Utilisation. Journal*, vol. 12, no. 2, pp. 47–52, 2006.

[40] K. Takagi and H. Fujita, "Dynamic control and performance of an isolated dual-active-bridge dc–dc converter," in *Power Electronics and ECCE Asia (ICPE-ECCE Asia), 2015 9th International Conference on*. IEEE, 2015, pp. 1521–1527.

[41] S. J. Chapman, *Electric Machinery Fundamentals*. McGraw-Hill, 2012.

[42] V. C. Valchev and A. Van den Bossche, *Inductors and transformers for power electronics*. CRC press, 2005.

[43] V. Ramanarayanan, "Course material on switched mode power conversion," *Indian Institute of Science*, 2006.

[44] M. Sippola and R. E. Sepponen, "Accurate prediction of high-frequency power-transformer losses and temperature rise," *IEEE Transactions on Power Electronics*, vol. 17, no. 5, pp. 835–847, 2002.

[45] P. Dowell, "Effects of eddy currents in transformer windings," in *Proceedings of the Institution of Electrical Engineers*, vol. 113, no. 8. IET, 1966, pp. 1387–1394.

[46] C. W. T. McLyman, *Transformer and inductor design handbook*. CRC press, 2016.

[47] H. Choi, "Overview of silicon carbide power devices," *Fairchild semiconductor*, 2017.

[48] R. Ramachandran and M. Nymand, "Switching losses in a 1.7 kw gan based full-bridge dc-dc converter with synchronous rectification," in *Power Electronics and Applications (EPE'15 ECCE-Europe), 2015 17th European Conference on*. IEEE, 2015, pp. 1–10.

[49] Y. Ando, Y. Shirahata, T. Oku, T. Matsumoto, Y. Ohishi, M. Yasuda, A. Shimono, Y. Takeda, and M. Murozono, “Comparison between sic-and si-based inverters for photovoltaic power generation systems,” *Journal of Power and Energy Engineering*, vol. 5, no. 01, p. 30, 2017.

[50] A. Chub, M. Zdanowski, A. Blinov, and J. Rabkowski, “Evaluation of gan hemts for high-voltage stage of isolated dc-dc converters,” in *Compatibility, Power Electronics and Power Engineering (CPE-POWERENG), 2016 10th International Conference on*. IEEE, 2016, pp. 375–379.

[51] S. Taranovich, “Si vs. gan vs. sic: Which process and supplier are best for my power design?” *March*, vol. 15, pp. 533–562, 2013.

[52] Y. Shi, R. Li, Y. Xue, and H. Li, “High-Frequency-Link-Based Grid-Tied PV System With Small DC-Link Capacitor and Low-Frequency Ripple-Free Maximum Power Point Tracking,” *IEEE Transactions on Power Electronics*, vol. 31, no. 1, pp. 328–339, Jan. 2016.

[53] Y. Shi and H. Li, “Isolated Modular Multilevel DC #8211;DC Converter With DC Fault Current Control Capability Based on Current-Fed Dual Active Bridge for MVDC Application,” *IEEE Transactions on Power Electronics*, vol. 33, no. 3, pp. 2145–2161, Mar. 2018.

[54] H. Akagi, T. Yamagishi, N. M. L. Tan, S. i Kinouchi, Y. Miyazaki, and M. Koyama, “Power-loss breakdown of a 750-V, 100-kW, 20-kHz bidirectional isolated DC-DC converter using SiC-MOSFET/SBD dual modules,” in *2014 International Power Electronics Conference (IPEC-Hiroshima 2014 - ECCE ASIA)*, May 2014, pp. 750–757.

[55] M. G. Villalva, J. R. Gazoli, and E. Ruppert Filho, “Comprehensive approach to modeling and simulation of photovoltaic arrays,” *IEEE Transactions on power electronics*, vol. 24, no. 5, pp. 1198–1208, 2009.

[56] C. R. S. Reinoso, D. H. Milone, and R. H. Buitrago, “Simulation of photovoltaic centrals with dynamic shading,” *Applied Energy*, vol. 103, pp. 278–289, 2013.

[57] System advisor model (sam). [Online]. Available: https://sam.nrel.gov/

[58] D. L. King, J. A. Kratochvil, and W. E. Boyson, *Photovoltaic array performance model*. Citeseer, 2004.

Appendix

A Power Switching Devices

This section presents data for some of the SiC MOSFETs, GaN HEMTs, and SiC Schottky diodes available in the market and compares them in terms of voltage and current ratings.

The datasheets for the switching devices utilized in simulations in this thesis are also provided here.

A.1 SiC MOSFETs

The MOSFETs with the lowest $R_{ds,on}$ for the same voltage rating from each manufacturer are presented here.

Table A1: Comparison of different manufacturers SiC MOSFETs at 25 °C.

Device	$V_{DS,max}$	I_D	$R_{ds,on}$	E_{on}	E_{off}
Cree C2M0045170D	1700 V	72 A	45 $m\Omega$	2.1 mJ	0.86 mJ
Rohm SCT2750NY	1700 V	6 A	750 $m\Omega$	0.076 mJ	0.033 mJ
Cree C2M0025120D	1200 V	90 A	25 $m\Omega$	1.4 mJ	0.3 mJ
Rohm SCT2080KE	1200 V	40 A	80 $m\Omega$	0.174 mJ	0.051 mJ
Rohm SCT3022KL	1200 V	95 A	22 $m\Omega$	0.632 mJ	0.243 mJ
USCi Cascode JFET UJC1206K	1200 V	38 A	60 $m\Omega$	0.657 mJ	0.147 mJ
USCi Cascode JFET UJ3C120040K3S	1200 V	65 A	35 $m\Omega$	0.930 mJ	0.299 mJ
Cree C3M0030090K	900 V	63 A	30 $m\Omega$	0.22 mJ	0.12 mJ
Rohm SCT3017AL	650 V	118 A	17 $m\Omega$	0.369 mJ	0.156 mJ
USCi Cascode JFET UJ3C065030B3	650 V	66 A	27 $m\Omega$	0.180 mJ	0.341 mJ
USCi Cascode JFET UJ3C065030T3S	650 V	85 A	27 $m\Omega$	0.427 mJ	0.257 mJ

C2M0025120D

Silicon Carbide Power MOSFET
C2M^{TM} MOSFET Technology

N-Channel Enhancement Mode

V_{DS}	1200 V
I_D @ 25˚C	90 A
$R_{DS(on)}$	25 mΩ

Features

- High Blocking Voltage with Low On-Resistance
- High Speed Switching with Low Capacitances
- Easy to Parallel and Simple to Drive
- Avalanche Ruggedness
- Resistant to Latch-Up
- Halogen Free, RoHS Compliant

Benefits

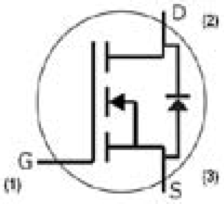
- Higher System Efficiency
- Reduced Cooling Requirements
- Increased Power Density
- Increased System Switching Frequency

Applications

- Solar Inverters
- Switch Mode Power Supplies
- High Voltage DC/DC converters
- Battery Chargers
- Motor Drive
- Pulsed Power Applications

Package

TO-247-3



Part Number	Package
C2M0025120D	TO-247-3

Maximum Ratings (T$_C$ = 25 ˚C unless otherwise specified)

Symbol	Parameter	Value	Unit	Test Conditions	Note
V_{DSmax}	Drain - Source Voltage	1200	V	V_{GS} = 0 V, I_D = 100 μA	
V_{GSmax}	Gate - Source Voltage	-10/+25	V	Absolute maximum values	
V_{GSop}	Gate - Source Voltage	-5/+20	V	Recommended operational values	
I_D	Continuous Drain Current	90	A	V_{GS} =20 V, T_C = 25˚C	Fig. 19
		60		V_{GS} =20 V, T_C = 100˚C	
$I_{D(pulse)}$	Pulsed Drain Current	250	A	Pulse width t_P limited by T_{jmax}	Fig. 22
P_D	Power Dissipation	463	W	T_C=25˚C, T_J = 150 ˚C	Fig. 20
T_J , T_{stg}	Operating Junction and Storage Temperature	-55 to +150	˚C		
T_L	Solder Temperature	260	˚C	1.6mm (0.063”) from case for 10s	
M_d	Mounting Torque	1 8.8	Nm lbf-in	M3 or 6-32 screw	

Electrical Characteristics (T_C = 25˚C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	1200			V	V_{GS} = 0 V, I_D = 100 μA	
$V_{GS(th)}$	Gate Threshold Voltage	2.0	2.6	4	V	V_{DS} = V_{GS}, I_D = 15mA	Fig. 11
			2.1		V	V_{DS} = V_{GS}, I_D = 15mA, T_J = 150 °C	
I_{DSS}	Zero Gate Voltage Drain Current		2	100	μA	V_{DS} = 1200 V, V_{GS} = 0 V	
I_{GSS}	Gate-Source Leakage Current			600	nA	V_{GS} = 20 V, V_{DS} = 0 V	
$R_{DS(on)}$	Drain-Source On-State Resistance		25	34	mΩ	V_{GS} = 20 V, I_D = 50 A	Fig. 4,5,6
			43			V_{GS} = 20 V, I_D = 50 A, T_J = 150 °C	
g_{fs}	Transconductance		23.6		S	V_{DS}= 20 V, I_{DS}= 50 A	Fig. 7
			21.7			V_{DS}= 20 V, I_{DS}= 50 A, T_J = 150 °C	
C_{iss}	Input Capacitance		2788		pF	V_{GS} = 0 V V_{DS} = 1000 V f = 1 MHz V_{AC} = 25 mV	Fig. 17,18
C_{oss}	Output Capacitance		220				
C_{rss}	Reverse Transfer Capacitance		15				
E_{oss}	C_{oss} Stored Energy		121		μJ		Fig 16
E_{AS}	Avalanche Energy, Single Pluse		3.5		J	I_D = 50A, V_{DD} = 50V	Fig. 29
E_{ON}	Turn-On Switching Energy		1.4		mJ	V_{DS} = 800 V, V_{GS} = -5/20 V, I_D = 50A, $R_{G(ext)}$ = 2.5Ω,L= 412 μH	Fig. 25
E_{OFF}	Turn Off Switching Energy		0.3				
$t_{d(on)}$	Turn-On Delay Time		14		ns	V_{DD} = 800 V, V_{GS} = -5/20 V I_D = 50 A, $R_{G(ext)}$ = 2.5 Ω, R_L = 16 Ω Timing relative to V_{DS} Per IEC60747-8-4 pg 83	Fig. 27
t_r	Rise Time		32				
$t_{d(off)}$	Turn-Off Delay Time		29				
t_f	Fall Time		28				
$R_{G(int)}$	Internal Gate Resistance		1.1		Ω	f = 1 MHz, V_{AC} = 25 mV, ESR of C_{ISS}	
Q_{gs}	Gate to Source Charge		46		nC	V_{DS} = 800 V, V_{GS} = -5/20 V I_D = 50 A Per IEC60747-8-4 pg 83	Fig. 12
Q_{gd}	Gate to Drain Charge		50				
Q_g	Total Gate Charge		161				

Reverse Diode Characteristics

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
V_{SD}	Diode Forward Voltage	3.3		V	V_{GS} = - 5 V, I_{SD} = 25 A	Fig. 8, 9, 10
		3.1		V	V_{GS} = - 5 V, I_{SD} = 25 A, T_J = 150 °C	
I_S	Continuous Diode Forward Current		90		T_C= 25 °C	Note 1
t_{rr}	Reverse Recovery Time	45		ns	V_{GS} = - 5 V, I_{SD} = 50 A ,T_J = 25 °C VR = 800 V dif/dt = 1000 A/μs	Note 1
Q_{rr}	Reverse Recovery Charge	406		nC		
I_{rrm}	Peak Reverse Recovery Current	13.5		A		

Note (1): When using SiC Body Diode the maximum recommended V_{GS} = -5V

Thermal Characteristics

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
$R_{θJC}$	Thermal Resistance from Junction to Case	0.24	0.27	°C/W		Fig. 21
$R_{θJC}$	Thermal Resistance from Junction to Ambient		40			

Typical Performance

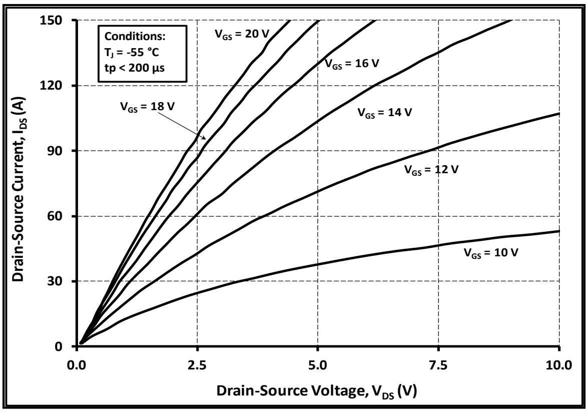


Figure 1. Output Characteristics T_J = -55 °C

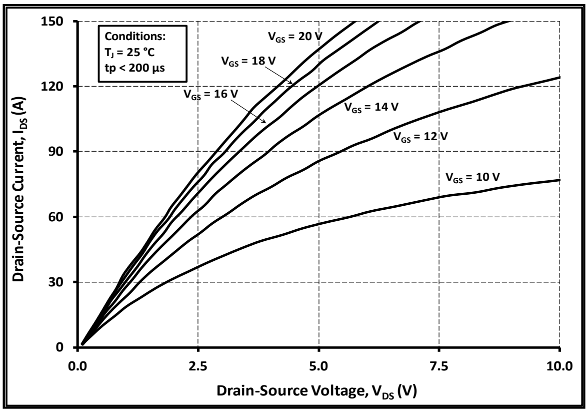


Figure 2. Output Characteristics T_J = 25 °C

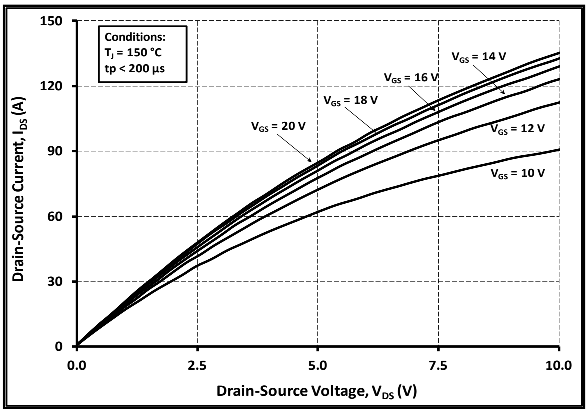


Figure 3. Output Characteristics T_J = 150 °C

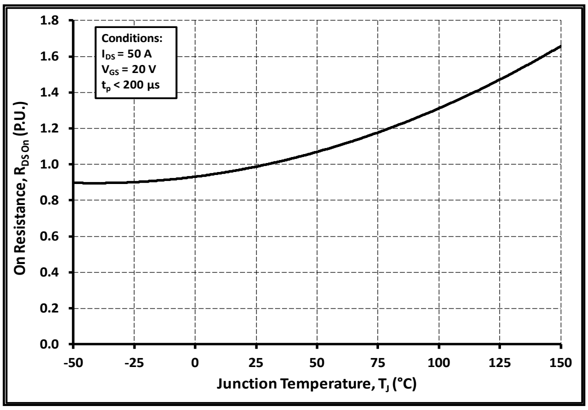


Figure 4. Normalized On-Resistance vs. Temperature

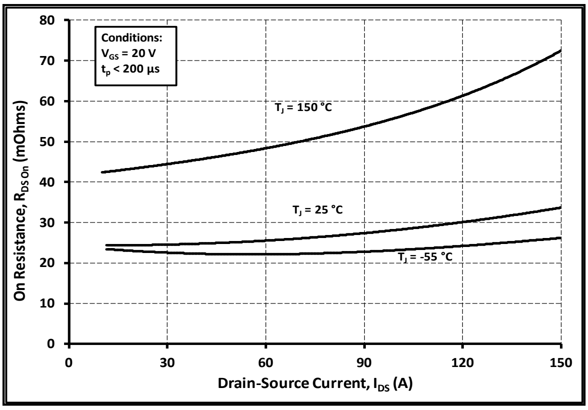


Figure 5. On-Resistance vs. Drain Current
For Various Temperatures

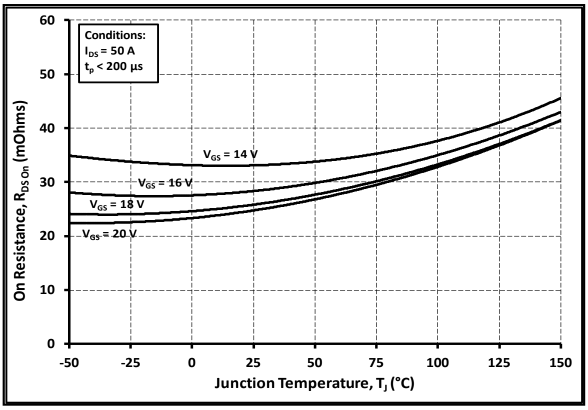


Figure 6. On-Resistance vs. Temperature
For Various Gate Voltage

Typical Performance

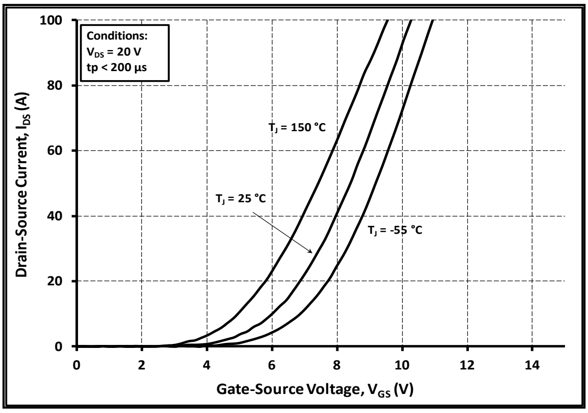


Figure 7. Transfer Characteristic For Various Junction Temperatures

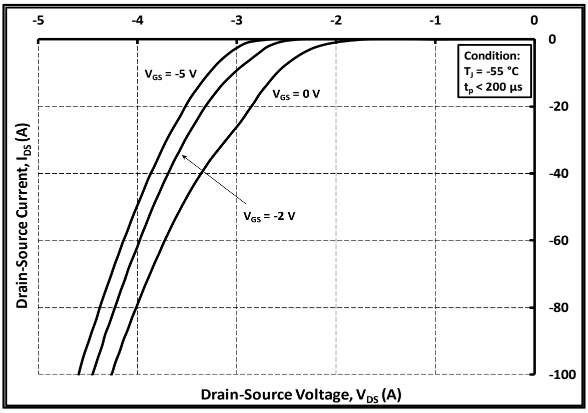


Figure 8. Body Diode Characteristic at -55 °C

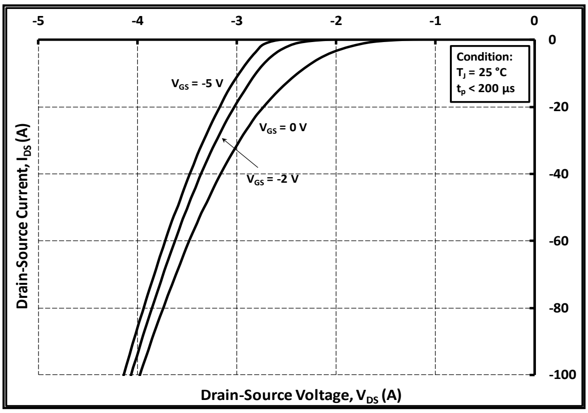


Figure 9. Body Diode Characteristic at 25 °C

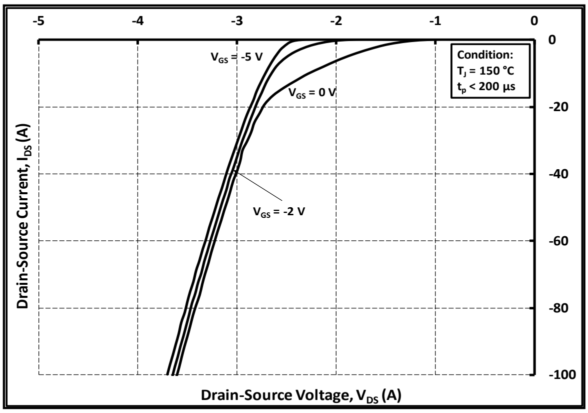


Figure 10. Body Diode Characteristic at 150 °C

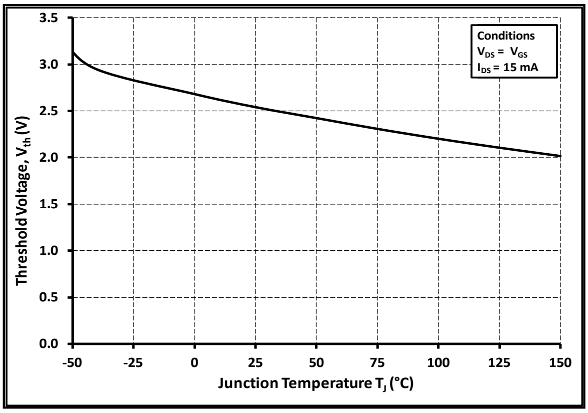


Figure 11. Threshold Voltage vs. Temperature

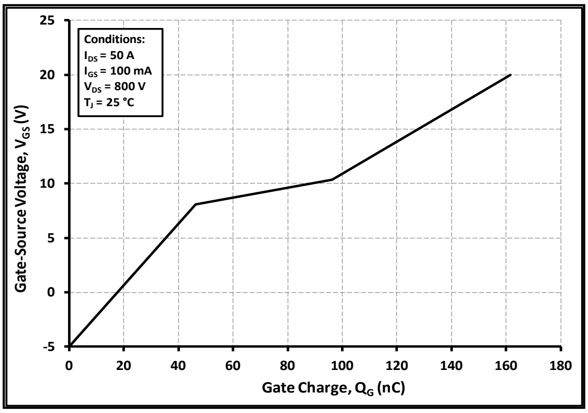
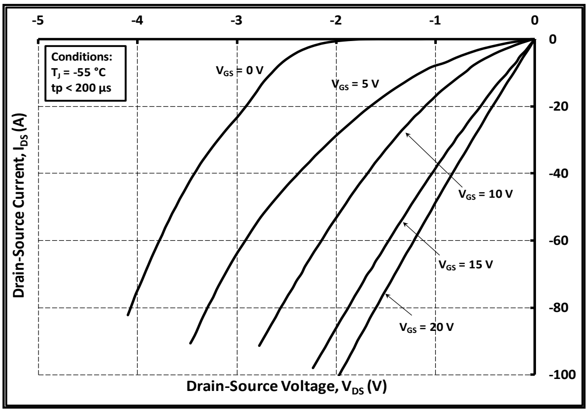


Figure 12. Gate Charge Characteristic

Typical Performance



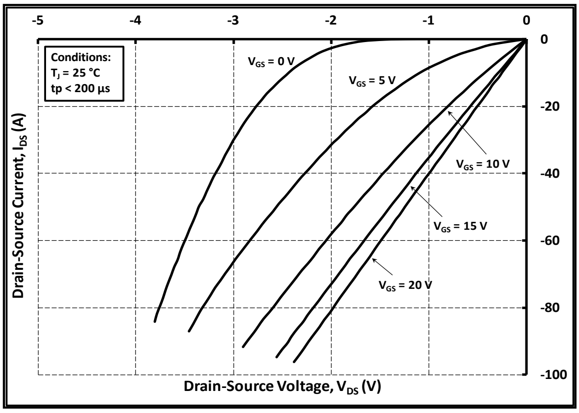
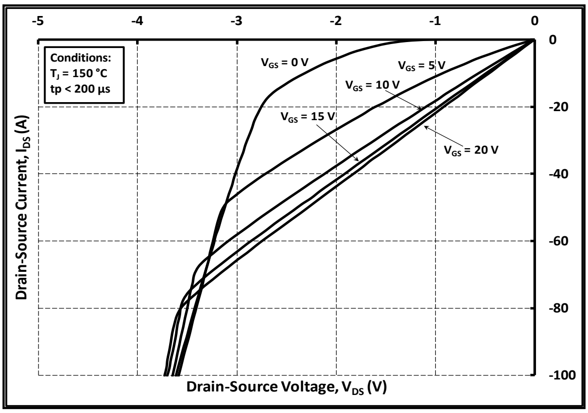


Figure 13. 3rd Quadrant Characteristic at -55 °C

Figure 14. 3rd Quadrant Characteristic at 25 °C



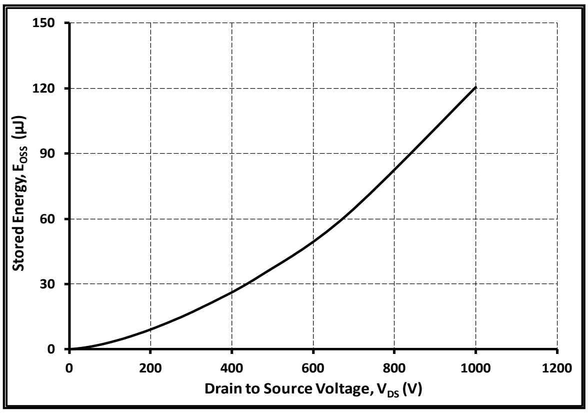
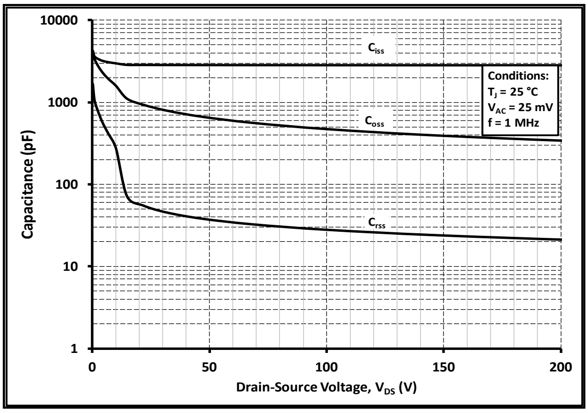


Figure 15. 3rd Quadrant Characteristic at 150 °C

Figure 16. Output Capacitor Stored Energy



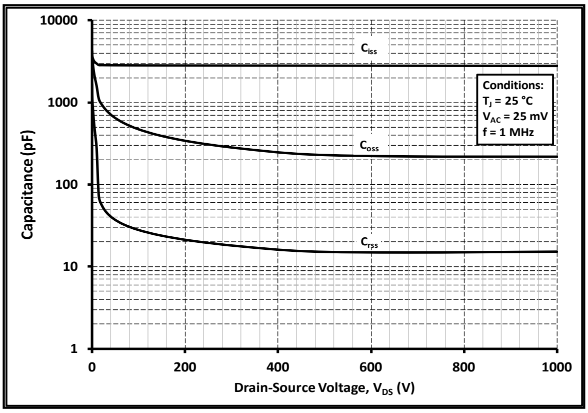


Figure 17. Capacitances vs. Drain-Source Voltage (0-200 V)

Figure 18. Capacitances vs. Drain-Source Voltage (0-1000 V)

Typical Performance

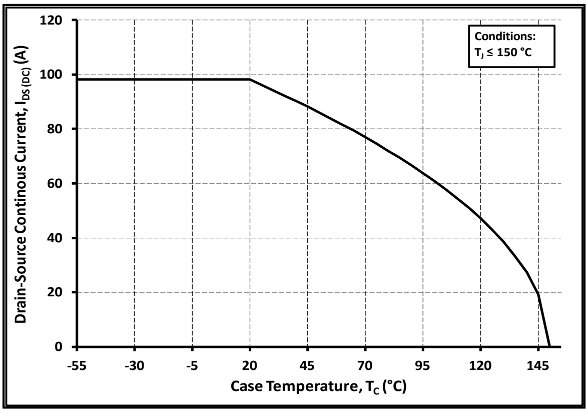


Figure 19. Continuous Drain Current Derating vs. Case Temperature

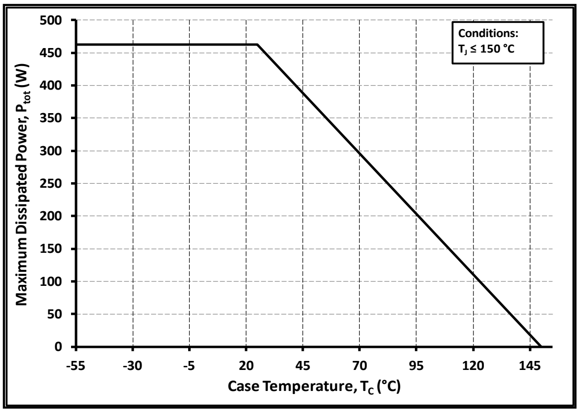


Figure 20. Maximum Power Dissipation Derating vs. Case Temperature

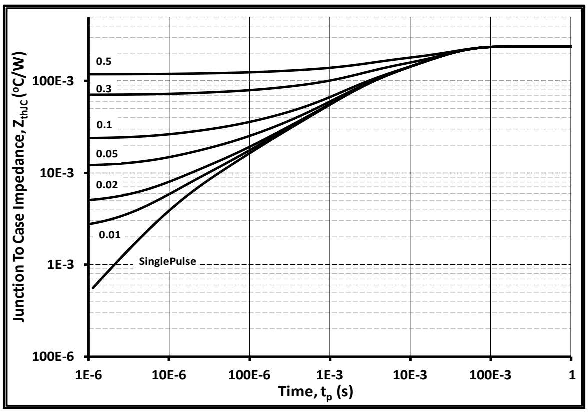


Figure 21. Transient Thermal Impedance (Junction - Case)

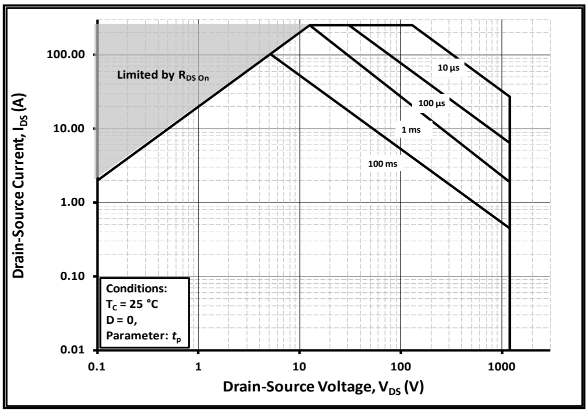


Figure 22. Safe Operating Area

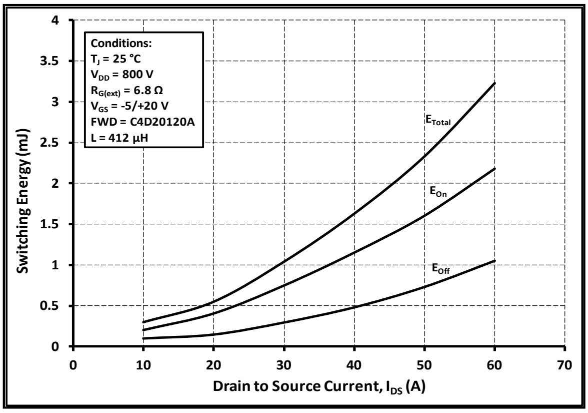


Figure 23. Clamped Inductive Switching Energy vs. Drain Current (V_{DD} = 800V)

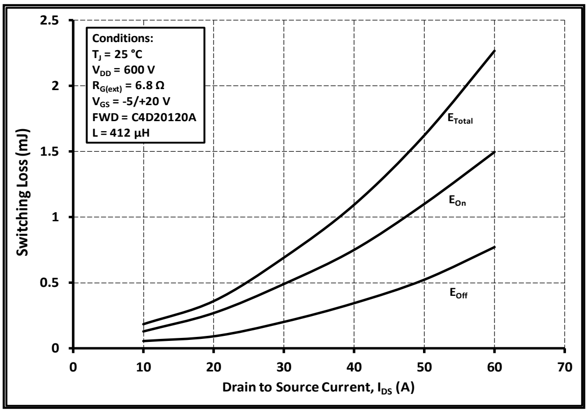


Figure 24. Clamped Inductive Switching Energy vs. Drain Current (V_{DD} = 600V)

Typical Performance

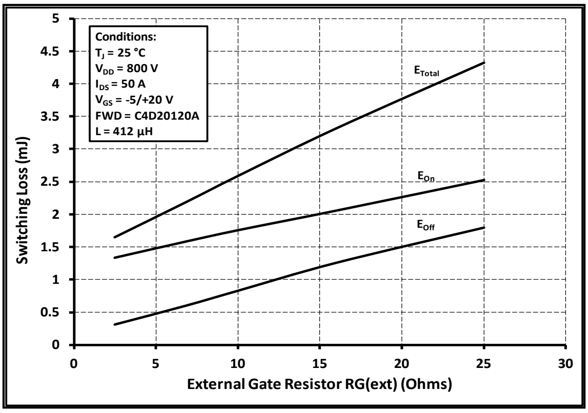


Figure 25. Clamped Inductive Switching Energy vs. $R_{G(ext)}$

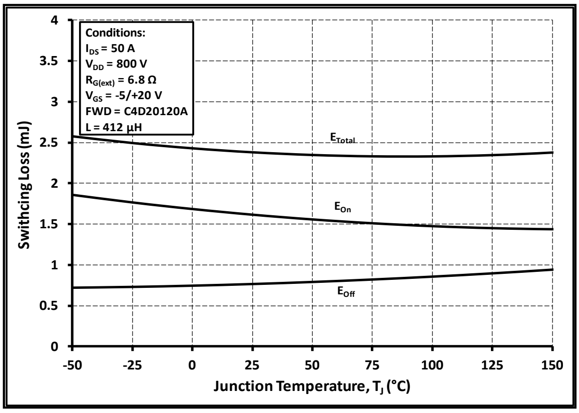


Figure 26. Clamped Inductive Switching Energy vs. Temperature

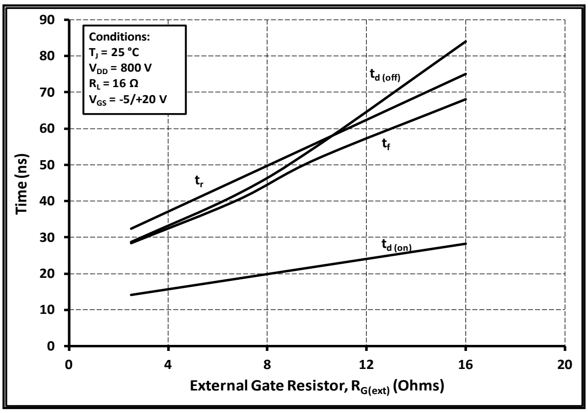
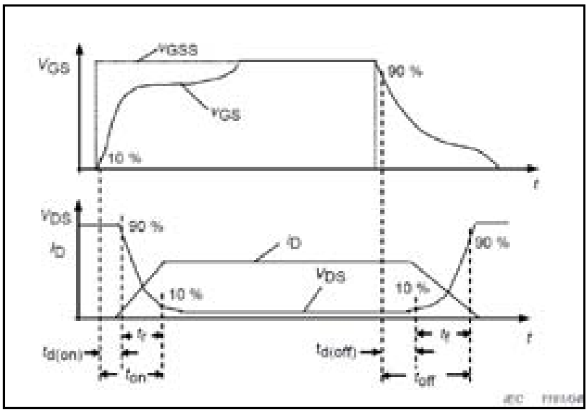


Figure 27. Switching Times vs. $R_{G(ext)}$



V_{GS}
V_{GSS}
V_{GS}
90 %
10 %
t
V_{DS}
I_D
90 %
I_D
V_{DS}
10 %
10 %
90 %
t
$t_{d(on)}$
t_r
t_{on}
$t_{d(off)}$
t_f
t_{off}
IEC

Figure 28. Switching Times Definition

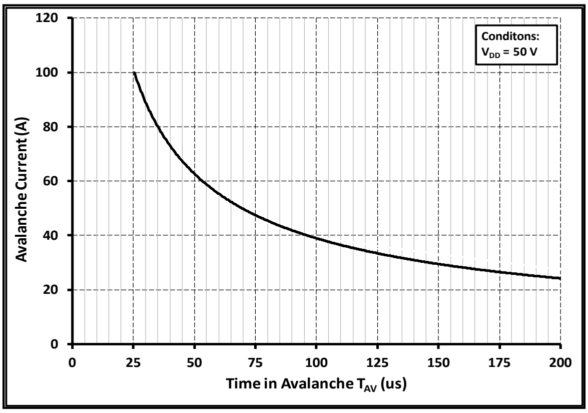
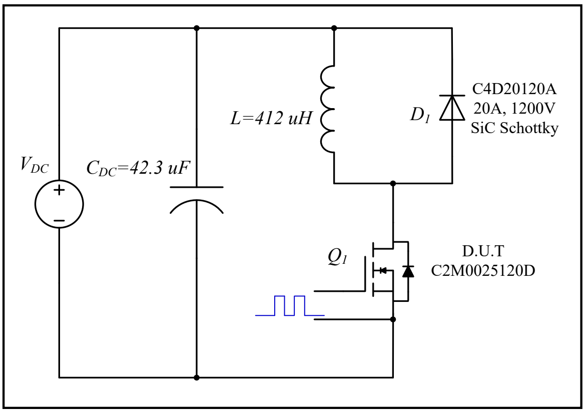


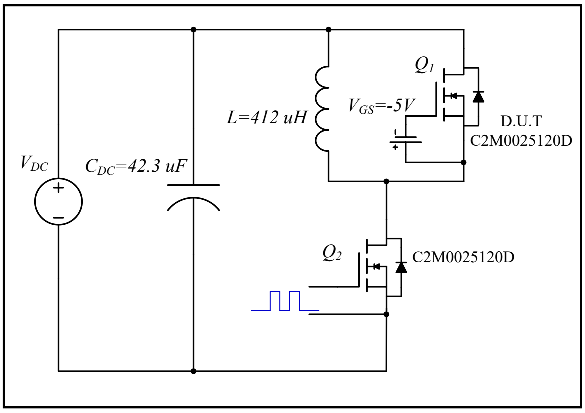
Figure 29. Single Avalanche SOA curve

Test Circuit Schematic



L=412 uH
D1
C4D20120A
20A, 1200V
SiC Schottky
VDC
+
–
CDC=42.3 uF
Q1
D.U.T
C2M0025120D

Figure 30. Clamped Inductive Switching Waveform Test Circuit



Q1
VGS=-5V
L=412 uH
D.U.T
C2M0025120D
VDC
+
–
CDC=42.3 uF
Q2
C2M0025120D

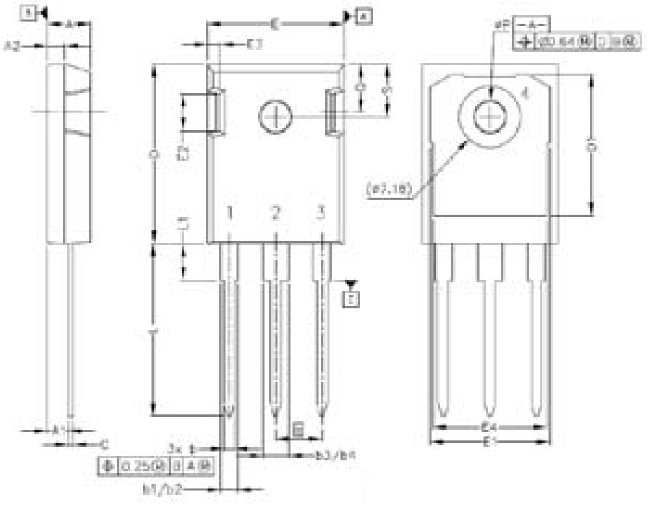
Figure 31. Body Diode Recovery Test Circuit

ESD Ratings

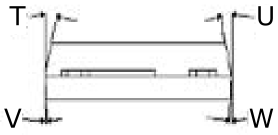
ESD Test	Total Devices Sampled	Resulting Classification
ESD-HBM	All Devices Passed 1000V	2 (>2000V)
ESD-MM	All Devices Passed 400V	C (>400V)
ESD-CDM	All Devices Passed 1000V	IV (>1000V)

Package Dimensions

Package TO-247-3



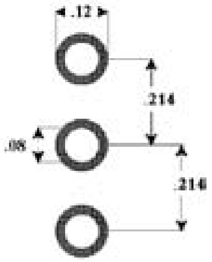
POS	Inches		Millimeters	
	Min	Max	Min	Max
A	.190	.205	4.83	5.21
A1	.090	.100	2.29	2.54
A2	.075	.085	1.91	2.16
b	.042	.052	1.07	1.33
b1	.075	.095	1.91	2.41
b2	.075	.085	1.91	2.16
b3	.113	.133	2.87	3.38
b4	.113	.123	2.87	3.13
c	.022	.027	0.55	0.68
D	.819	.831	20.80	21.10
D1	.640	.695	16.25	17.65
D2	.037	.049	0.95	1.25
E	.620	.635	15.75	16.13
E1	.516	.557	13.10	14.15
E2	.145	.201	3.68	5.10
E3	.039	.075	1.00	1.90
E4	.487	.529	12.38	13.43
e	.214 BSC		5.44 BSC	
N	3		3	
L	.780	.800	19.81	20.32
L1	.161	.173	4.10	4.40
ØP	.138	.144	3.51	3.65
Q	.216	.236	5.49	6.00
S	.238	.248	6.04	6.30
T	9°	11°	9°	11°
U	9°	11°	9°	11°
V	2°	8°	2°	8°
W	2°	8°	2°	8°



Pinout Information:

- Pin 1 = Gate
- Pin 2, 4 = Drain
- Pin 3 = Source

Recommended Solder Pad Layout



TO-247-3

Part Number	Package	Marking
C2M0025120D	TO-247-3	C2M0025120

Notes

- **RoHS Compliance**
  The levels of RoHS restricted materials in this product are below the maximum concentration values (also referred to as the threshold limits) permitted for such substances, or are used in an exempted application, in accordance with EU Directive 2011/65/EC (RoHS2), as implemented January 2, 2013. RoHS Declarations for this product can be obtained from your Cree representative or from the Product Documentation sections of www.cree.com.

- **REACh Compliance**
  REACh substances of high concern (SVHCs) information is available for this product. Since the European Chemical Agency (ECHA) has published notice of their intent to frequently revise the SVHC listing for the foreseeable future,please contact a Cree representative to insure you get the most up-to-date REACh SVHC Declaration. REACh banned substance information (REACh Article 67) is also available upon request.

- This product has not been designed or tested for use in, and is not intended for use in, applications implanted into the human body nor in applications in which failure of the product could lead to death, personal injury or property damage, including but not limited to equipment used in the operation of nuclear facilities, life-support machines, cardiac defibrillators or similar emergency medical equipment, aircraft navigation or communication or control systems, air traffic control systems.

Related Links

- **C2M PSPICE Models: http://wolfspeed.com/power/tools-and-support**
- **SiC MOSFET Isolated Gate Driver reference design: http://wolfspeed.com/power/tools-and-support**
- **SiC MOSFET Evaluation Board: http://wolfspeed.com/power/tools-and-support**

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A.2 GaN HEMTs

Table A2: Comparison of different manufacturers GaN Enchancement Mode HEMTs at 25 °C.

Device	$V_{DS,max}$	I_D	$R_{ds,on}$
GaN Systems GS66504B	650 V	15 A	100 $m\Omega$
GaN Systems GS66516B	650 V	60 A	25 $m\Omega$
GaN Systems GS-065-120-1-D Die	650 V	120 A	12 $m\Omega$
EPC2050	350 V	6.3 A	65 $m\Omega$
EPC2034	200 V	48 A	10 $m\Omega$
GaN Systems GS61008P	100 V	90 A	7 $m\Omega$
GaN Systems GS-010-120-1-P	100 V	120 A	5 $m\Omega$
EPC2022	100 V	90 A	3.2 $m\Omega$

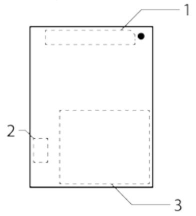
GS66504B
Bottom-side cooled 650 V E-mode GaN transistor
Preliminary Datasheet

Features

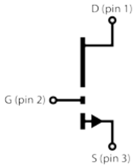
- 650 V enhancement mode power switch
- Bottom-side cooled configuration
- $R_{DS(on)}$ = 100 mΩ
- $I_{DS(max)}$ = 15 A
- Ultra-low FOM Island Technology® die
- Low inductance GaN*PX*® package
- Easy gate drive requirements (0 V to 6 V)
- Transient tolerant gate drive (-20 V / +10 V)
- Very high switching frequency (> 100 MHz)
- Fast and controllable fall and rise times
- Reverse current capability
- Zero reverse recovery loss
- Small 5.0 x 6.6 mm² PCB footprint
- RoHS 6 compliant

GaN
GS66504B
(e4)

Package Outline



Circuit Symbol



Applications

- High efficiency power conversion
- High density power conversion
- AC-DC Converters
- Bridgeless Totem Pole PFC
- ZVS Phase Shifted Full Bridge
- Half Bridge topologies
- Synchronous Buck or Boost
- Uninterruptable Power Supplies
- Industrial Motor Drives
- Single and 3Φ inverter legs
- Solar and Wind Power
- Fast Battery Charging
- Class D Audio amplifiers
- DC-DC converters
- On Board Battery Chargers
- Traction Drive

Description

The GS66504B is an enhancement mode GaN-on-silicon power transistor. The properties of GaN allow for high current, high voltage breakdown and high switching frequency. GaN Systems implements patented **Island Technology®** cell layout for high-current die performance & yield. **GaN*PX*®** packaging enables low inductance & low thermal resistance in a small package. The GS66504B is a bottom-side cooled transistor that offers very low junction-to-case thermal resistance for demanding high power applications. These features combine to provide very high efficiency power switching.

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Absolute Maximum Ratings (T_{case} = 25 °C except as noted)

Parameter	Symbol	Value	Unit
Operating Junction Temperature	T_J	-55 to +150	°C
Storage Temperature Range	T_S	-55 to +150	°C
Drain-to-Source Voltage	V_{DS}	650	V
Drain-to-Source Voltage - transient (note 1)	$V_{DS(transient)}$	750	V
Gate-to-Source Voltage	V_{GS}	-10 to +7	V
Gate-to-Source Voltage - transient (note 1)	$V_{GS(transient)}$	-20 to +10	V
Continuous Drain Current (T_{case} = 25 °C) (note 2)	I_{DS}	15	A
Continuous Drain Current (T_{case} = 100 °C) (note 2)	I_{DS}	12.5	A
Pulse Drain Current (Pulse width 100 µs)	$I_{DS\ Pulse}$	36	A

(1) Pulse $\leq$ 1 µs

(2) Limited by saturation

Thermal Characteristics (Typical values unless otherwise noted)

Parameter	Symbol	Value	Units
Thermal Resistance (junction-to-case) – bottom side	$R_{\Theta JC}$	1.0	°C /W
Thermal Resistance (junction-to-top)	$R_{\Theta JT}$	17	°C /W
Thermal Resistance (junction-to-ambient) (note 3)	$R_{\Theta JA}$	28	°C /W
Maximum Soldering Temperature (MSL3 rated)	T_{SOLD}	260	°C

(3) Device mounted on 1.6 mm PCB thickness FR4, 4-layer PCB with 2 oz. copper on each layer. The recommendation for thermal vias under the thermal pad are 0.3 mm diameter (12 mil) with 0.635 mm pitch (25 mil). The copper layers under the thermal pad and drain pad are 25 x 25 mm^2 each. The PCB is mounted in horizontal position without air stream cooling.

Ordering Information

Ordering code	Package type	Packing method	Qty	Reel Diameter	Reel Width
GS66504B-TR	GaN*PX*® Bottom-Side Cooled	Tape-and-Reel	3000	13” (330mm)	16mm
GS66504B-MR	GaN*PX*® Bottom-Side Cooled	Mini-Reel	250	7” (180mm)	16mm

Electrical Characteristics (Typical values at T_J = 25 °C, V_{GS} = 6 V unless otherwise noted)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Drain-to-Source Blocking Voltage	BV_{DS}	650			V	V_{GS} = 0 V I_{DSS} = 25 µA
Drain-to-Source On Resistance	$R_{DS(on)}$		100	130	mΩ	V_{GS} = 6 V, T_J = 25 °C I_{DS} = 4.5 A
Drain-to-Source On Resistance	$R_{DS(on)}$		258		mΩ	V_{GS} = 6 V T_J = 150 °C I_{DS} = 4.5 A
Gate-to-Source Threshold	$V_{GS(th)}$	1.1	1.3		V	V_{DS} = V_{GS} I_{DS} = 3.5 mA
Gate-to-Source Current	I_{GS}		80		µA	V_{GS} = 6 V, V_{DS} = 0 V
Gate Plateau Voltage	V_{plat}		3		V	V_{DS} = 400 V I_{DS} = 15 A
Drain-to-Source Leakage Current	I_{DSS}		1	25	µA	V_{DS} = 650 V V_{GS} = 0 V T_J = 25 °C
Drain-to-Source Leakage Current	I_{DSS}		200		µA	V_{DS} = 650 V V_{GS} = 0 V T_J = 150 °C
Internal Gate Resistance	R_G		1.36		Ω	f = 25MHz, open drain
Input Capacitance	C_{ISS}		130		pF	V_{DS} = 400 V V_{GS} = 0 V f = 1 MHz
Output Capacitance	C_{OSS}		33		pF	
Reverse Transfer Capacitance	C_{RSS}		1		pF	
Effective Output Capacitance, Energy Related (Note 4)	$C_{O(ER)}$		44		pF	V_{GS} = 0 V V_{DS} = 0 to 400 V
Effective Output Capacitance, Time Related (Note 5)	$C_{O(TR)}$		71		pF	
Total Gate Charge	Q_G		3.0		nC	V_{GS} = 0 to 6 V V_{DS} = 400 V
Gate-to-Source Charge	Q_{GS}		1.1		nC	
Gate-to-Drain Charge	Q_{GD}		0.84		nC	
Output Charge	Q_{OSS}		28.3		nC	V_{GS} = 0 V V_{DS} = 400 V
Reverse Recovery Charge	Q_{RR}		0		nC	

(4) $C_{O(ER)}$ is the fixed capacitance that would give the same stored energy as C_{OSS} while V_{DS} is rising from 0 V to the stated V_{DS}

(5) $C_{O(TR)}$ is the fixed capacitance that would give the same charging time as C_{OSS} while V_{DS} is rising from 0 V to the stated V_{DS}.

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Electrical Performance Graphs

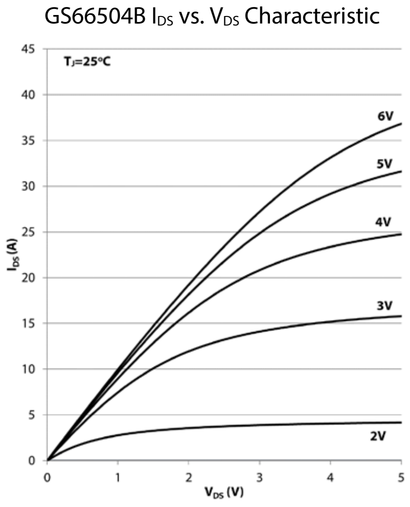

Figure 1: Typical I_{DS} vs. V_{DS} @ $T_J = 25\ ^0C$

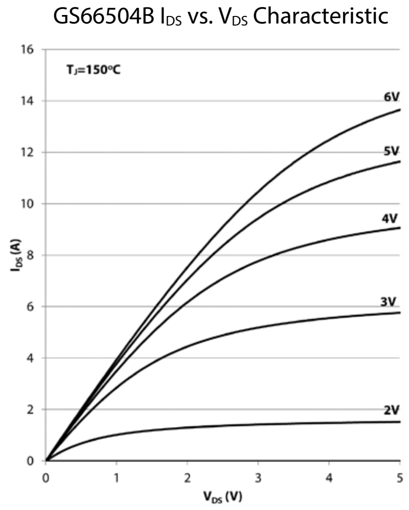

Figure 2: Typical I_{DS} vs. V_{DS} @ $T_J = 150\ ^0C$

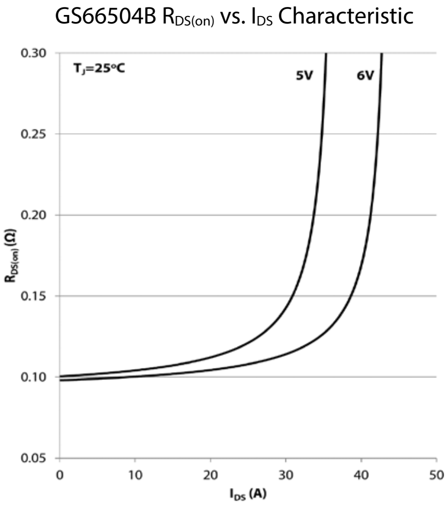

Figure 3: $R_{DS(on)}$ vs. I_{DS} at $T_J = 25\ ^0C$

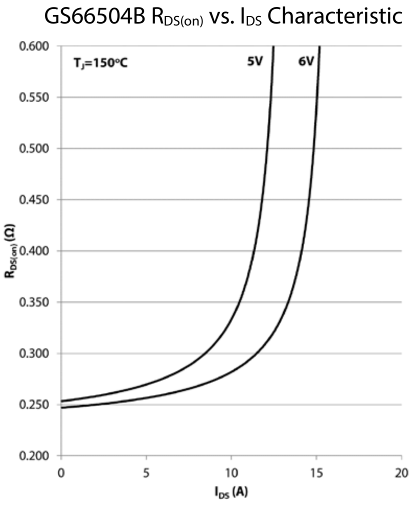

Figure 4: $R_{DS(on)}$ vs. I_{DS} at $T_J = 150\ ^0C$

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Electrical Performance Graphs

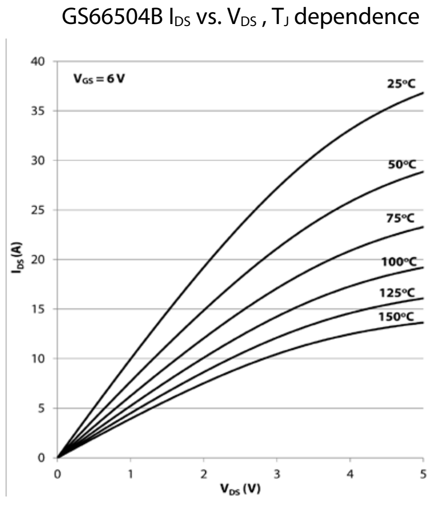

Figure 5: Typical I_{DS} vs. V_{DS} @ V_{GS} = 6 V

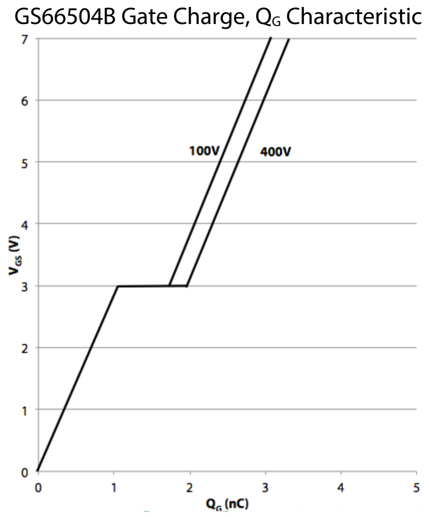

Figure 6: Typical V_{GS} vs. Q_G @ V_{DS} = 100, 400 V

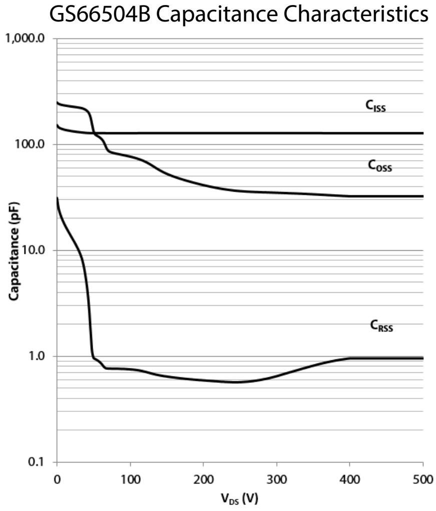

Figure 7: Typical C_{ISS}, C_{OSS}, C_{RSS} vs. V_{DS}

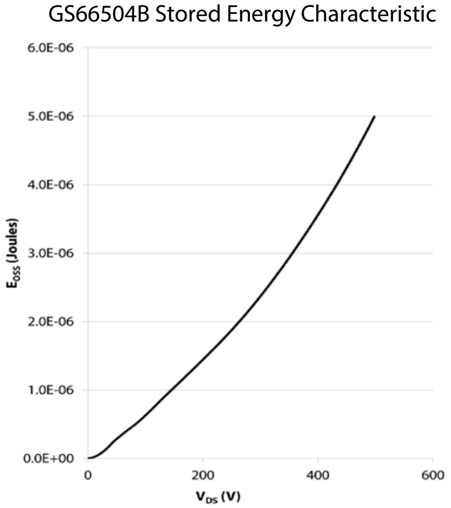

Figure 8: Typical C_{OSS} Stored Energy

This information pertains to a product under development. Its characteristics and specifications are subject to change without notice.

Electrical Performance Graphs

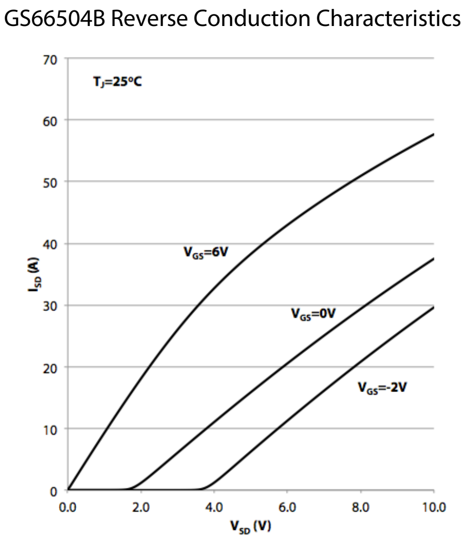
GS66504B Reverse Conduction Characteristics

Figure 9: Typical I_{SD} vs. V_{SD}

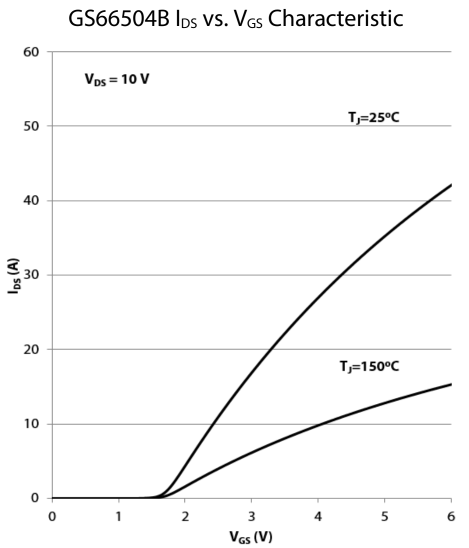
GS66504B I_{DS} vs. V_{GS} Characteristic

Figure 10: Typical I_{DS} vs. V_{GS}

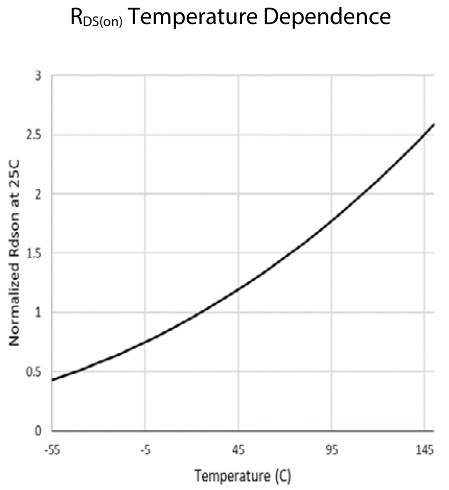
$R_{DS(on)}$ Temperature Dependence

Figure 11: Normalized $R_{DS(on)}$ as a function of T_J

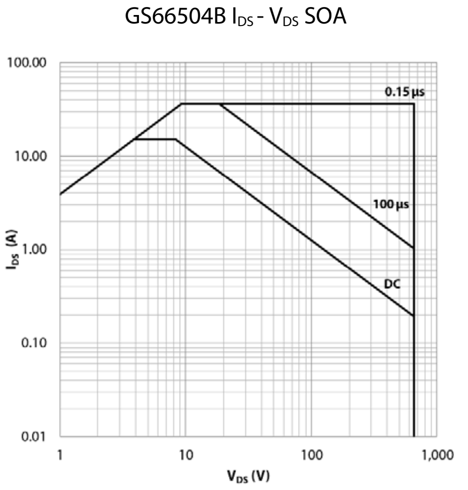
GS66504B I_{DS} - V_{DS} SOA

Figure 12: Safe Operating Area @ T_{case} = 25 °C

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Thermal Performance Graphs

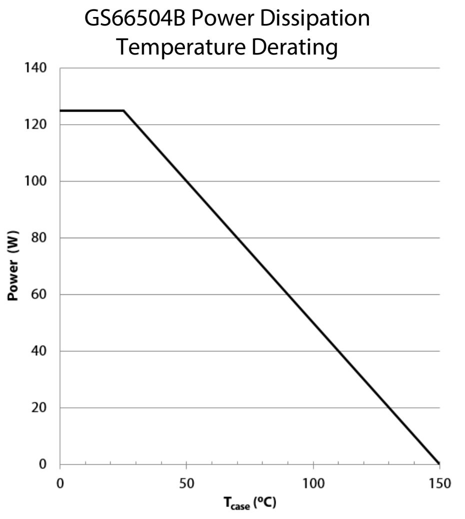

Figure 13: Power Derating vs. T_{case}

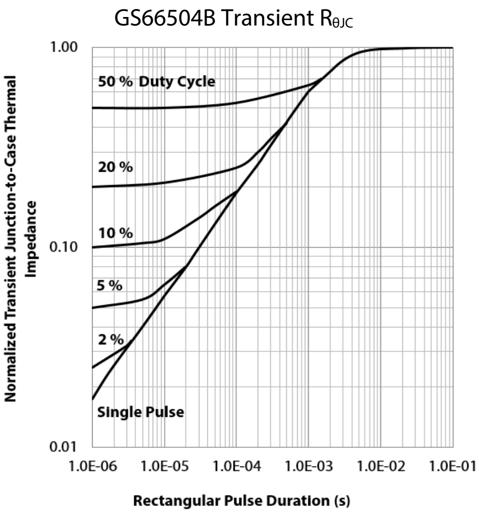

Figure 14: Transient Thermal Impedance
1.00 = Nominal DC thermal impedance

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Application Information

Gate Drive

The recommended gate drive voltage is 0 V to + 6 V for optimal $R_{DS(on)}$ performance and long life. The absolute maximum gate to source voltage rating is specified to be +7.0 V maximum DC. The gate drive can survive transients up to +10 V and – 20 V for pulses up to 1 µs. These specifications allow designers to easily use 6.0 V or even 6.5 V gate drive settings. At 6 V gate drive voltage, the enhancement mode high electron mobility transistor (E-HEMT) is fully enhanced and reaches its optimal efficiency point. A 5 V gate drive can be used but may result in lower operating efficiency. Inherently, GaN Systems E-HEMT do not require negative gate bias to turn off. Negative gate bias ensures safe operation against the voltage spike on the gate, however it increases the reverse conduction loss. For more details, please refer to the gate driver application note "GN001 How to Drive GaN Enhancement Mode Power Switching Transistors" which can be found at www.gansystems.com.

Similar to a silicon MOSFET, an external gate resistor can be used to control the switching speed and slew rate. Adjusting the resistor to achieve the desired slew rate may be needed. Lower turn-off gate resistance, $R_{G(OFF)}$ is recommended for better immunity to cross conduction. Please see the gate driver application note (GN001) for more details.

A standard MOSFET driver can be used as long as it supports 6 V for gate drive and the UVLO is suitable for 6 V operation. Gate drivers with low impedance and high peak current are recommended for fast switching speed. GaN Systems E-HEMTs have significantly lower Q_G when compared to equally sized $R_{DS(on)}$ MOSFETs, so high speed can be reached with smaller and lower cost gate drivers.

Some non-isolated half bridge MOSFET drivers are not compatible with 6 V gate drive due to their high under-voltage lockout threshold. Also, a simple bootstrap method for high side gate drive will not be able to provide tight tolerance on the gate voltage. Therefore, special care should be taken when you select and use the half bridge drivers. Please see the gate driver application note (GN001) for more details.

Parallel Operation

Design wide tracks or polygons on the PCB to distribute the gate drive signals to multiple devices. Keep the drive loop length to each device as short and equal length as possible.

GaN enhancement mode HEMTs have a positive temperature coefficient on-state resistance which helps to balance the current. However, special care should be taken in the driver circuit and PCB layout since the device switches at very fast speed. It is recommended to have a symmetric PCB layout and equal gate drive loop length (star connection if possible) on all parallel devices to ensure balanced dynamic current sharing. Adding a small gate resistor (1-2 Ω) on each gate is strongly recommended to minimize the gate parasitic oscillation.

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Source Sensing

Although the GS66504B does not have a dedicated source sense pin, the GaN*PX*® packaging utilizes no wire bonds so the source connection is already very low inductance. By simply using a dedicated "source sense" connection with a PCB trace from the gate driver output ground to the Source pad in a kelvin configuration with respect to the gate drive signal, the function can easily be implemented. It is recommended to implement a "source sense" connection to improve drive performance.

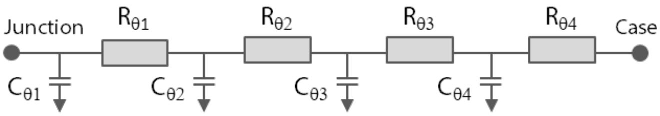
Thermal

The substrate is internally connected to the thermal pad and to the Source pad on the bottom side of the GS61004B. The transistor is designed to be cooled using the printed circuit board. The Drain pad is not as thermally conductive as the thermal pad. However, adding more copper under the Drain will improve thermal performance by reducing the package temperature.

Thermal Modeling

RC thermal models are available for customers that wish to perform detailed thermal simulation using SPICE. The thermal models are created using the Cauer model, an RC network model that reflects the real physical property and packaging structure of our devices. This approach allows our customers to extend the thermal model to their system by adding extra R_θ and C_θ to simulate the Thermal Interface Material (TIM) or Heatsink.

GS66504B RC thermal model:



RC breakdown of $R_{\Theta JC}$

R_θ (°C/W)	C_θ (W·s/°C)
$R_{\theta 1} = 0.03$	$C_{\theta 1} = 4.0E\text{-}05$
$R_{\theta 2} = 0.46$	$C_{\theta 2} = 3.7E\text{-}04$
$R_{\theta 3} = 0.48$	$C_{\theta 3} = 3.25E\text{-}03$
$R_{\theta 4} = 0.03$	$C_{\theta 4} = 1.0E\text{-}03$

For more detail, please refer to Application Note GN007 "Modeling Thermal Behavior of GaN Systems' GaN*PX*™ Using RC Thermal SPICE Models" available at www.gansystems.com

Reverse Conduction

GaN Systems enhancement mode HEMTs do not need an intrinsic body diode and there is zero reverse recovery charge. The devices are naturally capable of reverse conduction and exhibit different characteristics depending on the gate voltage. Anti-parallel diodes are not required for GaN Systems transistors as is the case for IGBTs to achieve reverse conduction performance.

This information pertains to a product under development. Its characteristics and specifications are subject to change without notice.

On-state condition ($V_{GS} = +6$ V): The reverse conduction characteristics of a GaN Systems enhancement mode HEMT in the on-state is similar to that of a silicon MOSFET, with the I-V curve symmetrical about the origin and it exhibits a channel resistance, $R_{DS(on)}$, similar to forward conduction operation.
Off-state condition ($V_{GS} \leq 0$ V): The reverse characteristics in the off-state are different from silicon MOSFETs as the GaN device has no body diode. In the reverse direction, the device starts to conduct when the gate voltage, with respect to the drain, V_{GD}, exceeds the gate threshold voltage. At this point the device exhibits a channel resistance. This condition can be modeled as a “body diode” with slightly higher V_F and no reverse recovery charge.

If negative gate voltage is used in the off-state, the source-drain voltage must be higher than $V_{GS(th)}+V_{GS(off)}$ in order to turn the device on. Therefore, a negative gate voltage will add to the reverse voltage drop “V_F” and hence increase the reverse conduction loss.

Blocking Voltage

The blocking voltage rating, $BV_{DS,}$ is defined by the drain leakage current. The hard (unrecoverable) breakdown voltage is approximately 30 % higher than the rated BV_{DS}. As a general practice, the maximum drain voltage should be de-rated in a similar manner as IGBTs or silicon MOSFETs. All GaN E-HEMTs do not avalanche and thus do not have an avalanche breakdown rating. The maximum drain-to-source rating is 650 V and doesn’t change with negative gate voltage. A transient drain-to-source voltage of 750 V for up to 1 µs is acceptable.

Packaging and Soldering

The package material is high temperature epoxy-based PCB material which is similar to FR4 but has a higher temperature rating, thus allowing the GS66504B device to be specified to 150 °C. The device can handle at least 3 reflow cycles.

It is recommended to use the reflow profile in IPC/JEDEC J-STD-020 REV D.1 (March 2008)

The basic temperature profiles for Pb-free (Sn-Ag-Cu) assembly are:

- Preheat/Soak: 60 - 120 seconds. $T_{min} = 150$ °C, $T_{max} = 200$ °C.
- Reflow: Ramp up rate 3 °C/sec, max. Peak temperature is 260 °C and time within 5 °C of peak temperature is 30 seconds.
- Cool down: Ramp down rate 6 °C/sec max.

Using “Non-Clean” soldering paste and operating at high temperatures may cause a reactivation of the “Non-Clean” flux residues. In extreme conditions, unwanted conduction paths may be created. Therefore, when the product operates at greater than 100 °C it is recommended to also clean the “Non-Clean” paste residues.

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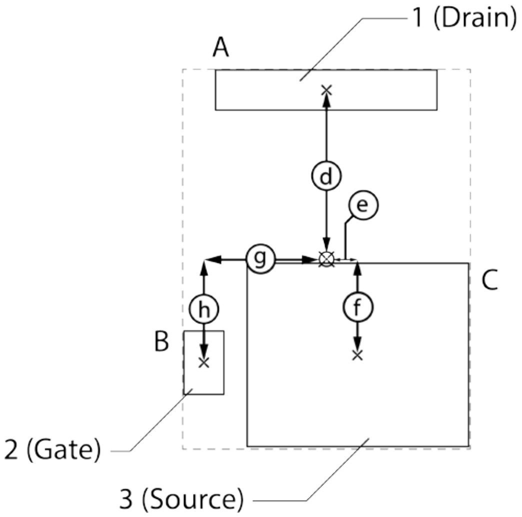
Recommended PCB Footprint for GS66504B



Pad sizes

	mm		Inches	
	X (width)	Y (height)	X (width)	Y (height)
A	3.86	0.70	0.152	0.028
B	0.70	1.10	0.028	0.043
C	3.86	3.17	0.152	0.125

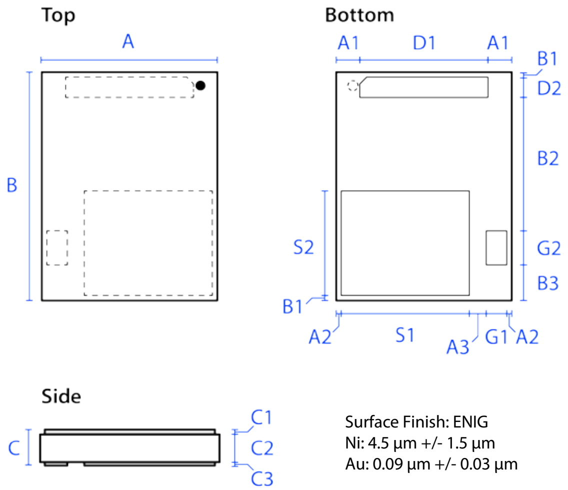
Dimensions

	mm	Inches
d	2.91	0.115
e	0.55	0.022
f	1.67	0.066
g	2.13	0.084
h	1.81	0.071

☐ PCB pad opennings

⬚ Package outline

Package Dimensions

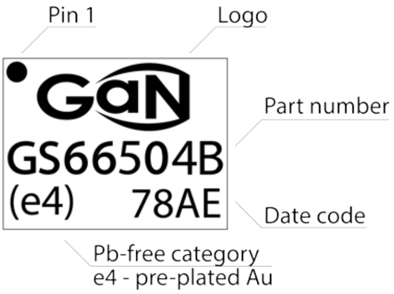

Top
A
B
Bottom
A1
D1
A1
B1
D2
B2
S2
G2
B3
B1
A2
S1
A3
G1
A2
Side
C
C1
C2
C3

Surface Finish: ENIG
Ni: 4.5 µm +/- 1.5 µm
Au: 0.09 µm +/- 0.03 µm

	mm	Inches	
A	5.01	0.197	± 0.10 mm (0.004”)
A1	0.625	0.025	± 0.05 mm (0.002”)
A2	0.075	0.003	± 0.05 mm (0.002”)
A3	0.50	0.020	
B	6.56	0.258	± 0.10 mm (0.004”)
B1	0.075	0.003	± 0.05 mm (0.002”)
B2	3.91	0.154	
B3	0.975	0.038	± 0.05 mm (0.002”)
C	0.51	0.0201	± 0.05 mm (0.002”)
C1	0.045	0.0018	
C2	0.45	0.0177	
C3	0.015	0.0006	
D1	3.76	0.148	
D2	0.60	0.024	
G1	0.60	0.024	
G2	1.00	0.039	
S1	3.76	0.148	
S2	3.07	0.121	

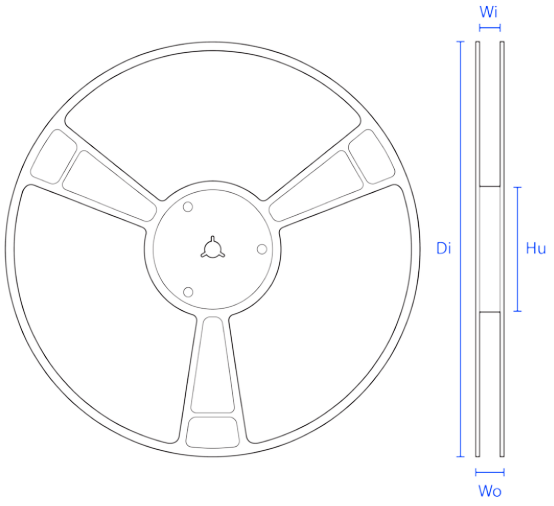
Note: Inch measurements are approximate values

GaN*PX*® Part Marking


Pin 1
Logo
GaN
GS66504B
(e4) 78AE
Part number
Date code
Pb-free category
e4 - pre-plated Au

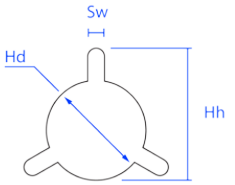
This information pertains to a product under development. Its characteristics and specifications are subject to change without notice.

GS660504B GaN*PX*® Tape and Reel Information

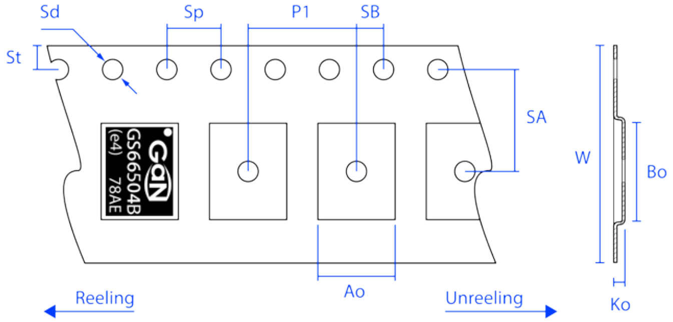


Dimensions (mm)

	13″ reel (330 mm)		7″ mini-reel (180 mm)	
	Nominal	Tolerance	Nominal	Tolerance
Di	330.0	+/- 1.5	180.0	+1.5 / - 2.0
Wo	22.4	MAX	22.4	MAX
Wi	16.4	+ 2.0 / - 0.0	16.4	+ 2.0 / - 0.1
Hu	100.0	+/- 1.5	60.0	+ 2.0 / - 0.0
Hh	17.2	+/- 0.2	17.0	+/- 0.8
Sw	2.2	+/- 0.2	2.0	+/- 0.5
Hd	13.0	+ 0.5 / - 0.2	13.1	+/- 0.3



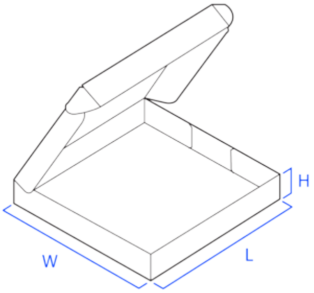
Note: Wo and Wi measured at hub


Sd
Sp
P1
SB
St
SA
GaN
GS66504B
(e4) 78AE
W
Bo
Ko
Ao
Reeling
Unreeling

Dimensions (mm)

	Nominal	Tolerance
P1	8.00	+/- 0.1
W	16.00	+ 0.3 / - 0.1
Ko	0.70	+/- 0.1
Ao	5.70	+/- 0.1
Bo	7.10	+/- 0.1
Sp	4.00	+/- 0.02
Sd	1.50	+ 0.1 / - 0.0
St	1.75	+/- 0.1
SA	7.50	+/- 0.1
SB	2.00	+/- 0.1

Tape and Reel Box Dimensions



Outside dimensions (mm)

	7" mini-reel	13" tape-reel
W	197	342
L	204	355
H	32	53

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A.3 SiC Schotty Diodes

Table A3: Comparison of different manufacturers SiC Schottky diodes at 25 °C.

Device	$V_{r,max}$	I_f
Cree C3D25170H	1700 V	25 A
Cree C4D40120D	1200 V	40 A
Cree C4D30120D	1200 V	30 A
Rohm SCS240KE2AHR	1200 V	40 A
USCi UJ3D1250K	1200 V	50 A
Cree C5D50065D	650 V	50 A
Rohm SCS320AM	650 V	20 A
Rohm SCS240AE2	650 V	40 A
USCi UJ3D06504	650 V	4 A
USCi UJ3D06560KS	650 V	60 A
Cree C3D20060D	600 V	20 A

C4D30120D

Silicon Carbide Schottky Diode

Z-REC® RECTIFIER

V_{RRM} = 1200 V
I_F (T_C=135°C) = 43A**
Q_c = 155nC**

Features

- 1.2kV Schottky Rectifier
- Zero Reverse Recovery Current
- High-Frequency Operation
- Temperature-Independent Switching
- Extremely Fast Switching

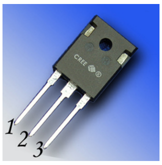
Benefits

- Replace Bipolar with Unipolar Rectifiers
- Essentially No Switching Losses
- Higher Efficiency
- Reduction of Heat Sink Requirements
- Parallel Devices Without Thermal Runaway

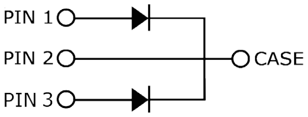
Applications

- Switch Mode Power Supplies (SMPS)
- Boost diodes in PFC or DC/DC stages
- Free Wheeling Diodes in Inverter stages
- AC/DC converters

Package



TO-247-3



Part Number	Package	Marking
C4D30120D	TO-247-3	C4D30120

Maximum Ratings (T_C=25°C unless otherwise specified)

Symbol	Parameter	Value	Unit	Test Conditions	Note
V_{RRM}	Repetitive Peak Reverse Voltage	1200	V		
V_{RSM}	Surge Peak Reverse Voltage	1300	V		
V_R	DC Peak Reverse Voltage	1200	V		
I_F	Continuous Forward Current (Per Leg/Device)	44/88 21.5/43 15/30	A	T_C=25°C T_C=135°C T_C=152°C	Fig. 3
I_{FRM}	Repetitive Peak Forward Surge Current	68* 44*	A	T_C=25°C, t_P=10 ms, Half Sine Pulse T_C=110°C, t_P=10 ms, Half Sine Pulse	
I_{FSM}	Non-Repetitive Forward Surge Current	100* 85*	A	T_C=25°C, t_P=10 ms, Half Sine Pulse T_C=110°C, t_P=10 ms, Half Sine Pulse	Fig. 8
$I_{F,Max}$	Non-Repetitive Peak Forward Current	900* 750*	A	T_C=25°C, t_P=10 µs, Pulse T_C=110°C, t_P=10 µs, Pulse	Fig. 8
P_{tot}	Power Dissipation (Per Leg/Device)	220/440 95/190	W	T_C=25°C T_C=110°C	Fig. 4
dV/dt	Diode dV/dt ruggedness	200	V/ns	V_R=0-960V	
$\int i^2dt$	i^2t value	50* 36*	A^2s	T_C=25°C, t_P=10 ms T_C=110°C, t_P=10 ms	
T_J	Operating Junction Range	-55 to +175	°C		
T_{stg}	Storage Temperature Range	-55 to +135	°C		
	TO-247 Mounting Torque	1 8.8	Nm lbf-in	M3 Screw 6-32 Screw	

* Per Leg, ** Per Device

Electrical Characteristics (Per Leg)

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
V_F	Forward Voltage	1.6 2.3	1.8 3	V	I_F = 15 A T_J=25°C I_F = 15 A T_J=175°C	Fig. 1
I_R	Reverse Current	35 120	200 300	μA	V_R = 1200 V T_J=25°C V_R = 1200 V T_J=175°C	Fig. 2
Q_C	Total Capacitive Charge	77.5		nC	V_R = 800 V, I_F = 15A di/dt = 200 A/μs T_J = 25°C	Fig. 5
C	Total Capacitance	1200 70 50		pF	V_R = 0 V, T_J = 25°C, f = 1 MHz V_R = 400 V, T_J = 25°C, f = 1 MHz V_R = 800 V, T_J = 25°C, f = 1 MHz	Fig. 6
E_C	Capacitance Stored Energy	22.1		μJ	V_R = 800 V	Fig. 7

Note:This is a majority carrier diode, so there is no reverse recovery charge.

Thermal Characteristics

Symbol	Parameter	Typ.	Unit	Note
$R_{\theta JC}$	Thermal Resistance from Junction to Case	0.34** 0.68*	°C/W	Fig. 9

** Per Device, * Per Leg

Typical Performance (Per Leg)

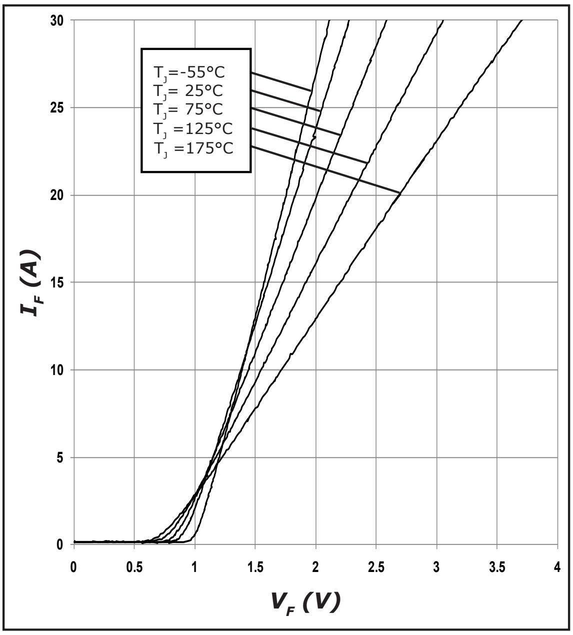


Figure 1. Forward Characteristics

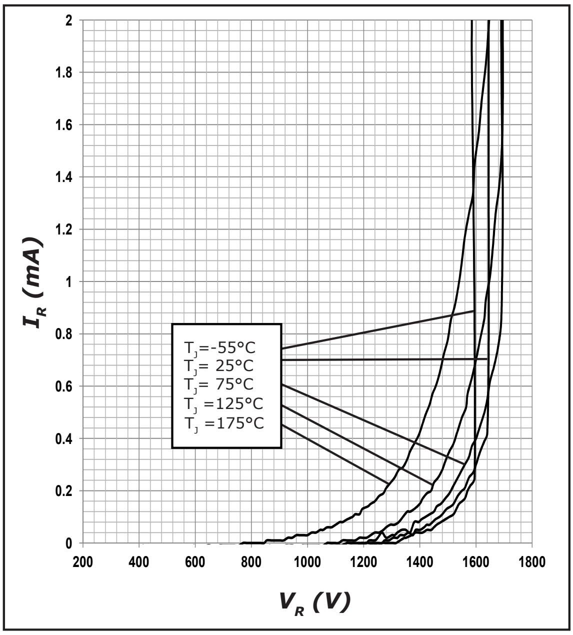


Figure 2. Reverse Characteristics

Typical Performance (Per Leg)

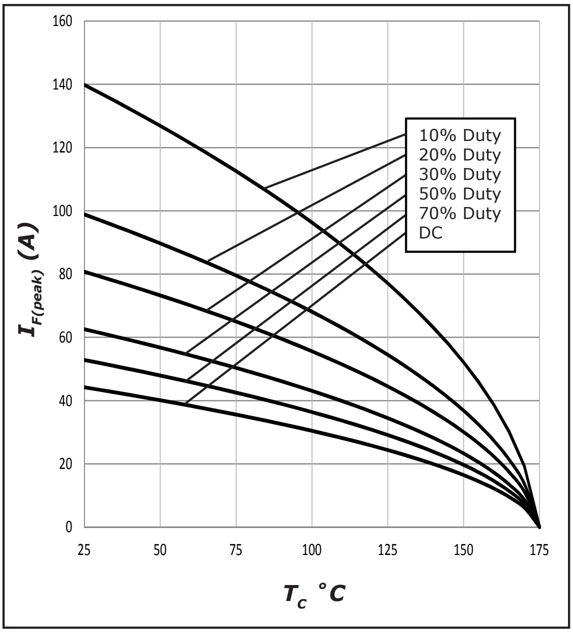


Figure 3. Current Derating

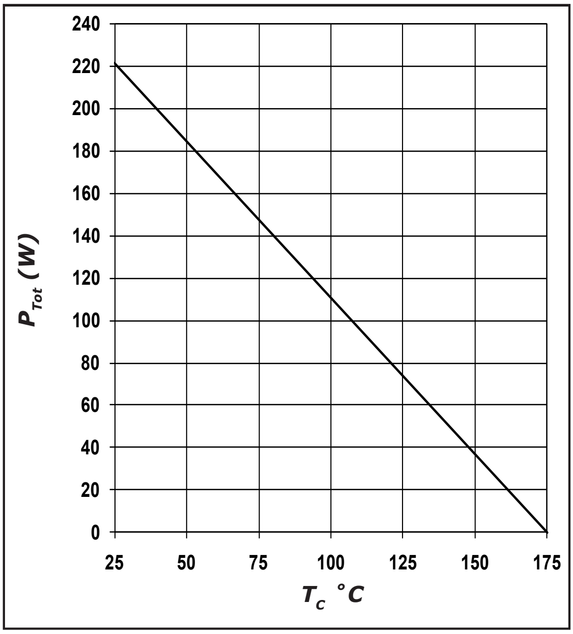


Figure 4. Power Derating

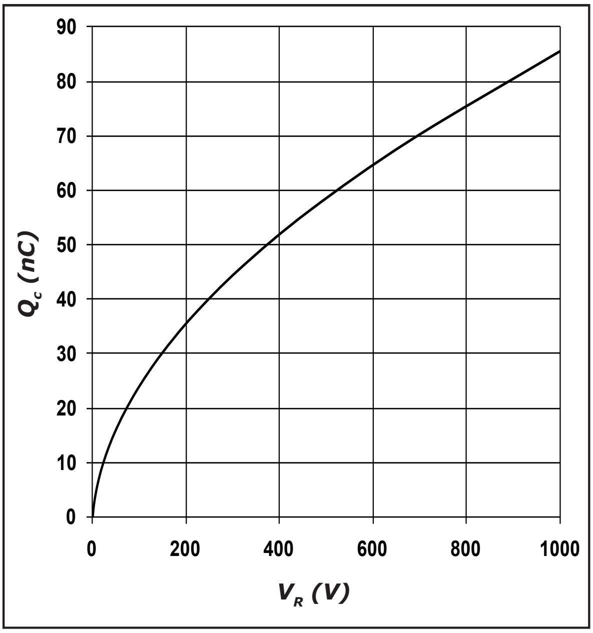


Figure 5. Recovery Charge vs. Reverse Voltage

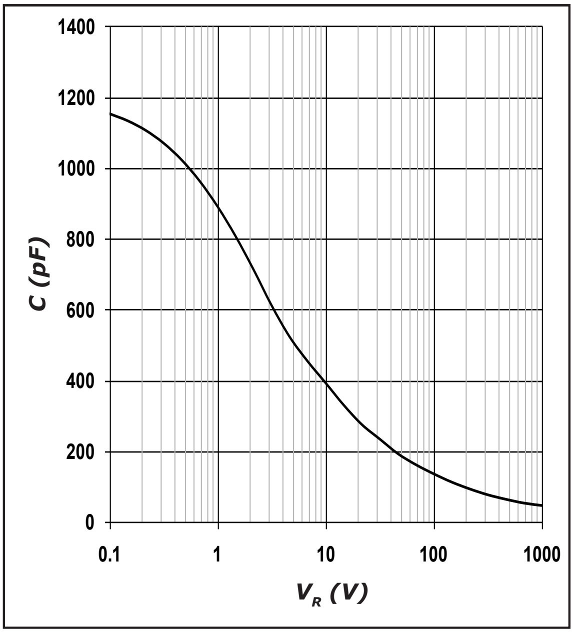


Figure 6. Capacitance vs. Reverse Voltage

Typical Performance

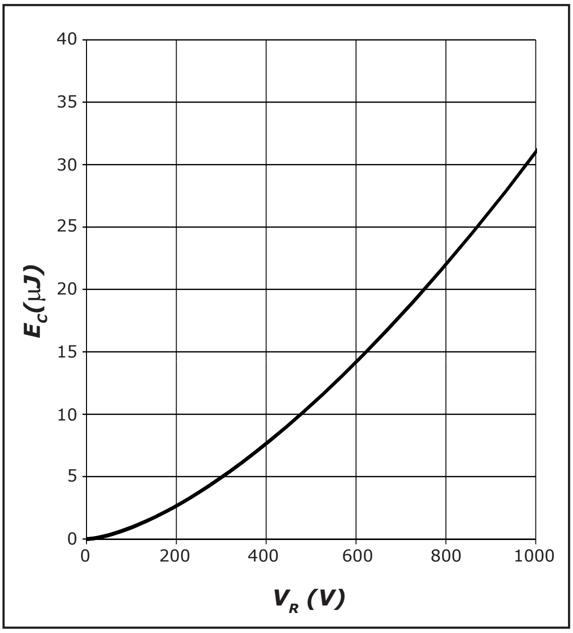


Figure 7. Typical Capacitance Stored Energy, per leg

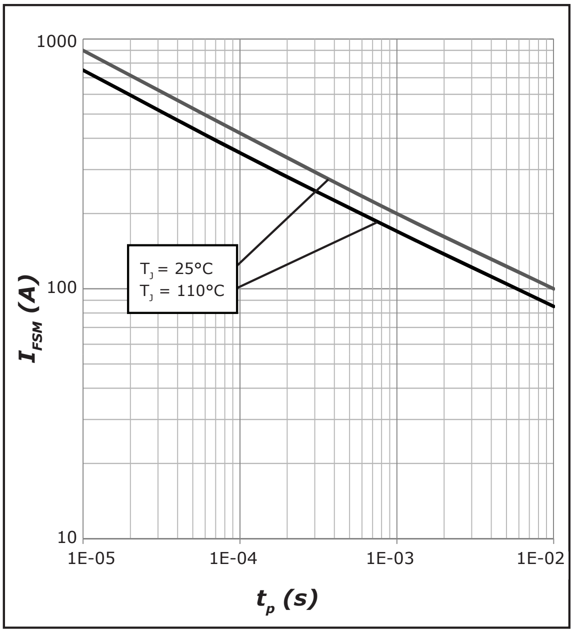


Figure 8. Non-Repetitive Peak Forward Surge Current versus Pulse Duration (sinusoidal waveform), per leg

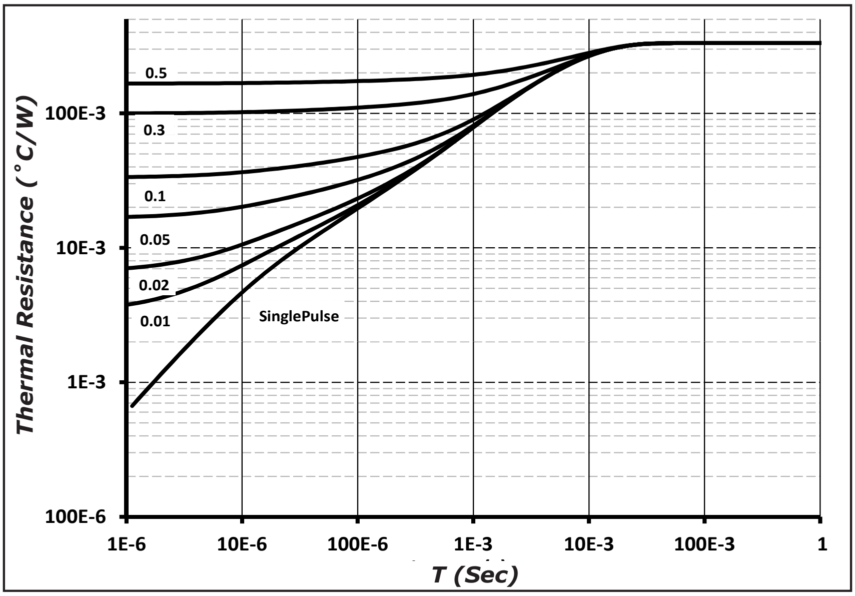
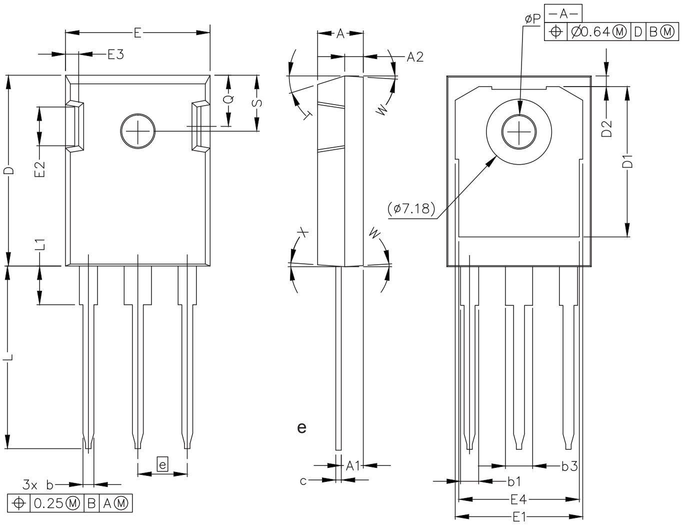


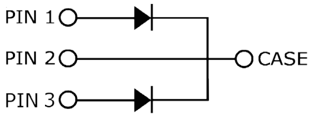
Figure 9. Device Transient Thermal Impedance

Package Dimensions

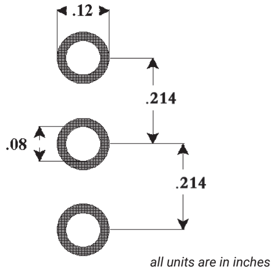
Package TO-247-3


E
E3
D
E2
L1
L
3x b
⌖ 0.25Ⓜ B AⓂ
e
A
A2
T
W
X
W
e
A1
c
ØP
–A–
⌖ Ø0.64Ⓜ D BⓂ
Q
S
(ø7.18)
D2
D1
b1
b3
E4
E1

POS	Inches		Millimeters	
	Min	Max	Min	Max
A	.190	.205	4.83	5.21
A1	.090	.100	2.29	2.54
A2	.075	.085	1.91	2.16
b	.042	.052	1.07	1.33
b1	.075	.095	1.91	2.41
b3	.113	.133	2.87	3.38
c	.022	.027	0.55	0.68
D	.819	.831	20.80	21.10
D1	.640	.695	16.25	17.65
D2	.037	.049	0.95	1.25
E	.620	.635	15.75	16.13
E1	.516	.557	13.10	14.15
E2	.145	.201	3.68	5.10
E3	.039	.075	1.00	1.90
E4	.487	.529	12.38	13.43
e	.214 BSC		5.44 BSC	
L	.780	.800	19.81	20.32
L1	.161	.173	4.10	4.40
N	3			
ØP	.138	.144	3.51	3.65
Q	.216	.236	5.49	6.00
S	.238	.248	6.04	6.30
T	17.5° REF			
W	3.5° REF			
X	4° REF			


PIN 1
PIN 2
PIN 3
CASE

Recommended Solder Pad Layout

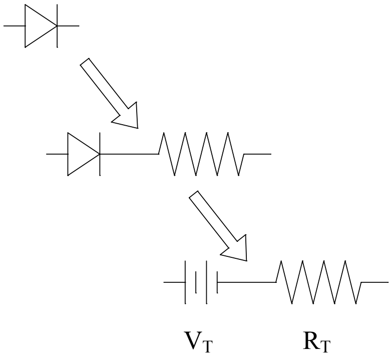

.12
.214
.08
.214
all units are in inches

TO-247-3

Part Number	Package	Marking
C4D30120D	TO-247-3	C4D30120

Note: Recommended soldering profiles can be found in the applications note here:
http://www.wolfspeed.com/power_app_notes/soldering

Diode Model



$$Vf_T = V_T + If * R_T$$

$$V_T = 0.97 + (T_j * -2.12*10^{-3})$$

$$R_T = 0.031 + (T_j * 3.92*10^{-4})$$

Note: T_j = Diode Junction Temperature In Degrees Celsius, valid from 25°C to 175°C

Notes

- **RoHS Compliance**
  The levels of RoHS restricted materials in this product are below the maximum concentration values (also referred to as the threshold limits) permitted for such substances, or are used in an exempted application, in accordance with EU Directive 2011/65/EC (RoHS2), as implemented January 2, 2013. RoHS Declarations for this product can be obtained from your Wolfspeed representative or from the Product Ecology section of our website at http://www.wolfspeed.com/power/tools-and-support/product-ecology.

- **REACh Compliance**
  REACh substances of high concern (SVHCs) information is available for this product. Since the European Chemical Agency (ECHA) has published notice of their intent to frequently revise the SVHC listing for the foreseeable future,please contact a Cree representative to insure you get the most up-to-date REACh SVHC Declaration. REACh banned substance information (REACh Article 67) is also available upon request.

- This product has not been designed or tested for use in, and is not intended for use in, applications implanted into the human body nor in applications in which failure of the product could lead to death, personal injury or property damage, including but not limited to equipment used in the operation of nuclear facilities, life-support machines, cardiac defibrillators or similar emergency medical equipment, aircraft navigation or communication or control systems, or air traffic control systems.

Related Links

- Cree SiC Schottky diode portfolio: http://www.wolfspeed.com/Power/Products#SiCSchottkyDiodes
- Schottky diode Spice models: http://www.wolfspeed.com/power/tools-and-support/DIODE-model-request2
- SiC MOSFET and diode reference designs: http://go.pardot.com/l/101562/2015-07-31/349i

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B Skin depth of copper wires

This section tabulates the skin depth of copper wires at different frequencies. The skin depth is given by:

$$\delta = \sqrt{\frac{2}{\omega\mu\sigma}} = \sqrt{\frac{2\rho}{\omega\mu}} \tag{1}$$

where $f = \omega/2\pi$. For an annealed copper wire, the resistivity ρcu is $1.72 * 10^{-8}\ \Omega m$, and the permeability μ_{cu} is $1.257 * 10^{-6}$. The resulting skin depth for different frequencies is tabulated in table A4

Table A4: Skin depth of copper wire at different frequencies.

Frequency f	*Skin depth δ*
50 Hz	9.3333 mm
100 Hz	6.5997 mm
150 Hz	5.3886 mm
200 Hz	4.6667 mm
250 Hz	4.1740 mm
500 Hz	2.9515 mm
1000 Hz	2.0870 mm