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Optimal design of wind turbine converters using advanced power semiconductor materials

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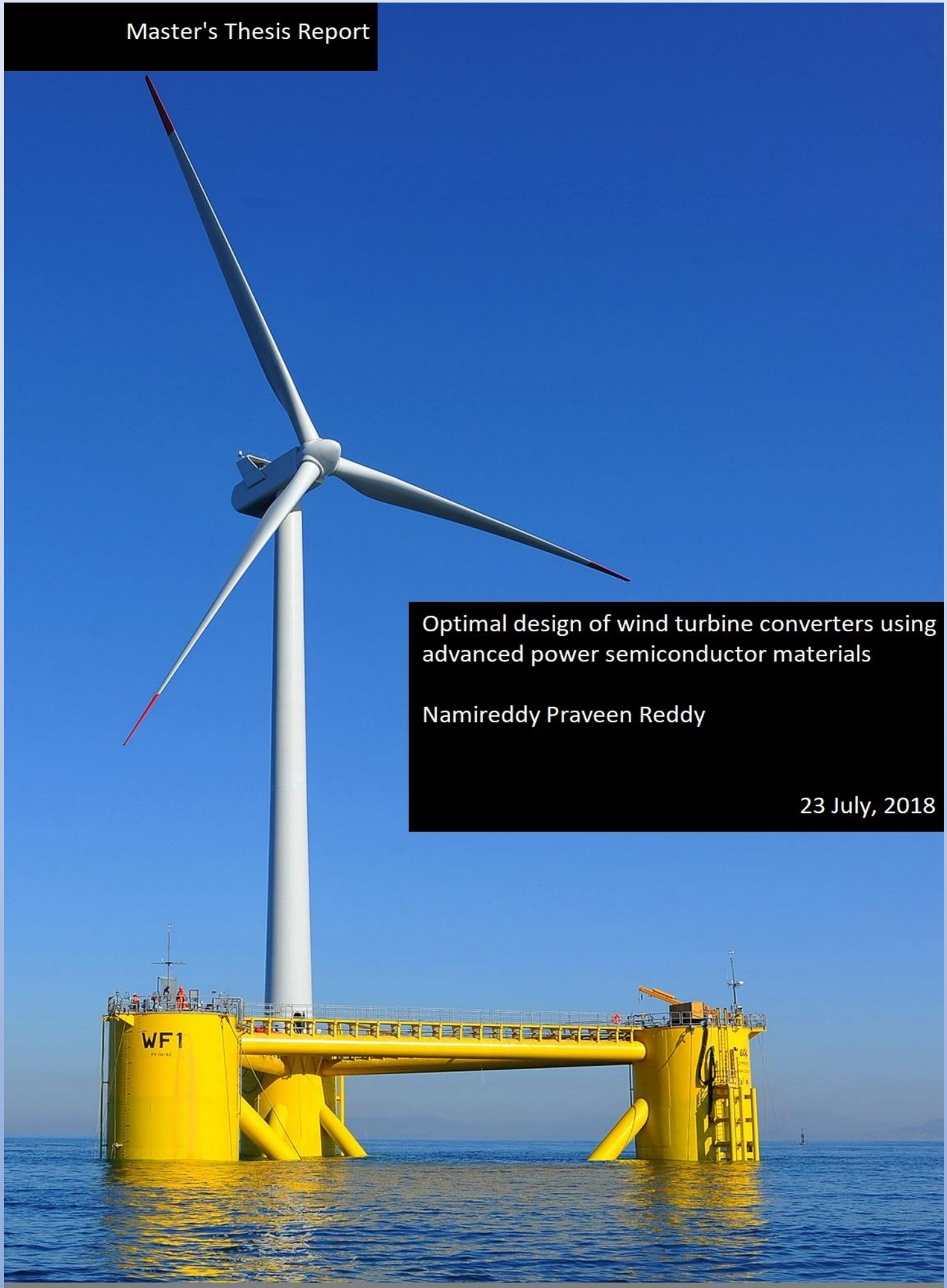
Master's Thesis Report



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NTNU

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Faculty of Information Technology and Electrical Engineering

Department of Electric Power Engineering
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by

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Place & date: Trondheim, 23 July 2018

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Summary

The tremendous increase in the wind farm installations worldwide during the last two decades is associated with the massive penetration of power electronic converters suitable to perform high efficiency electrical energy conversions. There exist several design and performance challenges related to these power electronic converters. These are not only related to the electrical and thermal performance of the converters, but also to the physical size of the complete system. Many of these challenges can be addressed by studying the power semiconductor devices, which are the heart of power electronic converters. Considering modern silicon-based semiconductors have already reached their theoretical material limits, there is need to utilise the advantageous performance of the recently developed wide band gap semiconductors. Silicon carbide power diodes and transistors are among the successful wide band gap power devices.

An all DC series connected wind farm configuration has minimum number of conversion stages. Modular multilevel converter has many advantages over other multilevel converter topologies and is a promising topology for medium and high-power applications. As silicon has reached its physical limits, wide band gap semiconductors are emerging as promising alternatives. A combination of all three suggested has not been researched so far for multiple objective optimization. This research is an attempt to realize benefits and challenges of this combination. The scope of optimization is semiconductor power losses, total harmonic distortion and operating junction temperature.

The research work is focused on reviewing the state of the art literature regarding modular multilevel converter to understand the operating principles, control methods. A wind generator side converter using modular multilevel converter topology and silicon carbide MOSFET is developed in Simulink/MATLAB environment. Sixty-two number of simulations are carried by varying the number of sub modules per arm and the number of parallel connected semiconductor devices. In each simulation, semiconductor power losses and total harmonic distortion are measured.

The simulation results show that the silicon carbide MOSFET with lowest voltage rating is found suitable due to higher number of sub modules and voltage levels, better voltage waveform, reduced filter requirement, lower semiconductor losses, less cost. Furthermore, minimum number of sub modules and maximum number of parallel connected devices result in lower losses.

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List of Abbreviations

WECS	Wind Energy Conversion system
VSC	Voltage Source Converter
VSR	Voltage Source Rectifier
VSI	Voltage Source Inverter
MMC	Modular Multilevel Converter
WBG	Wide Band Gap
SiC	Silicon Carbide
GaN	Gallium Nitride
PMSG	Permanent Magnet Synchronous Generator
MVDC	Medium Voltage Direct Current
MVAC	Medium Voltage Alternate Current
IGBT	Insulated Gate Bipolar Transistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
IGCT	Integrated Gate Commutated Thyristor
FRT	Fault Ride Through
LVAC	Low Voltage Alternating Current
HVDC	High Voltage Direct Current
MVDC	Medium Voltage Direct Current
SBD	Schottky Barrier Diode
JBS	Junction Barrier Schottky Diode
NPC	Neutral Point Clamped

OTC	Optimal Torque Control
EMI	Electro Magnetic Interference
SM	Sub Module
LL	Line to Line
RMS	Root Mean Square
THD	Total Harmonic Distortion
OJT	Operating Junction Temperature
PWM	Pulse Width Modulation
CPS	Carrier Phase Shifted

List of Symbols

N_{SM}/N	Number of Sub Modules per arm
N_P	Number of Parallel connected semiconductor devices
L_{arm}	Arm Inductance
R_{arm}	Arm Resistance
C_{SM}	Sub Module Capacitance
V_{DC}	DC side Voltage
V_{AC}	AC side Voltage
V_{grid}	Grid Voltage
f_c	Carrier Frequency
f	Fundamental Frequency
Ts	Sample Time
P	Active Power
I_{arm}/i_{arm}	Arm Current
i_{SM}	Sub Module Current
I_{MOSFET}	MOSFET Current

Thesis Layout

In Chapter 1, the research proposal prepared for master thesis is introduced. Objectives of the master thesis are presented.

In Chapter 2, basic knowledge about MMC is presented. This includes schematic diagram, classification of MMC, operating principles and dynamics.

In Chapter 3, steps involved in modeling the MMC in Simulink/MATLAB environment are explained. These steps include dimensioning the circuit parameters, modulation techniques, control methods for inner and outer dynamics and a summary of Simulink/MATLAB model.

In Chapter 4, the optimization criteria is presented. The methodology to calculate semiconductor power losses of SiC MOSFET in MMC for a given operating junction temperature and total harmonic distortion is elaborated.

In Chapter 5, simulations methodology and the results obtained by sixty-two number of simulations are presented. These simulations are carried for three different SiC MOSFETs by varying the number of sub modules per arm and the number of parallel connected semiconductor devices.

In Chapter 6, discussion, conclusion and future work are presented.

Chapter 1. Introduction

This project report is a master's thesis report, written to partially fulfil the graduation requirements of two years international Master of Science in electric power engineering at Norwegian University of Science and Technology (NTNU). The author was engaged in research and writing this report from 15th January 2018 to 23rd July 2018 at NTNU and Federal University of Minas Gerais, Brazil as part of INTPART project NB_POCCREI. INTPART (international partnerships for excellent education, research and innovation) is an initiative by research council of Norway. NB_POCCREI (Norwegian-Brazilian collaboration on power theories and cooperative control for renewable energy integration) is a project under INTPART.

1.1 Background

During the last two decades, the effects of global warming are felt across the world from extreme monsoons, droughts in Africa and India to slowing down Atlantic Ocean current (Atlantic Meridional Overturning Circulation), that keeps Europe and North America warm through exchange of cold water with warm water from Gulf stream. Paris climate agreement is a sign of unanimous acceptance and the urgency to address global warming. Many countries across the world are engaged in policy making to reduce the greenhouse gas emissions. Hence, early adaption of lower emission technologies could give an important competitive advantage in the coming years.

The energy consumed through power system today is around 30% and the transportation of people and goods accounts for about 27% of world's energy consumption. A major portion of the electricity generation and transportation are dependent on fossil fuels. The electrification of transportation along with moving electricity generation resources from fossil fuels to clean renewable energies could make about 60% of world's energy consumption free from greenhouse gas emissions. World's energy consumption is projected to grow at fast pace. Hence, it is vital for optimal design of a sustainable model for future electric power system based completely on renewable energy resources.

Wind energy is a promising renewable energy resource and is emerging as main stream source of electric power. During the last two decades, the cumulative wind energy installed capacity worldwide has increased exponentially from 6.1 GW in 1996 to 539.12 GW and is expected to reach 800 GW by 2021 according to Global Wind Energy Council. This increase in the wind

farm installations worldwide is also associated with the advancement in power electronic technologies.

1.2 Research Proposal

The research proposal is prepared based on the literature review carried as part of specialization project during autumn semester 2017. The literature review consists of the state of the art power electronic technologies used in wind energy conversion system. This includes power electronic converter topologies, control and modulation techniques, power semiconductor devices, wind turbine load profiles, wide band gap power semiconductor materials and devices. Furthermore, a comparative study of silicon carbide power semiconductor devices and silicon power semiconductor devices is carried to realize potential benefits, challenges, opportunities. The specialization project report can be downloaded from the google drive link provided in reference [1].

Power electronic converters play an important role in interfacing of uncontrolled renewable energy resources such as wind, solar with main power system. However, there are several challenges related to design and performance of power electronic converters. These challenges are related to the electrical and thermal performance, physical size. Many of these challenges can be addressed by the study of power semiconductor devices made by advanced wide band gap semiconductor materials such as silicon carbide and gallium nitride. Silicon carbide power diodes and transistors are among the successful wide band gap power semiconductor devices and are suitable for high power applications such as large wind energy conversion systems.

An all DC series connected wind farm configuration has minimum number of conversion stages as shown in Figure 1.1. Modular multilevel converter has many advantages over other multilevel converter topologies and is a promising topology for medium, high-power applications. SiC devices are the promising wide band gap devices suitable for high power applications. SiC MOSFET is relatively matured among all the SiC based power semiconductor switches and few commercial models of SiC MOSFET are introduced in the market recently. The combination of all three was proposed for master thesis.

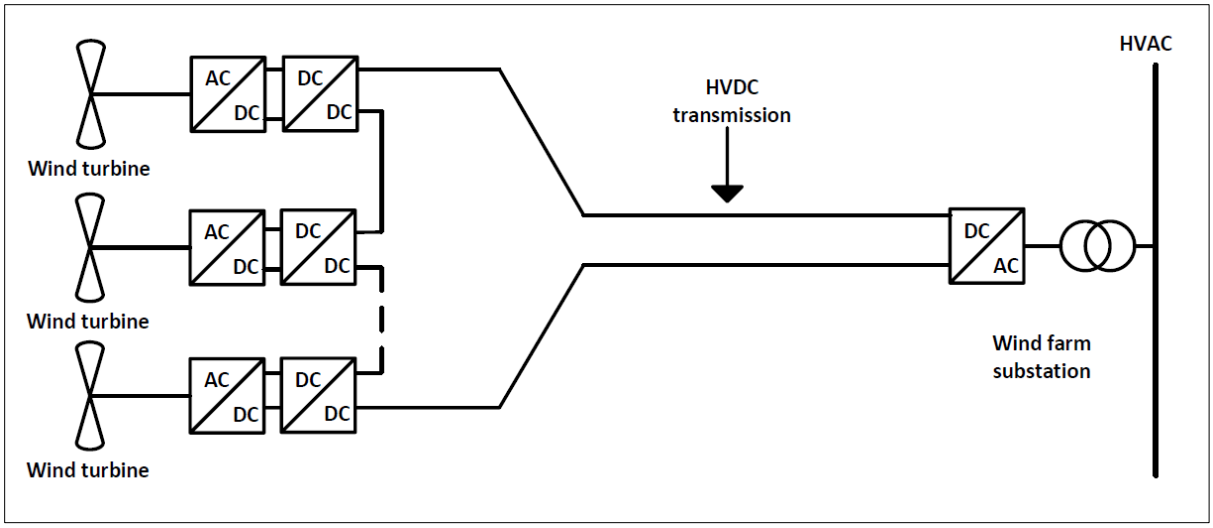


Figure 1.1 All DC series connected wind farm configuration

1.3 Objectives

The objective of this research work is to find optimal number of sub modules per arm and parallel connected semiconductor devices in MMC, that is intended to work as a wind generator side converter. The optimization is pursued by the study of semiconductor power losses, total harmonic distortion, operating junction temperature. The steps involved in pursuing the optimization are outlined as,

1. Understand the operating principles and dynamics of MMC
2. Literature review of state of the art MMC topologies and control methods
3. Develop a simulation model of MMC in Simulink/MATLAB environment
4. Study the methodology of semiconductor power loss calculation
5. Calculate the semiconductor power losses, total harmonic distortion at an operating junction temperature of 25°C, 125°C by varying the number of sub modules and number of parallel connected semiconductor devices
6. Analysis of results and propose the optimal number of sub modules and optimal number of parallel connected devices.

Chapter 2. The Modular Multilevel Converters

2.1 Introduction

The concept of the Modular Multilevel Converters was first introduced by Anton Lesnicar and Rainer Marquardt during The Power Tech Conference, Bologna-Italy in 2003 [2]. The design of MMC was provoked by the deregulation of international energy markets and the trend to decentralized electricity generation that required multiple voltage levels. Though it was proposed for transmission of electric power using HVDC initially, over the past few years efforts have been put towards addressing the technical challenges associated with the operation and control of the MMC as well as broadening its applications. The MMC was first used commercially in the Trans Bay Cable project in San Francisco, USA by Siemens that incorporates 216 Half-Bridge submodules in each arm and the rated voltage of each SM capacitor is 1 kV, which makes it efficient to generate 201 output voltage levels [3] [4].

The Modular Multilevel Converter has become attractive multilevel converter topology for medium/high power applications. The following technical and economic advantages of MMC over other multilevel converter topologies have significantly contributed for the development of MMCs for high power applications.

2.1.1 Advantages

The advantages of MMC are,

1. Modular realization
   - Scalable to different power and voltage levels
   - Independent of the state-of-the-art of fast evolving power semiconductor devices
2. Multilevel waveform
   - Expandable to any number of voltage steps
   - Low total harmonic distortion, specifically for high power applications where a large number of identical sub modules with low-voltage ratings are stacked up, thereby the size of passive filters can be reduced significantly
   - Dynamic division of voltage to the power semiconductor devices
3. High availability
   - Use of approved devices
   - Redundant operation
4. Failure management

- Fail safe operation for device failures
- Avoidance of mechanical destruction (high current magnetic forces and arcing)

5. Low switching frequency due to high number of levels, which leads to lower switching losses
6. High efficiency, which is important for high power applications
7. Absence of high voltage DC-link capacitors
8. Low investment and decreased lifecycle cost
   - Standard components
   - Modular construction [2]

2.1.2 General Schematic Diagram/Construction

A general schematic diagram of a three phase MMC is shown in Figure 2.1. A three phase MMC (AC/DC) has three identical phase legs. Each phase leg has two identical arms, they are upper arm and lower arm. Each arm has a series arm inductor (L_{arm}), a series arm resistor (R_{arm}) and 'N' number of series connected identical sub modules from SM_1 to SM_N. If a submodule is half bridge (HB) as shown in Figure 2.2, each sub module has one capacitor, two identical power semiconductor switches with anti-parallel diodes. Overall, a three phase MMC has 3 phase legs, 6 arms, 6 arm inductors, 6 arm resistors, 6*N number of sub modules, 6*N number of capacitors, 6*N*2 number of power semiconductor switches, 6*N*2 number of anti-parallel diodes. The purpose of arm inductor is to suppress high frequency components in the arm current, while sub modules are controlled to generate the desired output voltage waveform. Arm resistance is equivalent resistance of the inductor and the connections. The purpose of capacitor is to store the energy and to regulate the DC voltage of each sub module.

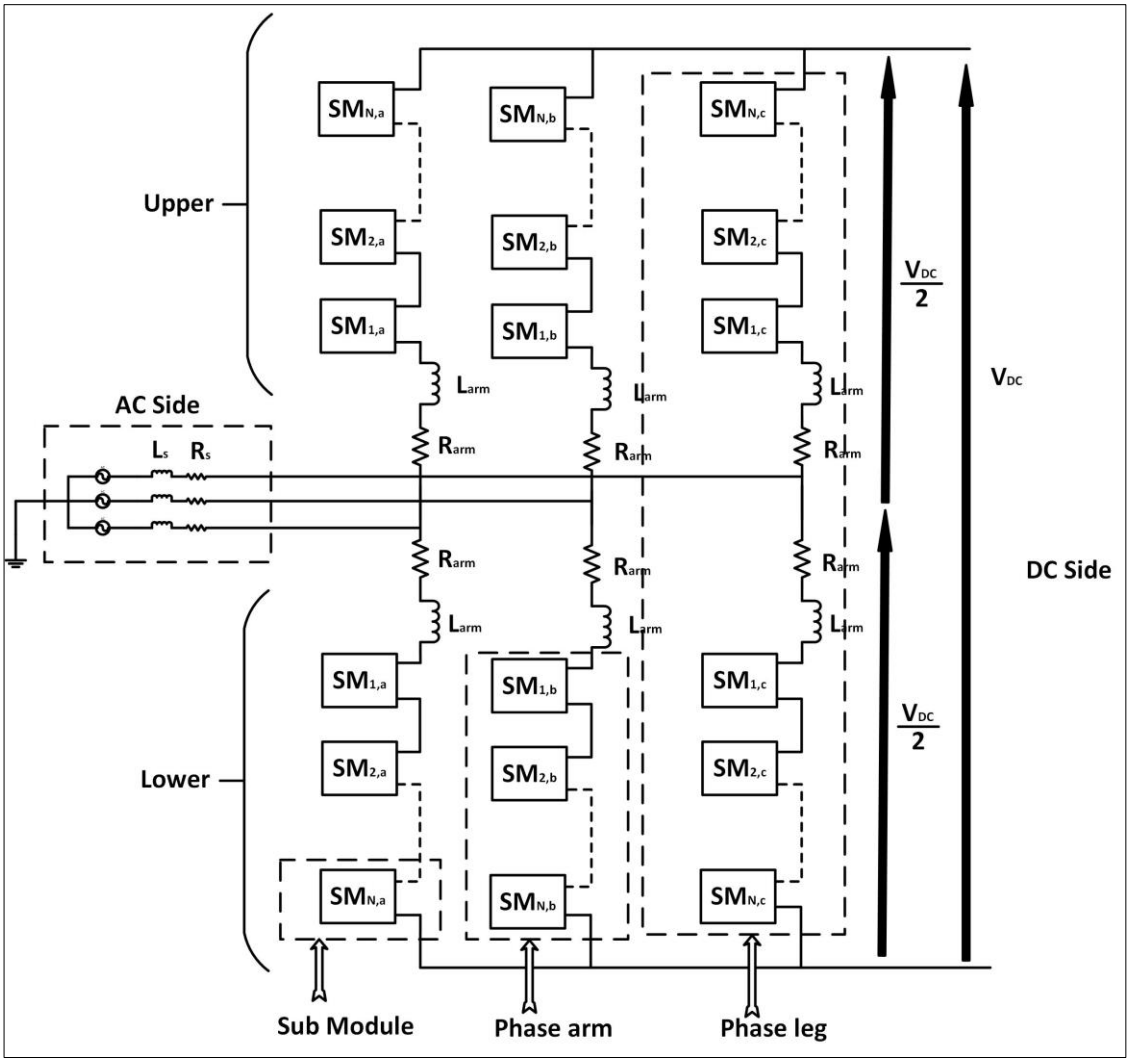


Figure 2.1 Schematic diagram of MMC

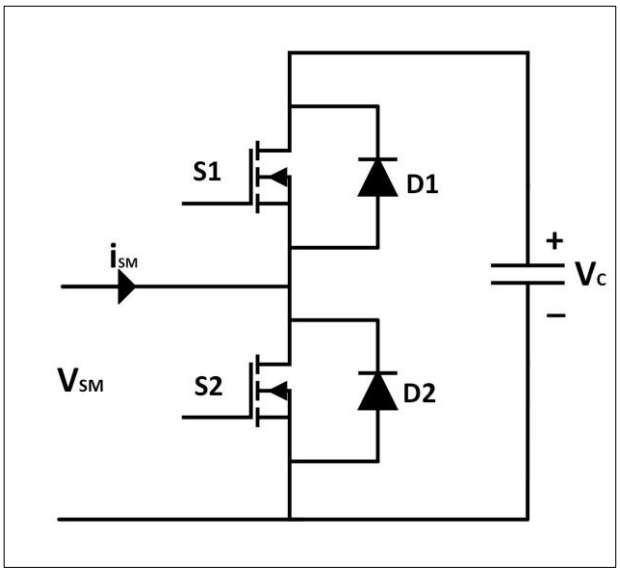


Figure 2.2 Schematic diagram of Half-Bridge Sub Module

2.2 Classification

2.2.1 Topology

Based on topologies, MMCs can be classified into:

1. Double-star-configured MMCs
2. A star-configured MMC
3. A delta-configured MMC
4. The dual MMC

The double-star-configured MMC topology possesses the common DC-link terminals as shown in Figure 2.1, which enable DC/AC and AC/DC power conversion. However, the star/delta-configured MMC topology has no common DC-link terminals as shown in Figure 2.3. As a result, it has no capability of achieving DC-to-AC and AC-to-DC power conversion although it can control active power back and forth between the three phase AC terminals and the floating DC capacitors. This implies that the star/delta-configured MMC topology is not applicable to industrial motor drives, but it is suitable for STATCOMs and energy storage systems. This is one of the most significant differences in function and application between the double-star-configured MMC topology and the star/delta-configured MMC topology. Figure 2.4 shows the dual configured MMC topology. Each DC side of positive and negative sub modules possesses a common DC capacitor, whereas its AC side is connected in parallel through two buffer inductors. The dual MMC is suitable for low-voltage large-current power conversion due to low arm current enabled by the parallel connection of buffer inductors [5].

Several alternative topologies of MMC have been proposed in literature. A few examples are shown in Figure 2.5. In the middle sub module MMC, the output phase is connected at the center of a sub module located in the middle of the phase leg. This structure can reduce the number of sub modules and hence the complexity of the control system because the balancing of power among the arms is performed only by this sub module [6]. The alternate arm MMC has an additional switch connected to each arm as shown. This switch controls the conduction period of each arm and could reduce the number of sub modules per arm [7]. The hybrid MMC uses two three-phase power units connected to the upper and lower arms as shown. These power units control the interchange of power among the arms [8]. Although these topologies improve some aspect of the MMC, they sacrifice modularity and reduce the reliability of the whole converter.

The interconnection of two AC networks can be performed using a back-to-back configuration or directly by a matrix MMC as shown. The main advantage of this configuration is the reduced number of arms required for the interconnection. However, the control becomes more complex due to the existence of two AC components in the arm currents [9]. The hexagonal MMC configuration can interconnect two three-phase AC systems using only six arms, but the control actions are restricted compared with matrix MMC, particularly for unbalanced grids, because each output phase is generated by a combination of only two input phases [10].

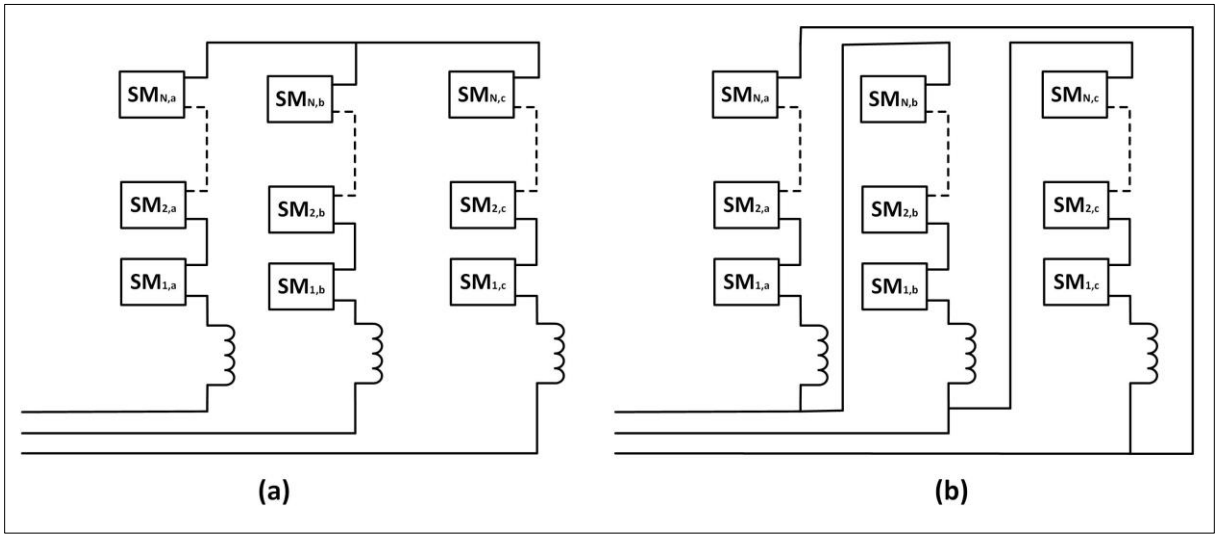


Figure 2.3 (a) Star configured MMC, (b) Delta configured MMC

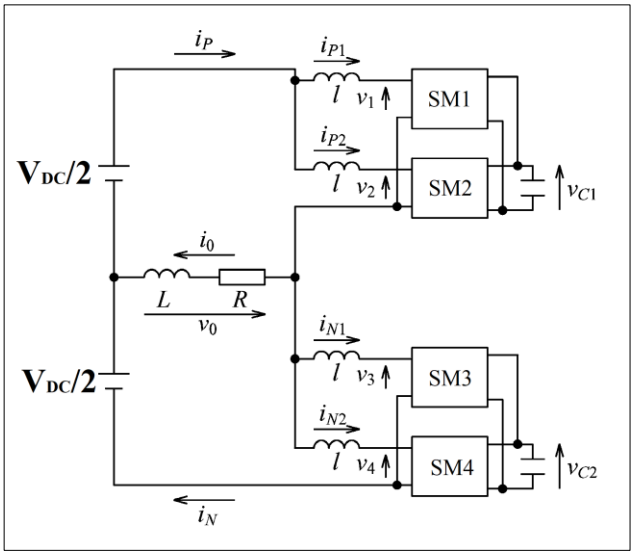


Figure 2.4 The dual configured MMC

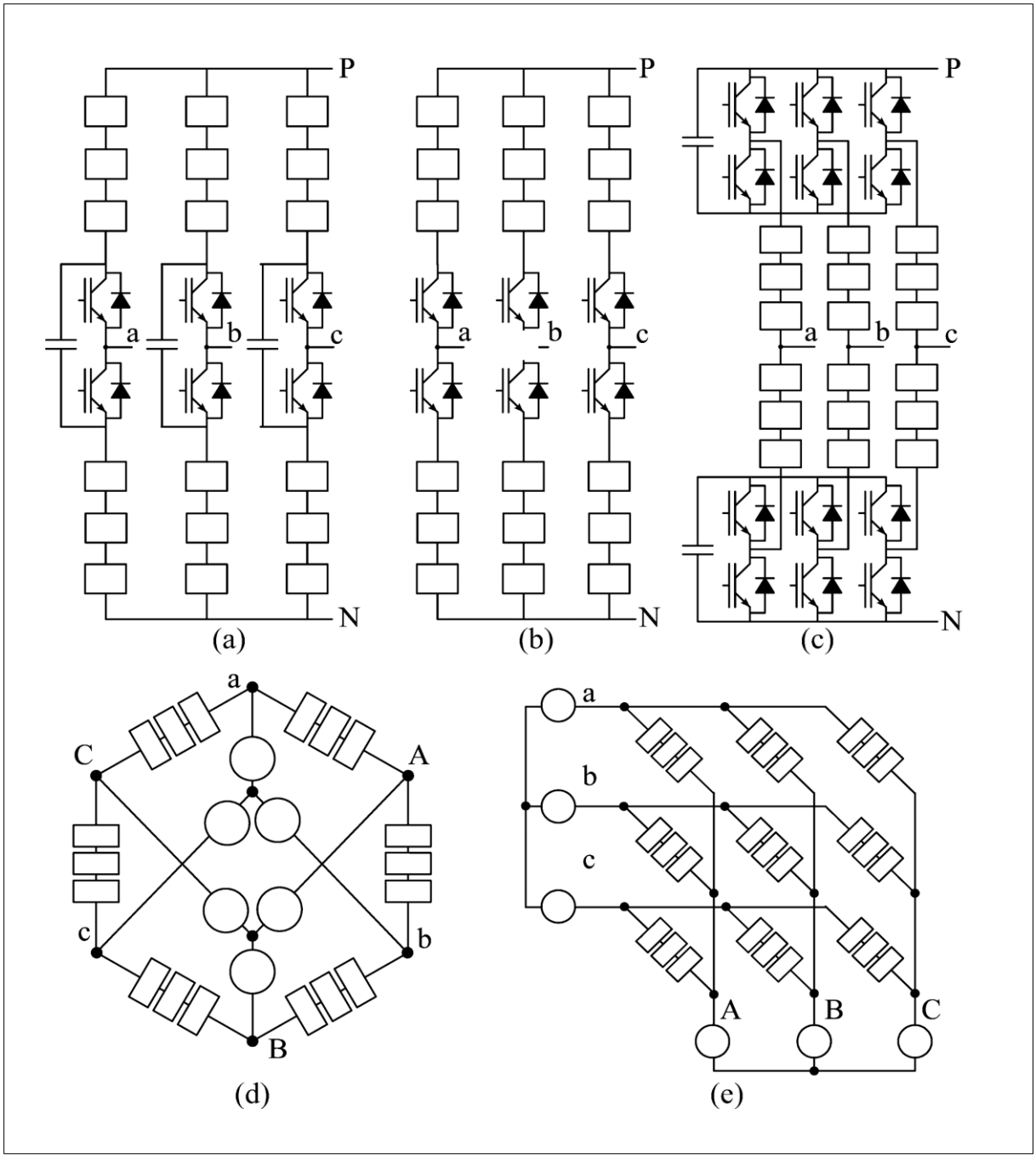


Figure 2.5 Advanced topologies of MMC. (a) Middle Sub Module MMC, (b) Alternate arm MMC, (c) Hybrid MMC, (d) Hexagonal MMC, (e) Matrix MMC [11]

2.2.2 Interconnection Function

MMCs can be classified based on the interfacing of two sides as,

1. Single-phase to Single-phase or Single-phase to DC
2. Three-phase to Single-phase or Three-phase to DC
3. Three-phase to Three-phase (Back-to-Back)

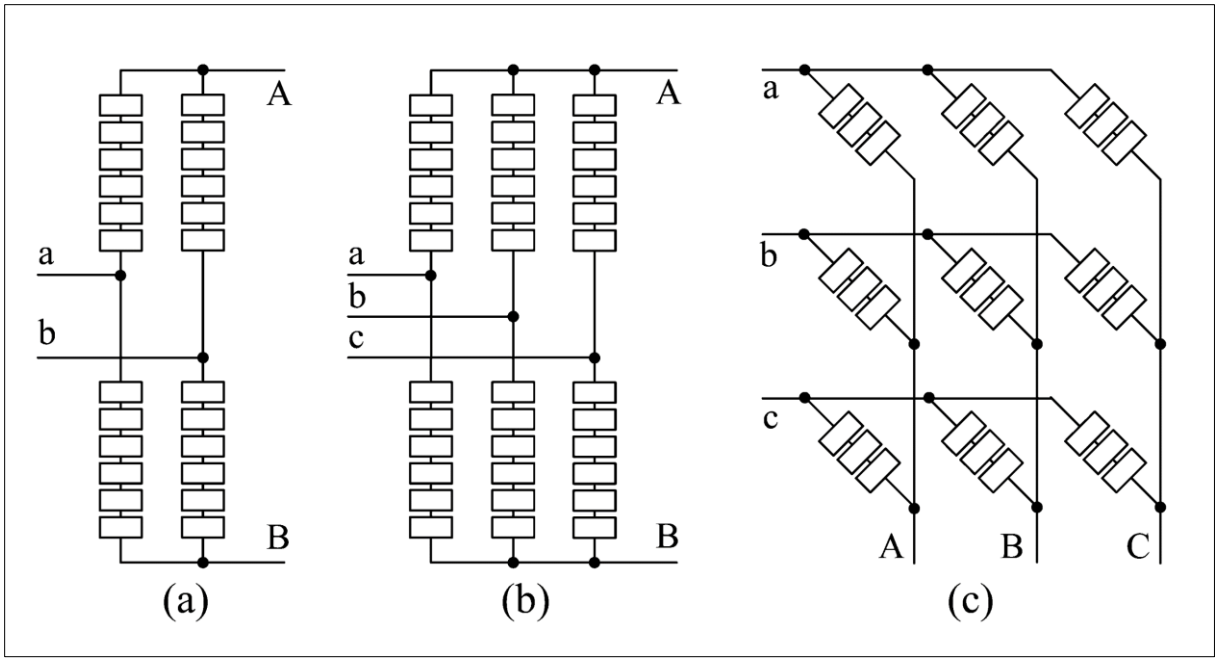


Figure 2.6 (a) Single-phase to Single-phase or Single-phase to DC, (b) Three-phase to Single-phase or Three-phase to DC, (c) Three-phase to Three-phase (Back-to-Back) [11]

2.2.3 Choice of the Sub Module

Submodules are different combinations of semiconductor switches, diodes and capacitors. Most popular topologies are half-bridge and full-bridge sub modules. Many researchers have proposed several submodule topologies with different advantages such as dimension reduction, DC-fault handling capability, higher numbers of voltage levels etc. However, this complicates the structure and control. With lot of research efforts to enhance the performance of MMC, number of submodule topologies has already gone beyond twenty and further increasing. In this Section, various topologies of SMs are categorized based on output voltage levels.

2.2.3.1 Two-Level Topologies

2.2.3.1.1 Half-Bridge Sub Module (HBSM)

Figure 2.7 shows schematic diagram of the Half-Bridge submodule. It has one capacitor and two switches with anti-parallel diodes. It is the simplest configuration capable of providing unipolar voltage by chopping the DC link voltage. Hence it is called Half-Bridge chopper cell. The output voltage of a Half-Bridge sub module is either equal to its capacitor voltage V_C (switched on/ inserted state) or zero (switched off/ bypassed state), depending on the switching states of the complimentary switch pairs, i.e., S1 and S2. Half-Bridge sub module has the capability of bidirectional current flow but unidirectional voltage blocking. Presence of only

two switches in SM structure gives high efficiency to Half-Bridge SM based MMC. The major drawback of HBSM is its inability of handling DC fault current. Handling DC-link short circuit fault current is a serious challenge, as antiparallel diodes of HBSM act as rectifier bridge when IGBT switches get blocked. AC side keeps feeding the fault current until circuit breaker operates [12] [13] [14].

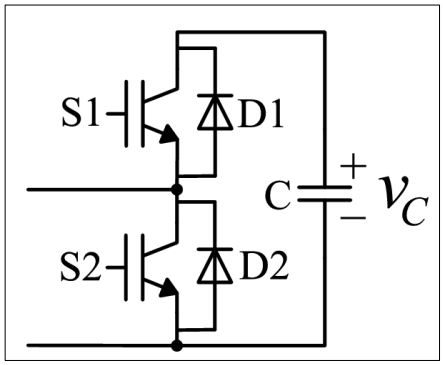


Figure 2.7 Schematic diagram of HBSM

2.2.3.1.2 Unipolar Full-Bridge Sub Module (UFBSM)

Figure 2.8 shows schematic diagram of the Unipolar FBSM. Unipolar voltage FBSM is proposed by Qin et al. [15]. This configuration is a modification of Full-Bridge SM (FBSM), which is shown in Figure 2.11. The S3 IGBT along with its antiparallel diode of full bridge module is replaced by a diode to obtain improved SM topology with DC handling capability without significant sacrifice in terms of efficiency and cost. The unipolar voltage SM can operate in either inserted or bypassed mode keeping S4 permanently ON. Thus, the module can generate '0' and 'V_C' output voltage levels. Under DC-link short circuit fault condition, the fault current takes path through antiparallel diode of S1, capacitor and antiparallel diode of S4 i.e. similar to fault current path in FBSM and thus gets blocked due to presence of capacitor [15]. The main drawback of this configuration is that the overall conduction losses of SM are more than the same for FBSM as under normal operating conditions.

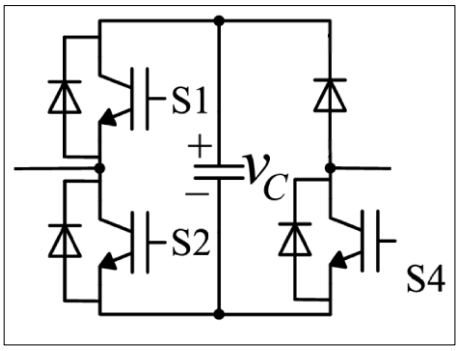


Figure 2.8 Schematic diagram of UFBSM

2.2.3.1.3 Unidirectional SM (USM)

Figure 2.9 shows schematic diagram of Unidirectional SM. Unidirectional SM is derived from HBSM, by replacing one of its switches by a diode to reduce the semiconductor components per SM. The USM has a restriction over switching states due to its dependency on current direction. Multiple other unidirectional configurations are proposed by De-Sousa et al. [16].

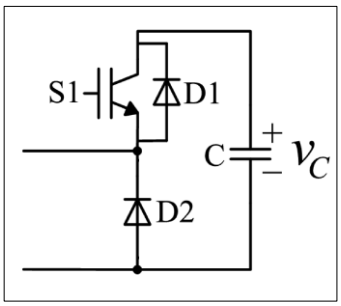


Figure 2.9 Schematic diagram of USM

2.2.3.1.4 Clamp Single SM (CSSM)

Figure 2.10 shows schematic diagram of Clamp Single SM. CSSM is a modification of three-level flying capacitor submodule (shown in Figure 2.13), obtained by eliminating one of the switches and replacing the capacitor by a diode. Unlike other two-level SMs, three-switch based configuration has DC fault handling capability [17].

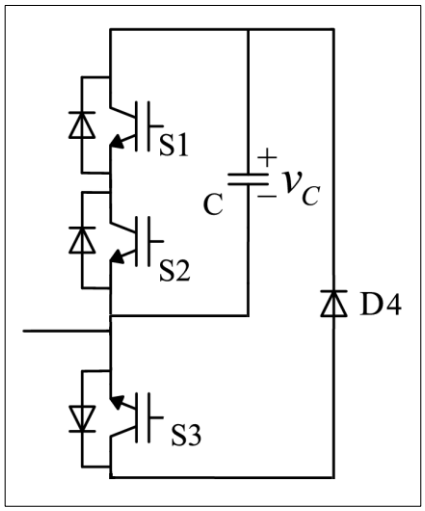


Figure 2.10 Schematic diagram of CSSM

2.2.3.2 Three-Level Topologies

2.2.3.2.1 Full Bridge Sub Module (FBSM)

Figure 2.11 shows schematic diagram of the Full-Bridge sub module. FBSM is made of four switches and one capacitor, can provide bipolar output voltage levels '+V_C', '-V_C' and '0',

through proper operation of the switching states of four switches S1 to S4. FBSM is capable of handling DC-link short circuit fault current via generating reverse voltage through capacitor voltage. Furthermore, FBSM based MMC has ability to be fully disconnected by switching off all the switches, whereas the same was not possible with HBSM. The main disadvantage of FBSM is that the number of semiconductor devices of a Full-Bridge SM is twice of a Half-Bridge SM, implies the power losses as well as the cost of an MMC based on the Full-Bridge SMs are significantly higher than that of an MMC based on the Half-Bridge SMs [13] [12] [18]. A double commutation cell can be obtained by parallel connection of two identical FBSMs, that can give four-quadrant operation as explained in [19].

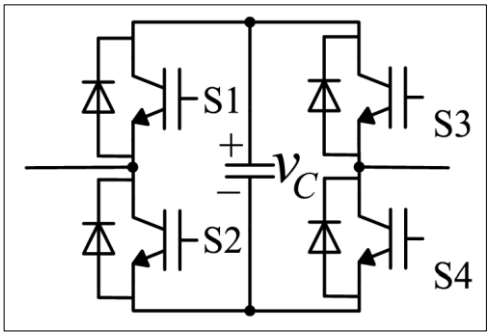


Figure 2.11 Schematic diagram of FBSM

2.2.3.2.2 Three Level Neutral Point Clamped SM (TLNPCFM)

Figure 2.12 shows schematic diagram of Three-Level NPC sub module. It has four switches, two diodes and two capacitors. The Three-Level NPC SM based MMC has higher semiconductor losses than the Half-Bridge MMC and lower than the Full-Bridge MMC. The main drawback of this configuration is lack of DC-link short circuit current handling capability. From a manufacturing perspective and control, this SM circuit is not very attractive because of high number of components, complex control and losses. There are several improved NPC topologies proposed in literature such as developed by Dargahi et al. [20]. One such improved topology is to replace two diodes by two switches, while the other can be derived using T-connection of semiconductor switches and the midpoint switches must perform blocking in both polarities [12].

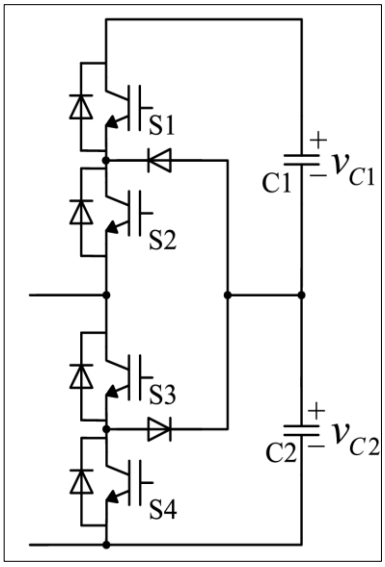


Figure 2.12 Schematic diagram of TLNPCSM

2.2.3.2.3 Three Level Flying Capacitor SM (TLFCSM)

Figure 2.13 shows the schematic diagram of Flying Capacitor sub module. It has four switches, equal to that of FBSM and two capacitors. The capacitor C1 operating voltage is twice of capacitor C2. The semiconductor losses are similar to that of Half-Bridge MMC. The main drawback of this configuration is lack of DC-link short circuit current handling capability. Considering this drawback, high number of switches and capacitors, high cost and complex control, it is not attractive configuration from a manufacturing perspective and control.

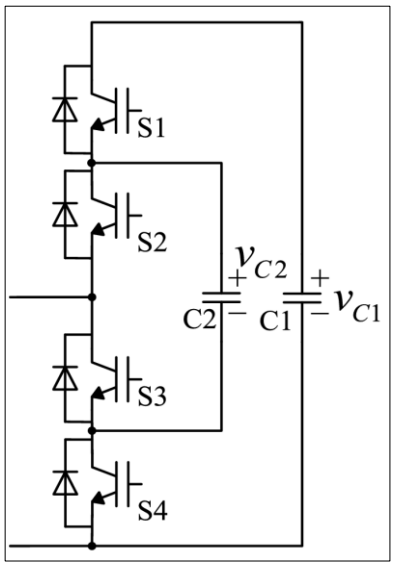


Figure 2.13 Schematic diagram of TLFCSM

There are several other Three-Level topologies proposed in literature. A Double submodule (DSM) proposed by Ilves et al. [21]. It is derived by connecting two FBSMs to enhance the capacitor voltage balancing without increasing power rating of SMs. Though, DSM is not bipolar, its maximum blocking voltage is twice that of FBSM. This has the capability of handling DC faults. Three-level Cross Connected SM (TLCCSM) proposed by Qin et al. [15]. In TLCCSM, two HBSMs are back-to-back cross connected using a switch and a diode. A Diagonal Bridge submodule (DBSM) proposed by Yu et al. [12]. DBSM is a modification of FBSM by replacing two diagonal switches with diodes. It gives three output voltages similar to FBSM but has only two switches as in HBSM. An improved hybrid submodule (IHSM) is explained in [17].

2.2.3.3 Four-Level Topologies

2.2.3.3.1 Clamp Double SM (CDSM)

Figure 2.14 shows schematic diagram of the Clamp Double SM. A clamp-double SM consists of two half-bridge SMs, two additional diodes and one extra IGBT with its anti-parallel diode. During normal operation, the switch S5 is always switched on and the clamp-double SM acts equivalent to two series connected half-bridge SMs. However, both capacitors demonstrate either series or parallel connection for CDSM, when the IGBT switches are blocked. Furthermore, the submodule can be operated as FBSM by parallel connection of both capacitors. To avoid paralleling issue, diodes of parallel path can be replaced by switches. CDSM can generate reverse voltage and thus possesses DC-link fault current handling capability but generates reverse voltage of '$0.5V_{dc}$' per arm only. In terms of semiconductor power losses, considering MMC with same voltage levels, CDSM lies in between HBSM and FBSM [12] [13] [22].

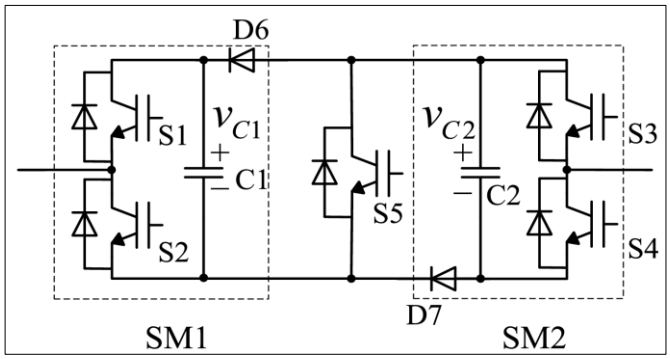


Figure 2.14 Schematic diagram of CDSM

2.2.3.3.2 Asymmetrical SM (ASM)

Asymmetrical SM is an alternative way of doubling the commutation sub module by combining two different sub modules. For example, Asymmetrical SM can be obtained by combining HBSM and FBSM. Being combination of two basic submodule structures, this ASM can provide both unipolar and bipolar operation. Furthermore, presence of FBSM furnishes it with DC fault current handling capability and series connection of FBSM and HBSM facilitate with the ability to generate four voltage levels [19].

2.2.3.3.3 Series Connected Double SM (SDSM)

Series connected double SM (SDSM is proposed by Zhang et al. [23], for blocking DC-link fault current. It is obtained by the connection of two HBSMs using an additional switch and diode, capable of extinguishing the DC arc and restoring the insulation on the event of short circuit. Furthermore, during normal operation, two HBSMs are connected as independent submodules and hence there is no necessity for modifying modulating and control strategies [23].

2.2.3.4 Five-Level Topologies

2.2.3.4.1 Five-Level Cross Connected SM (FLCCSM)

Figure 2.15 shows schematic diagram of Five Level Cross Connected sub module. Similar to CDSM, a five-level cross-connected SM is obtained by back to back cross connection of two half-bridge SMs through two extra switches (IGBTs) with their anti-parallel diodes. FLCCSM can provide reverse voltage similar to FBSM and has the ability to block DC fault current by producing blocking effect through series connection of the two capacitors of SM. Its semiconductor losses are the same as the clamp-double SM [13].

Other five level sub module topologies can be derived by cross (CCSM) or parallel (PCSM) connected SMs such as FBSM, HBSM. CCSM can generate symmetrical bipolar output voltages and achieve high voltage levels. In PCSM, connecting capacitors in parallel helps in reduction of capacitor voltage ripple. Using FBSM enables both SMs with DC-link fault current handling capability. Apart from these configurations, Ilves et al. [21], proposed an alternative way of parallel connection of capacitors with motive of reducing the device current rating.

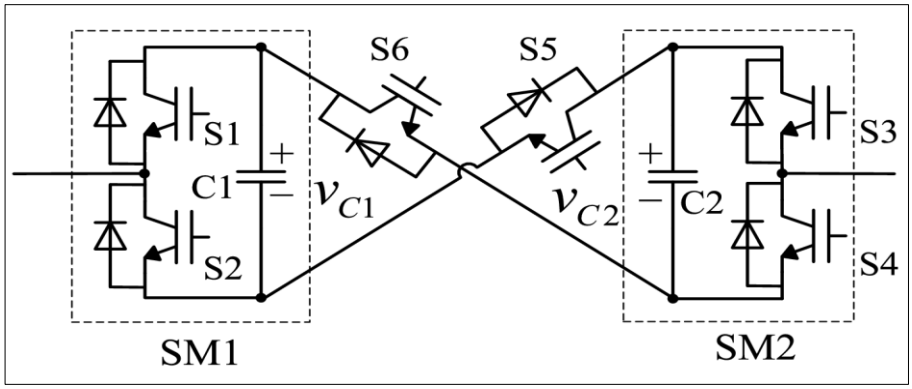


Figure 2.15 Schematic diagram of FLCCSM

2.2.3.5 Other Topologies

2.2.3.5.1 New SM (NSM)

Figure 2.16 shows schematic diagram of new sub module topology. This is proposed to increase the number of output voltage levels and to reduce the number of semiconductors used in the multi-level converter by X Li et al. in [24].

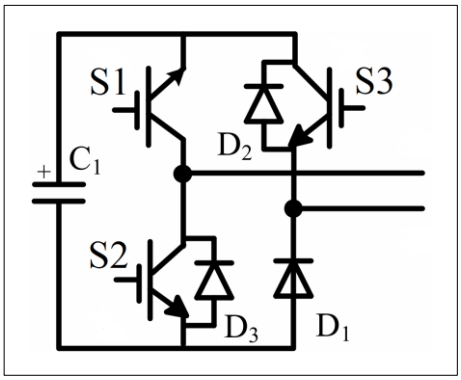


Figure 2.16 Schematic diagram of NSM

There are several other SM topologies proposed in literature with different and unique objectives. Riar et al. [25] suggests the modification in SMs for balancing the voltage using concept of inductive power transfer termed as sub module with resonant inverter for inductive power transfer. Perez et al. [26] propose to replace the voltage source DC link-based sub module topology by a current source DC link base sub module topology, as the current source SMs can achieve higher voltage and power ratings.

Table 2.1 Comparison of different Sub-Module topologies [27] [13]

Sub-Module	Voltage Levels	Losses	DC fault handling
Half-Bridge	0, $+V_C$	Low	No
Full-Bridge	0, $+V_C$, $-V_C$	High	Yes
NPC	0, V_{C1}, V_{C2}	Moderate	No
FC	0, V_{C1}, V_{C2}	Low	No
Clamp-Double	0, V_{C1}, V_{C2}, $(V_{C1}+V_{C2})$	Moderate	Yes
Five level Cross-Connected	0, V_{C1}, V_{C2}, $\pm(V_{C1}+V_{C2})$	Moderate	Yes

Table 2.1 presents a comparison of various submodule topologies based on their architecture, voltage levels, DC fault handling capability, etc. Also, the characteristics of concern while deciding sub module for MMC are mechanical design, internal fault protection system, capacitors requirement and complexity of control system. Among all the sub module circuit configurations, the Half-Bridge circuit has been the most popular SM adopted for the MMC. This is due to the presence of only two switches in the SM which results in a lower number of components and higher efficiency for the MMC. Hereafter, the double star MMC configuration for three-phase AC to DC interconnection with the Half-Bridge SM is considered for this master thesis.

2.3 Operation and Dynamics

2.3.1 Operation of Half-Bridge Sub Module

In the Figure 2.2, the two switches S1 and S2 of sub module is complementary during normal operation. When S1 is in ON-state and S2 is in OFF-state, the voltage of capacitor V_C appears across the terminals of sub module and the sub module is considered in service. When S2 is in ON-state and S1 is in OFF-state, the voltage across the terminals of sub module is '0' and the sub module is considered as bypassed.

When sub module is in service and current through sub module is positive i.e. $i_{SM} > 0$, the current flows through anti parallel diode D1. In this case, the capacitor of sub module is getting charged and hence the voltage across capacitor is increasing, which implies the capacitor voltage gradient is positive i.e. $dV_C/dt > 0$.

When sub module is in service and the current through sub module is negative i.e. $i_{SM} < 0$, the current flows through the power semiconductor switch (MOSFET). In this case, the capacitor of sub module is getting discharged and hence the voltage across capacitor is decreasing, which implies the capacitor voltage gradient is negative i.e. $dV_C/dt < 0$.

When S1 and S2 are in OFF-state, the sub module is considered in blocked state. This mode is used for energization of the converter. In this mode, the capacitor may charge through the anti-parallel diodes, but it cannot discharge. It may be used for few milliseconds during grid faults to protect transistor from overcurrent.

The four operating modes of a Half-Bridge sub module are summarized in the Table 2.2.

Table 2.2 Operating Modes of Half-Bridge Sub Module

Operating Mode		**S1**	**S2**	$\mathbf{i_{SM}}$	$\mathbf{V_{SM}}$	$\mathbf{dV_C/dt}$
1	Inserted	ON	OFF	> 0	V_C	> 0 (Charging)
2		ON	OFF	< 0	V_C	< 0 (Discharging)
3	Bypassed	OFF	ON	> 0	0	0 (Unchanged)
4		OFF	ON	< 0	0	0 (Unchanged)
5	Blocked	OFF	OFF	>= 0	0	>= 0 (Energization)

2.3.2 Dynamics

The schematic diagram of dynamics in MMC is shown in Figure 2.17. The MMC is connected to grid through grid impedance on AC side. The MMC is connected to DC voltage sources with midpoint grounded on DC side. The reference directions are as shown in the Figure 2.17.

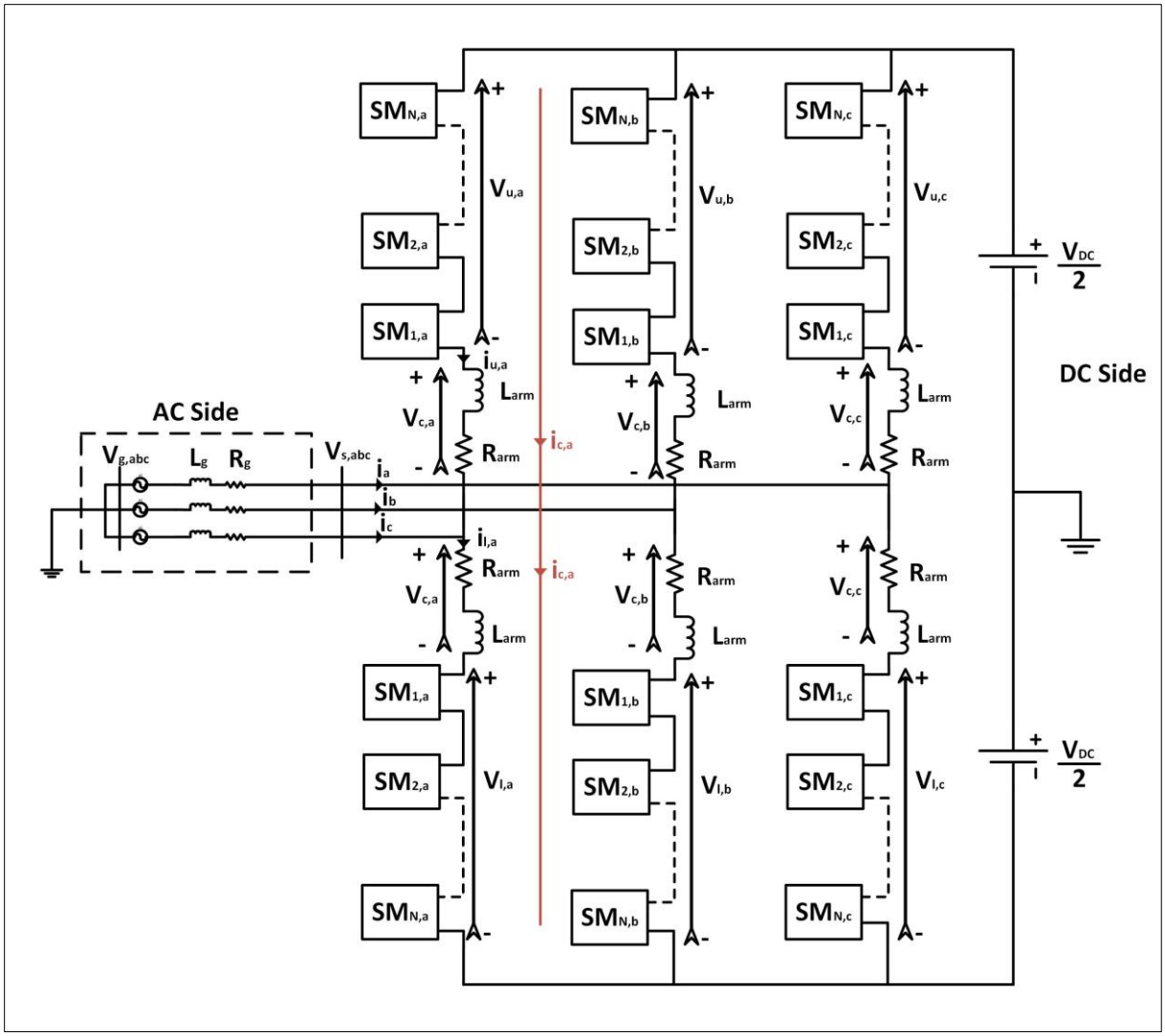


Figure 2.17 Schematic diagram of dynamics in MMC

Applying Kirchhoff's voltage law, the dynamic equations of phase 'a' can be written as,

$$\frac{V_{DC}}{2} - V_{u,a} - R_{arm} i_{u,a} - L_{arm} \frac{di_{u,a}}{dt} + R_g i_a + L_g \frac{di_a}{dt} - V_{g,a} = 0 \tag{2.1}$$

$$-\frac{V_{DC}}{2} + V_{l,a} + R_{arm} i_{l,a} + L_{arm} \frac{di_{l,a}}{dt} + R_g i_a + L_g \frac{di_a}{dt} - V_{g,a} = 0 \tag{2.2}$$

Current through each arm has three components, they are 1. AC side current, 2. DC side current (DC component of circulating current), 3. AC component of circulating current. AC side current is equally divided between upper and lower arm due to symmetry. DC side current is equally divided into three phases. AC component of circulating current is equal in each phase and the reference directions are as shown in the Figure 2.17. The upper and lower arm currents of phase a are expressed as,

$$i_{u,a} = \frac{I_{DC}}{3} + i_{c(AC),a} - \frac{i_a}{2} \tag{2.3}$$

$$i_{l,a} = \frac{I_{DC}}{3} + i_{c(AC),a} + \frac{i_a}{2} \tag{2.4}$$

Where $i_{c(AC),a}$ represents AC component of circulating current in phase a.

Adding and subtracting above two equations: (2.3) + (2.4), (2.3) - (2.4) yield,

$$i_{c(AC),a} = \frac{i_{u,a} + i_{l,a}}{2} - \frac{I_{DC}}{3} \tag{2.5}$$

$$i_a = i_{l,a} - i_{u,a} \tag{2.6}$$

Applying Kirchhoff's voltage law on AC side of MMC

$$R_g i_a + L_g \frac{di_a}{dt} - V_{g,a} = -V_{s,a} \tag{2.7}$$

Adding and subtracting two equations (2.1), (2.2), substituting the values from (2.5), (2.6), (2.7): (2.1) + (2.2), (2.1) - (2.2) yield,

$$L_{arm} \frac{di_a}{dt} = -V_{u,a} + V_{l,a} - R_{arm} i_a - 2V_{s,a} \tag{2.8}$$

$$L_{arm} \frac{di_{c,a}}{dt} = \frac{V_{u,a} + V_{l,a}}{2} - \frac{V_{dc}}{2} + R_{arm} i_{c,a} \tag{2.9}$$

Where $i_{c,a}$ is total circulating current in phase a expressed as,

$$i_{c,a} = i_{c(ac),a} + i_{c(dc),a} = \frac{i_{u,a} + i_{l,a}}{2}$$

Equation (2.8) represents the external dynamics of MMC, whereas equation (2.9) represents the internal dynamics of MMC.

Chapter 3. Modelling

For this master thesis mathematical modelling and Simulink/MATLAB modelling of wind generator side converter using MMC topology and SiC MOSFET is pursued. Mathematical modelling includes the dimensioning of semiconductor devices and various circuit parameters such as arm inductance, sub module capacitance. Simulink/MATLAB modelling includes structure (sub modules, arm inductance), implementation of control methods for internal and external dynamics.

3.1 Dimensioning of Circuit Parameters

MMC with many promising characteristics has found wide variety of medium/high power applications from initially intended HVDC transmission to renewable energy systems to medium voltage electric drives. Such wide range of applications for a single topology makes it challenging to understand the selection of components and circuit operational aspects. The dimensioning of various circuit parameters for different application is studied extensively in literature.

During normal operation, circulating current flows in each arm of MMC. Circulating current has both DC and AC components. DC component is responsible for power transfer through MMC. AC component increases power losses and voltage ripples across submodule capacitors. The AC component contains even order harmonics and needs to be suppressed. There are various control algorithms which reduce the AC component of circulating current. However, they increase complexity of the MMC controller. The AC component of circulating current is strongly dependent on the circuit parameters of MMC, such as: submodule capacitance and arm inductance. Arm capacitance arm inductance form a series resonance circuit in each arm and such resonance must be avoided. Appropriate selection of arm capacitance and inductance based on circulating current resonances and capacitor voltage ripples can drastically reduce the circulating current AC component, converter power losses and submodule capacitor voltage ripples [28]. Such components selection should be carried out at an early stage of the converter design.

3.1.1 Sub Module Capacitance

For MMC (wind generator side converter), sum of the sub module capacitor voltages in one arm is equal to the DC side voltage.

$$V_{SM} = \frac{V_{DC}}{N_{SM}} \tag{3.1}$$

Where V_{SM} is sub module capacitor voltage, V_{DC} is DC side voltage, N_{SM} is number of sub modules in one arm. This formula is valid with the assumption of balanced sub modules.

The selection of the SM capacitor is a compromise between the capacitor size, cost and the voltage requirements. The capacitance of the SM capacitor can be calculated based on desired voltage ripple factor having a value between 0 and 1 [29].

$$C_{SM} = \frac{\Delta W_{SM}}{2 * \varepsilon * V_{SM}^{2}} \tag{3.2}$$

Where ε is voltage ripple factor, ΔW_{SM} is the energy change in one SM estimated by

$$\Delta W_{SM} = \frac{2}{3} \frac{S}{(k * \omega_n * N_{SM})} \left(1 - \left(\frac{k * \cos(\varphi)}{2} \right)^{2} \right)^{\frac{3}{2}} \tag{3.3}$$

where S is the apparent power of the converter, ω_n is the output angular frequency, k is the voltage modulation index, and cos(φ) is power factor.

3.1.2 Arm Inductance

There are two main objectives that needs to be considered while selecting the value of the arm inductors in the MMC. The first is to suppress high frequency components of the arm currents caused by differences in upper and lower arm voltages. These differences can exist for example, due to different switching times of converter switches. The second is limiting the fault current during short circuit between the DC link terminals. The value of the arm inductance depends on the submodule capacitor voltage, the modulation technique, the switching frequency and an additional controller optionally used for suppressing the circulating current. The arm inductance is usually selected depending on the value of cumulative arm capacitance, in such a way that second order harmonic is eliminated. The value of arm inductance is calculated using the following formula. The reader may refer [28] for detailed assumptions and derivation.

$$L_{arm} = \frac{1}{C_{arm} * \omega^2} \frac{2\left(h^2 - 1\right) + m_a^2 h^2}{8\, h^2 \left(h^2 - 1\right)} \tag{3.4}$$

where h is the harmonic order (h=2n, n=1,2,…,∞), ω is angular frequency (ω = 2π·50 Hz = 314.15 rad/s), m_a is modulation index and L_{arm}, C_{arm} are the arm inductance and capacitance at which the resonance occurs. The value of arm inductance depends on the fundamental angular frequency ω, its harmonic order h, and the modulation index m_a, apart from arm capacitance. Typically, all these parameters are constant during the converter steady state operation. The arm inductance is usually selected depending on the value of cumulative arm capacitance, in such a way that second order harmonic is eliminated.

The maximum value of arm inductor is derived considering current derivative during DC faults is calculated with the following formula.

$$L_{arm\_\max} = \frac{V_{DC}}{\left(dI_{DC}/dt\right)_{critical}} \tag{3.5}$$

The critical current for the semiconductor devices is provided in the datasheets. The value of arm inductance can be obtained by inserting the value of critical current. Therefore, the maximum inductance value is lying in more broad range than the value of resonance inductance. Generally the value of arm inductance lies in the range of 0.5 to 0.15 per unit of the MMC rating [30] [31].

3.1.3 Semiconductor Devices

The main dimensioning factor of semiconductor devices is power rating. That is, the product of the rated voltage and the rated current. The semiconductor devices must be able to withstand the voltage of one submodule capacitor. For safety purposes, the actual voltage rating of the semiconductors would be chosen higher than the maximum expected operating voltage with a safety margin of 50%. This implies the semiconductor device voltage rating is 1.5 times that of maximum expected operating voltage. However, in order to quantify the semiconductor requirements in such a way that different topologies can be compared, the power rating is assumed to be equal to the product of the maximum expected operating voltage and the expected peak current. The maximum expected operating voltage of each semiconductor device, V_{rated}, is found by multiplying the nominal submodule voltage with the allowed increase in the capacitor voltages,

$$V_{rated} = \frac{V_{DC}}{N} k_{\max} \tag{3.6}$$

Where k_{max} indicates the safety margin to be allowed. For example, the value of k_{max} is 1.5 for a safety margin of 50%. The expected peak current I_{rated} is found by the following formula

$$I_{rated} = \hat{i}_s \left(\frac{1}{2} + \frac{1}{4} m \cos(\varphi) \right) \tag{3.7}$$

Where m is modulation index, $\cos(\varphi)$ is the power factor. The power rating of each semiconductor device is derived by the product of voltage and current,

$$P_{rated} = \frac{V_{DC}}{N} \left(\frac{1}{2} + \frac{1}{4} m \cos(\varphi) \right) k_{\max} \hat{i}_s \tag{3.8}$$

The combined power rating of all semiconductor switches in the converter is obtained by multiplying rated power of each semiconductor switch with the number of switches in the MMC. As each submodule has two switches and there are six arms, each arm with *N* submodules, the total number of switches in the converter is 12N. Also using formula of modulation index ($m = V_{Speak}/(V_{DC}/2)$) gives that the total power rating,

$$P_{rated,MMC} = \frac{16S}{m} \left(\frac{1}{2} + \frac{1}{4} m \cos(\varphi) \right) k_{\max} \hat{i}_s \tag{3.9}$$

Where, S is apparent power rating, $S = 3\left(\frac{\hat{V}_s \hat{i}_s}{2} \right)$

The reader may refer [32] for detailed understanding.

In MMC, switching losses are negligible due to lower switching frequency of the semiconductor switches. However, conduction losses in MMC may make thermal limitation as one of the dimensioning factors. For this master thesis, three SiC MOSFETs are considered, which are available in the commercial market. The usable voltage rating is chosen as less than or equals to $2/3^{rd}$ of actual voltage rating of the SiC MOSFETs. The usable current rating is calculated with the assumption of maximum operating junction temperature of 125°C. These steps are explained in detailed in the later Sections.

3.1.4 Other Parameters

In this report, the influence of the arm resistance R_{arm} on resonance frequencies or on the circulating current is not investigated. Therefore, the value of arm resistance should be kept as low as possible to reduce the converter power losses regardless of the application. Value of the arm resistance R_{arm} of 100 mΩ is used for this project.

The reader may refer to Table I in Zygmanowski et al. [28], to get a brief idea about the range of values used in various literature. It is also interesting to see the initial approach for modelling of MMC by A Lesnicar et al. [33]. There are several advanced dimensioning ways proposed in literature for specific application under unbalanced conditions and during faults such as [34].

3.2 Modulation Techniques

In this Section, the basics of various modulation methods proposed in literature are introduced.

3.2.1 Pulse Width Modulation Techniques

The basic principle of PWM modulation is generating switching states by comparing a reference waveform with a high frequency triangular carrier waveform. In a two-level VSC, there are two switches in each phase leg and one carrier waveform is needed to control two switches (upper and lower switch) with opposite switching states. However, there are 2N sub modules in each phase leg of MMC corresponding to N+1 voltage levels. Thus, N carrier waveforms are needed to control 2N switches (N switches in upper arm, N switches in lower arm). As the number of total inserted SMs in each phase leg is N, each carrier waveform control two SMs (one in upper arm and one in lower arm) with opposite switching states. There are two main PWM techniques by using one single reference waveform: Carrier-Disposition PWM (CD-PWM) and Carrier Phase Shifted PWM (CPS-PWM) [13] [35].

3.2.1.1 CD-PWM

This technique require N identical triangular carrier waveforms displaced symmetrically with respect to the zero axis for each phase of MMC. Each carrier will be compared with the phase voltage reference waveform to produce the desired phase voltage level. The resulted switching states are used to control an upper SM and its corresponding lower SM. Thus, independent SM modulation is achieved. According to the phase shift among carrier waveforms, CD-PWM can be further classified into phase disposition (PD), phase opposition disposition (POD) and alternate phase opposition disposition (APOD). These carrier waveforms are shown in

Figure 3.1.

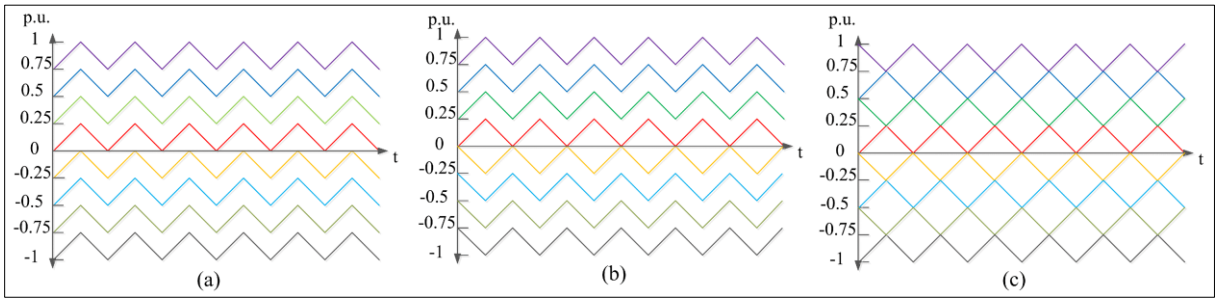


Figure 3.1 CD-PWM methods (a) PD, (b) POD, (c) APOD

The main disadvantage of using these techniques is unequal distribution of voltage ripple among the SM capacitors that results in large circulating currents and impact the harmonic distortion of the AC side voltages. Hence these techniques should be used together with SM capacitor voltage balancing methods, that are discussed in later sections. To improve the harmonic distortion of the AC side voltages, various carrier rotation/signal rotation techniques are proposed in literature to equalize the voltage distribution among all the SM capacitors. Despite proposed SM capacitor voltage balancing methods, the THD is relatively high. To improve the performance further, several modifications are proposed for CD-PWM for better integration of SM capacitor voltage balancing techniques. The reader may refer [35] for details and references.

3.2.1.2 CPS-PWM

This technique requires N identical triangular or sawtooth carrier waveforms for each arm of MMC. As shown in the Figure 3.2, the carrier waveforms are phase shifted by an angle equals to $360^o / N$ with respect to each other. A detailed analysis and comparison of CPS-PWM, PD-PWM is not pursued during this project.

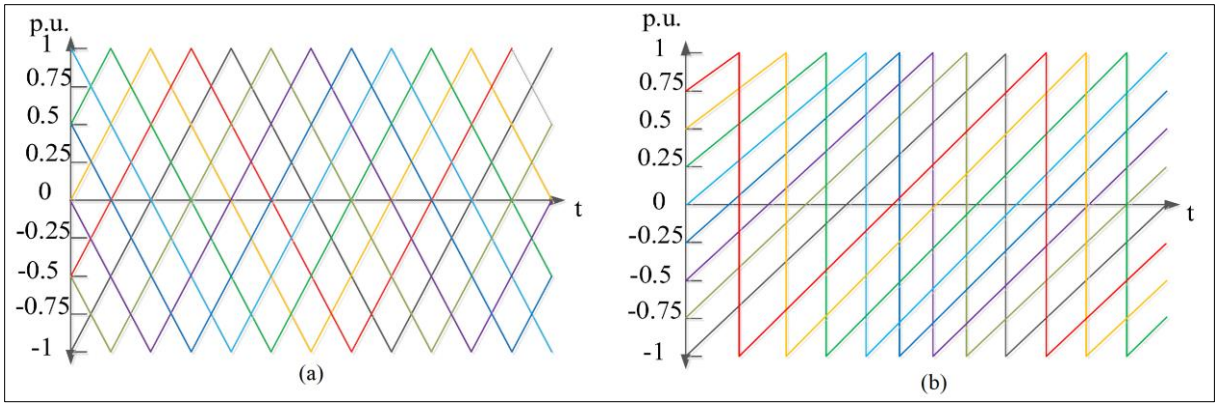


Figure 3.2 CPS-PWM (a) Triangular waveforms, (b) Sawtooth waveforms

3.2.1.3 Multiple Reference-Based Modulation

There are several modulation techniques based on using multiple reference waveforms. These modulation techniques include

1. Direct Modulation
2. Indirect Modulation
   a) Closed Loop Control
   b) Open Loop Control

In direct modulation technique, the upper and lower arm voltages of each phase are controlled by two complementary sinusoidal reference waveforms for the number of inserted sub modules in upper and lower arms. The insertion index is defined as

$$n_{l,u} = \frac{1 \pm m_a \sin(\omega t)}{2}, \left\{ m_a = 2\hat{V}_s / V_{DC} \right\} \tag{3.10}$$

Where $n_{l,u}$ is lower and upper insertion index respectively, m_a is modulation index, V_s is AC side voltage, V_{DC} is DC side voltage of MMC. These sinusoidal waveforms are compared with carrier waveforms to generate switching states. The main disadvantage of the direct modulation technique is presence of circulating currents (with predominant second harmonic), which increase the converter power losses and rating values of the components.

In indirect modulation, the main objective of insertion index for upper and lower arms is to compensate for sub module capacitor voltage ripple, thus suppressing the circulating current. The insertion index is defined as $n_{u,l} = V^*_{cu,l} / V^{\Sigma *}_{cu,l}$. Indirect modulation is further classified into two types based on the way of calculating the insertion indices. The first is closed loop control, where sum capacitor voltages need to be measured to calculate the insertion indices. The main disadvantage in closed loop control is time delay in capacitor voltage measurements. The second is open loop control, where capacitor voltages are estimated to eliminate the higher order harmonics in capacitor voltage ripple, thus suppressing the circulating current. The open loop control is elaborated in the later sections. The reader may refer Chapter 3 of [36] for detailed derivation and explanation.

3.2.2 Other Modulation Methods

Apart from mentioned PWM techniques, several other techniques are proposed in literature with various objectives. A selective harmonic elimination (SHE) PWM technique is proposed, where the switching states are determined to eliminate the low-order harmonics of the output

voltage waveform. A nearest level control (NLC) modulation technique is proposed, where the voltage level nearest to the desired voltage waveform is selected. Compared to the SHE-PWM, the NLC technique is easy to implement, requires less computational efforts, and uses a lower switching frequency when compared to the PWM techniques [13]. Space Vector Pulse Width Modulation (SVPWM) provides more flexibility to optimize switching waveforms with redundant switching states and adjustable duty cycles. It is suitable for digital implementation. The main disadvantage of SVPWM is that the complexity of algorithm increases with increase in number of submodules per arm, i.e. voltage levels [37].

CPS-PWM with triangular carrier waveforms with multiple reference waveforms is chosen for this project. The CPS-PWM block in Simulink is modified to suit the reference signal used.

3.3 Control Methods

The main parameters that needs to be controlled in MMC are voltages and currents at its terminals depending on the intended application. In this project, the MMC is designed for wind generator side converter (rectifier) in an all DC series connected wind farm. The MMC works as an energy interface between input and output using the sub module capacitors as energy storage elements. The primary objective is to control the steady state average capacitor voltage for stable operation. Additionally, there are secondary control objectives such as the circulating current suppression and equalizing stress on the sub module capacitors, low switching losses, etc. Therefore, the control of the MMC can be divided into two classes, they are internal dynamics and external dynamics. Internal dynamics involve sub module capacitor voltage balancing and circulating current suppression etc. External dynamics include voltage and current control on input and output side [11]. Figure 3.3 shows the schematic diagram of control system developed for the current project.

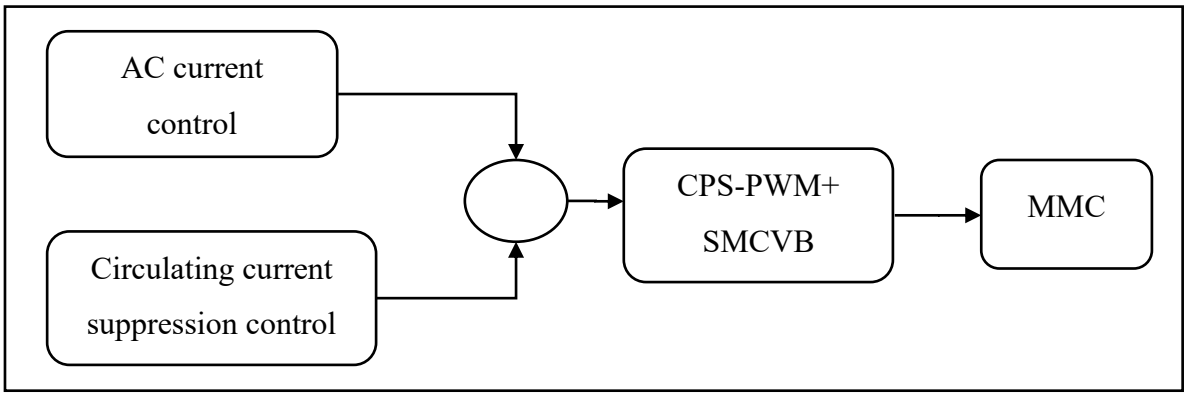


Figure 3.3 Schematic diagram of MMC control system

3.3.1 Internal Dynamics

3.3.1.1 SM Capacitor Voltage Balancing (SMCVB)

The voltages of the sub module capacitors change depending on the current flowing through the SM. The voltage of individual sub module capacitor should be kept approximately equal to its theoretical value V_{DC}/N. For this, the SM voltage must be measured and the appropriate SM capacitor voltage balancing measures must be taken. Otherwise, the unbalancing among sub module capacitor voltages will increase and the output voltage cannot be controlled [38].

Several capacitor voltage balancing algorithms have been proposed in literature. The most commonly used algorithm chooses the SMs that must be ON based on the direction of the arm current and sub module capacitor voltages. A combination of the averaged control and the balanced control is proposed by M. Hagiwara et al. [5]. A predictive control, based on minimizing a cost function can be used for capacitor voltages balancing, circulating currents suppression and the output current control under various operating conditions [39]. A method, where arm current does not need to be measured eliminates current sensors, thus reducing costs and simplifying the voltage balance control algorithm is proposed by Deng et al. [40]. For this master thesis, the following three methods are explored,

1. Sorting algorithm including reduced switching frequency voltage balancing by Tu et al. [41]
2. Averaged control along with the balanced control by M. Hagiwara et al. [5]
3. Open loop voltage/energy control with ripple estimation by Lennart Ängquist et al. [42]

3.3.1.1.1 Sorting Algorithm

The sorting algorithm is the most widely used method for SM capacitor voltage balancing. The selection of the SMs to be inserted is performed based on this SM capacitor voltage balancing algorithm. This balancing algorithm is implemented in each arm of MMC and the switching pulses are generated based on SM capacitor voltage measurements and the direction of arm current. The gate signals are updated at the sampling control frequency. The selection of SMs according to conventional sorting algorithm as follows,

- If the arm current is charging the SM capacitors, SMs with the lowest voltages are inserted so that the capacitors are charged, and their voltages increase

- If the arm current is discharging SM capacitors, SMs with the highest voltages are inserted so that the capacitors are discharged, and their voltages decrease

If the SMs are bypassed, no current flows through the SM capacitor and hence the voltages will not change. This algorithm is simple and easy to implement. However, this results in increased switching frequency, which increases switching losses. Various modifications are proposed to reduce the switching frequency. One such Reduced Switching Frequency (RSF) algorithm is proposed in [41], is as shown in Figure 3.4.

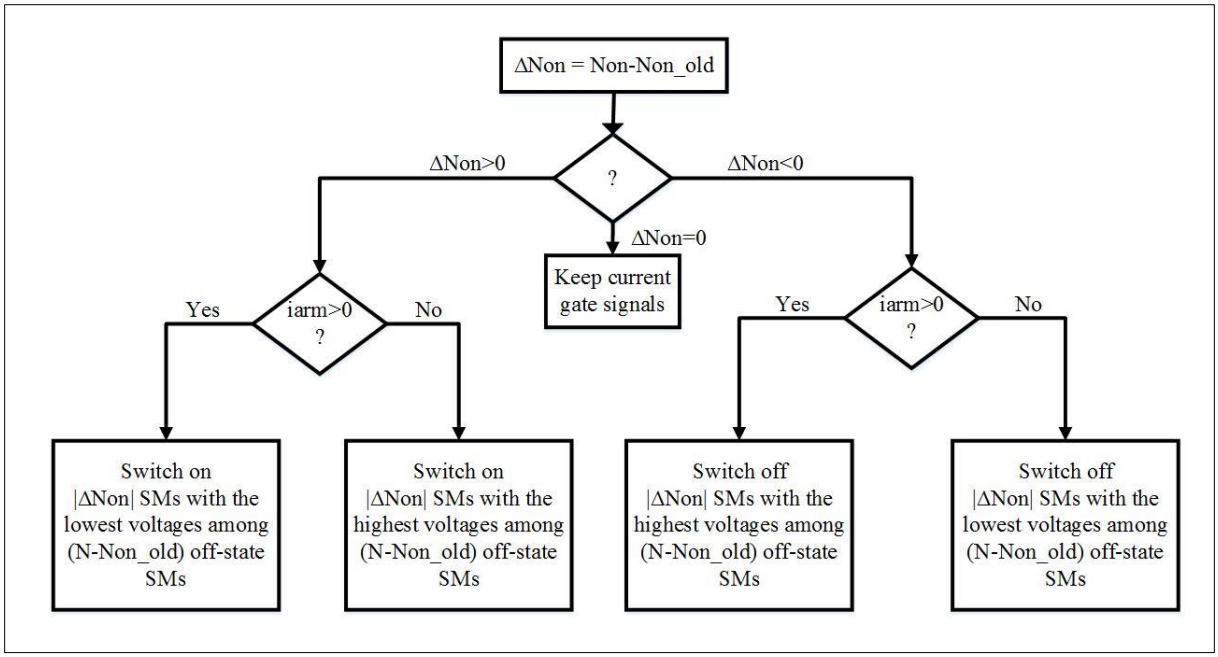


Figure 3.4 RSF SM Capacitor Voltage Balancing Algorithm

Where N_{on_old} is the number of SMs that are inserted in the previous control cycle, N_{on} is the newly calculated number of sub modules. ΔN_{on} is the additional number of SMs, that need to be switched on when positive (or switched off when negative) in the following control cycle. i_{arm} is the corresponding arm current, is positive when charging the capacitors and negative when discharging the capacitors. The RSF voltage-balancing algorithm is summarized as follows,

- If additional SMs need to be switched on during the following control cycle (i.e. ΔN_{on} is positive), no switching is applied to the SMs inserted. The conventional sorting algorithm mentioned before will only be applied to those SMs bypassed.
- If some of the SMs inserted need to be switched off during the following control cycle (i.e. ΔN_{on} is negative), no additional SMs that are currently bypassed will be switched on. The conventional sorting algorithm mentioned before will only be applied to the SMs inserted.

Compared to the conventional method, the proposed RSF voltage balancing algorithm significantly reduces the average device switching frequency and the total switching losses of the converter. However, it sacrifices the voltage balancing.

Several advanced sorting algorithms based on predictive control, a combination of RSF algorithm and predictive control (hybrid balancing algorithm), fundamental switching frequency algorithms have been proposed in literature. However, for this project, conventional sorting algorithm is adopted for ease of implementation and due to the fact that the switching losses of SiC MOSFET are negligible.

3.3.1.1.2 Averaging + Balancing

The block diagram of averaging control and balancing control is shown in Figure 3.5. In averaging control, average phase sub module capacitor voltage follows the command i.e, theoretical reference value (V_{DC}/N_{SM}) and circulating current follows the command i_c (Ref.) i.e, output of first PI controller. The voltage reference obtained through averaging control for a given phase is V_A. The gains of PI controller are calculated by trial and error method.

In balancing control, the individual sub module capacitor voltage follows the command V_C i.e, theoretical reference value (V_{DC}/N_{SM}). The voltage reference obtained through balancing control is V_B for individual capacitor. The polarity of V_B is changed according to the polarity of i_{arm} (upper arm current/lower arm current).

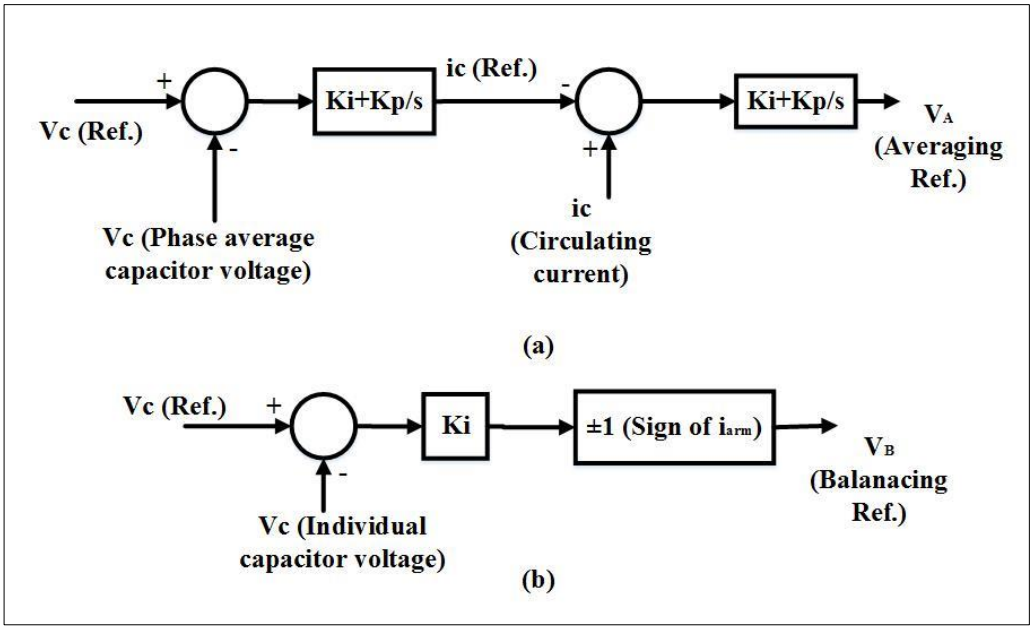


Figure 3.5 Block diagram of (a) Averaging control (b) Balancing control

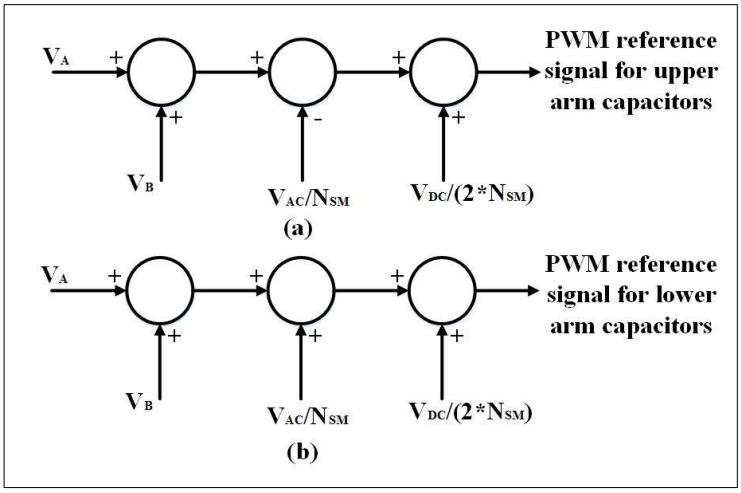


Figure 3.6 Voltage command of (a) Upper arm (b) Lower arm

The voltage reference signals for PWM are generated as shown in the Figure 3.6 (a) and (b) for the individual sub modules in upper and lower arm respectively. This voltage reference signal is compared with a triangular carrier waveform with a carrier frequency f_C, in order to generate the gate signals for individual sub modules of MMC.

For a detailed understanding, the reader may refer Hagiwara et el. [5].

3.3.1.1.3 Open Loop Voltage/Energy Control with Ripple Estimation

In this Section, an open loop controller is suggested to calculate the insertion index (number of sub modules inserted in each arm divided with number of sub modules available in each arm), based on the estimation of stored energy in upper/lower arm and capacitor voltage ripple of one phase. This estimation is based on the voltage reference and the measured phase current of the corresponding phase. The DC side voltage appears as a parameter in this approach. The insertion indices are described as,

$$n_{u,l} = \frac{v_{cu,l}}{v^{\Sigma}_{cu,l}} \tag{3.11}$$

Where, $v_{cu,l}$ is the reference for inserted voltage by upper/lower arm. In stable and balanced operation of MMC, $v_{cu,l}$ is expressed as,

$$v_{cu,l} = \frac{V_{DC}}{2} \mp v_s - v_c \tag{3.12}$$

Where V_{DC} is the DC side voltage, V_S is the internal converter voltage, V_C is the voltage that drives circulating current. And $v^{\Sigma}_{cu,l}$ is sum of all sub module capacitor voltages in upper/lower arm. It is calculated based on the estimation stored energy in upper/lower arm as,

$$v^{\Sigma}_{cu,l} = \sqrt{\frac{2NW^{\Sigma}_{cu,l}}{C}} \tag{3.13}$$

Where N is the number of sub modules available in each arm, C is sub module capacitance, $W^{\Sigma}_{cu,l}$ is energy stored in all the capacitors of upper/lower arm. The calculation of $W^{\Sigma}_{cu,l}$ is as shown in the Figure 3.7. The detailed estimation of $W^{\Sigma}_{cu,l}$ considering sub module capacitor voltage/energy ripple is explained by Lennart Ängquist et. al. [42] or in Chapter 3 of [36].

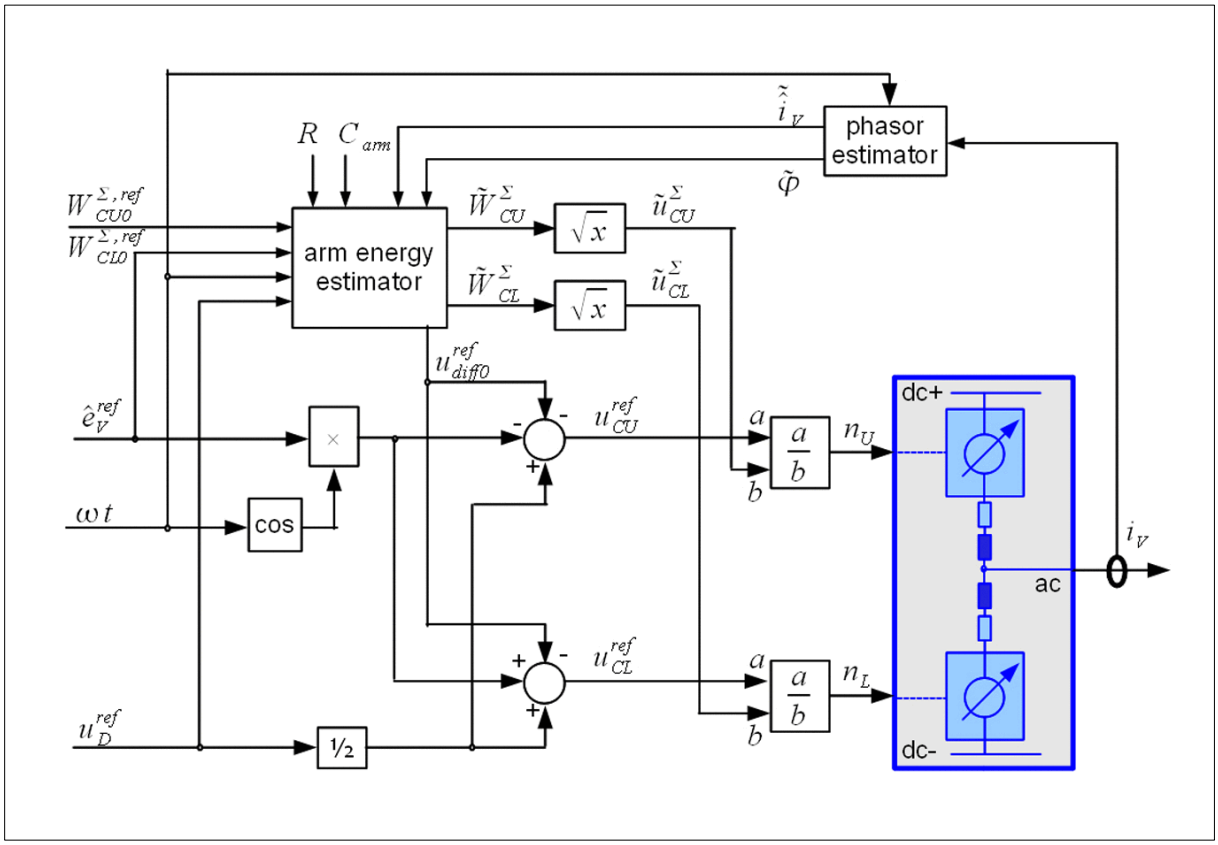


Figure 3.7 Block diagram of open loop controller [42]

All the three methods presented for sub module capacitor voltage balancing has been implemented in the MATLAB/Simulink environment. However, for simplicity and to reduce the computations and simulation time, only simple sorting algorithm has been used. This is due to the fact that sixty number of simulations are carried by varying the number of sub modules and number of parallel connected semiconductor devices as presented in the later sections.

3.3.1.2 Circulating Current Suppression Control (CCSC)

The circulating current has two components 1. DC component and 2. AC component. The DC circulating current component is equal to one-third of the total DC side current and is responsible for power transfer from AC to DC and vice versa. However, AC component with a predominant second harmonic increase the rms values of the arm currents and, thus, result in higher converter power losses. Hence AC component of circulating current needs to be suppressed. The AC component of circulating current in the MMC is generated by the sub module capacitor voltage unbalancing and the voltage difference between upper arm and lower arm of individual phase leg. This AC circulating current component tries to contain the voltage unbalancing, that caused it.

In each phase leg, the sub module capacitor voltages have ripple with a major fundamental component. This fundamental component produces second-order harmonic in the output voltage of the SMs, that causes second-order harmonic in the circulating current, which is negative sequence and flows through the DC side and the phase leg, leading to the unbalance of capacitor voltage. Without proper control, the amplitude of the second-order circulating current can be significant, and it triggers fourth-order current harmonic, which is positive sequence. The fourth-order circulating current triggers sixth-order current harmonic which is zero-sequence, extension as the before. FFT analysis of circulating current indicates that the circulating current only has even-order harmonics. The harmonics in the circulating current increase power losses and reduce service life of power devices. Moreover, they cause instability during transients, and threaten the safety of the power devices and capacitors [41] [43].

The circulating current can be suppressed through hardware or software. In hardware, increasing the value of arm inductors can reduce the circulating current passively. However, this cannot eliminate it, and the dynamic response characteristic may be degraded. Besides, the cost and size of the system may increase. Based on software methods, many control strategies are proposed. A pair of PI controllers based on the second fundamental frequency, negative sequence rotational reference frame were proposed in [41]. It is efficient to eliminate the second-order harmonic, but it cannot eliminate the higher-order harmonics. To eliminate all even-order harmonics, Z Li et al. [44] proposed a method based on Proportional-Resonant (PR) controllers, one PR controller to eliminate each even order harmonic present in the circulating current. However, it needs too many PR controllers to eliminate all the even order harmonics present, and it is not pragmatic. H Ji et al. [43] proposed a pragmatic method to eliminate second and fourth order harmonic components, which are predominant. For this master thesis, two

alternatives are explored. One is proposed by Tu et al. [41] as shown in Figure 3.8 and the Figure 3.9 shows the effectiveness of circulating current suppression controller. Second is a simple PI controller as shown in Figure 3.10, where the circulating current reference is the DC component of each phase. Modulus optimum method and PID tuner in MATLAB are explored for tuning the controller. However, the gain values obtained through these methods are not found efficient due to inaccuracies in modelling the system transfer function. The PI controller is tuned by trial and error method, to make sure the output is 10% to 20% of the reference signal to PWM. Figure 3.11 shows the plot of circulating current with/without controller. It can be observed that circulating current component is varying about the DC reference and is suppressed. The simple PI controller is found efficient for this master thesis.

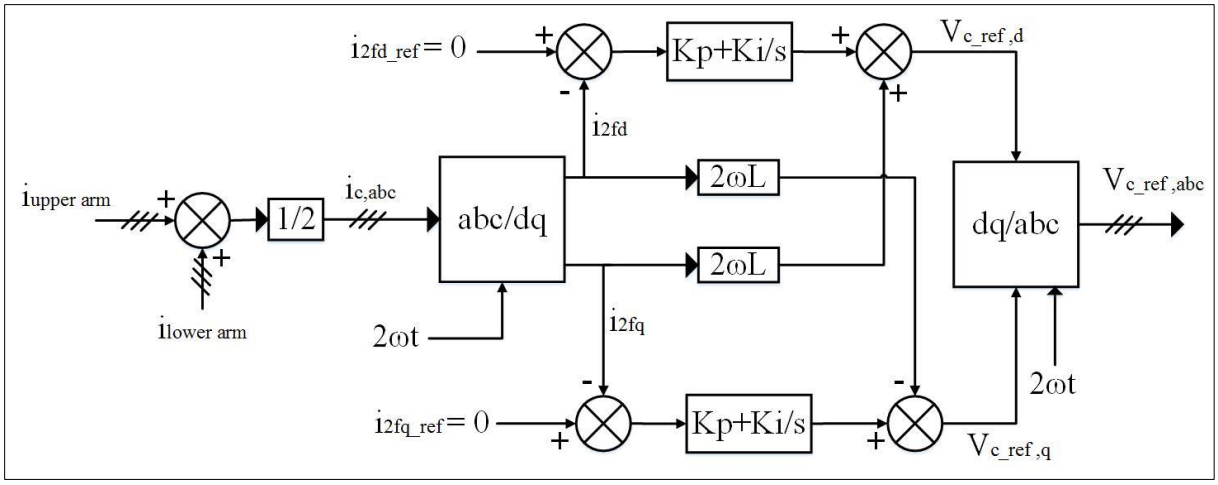


Figure 3.8 Block diagram of circulating current suppressing controller

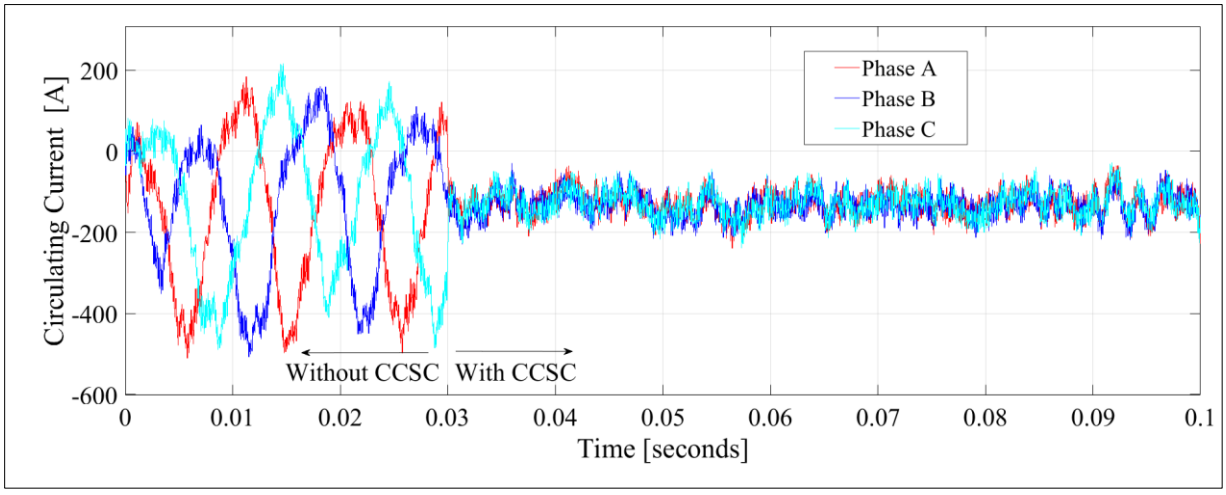


Figure 3.9 Circulating current without/with CCSC

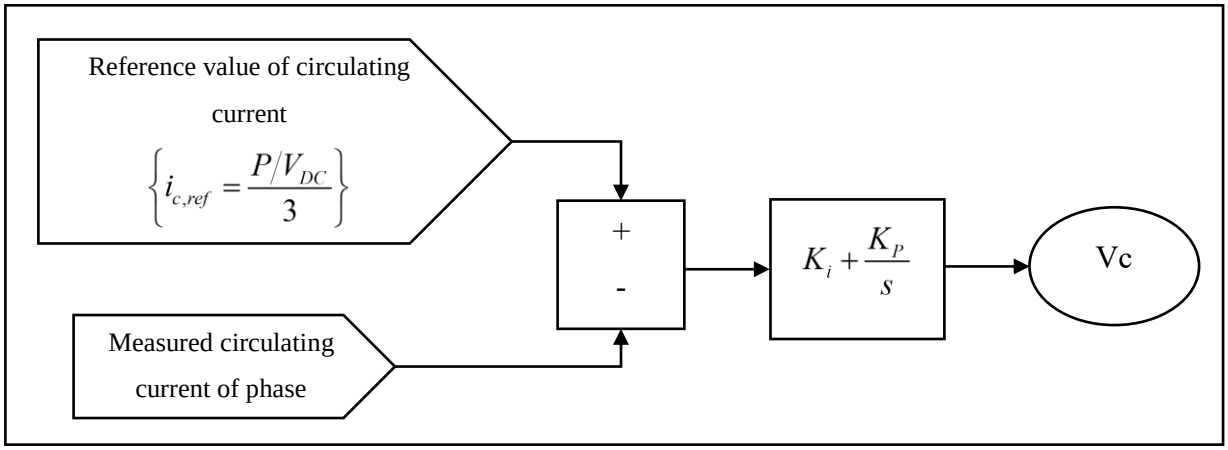


Figure 3.10 Block diagram of circulating current suppression controller

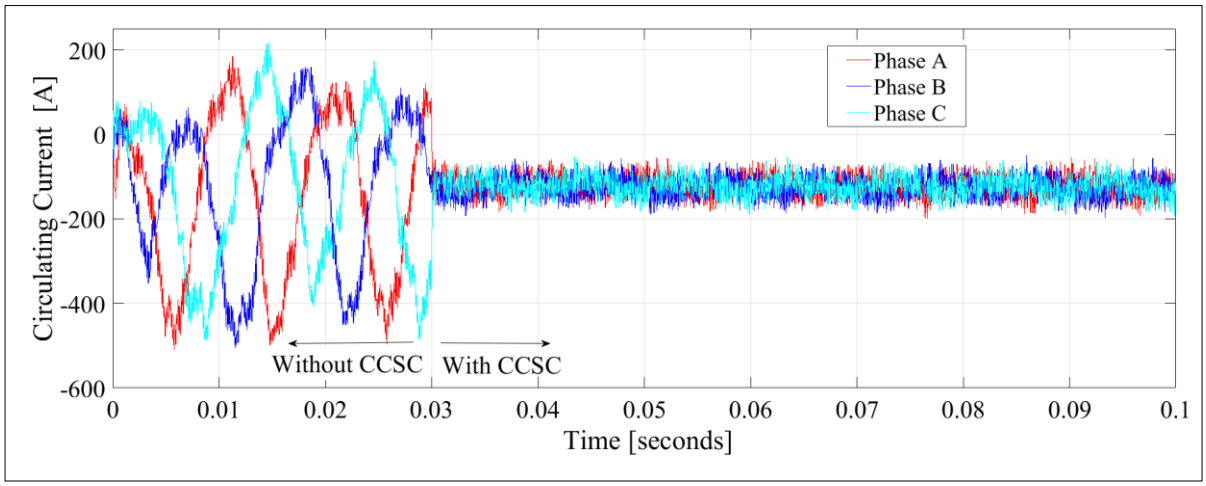


Figure 3.11 Circulating current without/with CCSC

3.3.2 External Dynamics

3.3.2.1 AC Current Control

The AC side dynamics of phase a of MMC are presented based on the Figure 2.17,

$$R_g i_a + L_g \frac{di_a}{dt} = V_{g,a} - V_{s,a} \tag{3.14}$$

This can be transformed into dq state-space form in order to control active power and reactive power independently as,

$$R_g i_d + L_g \frac{di_d}{dt} = V_{g,d} - V_{s,d} + \omega L i_q \tag{3.15}$$

$$R_g i_q + L_g \frac{di_q}{dt} = V_{g,q} - V_{s,q} - \omega L i_d \tag{3.16}$$

Where, $V_{g,d}$ and $V_{g,q}$ are grid voltages in dq state-space form respectively. $V_{s,d}$ and $V_{s,q}$ are MMC output voltage on AC side in dq state-space form respectively. i_d, i_q are AC side current in dq state-space form respectively. $\omega L i_d$ and $\omega L i_q$ are coupling terms. The AC current control can be realized base on the above equations 3.15 and 3.16 as shown in the Figure 3.12.

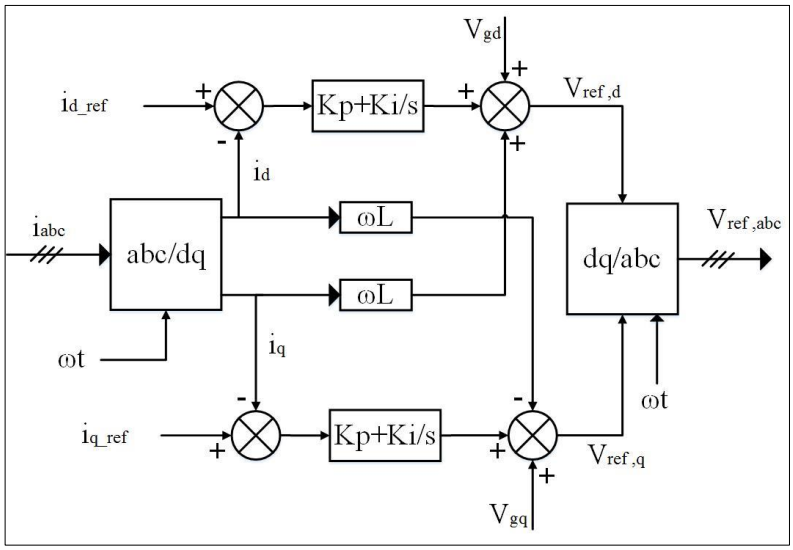


Figure 3.12 Block diagram of AC current controller

Similar to circulating current suppression controller, modulus optimum method and PID tuner in MATLAB are explored for tuning the AC current controller. However, the gain values obtained through these methods are not found efficient due to inaccuracies in modelling the transfer function. The PI controller is tuned by trial and error method.

3.4 Summary of Simulink/MATLAB Model

In this Section, the MATLAB/Simulink model used for simulations is briefly summarized. In this project, the study was focused on the wind generator side converter implemented using MMC topology. On the AC side, MMC is connected to a three-phase grid through grid impedance. The DC side of MMC is represented by two DC voltage sources with midpoint connected to the ground, assuming that the other MMC in an all DC series connected wind farm configuration keeps the DC bus voltage constant. The schematic diagram of the system implemented in Simulink/MATLAB environment is shown in Figure 3.13.

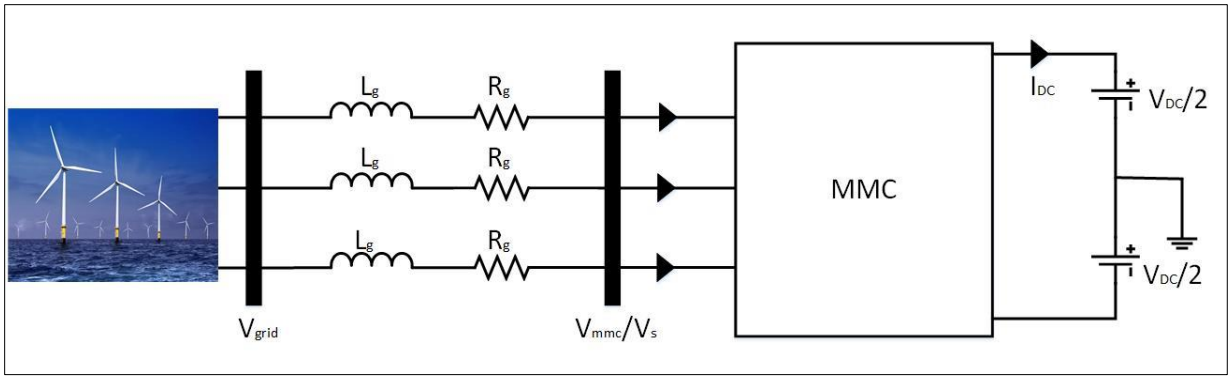


Figure 3.13 Schematic diagram of the Simulink/ MATLAB model

The parameters of MMC such as arm inductance, number of sub modules per arm, sub module capacitance etc. are calculated according to the method described in the above Sections. A simple control system is implemented, as the main objective of the project is to focus on the study of semiconductor device characteristics such as losses, operating junction temperature and total harmonic distortion etc.

Table 3.1 Circuit parameters of MMC

Parameter	**Abbreviation**	**Value**
AC side voltage (LLRMS)	$V_{AC,LLRMS}$	3300 V
DC side voltage	V_{DC}	9000 V
Active Power	P	2 MW
Carrier frequency	f_c	1000 Hz
Sampling time	T_S	10E-6

3.4.1 Summary of Control Methods

- Modulation Technique
  - Carrier Phase Shifted Pulse Width Modulation
- Sub Module Voltage Balancing Algorithm
  - Sorting algorithm
- Circulating Current Suppression Control
  - Simple PI control with DC circulating current component as reference
  - dq state-space PI control to eliminate second order harmonic

- Open loop voltage/energy control with capacitor voltage ripple estimation

- AC Current Control
  - dq state-space PI control

Snapshots of Simulink/MATLAB model including control methods are presented in the Appendix.

Chapter 4. Optimization Criteria

The wind turbine capacity is increasing beyond 10 MW, with General Electric announcing 12 MW wind turbine recently. For such high power levels every aspect of wind energy conversion system needs to be optimized to achieve maximum efficiency at system level. The possible areas of optimization in wind energy conversion system are shown in Figure 4.1. In this research work, the optimal number of sub modules and parallel connected semiconductor devices in modular multilevel converter (intended to work as a wind generator side converter) is pursued with respect to semiconductor power losses, total harmonic distortion, operating junction temperature.

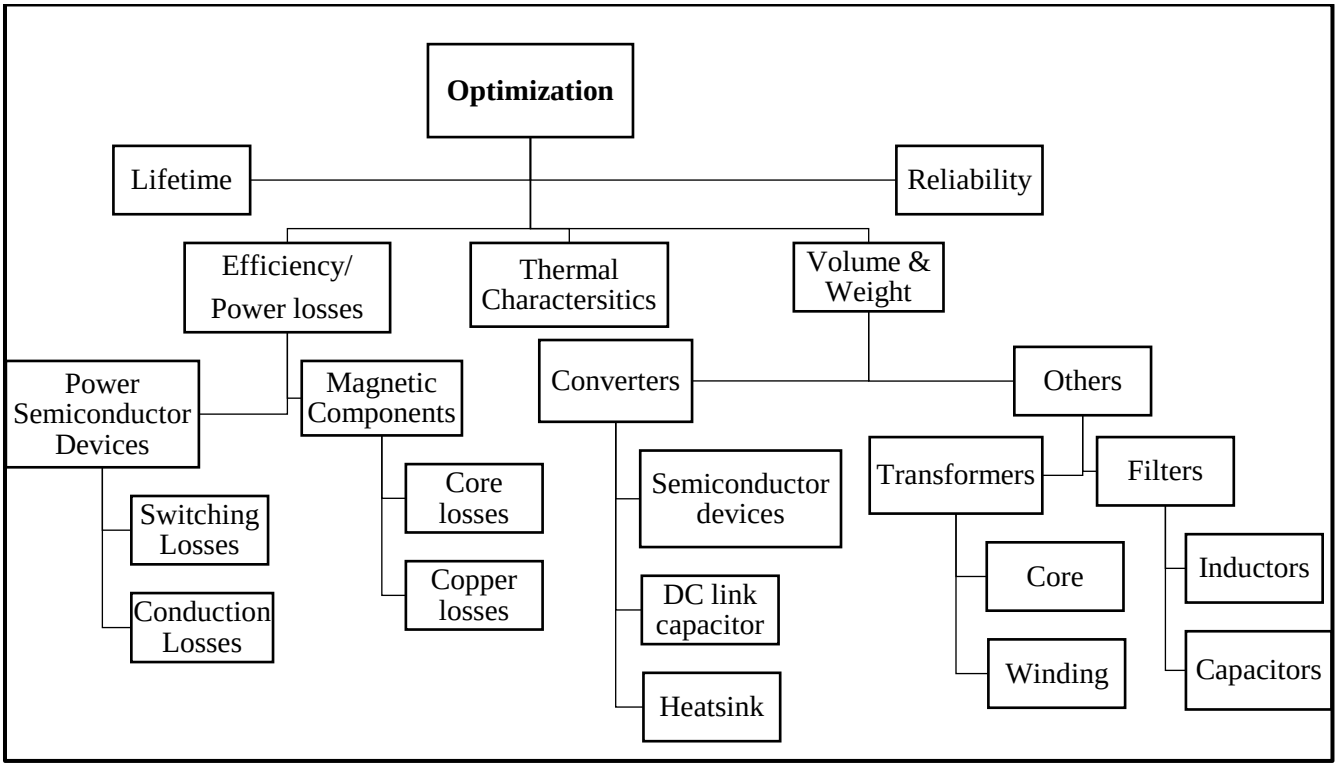
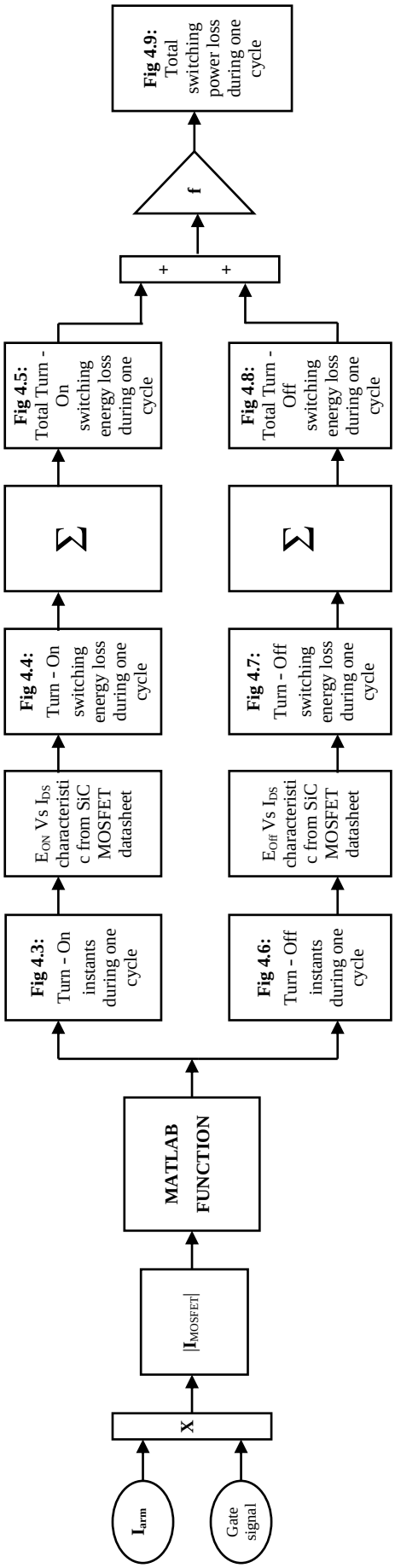


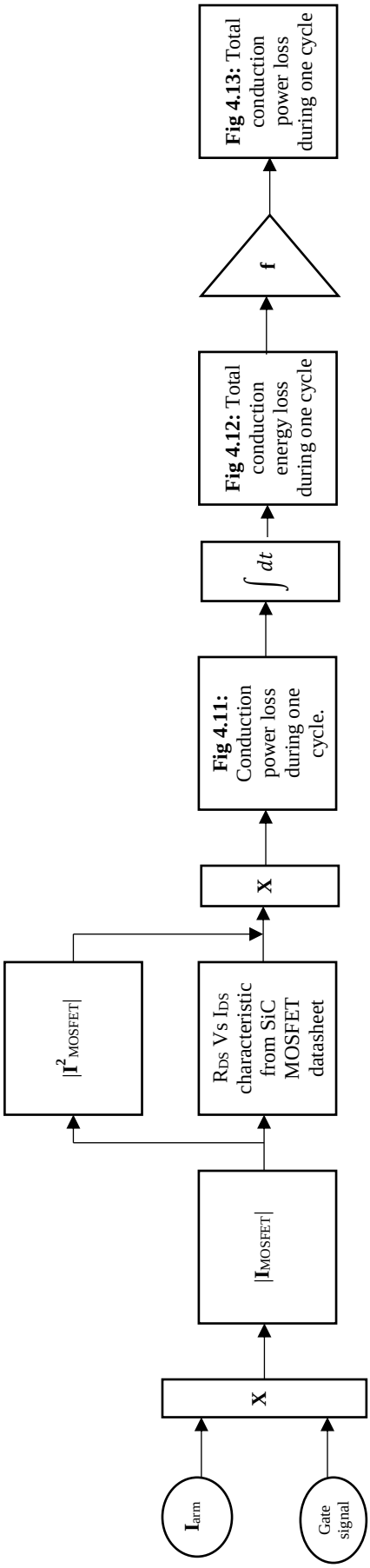
Figure 4.1 Possible areas of optimization in WECS [4].

4.1 Semiconductor Power Loss Calculation

The semiconductor power losses in MMC are calculated based on the simulated voltage and current waveforms, the semiconductor specifications from the manufacturer. In this project, three different SiC MOSFETs made by Wolfspeed (A Cree Company) are used. The specifications of three SiC MOSFETs are provided in the datasheets, that can be downloaded from company website using the model number. The characteristic curves of the SiC MOSFET



Flow Chart 4.1 SiC MOSFET switching power loss calculation



Flow Chart 4.2 SiC MOSFET conduction power loss calculation

required for the conduction and switching losses calculation are approximated, in order to be programmed in Simulink/ MATLAB environment.

4.1.1 Switching Power Losses

The switching power losses are generated during the transition of state of MOSFET from off-to-on and on-to-off, due to the nonzero values of drain to source current and drain to source voltage. The switching could be obtained mathematically by the product of nonzero values of drain to source current and drain to source voltage during switching transitions. The intrinsic parasitic capacitance of MOSFET stores energy and dissipates energy during each switching transition. The switching power losses are proportional to the switching frequency and the values of the parasitic capacitances. The value of intrinsic parasitic capacitance of MOSFET increases with its physical size, which results in increased switching power losses. Generally, MOSFET has much lesser switching losses compared to IGBT. SiC MOSFET is much smaller than Si counterpart and hence lower parasitic capacitance, lower switching losses. In this project, modular multilevel converter is used as wind generator side converter. In modular multilevel converter, sub module switching frequency is approximately $1/N_{SM}$ of carrier switching frequency, where N_{SM} is the number of submodules per arm. Hence switching losses in this project can be assumed negligible. However, switching losses are calculated in Simulink/MATLAB environment as shown in Flow Chart 4.1. The figures mentioned in the Flow Chart 4.1 are shown in the following pages for a specific case. The procedure is explained as follows,

1. The arm current is multiplied with gate signal of SiC MOSFET to obtain the current profile through SiC MOSFET.
2. A MATLAB function (code) is implemented, that will give current magnitude corresponding to MOSFET turn-on and turn-off instants as output as shown in Figure 4.3 and Figure 4.6 respectively.
3. The value of turn-on/turn-off switching energy loss corresponding to the value of drain-source current magnitude and operating junction temperature is calculated (through the turn-on/turn-off switching energy loss versus operating junction temperature and the turn-on/turn-off switching energy loss versus drain-source current magnitude characteristic plots provided in MOSFET datasheet). These plots are shown in Figure 4.4 and Figure 4.7 respectively.

4. Total turn-on/turn-off switching energy losses during one cycle are obtained by the summation of all the values from Figure 4.4 and Figure 4.7 during one cycle as shown in Figure 4.5 and Figure 4.8 respectively.
5. Total turn-on/turn-off switching power losses are obtained by multiplying total turn-on/turn-off switching energy losses with fundamental frequency.
6. Total switching power losses are obtained by the summation of total turn-on and turn-off switching power losses as shown in Figure 4.9.

4.1.2 Conduction Power Losses

The conduction power losses are generated when the MOSFET is in on-state, due to the on-state resistance. An on-state resistance is the intrinsic resistance from drain-to-source of a MOSFET, represented as $R_{DS,ON}$. The value of on-state resistance is influenced by several factors such as operating junction temperature and drain-source current magnitude. The on-state resistance of a transistor increases with increase in operating junction temperature and increases with increase in drain-source current magnitude. The on-state resistance versus operating junction temperature and the on-state resistance versus drain-source current magnitude characteristics are generally provided in the datasheet of SiC MOSFET. The conduction power losses of MOSFET can be obtained by the following equation

$$P_{conduction} = I^2_{DS} * R_{DS.ON} \tag{4.1}$$

Where $P_{conduction}$ is conduction power loss, I_{DS} is drain-source current magnitude, $R_{DS.ON}$ is the on-state drain source resistance corresponding to the value of I_{DS} and operating junction temperature.

The SiC MOSFET conduction power loss calculation method in Simulink/MATLAB environment is as shown in the Flow Chart 4.2. The figures mentioned in the Flow Chart 4.2 are shown in the following pages for a specific case. The procedure is explained as follows,

1. The arm current is multiplied with gate signal of SiC MOSFET to obtain the current profile through SiC MOSFET.
2. The value of on-state drain to source resistance corresponding to the value of drain-source current magnitude and operating junction temperature is calculated (through the on-state resistance versus operating junction temperature and the on-state resistance versus drain-source current magnitude characteristic plots provided in MOSFET datasheet). This is shown in Figure 4.10.

3. A plot of conduction power loss versus time during one cycle is obtained by equation 4.1 as shown in Figure 4.11.
4. The area under the plot Figure 4.11 is obtained by integrating with respect to time, which gives total conduction energy loss during one cycle as shown in Figure 4.12.
5. The total conduction energy loss is multiplied by fundamental frequency to obtain total conduction power loss.

A very important point to be noted is that the SiC MOSFETs in the half-bridge sub module of MMC have antiparallel body diodes. However, the diode-less operation of the SiC MOSFETs is possible when the reverse (i.e. negative) current flows through the channel of the SiC MOSFET, since the on-state voltage drop of the channel is much lower than the one of the antiparallel body diodes. This means that the antiparallel body diodes only conduct for the time intervals of the blanking times, which are significantly shorter compared to the channel conduction intervals.

The on-state drain to source resistance must be minimized to reduce the conduction power loss of SiC MOSFET. This can be done by,

1. Reducing the current flow through SiC MOSFET through the parallel connection of semiconductor devices, which will result in increased number of devices and hence increased cost. Here a tradeoff may be found by calculating the cost of energy saved and cost of SiC MOSFET. At present SiC devices are expensive as the technology is in development stage, hence it can be said that the minimum possible number of devices may be used. But this may change as the technology and market matures resulting in rapid decrease of prices of SiC devices.
2. Reducing the operating junction temperature. Operating junction temperature can be reduced by lowering power losses. Power losses are minimized by reducing current flow through MOSFET, which goes back to point 1.
3. Increasing the doping in drift region. A major part of on-state drain to source resistance of SiC MOSFET is due to lower doping in the drift region. Hence the on-state resistance can be reduced by increase in drift region doping, that will increase the number of carriers in drift region resulting in reduced on-state resistance. However, this will reduce the device voltage blocking capability. Hence the SiC MOSFET is optimized to find a tradeoff between on-state resistance and voltage blocking capability. This is in the scope of manufacturer.

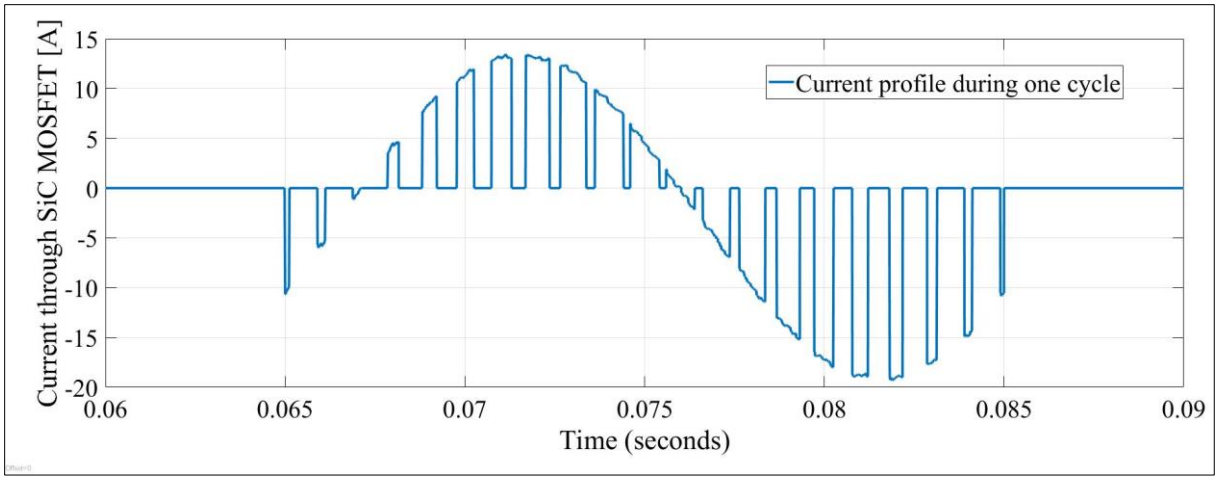


Figure 4.2 SiC MOFET current profile during one cycle

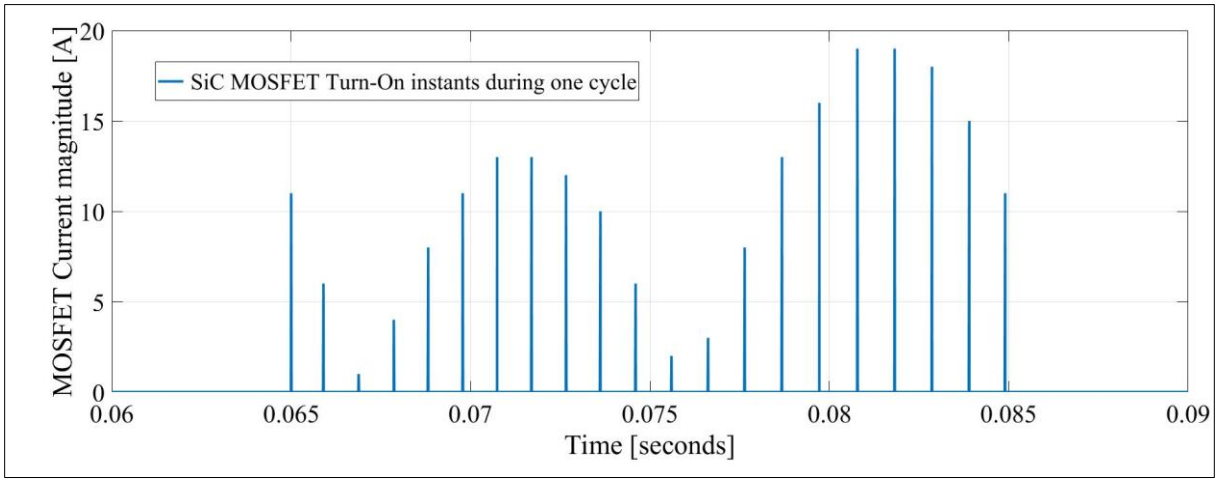


Figure 4.3 SiC MOSFET current magnitude for turn-on instants during one cycle

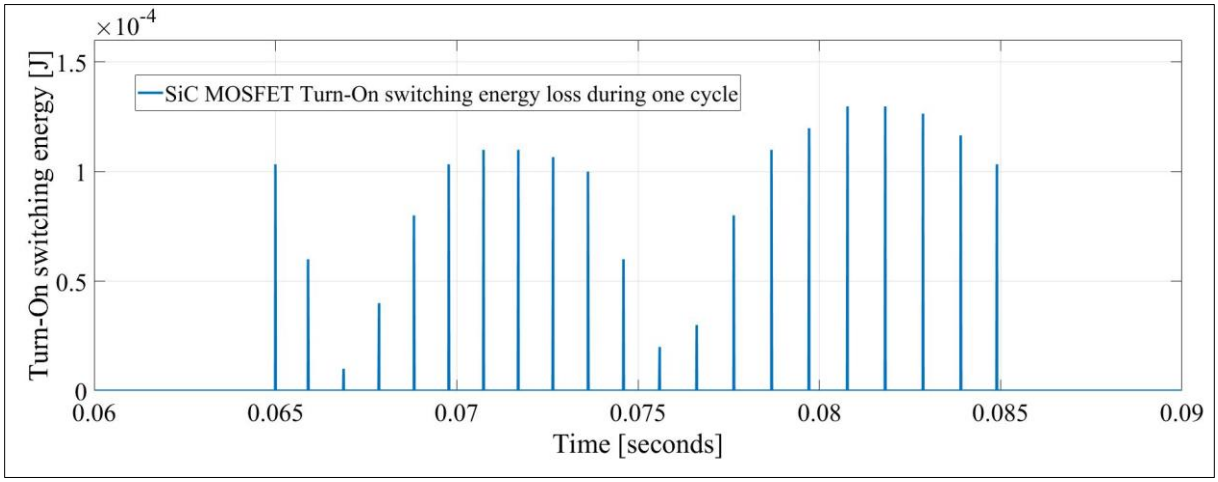


Figure 4.4 SiC MOSFET switching energy loss for turn-on instants during one cycle

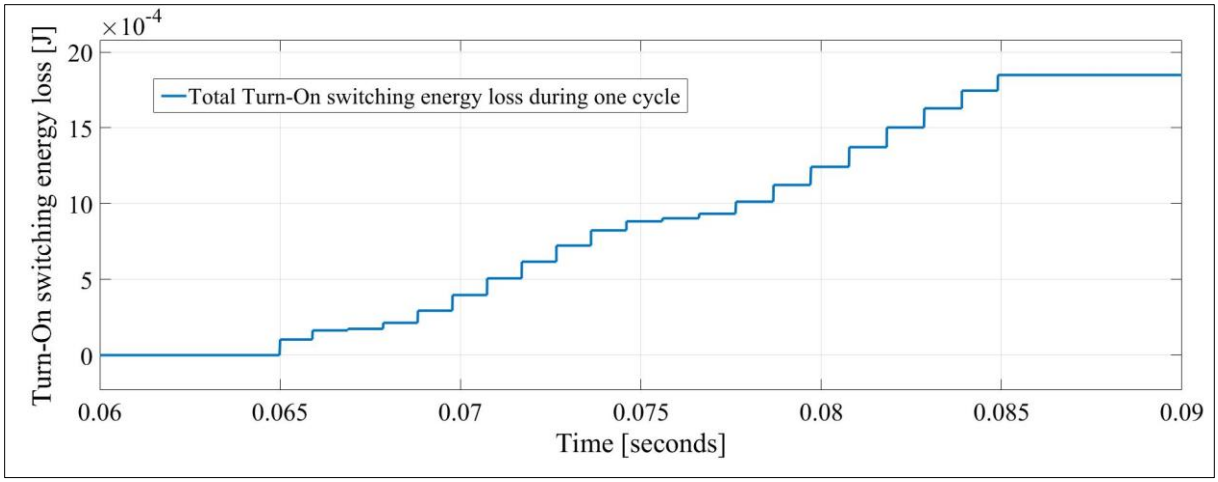


Figure 4.5 SiC MOSFET total turn-on switching energy loss during one cycle

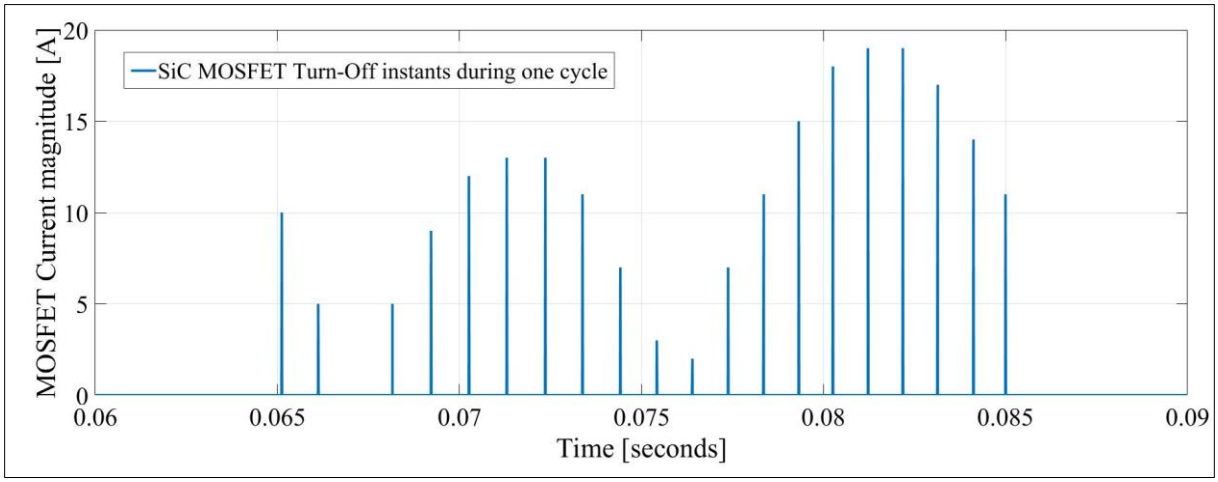


Figure 4.6 SiC MOSFET current magnitude for turn-off instants during one cycle

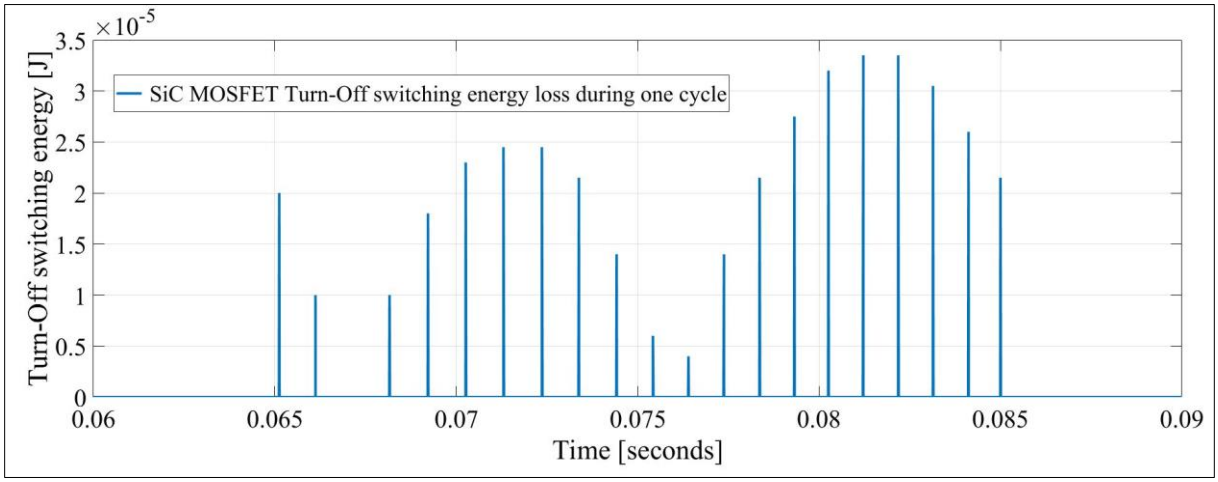


Figure 4.7 SiC MOSFET switching energy loss for turn-off instants during one cycle

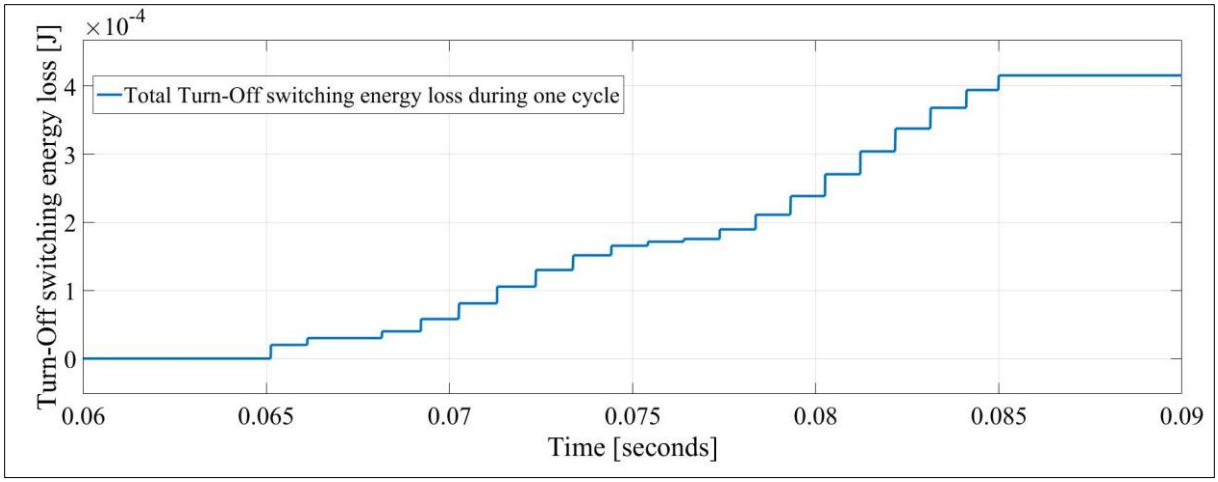


Figure 4.8 SiC MOSFET total turn-off switching energy loss during one cycle

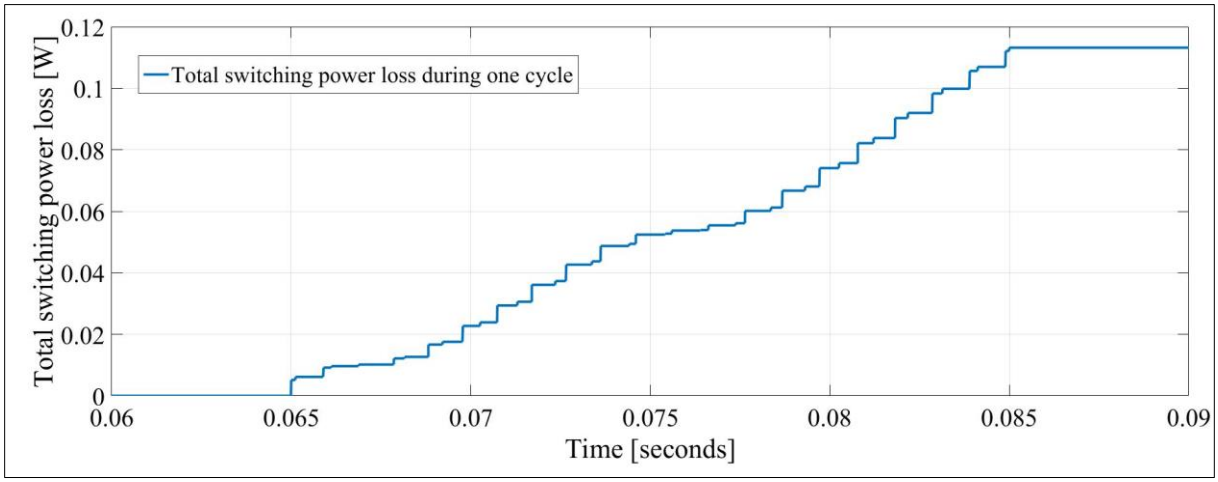


Figure 4.9 SiC MOSFET total switching power loss during one cycle

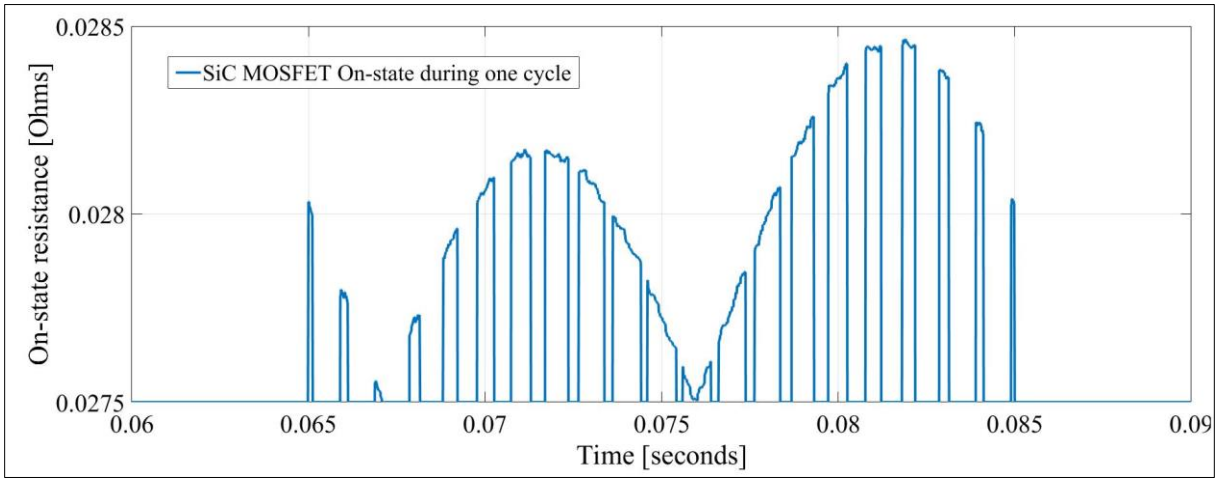


Figure 4.10 SiC MOSFET on-state resistance during one cycle

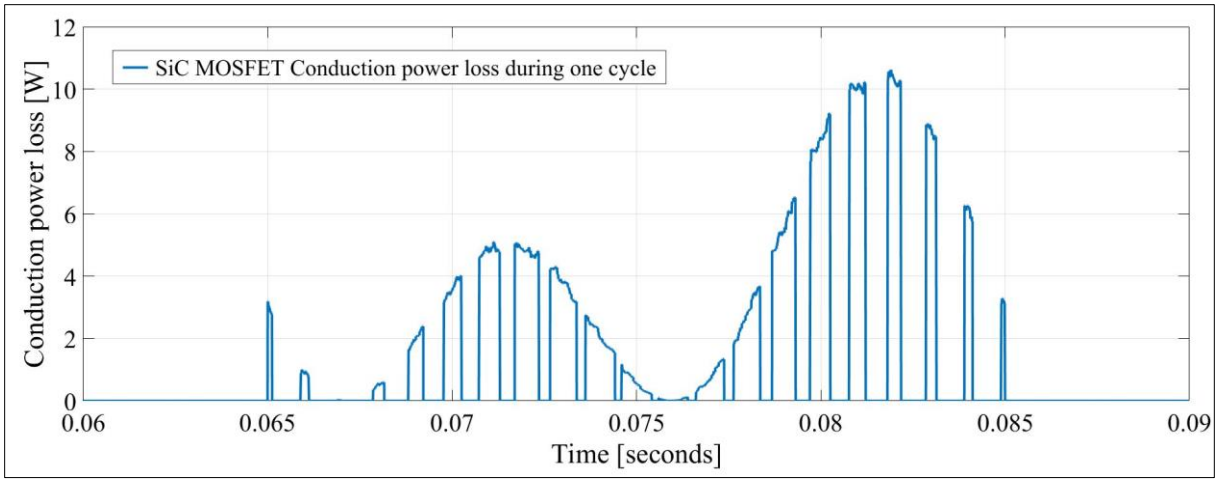


Figure 4.11 SiC MOSFET conduction power loss during one cycle

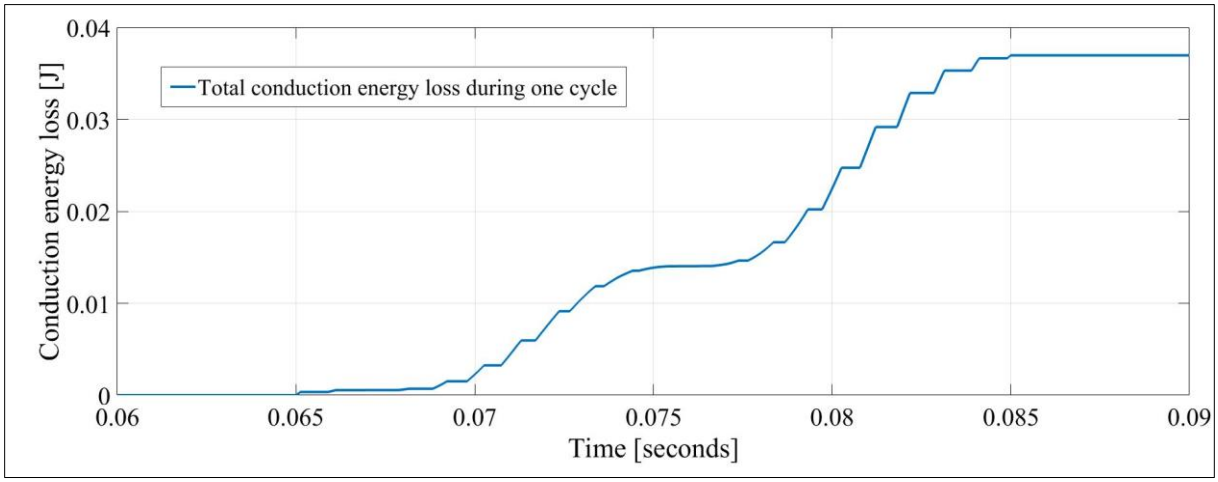


Figure 4.12 SiC MOSFET total conduction energy loss during one cycle

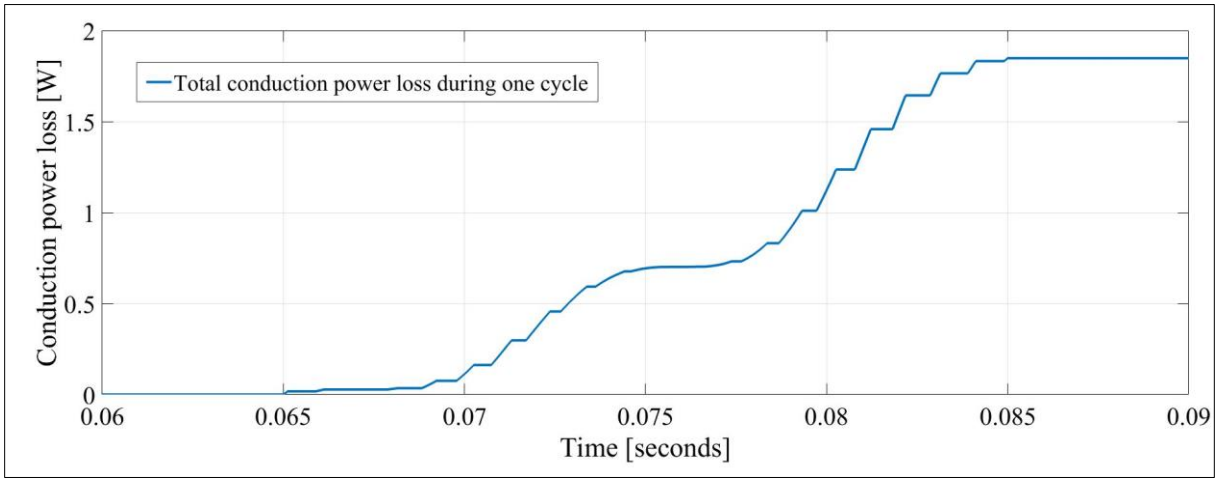


Figure 4.13 SiC MOSFET total conduction power loss during one cycle

4.2 Total Harmonic Distortion (THD)

Total harmonic distortion is measured for the AC side voltage in Simulink/MATLAB environment. The results are presented in the later chapters.

4.3 Operating junction temperature

The maximum current through SiC MOSFET is calculated assuming the maximum operating junction temperature of $125^0 C$. The value of power that can be dissipated from junction to case is,

$$P_{thermal} = \frac{T_j - T_c}{R_{th}} \tag{4.2}$$

Where $P_{thermal}$ is thermal power (power loss, that can be dissipated through heatsink without the junction temperature exceeding a value of 125°C), T_j is operating junction temperature, T_c is operating case temperature, R_{th} is thermal resistance from junction to heatsink. Where $R_{th} = R_{th-jc} + R_{th-chs}$. R_{th-jc} is thermal resistance from junction to case, this value can be read from datasheet of SiC MOSFET. R_{th-chs} is thermal resistance from case to heatsink, this value can be found for the type of SiC MOSFET package. The package for the three SiC MOSFETs used for this project is TO-247-3, whose thermal resistance from case to heatsink is approximately 0.24 ^{O}C/W.

The power loss in SiC MOSFET is calculated as,

$$P_{loss} = I^2 R_{DSon} \tag{4.3}$$

For the maximum operating junction temperature of 125°C,

$$P_{loss} = I^2 R_{DSon} = P_{thermal} = \frac{T_j - T_c}{R_{th}} \tag{4.4}$$

$$\mathrm{I}_{max} = \sqrt{\frac{\frac{T_j - T_c}{R_{th}}}{R_{DSon}}} \tag{4.5}$$

In the equation 4.5, variables $R_{DSon}, T_j, T_c, R_{th}$ are known. Thus, the maximum current through SiC MOSFET can be calculated. Based on this value, the minimum number of SiC MOSFETs required to be connected in parallel are calculated as,

$$N_P = \frac{\mathrm{I}_{arm}}{\mathrm{I}_{max}} \tag{4.6}$$

Where, N_P is the number of parallel connected semiconductor devices. Therefore, the maximum current through SiC MOSFET and power losses are thermally limited. The semiconductor losses measured for the Simulink/MATLAB model of MMC by varying the number parallel connected SiC MOSFETs are presented in the later Sections.

Chapter 5. Simulations and Results

To verify the optimization criteria proposed in the previous chapter, three SiC MOSFET made by Wolf speed (a Cree company) are chosen. The specifications of three SiC MOSFETs are presented in the Table 5.1. The detailed datasheets can be downloaded from the Wolf speed website using the model number of SiC MOSFET.

Table 5.1 Specifications of SiC MOSFETs

Model Number	SiC MOSFET voltage rating (V)	Usable voltage rating (50%-60%)	N_{SM} (number of sub modules per arm)
C3M0030090K	900	450	20
C2M0025120D	1200	600	15
C2M0045170D	1700	1000	9

To confirm the influence of number of submodules, number of parallel connected semiconductor devices on semiconductor losses and total harmonic distortion in the given system, the following two sets of simulations are carried for three different SiC MOSFETs using the Simulink/MATLAB model developed,

1. Number of sub modules per arm in MMC indicates the voltage drop across each semiconductor device, which is a SiC MOSFET in this project. The minimum number of sub modules is calculated for each MOSFET and the number of sub modules is increased up to 10 levels, one level at a time. The semiconductor losses and total harmonic distortion are measured in Simulink/MATLAB environment as described in the previous chapters.
2. Number of parallel connected semiconductor devices in MMC indicates the current flow through each semiconductor device, which is a SiC MOSFET in this project. The minimum number of parallel connected devices is determined for each MOSFET considering the operating junction temperature of 125 degree Celsius. The minimum number of parallel connected devices is increased up to 10 levels, one level at a time. The semiconductor losses and total harmonic distortion are measured in Simulink/MATLAB environment as described in the previous chapters.

The results are presented for each MOSFET in the following sections.

5.1 900 [V] SiC MOSFET (C3M0030090K)

The minimum number of sub modules for a 900 V SiC MOSFET in the given system is 20. The minimum number of parallel connected SiC MOSFETs is 16. These values are increased to measure the influence of them on the semiconductor losses in the MMC and total harmonic distortion.

5.1.1 Variation of N_{SM}

In this Section, the number of sub modules is increased from 20 to 30, one at a time. The losses measured at the operating junction temperatures of 25°C, 125°C and total harmonic distortion (THD) are presented in the Table 5.2.

Table 5.2 Losses in MMC with variation of N_{SM}

S.No	SiC MOSFET rating [V]	Maximum usable rating [V]	N_{SM}	V_{SM} [V]	T=25°C			T=125°C	THD [%]
					Conduction losses [kW]	Switching losses [kW]	Total losses [kW]	Conduction losses [kW]	
1	900	450	20	450	18.76	0.566	19.326	24.54	3.5
2	900	450	21	428.57	19.77	0.598	20.368	25.86	3.1
3	900	450	22	409.09	20.61	0.624	21.234	26.97	2.7
4	900	450	23	391.30	21.47	0.654	22.124	28.1	2.6
5	900	450	24	375	22.11	0.675	22.785	28.93	2.35
6	900	450	25	360	22.75	0.702	23.452	29.76	2.3
7	900	450	26	346.15	23.84	0.735	24.575	31.19	2.25
8	900	450	27	333.33	24.81	0.765	25.575	32.46	2.15
9	900	450	28	321.42	25.64	0.79	26.43	33.54	2.1
10	900	450	29	310.34	26.37	0.816	27.186	34.5	1.8
11	900	450	30	300	27.13	0.839	27.969	35.5	1.43

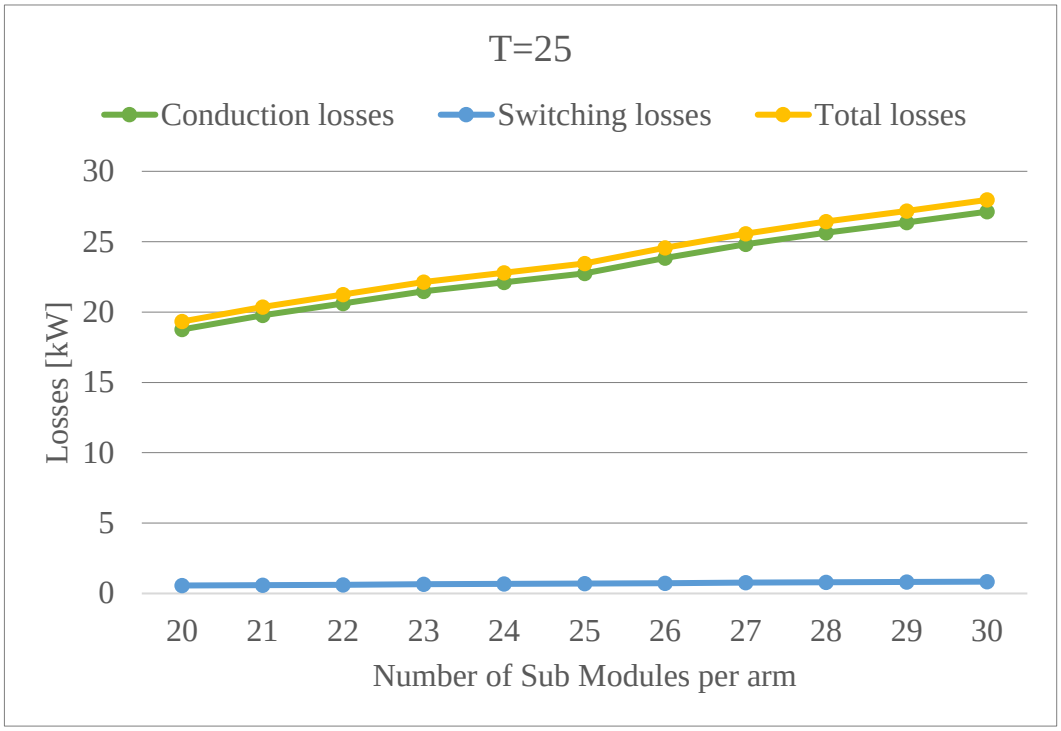


Figure 5.1 Losses at the temperature of 25°C

Figure 5.2 Conduction losses Versus N_{SM}

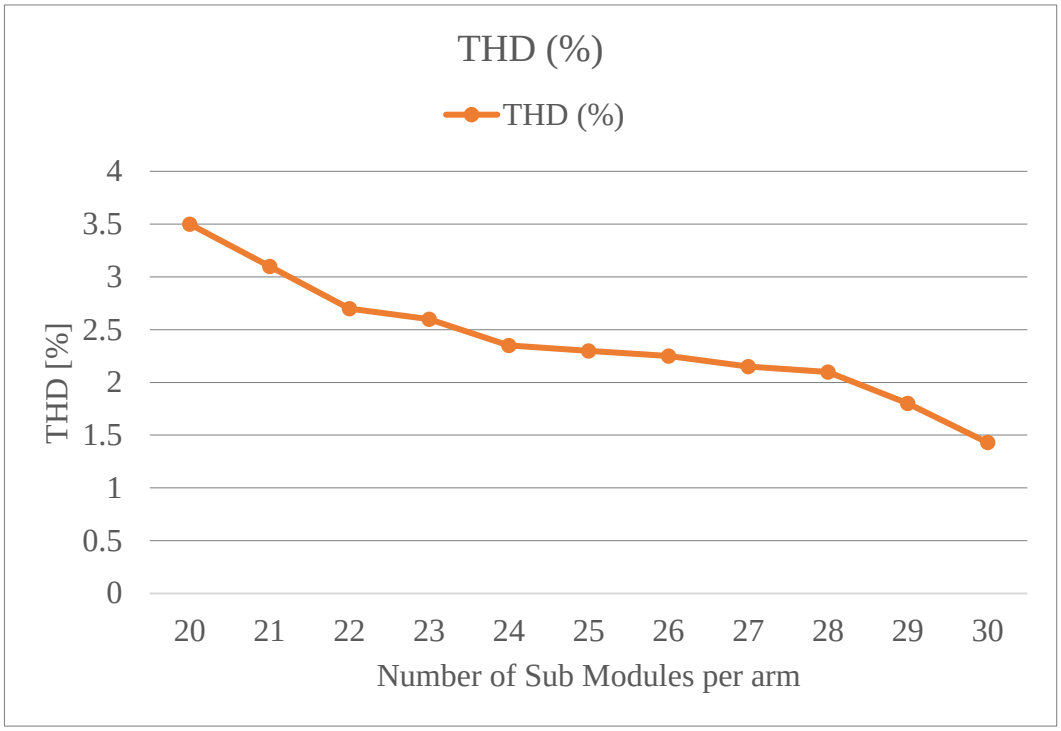


Figure 5.3 Total Harmonic Distortion (THD) Versus N_{SM}

The following points can be observed from the above results and plots,

1. The voltage capacity utilization of SiC MOSFET is decreasing with the increase in number of sub modules. This is a disadvantage as the SiC devices are expensive in the current market.
2. The switching losses can be assumed negligible compared to the conduction losses as shown in the Figure 5.1. This allows further increase of switching frequency, that will improve the waveform with respect to harmonics.
3. The losses (conduction and switching) usually increases with increase in the number of sub modules. This is due to the fact that predominant conduction losses depend upon the current through MOSFET and on-state drain to source resistance. Current through MOSFETs remains constant despite the increase in the number of sub modules. However, the number of MOSFETs increase with the increase in number of sub modules. Hence the losses increase with the increase in the number of sub modules.
4. The conduction losses at the operating junction temperature 125°C are significantly higher than compared to the operating junction temperature of 25°C. This is due to the fact that the on-state drain to source resistance of the SiC MOSFET increases with increase in temperature as shown in the datasheet of 900 V SiC MOSFET.

5. Total Harmonic Distortion (THD) decreases with the increase in the number of sub modules per arm in MMC. This is an advantage as the grid regulations are getting stricter with massive penetration of power electronics in electric power system from generation to transmission to consumer level.

5.1.2 Variation of N_P

In this Section, the number of parallel connected SiC MOSFETs (N_P) is increased from 16 to 25, one at a time. The losses measured at the operating junction temperatures of 25°C, 125°C are presented in the Table 5.3.

Table 5.3 Losses in MMC with variation of N_P

S.No	SiC MOSFET rating [V]	Maximum usable rating [V]	N_P	N_{SM}	V_{SM} [V]	T=25°C			T=125°C
						Conduction losses [kW]	Switching losses [kW]	Total losses [kW]	Conduction losses [kW]
1	900	450	16	20	450	18.76	0.566	19.326	24.54
2	900	450	17	20	450	17.63	0.578	18.208	23.07
3	900	450	18	20	450	16.63	0.588	17.218	21.67
4	900	450	19	20	450	15.73	0.598	16.328	20.6
5	900	450	20	20	450	14.93	0.608	15.538	19.55
6	900	450	21	20	450	14.2	0.62	14.82	18.61
7	900	450	22	20	450	13.54	0.628	14.168	17.75
8	900	450	23	20	450	12.94	0.642	13.582	16.97
9	900	450	24	20	450	12.39	0.645	13.035	16.26
10	900	450	25	20	450	11.88	0.66	12.54	15.6

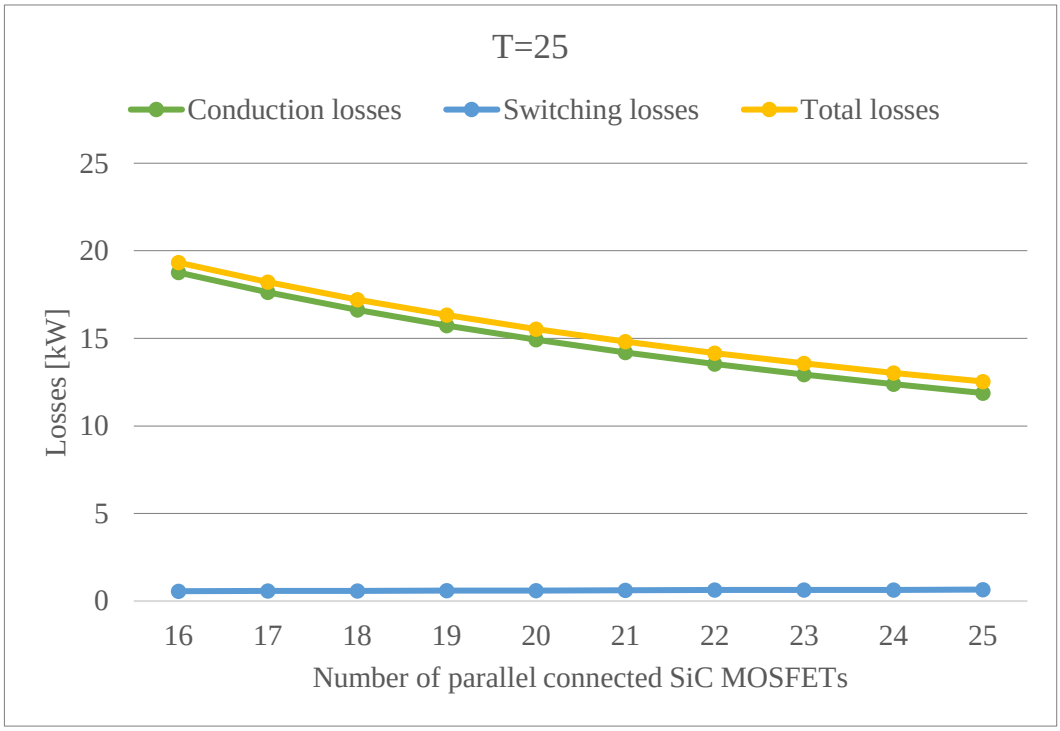


Figure 5.4 Losses at the temperature of 25°C

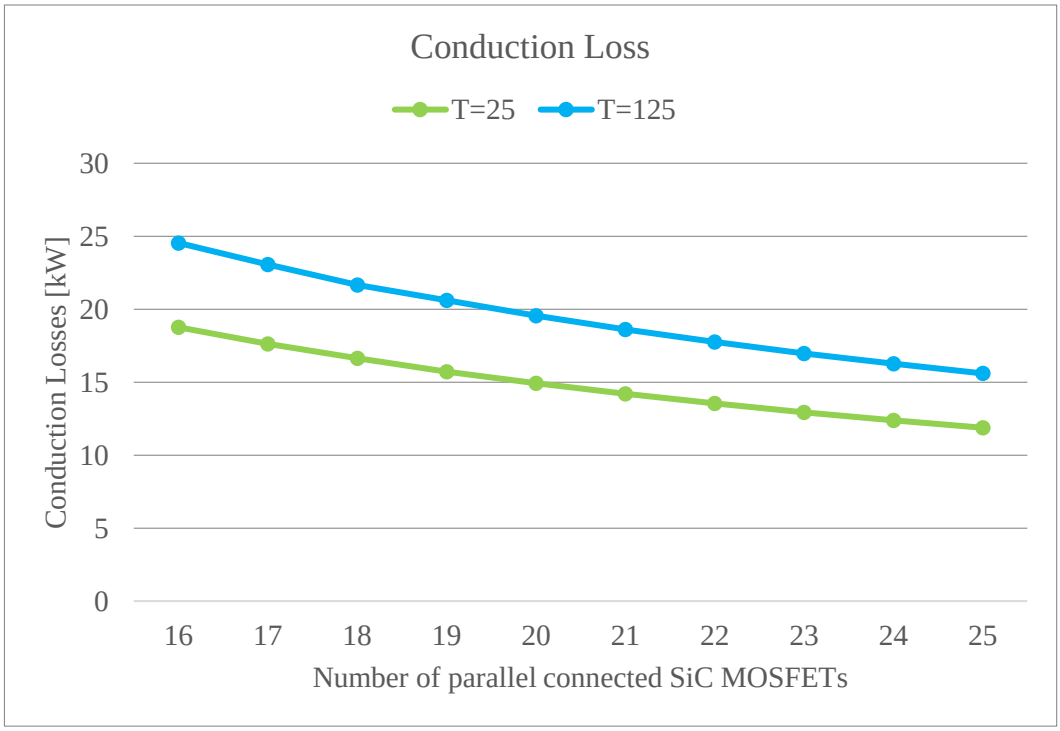


Figure 5.5 Conduction losses Versus N_P

The following points can be observed from the above results and plots,

1. The voltage capacity utilization of SiC MOSFET remains same with the increase in the number of parallel connected SiC MOSFETs. However, the current flowing through SiC MOSFET decreases with the increase in the number of parallel connected SiC MOSFETs.
2. The switching losses can be assumed negligible compared to the conduction losses as shown in the Figure 5.4. This allows further increase of switching frequency, that will improve the waveform with respect to harmonics.
3. The conduction losses decrease with increase in the number of parallel connected SiC MOSFETs, despite the increase in number of SiC MOSFETs in the given system. This is due to the fact that current through individual MOSFET decreases resulting in the decrease of the value of on-state drain to source resistance at a given temperature. However, the switching losses increase with increase in the number of parallel connected SiC MOSFETs, due to the increase in the number of SiC MOSFETs in the given system.
4. Moreover, the conduction losses at the operating junction temperature of $125^{O}C$ are significantly higher than compared to the operating junction temperature of $25^{O}C$. This is due to the fact that the on-state drain to source resistance of the SiC MOSFET increases with increase in temperature as shown in the datasheet of 900 V SiC MOSFET.
5. Total Harmonic Distortion (THD) remains same with the increase in the number of parallel connected SiC MOSFETs. This due to the fact that voltage levels remain same and hence voltage waveform remains unchanged.

5.2 1200 [V] SiC MOSFET (C2M0025120D)

The minimum number of sub modules for a 1200 V SiC MOSFET in the given system is 15. The minimum number of parallel connected SiC MOSFETs is 13. These values are increased to measure the influence of them on semiconductor losses in the MMC and total harmonic distortion.

5.2.1 Variation of N_{SM}

In this section, the number of sub modules is increased from 15 to 25, one at a time. The losses measured at the operating junction temperatures of 25°C, 125°C and total harmonic distortion (THD) are presented in the Table 5.4.

Table 5.4 Losses in MMC with variation of N_{SM}

S.No	SiC MOSFET rating [V]	Maximum usable rating [V]	N_{SM}	V_{SM} [V]	T=25°C			T=125 ^{O}C	THD [%]
					Conduction losses [kW]	Switching losses [kW]	Total losses [kW]	Conduction losses [kW]	
1	1200	600	15	600	15.29	1.137	16.427	27.04	6.2
2	1200	600	16	562.5	16.26	1.205	17.465	28.75	5.2
3	1200	600	17	529.41	17.16	1.262	18.422	30.34	4.9
4	1200	600	18	500	18.15	1.335	19.485	32.1	4.4
5	1200	600	19	473.68	19.09	1.408	20.498	33.76	4.15
6	1200	600	20	450	20.12	1.48	21.6	35.59	3.8
7	1200	600	21	428.57	20.9	1.546	22.446	36.95	3.6
8	1200	600	22	409.09	21.94	1.619	23.559	38.78	3.4
9	1200	600	23	391.30	22.86	1.684	24.544	40.41	3.1
10	1200	600	24	375	23.84	1.769	25.609	42.14	2.9
11	1200	600	25	360	24.7	1.848	26.548	43.66	2.7

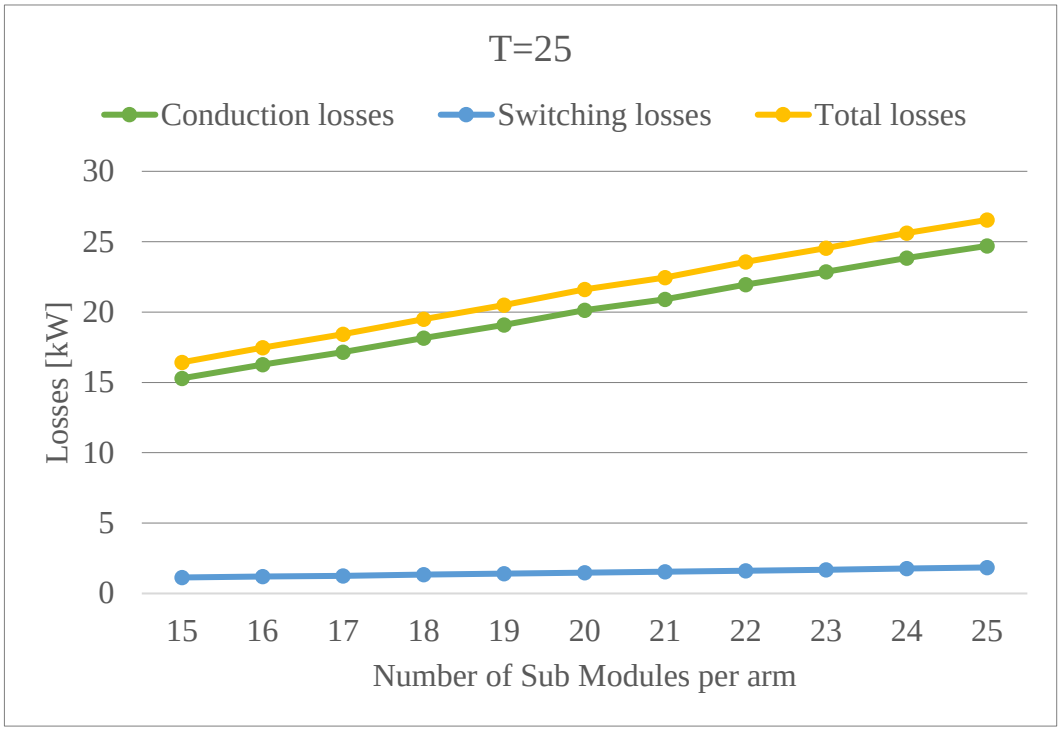


Figure 5.6 Losses at the temperature of 25°C

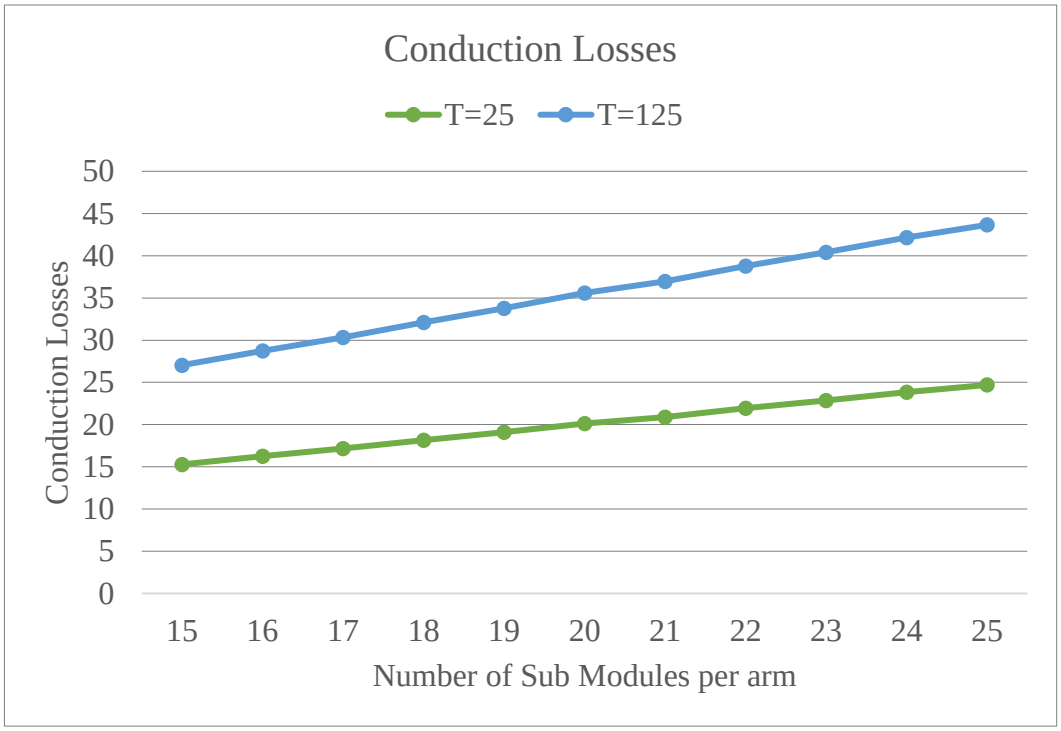


Figure 5.7 Conduction losses Versus N_{SM}

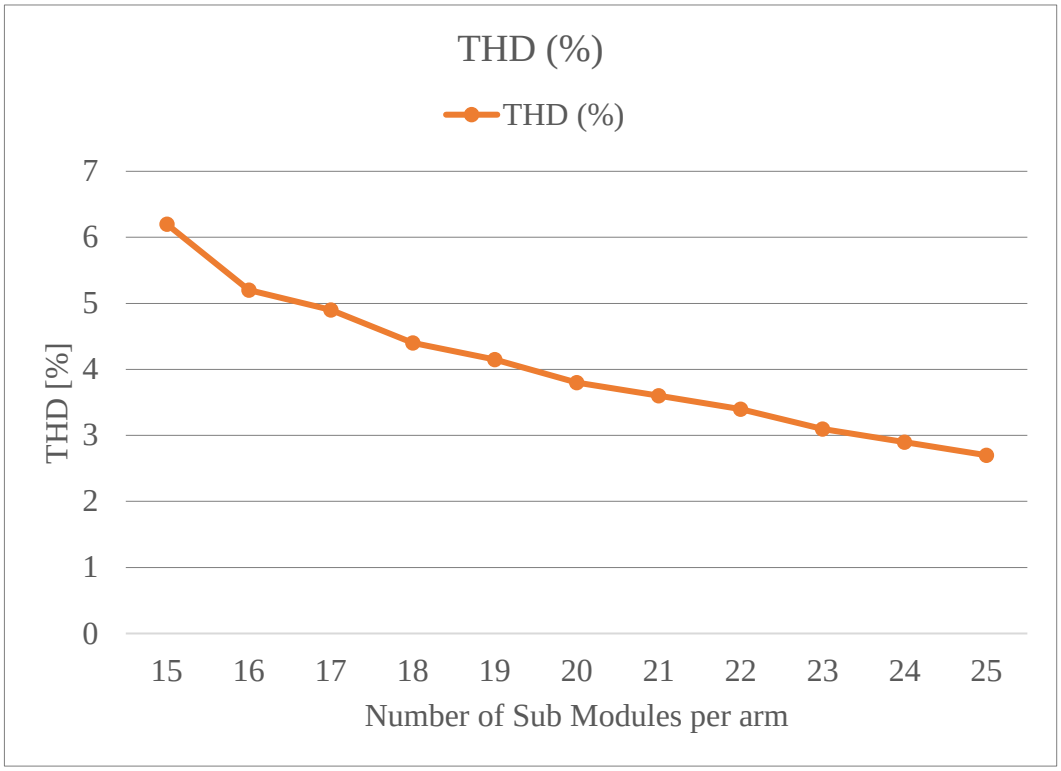


Figure 5.8 Total Harmonic Distortion (THD) Versus N_{SM}

The observations are similar to that of 900 V SiC MOSFET.

5.2.2 Variation of N_P

In this Section, the number of parallel connected SiC MOSFETs (N_P) is increased from 13 to 20, one at a time. The losses measured at the operating junction temperatures of 25°C, 125°C are presented in the Table 5.5.

Table 5.5 Losses in MMC with variation of N_P

S.No	SiC MOSFET rating [V]	Maximum usable rating [V]	N_P	N_{SM}	V_{SM} [V]	T=25 ^{O}C			T=125 ^{O}C
						Conduction losses [kW]	Switching losses [kW]	Total losses [kW]	Conduction losses [kW]
1	1200	600	13	15	600	15.29	1.137	16.427	27.04
2	1200	600	14	15	600	14.15	1.089	15.239	24.95
3	1200	600	15	15	600	13.16	1.055	14.215	23.16
4	1200	600	16	15	600	12.31	1.026	13.336	21.62
5	1200	600	17	15	600	11.55	0.994	12.544	20.28
6	1200	600	18	15	600	10.88	0.973	11.853	19.1
7	1200	600	19	15	600	10.29	0.958	11.248	18.05
8	1200	600	20	15	600	9.752	0.943	10.695	17.11

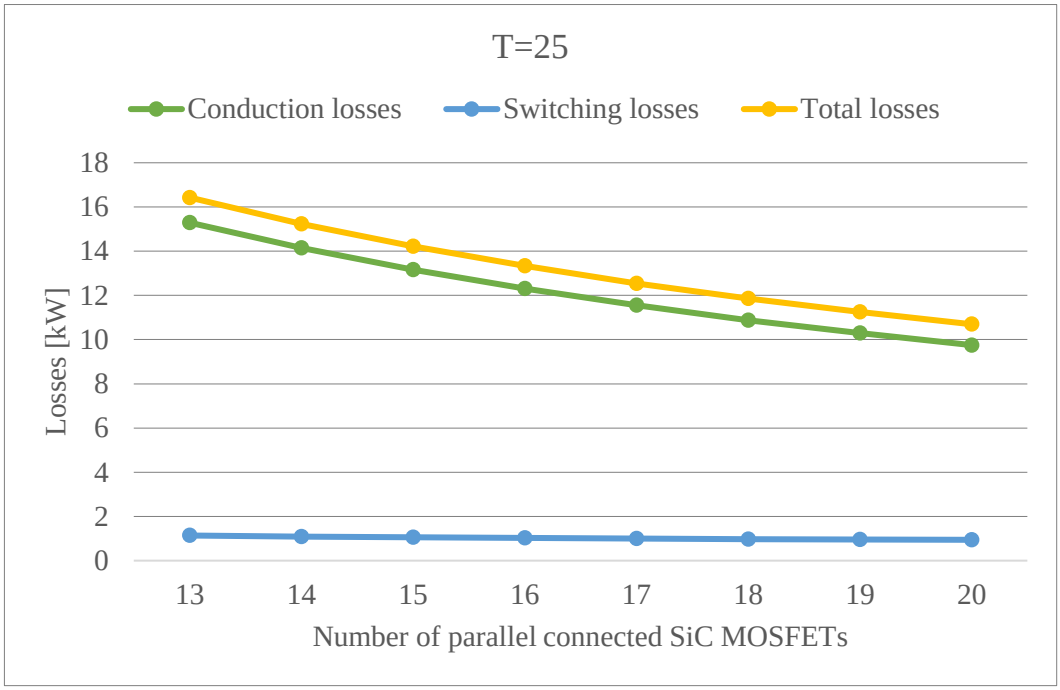


Figure 5.9 Losses at the temperature of 25°C

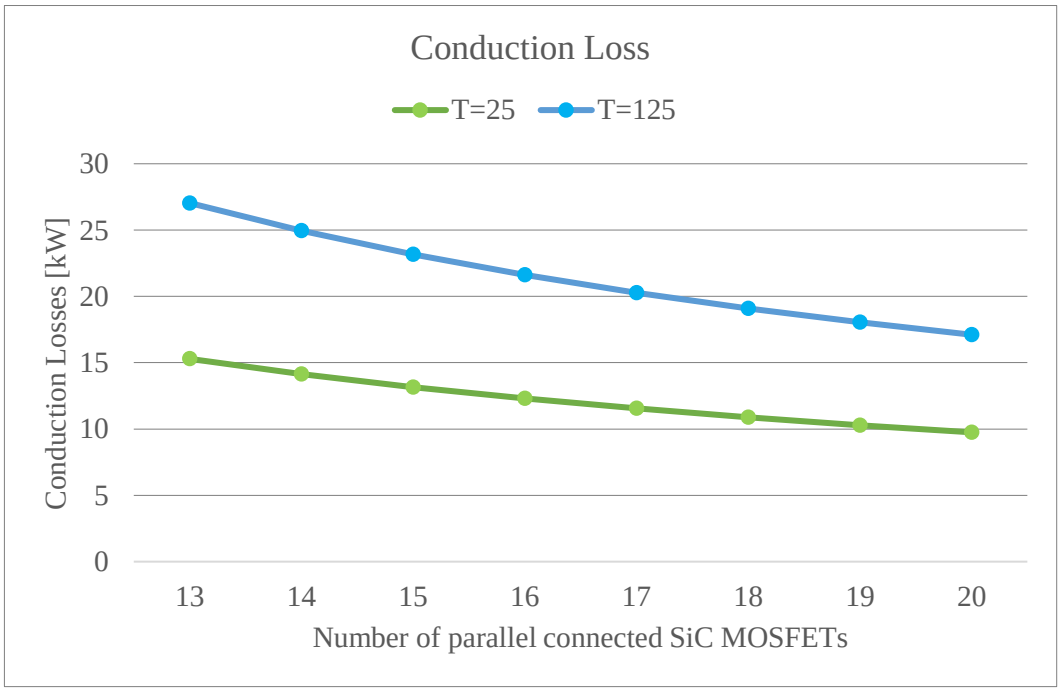


Figure 5.10 Conduction losses Versus N_P

The observations are similar to that of 900 V SiC MOSFET.

5.3 1700 [V] SiC MOSFET (C3M0030090K)

The minimum number of sub modules for a 1700 V SiC MOSFET in the given system is 9. The minimum number of parallel connected SiC MOSFETs is 16. These values are increased to measure the influence of them on the semiconductor losses in the MMC and total harmonic distortion.

5.3.1 Variation of N_{SM}

In this Section, the number of sub modules is increased from 9 to 20, one at a time. The losses measured at the operating junction temperatures of 25°C, 125°C and total harmonic distortion (THD) are presented in the Table 5.6.

Table 5.6 Losses in MMC with variation of N_{SM}

S.No	SiC MOSFET rating [V]	Maximum usable rating [V]	N_{SM}	V_{SM} [V]	T=25 ^{O}C			T=125 ^{O}C	THD [%]
					Conduction losses [kW]	Switching losses [kW]	Total losses [kW]	Conduction losses [kW]	
1	1700	1000	9	1000	12.07	1.297	13.367	24.94	8.2
2	1700	1000	10	900	13.36	1.436	14.796	27.6	7.8
3	1700	1000	11	818.18	14.57	1.57	16.14	30.11	7.34
4	1700	1000	12	750	15.86	1.719	17.579	32.77	7
5	1700	1000	13	692.30	17.11	1.868	18.978	35.35	6.9
6	1700	1000	14	642.85	18.27	1.997	20.267	37.77	6.4
7	1700	1000	15	600	19.41	2.128	21.538	40.11	6.15
8	1700	1000	16	562.5	20.7	2.27	22.97	42.78	5.48
9	1700	1000	17	529.41	21.95	2.413	24.363	45.37	4.74
10	1700	1000	18	500	22.98	2.533	25.513	47.51	4.27
11	1700	1000	19	473.68	24.06	2.673	26.733	49.74	3.36
12	1700	1000	20	450	25.36	2.815	28.175	52.44	3.33

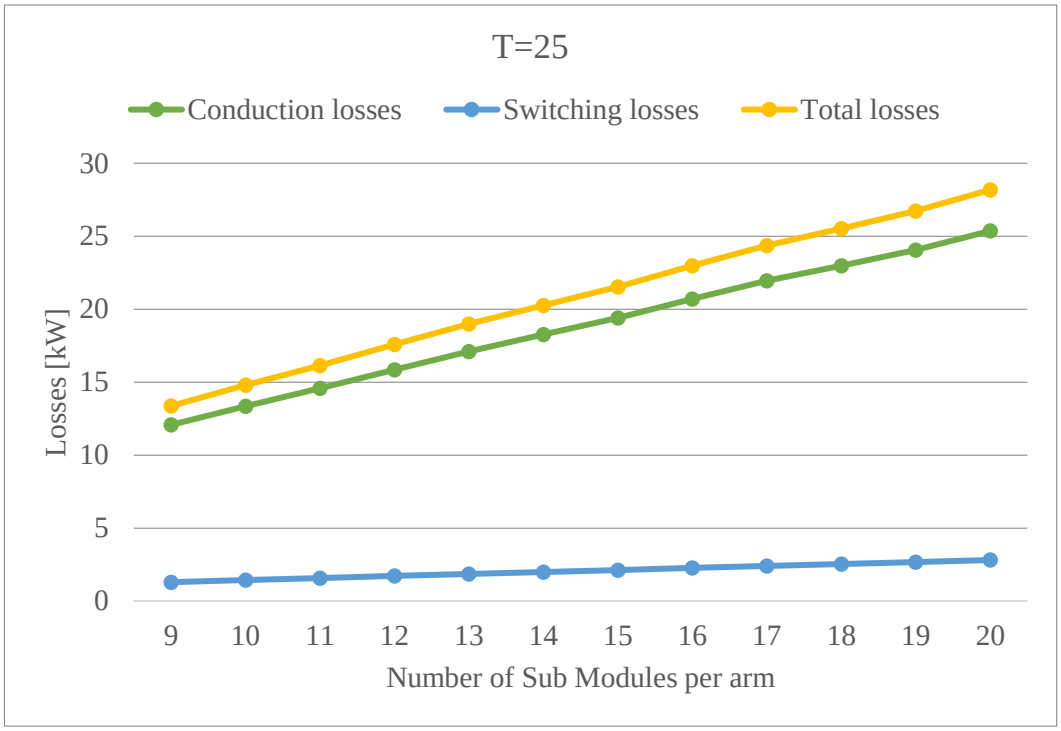


Figure 5.11 Losses at the temperature of 25°C

Figure 5.12 Conduction losses Versus N_{SM}

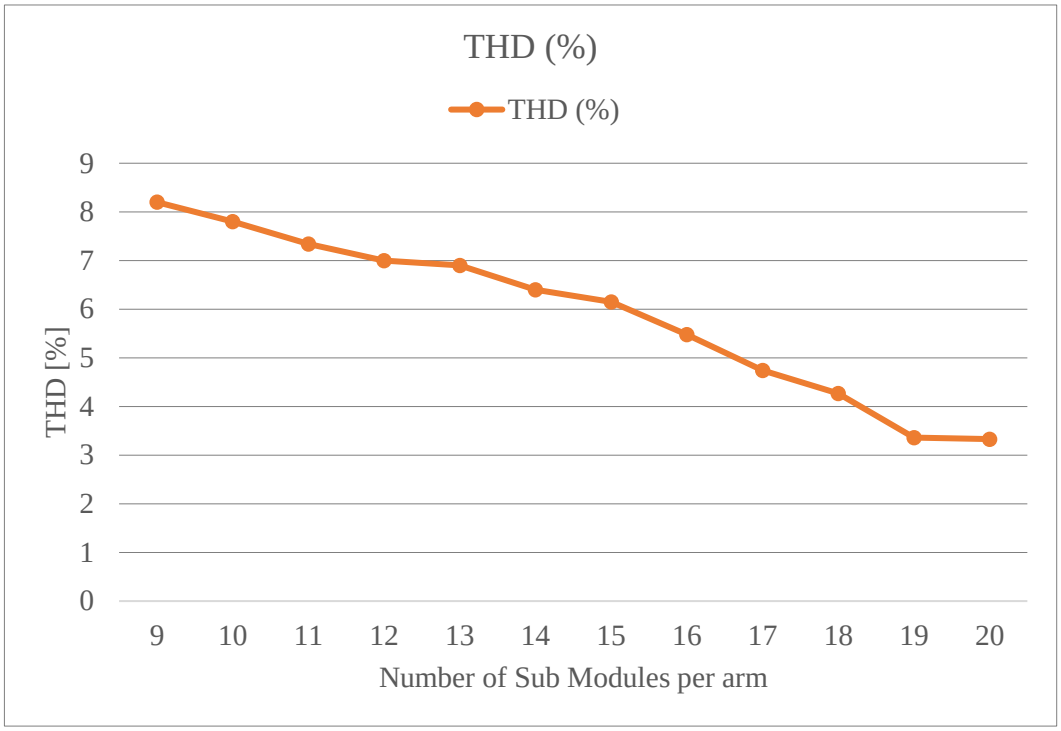


Figure 5.13 Total Harmonic Distortion (THD) Versus N_{SM}

The observations are similar to that of 900 V SiC MOSFET.

5.3.2 Variation of N_P

In this Section, the number of parallel connected SiC MOSFETs (N_P) is increased from 16 to 25, one at a time. The losses measured at the operating junction temperatures of 25°C, 125°C are presented in the Table 5.7.

Table 5.7 Losses in MMC with variation of N_P

S.No	SiC MOSFET rating [V]	Maximum usable rating [V]	N_P	N_{SM}	V_{SM} [V]	T=25 ^{O}C			T=125 ^{O}C
						Conduction losses [kW]	Switching losses [kW]	Total losses [kW]	Conduction losses [kW]
1	1700	1000	16	9	1000	12.07	1.297	13.367	24.94
2	1700	1000	17	9	1000	11.29	1.318	12.608	23.37
3	1700	1000	18	9	1000	10.61	1.333	11.943	21.99
4	1700	1000	19	9	1000	10	1.344	11.344	20.77
5	1700	1000	20	9	1000	9.462	1.363	10.825	19.67
6	1700	1000	21	9	1000	8.977	1.371	10.348	18.68
7	1700	1000	22	9	1000	8.538	1.386	9.924	17.79
8	1700	1000	23	9	1000	8.14	1.4	9.54	16.98
9	1700	1000	24	9	1000	7.78	1.413	9.193	16.24
10	1700	1000	25	9	1000	7.446	1.436	8.882	15.56

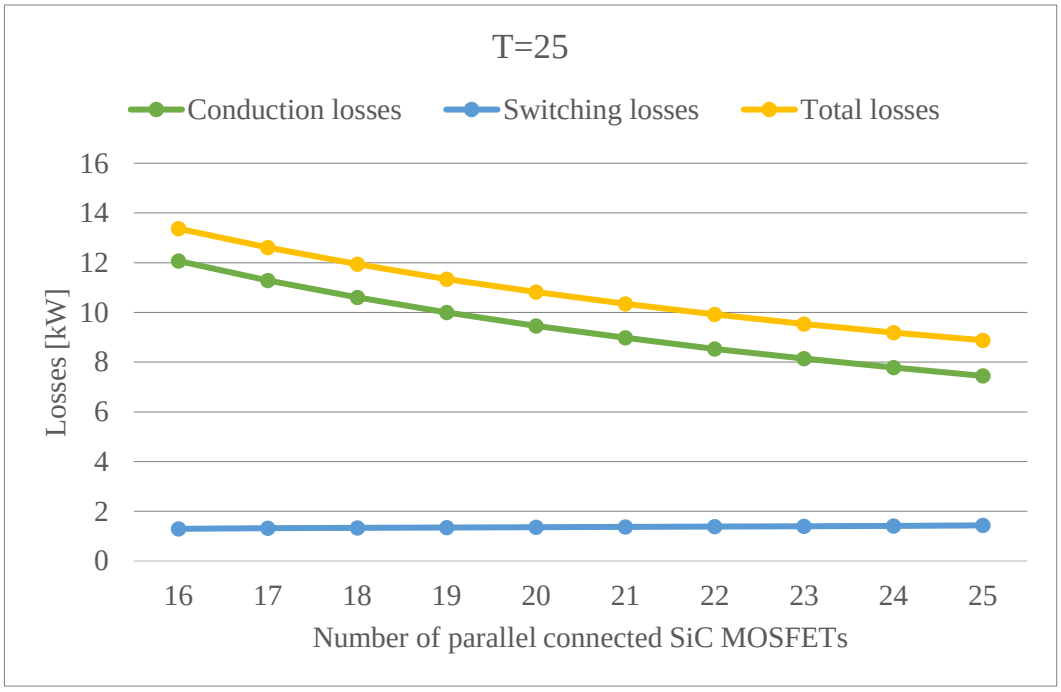


Figure 5.14 Losses at the temperature of 25°C

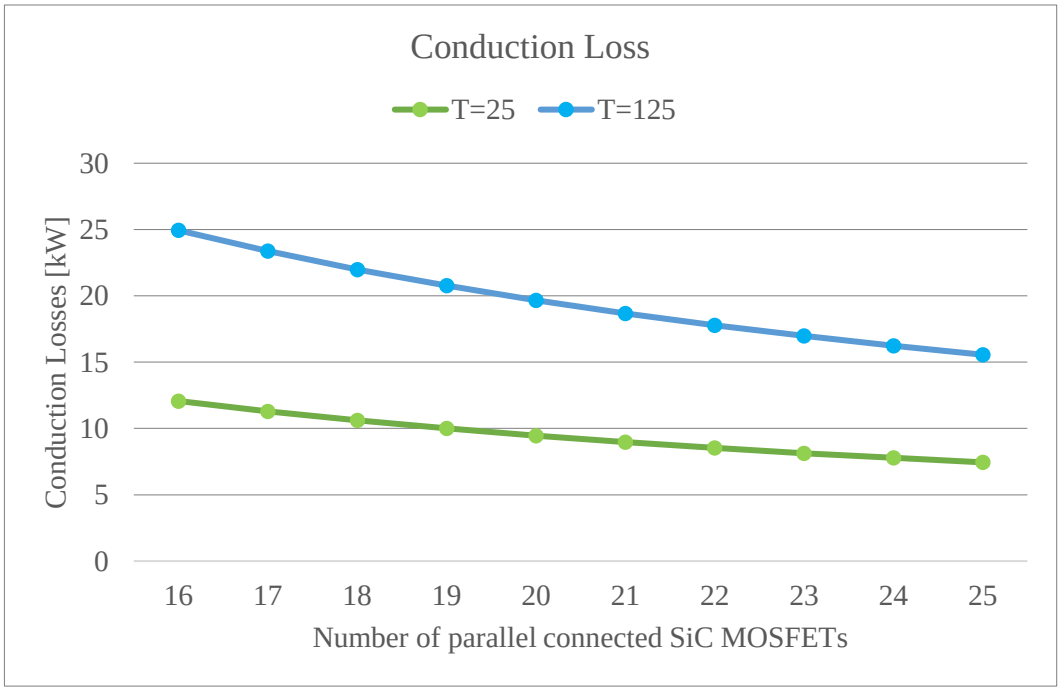


Figure 5.15 Conduction losses Versus N_P

The observations are similar to that of 900 V SiC MOSFET.

5.4 A Comparison of different SiC MOSFETs

A comparison of three SiC MOSFETs is shown in Table 5.8. Comparing losses of three different SiC MOSFETs with the minimum number of sub modules and minimum number of parallel connected SiC MOSFETs in the given system may not be appropriate, as the number of devices in the given system are different for different SiC MOSFs. However, comparison with equal N_{SM}, N_P is pursued, whereas this would reflect device characteristics provided in the datasheets of SiC MOSFETs. Comparison of different SiC MOSFETs may not be necessary, as the optimization of devices and device characteristics is within the scope of manufacturer.

Table 5.8 A comparison of three SiC MOSFETs

S.No	SiC MOSFET rating [V]	Usable rating [V]	N_P	N_{SM}	V_{SM} [V]	T=25 °C		T=125 °C
						Conduction losses [kW]	Switching losses [kW]	Conduction losses [kW]
1	900	450	20	20	450	14.93	0.608	19.55
2	1200	600	20	20	450	12.84	1.24	22.52
3	1700	1000	20	20	450	19.89	2.94	41.39

From Table 5.8, it can be observed that the losses pattern reflects the device characteristics from datasheets of SiC MOSFETs as shown in Figure 5.16. This is due to the fact that the voltage and current through all three SiC MOSFETs in the Simulink/MATLAB MMC model are same, since N_{SM} and N_P are same respectively. However, the capacity utilization is different.

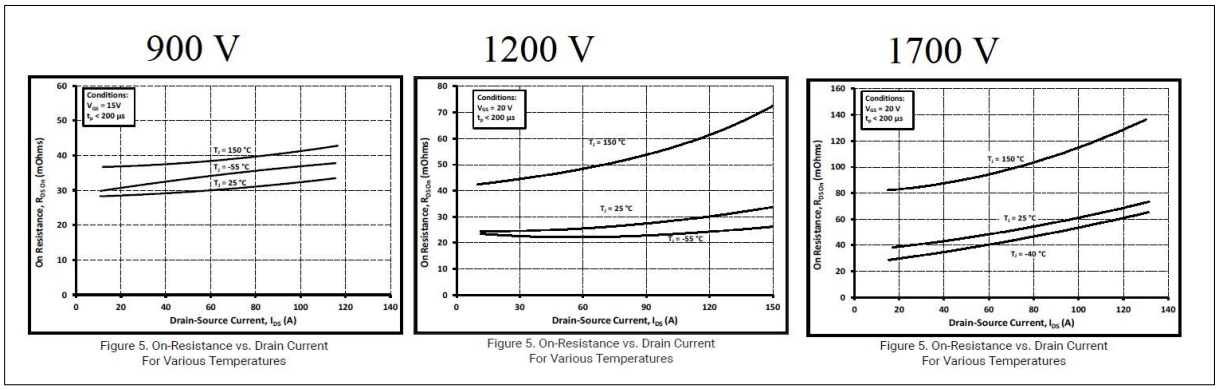


Figure 5.16 Device characteristics of different MOSFETs

Generally, it is recommended to use the SiC MOSFET with lowest rating for MMC, since this will result in maximum number of voltage levels, which implies minimum total harmonic distortion and minimum filter requirements. However, this has to be concluded by extending the Simulink/MATLAB model to complete wind energy conversion and running the required simulations.

Chapter 6. Discussion, Conclusion, Future work

6.1 Wind Energy Conversion System

The wind turbine capacity is increasing beyond 10 MW, with General Electric announcing 12 MW wind turbine. At such higher power levels, medium voltage wind energy conversion system with full scale power electronic converter is emerging as a promising choice. Medium voltage will reduce the conduction losses in all electric equipment including generator, cables, power semiconductor devices of power electronic converter, while increasing the insulation requirement. The modular multilevel converter is promising for medium voltage, high power levels due to its advantages compared to other multilevel topologies. However, it is complex to implement compared to two level topologies.

An all DC series connected wind farm configuration has the minimum number of conversion stages among all the wind farm configurations present in the current market. However, the reliability of this configuration is lowest since the whole wind farms goes down due to one wind turbine failure. A modular arrangement of wind farm may be possible similar to modular multilevel converter, where a failed wind turbine can be bypassed, and the rest of the wind farm can continue to be in operation. This is technically possible with the advancement in power electronic technologies such as MVDC breakers. However, the author is skeptical about the economic viability of such an arrangement. With this hypothetical assumption, an all DC wind farm configuration is proposed for this master. While the possible optimization of wind turbine conversion system is broad, a small part of it is pursued considering the time limitation. The optimization pursued in this project is applicable irrespective of wind farm configuration.

6.2 The Modular Multilevel Converter

The modular multilevel converter is emerging as a promising, futuristic topology for medium voltage high power wind energy conversion system, yet complex to implement. There are several MMC topologies and many sub module topologies. For this master thesis, wind generator side converter is designed using double star MMC topology with half-bridge sub module intended for three-phase AC to DC conversion. The half-bridge sub module is chosen since it is simple to implement and most popular among all the sub module topologies.

The author feels that, one needs to develop deeper and intuitive understanding to implement MMC in Simulink/MATLAB or a hardware prototype. Hence the students working on MMC for master thesis may be given more time to digest all the dynamics. Moreover, the simulations

are cumbersome, slow and time consuming, hence it is recommended to provide access to super computer. Sixty two number of simulations are carried during this project, each simulation taking two to three hours. This time can be reduced significantly using a high speed computer.

6.3 SiC devices

Wide band gap semiconductor devices are emerging as a promising alternative, as silicon has reached its theoretical material (physical) limits. Silicon Carbide is promising for high voltage, high power levels among all the wide band gap materials due to its advantageous characteristics.

SiC semiconductor devices are in development stages. SiC MOSFET is in the advanced stage of development among SiC switches. There are few commercial models of SiC MOSFET such as 900 V, 1200 V, 1700 V in the current market. For this project, all three mentioned SiC MOSFETs are used manufactured by Wolfspeed (A Cree Company). In MMC, it may be recommended to use SiC MOSFET with lowest voltage rating because,

1. Higher number of sub modules, voltage levels
2. Better voltage waveform
3. Reduced filter requirement
4. Reduced semiconductor losses
5. Lower cost

6.4 Optimization

The scope for optimization in wind energy conversion system is broad. In this project, the study and optimization are focused on semiconductor power losses, total harmonic distortion in an MMC intended to operate as wind generator side converter. Semiconductor losses and total harmonic distortion are measured in Simulink/MATLAB environment by varying the number of submodules and the number of parallel connected semiconductor devices for three SiC MOSFETs with rating 900 V, 1200 V, 1700 V manufactured by Wolfspeed (Cree Company). The following observations can be made through the results obtained,

1. Conduction losses are predominant compared to switching losses because SiC MOSFET is faster and sub module switching frequency in MMC is lower.
2. The semiconductor losses (conduction losses) increase with increase in the number of sub modules. This is due to the fact that the current through sub modules remains same and additional sub modules are added. Hence, the minimum number of sub modules must be used to achieve maximum efficiency. However, the voltage waveform improves

resulting in the reduced filter requirement. Hence the study of losses should be extended for wind energy conversion system in order to calculate the optimal number of sub modules.

3. The on-state resistance of SiC MOSFET increases with increase in current and increase in junction operating temperature. Conduction power losses of SiC MOSFET depends upon on-state resistance and current. Conduction power losses are limited by the maximum operating junction temperature due to thermal limitation. Therefore, maximum current of SiC MOSFET is calculated assuming the maximum operating junction temperature of 125°C. The number of parallel connected MOSFETs can be determined based on the maximum current allowed to flow through SiC MOSFET and arm current. The semiconductor losses decrease with increase in the number of parallel connected SiC MOSFETs. Hence, efficiency can be further increased by increase in number of parallel connected MOSFETs. However, economic viability depends on the cost of SiC MOSFET and cost of energy (conduction power losses).
4. The wind turbine load profile is not considered in this project. However, it plays an important role in determining the optimal number of sub modules, parallel connected devices, operating junction temperature.

As a Future work, it would be interesting to extend the Simulink/ MATLAB model to the complete wind energy conversion system and running the simulations with different power electronic converter topologies using SiC devices and their Si counterparts.

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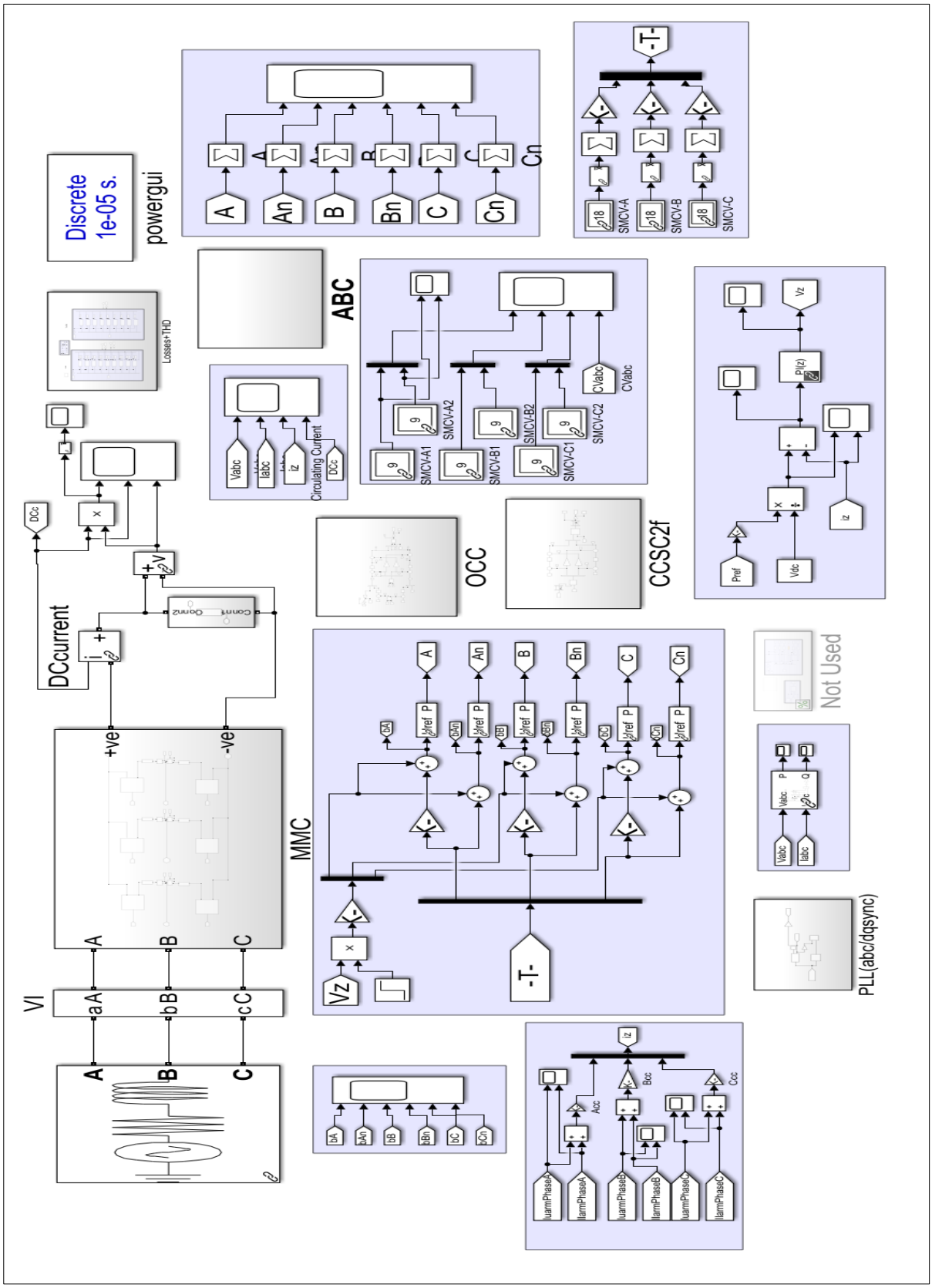
Appendix

The Snapshot of Simulink/MATLAB Model



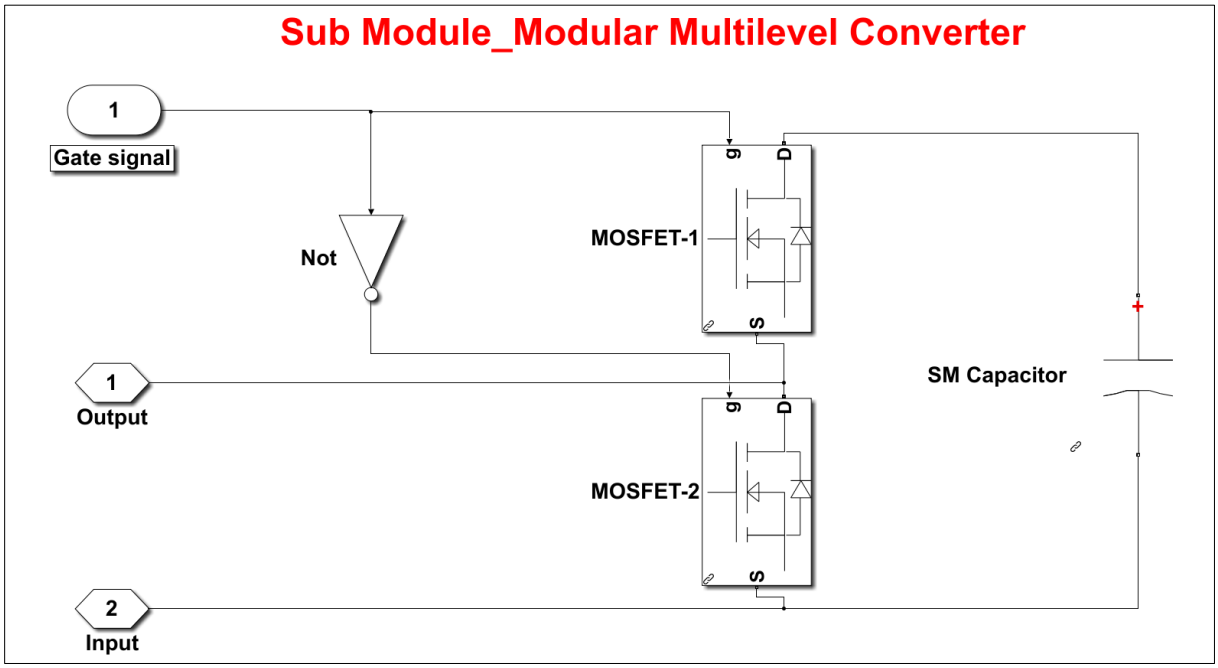


Figure A.1 Snapshot of Sub Module in Simulink

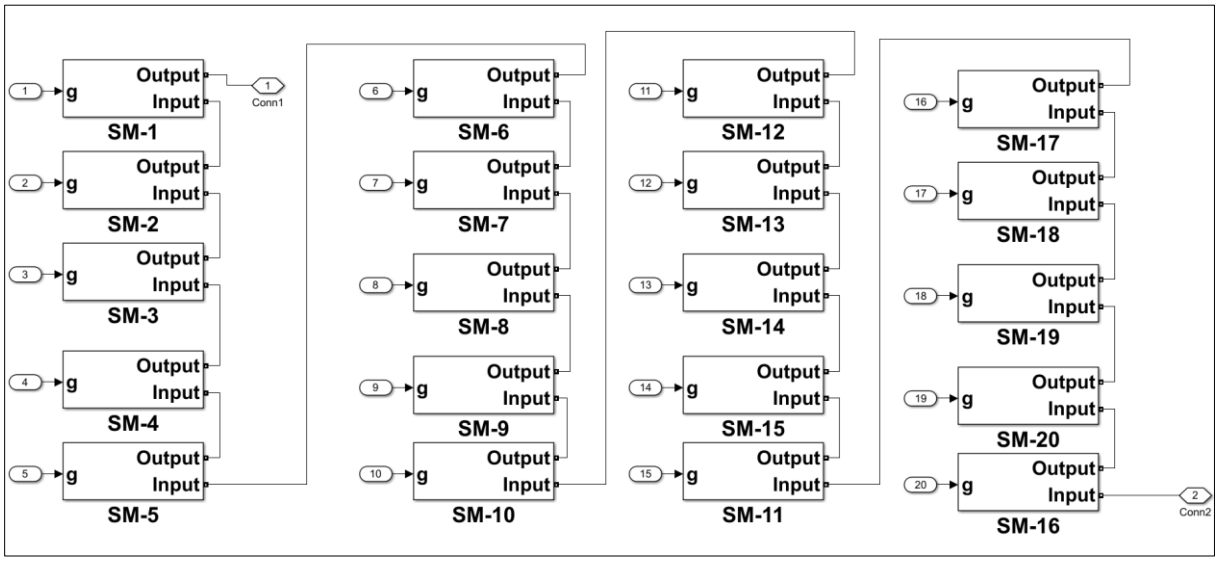


Figure A.2 Snapshot of series connection of Sub Modules for each arm

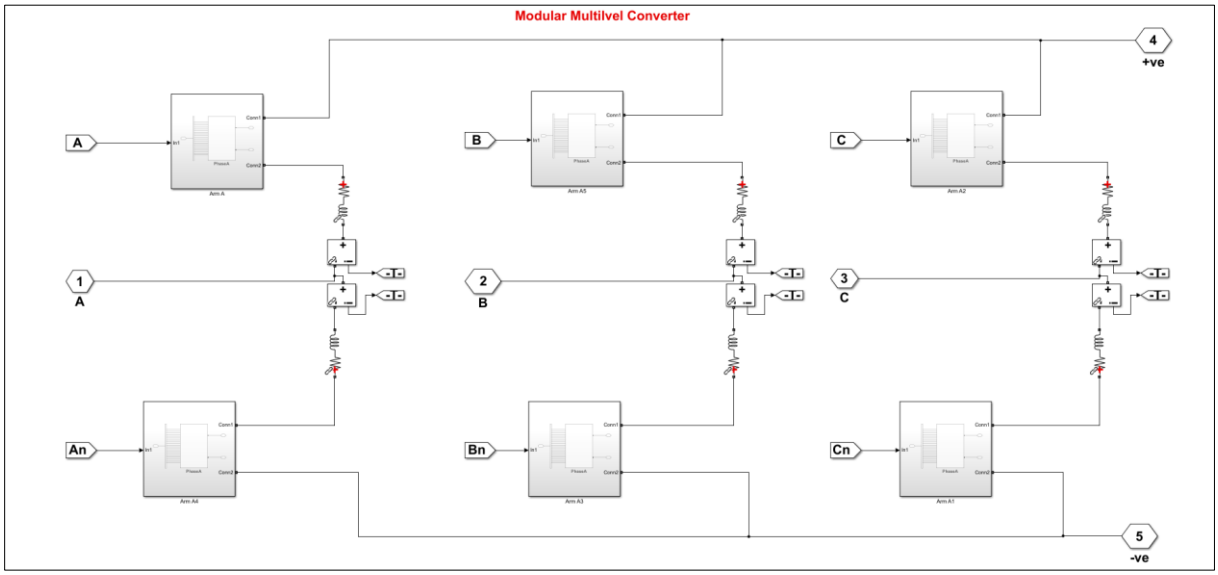


Figure A.3 Snapshot of MMC

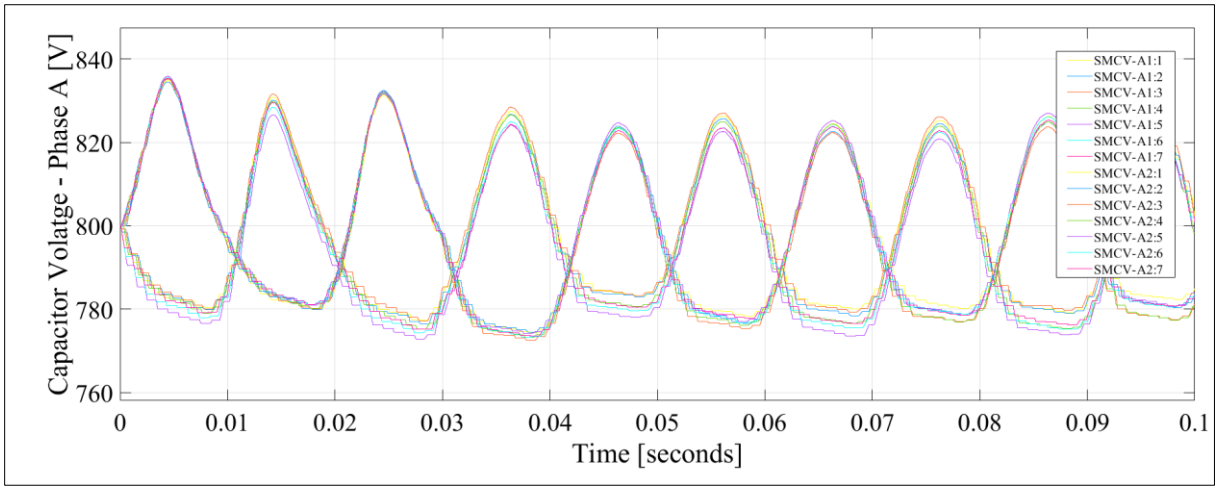


Figure A.4 Sub Module Capacitor Voltage Ripple

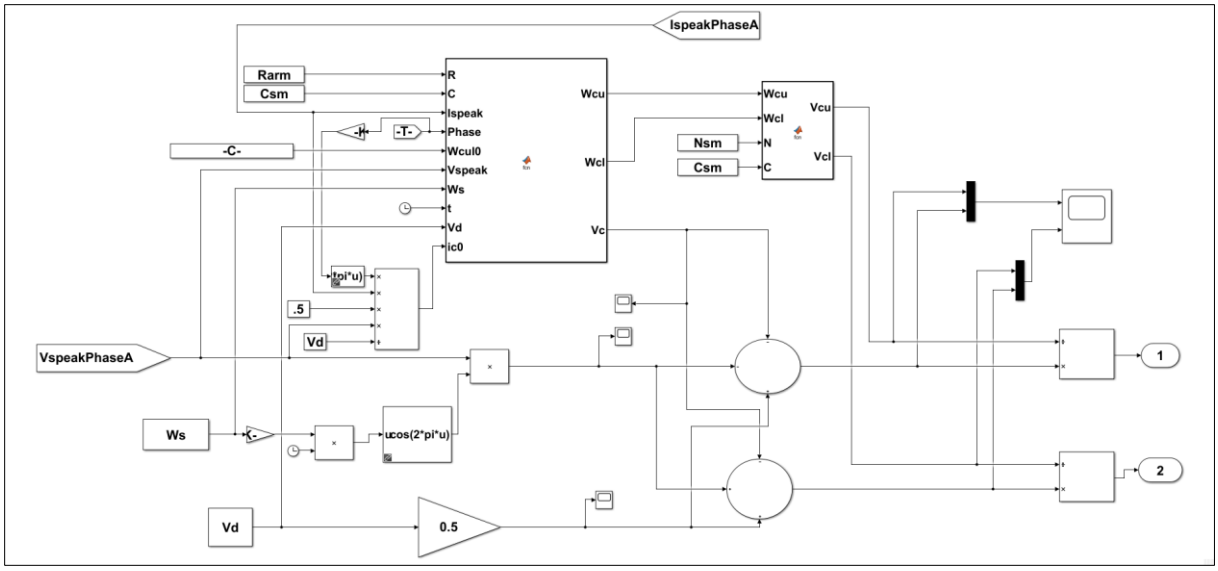


Figure A.5 Snapshot of Open-Loop Control

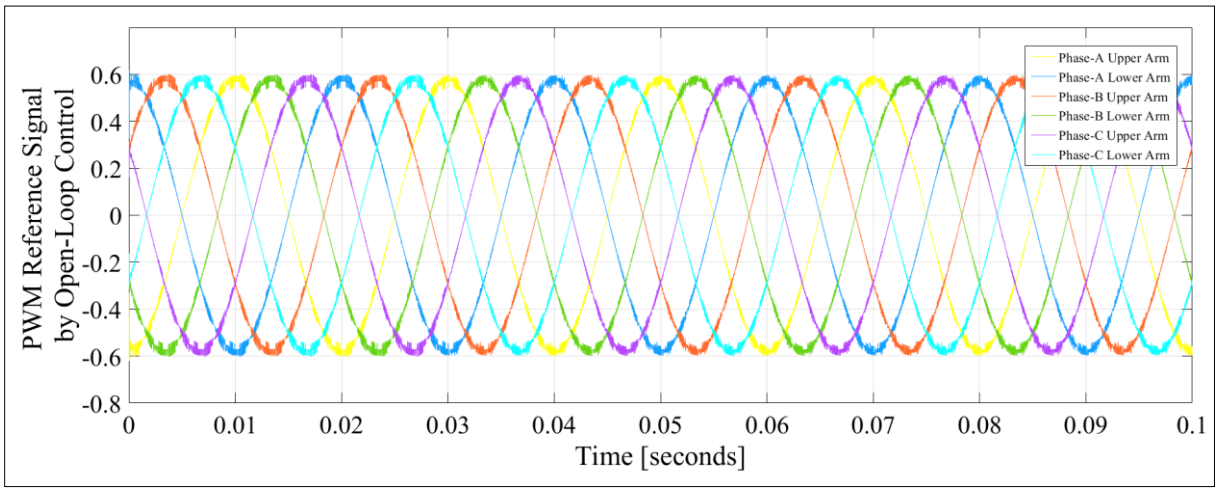


Figure A.6 PWM Reference Signal by Open-Loop Control (Modulation index = 0.6)

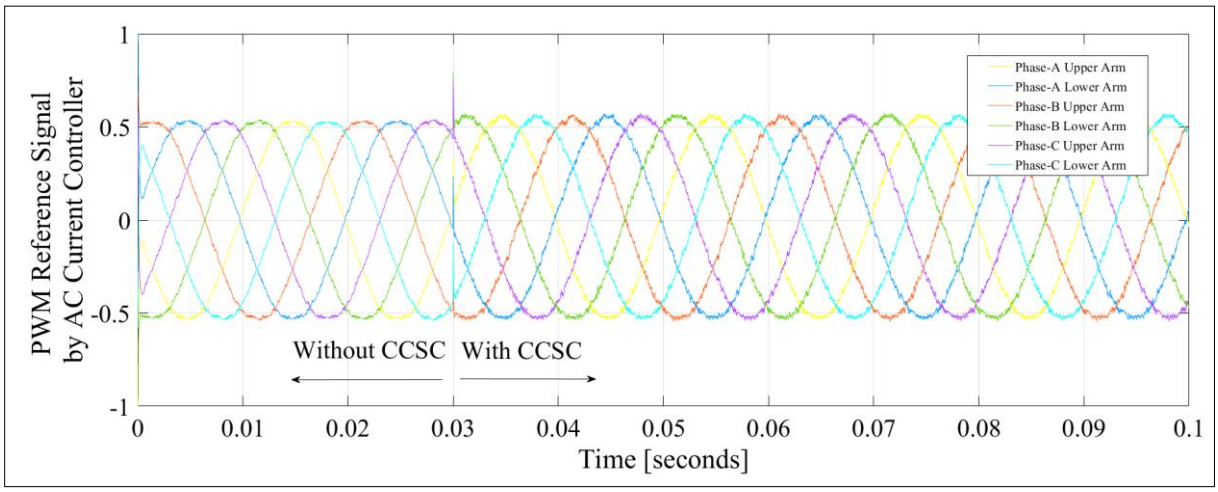


Figure A.7 PWM Reference Signal by AC Current Controller (Modulation index = 0.6)

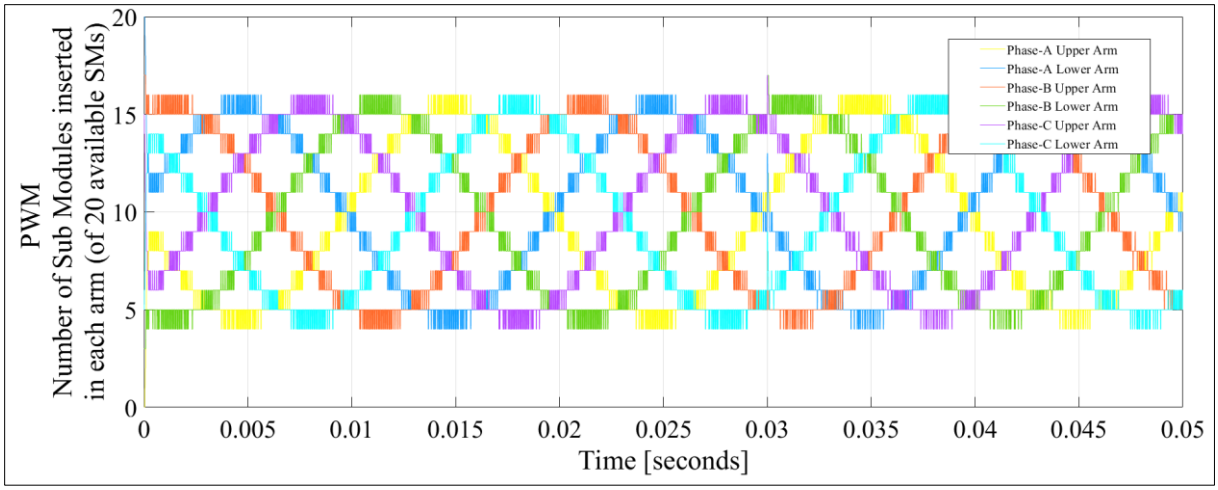


Figure A.8 CPS-PWM output Signal (Modulation index = 0.6)

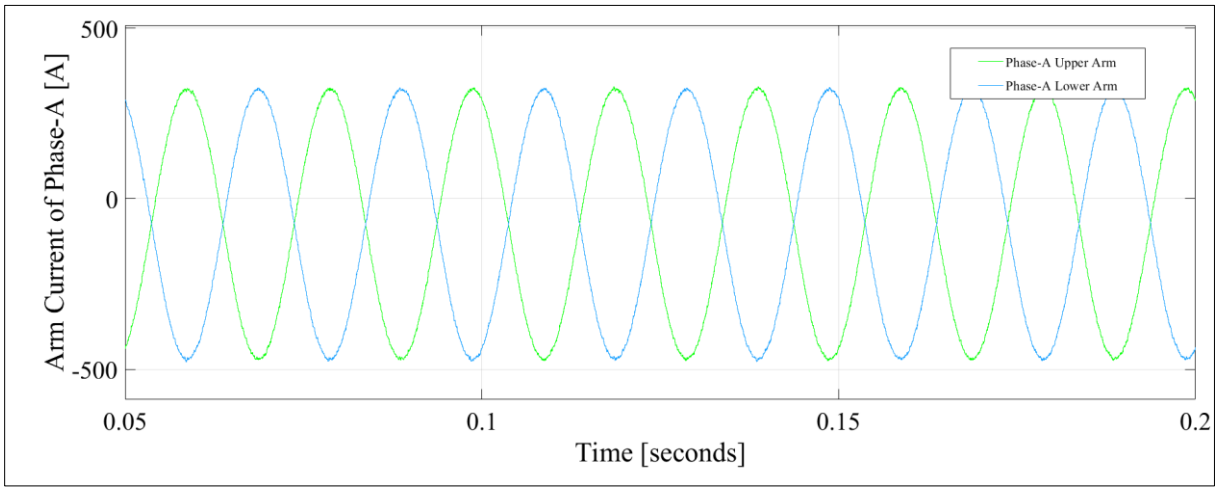


Figure A.9 Arm Current in Phase-A