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Design and Implementation of a High Resolution, Discrete-Time Delta-Sigma ADC

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Master of Science in Electronics
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Norwegian University of Science and Technology
Department of Electronic Systems

PROJECT ASSIGNMENT

Candidate name: Duvarahan Kirishnathasan

Assignment title: Embedded High-Resolution Delta-Sigma ADC for Microcontrollers

Assignment text:

The main objective is to define a state of the art high-resolution delta sigma ADC. Main features are approx 16 bits resolution and above 10MHz conversion rate.

In this project the student will do a study on delta-sigma type ADC converters to find good trade-offs and optimize a design for high-resolution conversion in embedded applications. The chosen approach shall then be assessed and modelled to develop a complete ADC design specification.

The project will be suitable for students with analog and mixed-signal specialization, and an interest for analog-to-digital converters in particular. Microchip will offer the opportunity for enthusiastic students to develop their skills in a leading edge electronics R&D environment.

The required software, hardware and a working place at Microchip's office could be provided.

Assignment proposer / Co-supervisor: Ivar Løkken

Supervisor: Trond Ytterdal

Abstract

This thesis do a study on ΔΣ type A/D converters to find good trade-offs and optimize a design for high resolution conversion in embedded applications. The main objective is to define a state of the art high-resolution ΔΣ ADC with main feature such as approximate 16 bits resolution and above 10MHz conversion rate. A behavioral model was developed in the the feasibility study to derive a complete design specification for a third-order fully differential discrete ΔΣ modulator. The specifications were used in this thesis to implement the modulator in transistor-level. The circuit is developed in a $0.18\mu m$ CMOS process technology that employs a standard supply voltage of 1.8 V.

The OTAs are designed using folded cascode topology. A wide swing current mirror is used to bias the transistors, and switched CMFB circuit is implemented to stabilize the common mode output of the OTAs. A methodology called g_m/I_D is used to find dimensions for the transistors of the OTAs by characterizing their performances. The 1-bit quantizer is implemented as a latched comparator with low hysteresis. A two-phase non-overlapping clock generator with delayed phases is designed in order to operate the discrete circuit. The simulations on each corner of the technology confirm that the modulator satisfies the specifications, even in the worst case. The nominal simulation with transient noise gives a SINAD equals to 98.23dB which corresponds to a resolution of 16.2 bits. The total static power dissipation is $87\mu W$ with a FoM of $0.20pJ/step$. The are was estimated to $0.077mm^2$.

Sammendrag

Denne masteroppgaven gjør en studie av ΔΣ type A/D konverterer for å finne gode kompromisser og optimalisere et design for en konverterer med høy oppløsning i innvevde applikasjoner. Hovedmålet er å definiere det nyeste innenfor høy-oppløsning ΔΣ ADC med tilnærmet 16 bits oppløsing og over 10MHz konverteringsfrekvens. En adferdsmodell ble utviklet i forprosjektet for finne en fullstendig liste med spesifikasjoner for en tredje ordens, fullt differensial diskret ΔΣ modulator. Spesifikasjonene ble brukt i masteroppgaven til å implementere modulatoren i transistor-nivå. Kretsen er utviklet i $0.18\mu m$ CMOS prosess og det er brukt en forsyningsspenning på 1.8 V.

OTA-ene er designet ved hjelp av folded cascode-arkitektur. Et strømspeil med bredt sving er brukt til å forspenne transistorene, og en CMFB-krets er implementert til å stabilisere utgangen av OTA-ene. En metodikk kalt g_m/I_D er brukt til å finne størrelsene til transistorene som OTA-ene består av, ved å karakterisere deres oppførsel. En 1-bit kvantitisator er implementert som en låst komparator med lav hysterese. En ikke-overlappende klokkegenerator som generer to faser og deres respektive forsinkende faser har blitt designet for å operere den diskrete kretsen. Simulasjonen i hvert hjørne av prosessen bekrefter at modulatoren tilfredsstiller spesifikasjonene, også for det verste tilfellet. Nominell simulasjon med flyktig støy gir en SINAD på 98.23dB som tilsvarer en oppløsning på 16.2 bits. Det totale statiske effektforbruket ble $87\mu W$ med en FoM på $0.20pJ/step$. Arealet ble estimert til $0.077mm^2$.

Preface

This thesis was carried out during Spring 2018 and submitted to NTNU, Trondheim June 18, 2018.

I would like to thank Microchip Technology for letting me stay and work in their office, and for providing design tools to complete my task. I like to especially thank my supervisor Ivar Løkken for providing great support, guidance and insight throughout the work with this thesis.

I would also like to thank Trond Ytterdal for offering great input, guidance and for sharing his great experience in circuit design which made the process of the design much easier.

Trondheim, June 18, 2018,

Duvarahhan Kirishnathasan

Abbreviations & Symbols

A/D: Analog-to-Digital

AAF: Anti-Aliasing Filter

ADC: Analog-to-Digital Converter

CMFB: Common Mode Feedback Block

CMOS: Complementary Metal Oxide Semiconductor

CT: Continuous Time

DAC: Digital-to-Analog Converter

DC: Direct Current

DR: Dynamic Range

DSP: Digital Signal Processor

DT: Discrete Time

ENOB: Effective Number of Bits

FoM: Figure of Merit

GBW: Gain-Bandwidth Product

IC Integrated Circuit

NMOS: N-Channel MOSFET

NTF: Noise Transfer Function

OSR: Oversampling Ratio

OTA: Operational Transconductance Amplifier

PMOS: P-Channel MOSFET

PSD: Power Spectral Density

PVT: Process, Voltage, Temperature

SC: Switched Capacitor

STF: Signal Transfer Function

OSR: Oversampling Ratio

S/H: Sample-and-Hold

SFDR: Spurious Free Dynamic Range

SINAD: Signal-to-Noise-Distortion Ratio

SNR: Signal-to-Noise Ratio

SNDR: Signal-to-Noise-Distortion Ratio

SoC: System on Chip

SQNR: Signal-to-Quantization-Noise Ratio

THD: Third Harmonic Distortion

VLSI: Very Large Scale of Integration

A_o**:** DC Amplifier Gain

C_s**:** Sampling Capacitor

C_i**:** Integrating Capacitor

f_b**:** Input Signal Bandwidth

f_s**:** Sampling Frequency

ΔΣ: Delta-Sigma

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Chapter 1

Introduction

Computational and signal processing tasks can be performed by digital circuits, since they are robust and can be realized by small and simple structures to obtain complex, fast and accurate systems. As the time passes the speed and density of digital integrated circuits have increased, but the physical world has remained the same, which means that the data converters are still needed to be able to communicate with it by utilizing digital signal processing (DSP). One thing to note is that digital circuits in the modern technology offer fast transistors biased at low voltage, which introduce drawbacks in the analog design such as the short-channel effects and larger leakage currents.

Analog-to-digital (ADC) converters are an important part of microcontrollers and system-on-chip (SoC) products. More applications demand higher resolution and slower converters, for example for applications such as battery management and sensor measurement. This is driven by the desire to measure very small input signals, for which a $\Delta\Sigma$ ADC is very suitable. Figure 1.1 exhibit the trade-off between accuracy and speed for various ADC structures. The fastest one with lowest obtainable resolution is flash ADC. With a conversion speed of 1GHz it can only achieve a resolution up to 8 bits. The reason being the area grows proportional with 2^M (Where M is the number of bits). The folding and SAR ADCs manage to give better resolution than the flash ADC, but at the cost of

slower conversion speed. These can be used on applications which require medium speed and medium resolution. Pipeline ADC is good to use to achieve resolution up to 14 bits with a high conversion speed from 1MHz to 100MHz. When high resolution is required, the integrating ADC is a good alternative, but it requires 2^M clock periods to convert a single sample. Hence, it is a good choice for applications with high resolution and very low frequency demand.The ADCs discussed are Nyquist-rate converter, and as seen they cannot not provide good accuracy with high speed. Oversampling converters like ΔΣ converters on the other hand are well suited, with high resolution acquisition and low power consumption. They are also widely used ADC architecture, as they relax the requirements of the analog building blocks by the use of oversampling and noise-shaping.

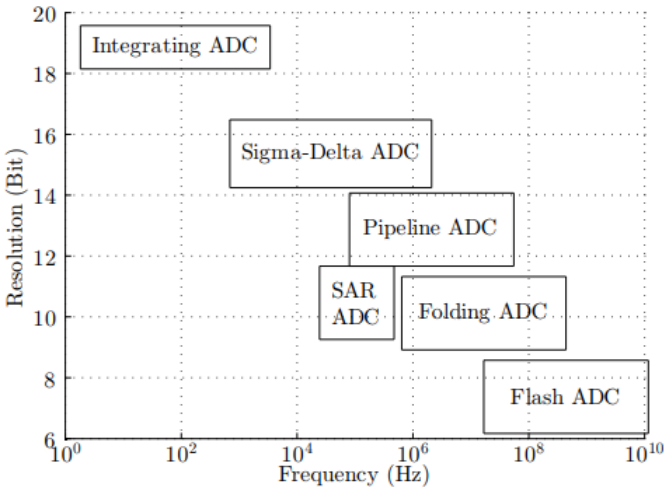


Figure 1.1: Bandwidth and resolution specifications of different ADC architectures

However the design of ΔΣ is not a easy task, as it relies on analog design techniques as well as advanced filtering and signal processing techniques. To find a good architecture depends on proper modelling of the behaviour of the converter. Designing a ΔΣ modulator which reaches the application's specifications featuring low power is of big interest, and is proven to be a challenge.

1.1 Thesis Contribution

This thesis aims at showing the design and implementation of a $\Delta\Sigma$ modulator based on the feasibility study[2] done in Autumn. The main objective is to achieve approximately 16 bits resolution and manage to sample it at 10MHz. The modulator was designed using 180nm complementary-metal-oxide-semiconductor (CMOS) process technology with 1.8V of supply voltage. The modulator implemented is a fully-differential, third order discrete time modulator which uses three low pass filters, a latched comparator acting as a 1-bit quantizer and a 1-bit feedback digital-to-analog (DAC) to obtain the desired resolution.

Figure 1.2 depict the design flow of the $\Delta\Sigma$ modulator. It can be seen that a higher level define specification for a lower level. A bottom-up approach was used to verify the system i.e. starting with verifying from transistor-level and working up to system-level. The work can be divided into three stages, as described below.

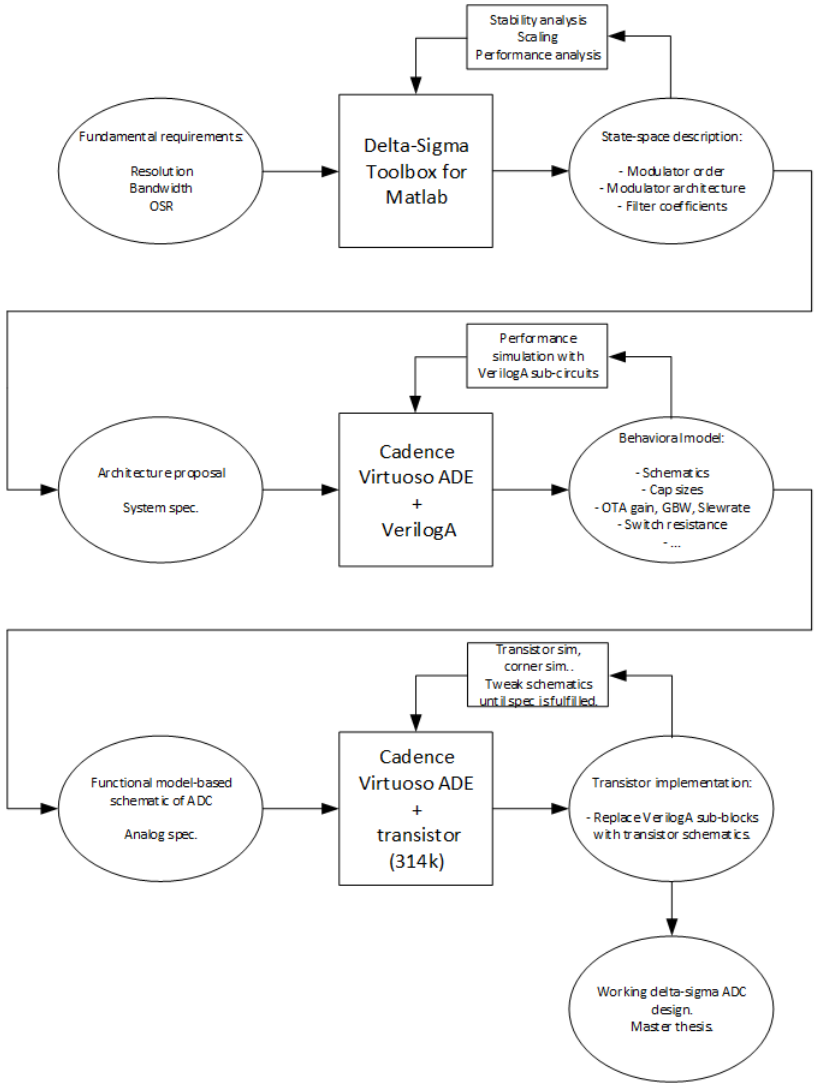


Figure 1.2: Design flow of the ΔΣ modulator

The model was first synthesized using Richard. Schreier's ΔΣ toolbox in MatLab[27] based on the fundamental requirements, such as resolution, bandwidth and OSR. The results from the toolbox were used to derive a state description based on the modulator order, filter coefficients, number of bits of the quantizer and loop topology. Stability and performance analysis were performed in order to maintain the modulator's integrity.

VerilogA was used to implement the analog blocks from the architectural performance. Behavioral model was done by Cadence Virtuoso ADE to derive the specifications of the analog blocks such that the fabrication process variations do not affect the system performance.

Finally the VerilogA models were replaced by transistor schematics. These schematics were verified according to the specifications found in behavioural modeling using nominal and process, supply voltage and temperature variations (PVT simulations) using Spectre.

1.2 Thesis Outline

Chapter 2 - Background theory: The fundamentals of $\Delta\Sigma$ concept of oversampling, noise-shaping and switched-capacitor circuits are presented. Additionally the theory behind the g_m/I_D methodology used to size the transistors of the OTAs is also presented.

Chapter 3 - Proposed architecture: The decision of the architecture based on loop filter order, topologies, time-domain, number of quantizer bit and operational transconductance amplifier (OTA) architectures is also discussed.

Chapter 4 - Specifications of the design: The results obtained in the feasibility study is summarized and discussed here. They were used as specifications to implement the analog blocks in transistor level.

Chapter 5 - Circuit design: It contains the complete design methodology adopted to the successful implementation of the modulator. It also presents the analysis and the design of the analog blocks used, such as: switches, two phase clock generator, OTAs and comparator.

Chapter 6 - Results: Here the results and discussion of all the blocks designed and implemented are presented, where the results are presented by both nominal and PVT simulations. The nominal and PVT simulations of the whole modulator are given as final results for the thesis.

Chapter 7 - Conclusion : A summary and conclusion of the work are presented. Some suggestions regarding the future works are also presented.

Chapter 2

Background Theory

2.1 ADC Converters Fundamentals

The structure of an typical ADC is shown in the Fig. 2.1. It consists of four main blocks: an anti aliasing filter(AAF), a sample and hold circuit(S/H), a quantizer and a digital filter(decimator).

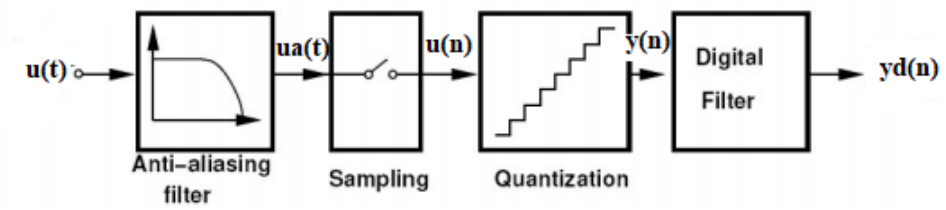


Figure 2.1: Block diagram of a an ADC

The AAF is placed in front of the S/H circuit to remove spectral components higher than the bandwidth $\mid \frac{f_s}{2} \mid$ from the input signal $u(t)$, where f_s is the sampling frequency. Thus by band-limiting the signal, it makes sure that the S/H circuit won't fold unwanted high spectral components into the band of interest. Despite being an essential block of the

converters, it has to be implemented off-chip and not integrated in a ADC at a SoC-system, due to the large component values needed to realize it.

After the signal has been conditioned to a band, the AAF's output $u_a(t)$ is sampled by the S/H circuit at the sampling frequency f_s. The output of the circuit will be $u(n) = u_a(nT_s)$, where T_s is the sampling period($\frac{1}{f_s}$), and n is an integer in the range of 0 and the total number of samples. The next stage of the conversion process is done by the quantizer. It takes a continuous values of the sample data $u(n)$, and maps them onto a finite number of discrete values/levels. It will introduce a distinction between the mapped values and the actual analog value. This distinction is often called the quantization error(ε_Q) that is often referred to as the quantization noise of the ADC. If we assume that the quantizer's input signal $u(n)$ varies quite rapidly, then we approximate the quantizer noise to a uniformly distributed additive white noise. Hence we usually choose to model the quantizer noise as white noise with the average power given by the following expression:

$$P_E = \frac{\Delta^2}{12}, \tag{2.1}$$

where

$$\Delta = \frac{V_{FS}}{k}, \tag{2.2}$$

V_{FS} is the full-scale of the quantizer, while k is the number levels the quantizer consists of. Meaning if we have a N-bit quantizer, then the number of levels is given by $k = 2^N$.

The output signal $y(n)$ of the quantizer is a digital pulse train that gets sent to the digital filter. The digital filter performs low-pass filtering and down-sampling on the signal $y(n)$ to eliminate out of band noise above the bandwidth $\frac{f_s}{2}$, and providing an output with Nyquist rate with a bit width corresponding to the ADC's resolution.

2.2 Performance Metrics

There are many metrics used to determine the performance of an ADC as shown in [4], [5], [6], [7], [12] and [17]. We will look at those which are most useful to measure the performance of a $\Delta\Sigma$ modulator. These are used to analyze the output spectrum of the modulator. For example we can obtain metrics such as SNR, SNDR, DR and ENOB by analyzing outputs as depicted in Fig. 2.2 for a determined input power.

2.2.1 Resolution

Resolution of a converter is defined as the distinct number of analog levels corresponding to the different digital words. Thus, if the ADC has a N-bit resolution, the converter can resolve 2^N distinct analog levels.

2.2.2 Dynamic Range (DR)

Dynamic range of an ADC is defined as the range of amplitudes the ADC can effectively resolve. The ADC can overload if the signal is too large, and can get lost in the quantization noise if it too small. It can be defined in two ways. One is the ratio of the full scale value to the smallest difference it can resolve i.e. V_{LSB}

$$DR = 6.02N. \tag{2.3}$$

The other definition is the power of the input signal where the SNR (or the SNDR) is $0dB$.

2.2.3 Signal-to-Noise Ratio (SNR)

Signal-to-noise ratio is the ratio between the signal power and the total noise power at the output. When the case is only quantization noise, it is called signal-to-quantization-noise ratio(SQNR).

2.2.4 Signal-to-Noise-Distortion Ratio (SNDR)

SNDR is the ratio of the signal power to the total noise and the harmonic power at the output. The parameter is also called signal-to-noise and distortion ratio(SINAD).

2.2.5 Spurious Free Dynamic Range (SFDR)

SFDR is defined as the ratio between the RMS value of the input sine wave for an ADC and the RMS value of the peak spur(the strongest harmonic component power) observed in the frequency domain. Some communication application require maximizing the dynamic range of the converter, here SFDR is an important parameter.

2.2.6 Total Harmonic Distortion (THD)

THD is defined as the ratio between the sum of the powers of the harmonic frequencies inside the signal bandwidth and the power of the fundamental frequency. Thus the definition can be expressed as:

$$THD = \frac{\sum Harmonic\,frequencies}{Fundamental\,frequency} = \sqrt{\frac{V_2^2 + V_3^2 + ..+}{V_1^2}} \tag{2.4}$$

2.2.7 Effective Number of Bits (ENOB)

This metric gives actual number of bits for a given SNDR or SINAD. It is defined by the following equation:

$$ENOB = \frac{SNDR - 1.76}{6.02} \tag{2.5}$$

2.2.8 Overload Level

It is the maximum level of input amplitude for which the system can still operate correctly.

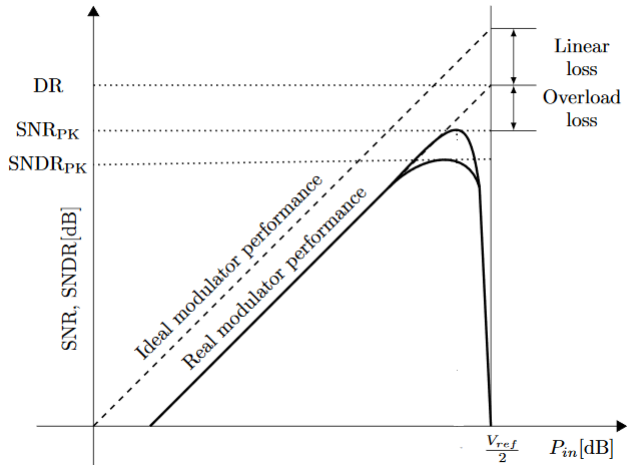


Figure 2.2: Typical SNR vs. Input power

2.3 Classification of Data Converters

Which category the data converters is placed in is influenced by the sampling frequency used for the conversion process. Broadly speaking the data converters can be classified into two categories; Nyquist-rate -and oversampling converters[3].

2.3.1 Nyquist-Rate Converters

The Nyquist-rate converters are based on the well known sampling theorem also known as the Nyquist theorem, which state the sampling frequency f_s should be at least twice as large as the bandwidth f_b in order to avoid aliasing and successfully reproduce the signal after filtering. Hence it will use an input occupying a large portion of the available bandwidth. The quantization noise in a Nyquist-rate converter is given by expression: 2.1. In Nyquist-rate converters, the sampling frequency is usually at least twice the signal bandwidth. The maximum SQNR of a Nyquist-rate converter can be obtained[1][Chapter 1.1], as seen in expression(2.4), where N is the number of bits.

$$SQNR_{maxNQ} = 6.02N + 1.76dB \tag{2.6}$$

2.3.2 Oversampling Converters

In the preceding section it was mentioned that Nyquist-rate converters will use an input occupying a large potion of the available bandwidth. Oversampling converters on the other hand only occupy a small portion of the bandwidth, thus spreading the quantization noise over a wider frequency range as depicted in Fig. 2.3. This causes the quantization noise to be reduced.

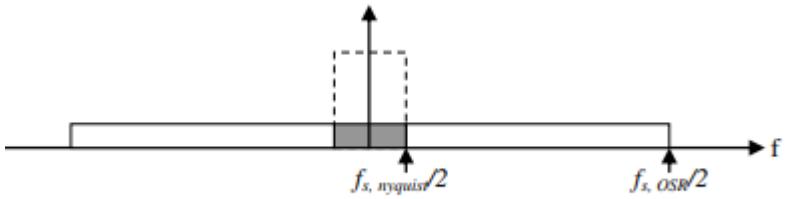


Figure 2.3: Quantization noise spectrum of a Nyquist-rate and a oversampling converter

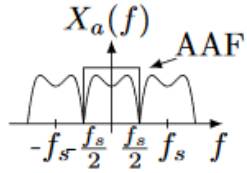
To be able to operate in such small portion of the bandwidth, the oversampling converters have to sample the input signal in a much higher rate than the Nyquist-rate converters. This rate is given by the oversampling ratio (OSR) which is defined as,

$$OSR = \frac{f_s}{2f_b} \tag{2.7}$$

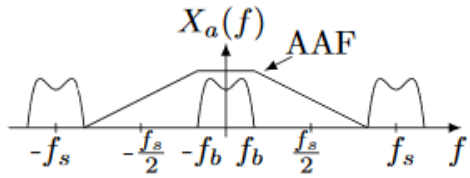
To establish the advantage of oversampling converters compared to Nyquist-rate converters, we can look at the maximum SQNR for a oversampling converter. It can be calculated for oversampling converters[5][Ch 18.3], as seen in expression 2.8, where N is the number of bits.

$$SQNR_{maxOS} = 6.02N + 1.76 + 10\log_{10}(OSR)dB \tag{2.8}$$

If we compare equation 2.8 with equation 2.6, we can see that the oversampling rate ADC can achieve the same SQNR performance as a Nyquist-rate ADC with fewer bits. Further



(a) Anti aliasing filter for Nyquist-rate converter



(b) Anti aliasing filter for Oversampling converter

Figure 2.4: Anti aliasing filter for Nyquist-rate and Oversampling converters

it can be seen that for every doubling of OSR improves the SQNR with $3dB$, or ENOB by $0.5bits/octave$.

Another advantage of using oversampling ADCs is that the specifications of the AAF are relaxed, because the signal bandwidth is smaller than $\frac{f_s}{2}$. As shown in Fig. 2.4, the spectral components higher than the bandwidth f_b in a oversampling converter are more separated than in a Nyquist-rate converter.

2.4 Noise-Shaping ADC

To get a better understanding of noise-shaping, we have to first look at the ΔΣ modulator. The structure of typical ΔΣ ADC is shown in Fig. 2.5, which consists of four main blocks: a AAF, a S/H circuit, a ΔΣ modulator and a decimator. The AAF, S/H circuit and the decimator operates as explained in section 2.1.

Even though all four blocks are essential to the ADC, our main focus for this thesis is the ΔΣ modulator. As shown from the Fig. 2.5, the ΔΣ modulator consists of a loop

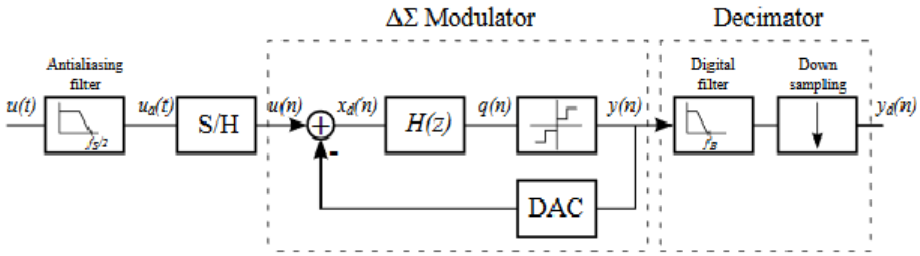


Figure 2.5: Block diagram of a discrete-time (DT) ΔΣ ADC[8]

filter ($H(z)$) along with an internal quantizer and a DAC, which together makes a negative feedback loop. The basic operation of the modulator is to compare the input signal with an estimate of the output data and quantizing this difference. This structure is advantageous for oversampling signals since the amplitude of the subtracted signal $x_d(n)$ is smaller than for the input signal $u(n)$. By having a loop filter with a very high gain in the signal band, the in-band quantization noise is strongly attenuated by the feedback loop. The input signal will nearly pass unaffected through to the output. This process is known as *noise-shaping*.

2.5 First Order ΔΣ Modulator

To get the basic understanding in how this system works, a linear model of the ΔΣ modulator is shown in Fig. 2.6. The quantizer is replaced with its noise source *e(n)* which we assume is white noise, and the DAC is replaced with a wire since we assume it is ideal. The system can be described by the transfer from each of the independent inputs: *e(n)* and *u(n)* to the output *y(n)*.

$$Y(Z) = \frac{H(z)}{1+H(z)}U(z) + \frac{1}{1+H(z)}E(z) \tag{2.9}$$

Here we can define signal transfer function *STF* and noise transfer function *NTF* as

$$STF(z) = \frac{H(z)}{1+H(z)}U(z) \tag{2.10}$$

and

$$NTF(z) = \frac{1}{1+H(z)}E(z) \tag{2.11}$$

As mentioned the loop filter *H(z)* has to have high gain in-band, while it may decrease outside. A commonly used filter is the delaying discrete time integrator

$$H(z) = \frac{z^{-1}}{1-z^{-1}} \tag{2.12}$$

By inserting equation 2.12 onto 2.10 and 2.11, we get

$$STF(z) = \frac{\frac{z^{-1}}{1-z^{-1}}}{1+\frac{z^{-1}}{1-z^{-1}}} = z^{-1} \tag{2.13}$$

and

$$NTF(z) = \frac{1}{1+\frac{z^{-1}}{1-z^{-1}}} = 1-z^{-1} \tag{2.14}$$

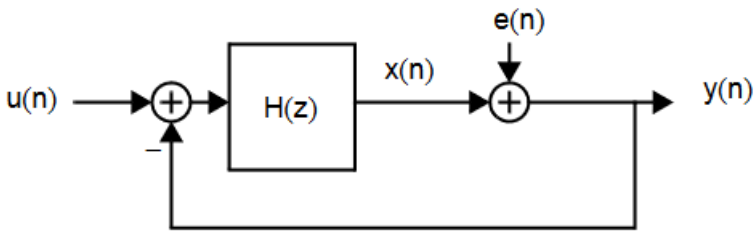


Figure 2.6: Linear model of ΔΣ modulator with inclusion of quantization noise [5]

We can see from equation 2.14 that the NTF is a high-pass filter. Therefore the in-band noise that resides on the lower frequency will be attenuated, and we can see the noise-shaping feature of the ΔΣ modulator. The STF 2.13 becomes a simple unit delay. This is seen as first order ΔΣ modulator, and the maximum SQNR is given in [5, Ch.18.2.2]

$$SQNR_{max} = 6.02N + 1.76 - 5.17 + 30log_{10}(OSR) \tag{2.15}$$

From equation 2.15, it can be noted that for every doubling of OSR, the SQNR improves with 9dB or ENOB with 1.5bits/octave. Compared with oversampling with no noise-shaping expression 2.6, we can see that the improvement is three times as good.

In the next chapter while exploring the different aspects of the ΔΣ modulator, we will see how increasing the order of the loop filter H(z), can further improve the noise-shaping and thereby improve the $SQNR_{max}$.

2.6 Switched-Capacitor Circuits

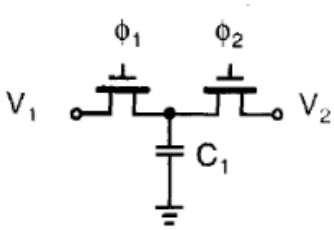
The resistors occupy huge space in a layout and they are also the sources of noises, which makes them unattractive to use in integrated circuits. A switched capacitor circuit can be used to emulate the behaviour of a resistor by a capacitor in and out of the circuit. Figure 2.7a depict a switch-capacitor circuit, where V_1 and V_2 are two dc voltage sources. The clock periods ϕ_1 and ϕ_2 are a pair of overlapping clocks, which means that the capacitor C_1 is charged to V_1 and then V_2 during each clock period. This charge transfer is repeated every clock period with a clock period of T_s. Thus, the average current is given by the charge moved in one clock period[5]:

$$I_{avg} = \frac{C_1(V_1 - V_2)}{T_s} \tag{2.16}$$

From the equivalent resistor circuit shown in figure 2.7b, we have that the current through the resistor is:

$$I = \frac{V_1 - V_2}{R_{eq}} \tag{2.17}$$

Comparing equations 2.16 and 2.17, we see that the average current through the SC circuit will be equal to the resistor circuit if:



(a) Switched-capacitor circuit

(b) Resistor equivalent

Figure 2.7: Resistor equivalence of switched capacitor capacitor

$$R_{eq} = \frac{T_s}{C_1} = \frac{1}{C_1 f_s} \tag{2.18}$$

A disadvantage is that the switches are implemented using transistors, and their non-idealities can degrade the SC circuit performance.

2.7 Switched-Capacitor Integrators

A differential switched-capacitor integrator circuit is shown in Fig. 2.8. It is known for its insensitive to parasitic capacitance of the sampling capacitor (C_s). The operation of the SC integrator can be explained by examining the charges on the capacitors on each clock phase. For simplicity we will only look at the top half circuit, since the bottom one has the same operation. It is assumed that the initial voltage stored in C_f is zero. Switches *S1* and *S3* are closed during phase Φ_1, while the others are closed during phase Φ_2. Note that Φ_1 and Φ_2 are two non-overlapping phases. When *S1* and *S3* are closed, the input source charges the capacitor C_s to a initial charge of $C_s V_{IN}$. During phase Φ_2, switches *S2* and *S4* are closed. Thus the input is disconnected from the circuit, and the bottom plate of capacitor C_s is connected to ground. Therefore the charge stored on the capacitor C_s is transferred to the capacitor C_f. Then when phase Φ_1 is active again the input voltage charge C_s with a new sample. Then during phase Φ_2, the charge from the new sample is transferred to the capacitor C_f where it accumulates with the previous charge from the first operation. The integrator corresponds to a non-inverting one, and the transfer function is

given by equation 4.1.

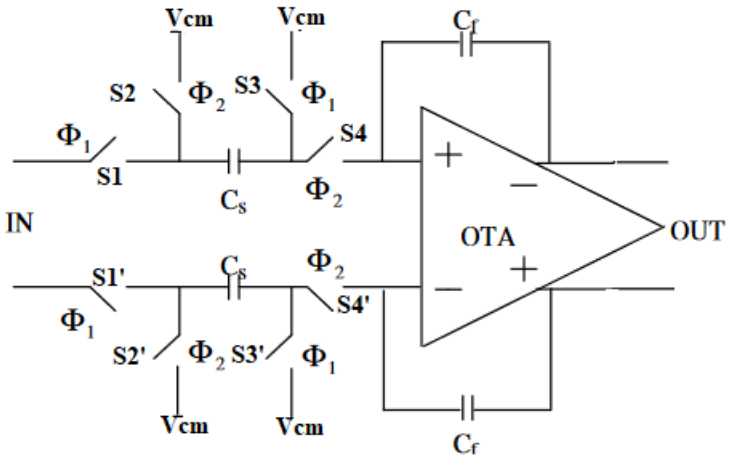


Figure 2.8: Parasitic-insensitive integrator

2.7.1 Channel Charge Injection and Bottom-Plate Sampling

Charge injection can be understood using the circuit in Fig. 2.9. When the MOSFET switch is *on* and V_{DS} is small, there is a charge present in the inversion layer called channel charge Q_{ch}. When the MOSFET turns of, this charge is injected onto the capacitor C_{load} and into V_{in}. Since V_{in} is assumed to be a low-impedance, source driven node, the injected charge has no effect on this node. However, the charge injected onto C_{load} results in a change in voltage across it, introducing an error in reading the correct input signal.

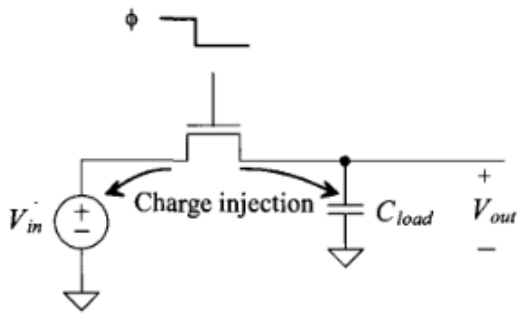


Figure 2.9: Charge injection in a sampling circuit

Although charge injection mechanism is complex to characterize, many techniques have been used to minimize its effect. One being bottom-plate sampling technique[7] which is employed to make charge injection of switches independent of the input signal. Figure 2.10 shows the integrator again, but now with delayed phases Φ_{1d} and Φ_{2d} with respect to phases Φ_1 and Φ_2 respectively. Switches *S3* and *S4* are turned off slightly before switches *S1* and *S2*, so that C_s sees a high impedance. Thus, the charge injection introduced by switches *S1* and *S3* flows towards the low-impedance source node and almost no charge is accumulated onto sampling capacitor C_s.

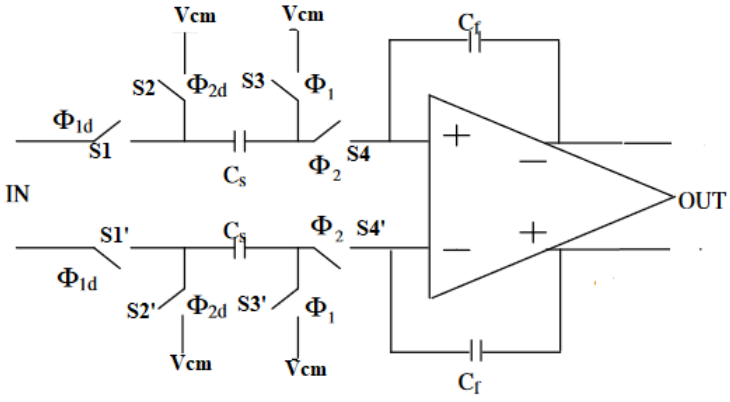


Figure 2.10: Integrator with bottom-sampling technique

2.7.2 Correlated Double Sampling

Correlated double sampling (CDS) technique was first introduced by White, Lampe, Biaha and Mack [21] as a technique for removal of switching transients and elimination of the Nyquist noise. What is more interesting is that it can be used to attenuate errors due to flicker noise $1/f$, finite offset voltage and finite opamp gain [18]. The technique is only used on the first integrator since the noise contribution is most critical in it. The noise contribution in the subsequent integrators are small, since the noise will be significantly attenuated as discussed in the feasibility study.

We will use a simple SC integrator depicted in Fig. 2.11 to illustrate how the CDS technique works. During ϕ_1, the capacitor C_2' samples the input offset voltage of the opamp. Then C_2' is connected in series with the opamp's inverting input during phase ϕ_2. The error from the opamp gets subtracted from the one stored in C_2', thus minimizing it. For a differential SC integrator a symmetrical circuit of the one shown in 2.11 is connected to the non-inverting input.

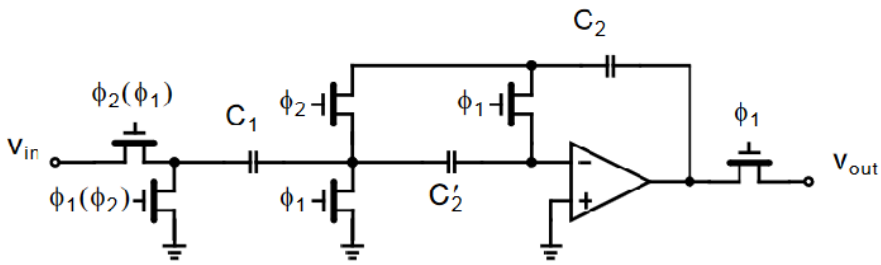


Figure 2.11: Simple SC integrator using CDS technique [5]

Another thing to note is that CDS will square the effective gain to the opamp due the extra capacitors, so the open-loop gain of the OTA for integrator will get relaxed, as seen in table 4.6, but at the expanse of bigger area. The resulting schematic of integrator 1 is shown in Fig. B.1, and the schematic used for the other two integrators is shown in Fig. B.2 in appendix B.

2.8 The g_m/I_D Methodology

With the emergence of advanced fabric processes the transistor dimensions have reduced drastically. As a consequence the traditional long-channel equations employed in the analog design were no longer producing desired results. In order to treat this inconvenience a new methodology was introduced by F. Silveria, D. Flandre and P. G. A. Jespers [14]. The method exploits the relationship between the ratio of the tranceconductance g_m over DC drain current I_D and the normalized drain current $I' = I_D/W$. It uses this relationship to determine the transistor dimensions to satisfy specifications like the GBW, low power, gain, etc. The g_m/I_D ratio can be obtained by characterization of the process of the PMOS and NMOS transistors. Some of the key elements with the g_m/I_D based design are described as follows[14],[25]:

- This method characterizes the performance of a transistor in all regions of operation. The curve generated for a particular process of a transistor is continuous and there are no transition in equations from various regions of operation, as it would be in the conventional long-channel equations. Thus we can freely select the device operation as per our needs.
- With the generated curve one can easily derive the transistor dimensions meeting the specifications, as we will see later.
- The amount of iteration in designing complex analog circuits is drastically reduced. The method gives a complete characterization of the technology, which involves taking into account the parasitic influencing the device. Thus eliminating the approximate equation used to determine the device behaviour and improving the time used to design the circuits.

Chapter 3

Proposed Architecture

The $\Delta\Sigma$ modulator was first introduced by Inose, Yasuda and Murakami in 1962 [15]. Since then many modifications to the architecture have been proposed to improve its performance. There are four main aspects of the architecture where one can modify it: time-domain, order of loop filter, topology and the number of bits of the quantizer. In this chapter we will review the different alternatives for an architecture with respect to the four aspects. To ease the discussion, we will mainly focus on single-loop architectures, since it will be integrated in a microcontroller and a simple architecture is desired. By designing a more complex system, we will only end up with an over-engineered proposal.

A small discussion of the proposed architecture found in the feasibility study will be presented in the last section. The bases for the discussion is based on the well known book; *Understanding Delta-Sigma Data Converters*[1]. Additionally a discussion around different topology of OTAs, and the choice between single ended and fully differential output will be discussed.

3.1 Order of Loop Filter

The expression of maximum SQNR for first order ΔΣ modulator 2.6 showed that for every doubling of the OSR yielded in increasing the SQNR with 9dB or ENOB with 1.5bits/octave. To be able to achieve a higher resolution i.e. higher ENOB, a larger OSR has to be used. The drawback with using a large OSR is that it requires large f_s/f_b, which can be hard or impossible to realize.

An obvious way to increase ENOB of the ΔΣ modulator is to use a high-order loop-filter. It can done by replacing the integrator in Fig. 2.6 with L number of integrator consecutively, where L corresponds to the order of the loop-filter. The NTF can then be given by

$$NTF = (1 - z^{-1})^L \tag{3.1}$$

In figures 3.1 and 3.2 it is shown how much OSR one need to achieve ideal SQNR and ENOB respectively, for different order of integrator. It can be observed to achieve 16 bit resolution, modulators on the order of 2 and 3 is sufficient. It can also be observed that the modulator with order 2 needs much larger OSR, which can cause problems with f_s/f_b.

Instability is an issue higher-order filters are struggling with. For first and second order filters, this is not a problem, but as the order of the filters gets bigger, the out-of-band gain(OBG) of the modulator gets more aggressive. The high OBG can cause overloading of the quantizer which can make the modulator unstable.

One can achieve stable operation by letting the input level be less or equal to the fullscale of the first feedback DAC. For high-order single-bit ΔΣ modulators this input range should be a few dB below the DAC fullscale[1, Chapter 4.2]. A rule of thumb to check if a high-order single bit ΔΣ modulator is stable is to use Lee's Criterion[20]:

$$|NTF_{max}| \leq 1.5 \tag{3.2}$$

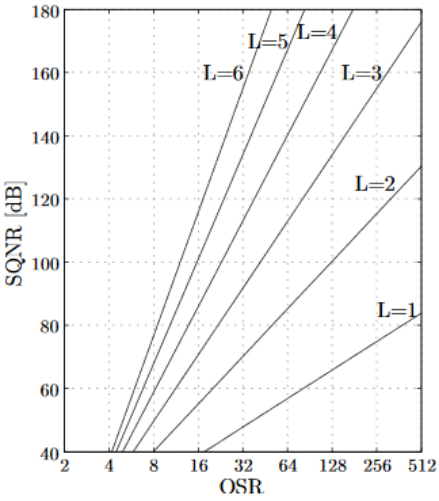


Figure 3.1: Ideal SQNR vs OSR[10]

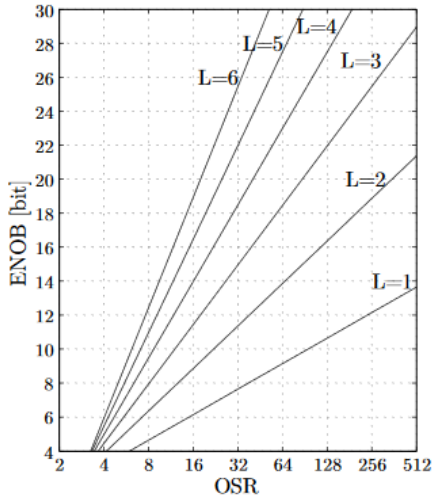


Figure 3.2: Ideal ENOB vs OSR[10]

where $|NTF_{max}|$ is the maximum magnitude over all frequency. Even when the criteria is fulfilled, there is a change the system will become unstable, because of the quantizer in the loop can turn the system into non-linear one[1].

3.2 Topologies

The alternatives to implement a ΔΣ modulators can be categorized into two categories: a single-loop or a cascade architecture. The first one refer to the use of only one quantizer, as seen in the section 2.5. The other one refer to multi-stage noise-shaping (MASH) modulator which is a popular structure that eases the stability problems associated with high-order modulators. Even though it has its advantages, we will not look into MASH modulators. The single-loop architectures are simpler to design and they are able to achieve the specifications given in chapter 1 at a ΔΣ order of 2 and 3. We will now look at the two most used single-loop architectures; feedforward and feedback topologies.

3.2.1 Feedback Topology

The figure 3.3a depict an example of 3^{rd} order feedback topology. The STF and NTF for this topology is given by

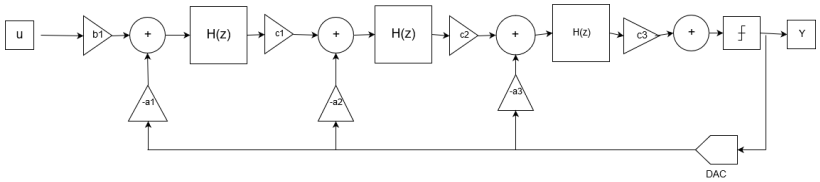
$$STF = \frac{b_1 c_1 c_2 c_3 H^3(z)}{1 + a_3 c_3 H(z) + a_2 c_2 c_3 H^2(z) + a_1 c_1 c_2 c_3 H^3(z)} \tag{3.3}$$

and

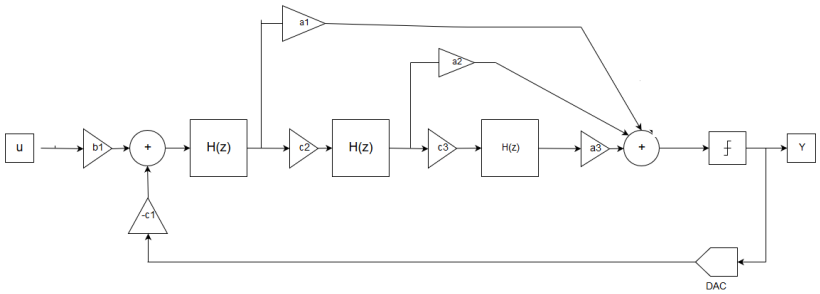
$$NTF = \frac{1}{1 + a_3 c_3 H(z) + a_2 c_2 c_3 H^2(z) + a_1 c_1 c_2 c_3 H^3(z)} \tag{3.4}$$

Here the forward coefficients (c_1, c_2 and c_3) represent the scaling or weighed of the integrators. The purpose of them is to scale the output dynamic range of the integrators. The coefficients on the feedback path (a_2 and a_3) are used to create a transfer function that gives a noise-shaping, while the feedback coefficient a_1 ensure that the output from the quantizer tracks the input.

One of the major drawbacks with this topology is that the output swings of the integrators tends to get big, which means that the the op-amp requirement has to be increased to avoid overloading. Furthermore the forward coefficients c_i has to become smaller in order to scale down the swing. The drawback on having small coefficients is that the area to maintain the same capacitor noise gets bigger, which leads to more power to charge capacitor. Another drawback is that unlike the feedforward-path, the output of the first integrator contains some amount of the input amplitude. This leads to higher swing capabilities, which again leads to a more power-consuming system.



(a) Feedback



(b) Feedforward

Figure 3.3: 3^{rd} order loop realization structures for feedforward and feedback

3.2.2 Feedforward Topology

An example on the 3^{rd} order feedforward topology is depicted in figure 3.3b. Unlike the feedback topology, this one has only one feedback from the quantized output. The coefficients (a_1, a_2 and a_3) are forwarded to the output, where their weight is added to the quantizer input. The STF and NTF are then given respectively,

$$STF = \frac{b_1(a_1H(z) + c_2a_2H^2(z) + c_2c_3a_3H^3(z))}{1 + b_1(a_1H(z) + c_2a_2H^2(z) + c_2c_3a_3H^3(z))} \tag{3.5}$$

$$NTF = \frac{1}{1 + b_1(a_1H(z) + c_2a_2H^2(z) + c_2c_3H^3(z))} \tag{3.6}$$

By moving the coefficients to the summation node in front of quantizer, the signal presented at integrators output will be significantly lower than at the feedback topology. This

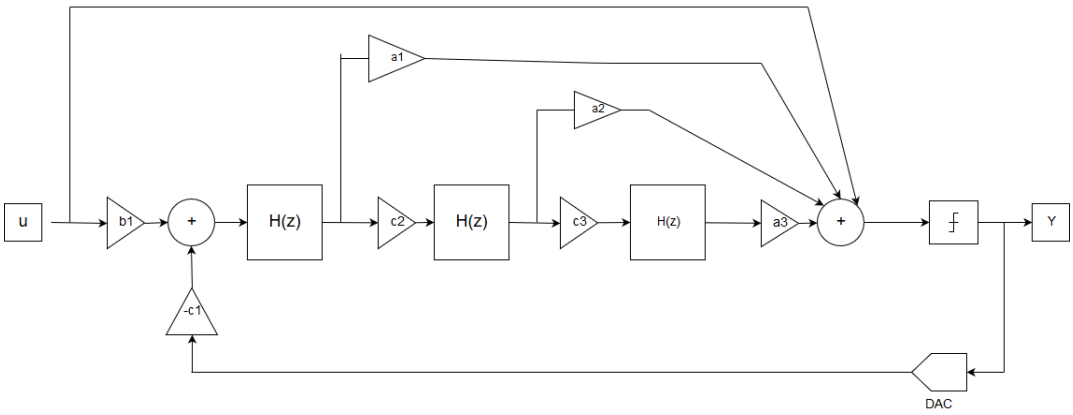


Figure 3.4: 3^{rd} order feedforward topology with input signal forwarded to summation node

leads to lesser swings and scaling, which means that the op-amp requirement can be relaxed, which leads to less power consumption. However one should be aware of operating on input amplitude near the reference voltage (V_{ref}), as this will drive the modulator to instability. The feedforward topology can further be improved by having a feedfoward path from input signal to the summation node in front of the quantizer, as shown in Fig. 3.4. This means that the integrators do not process the input signal, only quantization noise U, and this leads to low distortion[1, Ch.4.4.2], further relaxing the requirement for the integrator's op-amp. One thing to notice is that having fewer internal feedback DACs reduce the power dissipation significantly.

3.3 Time-Domain

The ΔΣ modulator can operate in a discrete-time domain (DT) or in the continuous-time domain(CT)[1]. We have already seen how DT modulator operates in chapter 2. Figure 3.5 illustrates a simple first order continuous time (CT) ΔΣ modulator. Unlike the DT ΔΣ modulator, the input signal and the integrator are continuous and the sampling occurs only before quantization. The STF and NTF for CT modulators has the same as the DT one.

The main difference, is the way they are implemented. The DT ΔΣ modulators employ switched-capacitor (SC) integrators while CT systems use active-RC integrators in the modulators. To choose the right domain for a application, one has to look at the advantages and disadvantages of associated with each option.

Switched-capacitor has the perk of taking advantages on fine-line very large scale of integration (VLSI) capabilities by eliminating the need to use physical resistors. Furthermore capacitors have high linearity, which is difficult to achieve with on-chip resistors in a standard CMOS process. In addition, the resistors in CT integrators can not afford to get too big as it can affect the thermal noise by increasing it, but having small resistors can increase the feedback capacitors, if one want to preserve the same settling time.

The accuracy of SC integrators is good, since the matching between capacitors are much better than matching between capacitor and resistors. Hence, the accuracy of the CT integrators will be inferior to SC integrators[1, Ch.6.6]. Another advantage is that the SC systems is less sensitive to clock jitter.

The CT modulators is attractive to high-speed applications as it can achieve very high OSR and is four times faster than DT modulators[1]. The DT modulators are limited by the achievable bandwidth of the opamps. Instead of having AAF outside the modulator as the DT modulator, the CT modulator has implicit AAF, since the sampling happens outside the loop-filter which is low-pass. The elimination of this filter can lead to power savings for the receiver.

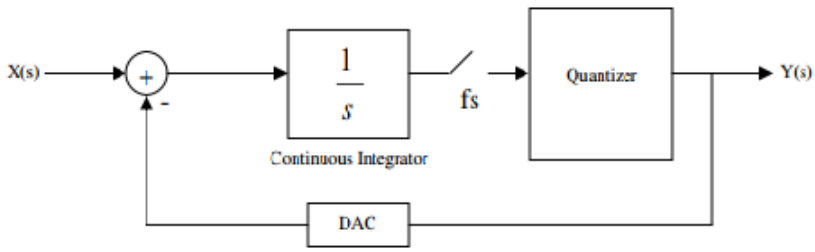


Figure 3.5: Linear model of CT first order ΔΣ modulator

3.4 Single-Bit vs Multi-Bit Quantizer

For a full-scale, the quantization error is reduced by 6dB for every bit added to the resolution of the quantizer[1, Ch.6]. Meaning that the SQNR will increase with this amount leading to a more stable operation. This is especially good for modulators of high order. Also the feedback loop becomes more linear, consequently allowing us to choose NTF more aggressively. Hence even better SQNR can be obtained, and larger input signals can be used. This and more advantages makes multi-bit quantizer attractive to use. However the errors introduced by DACs are not attenuated as quantization errors. Since the DAC's output goes to the input signal, the errors will get injected with the signal. As the linearity of the modulator is deepened on the linearity of the DAC. Multi-bit quantizer struggles with being linear, and need costly corrections techniques to keep up with the high linearity demand. This is not a problem for single-bit quantizer, since the DAC is inherently linear.

Another advantage with multi-bit quantizer is that it does not require large OSR as single-bit. Meaning the requirement for the bandwidth of a opamp can be relaxed. However adding more bits leads to a bigger power dissipation, making single-bit quantizer more attractive for applications that demand low power.

3.5 Choosing Architecture

The requirement of the modulator is to achieve 16-bit resolution. Three things were considered in choosing the right architecture: area, power and requirement for the system. The final architecture that was selected was a discrete-time third-order single-bit single-loop feedforward architecture with the input forwarded into the summation node, as shown in Fig. 3.4.

The choice of modulator order was between second and third order, which both satisfied the specification with OSRs: 256 and 128 respectively. As the mentioned in section 3.1, the high OSR of second order can cause the ratio between the sampling frequency and the bandwidth to become large. Furthermore, the high OSR also leads to stricter requirement

for the opamp. The third order modulator takes bigger area and has stricter stability requirement, but having a relax requirement seemed more desirable. However the OSR was chosen to be 170, as we want the theoretical SQNR to be 10-20dB more than the desired SNR in order to allow degradation in SQNR due circuits non-idealities and leave as much of the noise budget for thermal noise[1, Ch.9.2].

The feedforward topology was chosen because it gives the best SNR_{peak}. Moreover implementing feedback means that the power dispassion gets significantly larger, since the DAC's output is connected to the output of the integrators. One thing to remember is to have input amplitude a few dB under V_{ref}. Since V_{ref} was chosen to be 1V, the input amplitude was chosen to be 0.5.

Finally, DT-time single-bit architecture is the most suitable for the application, since it is easier to implement an SC integrator, and it is the best option considering noise budget and power savings. Also, with the superior linearity that follows with single-bit architecture, makes it more desirable to implement considering the cost in power and complexity it will take to reach stability. The specifications for the modulator have been summarized in table 3.1.

Table 3.1: Specification of modulator

Parameter	Value
Resolution	16
Fs	10MHz
OSR	170
Vdd	1.8V
V_{ref}	1V
Input amplitude	0.5
Order	3
Topology	Feed forward
Domain	DT
Quantizer level	2

3.6 Selection of OTA Topology

There are many architecture to choose from when designing a OTA, and they can be classified into two categories: single-stage and two-stage OTAs. In the single-stage category there are especially two architectures which are common to choose for low voltage/power operation: telescopic cascode and folded cascode. The conventional two-stage OTA is the miller configuration which commonly needs a class AB stage to enhance its speed [16],[24]. Table 3.2 compare the three OTAs in terms of power consummation, output-swing and speed.

Table 3.2: Comparison between folded, telescopic and two-stage amplifiers[6]

Topology	Power Consumption	Output Swing	Speed
Folded Cascode	Medium	Medium	Medium
Telescopic Cascode	Low	Low	High
Two-stage	High	High	Low

The two-stage amplifier has high power consumption due to the compensation capacitors which inevitably end up consuming a considerable amount of current. Single-stage amplifiers offers good self compensation, thus they do not need extra capacitors resulting in lower power consumption. Moreover it has a lower dominant pole than single-stage amplifiers, hence it is difficult to use in high frequency applications. Keeping all these aspects in mind, the single-stage amplifiers were chosen to be analyzed more.

The selection between folded cascode and telescopic cascode (shown in figures 3.7 and 3.6 respectively) depend on the performance requirements. The topologies have somewhat similar characteristics with both having gain in medium ranges. Note that the folded cascode has higher voltage output-swing than the telescopic cascode due to less number of transistors stacked in the output branch of the folded cascode. However higher voltage swings means higher power consumption, lower voltage gain, lower pole frequencies and higher noise. Another advantage with folded cascode compared to telescopic cascode is

that the input and output can be short together, and thereby relax the requirement of input common mode range (*ICMR*). Since the gain requirement were low and the voltage output swing was high as seen in table 4.6, the folded cascode was chosen to be the most suitable among the two architectures. Nonetheless a fully differential output was chosen.

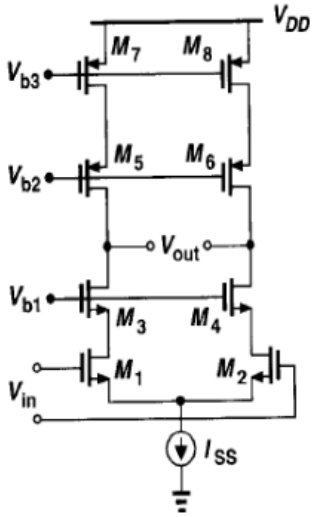


Figure 3.6: Telescopic OTA[6]

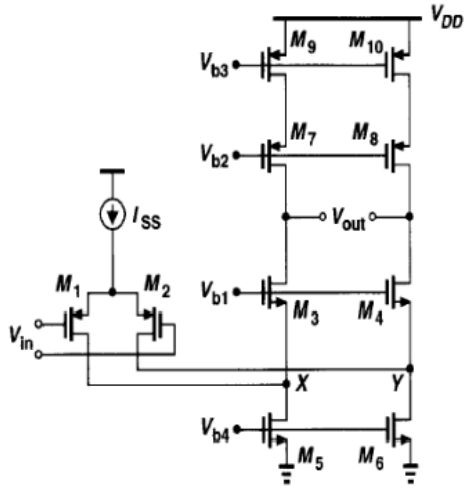


Figure 3.7: Folded cascode[6]

3.7 Single Ended vs Fully Differential Output

In practice, fully differential output is used because it has many advantages over single ended [5]. Some being:

- **Larger voltage output swing**: since the fully differential has twice as many output as the single ended one, the voltage output swing is almost double in magnitude.
- **Higher SNR**: Since the voltage output swing is large we get a higher signal-to-noise ratio (SNR). The signal output power becomes four times bigger because of twice the output voltage, also the noise power is doubled. Hence we get a overall 3dB improvement in SNR or 0.5 bit improvement in effective number of bits (ENOB).

- **Better noise rejection**: It is less susceptibility to common mode noise.

One important thing to note with fully differential circuits is that they need additional circuit to keep the output common mode level stable i.e. a common mode feedback circuit is needed, which we will discuss later. This additional circuit causes larger area and higher power consumption compared to single ended topology[4].

Chapter 4

Specification of the Design

In the feasibility study a set of specifications were obtained using behavioural modeling. In this chapter a small discussion of the results will be presented with additional specifications needed to implement the circuit design.

The specifications can be divided into two categories as listed below.

- **Requirements for the integrators**: The requirement for the total noise was derived in the feasibility study to find the optimal size for the capacitors used by the integrators and the summing node. In the feasibility study it was found that matching requirements were needed, and with parameters given by *Microchip* [22], we could calculate realizable capacitors values. In this thesis the matching requirements are the same, but the parameters are different, thus giving us a new set of capacitors values. The switch's on resistance were found after an exhaustive iteration of simulation.
- **Requirements for the Amplifier**: After an exhaustive iteration of simulation, the specifications for the finite DC gain, GBW and slew rate were found. The output-swing and the load capacitance seen from each output of the OTAs are also presented here.

4.1 Sizing of Capacitors

The proposed architecture was a discrete-time third-order single-bit single-loop feedforward ΔΣ modulator, as shown in figure 3.4. The transfer function for the non-inverting integrators is given by,

$$H(z) = \frac{C_s}{C_i} \cdot \frac{z^{-1}}{1 - z^{-1}} \tag{4.1}$$

where C_s is the sampling capacitor and C_i is the integrating capacitor. The coefficients b_1, c_2 and c_3 describe the relationship between these capacitors for integrator 1, 2 and 3 respectively. For instance the capacitors' relationship of integrator 1 can be described by

$$b_1 = \frac{C_s}{C_i} \tag{4.2}$$

The feedforward coefficients a_1, a_2 and a_3 describe the parallel network of capacitors in the summation circuit shown in appendix B.3.

The coefficients found in the feasibility study are given in table 4.1.

Table 4.1: Coefficients

Coefficients	
b_1	0.32
c_2	0.69
c_3	0.16
a_1	2.56
a_2	1.32
a_3	1.27

The matching requirements is given in table 4.2.

Table 4.2: Matching requirement

Coefficients	Matching
a_1	$\pm 4\%$
a_2	$\pm 4\%$
a_3	$\pm 4\%$
c_2	$\pm 2\%$
c_3	$\pm 1\%$

Using the coefficients with the matching requirements and parameters given by *Microchip*, the final values can be computed. The capacitors that realize a_1, a_2 and a_3 are matched to the same reference (the feed-forward capacitor). Thus, the realization of the coefficients is summarized in table 4.3.

Table 4.3: Realizable coefficients

Coefficients	Ideal value	Fractional value	Cap realization
b1	0.32	542/1779	2.05p/6.58p
a1	2.56	64/25	236.8fF/92.5fF
a2	1.32	33/25	122.1fF/92.5fF
a3	1.27	32/25	118.4fF/92.5fF
c2	0.69	7/10	76fF/106.4fF
c3	0.16	3/19	45.6fF/288.8fF

4.2 Switches' On-Resistance

The size of the switches' on-resistance have to be specified to estimate the cost of implementing it on transistor-level. Having small on-resistance will lead to bigger area usage, and it will therefore be costly to implement. The goal in the feasibility study was to find the largest on-resistance for the integrators that will give the desired performance. The final values are summarized in table 4.4.

Table 4.4: Final specification for the switches' on-resistance

Specifications	Integrator 1	Integrator 2	Integrator 3	Summing node	
Ron	0.9	1.5	1.6	1.7	$k\Omega$

4.3 Finite DC-Gain

Finite DC-gain will give integrator leakage, which can in general be expressed as:

$$H(z) = \frac{1}{z-\alpha}, \alpha = 1 - \frac{1}{A_0} \tag{4.3}$$

This means the integrator has a DC-gain limited by opamp's open-loop gain, which again means that the DC-attenuation of the NTF is also limited. In general the cascade of opamps' gains much be much higher than the desired NTF DC-attenuation, or in other words higher than the resolution. The effect of limiting gain is shown in Fig. 4.1. As seen the third order modulator has small open-loop gain, raging from 35dB to 45dB. The reason being all the NTF's zeroes will be in DC. Therefore the cascade of open-loop gains of the integrators are sufficient enough to give the desirable performance. Another advantage of having small gains is that the specifications for gain for each OTA are relaxed, thus one can easily achieve the requirement with a one stage OTA.

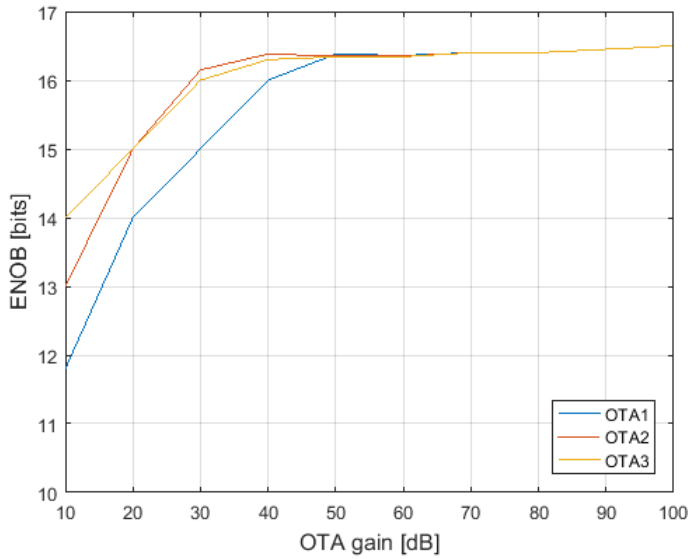


Figure 4.1: ENOB limitation due to finite open

4.4 Output swing

In Fig. 4.2 we see the output swing of integrator 1, 2 and 3. We have that for integrator 1 and 2 the output swings from 0.6 to 1.2, while for integrator 3 it swings from 0.7 to 1. This gives us voltage change ($\Delta V_{1,2}$) of 0.6 for integrator 1 and 2, and ΔV_3 of 0.3 for integrator 3. It is worth mentioning that when the output voltage is closer to limits, the response is distorted.

4.5 Gain-Bandwidth Product and Slew-Rate

Finite gain-bandwidth (GBW) of the OTA will lead to incomplete linear settling as the output will not settle to its final value. This will cause the ENOB to degrade, therefore we need to find sufficient GBW to achieve the desired ENOB. The degradation of ENOB with falling GBW is shown in figure 4.3. It was found that the minimal GBW should be between 28MHz and 38MHz. If we choose smaller GBW, the performance will degrade

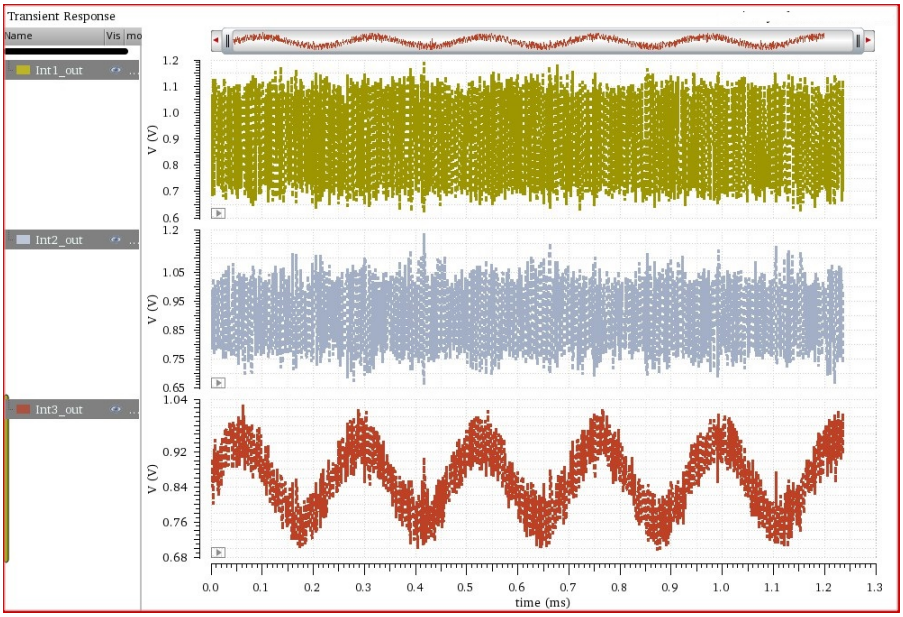


Figure 4.2: Output swing of integrator 1, 2 and 3

rapidly which makes this specification one of the most critical.

Unlike GBW, slewing causes non-linear settling error which degrade the ADCs linearity. The slew-rate must be high enough to avoid slewing to cause non-linear settling error. Meaning it must be high enough to settle the output in $\frac{T_s}{2}$, where T_s is the sampling period. This gives us the requirement for minimum slew-rate:

$$\frac{\Delta V}{SR} > \frac{T_s}{2} \tag{4.4}$$

where ΔV is the output change of the integrator. We have from section 4.4, that the output change is 0.6 for integrator 1,2 and 0.3 for integrator 3. By performing transient analysis we found out the slew-rates given by equation 4.4 are not sufficient. An exhaustive simulation process was launched, and the final values are listed in table 4.5 with the calculated.

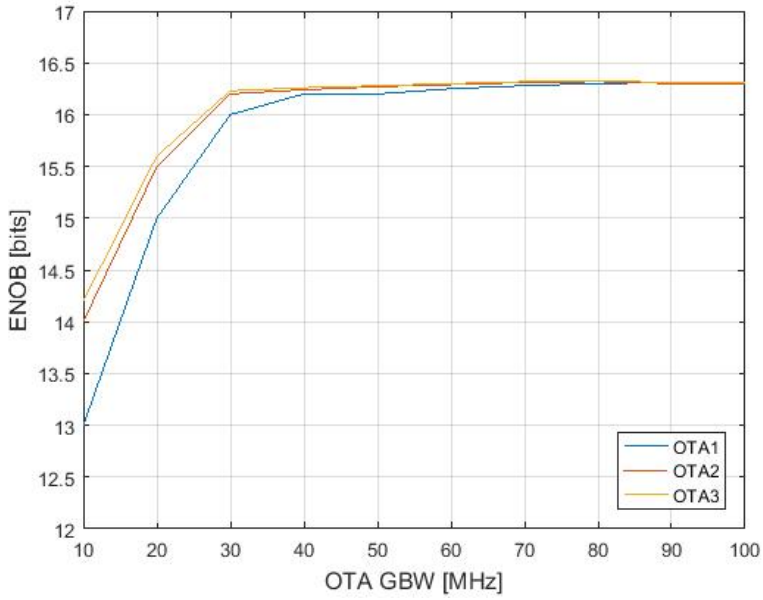


Figure 4.3: ENOB limitation due to GBW

Table 4.5: Theoretical and Simulated Values of SR

Integrator	Calculated	Simulated
1	12MV/sec	28MV/sec
2	12MV/sec	28MV/sec
3	6MV/sec	28MV/sec

4.6 Load Capacitance

To be able to design the OTAs correctly so that they function properly in the whole system, we need to find the load capacitance they see at their output. Using method introduced in [13], we can estimate what the load capacitance for each OTA will be. As an example we can compute for the first OTA. We have that:

$$C_{L1} = C_{s1}||C_{i1} + C_{s2} + C_{ff1} + 0.2\dot{(}C_{i1} + C_{s2} + C_{ff1}) \approx 3.5p \tag{4.5}$$

where C_{s1}, C_{i1} and C_{ff1} are the sampling, integrating and feedforward capacitor of the first integrator. Same way we can find the load capacitance for second and third OTA, and they are $0.6p$ and $0.3p$ respectively.

4.7 Specifications of the Amplifier

Table 4.6 summarize the requirements for the amplifiers of integrator 1, 2 and 3. It has also been included a specification for phase margin. It has been chosen to be greater than 60°, because it guarantee stability and allows for the fastest settling time when attempting to follow a voltage step input [19].

Table 4.6: Specifications of the Amplifiers

Parameter	OTA1	OTA2	OTA3
A_O	>45dB	>35dB	>35dB
GBW	>38MHz	>30MHz	>28MHz
SR	>28MV/sec	>28MV/sec	>28MV/sec
Output Swing [V]	0.6<Vout1<1.2	0.6<Vout2<1.2	0.7<Vout3<1
Phase Margin	>60°	>60°	>60°
Load Capacitance	3.5p	0.6p	0.3p

4.8 Impact of Nonidealities

The non-ideal model of the modulator was simulated using the first three specifications given by table 4.6, and the capacitance summarized in table 4.3. The output spectra is shown in figure 4.4, where the SNR and ENOB values are also shown. It can be noted that the main objective of achieving ENOB of 16 bits was satisfied.

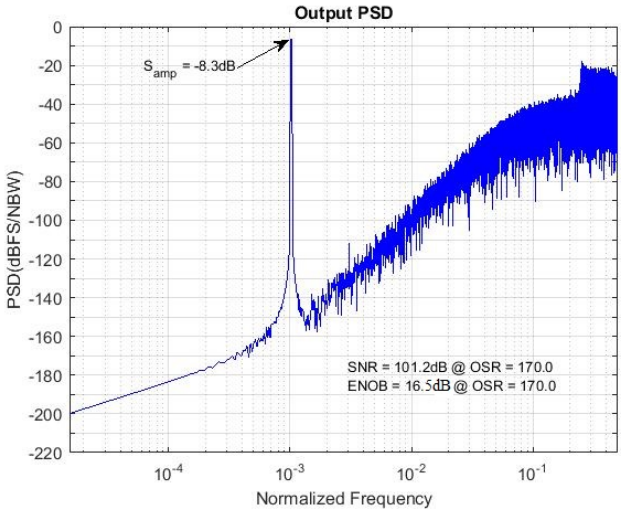


Figure 4.4: PSD of the output signal using non-ideal model

Chapter 5

Circuit Design

This chapter describe the design methodology of implementing analog blocks used in third order $\Delta\Sigma$ modulator, and also address the issues involving the design of the modulator. Moreover the procedure to obtain the final transistor dimensions were based on the gm/I_D methodology and on iterative simulations, since the equations used in the SPICE level 1 are not accurate.

5.1 Switches

Sampling switches is one of the most fundamentals analog blocks of ADC operating on discrete-time. An ideal switch is just short circuit when it is on and an open circuit when it is off. In other words when the switch is on there should be zero resistance, and when the switch is off there should be an infinity resistance. But as discussed in section 4.2, these values are not feasible. Therefore designing the switches with adequate on-resistances without degrading the performance is a crucial part in the design of integrated circuits (ICs).

The commonly used switch implementations are: a NMOS transistor, a PMOS transistor or a transmission gate (TG). The on-resistance of a MOSFET depends on the input signal,

as given in [4], and rewritten in expression 5.1:

$$R_{on} = \frac{1}{\mu C_{ox} \frac{W}{L} (V_{GS} - V_T)} \tag{5.1}$$

Where the mobility μ is different depending on if we look at NMOS or PMOS transistor. We have that the time-constant increases for more positive NMOS or negative PMOS inputs. Designing a switch with large enough input swing capability is a challenge in low-voltage application. The reason being that as the technology scales, the supply voltage scales down much faster than the threshold voltage of a transistor. For a NMOS the operation is restricted to a input swing lower than $V_{DD} - V_{thn}$, and for PMOS the swing must be greater than V_{thp}.

Transmission gate is a technique that can be used to accommodate greater swings [7]. It consists of a PMOS in parallel with a NMOS transistor as shown in Fig. 5.1. The disadvantage of such switch is to have extra circuit to implement the complementary clocks, but it is a small price to pay for an improvement as good as rail-to.rail swing across the switch.

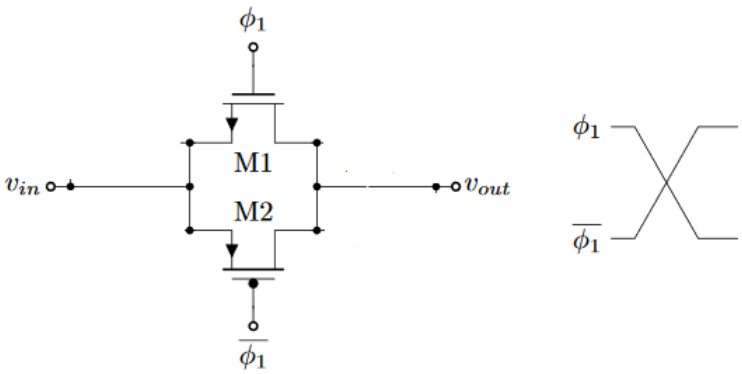


Figure 5.1: Circuit implementation of a TG switch

After choosing the topology for the switch, the dimensions of the transistors were found. Using equation 5.1 and Fig. 5.1 we get that: $V_{GS} = \phi_1 - v_{in}$, where ϕ_1 is $V_{DD} = 1.8V$ when it is on and 0V when it is off. After completing a simulation it was found out that the on-

resistance for the resistors were too high. We cannot change the swing of the input voltage V_{in}, since it is given by the system. The options were either to increase the dimension $\frac{W}{L}$ or increase the gate voltage ϕ when it is high. Since we want to keep the dimensions as small as possible, we increased the gate voltage. In order to increase the supply voltage V_{DD} a charge pump was used [9]. It is a Dc-to-Dc converter that can take a a DC source from one level to another. In our case it was found out that doubling V_{DD} was sufficient enough to get the on-resistance in the range we wanted. The charge pump was not implemented on circuit level, instead an ideal DC source was used to mimic the behaviour of the charge pump. Finally we used a level-shifter [11] to translate signals from one voltage domain to another, namely $[0, V_{DD}]$ to $[0, 2V_{DD}]$.

The switches were chosen to have minimum dimensions. Moreover the PMOS transistors were chosen to be three times bigger than the NMOS transistors to account for lower mobility. The final dimensions for the switches of integrator 1 are listed in table 5.1 and for integrator 2,3 and the sum block in tables A.1, A.2 and A.3 respectively in appendix A. Compared with table 4.2 we see that the on-resistance of the switches of the integrators approximately meets the specifications. It does not matter if the on-resistances varies with a couple of Ωs since it only affect the performance to a small degree. The same justifications apply for the other analog blocks.

Table 5.1: Switch transistors' dimensions and resistances of integrator 1

Switch	PMOS(W/L)μm	NMOS(W/L)μm	$R_{ON}(\Omega)$
I23	13.5/0.55	4.5/0.55	904.9
I9	14.7/0.55	4.9/0.55	907.2
I18	13.2/0.55	4.4/0.55	892.2
I20	11.7/0.55	3.9/0.55	903.8

5.2 Operational Tranceconductance Amplifier

Operational tranceconductance amplifier (OTA) is the most important component of integrators in the $\Delta\Sigma$ modulator. Its specifications determine the performance of the integrator,

thus of the whole modulator. The design procedure to meet the specifications given by table 4.6 will be discussed in the subsequent sections.

5.2.1 Design Procedure of OTA

The selected folded cascode architecture is illustrated in Fig. 5.2, and it shows the currents flowing through the different branches. The input pairs is PMOS differential pair. The flicker noise is less in a PMOS transistor, since its mobility is lower than of NMOS transistor[5]. From the slew-rate and load capacitance (C_L) values listed in table 4.6, the bias current I_1 can be determined:

$$I_1 \geq SR * C_L \tag{5.2}$$

As a rule of thumb, the load current I_2 should be in the range to keep all the transistors in saturation[6]:

$$1.2I_1 < I_2 < 2I_1 \tag{5.3}$$

Thus making I_3 equal to:

$$I_3 = \frac{I_1}{2} + I_2 \tag{5.4}$$

Tranceconductance of the circuit is given by GBW and C_L as follows:

$$gm_1 = GBW \cdot 2\pi \cdot C_L \tag{5.5}$$

The resulting bias currents and the tranceconductance of the circuit of OTA 1, 2 and 3 are listed in 5.2. These parameters can be used with the g_m/I_D methodology to find the dimensions of the input transistors M_1 and M_2, as it will be described in the next section.

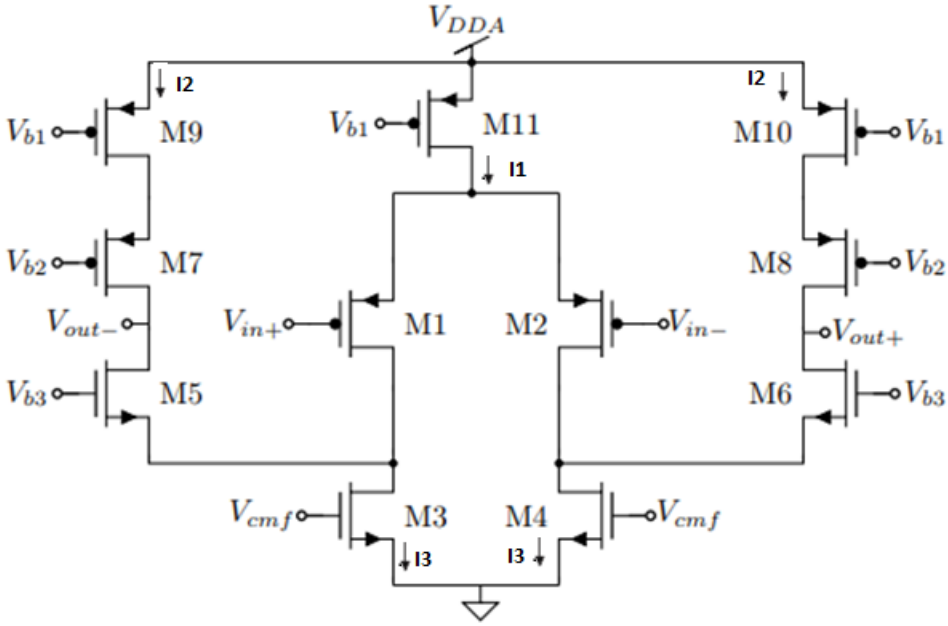


Figure 5.2: Folded cascode architecture with the current I_1, I_2 and I_3 flowing in different branches [23]

5.2.2 Obtaining Transistor Dimensions Using g_m/I_D Methodology

Using the design flow depicted in Fig.5.3, the procedure to find the dimensions of the transistors can be explained. The g_m and I_D is the tranceconductance and the drain current through a transistor respectively.

Table 5.2: The tranceconductance and bias current of OTA 1, 2 and 3

OTA	$gm_1[\mu S]$	$I_1[\mu A]$
1	0.85	100
2	0.15	20
3	0.06	10

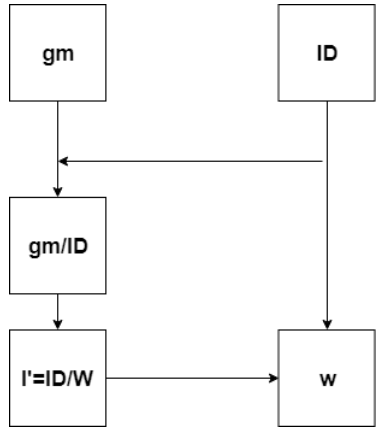


Figure 5.3: Design flow

First step in the device characterization is to generate the plot of g_m/I_D vs I_D/W. Fig. 5.4 shows a PMOS setup in cadence which is used to generate the plot. In a similar manner a NMOS transistor is setup to obtain the same plot. For this simulation transistor dimensions of $\frac{W}{L} = \frac{5\mu}{0.7\mu}$ is chosen. A comparison between the values of PMOS and NMOS transistors is shown in Fig. 5.5.

For illustrative purpose we will find the dimensions of transistor M_1 of OTA 1 and use the design flow in Fig. 5.3 to get an insight on how the g_m/I_D method works. From table 5.2 we have that the $gm_1 = 0.85\mu S$ and the drain current through the transistor is given by:

$$I_{M1} = \frac{I_1}{2} = 50\mu A \tag{5.6}$$

which gives us:

$$gm_1/I_{M1} = 17 \tag{5.7}$$

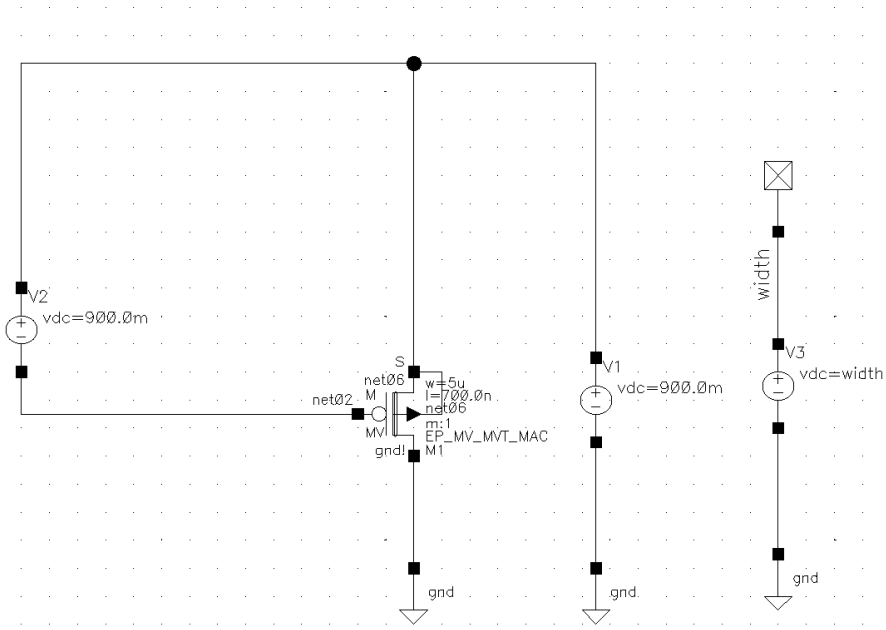


Figure 5.4: Schematic of the PMOS transistor setup in cadence

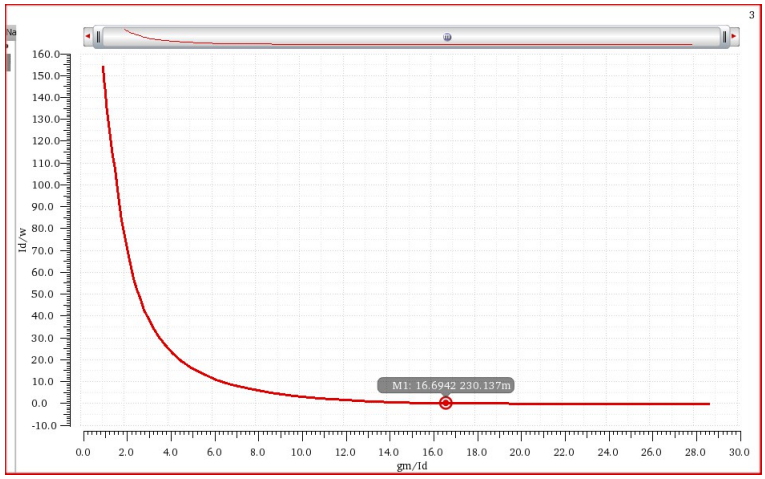
We then uses g_m/I_D vs I_D/W plot from Fig. 5.5a to obtain the value $I_D/W = 230.137mm$ which corresponds to the g_m/I_D value obtained in equation 5.7. The final width of the transistor is:

$$W = \frac{I_D}{I_D/W} = 217\mu m \tag{5.8}$$

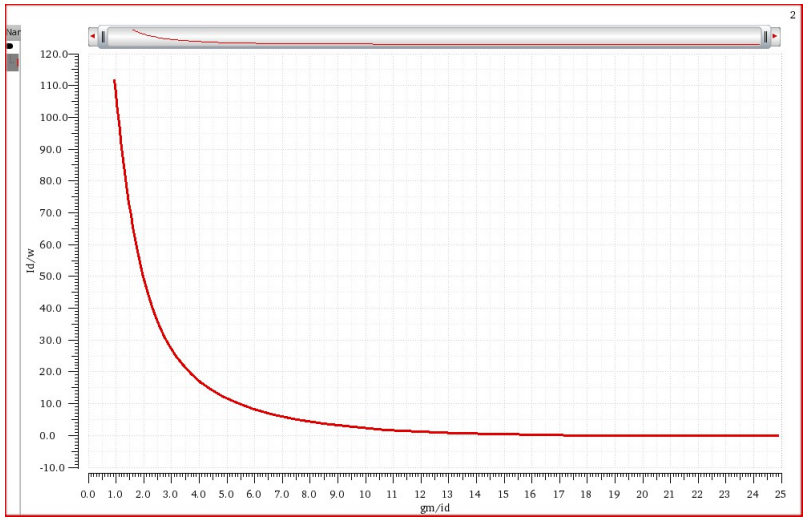
with the length to the transistor equal to $L = 0.7\mu$, we get:

$$\frac{W}{L} = \frac{217\mu}{0.7\mu} \tag{5.9}$$

As we will see in the table 5.3, this method gives us good accuracy of the desired values needed to satisfy the specifications of the application.



(a) PMOS



(b) NMOS

Figure 5.5: Comparison of PMOS and NMOS transistors for g_m/I_D vs I_D/W

5.2.3 Final Dimensions of the Transistors

The dimensions for the input transistors of OTA 2 and 3 can be found in a similar manner as it was done for OTA 1 by using table 5.2, but for transistors $M_3 - M_{11}$ we need to additionally look at the output-swing specification given i table 4.6 for the different OTAs. For folded cascode we have a maximum output voltage swing requirement given by[6]:

$$VO_{max} = V_{DDA} - (V_{OD7} + V_{OD9}) \tag{5.10}$$

$$VO_{min} = V_{OD3} + V_{OD5} \tag{5.11}$$

Where VO_{max} is the upper end and VO_{min} is the lower end of the swing. V_{OD} is the overdrive voltage which define the region the transistor operate in, and is given by the gate voltage and threshold voltage of the transistor:

$$V_{OD} = V_{GS} - V_{th} \tag{5.12}$$

Since V_{GS} depends on the bias voltage V_b we can freely choose which region a transistor will operate in. Transistors in strong inversion has poor current efficiency and low output range, but it is small and the transient frequency is high. Transistors in weak inversion on the other hand has good current efficiency and high output voltage range, but at the cost of a larger transistor and low transient frequency. Moderate inversion is a good compromise between these two regions [25]. The goal was to size the transistor to operate as close as possible in this region, thus having good output voltage range while maintaining small area.

The next step is to use g_m/I_D method to find dimensions for the transistors. The drain current through each transistor can be find using equations: 5.2, 5.3 and 5.4. The transconductance (g_m) of the transistors can be expressed with the help of V_{OD} as follows:

$$gm = \sqrt{2I_D C_{ox} \frac{W}{L}} = \frac{2I_D}{V_{OD}} \tag{5.13}$$

With the right choice of V_{OD} we can compute the g_m/I_D for a transistor that operate in the moderate inversion region. Then we can use the value of g_m/I_D with the plot in Fig. 5.5a or 5.5b (depending on if we look at PMOS or NMOS transistor) to find the dimension of the transistor, as it was done for transistor M_1. This procedure was used as a starting point for sizing the transistors. The final dimensions for the three OTAs were set by using PVT simulations and are summarized in table 5.3. The design accomplished the requirements mentioned in table 4.6, as it will be seen in chapter 6.

Table 5.3: Transistor dimensions of OTA 1, 2 and 3

Device	OTA_1		OTA_2		OTA_3	
	W[μm]	L[μm]	W[μm]	L[μm]	W[μm]	L[μm]
M_1	217	0.7	180	0.7	163	0.7
M_2	217	0.7	180	0.7	163	0.7
M_3	126	1	97	1	81	1
M_4	126	1	97	1	81	1
M_5	23	0.7	35	0.7	25	0.7
M_6	23	0.7	35	0.7	25	0.7
M_7	87	0.7	70	0.7	52	0.7
M_8	87	0.7	70	0.7	52	0.7
M_9	56	1	43	1	40	1
M_{10}	56	1	43	1	40	1
M_{11}	98	1	77	1	66	1

5.2.4 Bias Circuit

The points V_{b1}, V_{b2} and V_{b3} in Fig. 5.2 are the DC voltages used to bias the transistors, while V_{cmf} controls the common output mode of the OTA. Figure 5.6 shows a wide swing current mirror [4] which is used to generate the necessary bias voltages in the cascode

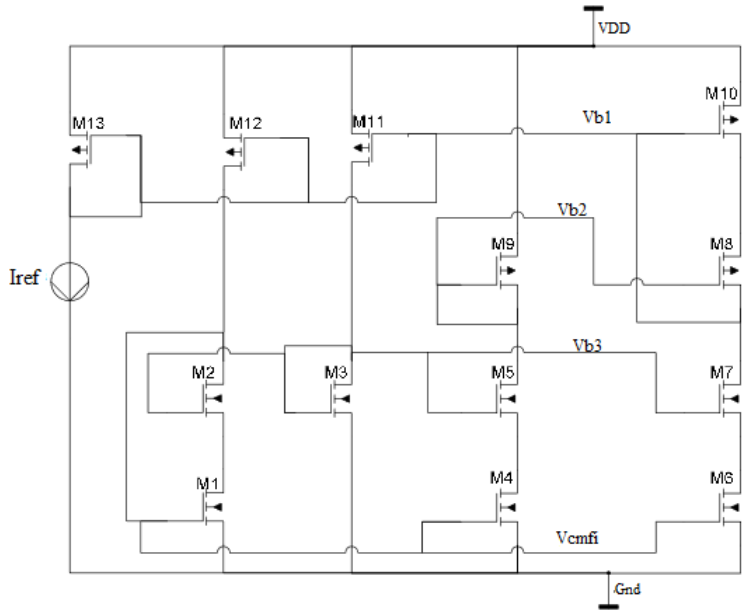


Figure 5.6: Wide swing current mirror

pair. A wide swing current mirror topology has the perks of not limiting the signal swing as much as the other conventional current mirrors. It also provides a better matching of the currents and higher output resistance. To get a lower power consumption the reference current I_{ref} is set to $10\mu A$, $2\mu A$ and $1\mu A$ for OTA 1, 2 and 3 respectively. With such low currents, especially for OTA 2 and 3, large amounts of noise are generated. This will not be a problem for our ADC, since the noise will be considerably attenuated for OTA 2 and 3. The transistors $M_1 - M_3$ and $M_{11} - M_{13}$ are made ten times smaller than the transistors in the cascode of the OTAs. While the dimensions of the transistors $M_4 - M_{10}$ are the same as the one used in the cascode to make sure that the bias currents listed in table 5.2 are properly mirrored into the OTAs. Transistors M_3 and M_9 are made four times smaller than transistors M_2 and M_8 respectively to ensure proper generation of the bias voltages[5]. The gate length of the transistors are made to be approximately two times longer than the allowable minimum length to get better matching during layout. Table 5.4 summarize the

transistors dimensions of the circuit for OTA 1, 2 and 3.

Table 5.4: Transistor dimensions of the OTAs bias circuits

Transistor	OTA_1		OTA_2		OTA_3	
	W[μm]	L[μm]	W[μm]	L[μm]	W[μm]	L[μm]
M_1	12.6	1	9.7	1	8.1	1
M_2	3.3	1	5.6	1	3.6	1
M_3	0.82	1	1.4	1	0.9	1
M_4	126	1	97	1	81	1
M_5	32.8	1	56	1	35.7	1
M_6	126	1	97	1	81	1
M_7	32.8	1	56	1	35.7	1
M_8	124.3	1	100	1	74.3	1
M_9	31.1	1	25	1	18.6	1
M_{10}	98	1	77	1	66	1
M_{11}	9.8	1	7.7	1	6.6	1
M_{12}	9.8	1	7.7	1	6.6	1
M_{13}	9.8	1	7.7	1	6.6	1

5.2.5 Common Mode Feedback Block

As mentioned one of the biggest disadvantage of a fully differential OTAs is that; if the common mode output is not controlled it can either go to positive or negative rail and thereby drive some transistors out of the saturation/active region. Hence an additional circuit is required to keep the common mode output stable. Figure 5.7 shows a switched capacitor common mode feedback block which is a simple circuit used generally in discrete-time circuit. The circuit produce the output common mode voltage by comparing the average of the differential output voltages with the desired common mode voltage. Then the difference between these two voltage (V_{cmf}) is used to bring the OTA's common mode voltage back to the desired common mode level. Since the stability of the OTA gets changed when introducing extra capacitors at the output, capacitor C_1 and C_2 has to be chosen with care. The values were determined by simulation, as a rule of thumb capacitor C_2 should be five times larger than C_1[5]. Table 5.5 list up the capacitance values for OTA 1, 2 and 3.

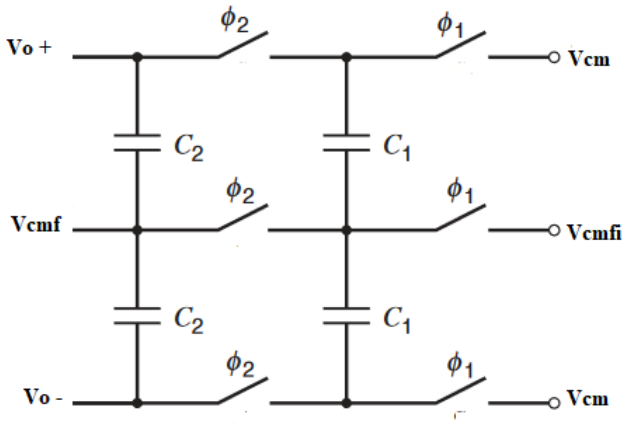


Figure 5.7: Switched capacitor CMFB circuit[23]

Table 5.5: CMFB capacitance values

Capacitor	OTA_1	OTA_2	OTA_3
$C_1[pF]$	1	1.35	2.1
$C_2[pF]$	0.2	0.27	0.42

5.3 Quantizer

The quantizer in a $\Delta\Sigma$ ADC has to work at a high oversampling frequency, but its resolution is 1-bit. Therefore we have chosen to implement a latched comparator[28] shown in Fig. 5.8 that focus more on high-speed operation than accuracy. The comparator is clocked in order to synchronize its operation with other circuits in the ADC. The main parameter of concern was hysteresis, since the input offset and input referred noise get attenuated by the feedback loop of the modulator.

The input M_1 and M_4 are the discharge controlling transistors which are connected to the flip-flop M_2 and M_3 in a feedback network. M_5 and M_6 are control transistors which keep track of holding the comparator synchronized with the rest of the ADC. M_8 and M_9 are another flip-flop connected in feedback with transistors M_7 and M_{10}, which are precharge transistors used for refreshing the internal nodes when they are not in operation, to reduce hysteresis. Inverters M_{11-12} and M_{13-14} act as buffers to isolate the latch from the output load and to amplify the comparator output.

When the *Clk* is low, transistors M_5 and M_6 gets cut off and the input signal will not influence the comparator. The voltages V_{io+} and V_{io-} will be pulled to the positive rail V_{DD}, and because of the inverters the output will be pulled to ground. At the same time the voltages V_a+ and V_a- gets discharged to ground by transistors M_1 and M_4. Suppose V_{in+} is greater than V_{in-}. When the *Clk* goes high, both voltages V_{io+} and V_{io-} drop from the positive rail and the voltages V_a+ and V_a- rise from the ground. However, M_1 draws more current than M_2, and thereby more current is flowing through M_3. This causes V_{a-} to rise faster than V_{a+}. Since more current flows through M_5 than M_6, the voltage V_{io+} drops faster than V_{io-}. The regenerative action of M_8 and M_9 together with that of M_2 and M_3

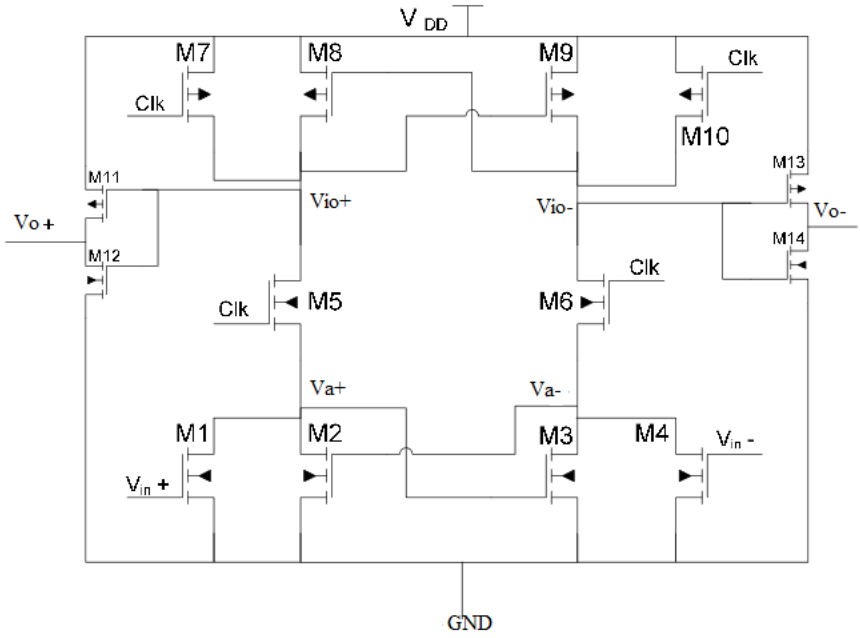


Figure 5.8: Latched comparator[28]

pulls V_{io+} to ground and pulls V_{io-} to positive rail. Hence, V_{0+} goes high while V_{0-} goes low. The operation is similar when V_{in-} is greater than V_{in+}.

The circuit has digital behaviour with the exception of transistors M_1 and M_4 that amplify the input signal. Hence, the transistors that operate as digital circuit have minimum dimensions, while the input transistors have a larger length to avoid mismatch effects. The transistor dimensions are listed up in table 5.6.

Table 5.6: Transistor dimensions of the latched comparator

Transistor	W[μm]	L[μm]
M_1	1	1
M_2	0.5	0.55
M_3	0.5	0.55
M_4	1	1
M_5	0.5	0.55
M_6	0.5	0.55
M_7	1	0.55
M_8	1	0.55
M_9	1	0.55
M_{10}	1	0.55
M_{11}	0.5	0.55
M_{12}	0.5	0.55
M_{13}	0.5	0.55
M_{14}	0.5	0.55

Finally, the output of the comparator is only valid in phase ϕ_1, and the output of the feedback DAC gets sampled on integrator 1 at phase ϕ_2. In order to keep the comparator output valid in both phases, a SR-latch is placed in front of the comparator. Since the circuit is purely digital, the dimensions are also here set to minimum. The SR-latch is shown in Fig. B.5 in appendix B.

5.4 Non-Overlapping Clock Generator

The implemented clock generator is a two-phase non-overlapping circuit. It was designed with the intention of maximize the time available, and make the early and late phases start at the same time, i.e. ϕ_1 and ϕ_{1d} start at the same time. The same apply for phases ϕ_2 and ϕ_{2d}. The generator consists of NAND-gates and inverters as shown in Fig. The

logic gates have minimum dimensions where the dimensions of the PMOS transistors is three times the NMOS ones. Further delayed clock can be produced by adding more delay inverters on the path from the outputs of the generator to the input of the NOR-gates. Since the switches are transmission gates, each phase needs a complementary singal for proper operation. Complementary signals $\overline{\phi_1}$, $\overline{\phi_{1d}}$, $\overline{\phi_2}$ and $\overline{\phi_{2d}}$ are realized by putting an inverter in front of the outputs of the generator.

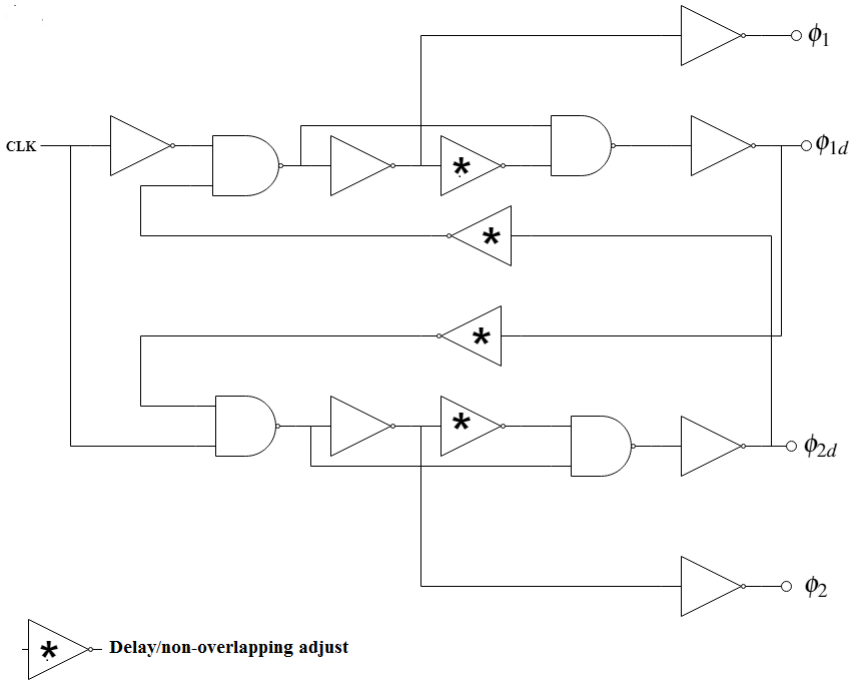


Figure 5.9: 1-bit DAC

5.5 DAC

The 1-bit DAC implemented is shown in Fig. 5.10, and the functionality is simple. For instance, depending on if the input signal dacp_1 is either high or low the feedback out back to integrator 1 is either vrefp or vrefn which is the reference voltages. Similarly the output vfbp depends on the level of input dacn_1. In a differential circuit, the reference voltages must be centered at the analog ground $V_{cm} = 0.9V$. Hence, they have to be imple-

mented so they are symmetric with respect to V_{cm} such that their difference is equal to V_{ref} (listed in table 3.1). The reference voltages are chosen to be ± 0.5 around V_{cm}. Therefore, vrefp is 1.4V and vrefn is 0.4V. The switches is implemented as TG switch with the dimensions of PMOS switch being $\frac{W}{L}_p = \frac{10.5}{0.55}\mu m$ and $\frac{W}{L}_n = \frac{3.5}{0.55}\mu m$, giving an on-resistance of 905.4Ω.

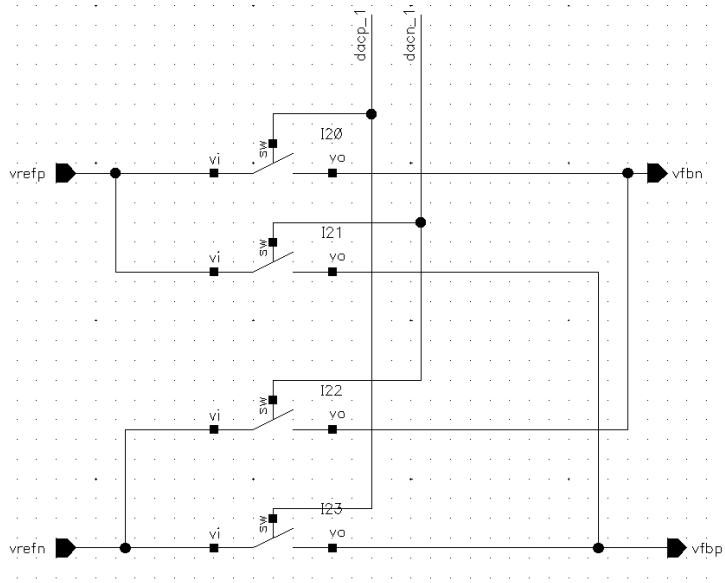


Figure 5.10: 1-bit DAC

Chapter 6

Results

The results for the analog blocks were obtained by using spectre simulator in Cadence Virtuoso ADE. In case of noise simulation a transient noise was imposed. The functionality and integrity of the modulator and the analog blocks were validated using Nominal simulation. Additionally PVT simulations were performed on the modulator,the OTAs,the quantizer and the clock generator in order to verify the robustness of these blocks. The nominal simulation operate with typical transistor model at room temperature and standard supply voltage. PVT simulation on the other hand operate with corner models of the the process where the range of the temperatures are between -40° and 105°, and 2.5 V and 5.5 V for the supply voltage. Furthermore it also consists of performing many simulations based on the statistical model of the transistors, namely 16. The corners model of the transistors provided by Microchip Technology are: slow, fast, slow-NMOS-fast-PMOS (SNFP) and fast-NMOS-slow-PMOS (FNSP).

6.1 Non-Overlapping Clock

The output signals from the designed non-overlapping clock generator is shown in Fig. 6.1. The non-overlapping time is 23.52nsec between ϕ_1 and ϕ_2, and ϕ_{1d} is delayed from ϕ_1 with 10nec, the same delay apply for ϕ_{2d} and ϕ_2. It should be noted that the delays are

not affected by mismatch effects and process variation.

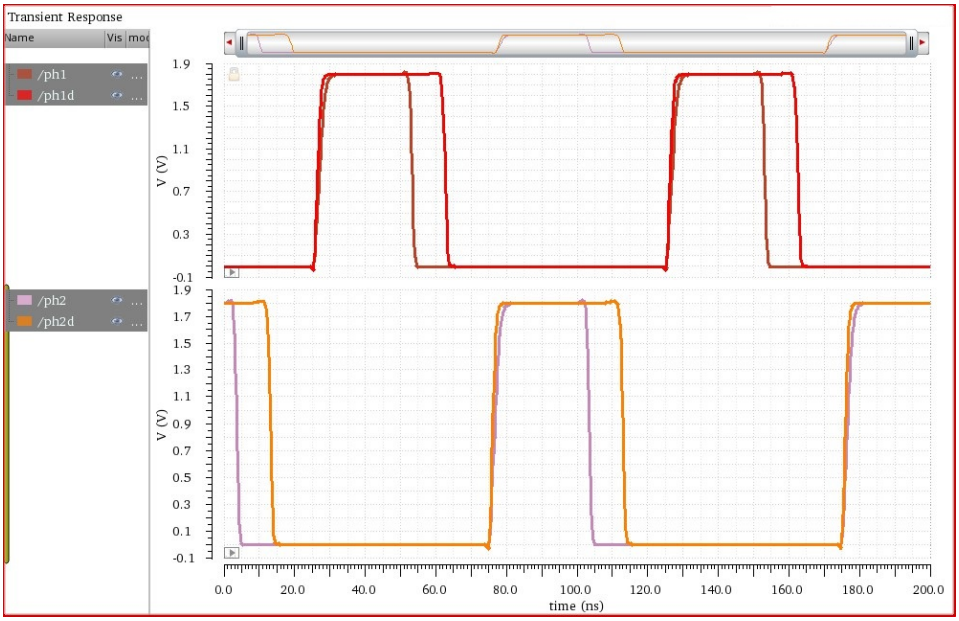


Figure 6.1: Clock phases

6.2 Quantizer

The quantizer used is simply a latched comparator which switches to the rail supply depending on the input signals. It is designed as per the methodology discussed earlier. The quantizer was simulated using three input signals: V_{in+}, V_{in-} and CLK. The positive and negative input voltages are signals that vary from ground to V_{DD} and from V_{DD} to ground respectively. The output only changes at the rising edge of the clock. As mentioned in the methodology the hysteresis parameter was used to validate the quantizer, since the input offset and the input referred noise get attenuated by the feedback loop of the modulator. Figure 6.2 shows when the output gets updated as the input voltages V_{in+} and V_{in-} vary. Due to the regenerative latch the hysteresis of the quantizer was measured as small as $5.86mV/V$. PVT simulations were performed with no corners being critical to the quantizer's performance.

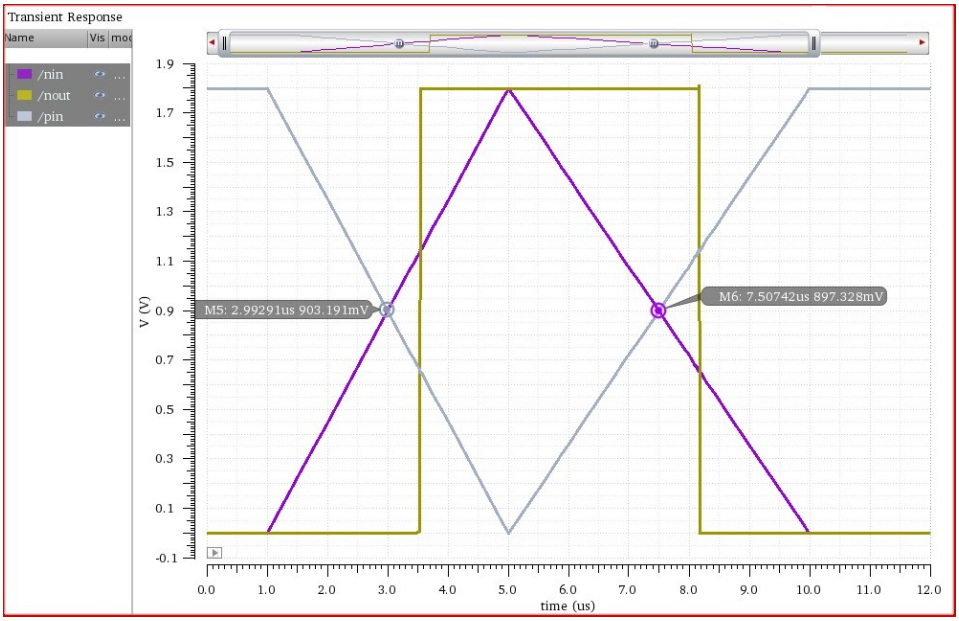


Figure 6.2: Hysteresis of the comparator

6.3 OTA

With the use of nominal and PVT simulation the specifications were validated. The results of the simulation are based on the set of requirements listed in table 4.6.

6.3.1 Nominal Simulations

The main results of the nominal simulations of OTA 1, 2 and 3 are listed in table 6.1, and frequency responses are depicted in Fig. 6.3. As discussed in chapter 3 the specifications of the OTAs are indeed relaxed, which made the design process that much easier. The DC-gain and GBW fulfill the specifications with good margin for all three OTAs. Even with the common mode feedback block which effect the stability, the phase margin of the three OTAs exceeds the requirements. Additionally the power consumption including the bias circuit were around 22.3 μW, 11.7μW and 8.5μW for OTA 1, 2 and 3 respectively. One thing to notice is that the power consumption of OTA 1 is greater than for OTA 2

Table 6.1: Nominal results from OTA 1, 2 and 3

Specification	OTA 1	OTA 2	OTA 3
DC gain	60dB	42dB	40dB
GBW	43.2MHz	36.7MHz	38.2MHz
Phase margin	75.6°	70°	78.4°
Power	22.3μW	11.7μW	8.5μW
Slew rate	42.12MV/sec	46.23MV/sec	47.76MV/sec
Maximum output voltage	1.15	1.2	1
Minimum output voltage	0.65	0.65	0.7

and 3 due to the slew rate requirement. Different topologies can be used to reduce the power consumption of OTA 1, such as an adaptive bias circuit [29]. It has the advantage of improving the power efficiency while achieving high slew rate.

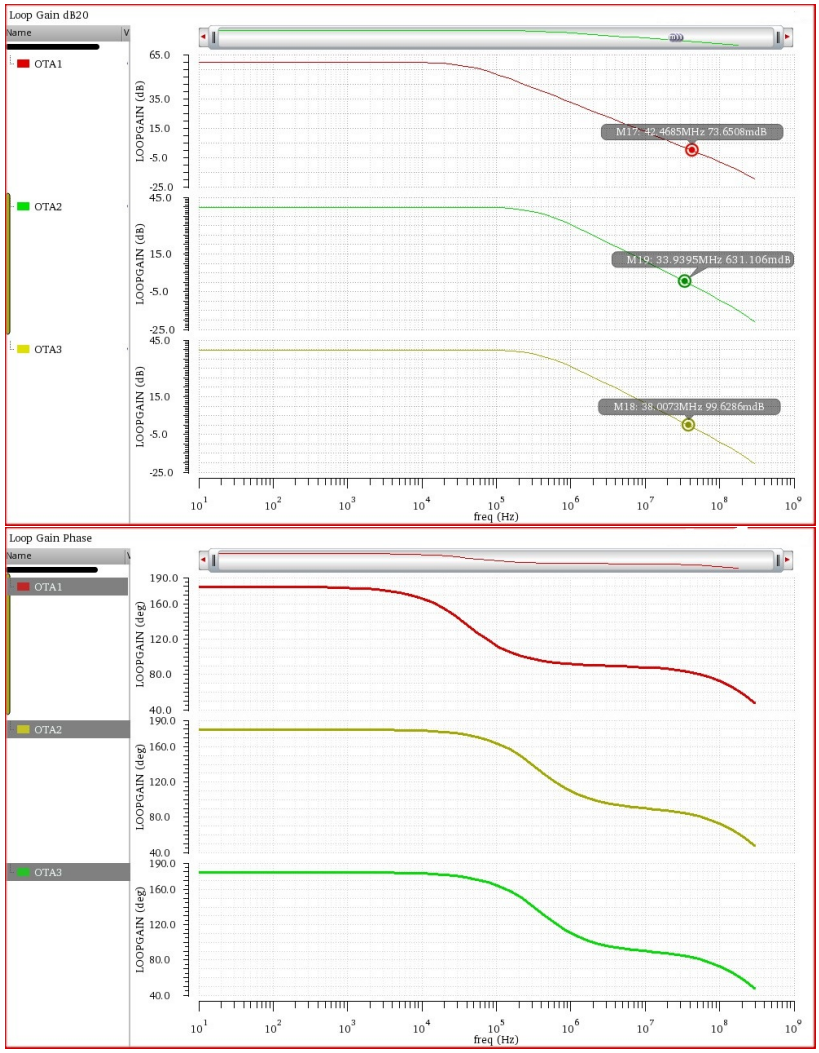


Figure 6.3: Frequency response of OTA 1,2 and 3

The maximum and minimum output voltages of OTA 1 and 2 are within the requirements in table 4.6 with headroom to spare, since the transistors M_3, M_4, M_9 and M_10 operated in moderate region. However the maximum and minimum output voltages of OTA 3 fulfill the requirements just barley. This will not affect the performance of the modulator as it will be seen in subsequent sections.

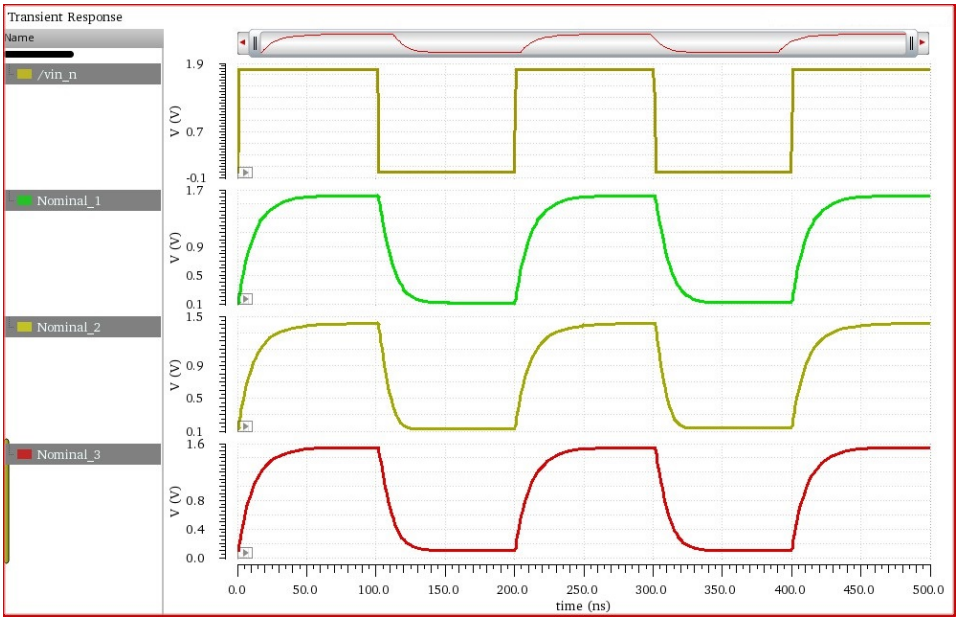


Figure 6.4: Slew rate of OTA 1, 2 and 3

The slew rates of the OTAs were found to be 42.12MV/sec, 46.23MV/sec 47.76MV/sec for OTA 1, 2 and 3 respectively, shown in Fig 6.4. With these high slew rates one can ensure that the non-linear settling error will not occur.

6.3.2 PVT Simulations

Table 6.2 summarize the maximum and minimum values of the OTAs 1, 2 and 3 parameters for the PVT simulations. It can be seen that the results fulfill the specifications of the amplifier. Table 6.3 list up the different environment used to perform the PVT simulations.

Table 6.2: PVT results for OTA 1, 2 and 3

Specification	Minimum		Maximum	
	Corner	Value	Corner	Value
DC gain 1	Corner 10	58.6dB	Corner 11	63.4dB
DC gain 2	Corner 6	39.2dB	Corner 11	43.3dB
DC gain 3	Corner 10	38.7dB	Corner 11	41.8dB
GBW 1	Corner 3	40.63MHz	Corner 6	47.13MHz
GBW 2	Corner 3	33.7MHz	Corner 6	40.3MHz
GBW 3	Corner 3	34.1MHz	Corner 6	41.5MHz
Phase margin 1	Corner 6	70.5°	Corner 13	81.4°
Phase margin 2	Corner 6	67.1°	Corner 15	75.5°
Phase margin 3	Corner 6	71.4°	Corner 15	82.8°
Power 1	Corner 0	14.5μW	Corner 3	45.3μW
Power 2	Corner 0	7.6μW	Corner 3	22.5μW
Power 3	Corner 0	4.7μW	Corner 3	17.3μW
Slew rate 1	Corner 5	36.9MV/sec	Corner 10	48.31MV/sec
Slew rate 2	Corner 5	40.3MV/sec	Corner 6	50.4MV/sec
Slew rate 3	Corner 5	38.9MV/sec	Corner 6	51.2MV/sec

The most critical environment for all three OTAs is corner 3, where the power consumption is the largest and the GBW is the lowest. However the GBW still satisfy the requirement for the minimum allowed value for all three OTAs to assure a stable charge transfer.

Table 6.3: PVT Corners

Corners	Transistor model	Supply voltage	Temperature
Corner 0	slow	2.5 V	-40°
Corner 1	slow	2.5 V	105°
Corner 2	slow	5.5 V	-40°
Corner 3	slow	5.5V	105°
Corner 4	fast	2.5 V	-40° V
Corner 5	fast	2.5 V	105°
Corner 6	fast	5.5 V	-40°
Corner 7	fast	5.5 V	105°
Corner 8	SNFP	2.5 V	-40°V
Corner 9	SNFP	2.5 V	105°
Corner 10	SNFP	5.5 V	-40°
Corner 11	SNFP	5.5 V	105°
Corner 12	FNSP	2.5 V	-40°
Corner 13	FNSP	2.5 V	105°
Corner 14	FNSP	5.5 V	-40°
Corner 15	FNSP	5.5 V	105°

Power consumption is nearly double of the nominal value for all three OTAs in corner 3, with the consumption of OTA 1 being noticeable big i.e. 45.4 μW. The technique mentioned in the previous section can be used to reduce it.

Figures 6.5, 6.6 and 6.7 illustrate the plots of the frequency responses for all corners for OTA 1, 2 and 3 respectively. As seen the DC gain for OTA 1 and 3 are worst in corner 10, while for OTA 2 it is worst in corner 6. Both corners have high supply voltage and low temperature. Nevertheless the DC gains satisfy the specifications of table 4.6 with good margin. The phase margins also fulfill the specifications in the worst corner 6, and thereby ensuring fastest settling time.

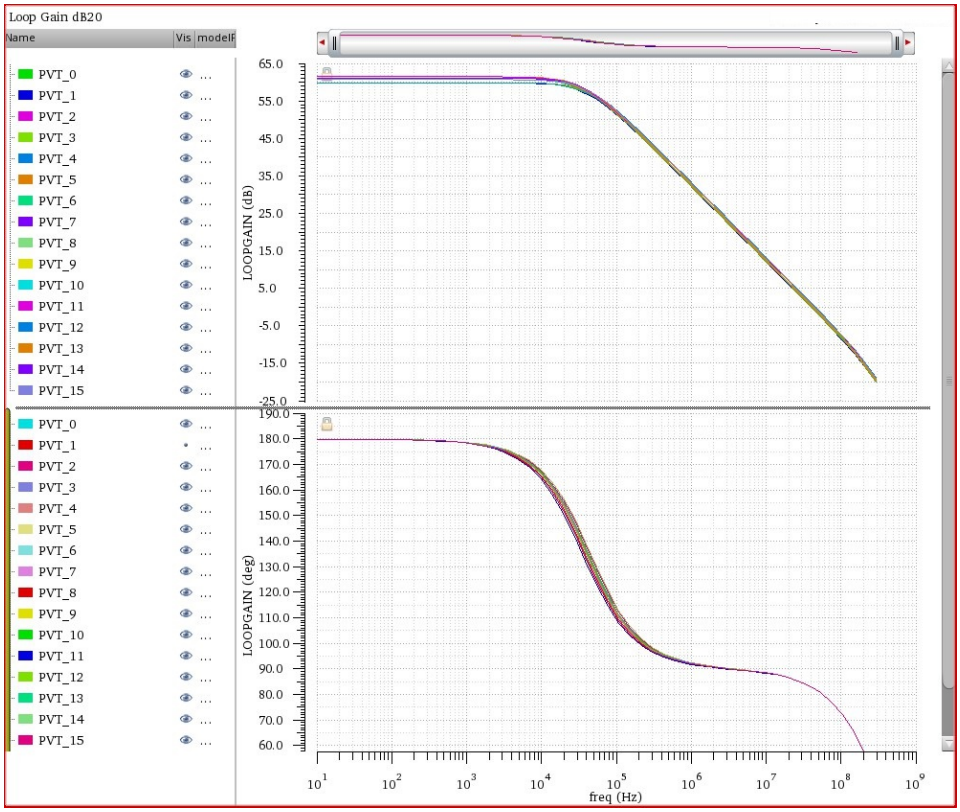


Figure 6.5: Corner simulation of the OTA 1 frequency response

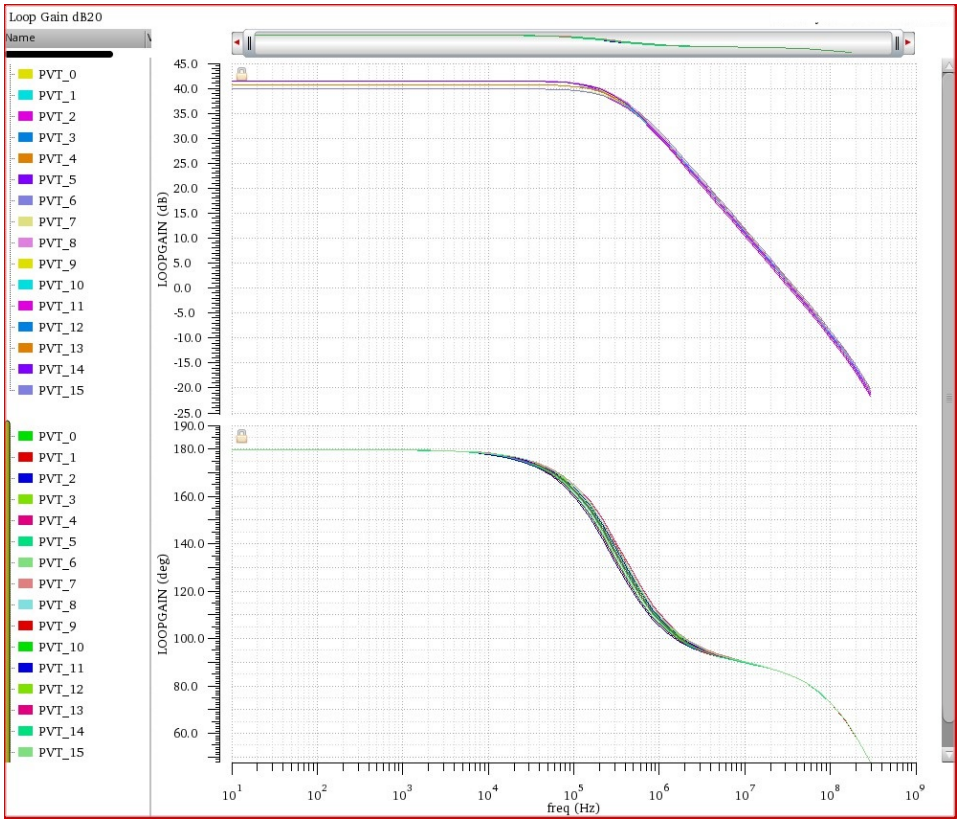


Figure 6.6: Corner simulation of the OTA 2 frequency response

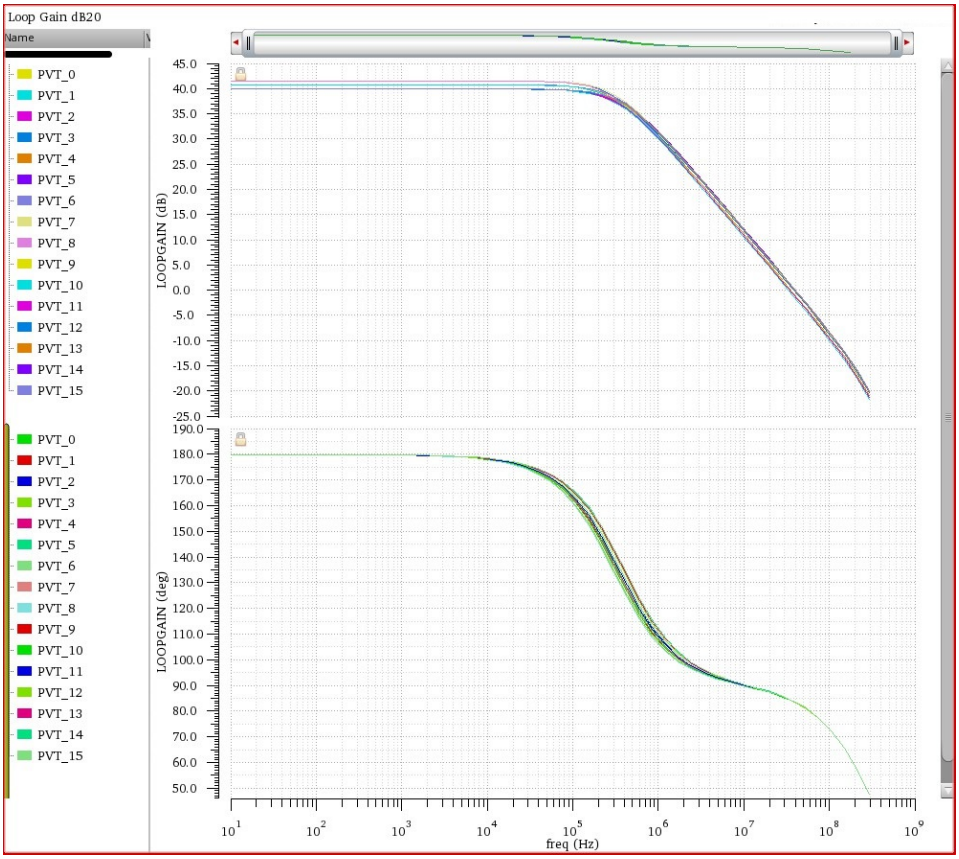


Figure 6.7: Corner simulation of the OTA 3 frequency response

The slew rates for all corners for OTA 1, 2 and 3 are depicted in figures 6.8, 6.9 and 6.10, and all have worst case in corner 5. With slew rates of 36.9MV/sec, 40.3MV/sec and 38.9MV/sec one can ensure a good enough settling time with good margin.

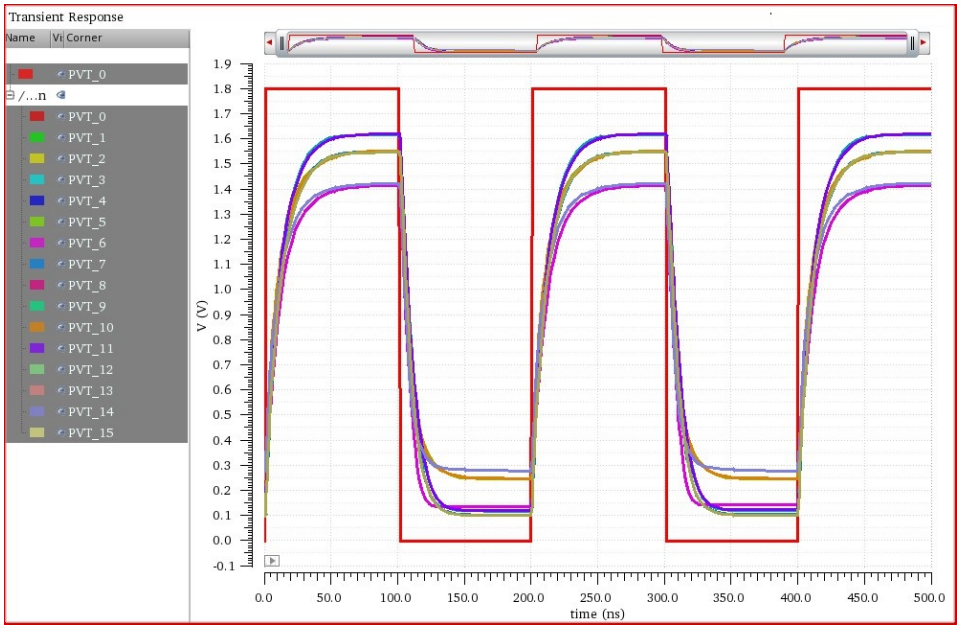


Figure 6.8: Corner simulation of the OTA 1 slew rate

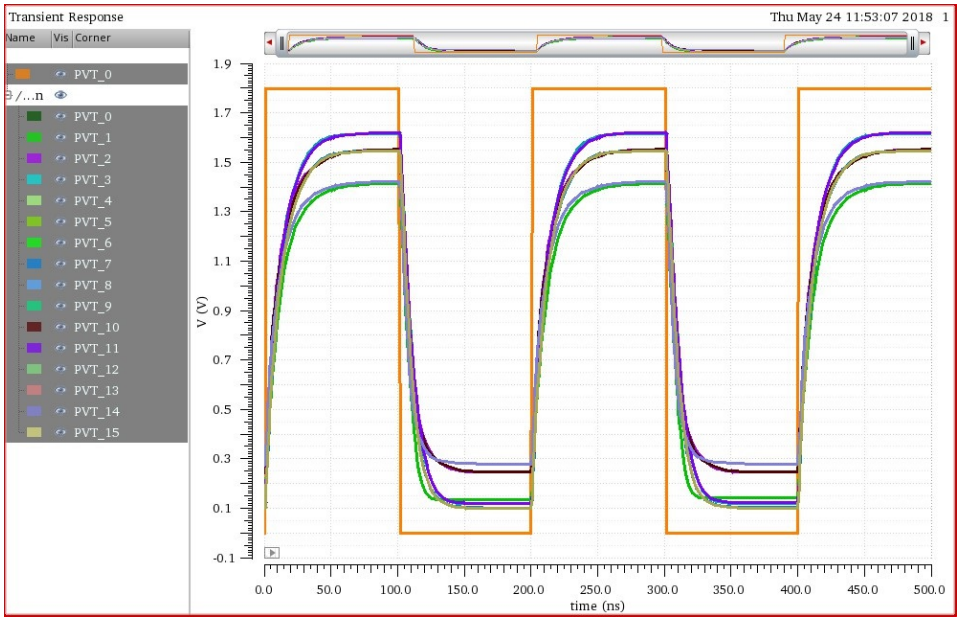


Figure 6.9: Corner simulation of the OTA 2 slew rate

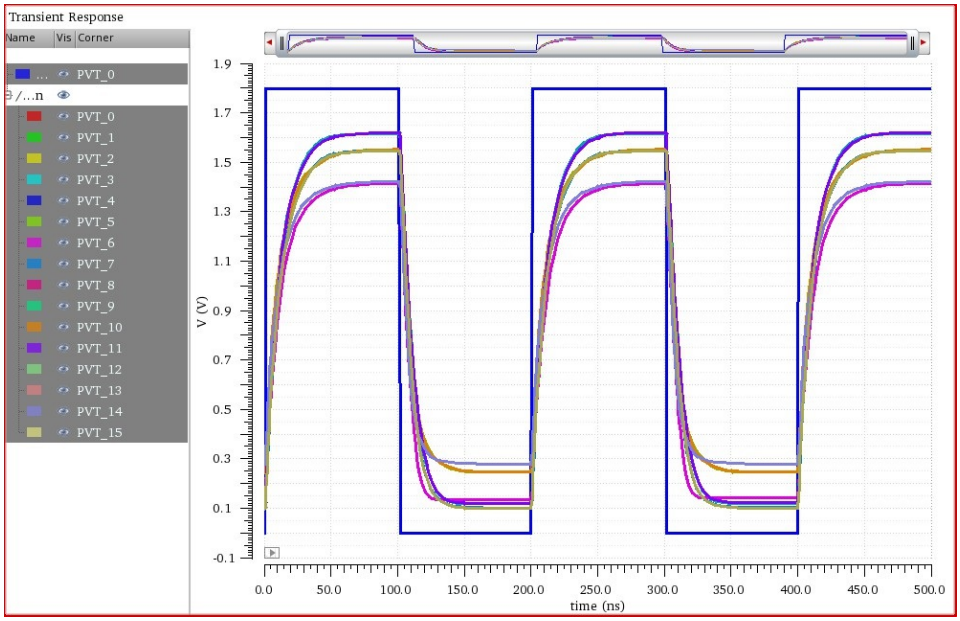


Figure 6.10: Corner simulation of the OTA 3 slew rate

6.4 Modulator

The response of the modulator was validated using nominal and PVT simulations with the corners listed in table 6.3. A Noiseless and noisy simulations were simulated to confirm that the specification given by the thesis is achieved.

6.4.1 Noiseless Simulations

The modulator was simulates using transient analysis without imposing device noise. Nominal simulation was simulated, and the PSD of the output signal is shown in Fig 6.11. The modulator achive a SNR of 101.20dB, a SINAD of 100.11dB and a ENOB of 16.5 bits. Here the only noise source is produced by the quantizer.

Table 6.4 summarize the SNRs, SINADs and ENOBs for all sixteen corners. It can be observed that all the corners fulfill the requirement of 16 bits, with corner 12 producing the lowest. Note that corner 12 is one of the corners with the lowest power consumption.

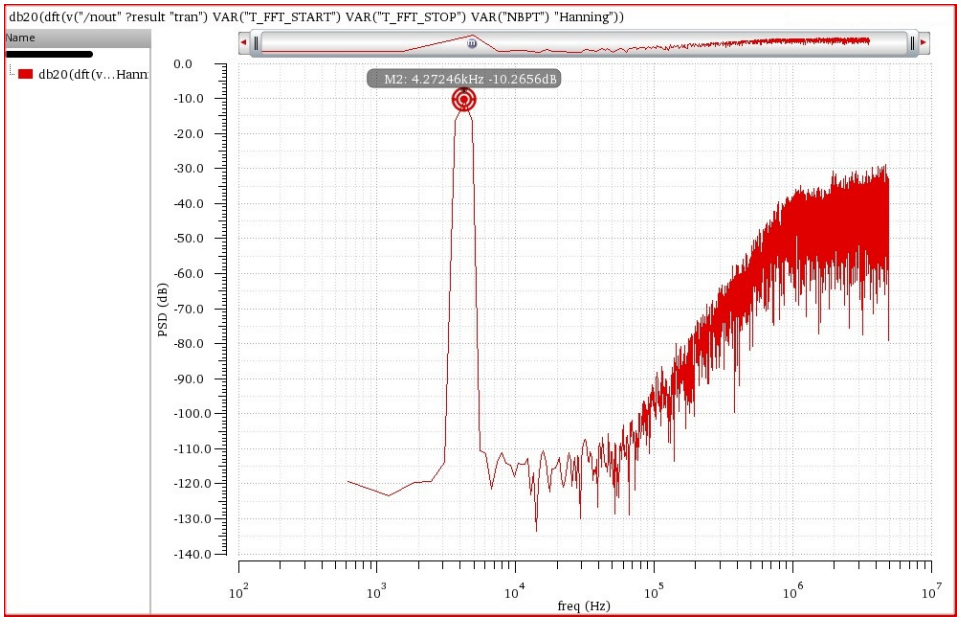


Figure 6.11: Nominal PSD of the modulator

Table 6.4: Results of the PVT simulations of the noiseless modulator

Simulation	SINAD[dB]	SNR[dB]	ENOB[bits]
Nominal	100.11	101.20	16.5
Corner 0	97.52	99.71	16.2
Corner 1	99.12	100.62	16.3
Corner 2	101.22	101.50	16.6
Corner 3	101.95	102.90	16.8
Corner 4	98.83	100.31	16.3
Corner 5	100.46	101.91	16.6
Corner 6	101.45	101.83	16.6
Corner 7	100.78	101.32	16.5
Corner 8	99.39	100.84	16.4
Corner 9	101.94	102.19	16.7
Corner 10	99.89	101.43	16.6
Corner 11	101.86	102.31	16.7
Corner 12	96.29	97.30	16.1
Corner 13	98.54	99.62	16.2
Corner 14	100.67	101.44	16.5
Corner 15	100.74	101.61	16.5

6.4.2 Noise Simulation

The modulator was simulated transient noise feature of the simulator. The PSD of the output signal is depicted in Fig 6.12. The PVT simulations are listed in table 6.5 where it can be observed that all corners except corners 0 and 12 achieve the specification of 16 bit. Nonetheless this is not a big problem as it is expected when introducing noise. Furthermore 15.7 and 15.8 bits are quite close to 16 bits.

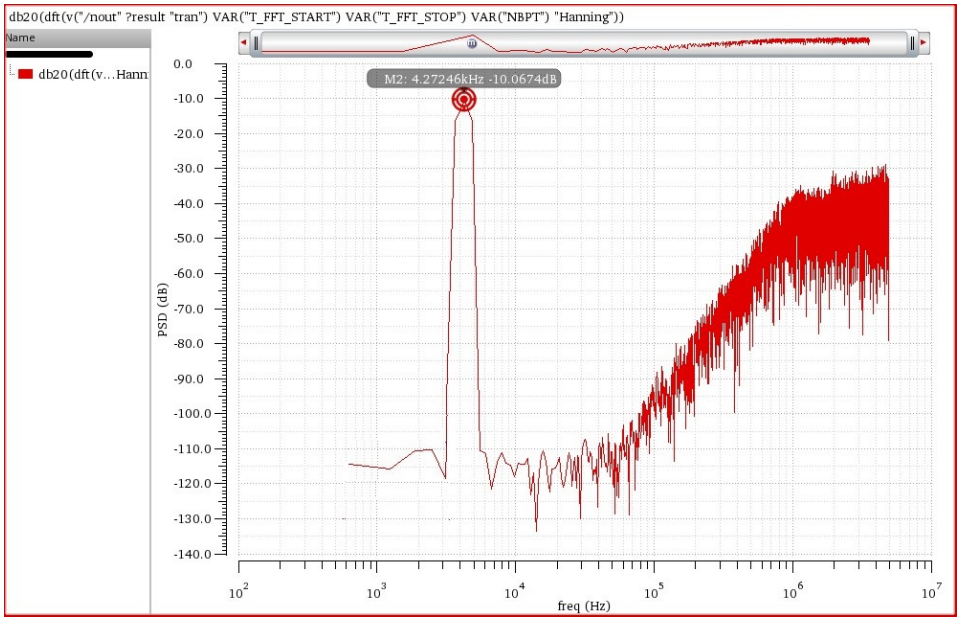


Figure 6.12: Nominal noisy PSD of the modulator output

Table 6.5: Results of the PVT simulations of the noisy modulator

Simulation	SINAD[dB]	SNR[dB]	ENOB[bits]
Nominal	98.23	99.67	16.2
Corner 0	93.65	94.86	15.8
Corner 1	95.78	96.31	16.0
Corner 2	98.93	100.54	16.3
Corner 3	100.76	101.12	16.4
Corner 4	96.59	97.23	16.1
Corner 5	99.41	100.73	16.3
Corner 6	96.78	97.20	16.1
Corner 7	98.26	99.75	16.2
Corner 8	95.84	96.44	16.0
Corner 9	100.77	101.34	16.5
Corner 10	99.00	100.75	16.4
Corner 11	100.78	101.55	16.6
Corner 12	93.89	94.2	15.7
Corner 13	95.55	96.15	16
Corner 14	96.69	97.23	16.1
Corner 15	98.76	99.9	16.3

6.5 Summary of the Performance

Tables 6.6 and 6.7 summarize the main results[1] and compare it with similar works. It can be seen that the figure of merit (FoM)[2] is not the lowest, but it has the potential to get smaller by using techniques to reduce the power consumption. However, it seems to stand the ground with other works using $0.18\mu m$ CMOS process. The roughly estimated area was found by opening *Layout XL* from schematic, then we chose generate from all

[1] Main results from nominal simulation with transient noise.

[2] $FoM = \frac{P}{2^{ENOB} \cdot 2 f_b} [\frac{pJ}{step}]$

source from the *Connective* menu. An area utilization of 75% were chosen, and the final estimated area is $0.077mm^2$.

Table 6.6: Comparison with other works

Ref.	Process [μm]	OSR	fs [MHz]	Supply [V]	BW [kHz]
[26]	1.5	64	10.24	5	160
[30]	3	256	4	5	8
[31]	0.35	256	12.8	3.3	25
[10]	0.18	256	1	1.8	2
[32]	0.18	128	0.256	1.5	1.0
[33]	0.13	40	1.048	1	8.0
[34]	0.18	256	5.12	3.3	10
[35]	0.18	250	5	1.8	10
[36]	0.18	64	1.28	1.8	10
[37]	0.13	40	0.8	0.8	10
This work	0.18	170	10	1.8	29

Table 6.7: Comparison with other works continued

Ref.	Power [μW]	SINAD [dB]	ENOB [bit]	FoM [pJ/step]	Estimated Area[mm^2]
[26]	7600	91	16	0.37	-
[30]	1200	89	14.5	3.24	-
[31]	6600	82	14	16.11	-
[10]	61	102.1	16.7	0.14	-
[32]	1350	93	15.2	18.49	-
[33]	38.0	92	15.0	0.07	-
[34]	1630	99	16.2	1.12	-
[35]	83	84.7	15	0.13	-
[36]	210	95	15.5	0.23	-
[37]	48	82	13.3	0.23	-
This work	87	98.2	16.2	0.20	0.077

Chapter 7

Conclusion

In this work a ΔΣ modulator was implemented in transistor-level based on the behavioural model derived in the feasibility study. The modulator was designed in a 180nm technology at an operating voltage of 1.8V. The final design is a third-order, fully differential, ΔΣ modulator with an oversampling ratio of 170. Through nominal and PVT simulations the robustness of the modulator was validated. It met the performance requirements with approximately reaching a resolution of 16 bit with a SINAD greater than 93 dB.

The OTAs were designed using folded cascode topology, which ended up with stratifying the specifications given in the feasibility study. One thing to notice is that the power consumption of OTA 1 seems to have a consumption greater than the rest of the OTAs. The use of transistors in moderate region have indeed proven to avoid problems involving limiting the output swing. Furthermore the use of g_m/I_D methodology has made it easier and faster to find the suitable dimensions for the transistors by characterizing the performance of NMOS and PMOS transistors in all regions of operation. A wide swing current mirror was used to bias the transistors, as the topology has the perks of not limiting the signal swing as much as the other conventional current mirrors. To control the common mode output, a switched capacitor CMFB circuit was implemented. It was seen that the stability did not degrade much.

The quantizer was implemented as a latched comparator, since its resolution is 1-bit. Because of the low resolution, a topology that focus more on high-speed operation than accuracy was chosen. The hysteresis was the main parameter of concern, and it was found to be as small as $5.86mV/V$. A two-phase non-overlapping clock generator circuits with delayed phases was implemented with the intention of operating the comparator and the TG switches in a synchronized manner. The on-resistances of the TG switches were also a concern. Through an exhaustive iteration of tuning the dimensions of the transistors in the TG switches, a set of values of the on-resistance were found. Although these values diverged some from the ones given by the specifications, there were no noticeable degradation in the performance of the modulator.

7.1 Future Work

This section describe possible steps that can be done to further improve, analyze and expand the ΔΣ ADC in both system and circuit level.

7.1.1 System Level

This thesis has provided useful insight about the flow of designing and implementing a ΔΣ ADC. It could be especially interesting to implement and compare a second order ΔΣ modulator with this work, since it has advantages such as relaxed stability requirement and reduced area usage. The methodology presented in the feasibility study and the thesis could easily be used as a guidance to implement the modulator.

The next step in the design process of the ADC could be to integrate the modulator with other blocks in the receive path to demonstrate an overall system. One of these blocks required to complete the ADC is a decimation filter, which is a challenge in itself. The decimation filter performs two important tasks. One being filtering out frequency components above f_b from the output signal from the quantizer, the other is down-sampling the data from the oversampling frequency to the Nyquist rate. Another thing to look at is a way of generating the three bias currents used in the OTAs.

Monte Carlo simulations of the modulator could be useful for deriving a model that includes the statistical variation of the parameters. It would both help in finding the statistical specifications of the integrators and verify that the mismatch effects do not affect the modulator performance.

7.1.2 Circuit Level

It was observed that the power consumption of OTA 1 was a little high. A way of reducing it is to implement an adaptive bias circuit with the folded cascode architecture which improves the power efficiency while achieving high slew rate. It will operate in class AB.

Monte Carlo simulations should be done for the OTAs, as the effects of mismatch on these important analog blocks are of interest.

Finally a layout should be realized of the modulator to verify that the parasitic capacitors do not affect its response. It could also be interesting to fabricate and measure a test-chip based on the modulator core.

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Appendix A

Switch Transistors' Dimensions and Resistance

A.1 Integrator 2

Table A.1: Switch transistors' dimensions and resistances of integrator 2

Switch	PMOS(W/L)μm	NMOS(W/L)μm	$R_{ON}(\Omega)$
I15	9.3/0.55	3.1/0.55	1493
I17	9/0.55	3/0.55	1531
I21	7.8/0.55	2.6/0.55	1530

A.2 Integrator 3

Table A.2: Switch transistors' dimensions and resistances of integrator 3

Switch	PMOS(W/L)μm	NMOS(W/L)μm	$R_{ON}(\Omega)$
I15	7.8/0.55	2.6/0.55	1635
I21	7.9/0.55	2.63/0.55	1630

A.3 Sum Block

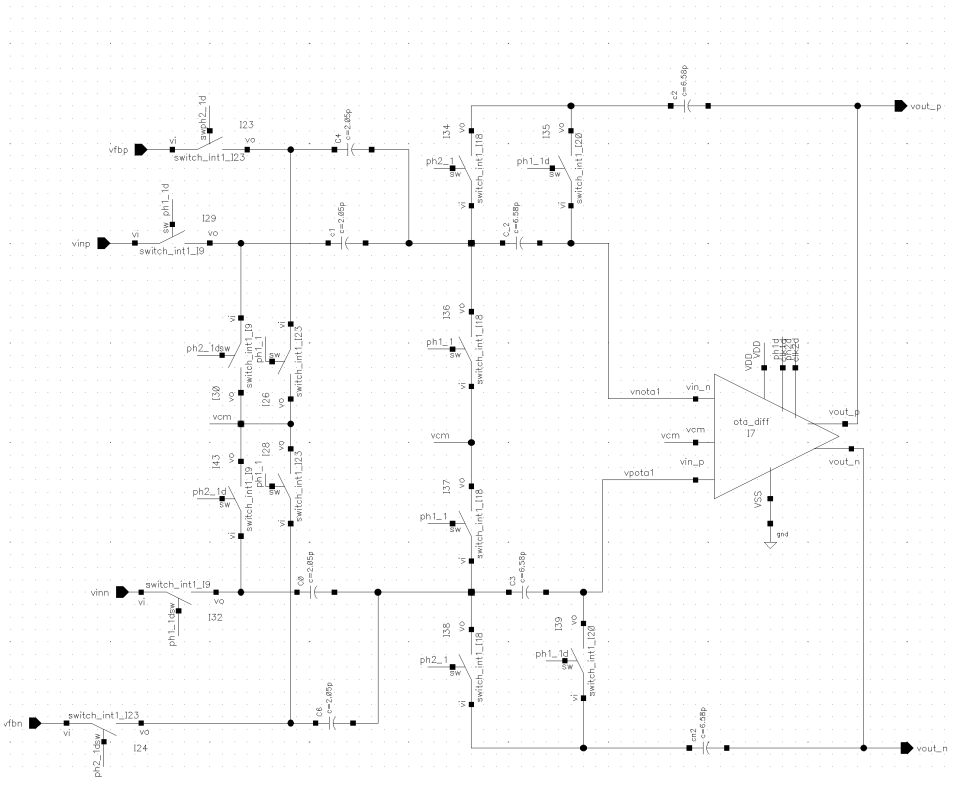
Table A.3: Switch transistors' dimensions and resistances of sum block

Switch	PMOS(W/L)μm	NMOS(W/L)μm	$R_{ON}(\Omega)$
I7	7.2/0.55	2.4/0.55	1700
I5	8.1/0.55	2.7/0.55	1701
I4	9/0.55	3/0.55	1705
I3	7.8/0.55	2.6/0.55	1743
I35	6.6/0.55	2.2/0.55	1706

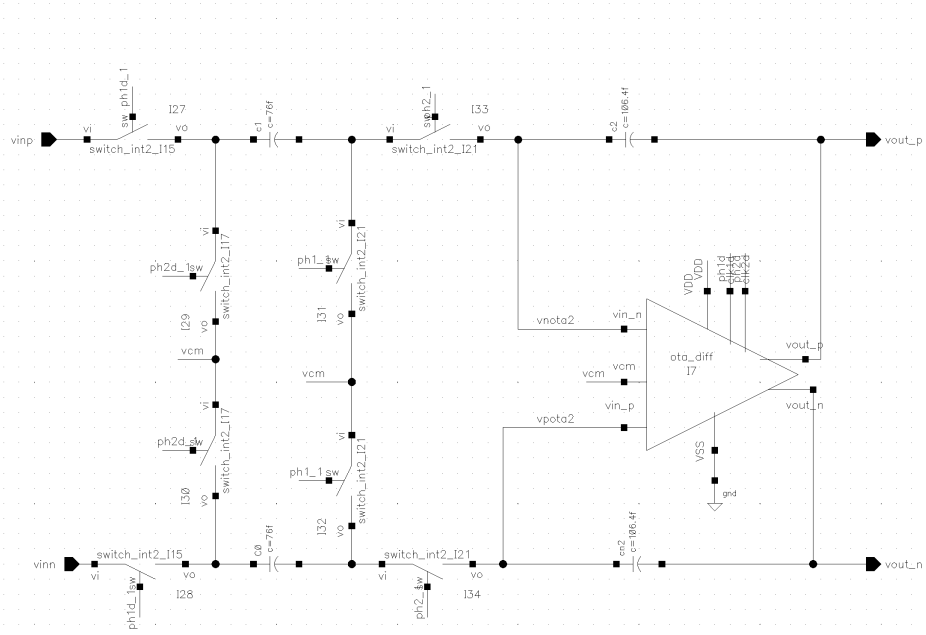
Appendix B

Circuits

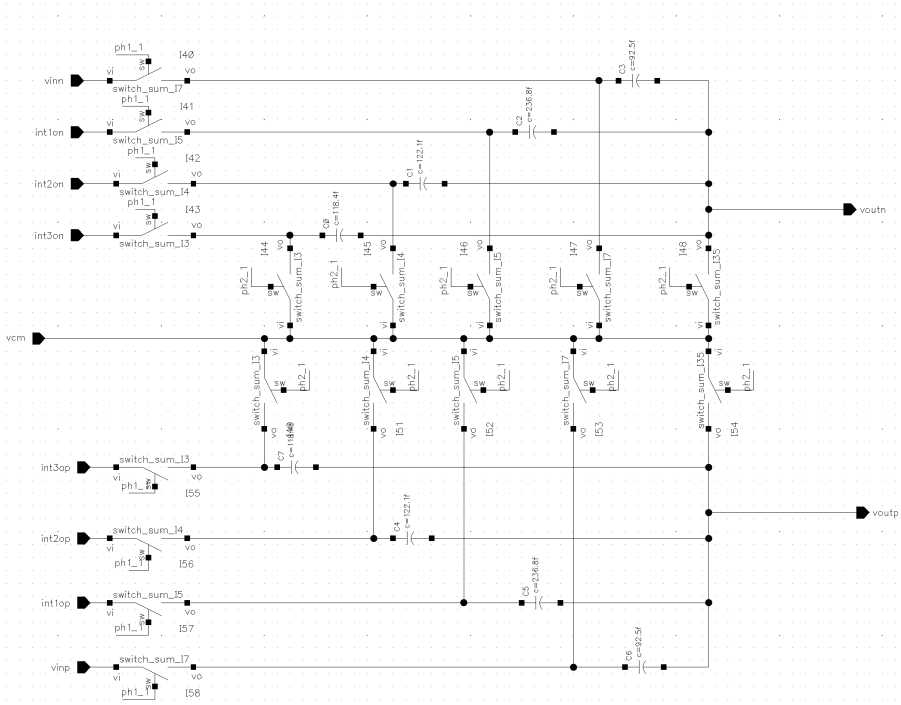
B.1 Integrator 1



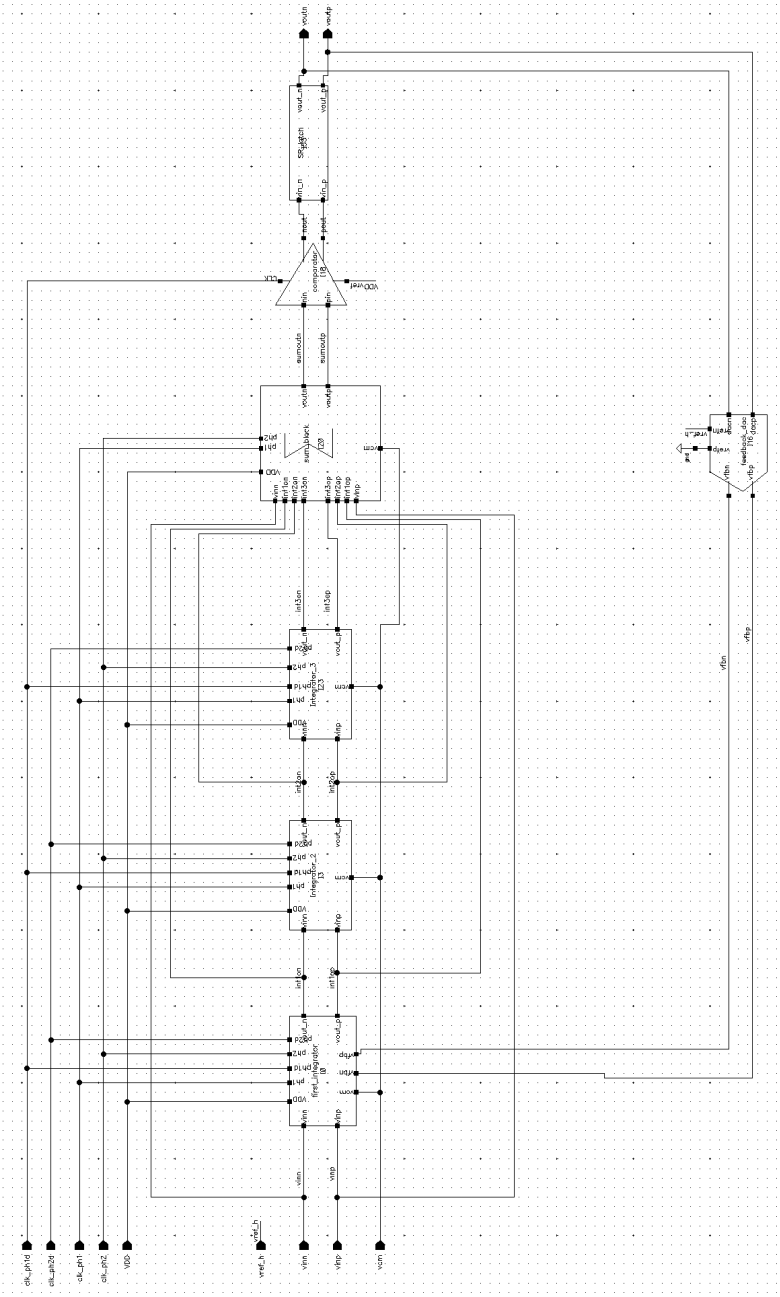
B.2 Remaining integrators



B.3 Summation node



B.4 Top module



B.5 SR latch circuit