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Design of a Harmonically Tuned Two-Stage Broadband Power Amplifier in Discrete GaN Technology

A Harmonic Loadpull and Harmonic Termination Approach

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Dedicated to my Mom, my Dad and my Sister

for always believing in me

Preface

This Master's Thesis has been developed for the Department of Electronic Systems at NTNU with guidance from associate professor Morten Olavsbråten. The intent of this thesis were to go in depth in the design procedures of a two-stage power amplifier, contemplating the harmonic loadpull and sourcepull design techniques. The amplifier were intended for further work incorporating dynamic drain and gate biasing in envelope tracking applications. The simulation results in this Master's Thesis was obtained using Keysight's Advanced Design System (ADS) software and the discrete gallium nitride high electron mobility transistors from Wolfspeed.

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I would like to thank my supervisor Associate Professor Morten Olavsbråten for his guidance and support throughout the project. His valuable advices, knowledge and passion for the subject has been of great importance and an exceedingly motivational factor.

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Finally, I am grateful to my family and friends who have supported me along the way.

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Summary

In this master's thesis a two-stage broadband power amplifier, along with the corresponding separate driver and power stages, has been designed with an in-depth analysis of the harmonic source- and loadpull methods and the harmonic termination technique. The power amplifiers were subsequently measured.

The power stage amplifier exhibit a mean transducer power gain of 13.5dB, a maximum linear output power of 25dBm, a mean saturated output power of 41.5dBm, and a mean peak Power Added Efficiency (PAE) of 54% at a quiescent voltage bias of 28V and a quiescent current bias of 200mA; The driver stage amplifier exhibit a mean transducer power gain of 17.5dB, a maximum linear output power of 25dBm, a mean saturated output power of 37.8dBm, and a mean peak PAE of 55% at a quiescent voltage bias of 28V and a quiescent current bias of 165mA; and the two-stage amplifier exhibit a mean transducer power gain of 29.8dB, a maximum linear output power of 25dBm, a mean saturated output power of 41.3dBm, and a mean peak PAE of 44.5% at a quiescent voltage bias of 28V and a quiescent current bias of 165mA and 200mA.

The power amplifiers were designed for 2.4GHz application with a bandwidth of 800MHz, but also exhibited promising performance down to 1GHz given some modifications, thus virtually doubling the intended bandwidth. The power amplifiers were designed using the gallium nitride high electron mobility transistors CGH40006P and CGH40010F from Wolfspeed.

Sammendrag

I denne masteroppgaven har en to-stegs bredbåndet effektforsterker, med tilhørende separate driver- og effektsteg, blitt designet ved bruk av en grundig analyse gjennom metodene for harmonisk kilde- og lastvariasjon, og teknikker for harmonisk terminering. Effektforsterkerene har deretter blitt målt.

Effektstegsforsterkeren viste en gjennomsnittlig effektvinning på 13.5dB, en maximal lineær uteffekt på 25dBm, en gjennomsnittlig mettet uteffekt på 41.5dBm, og en gjennomsnittlig maksimal tilført effektivitet på 54% ved en hvilespenning på 28V og en hvilestrøm på 200mA; driverstegsforsterkeren viste en gjennomsnittlig effektvinning på 17.5dB, en maximal lineær uteffekt på 25dBm, en gjennomsnittlig mettet uteffekt på 37.8dBm, og en gjennomsnittlig maksimal tilført effektivitet på 55% ved en hvilespenning på 28V og en hvilestrøm på 165mA; og to-stegs forsterkeren viste en gjennomsnittlig effktvinning på 29.8dB, en maximal lineær uteffekt på 25dBm, en gjennomsnittlig mettet uteffekt på 41.3dBm, og en gjennomsnittlig maksimal tilført effektivitet på 44.5% ved en hvilespenning på 28V og en hvilestrøm på 165mA og å 200mA.

Effektforsterkerene ble designet for 2.4GHz applikasjoner med en båndbredde på 800MHz, men viste også lovende ytelse ned til 1GHz gitt noen modifikasjoner, og derav så og si doblet tiltenkt båndbredde. Effektforsterkerene ble deignet ved bruk av galliumnitrid høy elektronmobilitet transistorene CGH40006P og CGH40010F fra Wolfspeed.

Abbreviations

ADS	Advanced Design System
BJT	Bipolar Junction Transistor
DBN	Drain Bias Network
DUT	Device Under Test
FET	Field Effect transistor
GBN	Gate Bias Network
HEMT	High Electron Mobility Transistor
HLP	Harmonic Loadpull
HSP	Harmonic Sourcepull
IMD	Intermodulation Distortion
IMN	Input Matching Network
IP3	Third-order Intercept Point
MAG	Maximum Available Gain
MESFET	Metal-Semiconductor Field Effect Transistor
MSG	Maximum Stable Gain
OMN	Output Matching Network
PAE	Power Added Efficiency
PCB	Printed Circuit Board
PDK	Process Design Kit
TOI	Third-order Intercept Point

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Introduction

Chapter 1

Introduction

In wireless receivers and transmitters the amplification of signals have a crucial role, and virtually all microwave and RF amplifiers today use three-terminal solid state devices such as gallium arsenide (GaAs) field effect transistors (FET), silicon (Si) or silicon germanium (SiGe) bipolar transistors, and lately gallium nitride (GaN) high electron mobility transistors (HEMT) [23]. GaAs has long been the automatic choice of semiconductor material for high frequency solid-state devices. However, during the last decade, GaN has become more popular in applications where high-frequency and high-power are required. It has certain traits that support smaller circuits for a given frequency and power level, allowing the higher power densities and efficiencies much sought after by designers of power-efficient wireless base stations and microcells. [6]. Both GaAs and GaN technologies have good performances in regards to both low-noise amplifiers (LNA) and power amplifiers (PA), and in companies developing radio equipment for wireless applications and in universities and science centers there are significant activities around these subjects. The PA is of great economical and technical significance because it constitute a substantial part of the costs in both development and production of radio equipment. In portable devices the PA is demanding a significant load on the batteries, and in base stations the PA consumes a considerable amount of energy and dissipates a substantial amount of power. Hence, good technical solutions are crucial for having a competitive advantage in the market.

Because transistors are nonlinear devices, the transistor amplifier exhibit nonlinear effects such as saturation and harmonic distortion. The former is due to a limited source of input power and the power handling capabilities of the transistor, while the latter is a more

prevalent problem related to the fact that the harmonics of input signals are generated at the output of an amplifier. For multiple input signals a set of harmonic mixing products where some will lie within the baseband, which leads to distortion of the signals. Generally the power levels of these harmonics is very low, but as input power increases the effects can be significant. [5]

In order to overcome these problems and be able to design PAs that perform as desired, one must be able to understand the behavior of the transistor in the specific operating conditions of the application. The most widely used technique in the microwave industry to accurately characterize devices in power amplifier applications is the loadpull method, which extrapolates the loadline method described by the I-V curves of the transistor and the load impedance. An extension of this method is the harmonic loadpull (HLP), which also considers the impedances at the harmonic frequencies, and the harmonic sourcepull (HSP) which evaluates the input instead of the output of the PA. Correspondingly the design method of harmonic termination is adopted to conform to the restrictions of the harmonic impedances.

1.1 Goals and requirements

The objective of this thesis is to design a two-stage broadband power amplifier for envelope tracking applications, while going in depth in the design process of a power amplifier using the harmonic loadpull and sourcepull techniques, and the harmonic termination design method. During the design process the focus is to find the optimal desired tradeoffs between gain, efficiency, output power and linearity. A comparison of the two-stage amplifier and each amplifier stage should be an integral part of the analysis. The power amplifier

Table 1.1: Initial PA design requirements

Parameter	Requirement
Frequency	2.4GHz
Bandwidth(-1dB)	800MHz
Gain	best possible tradeoff
Output power	best possible tradeoff
Efficiency	best possible tradeoff
Linearity	best possible tradeoff

should be designed using the CGH40006P and CGH40010F transistors from Wolfspeed for 2.4GHz applications and have a bandwidth of 800MHz.

1.2 Structure of the Thesis

The thesis is structured into 8 chapters, following each step in the design procedures chronologically, and additional appendices. **Chapter 1** serves as a short introduction to the subject of the master's thesis and presents the goals and requirements for the power amplifier design. **Chapter 2** contains the relevant theory for the design procedures and lays the theoretical foundation for the following chapter. **Chapter 3** elaborates on the preliminary design consideration. **Chapter 4** and **chapter 5** contains the design process and evaluations of the power and driver stage respectively. **Chapter 6** contains the design process and evaluation of the two-stage amplifier, and **chapter 7** presents the measurement results of the power, driver and two-stage amplifier. **Chapter 8** summarizes the entire process and discusses the results. **Appendix A** contains the schematic simulation setups used throughout the project, **appendix B** contains the large-signal measurement results, and **appendix C** contains photos of each of the amplifiers.

Background and Theory

Chapter 2

Background and Theory

In this chapter we will elaborate on the transistor technology and the theoretical foundations for the design procedures of the amplifier stages in the following chapters. The theory includes definitions of the transistor properties, classes of operation, the loadline method and the loadpull methods. Harmonic termination are also discussed briefly in relation to class F amplifiers.

2.1 Transistor technology

There are several different materials and technologies used for high-frequency applications available on the market, such as the III-V materials like gallium-arsenide (GaAs), indium-phosphide (InP), gallium-phosphide (GaP) and gallium-nitride (GaN) along IV materials like silicon (Si) and silicon-carbide (SiC). Each material properties are suitable to different applications. For some time the choice of transistors in microwave applications was essentially between silicon and GaAs. However recently GaN have had an increasing dominance as a high-frequency solid-state power amplifier and the combination of GaN and SiC offers additional performance [26]. The material properties of the silicon, GaAs, SiC and GaN is shown in table 2.1. The main advantages of the GaN in high-frequency and high-voltage operations is the wide bandgap and the high saturated electron velocity [12]. GaN also has a higher thermal conductivity than both Si and GaAs and combining it with a SiC substrate, GaN on SiC can provide excellent thermal properties due to the high thermal conductivity of SiC, which is crusial in high-power applications.

Table 2.1: A collection of key material properties for each of the semiconductors.

Semiconductor		Si	SiC	GaAs	GaN
Characteristics	Units				
Bandgap	eV	1.1	3.25	1.42	3.49
Electron Mobility at 300°K	cm^2/Vs	1500	700	8500	1000-2000
Saturated Electron Velocity	$\times 10^7 cm/s$	1	2	1.3	2.5
Breakdown Field	MV/cm	0.3	3	0.4	3.3
Thermal Conductivity	$W/cm°$K	1.5	4.5	0.5	>1.5
Relative dielectric constant	ϵ_r	11.8	10	12.8	9

2.2 GaN Technology

The GaN technology appeared early in the 1990's and was deemed an excellent semiconductor material for high-power high-frequency transistors based on the material parameters of bandgap, electron mobility and saturated electron velocity, as shown in figure 2.1. The lack of a bulk GaN source material led to the need for GaN growth on mismatched substrates such as Si, SiC and sapphire, and further advancements in the growth of device-grade aluminum gallium nitride (AlGaN) led to record power density RF amplifiers. Both defense and commercial applications of RF power transistors demand more power and wider bandwidths at higher frequencies, where GaN technology has been proven to be an excellent choice. [26]

The wide bandgap of GaN ($3.49eV$) compared to GaAs ($1.42eV$) and Si ($1.1eV$) ensures a larger breakdown voltage of the GaN devices such that they can operate at higher voltages, and the high saturated electron velocity of $2.5 \times 10^7 cm/s$ compared to GaAs ($1.3 \times 10^7 cm/s$) and Si ($1.0 \times 10^7 cm/s$) assures a higher current density. The high voltage and current density results in high power density and makes the GaN devices useful in high power applications. Because of the higher power density, the GaN devices can deliver more power using the same surface area, and for a given power application this property assures lower parasitic capacitance making it more suitable to wide bandwidth application. Smaller devices also have lower combining loss such that higher efficiency, gain and power are achievable. The GaN on SiC ensures excellent thermal properties due to the high thermal conductivity, which means that GaN on SiC will be significantly cooler than e.g. GaN on Si or GaAs on Si while dissipating the same amount of power. [12]

2.3 Transistor types

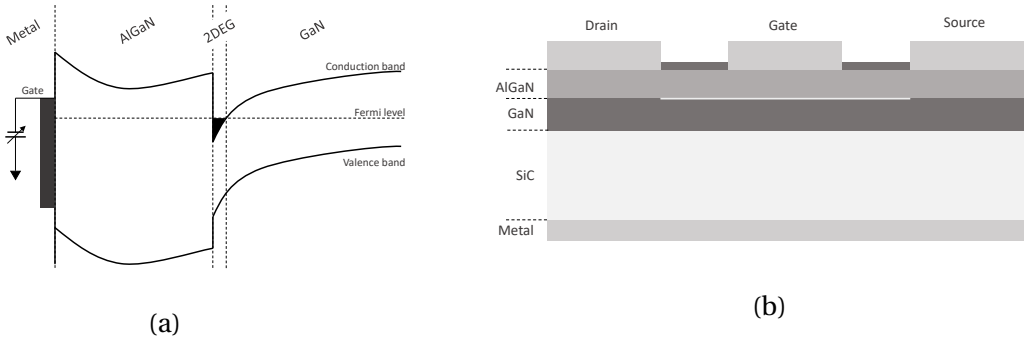
Transistors are usually divided into two classes; bipolar and unipolar transistors. The bipolar transistors induces currents of both major and minor carriers while the unipolar transistors induces currents of only the major carriers. In Bipolar Junction Transistors (BJTs) the output current is controlled by an input current, while in the unipolar Field Effect transistors (FETs) the output current is controlled by an input voltage. [12]

2.3.1 Metal-Semiconductor Field Effect Transistors

The Metal-Semiconductor Field Effect Transistors (MESFETs) is a type of unipolar transistor consisting of four terminals - drain, source, bulk and gate. Because of the higher mobility of electrons compared to holes, the MESFETs are usually n-type devices, where the bulk and source are connected to ground. The transistor will therefore have two bias voltages - the gate-to-source and drain-to-source voltages. By applying a reverse gate voltage a depletion region is formed in the conducting channel between drain and source, modulating the thickness of the conducting channel and thereby also the current. Applying an increasing drain-to-source voltage with constant gate voltage increases the electric field, and thereby also the width of the depletion region, on the drain side, making the conducting channel narrower. Although the conducting channel is narrower the larger electric field causes a higher electron velocity and thereby increases the current until the depletion region spreads across the whole channel, in which the electron velocity and thereby also the drain current saturates. In the saturated region the current can still be modulated by the gate-to-source voltage and will therefore act as a voltage controlled current source. [12]

2.3.2 High Electron Mobility Transistors

The HEMT or Heterostructure FET is a unipolar field-effect transistor, much like the MESFET, but instead of using a doped region as the conducting channel, the channel is incorporated as a junction between two materials with different bandgaps.[7] The bandgap difference creates an electron-well such that electrons will diffuse to the adjacent narrow-band material until the potentials reach an equilibrium, which results in a thin layer with high electron density. This accumulated layer, usually known as the 2-dimensional electron gas



(a) (b)

Figure 2.1: The (a) Band diagram [7] and (b) layer structure of an AlGaN/GaN on SiC HEMT.

(2DEG) layer, has a higher electron mobility because of the free electrons and can therefore support higher currents. The bandgap architecture of an AlGaN/GaN structure is shown in figure 2.1a. As seen from the figure the 2DEG layer is caused by the discontinuity between AlGaN and GaN conduction bands that dips under the Fermi level of the bands.

2.4 High-frequency Power Amplifier properties

The main goal of an amplifier is to replicate the input signal at the output with a greater magnitude, without distortion and as efficiently as possible. To manage this the amplifier needs an additional source of power that can be converted into the desired amplified signal. The high-frequency power amplifier makes use of a DC power source to generate the amplification of an RF signal, and optimizes the power conversion mainly based on the power delivered to the load of the amplifier. Practical amplifiers are not ideal and will produce non-linearities during the conversion which affect the performance of the amplifier. It is therefore necessary to evaluate the characteristics of the amplifier to be able to make the necessary tradeoffs for the specific application of the amplifier. Such parameters are e.g. stability, gain, linearity and efficiency as described in the following sections.

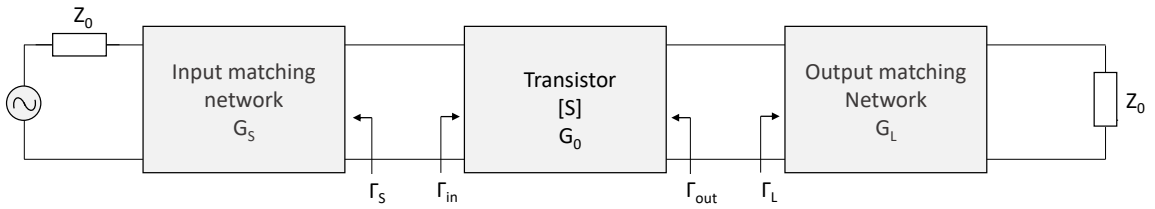


Figure 2.2: The general transistor amplifier circuit [23, p.198]

2.4.1 Stability

The stability of an amplifier refers to the amplifier's immunity to oscillations. Such oscillations are possible if either the input or output port impedance has a negative real part, which would imply that $|\Gamma_{in}| > 1$ or $|\Gamma_{out}| > 1$. Because Γ_{in} and Γ_{out} depend on the input and output matching networks, they are also dependant on Γ_S and Γ_L, see figure 2.2. [23] For different values of Γ_s and Γ_L the stability will thereby be either stable or unstable, which leads to two types of amplifier stability:

☞ **Unconditional stability**: The network is unconditionally stable if $\Gamma_{in} < 1$ and $\Gamma_{out} < 1$ for all passive source and load impedances (i.e. $|\Gamma_S| < 1$ or $|\Gamma_L| < 1$).

☞ **Conditional stability**: The network is conditionally stable if $\Gamma_{in} < 1$ and $\Gamma_{out} < 1$ for a certain range of passive source and load impedances.

Both $|\Gamma_S|$ and $|\Gamma_L|$ are frequency dependant, which means that the impedance of the system also will change as the frequency changes.

Stability Circles

By inspection of the limit for unconditional stability described above we get the following conditions for Γ_S and Γ_L:

$$|\Gamma_{in,out}| = \left| S_{11,22} + \frac{S_{21}S_{12}\Gamma_{L,S}}{1 - S_{22,11}\Gamma_{L,S}} \right| = 1 \tag{2.1}$$

which can also be written in the form $|\Gamma - C| = R$, representing a circle in the complex Γ plane with center C and radius R:

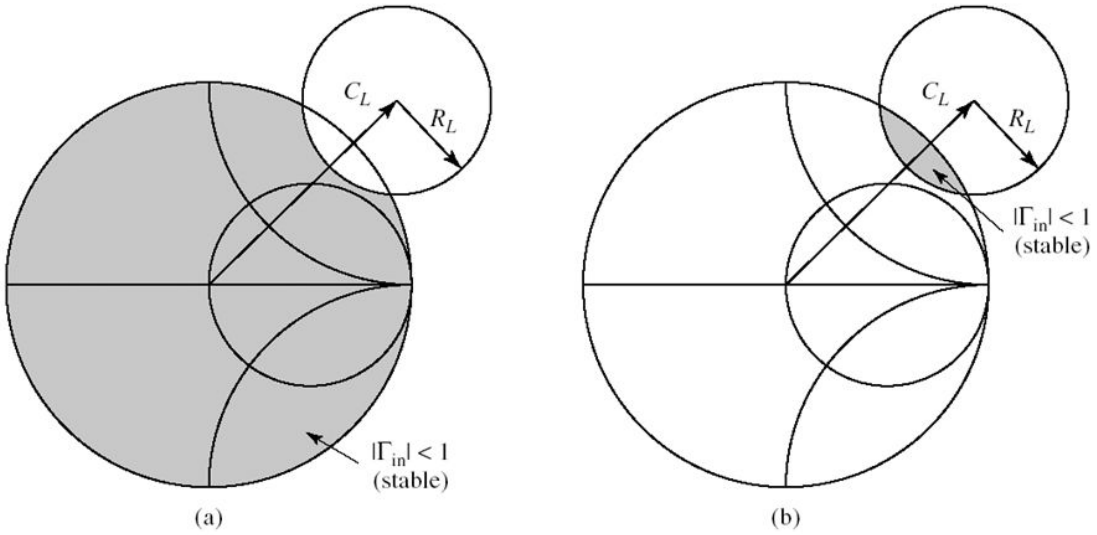


Figure 2.3: The regions of stability for a conditionally stable device where (a) $|S_{11}| < 1$ and (b) $|S_{11}| > 1$. [23]

$$\left|\Gamma_{L,S} - \frac{(S_{22,11} - \Delta S^*_{11,22})^*}{|S_{22,11}|^2 - |\Delta|^2}\right| = \left|\frac{S_{12}S_{21}}{|S_{22,11}|^2 - |\Delta|^2}\right| \tag{2.2}$$

where

$$C_{L,S} = \frac{(S_{22,11} - \Delta S^*_{11,22})^*}{|S_{22,11}|^2 - |\Delta|^2} \qquad \text{(center)} \tag{2.3a}$$

$$R_{L,S} = \left|\frac{S_{12}S_{21}}{|S_{22,11}|^2 - |\Delta|^2}\right| \qquad \text{(radius)} \tag{2.3b}$$

and Δ is the determinant of the scattering matrix

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \tag{2.4}$$

Considering the S-parameters of a transistor, we can plot the input and output stability circles for $|\Gamma_{in}| = 1$ and $|\Gamma_{out}| = 1$ where the inside and outside of the circle represent either a stable or unstable region. To determine which region is stable a test load (e.g $Z_L = Z_0$) has to be applied to the transistor. If the transistor is stable, all other points in that region is stable and vice versa. If the stability circle intersects the smith chart, both regions are contained

within the smith chart and the transistor is conditionally stable [1], as shown in figure 2.3. If the stability circle is completely outside the smith chart or encircles the whole smith chart the transistor is unconditionally stable.

Rollett's condition, K-Δ test

A simple test to figure out if an amplifier is unconditionally stable is the Rollett's conditions or K-Δ test, defined as

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2|}{2|S_{12}S_{21}|} > 1 \tag{2.5}$$

and

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| < 1 \tag{2.6}$$

The two conditions are sufficient to determine if an amplifier is unconditionally stable, but it says nothing about the relative stability of the device.

μ-parameter

Another test to check the stability of the amplifier is the μ-parameter, defined as

$$\mu_{load,source} = \frac{1 - |S_{11,22}|^2}{|S_{22,11} - \Delta S^*_{11,22}| + |S_{12}S_{21}|} > 1 \tag{2.7}$$

This parameter, as opposed to Rollett's conditions, includes a relative stability measure. If $\mu > 1$ the amplifier is unconditionally stable, and greater values of μ imply greater stability.

2.4.2 Power Gain

The power gain of a two-port network, in this case an amplifier, is defined as the ratio of the output power to the input power, but this can be defined in several ways. The three most common definitions are the transducer power gain (G_T), the available power gain (G_A) and the operating power gain (G_P). The definitions are as follows: [5]

[1] A conditionally stable transistor may also be referred to as potentially unstable

$$G_T = \frac{\text{power delivered to the load}}{\text{power available from the source}} = \frac{P_L}{P_{avs}} \tag{2.8a}$$

$$G_A = \frac{\text{power available from the network}}{\text{power available from the source}} = \frac{P_{avn}}{P_{avs}} \tag{2.8b}$$

$$G_P = \frac{\text{power delivered to the load}}{\text{power delivered to the network}} = \frac{P_L}{P_{in}} \tag{2.8c}$$

From the equations we see that the transducer power gain (G_T) is dependant on both the source and load impedances, while the available power gain (G_A) and the operating power gain (G_P) are dependant only on the source and load impedances respectively. The difference between these gain definitions is how they define the impedance match between the device and the source and load networks. If both networks are conjugately matched the definitions give the same result. The transducer power gain is the most useful of these definitions as it accounts for impedance mismatch in both networks and it's the most commonly used definition for amplifier. The transducer power gain can be written as

$$G_T = \frac{|S_{21}|^2(1-|\Gamma_S|^2)(1-|\Gamma_L|^2)}{|1-\Gamma_s\Gamma_{in}|^2|1-S_{22}\Gamma_L|^2} = \frac{|S_{21}|^2(1-|\Gamma_S|^2)(1-|\Gamma_L|^2)}{|(1-S_{11}\Gamma_S)(1-S_{22}\Gamma_L)-S_{12}S_{21}\Gamma_S\Gamma_L|^2} \tag{2.9}$$

where the substitution $\Gamma_{in} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1-S_{22}\Gamma_L}$ has been made. For a unilateral two-port network,

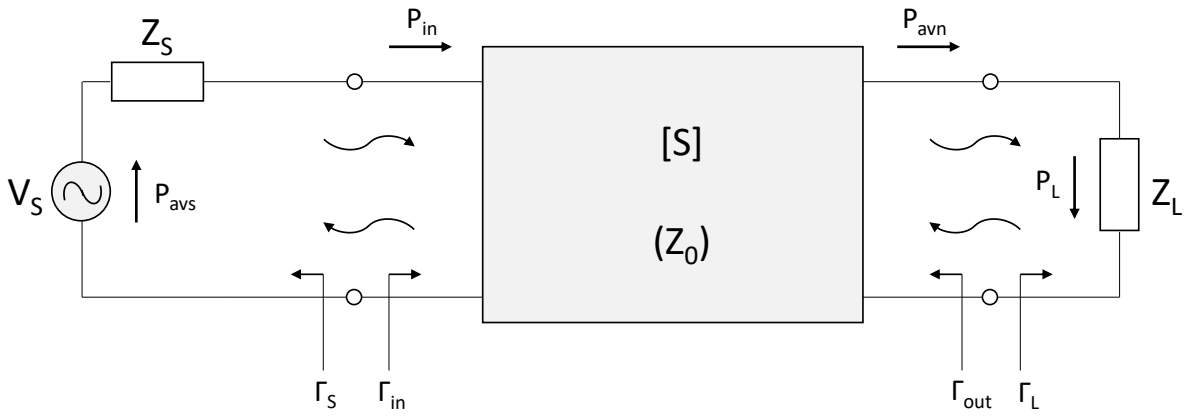


Figure 2.4: A two-port network with general source and load impedances, indicating power available and delivered in the components.

the reverse power gain is set to zero ($|S_{12}| = 0$) and the transducer power gain becomes

$$G_{TU} = \frac{|S_{21}|^2(1-|\Gamma_S|^2)(1-|\Gamma_L|^2)}{|(1-S_{11}\Gamma_S)(1-S_{22}\Gamma_L)|^2} = G_S G_0 G_L \tag{2.10}$$

where

$$G_{S,L} = \frac{(1-|\Gamma_{S,L}|^2)}{|(1-S_{11,22}\Gamma_{S,L})|^2} \quad \text{and} \quad G_0 = |S_{21}|^2 \tag{2.11}$$

For the available power gain (G_A) and the operating power gain (G_P) they can be expressed as

$$G_A = \frac{|S_{21}|^2(1-|\Gamma_S|^2)}{|1-S_{11}\Gamma_S|^2(1-|\Gamma_{out}|^2)} = G_S G_0 \frac{1}{1-|\Gamma_{out}|^2} \tag{2.12a}$$

$$G_P = \frac{|S_{21}|^2(1-|\Gamma_L|^2)}{(1-|\Gamma_{in}|^2)|1-S_{22}\Gamma_L|^2} = \frac{1}{1-|\Gamma_{in}|^2} G_0 G_L \tag{2.12b}$$

Maximum Available and Stable Gain

The maximum power transfer between the input matching network and the transistor, and the transistor and the output matching network occurs when the networks are conjugately matched, that is

$$\Gamma_{in} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1-S_{22}\Gamma_L} = \Gamma_S^* \tag{2.13a}$$

$$\Gamma_{out} = S_{22} + \frac{S_{12}S_{21}\Gamma_L}{1-S_{11}\Gamma_S} = \Gamma_L^*. \tag{2.13b}$$

Solving these equations for Γ_S and Γ_L separately gives a quadratic equation with real solutions only for a positive square root, equivalent to the condition of $K > 1$. Thus, unconditionally stable devices can always be conjugately matched, while conditionally stable devices also must satisfy $\Delta < 1$. For an unconditionally stable transistor the quadratic terms of equations (2.13a) and (2.13b) can be inserted into equation (2.9) for a K-dependant expression of the maximum transducer power gain[23]:

$$MAG = G_{T_{max}} = \frac{|S_{21}|}{|S_{12}|}(K - \sqrt{K^2-1}) \tag{2.14}$$

The maximum transducer power gain ($G_{T_{max}}$) are equal to the maximum available power gain ($G_{A_{max}}$) and the maximum operating power gain ($G_{P_{max}}$), as they describe the same case

of both conjugately matched input and output networks. The maximum gain, also referred to as matched gain or maximum available gain, is commonly denoted MAG. Since MAG does not make sense for $K < 1$, the limiting case where $K = 1$ is a useful figure of merit and is called the maximum stable gain (MSG):

$$MSG = (G_{T_{max}})\big|_{K=1} = \frac{|S_{21}|}{|S_{12}|} \tag{2.15}$$

Constant Gain Circles

In many cases it is preferable to design for less than maximum gain in order to improve the bandwidth of the amplifier, obtain a specific amplifier gain or reduce device variations. This can be achieved by introducing an impedance mismatch. Assuming $|S_{12}|$ is of negligible size, as in the unilateral case, the expressions for G_S and G_L from equation (2.11) can be used. The gain is maximized for conjugate matching; $\Gamma_S = S_{11}^*$ and $\Gamma_L = S_{22}^*$ resulting in

$$G_{S_{max}} = \frac{1}{1-|S_{11}|^2} \tag{2.16a}$$

$$G_{L_{max}} = \frac{1}{1-|S_{22}|^2} \tag{2.16b}$$

The normalized gain factor $g_S = G_S/G_{S_{max}}$ and $g_L = G_L/G_{L_{max}}$ would then represent constant

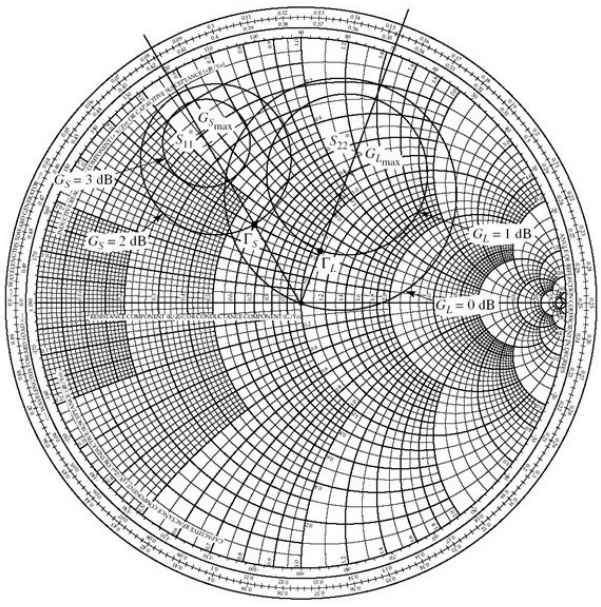


Figure 2.5: Constant source and load gain circles [23]

gain circles in the Γ_S or Γ_L plane, as shown in figure 2.5, with its center and radius given by

$$C_{S,L} = \frac{g_{S,L} S^*_{11,22}}{1-(1-g_{S,L})|S_{11,22}|^2} \qquad \text{(center)} \tag{2.17a}$$

$$R_{S,L} = \frac{\sqrt{1-g_{S,L}}(1-|S_{11,22}|^2)}{1-(1-g_{S,L})|S_{11,22}|^2} \qquad \text{(radius)} \tag{2.17b}$$

2.4.3 Linearity

An amplifier is called linear if the output power of the amplifier increases linearly with the input power, and the linearity is defined by the level of distortion in the device. Some figure of merits that quantify the distortion are the 1dB compression point (P_{1dB}), the intermodulation distorion (IMD) and the third-order intercept point (TOI or IP3).

Gain Compression

By the principle of conservation of energy, since the DC power supplied to an amplifier is limited the output power of the amplifier will also be limited. Thus, for higher input power levels the gain of the amplifier have to drop. This effect is called gain compression and leads to a non-linear amplification of the signal. This non-linearity can be modelled using a Taylor series and plotting output power versus input power. For a one-tone input signal

$$v_i = V_0 \cos \omega_0 t \tag{2.18}$$

the output power would be

$$\begin{aligned} v_o =& a_0 + a_1 V_0 \cos(\omega_0 t) + a_2 V_0^2 \cos^2(\omega_0 t) + a_3 V_0^3 \cos^3(\omega_0 t) + ... \\ =& (a_0 + \frac{1}{2} a_2 V_0^2) + (a_1 V_0 + \frac{3}{4} a_3 V_0^3) \cos(\omega_0 t) \\ &+ \frac{1}{2} a_2 V_0^2 \cos(2\omega_0 t) + \frac{1}{4} a_3 V_0^3 \cos(3\omega_0 t) + ... \end{aligned} \tag{2.19}$$

and the voltage gain of the sinusoidal signal, limited to the third order terms, becomes

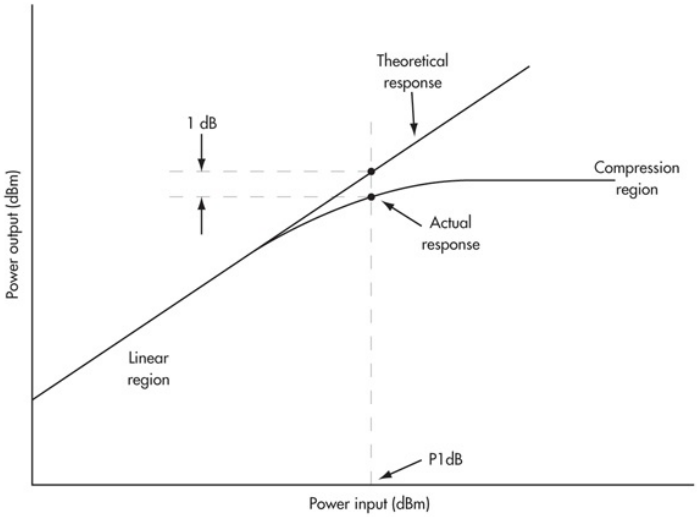


Figure 2.6: The 1 dB compression point for a nonlinear amplifier [11]

$$G_v = \frac{v_o}{v_i} = \frac{a_1 V_0 + \frac{3}{4} a_3 V_0}{V_0} = a_1 + \frac{3}{4} a_3 V_0^2. \tag{2.20}$$

The additional term containing a_3 is usually negative and causes gain compression for increasing values of V_0 [23]. To quantify the linear operating range of the amplifier one can define a point where the power level has decreased noticeably from the ideal case, such as the 1 dB compression point, as shown in figure 2.6.

Intermodulation Distortion

From the expansion of (2.19) we see that the single tone input creates harmonic frequencies of $n\omega_0$, where $n = 0, 1, 2, ...$, which usually would be outside the frequency band of the amplifier. For a two-tone signal such as

$$v_i = V_0(\cos(\omega_1 t) + \cos(\omega_2 t)) \tag{2.21}$$

a harmonic combination of the input frequencies $m\omega_1 + n\omega_2$ is created, where $m, n = 0, \pm 1, \pm 2, \pm 3, ...$ The sums and differences between the harmonics of the two input frequencies are called intermodulation products. If the intermodulation products appear close to the desired output frequencies they will distort the output signal, hence the term intermodulation distortion (IMD). [23]

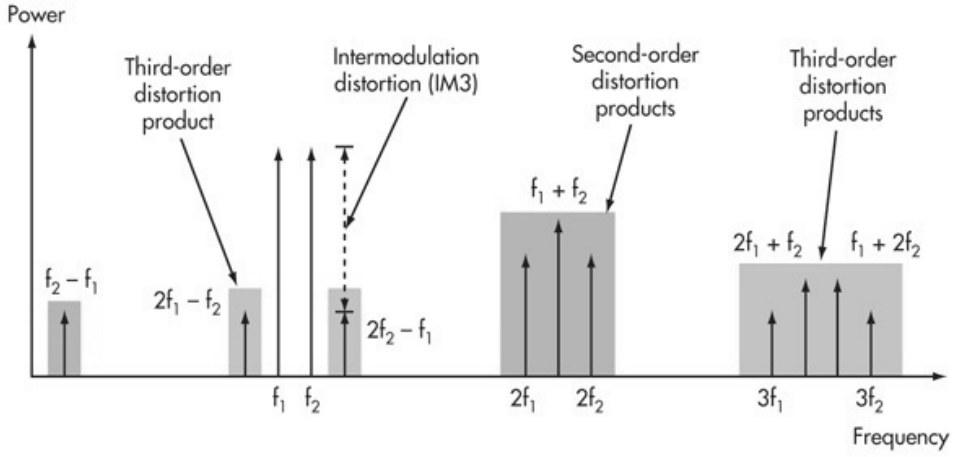


Figure 2.7: Output spectrum with intermodulation products [13]

Third-order Intercept Point

The third order products increase as V_0^3, and therefore also as the cube of the input power. Hence, on a $P_o - P_i$ log-log scale the third-order products increase by a slope of three compared to the slope of one for the first-order products. Both first- and third-order responses exhibit compression, but a hypothetical point, using the intersections between the ideal responses, can be used to quantify the effects. This point is called the third-order intercept point, usually denoted TOI or IP3, and shown in figure 2.8.

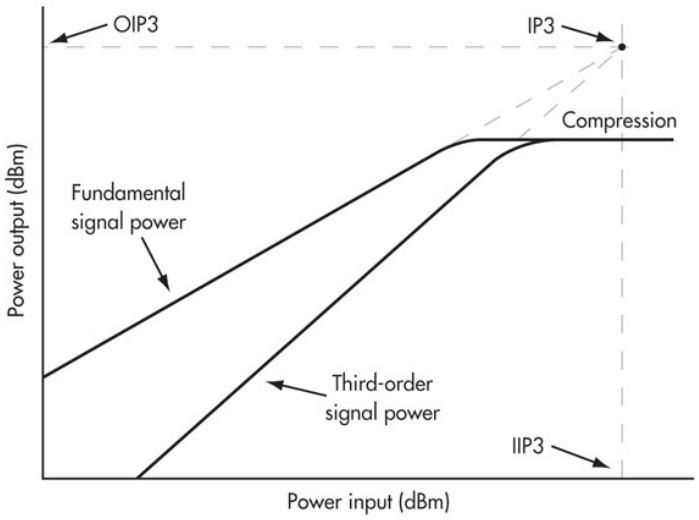


Figure 2.8: Third-Order intercept point [11]

2.4.4 Efficiency

The efficiency of a power amplifier is a measure of how well the amplifier can convert a given input power to a desired output power without waste, generally in the form of dissipated heat.

Drain Efficiency

The drain efficiency (η) is the ratio of the output power of the power amplifier to the input power of the DC supply, and is a measure of how much DC power that is converted to usable output power. From the flow diagram in figure 2.9 the drain efficiency is

$$\eta = \frac{P_{out}}{P_{DC}} \tag{2.22}$$

where $P_{DC} = V_{DC} I_{DC}$ and P_{out} is the power of the fundamental harmonic. A drawback of this measure is that it does not account for the input power of the incident RF signal into the device. The drain efficiency refers to FET devices, but can be interchanged by the equivalent collector efficiency for reference to bipolar devices.

Power Added Efficiency

The PAE is similar to the drain efficiency but takes into account the incident RF power. The input power can be significant in RF power amplifiers and the PAE is therefore a more accepted figure-of-merit than the drain efficiency. The PAE is the ratio of the difference in output and input RF power to the input power of the DC supply

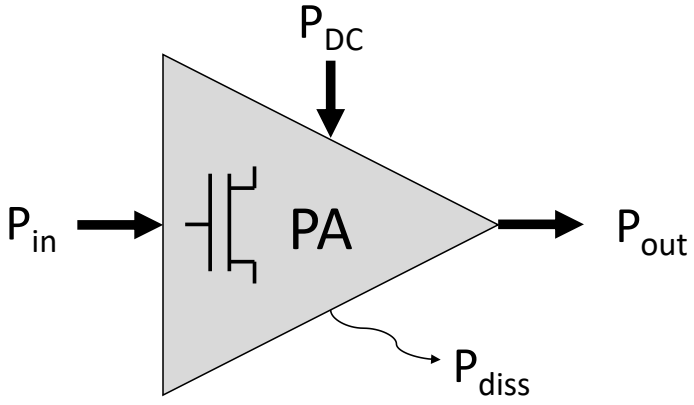


Figure 2.9: Power flow diagram of a Power Amplifier

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} = \frac{P_{out} - \frac{P_{out}}{G}}{P_{DC}} = (1 - \frac{1}{G}) \cdot \eta \tag{2.23}$$

where $G = P_{out}/P_{in}$ is the power gain of the power amplifier. The PAE is always less than the drain efficiency and for amplifiers that have less than 10dB transducer power gain, the input power significantly reduces the PAE compared to drain efficiency.

Overall Efficiency

The overall efficiency uses the input RF power in a different way than PAE, as in the ratio of output power to input powers.

$$\eta_{overall} = \frac{P_{out}}{P_{DC} + P_{in}} = \frac{P_{out}}{P_{DC} + \frac{P_{out}}{G}} = (\frac{1}{1 + \frac{\eta}{G}}) \cdot \eta \tag{2.24}$$

The overall efficiency makes more sense in a thermodynamic point of view and is always less than the drain efficiency. Note also that the overall efficiency can not be less than zero, as in the case for the PAE.

2.5 Amplifier Design Techniques

2.5.1 Power Amplifier Classes

In amplifier design it is important to select a known bias or operating point for the transistor, known as the DC quiescent point or simply Q-point. This point determines the characteristics of the amplifier regarding noise figure, gain, bandwidth, output power, efficiency and linearity performance. The basic RF power amplifiers can from these characteristics be separated into certain classes. Class A is the linear amplifier while class AB, B and C are classes with reduced reduction angle. The Q-points for each class are superimposed on the I-V curves in figure 2.10. Class F amplifiers are based on switching transistors and often biased like class AB or B, and bring the concept of harmonic tuning by terminating harmonics in different loads.

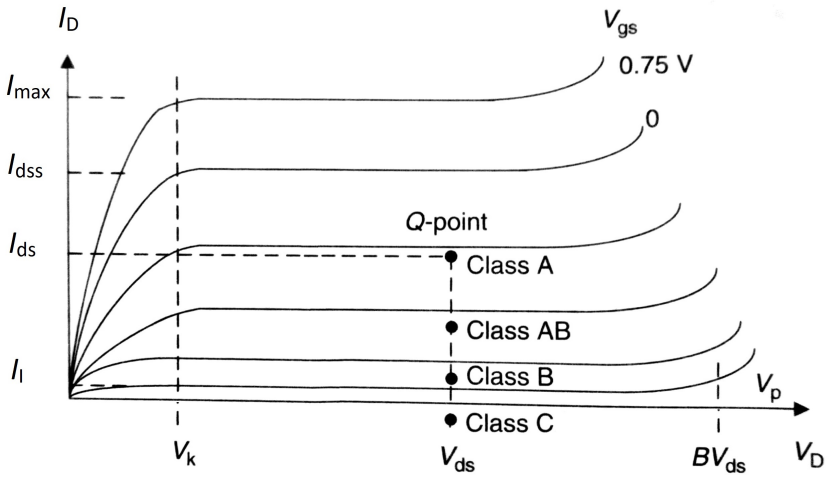


Figure 2.10: DC quiescent bias point for the linear amplifier classes. [5]

Class A

The characteristics of a class A power amplifier is that it conducts over a full cycle (360°) of the input sinusoidal signal by selecting the quiescent point approximately at the center of the device currents ($\frac{I_{max}}{2}$) and voltages ($\frac{BV_{ds}-V_k}{2}$) as shown in figure 2.10. It presents a linear transfer characteristic and high power gain, but is limited to a maximum theoretical drain efficiency of 50%. [5]

Class B

The class B power amplifier quiescent point is positioned at the edge the device cutoff region and thereby conducts for only half a cycle (180°). Hence, the linearity performance is worse than class A, but it has greater efficiency performance with a theoretical maximum drain efficiency of 78.5%. [5]

Class AB

The class AB power amplifier quiescent point positioned between class A and class B and are in a sense a combination of both, conducting between a half and a full cycle. It achieves a better linearity than the class B power amplifier and a higher efficiency than the class A power amplifier. [5]

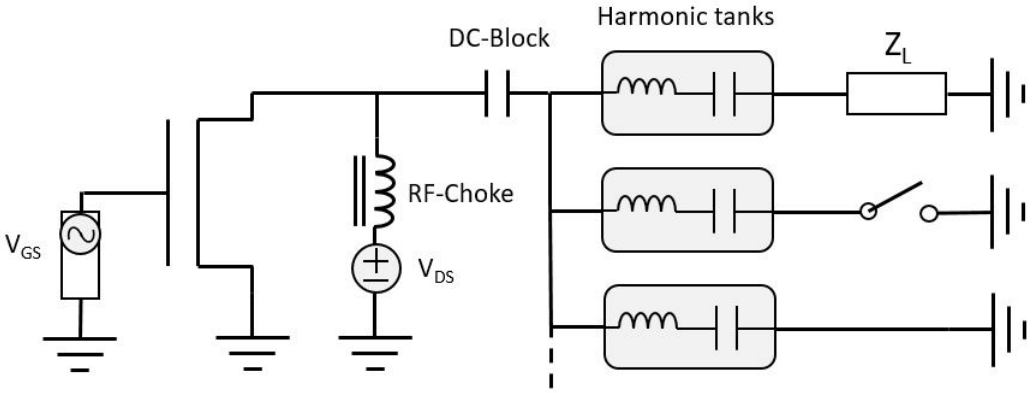


Figure 2.11: Harmonically tuned class F power amplifier

Class C

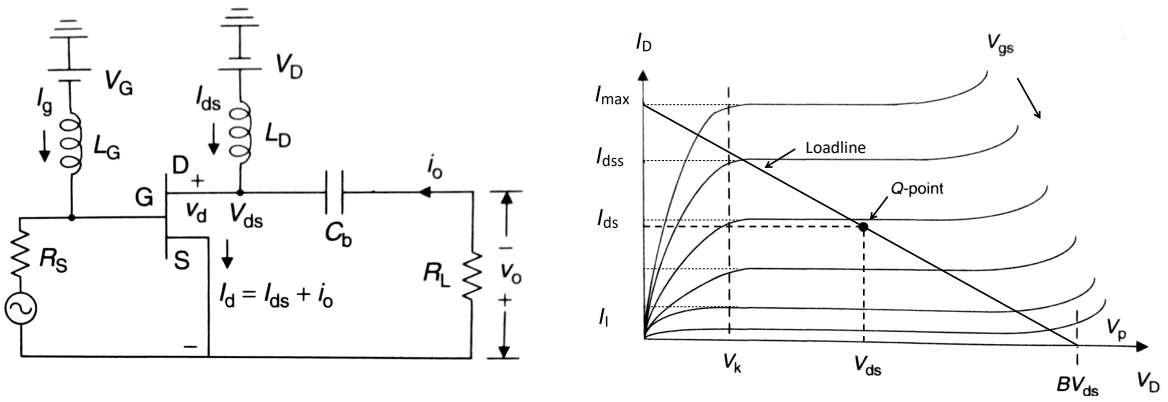
The class C power amplifier quiescent point is positioned within the device cutoff region and thereby conducts for less than half a cycle. These amplifiers are highly nonlinear, but have an efficiency performance greater than the other classes. Because of the nonlinear behavior of this amplifier it is mostly used in applications where linearity is not required. [5]

Harmonic termination, class F

Harmonic termination is an impedance matching technique where resonant tanks are used to terminate the harmonic frequencies in the desired loads. This technique is e.g. used in harmonically tuned class F power amplifiers to terminate the even harmonics in short circuits and the odd harmonics in open circuits to shape the voltage output to a square wave. A general model is shown in figure 2.11.

2.5.2 Loadline Method

Traditionally, a power amplifier can be designed using the loadline method, where the loadline determines the ac operating conditions for a given input signal and sets the maximum ratio of the peak-to-peak voltage and current for linear operations. The knee voltage, breakdown voltage, pinch-off voltage and maximum power that can be dissipated in the device put additional restrictions on the possible quiescent biases of the device. Considering the general transistor amplifier schematic in figure 2.12a and assuming that the transistor can be modelled as a voltage-controlled current-source with I-V characteristic as shown in fig-



(a) (b)

Figure 2.12: (a) Schematic of general transistor amplifier [5] and (b) its class A loadline superimposed on the I-V characteristics.

ure 2.12b, we can superimpose the class A loadline in order to calculate the properties of the device. The knee and breakdown voltage limits minimum and maximum drain voltage of the linear region, and the pinch-off voltage limits the minimum gate voltage.

The optimum load condition of the transistor is given by the slope of the loadline

$$R_{LL} = \frac{\Delta I}{\Delta V} = \frac{I_{max} - I_l}{V_k - BV_{ds}} \tag{2.25}$$

which for the ideal case ($V_k = 0$ and $I_l = 0$) reduces to

$$R_{LL_i} = \frac{I_{max}}{2V_{ds}} = \frac{I_{ds}}{V_{ds}}. \tag{2.26}$$

The DC power is given by

$$P_{DC_i} = V_{ds} I_{ds} \tag{2.27}$$

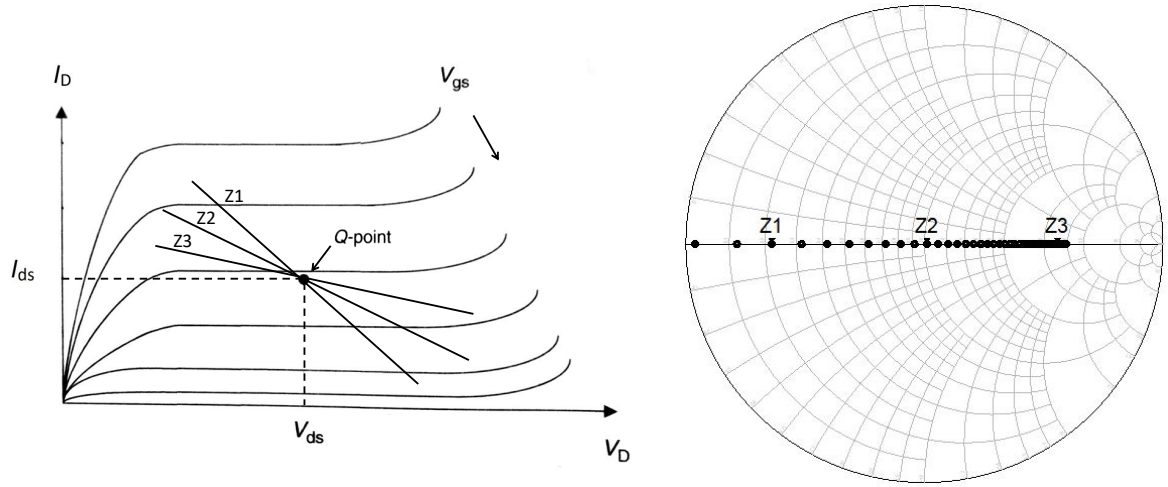
and, for a sinusoidal RF signal in maximum power transfer condition, the power delivered becomes

$$P_{o_i} = V_o I_o = \frac{V_{ds}}{\sqrt{2}} \frac{I_{ds}}{\sqrt{2}} = \frac{V_{ds} I_{ds}}{2} \tag{2.28}$$

resulting in a drain efficiency of

$$\eta = \frac{P_{o_i}}{P_{DC_i}} = \frac{1}{2} = 50\%, \tag{2.29}$$

as predicted for a class A amplifier.



(a) (b)

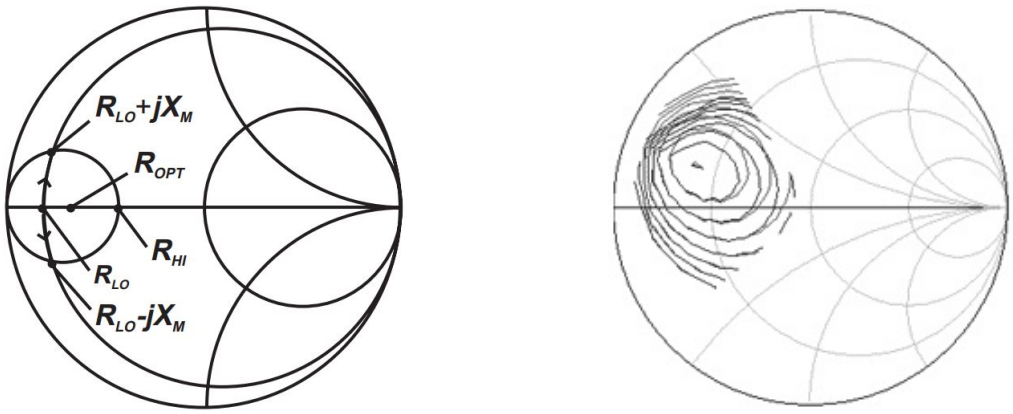
Figure 2.13: (a) The loadlines of different load resistances superimposed on the I-V characteristics, and (b) the representation of the same load resistances in the smith chart.

2.5.3 Loadpull

In loadpull the load impedance presented to the device is varied in order to find the key performances of the device under specified load conditions. The loadpull data can then be plotted in the smith chart as constant performance contours such that the optimal load impedance for the device can be found. The contours of these measurements also show how the device is behaving for deviations from this optimal point, and how tradeoffs can be implemented to satisfy a specific set of requirements.

The loadline method can be incorporated as a loadline measurement by realizing that each real valued load impedance represented by the loadline can be seen as a single point along the real axis of the smith chart, as is shown in figure 2.13b and 2.13a. Assuming that the optimal load resistance, R_{opt}, for a device results in the optimal power delivered P_{opt}, changing the resistance by a factor of p will reduce the power to P_{opt}/p. This is the case for both $R_{HI} = R_{opt}p$ and $R_{LO} = R_{opt}/p$. By allowing the load to be capacitive or inductive while ensuring that the magnitude of the load is still equal to R_{opt}, the load impedance can be extended into the imaginary axis of the smith chart as constant resistance and constant conductance circles. These circles intersects at some point and define a closed contour plot of constant performance equal to P_{opt}/p.

For low frequency applications where parasitics are negligible these contours are valid, but at higher frequencies the parasitic effects become significant and the optimal point moves



(a) (b)

Figure 2.14: (a) Constant resistance and conductance circles at P_{opt}/p [8]. (b) Loadpull contours affected by parasitics.

off the real axis, as can be seen in the contours of figure 2.14b. Since the effect of parasitics are frequency dependant, the optimal load impedance is also frequency dependant and moves counterclockwise in the smith chart, acting like a non-foster circuit.

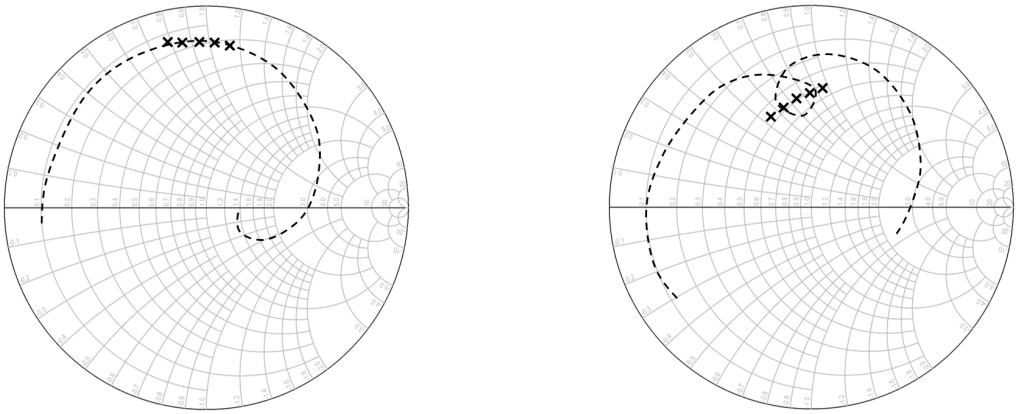
Harmonic Loadpull

In Harmonic Loadpull (HLP) the fundamental load impedance is fixed while varying the load impedance at a higher harmonic frequency and measuring the device performance at the fundamental frequency. The harmonic load impedances up to the 3rd harmonic can have significant effect on the performance of the device, which are strongly dependant on the fundamental load tuning, the operating point of the device and the drive power. In HLP the optimal harmonic load impedances are usually located at the edge of the smith chart reducing the loadpull to a harmonic phase sweep where the reflection coefficient is set to one.

Network matching techniques

An important observation to consider when designing the architecture of the output matching network is that the optimal load impedances travel counter-clockwise in the smith chart, behaving like a non-Foster circuit, while the impedance of the network travels clockwise with increasing frequencies, behaving like Foster circuits. Because of this the mismatch error between the network impedances and the optimal impedances of the network can not be sat-

isfied at every frequency. The options for achieving the least mismatch error are then either traversing the optimal points as they get closer, or introduce resonances that creates twirls in the impedance trajectory of the network in order to follow the optimal load impedances more closely for a short frequency span. These options are illustrated in figure 2.15. The through-matching generally reduces complexity of the implemented circuit and are often a good choice for matching of higher harmonics as they have less effect on the device performance, while the twirl-matching can give a higher degree of matching for a short span of frequencies, which can be beneficial for the fundamental frequencies.



(a) (b)

Figure 2.15: Illustrations of the (a) through- and (b) twirl impedance matching techniques.

Preliminary design considerations

Chapter 3

Preliminary design considerations

In this chapter the available devices and equipment for the design of the two-stage amplifier is presented. A preliminary evaluation of the transistors, design space and components are reviewed, and the design of the biasing network is presented.

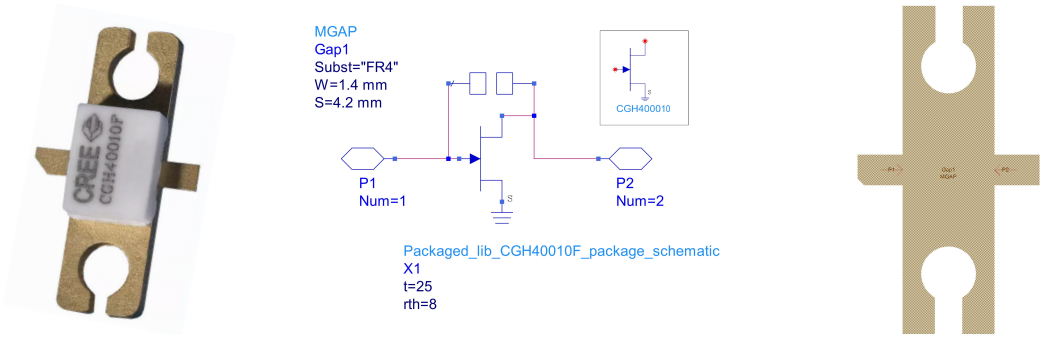
3.1 Transistors

The transistors selected for the two-stage amplifier are Wolfspeed's CGH40010F 10W and CGH40006P 6W, RF Power GaN HEMTs, for the Power Stage and Driver Stage respectively. The transistors offer a general purpose, broadband solution for a variety of RF and microwave applications, operating from a 28V rail; with both high efficiency, gain and bandwidth capabilities. The transistor models are validated for operating frequencies up to 6 GHz, with key characteristics as summarized in the following sections. The datasheets and additional documents for each transistor can be found on Wolfspeed's product pages [28, 29].

The Process Design Kit (PDK) of the packaged transistors contains a model library with a schematic simulation model of each transistor. In order to model the implementation of the packaged transistors on the printed circuit board (PCB), new cells are created in the Advanced Design System (ADS) library containing a modified schematic simulation model and a layout model. These models are used throughout the following design procedures.

3.1.1 Power Stage transistor

The CGH40010 transistor is available in both solder-down pill package (CGH40010P) and screw-down flange package (CGH40010F). The latter package type is used because of its better thermal connection to the aluminium plate heat sink. The aluminum plate has threaded holes positioned to match the flange of the transistor, thereby limiting the position of the transistor to certain fixed alternatives. The CGH40010F transistor is shown in the picture in figure 3.1a. The layout model consists of a package-layer created according to the di-



(a) (b) (c)

Figure 3.1: (a) A picture of the screw-down flange package, (b) the modified simulation schematic, and (c) the layout model of Wolfspeed's CGH40010F, 10W RF Power GaN HEMT.

Table 3.1: Excerpt from the datasheet of Wolfspeed's CGH40010F transistor, presenting its maximum ratings and electrical characteristics.

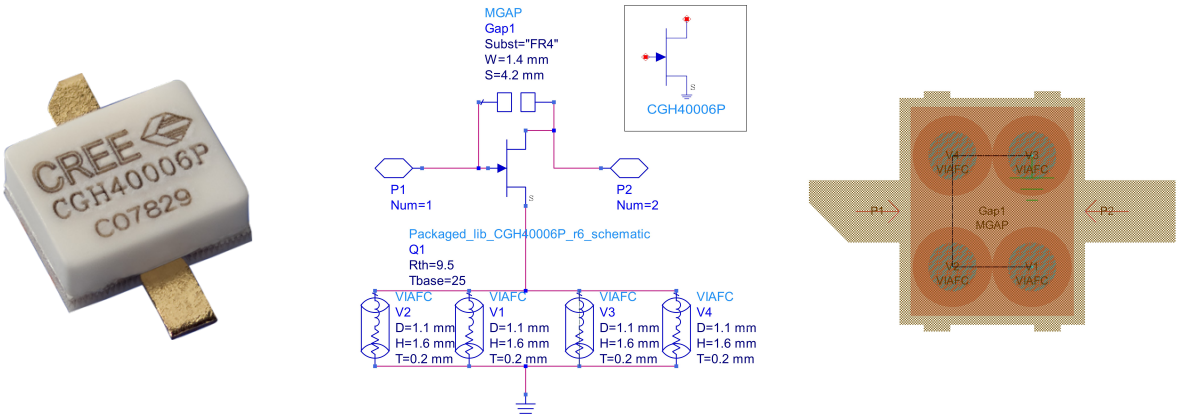
Transistor absolute maximum ratings						
Parameter	Symbol	Rating			Unit	Conditions
Drain-Source Voltage	V_{DSS}	84			Volts	25 °C
Gate-Source Voltage	V_{GS}	-10,+2			Volts	25 °C
Maximum Forward Gate Current	I_{GMAX}	4.0			mA	25 °C
Maximum Drain Current	I_{DMAX}	1.5			A	25 °C
Operating Junction Temperature	T_J	225			°C	
Maximum Power Dissipation	$P_{DISSMAX}$	14			W	< 113°C
Transistor Electrical Characteristics						
Characteristic	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate Threshold Voltage	$V_{GS(th)}$	-3.8	-3.0	-2.3	V_{DC}	$V_{DS} = 10V, I_D = 3.6mA$
Gate Quiescent Voltage	$V_{GS(Q)}$	-	-2.7	-	V_{DC}	$V_{DS} = 28V, I_D = 200mA$
Saturated Drain Current	I_{DS}	2.9	3.5	-	A	$V_{DS} = 6V, V_{GS} = 2V$
Small Signal Gain	G_{SS}	12.5	14.5	-	dB	$V_{DD} = 28V, I_{DQ} = 200mA$
Power Output at P^*_{sat}	P_{out}	10	12.5	-	W	$V_{DD} = 28V, I_{DQ} = 200mA$
Drain Efficiency at P^*_{sat}	η_D	55	65	-	%	$V_{DD} = 28V, I_{DQ} = 200mA$

* P_{sat} is defined as $I_G = 0.36mA$

mensions of the flange and tab sizes specified in the datasheet, and the reference plane of the transistor is at the edge of the transistor package. The layout model and the equivalent schematic simulation model are shown in figure 3.1. Relevant characteristics of the transistor, extracted from the datasheet, are summarized in table 3.1.

3.1.2 Driver Stage transistor

The CGH40006P transistor is available in a solder-down, pill package as shown in figure 3.2a. The layout model consists of a package-layer that is created according to the dimensions of the pill package and tab sizes specified in the datasheet, and a cond-layer consisting of a solder pad with the same size as the source terminal of the transistor package. Four via holes are placed on the on the solder pad for good thermal connection to the ground layer, and the drill holes for the vias are placed in the hole-layer. The reference plane of the transistor is at the edge of the transistor package. The layout model, with the equivalent schematic simulation model, is shown in figure 3.2. Relevant characteristics of the transistor, extracted from the datasheet, are summarized in table 3.2 for convenience.



(a) (b) (c)

Figure 3.2: (a) A picture of the screw-down flange package, (b) the modified simulation schematic, and (c) the layout model of Wolfspeed's CGH40006P, 6WW RF Power GaN HEMT.

Table 3.2: Excerpt from the datasheet of Wolfspeed's CGH40006P transistor, presenting its maximum ratings and electrical characteristics.

Transistor absolute maximum ratings				
Parameter	Symbol	Rating	Unit	Conditions
Drain-Source Voltage	V_{DSS}	84	Volts	25 °C
Gate-Source Voltage	V_{GS}	-10,+2	Volts	25 °C
Maximum Forward Gate Current	I_{GMAX}	2.1	mA	25 °C
Maximum Drain Current	I_{DMAX}	0.75	A	25 °C
Operating Junction Temperature	T_J	225	°C	
Maximum Power Dissipation	$P_{DISSMAX}$	8.4	W	$< 140°C$

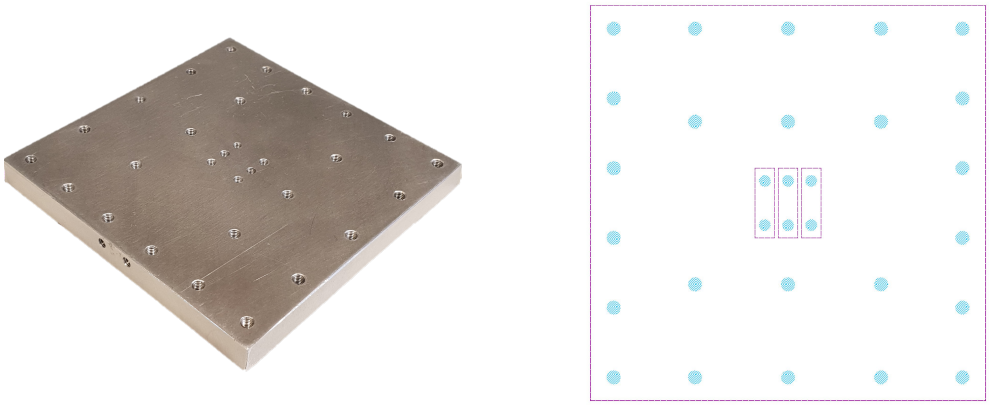
Transistor Electrical Characteristics						
Characteristic	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate Threshold Voltage	$V_{GS(th)}$	-3.8	-3.0	-2.3	V_{DC}	$V_{DS} = 10V, I_D = 2.1mA$
Gate Quiescent Voltage	$V_{GS(Q)}$	-	-2.7	-	V_{DC}	$V_{DS} = 28V, I_D = 100mA$
Saturated Drain Current	I_{DS}	1.7	2.1	-	A	$V_{DS} = 6V, V_{GS} = 2V$
Small Signal Gain	G_{SS}	11.5	13	-	dB	$V_{DD} = 28V, I_{DQ} = 100mA$
Power Output at $P_{in} = 32dBm$	P_{out}	7.0	9	-	W	$V_{DD} = 28V, I_{DQ} = 100mA$
Drain Efficiency at $P_{in} = 32dBm$	η_D	53	65	-	%	$V_{DD} = 28V, I_{DQ} = 100mA$

3.2 Equipment

3.2.1 Connectors

The connectors used for board-to-wire connections are the SMA607B-12 connector depicted in figure 3.3. The tab of the connector has a width of 1.4mm and a length of 2.05mm corresponding to a transmission line of 75Ω and 10.4 degrees at 2.4GHz.

Figure 3.3: Picture of the SMA607B-12 connectors used for board-to-wire connections.



(a) (b)

Figure 3.4: (a) Isometric view and (b) layout of the aluminium plate heatsink.

3.2.2 Heatsink

To ensure proper cooling of the transistor, an aluminium plate, as depicted in figure 3.4a, is used as a heatsink. Thereby the PCB has restrictions corresponding to the layout of the aluminium plate. A layout model of the aluminium plate is shown in figure 3.4b. It consists of a 85mm x 85mm square boundary and three possible cutouts in the center for positioning of the CGH40010F transistor. The holes are aligned with the threaded holes in the aluminium plate, and bolts are used to attach the PCB and transistor firmly to the aluminium plate. In the middle of both the left and right sides of the aluminium plate there is an available position for an input/output SMA connector.

3.2.3 Circuit substrate

The substrate selected for the PCB is a regular FR-4 material with electrical properties as shown in table 3.3. The circuit board is a two-layer PCB with a copper thickness of 35µm and a substrate thickness of 1.6mm. The relative permittivity and loss tangent are estimated values based on previous measurements.

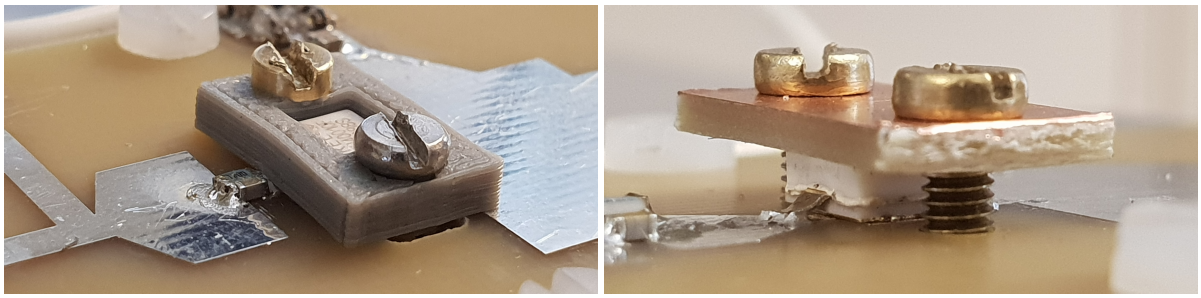
Table 3.3: Electrical properties of the FR-4 substrate

H (h_{substr})	Er (ϵ_r)	Mur (μ_r)	Cond (σ_{cond})	T (t_{cond})	TanD ($\tan\delta$)
1.6mm	4.4	1	$5.96 \cdot 10^7$ S/m	35µm	0.02

3.2.4 Transistor clamps

Because of the flange of the CGH40010F transistor package, the terminal tabs of the transistor are flush with the transmission lines on the top of the substrate. The clamp shown in figure 3.5a is used for the CGH40010F transistor in the power stage to put pressure on the terminal tabs, such that they do not need to be soldered to the transmission lines. The same transistor can thereby easily be move back and forth between the power stage amplifier and the two-stage amplifier circuits. The clamps is 3D-printed using ABS plastics.

Since the CGH40006P transistor package does not have a flange, it must lay on top of a copper pad with good connection to ground. In order to ensure a good connection the clamp shown in figure 3.5b is used to press the transistor down on the copper pad. Since the terminal tabs of this transistor is not flush with the transmission lines, neither of the clamps could be used on the terminals, thereby requiring them to be soldered. Both clamps also protect the user from touching the transistors, as they can get quite hot during operation. They do however affect the impedance of the transmission lines, but this effect is negligible.



(a) (b)

Figure 3.5: Pictures of the clamps used for the (a) power stage and the (b) driver stage

3.2.5 Component library

The lumped components available are the thin-film surface mount resistors in 0805 packages with values according to the E12 series from Johanson Dielectrics, and the R14S series capacitors [15] and L14 series inductors [16] in 0603 packages from Johanson Technologies with values as presented in table 3.5 and 3.5. Additional capacitors from Murata [17, 18, 19] in 1205 packages are also available for the high value capacitors presented in table 3.6. The component models of the capacitors and inductors are available in ADS, while the resistors are assumed to be ideal lumped components.

Table 3.4: Available component values for the R14S capacitors in pico farad.

0.3	0.5	0.8	1.0	1.2	1.5	1.8	2.2	2.7	3.3	3.6	3.9	4.7
5.6	6.8	7.5	8.2	9.1	10	12	15	18	20	22	24	27
30	33	36	39	43	47	56	68	82	100	120	150	180

Table 3.5: Available component values for the L14 inductors in nano henry.

1.0	1.5	1.8	2.2	2.7	3.3	3.9	4.7	5.6	6.8	8.2	10
12	15	16	18	20	22	27	33	39	47	56	68
82	100	120	150	180	220	330	390	560	1000	2200	6800

Table 3.6: Available components from Murata.[17, 18, 19]

GRM188R71H104KA93D	100nF
GRM31CR72A105KA01L	$1\mu F$
GRM31CR61H106KA12L	$10\mu F$

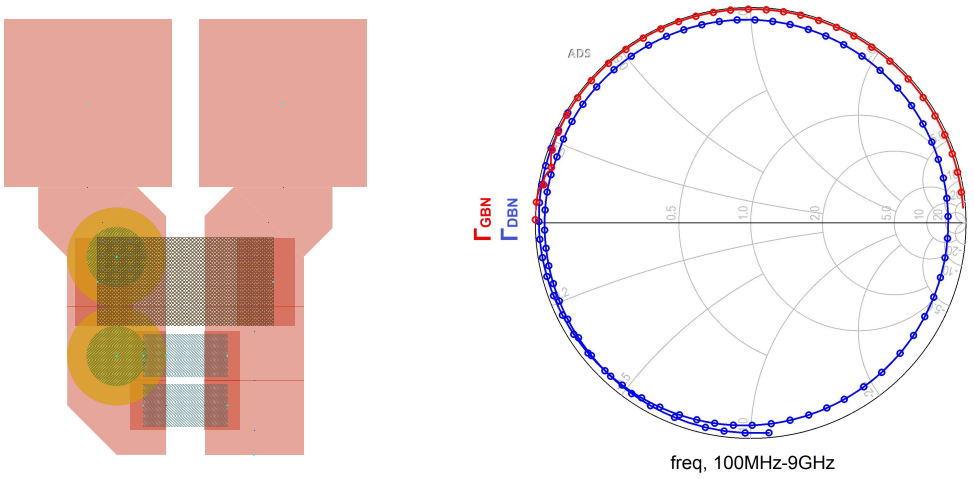
3.3 Design of the Bias Network

The purpose of the biasing network is to enable the user to apply a DC supply source to the amplifier without the RF energy leaking out through the bias port, which would degrade the RF performance of the device. The basic biasing network consists of a DC block and an RF choke, where the purpose is to present high impedance at the operating frequency to block the RF from leaking into the biasing network while acting as a DC short.

The biasing network could be designed as a standalone component or it could be designed as a part of the matching networks of the amplifier. The RF choke component of the bias network are left for the matching network optimizations in the later chapters, while the DC-block component of the bias network is presented in this section. The design is intended for easy soldering of the wires to the power supply and to act as a standalone component for both the DBN and the GBN. We also want to be able to use the amplifier in dynamic bias applications, and thereby the DC blocks must also be able to show a certain degree

of impedance at the bias port at the baseband frequency. Hence, assuming only optional dynamic drain biasing, the DBN and GBN are equivalent designs but differing only in the capacitors used in the design.

The bias networks consist of two 3.05mm by 3.05mm square IO solder pads for the DC supply and ground wire connections, and parallel transmission lines for soldering of the DC block capacitors. The transmission line width is determined by the fixed size of the via holes, and the spacing is determined by the physical size of the smallest capacitors. The transmission line length is determined by the width of two Johanson 0603 capacitors and one Murata 0805 capacitor. Two via holes are used to ensure a good connection to the ground plane. The bias network layout is shown in figure 3.6a with the 0805 Murata capacitor and the two 0603 Johanson capacitors. The capacitors used in the OMN are the 15pF and 18pF Johanson capacitors, while the IMN uses an additional 1µF Murata capacitor. The reflection coefficients of these networks are shown in figure 3.6b.



(a) (b)

Figure 3.6: (a) The bias network layout with both the Murata and Johanson capacitors, and (b) the reflection coefficients of the DBN and GBN.

3.4 Summary

In this chapter the selected transistors and an excerpt of their characteristics have been presented. The PDK model of the transistor has been modified to conform to the layout restrictions from the design space, where both the new simulation schematic model and lay-

out model have been presented. The substrate characteristics and restrictions attributed by the heatsink design have been presented, and the available SMD components, connectors and transistor clamps have been presented. Lastly the design of the biasing networks used throughout the design is presented and its characteristics evaluated. As described, the DBN primarily assumes a dynamic bias application, but in the case of a static bias the additional Murata capacitor could be included to ensure stability of the amplifier.

Power Amplifier stage design

Chapter 4

Power Amplifier Stage design

In this chapter we will go through the entire design process of the power amplifier stage, from the characterization of the transistor to both small-signal and large-signal analysis and matching network design. The I-V characteristics of the transistor will be used as an initial evaluation of its performance and to set the desired operation conditions of the transistor; the small-signal analysis will be used to ensure unconditional stability and to adjust the small-signal gain; and the large-signal analysis will be used to evaluate the performance of the transistor while designing the matching networks. The matching network design will primarily be based on the optimization results from the loadpull and sourcepull simulations.

4.1 Transistor loadline analysis

The I-V characteristics of the CGH40010F transistor are simulated by using the simulation setup shown in figure A.1 in the appendix, and the results are shown in figure 4.1. Superimposed on the I-V characteristics is the maximum power dissipation curve, given by the power dissipation de-rating curve in the datasheet [29] and noted in table 3.1. The CGH40010F transistor offer a general purpose broadband solution when operating from a 28V rail, thus a quiescent voltage bias of $V_{DSQ} = 28V$ is desired in this design. From the I-V characteristics it is evident that the knee voltage of the transistor is $V_{knee} = 5V$, thereby limiting the drain-source AC voltage swing and determining the maximum drain-source voltage, for linear class A operation. The class A loadline of the transistor is then determined by the maximum drain-source voltage and the maximum drain current at the knee voltage, as

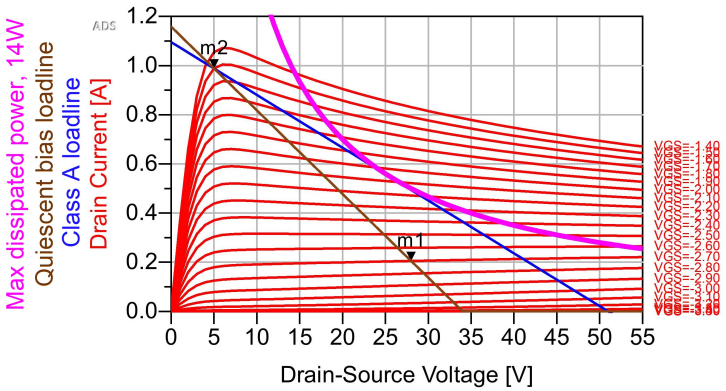


Figure 4.1: I-V characteristics of the CGH40010F transistor with superimposed maximum power dissipation, class A loadline, and loadline at quiescent bias m1.

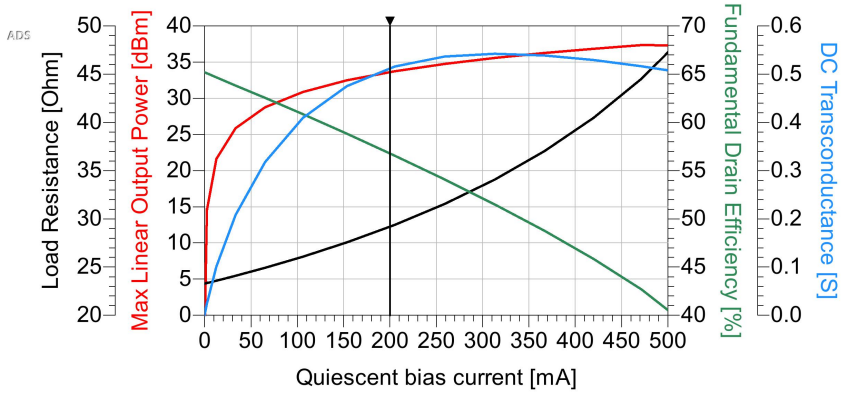


Figure 4.2: Maximum linear output power, fundamental drain efficiency and DC transconductance versus quiescent bias currents between class A and class B.

Table 4.1: I-V Properties of the CGH40010F transistor at the selected quiescent bias.

Property	Symbol	Min.	Q	Max.	Unit	Condition
Drain-Source Voltage	V_{DS}	5	28	51	V	
Drain Current	I_D	0	0.2	1	A	
Gate-Source Voltage	V_{GS}	-3.40	-2.7	-2.15	V	$V_{DS} = 28V$
Loadline Resistance	R_{load}	23^B	28.75	46^A	Ω	$V_{DS} = 28V$
Max Linear Output Power	$P_{out,lin}$	-	27.6	37.6^A	dBm	$V_{DS} = 28V$
DC Power Consumption	P_{DC}	8.913^B	10.154	14.0^A	W	$V_{DS} = 28V, P_{out,max}$
Drain efficiency	η_D	41.1^A	56.6	64.5^B	%	$V_{DS} = 28V, P_{out,max}$
DC transconductance	$g_{m,DC}$	0	0.52	0.55	S	$V_{DS} = 28V$

^{A}Class A operation, ^{B}Class B operation

shown in figure 4.1. By evaluating the maximum linear output power, drain efficiency and DC transconductance for each current bias between class A and class B as shown in figure 4.2, a desired quiescent current bias can be selected. Evidently, class A operation exhibits maximum linear output power and minimum drain efficiency, and vice versa for class B operation, while the higher class AB operations exhibit the greatest DC transconductance. The desired quiescent current bias is set to 200mA, shown by marker m1 in figure 4.1 and the vertical marker in figure 4.2, and the properties of the CGH40010F transistor from the loadline analysis are summarized in table 4.1.

4.2 Stability analysis

4.2.1 Small-signal stability

The stability of the CGH40006P transistor can be evaluated in accordance with Rollet's stability conditions through the $K-\Delta$-test, and the geometric load and source stability factors, μ_{load} and μ_{source}. By using the S-parameter simulation setup shown in figure A.2 in the appendix, the stability at a specific quiescent bias can be calculated. The stability factors shown in figure 4.3 are calculated at the most unstable bias of the transistor, at $I_{DQ} = 33mA$, and the corresponding source and load stability circles for the frequency range are plotted in figure 4.4. From the plots we can see that the transistor is potentially unstable at all frequencies below 16GHz, and especially below 2GHz. Hence a stabilization network is necessary to ensure unconditional stability.

At the higher frequencies we observe that the stability circles merely touch the outer edge of the smith chart, which can be adjusted by introducing a small loss at these frequencies. However at the lower frequencies the protrusion of the stability circles in the smith chart are larger, thereby requiring a greater loss. Additionally the protrusion at these frequencies is predominantly inductive. From the stability factors we also note the effect of a resonance close to the 10-12GHz frequencies, which can be reduced by using a lossy feedback stabilization network. The source terminal of the transistor is already connected directly to the ground through the flange of the package and the aluminium plate, thus making

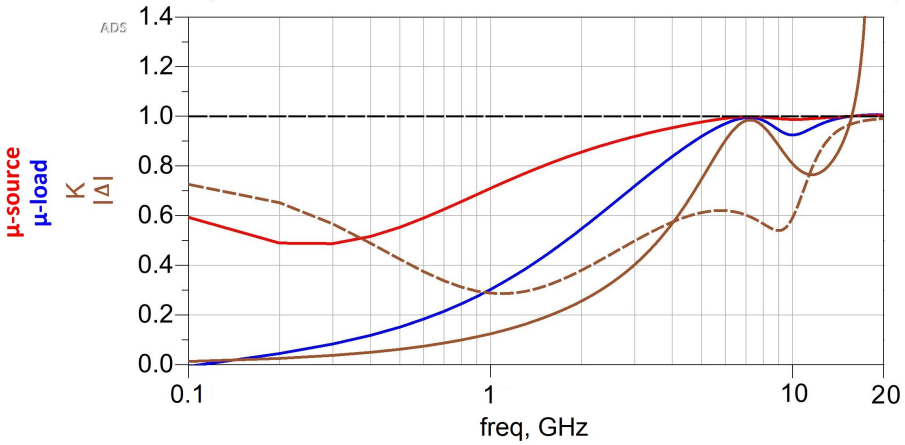
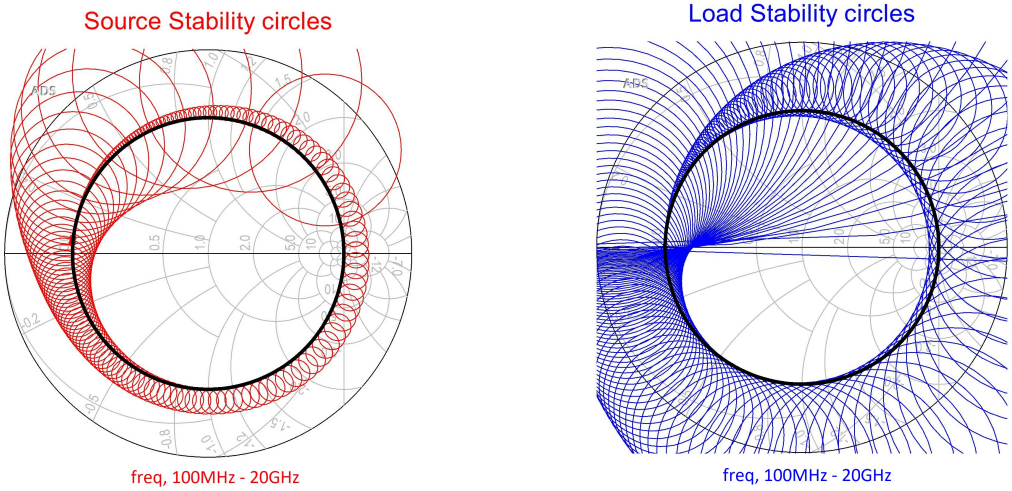


Figure 4.3: The stability factors of the CGH40010F transistor at $I_{DQ} = 33mA$.



(a) (b)

Figure 4.4: The (a) source and (b) load stability circles at $I_{DQ} = 33mA$.

a stabilization network at the source terminal unfeasible. A lossy stabilization network on the drain terminal would increase the DC power requirements and lower the RF output power, which is undesirable. A feedback stabilization network between the drain and gate terminal reduces the effects of the harmonic pole, but is not sufficient to ensure unconditional stability. However a stabilization scheme of a series resistor with a bypass capacitor for the higher frequencies at the gate terminal displayed the desired stabilization behavior and simplicity for the stabilization network, even though the effects of the harmonic pole was still prominent at the aforementioned frequencies.

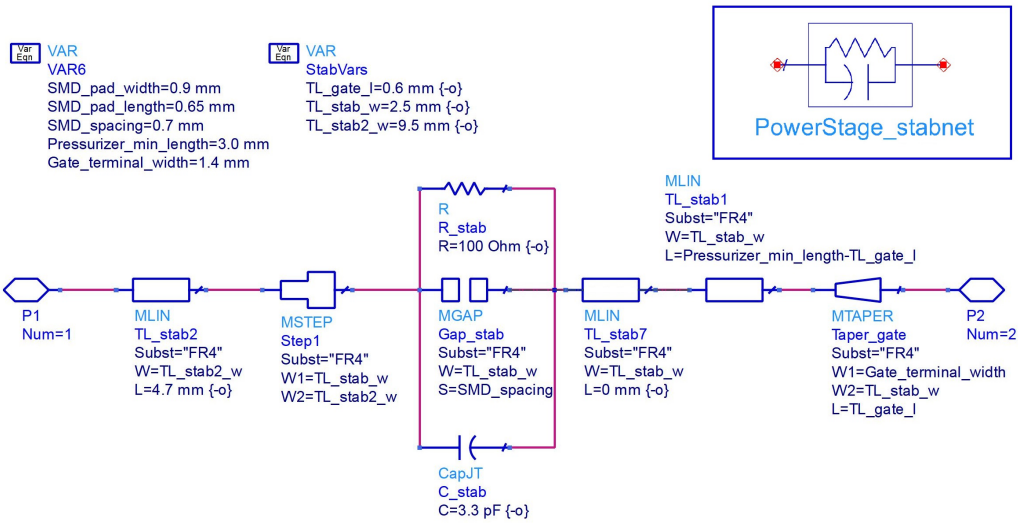


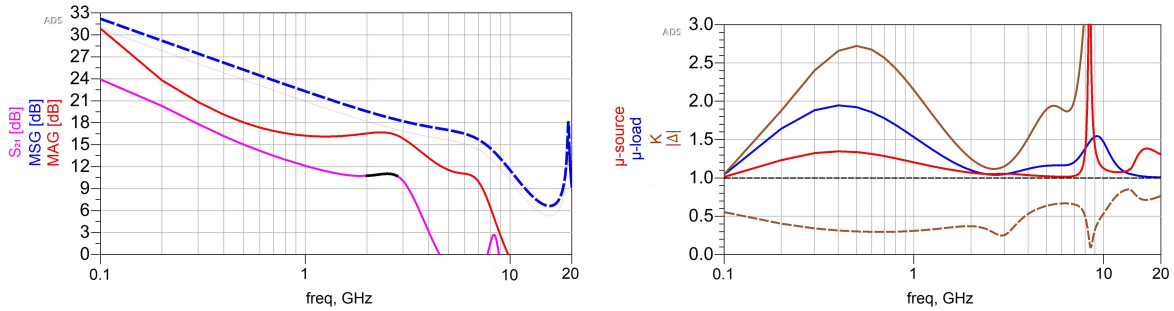
Figure 4.5: Simulation schematic of the stabilization network for the CGH40010F transistor.

4.2.2 Stabilization Network

The stabilization network is set up as shown in the simulation schematic in figure 4.5. In order to use the clamps shown in figure 3.5a, the components cannot be soldered closer than 3mm from the transistor casing. Hence a transmission line with a minimum length of 3mm must be used between the transistor casing and the components. The gate terminal tab of the transistor is 1.4mm wide and 2.05mm long, restricting the minimum transmission line width at the gate side to be greater than 1.4mm. The minimum pad width for the surface mount components is 0.9mm, thus restricting the transmission line width at each side of the resistor and capacitor to be greater than 1.8mm. The minimum pad length for the surface mount components is 0.65mm, thereby also limiting the minimum transmission line length at each side.

4.2.3 Stability and small-signal gain optimization

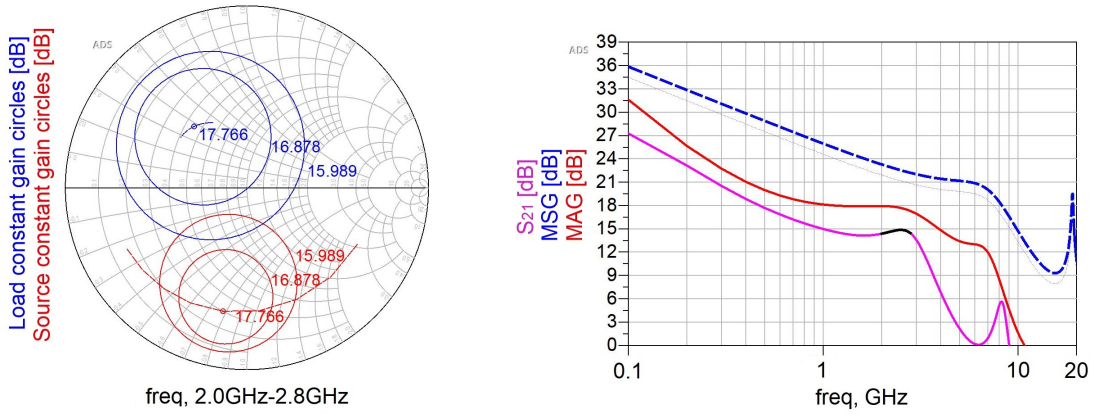
The simulation setup shown in figure A.2 was then used to optimize the stabilization network for stability over the whole frequency range and maximum flat small-signal gain in the frequency band, while the load impedance was set to the corresponding loadline resistance of 28.75Ω. The geometric stability factors were restricted to be greater than 1 to ensure that the stability circles were outside the smith chart; and the K-factor was restricted to $K > 1.05$ to ensure that the Maximum Available Gain (MAG) did not exceed the Maximum Stable Gain (MSG), and to establish a minimum degree of stable gain. The small-signal gain, S_{21}, was



(a) (b)

Figure 4.6: The (a) small-signal gain and (b) stability factors of the CGH40010F transistor with the stabilization network at $I_{DQ} = 33mA$.

subsequently maximized while maintaining its flatness in the frequency band. The result of the optimization is shown in figure 4.6a, and the corresponding stability factors are shown figure 4.6b. Evidently the transistor is unconditionally stable over the frequency range when biased at the most unstable quiescent bias. When changing the bias back to the desired quiescent bias of $I_{DQ} = 200mA$, the simulation results in the characteristics in figure 4.7. The small-signal gain in the frequency band is 13.669-14.200dB, and the MAG and MSG at the center frequency are 17.766dB and 22.662dB respectively. The constant matched gain circles for the source and load at the center frequency, including the MAG for each frequency in the frequency band, are shown in the smith chart. Noticeably the MAG load impedance match is confined within a relatively small region of the smith chart, while the MAG source impedance match traverse a more extensive portion of the smith chart. Thus a good impedance match



(a) (b)

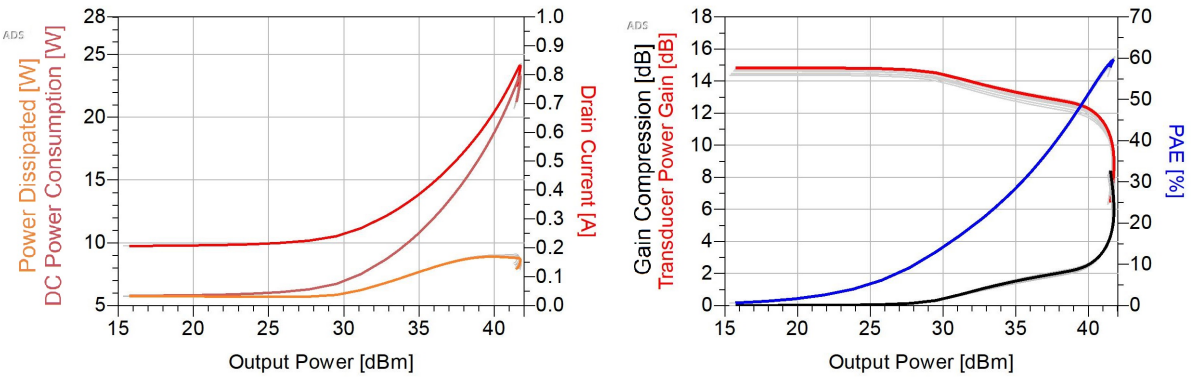
Figure 4.7: (a) Constant matched gain circles and (b) small-signal gain at $I_{DQ} = 200mA$.

for the MAG over the frequency band can be achieved at the load, but will be more difficult to accomplish at the source.

4.3 Large-signal analysis

4.3.1 Large-signal characteristics

The large-signal characteristics of the stabilized transistor can be calculated by using the harmonic balance simulation setup shown in figure A.3 in the appendix; using the quiescent bias at $V_{DSQ} = 28V$ and $I_{DQ} = 200mA$, and setting the load impedance to the corresponding loadline resistance of 28.75Ω. The results of the simulation are shown in figure 4.8 and summarized in table 4.2.



(a) (b)

Figure 4.8: (a) Power Dissipated, DC Power Consumption and Drain Current, and (b) Transducer Power Gain, Gain compression and PAE of the stabilized transistor, for the frequency range 2.0-2.8GHz, highlighting the center frequency of 2.4GHz.

Table 4.2: Properties of the stabilized transistor in accordance with the large-signal characteristics in figure 4.8

Parameter	Symbol	Value	Unit
Saturated Output Power	P_{sat}	41.8	dBm
Transducer Power Gain	G_t	14.6	dB
Peak PAE	PAE_{max}	60	%
Maximum Drain Current	$I_{D,max}$	830	mA
Maximum DC Power Consumption	P_{DC}	23.4	W
Maximum Dissipated Power	P_{diss}	9.1	W

4.3.2 Harmonic Loadpull

We want the load of the transistor to be terminated in a 50Ω-load and thus need an output matching network that can transform the load impedance to the preferred output impedance of the transistor. By using the HLP simulation setup shown in figure A.4 in the appendix and adjusting the reflection coefficients of the *LoadPullTB* component, we can find the optimal output impedances for e.g transducer power gain, PAE and delivered output power for each frequency in the frequency band. When the source is terminated in a 50Ω impedance, the optimal impedances for the center and outer frequencies for each of the aforementioned parameters are as shown in figure 4.9. The corresponding properties for each optimal impedance are presented in table 4.3.

From figure 4.9 we observe that the optimal impedances for delivered output power ($Z_{opt.Pdel}$) are close to the real axis at the value corresponding to the loadline resistance at the quiescent bias. The optimal load impedances for transducer power gain ($Z_{opt.Gt}$) are slightly more resistive and have a larger inductive component than the $Z_{opt.Pdel}$ impedances. The optimal impedances for PAE ($Z_{opt.PAE}$) also have the same resistance, but have a greater inductivity. Another observation is that all the optimal impedances describe a non-Foster circuit in the smith chart, where the larger inductive component seems to cause a larger

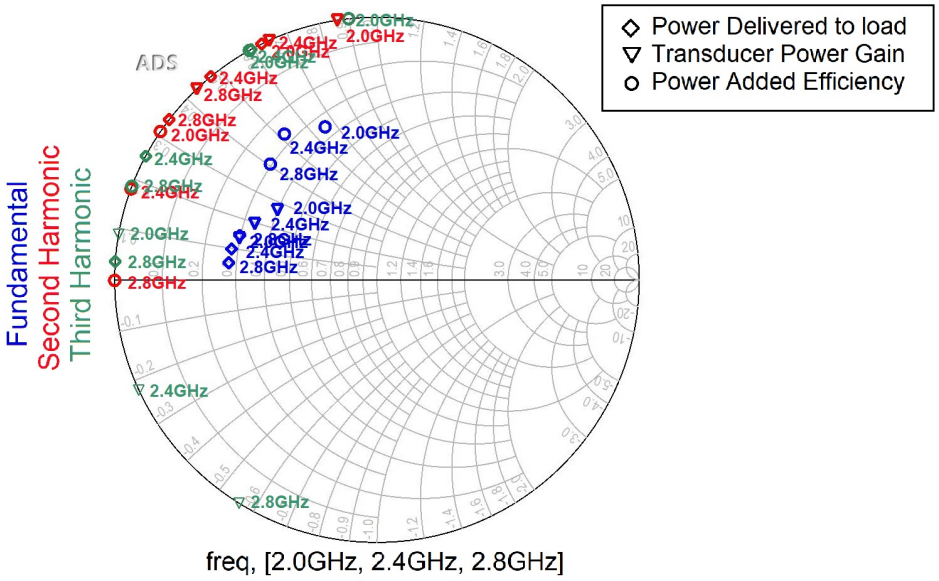


Figure 4.9: Optimal Harmonic Loadpull data for Power delivered, Transducer Power Gain and PAE at 2.0GHz, 2.4GHz and 2.8GHz.

step size between the optimal impedances. Hence, matching for a large bandwidth would e.g. be more difficult when using the $Z_{opt.PAE}$ rather than the $Z_{opt.Pdel}$. Also, since the matching network only uses passive components, it must act like a Foster matching network, tracing an impedance path in the clockwise direction. Since the optimal harmonic impedances of $Z_{opt.PAE}$ are located in a counter-clockwise direction relative to the optimal fundamental impedances, a good impedance match is difficult. However, the optimal harmonic impedances of both $Z_{opt.Pdel}$ and $Z_{opt.Gt}$ are located clockwise relative to the optimal fundamental impedances.

From table 4.3 we can see that the sensitivity of the transducer power gain is relatively low, with only 1.422dB maximum deviation. Contrary, the sensitivity of the PAE and power delivered are greater with 12.452 percentage points and 3.805dB deviation respectively. From these data the desired optimization goal and restrictions are set to

$$G_t > 14.5dB; \qquad P_{sat} > 41.5dBm; \qquad max(PAE). \tag{4.1}$$

The desired load impedances from the HLP simulation using these optimization goals are shown in figure 4.10, and as expected the desired load impedances are close to the $Z_{opt.Pdel}$ and $Z_{opt.Gt}$ impedances. The corresponding properties are presented in table 4.4. The fundamental, 2nd and 3rd harmonic loadpull contours for the transducer power gain and PAE are shown in figure 4.11 through 4.13, where the samples not fulfilling the desired power

Table 4.3: The Transducer Power Gain, PAE and Power delivered to the load, when the load impedances are matched to the optimal load impedances for the center and outer frequencies.

Parameter	Values			Unit	Optimization
Frequency	2.0	2.4	2.8	GHz	
Transducer Power Gain	**14.649**	**15.138**	**14.759**	dB	**Opt. Gain**
	13.896	14.369	14.235	dB	Opt. PAE
	14.304	14.877	14.604	dB	Opt. Pdel
Power Added Efficiency	75.668	75.060	73.466	%	Opt. Gain
	80.965	**79.245**	**78.121**	%	**Opt. PAE**
	69.141	68.941	68.513	%	Opt. Pdel
Power delivered	41.572	41.744	41.815	dBm	Opt. Gain
	38.743	38.771	39.782	dBm	Opt. PAE
	42.548	**42.473**	**42.409**	dBm	**Opt. Pdel**

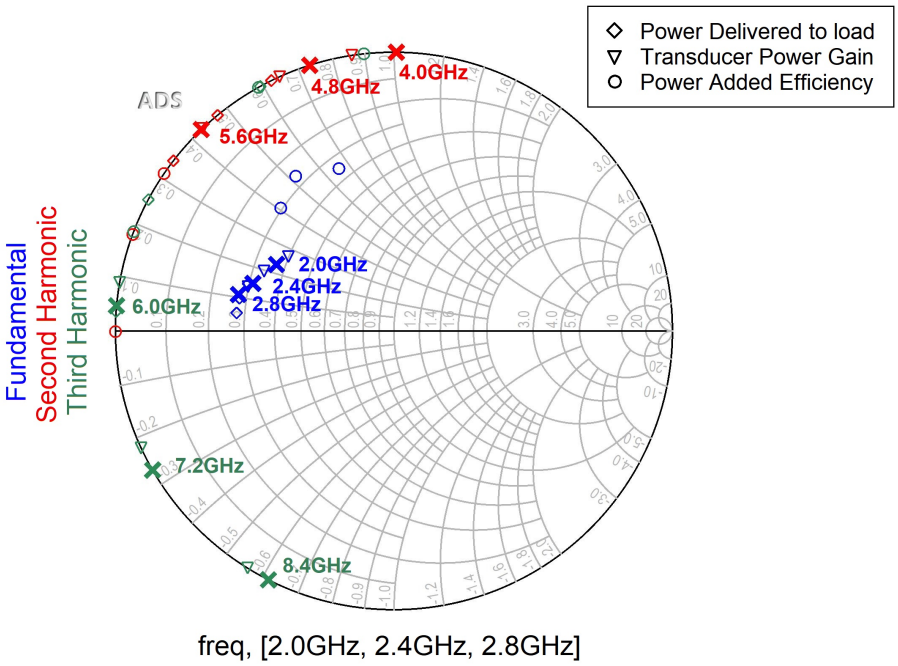


Figure 4.10: Desired load impedances, superimposed on the optimal impedances from figure 4.9.

Table 4.4: The Transducer Power Gain, PAE and Power delivered to the load, when the load impedances are matched to the desired load impedances for the center and outer frequencies.

Parameter	Values			Unit	Optimization
Frequency	2.0	2.4	2.8	GHz	
Transducer Power Gain	14.589	15.053	14.691	dB	Opt. desired
Power Added Efficiency	75.398	74.067	72.569	%	
Power delivered	41.863	42.061	42.041	dBm	

delivered are highlighted. The desired load impedance from the previous optimization is superimposed on the contour plot. During the fundamental loadpull the harmonic loads are terminated in the desired load impedances, and likewise for the fundamental and the other harmonic load during the harmonic loadpulls. As expected the sensitivity of higher harmonic terminations is decreasing, and is practically negligible after the third harmonic. Noticeably the valid region of the fundamental load impedance is quite small and the sensitivity is quite high, thus the fundamental load impedance match is critical. For the harmonic load impedance it is sufficient to remain within the first levels of the contour plots.

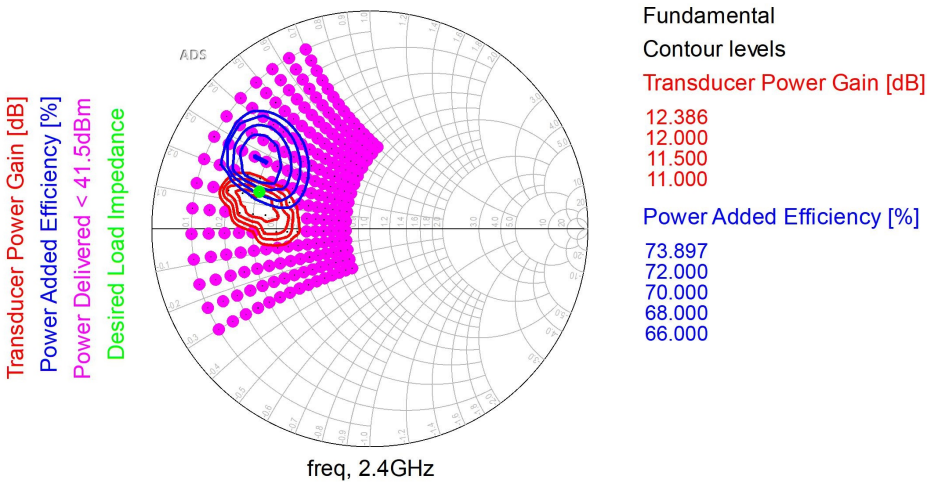


Figure 4.11: Fundamental loadpull contours for 41.5dBm desired power delivered at the center frequency, when terminated in the desired load impedances.

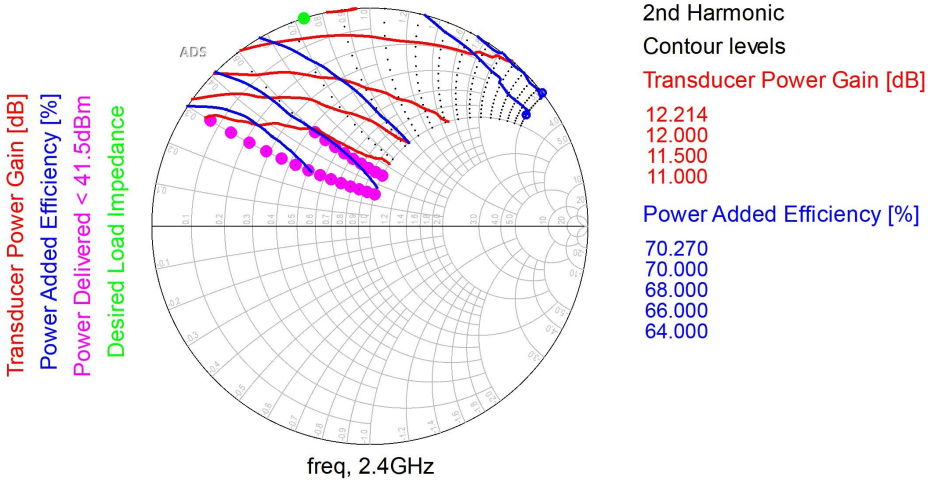


Figure 4.12: 2nd Harmonic loadpull contours for 41.5dBm desired power delivered at the center frequency, when terminated in the desired load impedances.

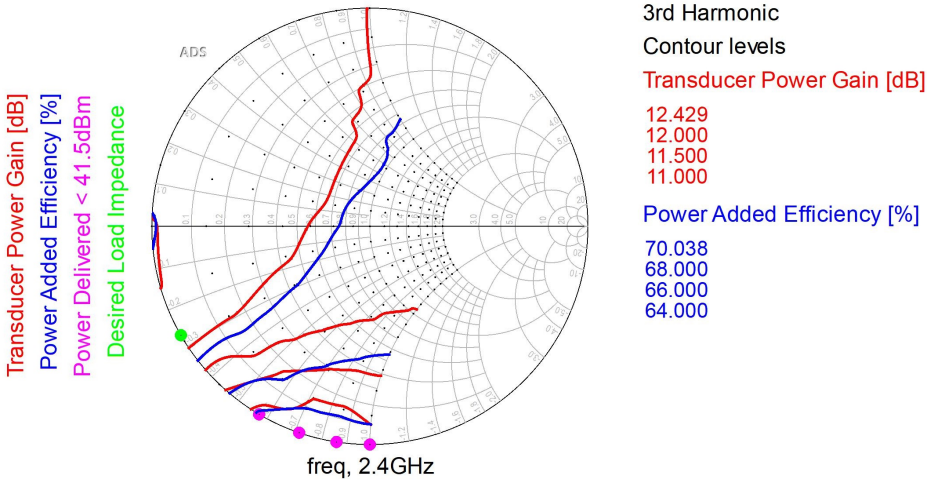
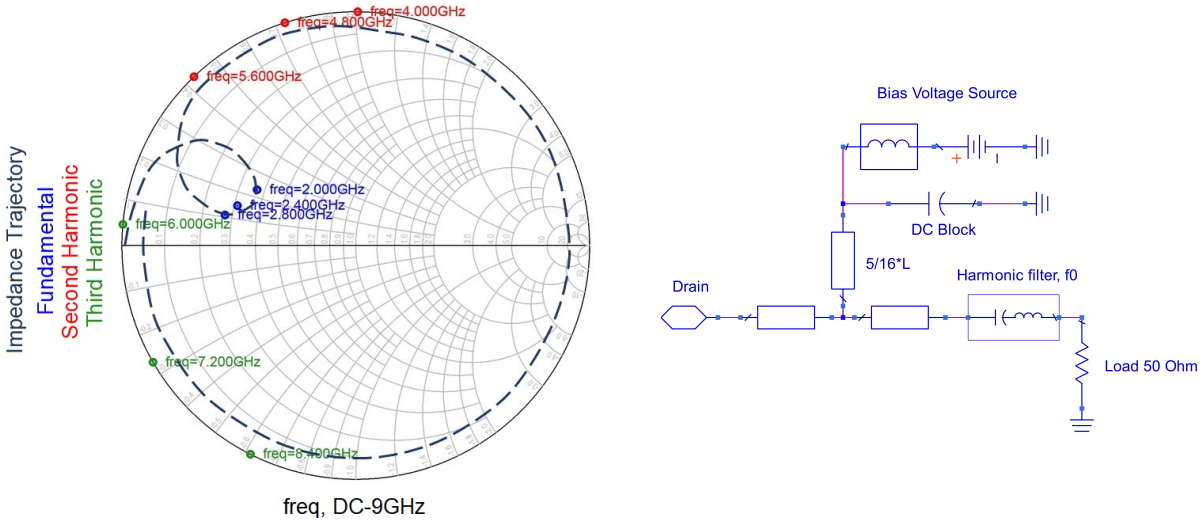


Figure 4.13: 3rd Harmonic loadpull contours for 41.5dBm desired power delivered at the center frequency, when terminated in the desired load impedances.

4.3.3 Output Network Impedance Trajectory

Now that the desired fundamental and harmonic load impedances, and the preferred sensitivity range, for the transistor are determined, the OMN can be designed according to these restrictions. We primarily only want the impedance trajectory to move inwards in the smith chart at the fundamental frequencies and remain at the outer edge of the smith chart for all the other frequencies. Thus, a twirl match is most suitable for the desired fundamental impedances. Since the desired harmonic load impedances are located at the edge of the smith chart and spaced widely, the most suitable matching technique for these impedances is a through match. Consequentially the load, modified by a proper matching network, should only be presented to the drain at the fundamental frequencies and otherwise be a high impedance load, while the bias network should be presented as a high impedance at the fundamental frequencies and otherwise be a low impedance load with proper phase according to the desired harmonic impedances. Subsequently, the desired impedance trajectory is shown in figure 4.14a, and the corresponding OMN schematic model is shown in figure 4.14b. The leftmost transmission line is the line out from the drain terminal, the $\frac{5}{16}\lambda$-line ensure the correct reactance for the harmonic frequencies, and the remaining transmission line and resonant tank for the fundamental frequency ensures the correct fundamental load impedance. The capacitor represents the DC block of the bias network.



(a) (b)

Figure 4.14: The (a) desired impedance trajectory and the (b) preliminary schematic, of the output matching network.

4.3.4 Design of the Output Matching Network

The OMN is set up as shown in the simulation schematic in figure 4.15 and is based on the preliminary schematic from figure 4.14b. The drain terminal of the transistor is 1.4mm wide and 2.05mm long. Thus the transmission line width from drain terminal must be greater than 1.4mm, but the length of the transmission line is not limited by the length of the terminal as long as the bias tee is large enough. However, the bias tee should be at least 1mm from the transistor to prevent coupling. The taper angle of the transmission lines is restricted to be less than 45 degrees and the DBN is set to a fixed distance of 11mm from the transistor drain terminal. The shunt stub at the bias tee is used as a supplement for the transmission line to the DBN in order to provide the desired harmonic termination. The remaining transmission lines are a part of the load impedance transformation from 50Ω to the desired fundamental load impedances.

The OMN is optimized using the network optimization simulation setup shown in figure A.5 in the appendix, where the distance between the input OMN impedance and the desired load impedances is minimized. The outcome of the optimization is shown in figure 4.15 and the corresponding impedance trajectory, along with the desired load impedances, is shown in figure 4.16. Evidently the fundamental load impedances are closely matched with the desired fundamental load impedances. By comparing the OMN harmonic load impedances to the HLP contours in figure 4.12 and 4.13 we see that they are matched well within a couple of contour levels. The second harmonic network impedances seem to cause the most mis-

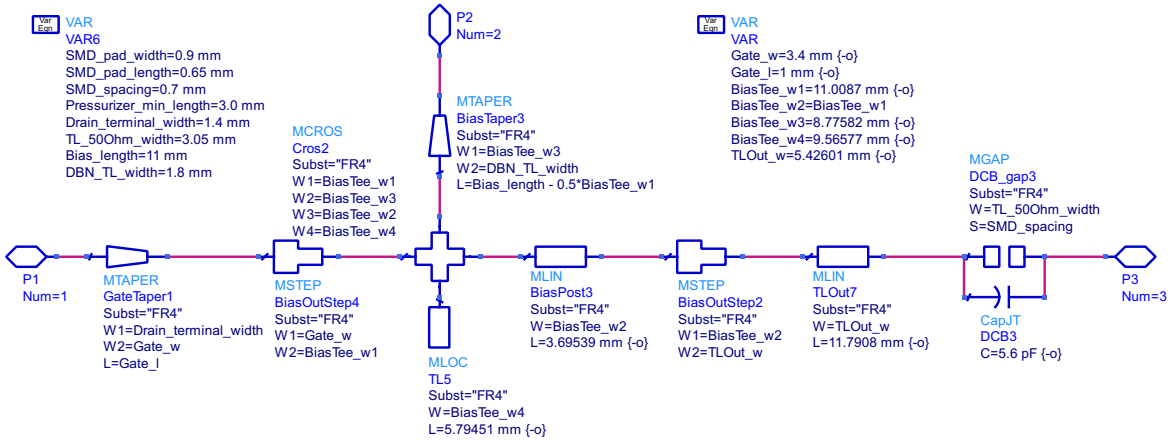


Figure 4.15: Schematic simulation model of the OMN.

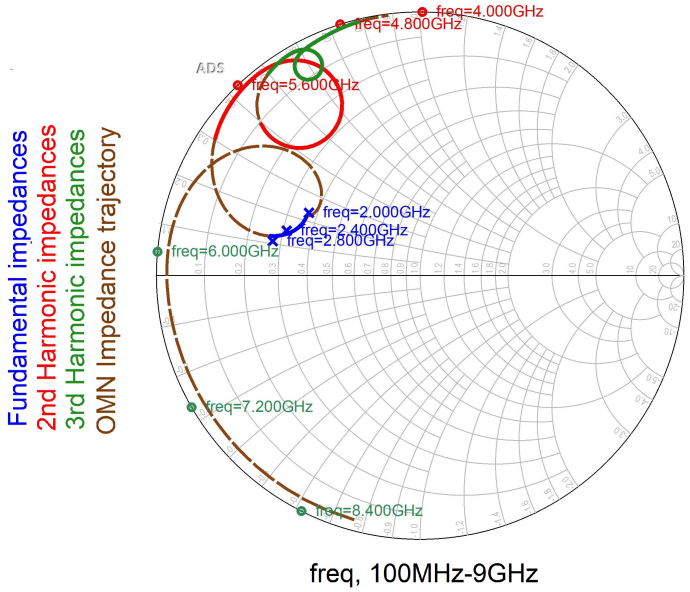
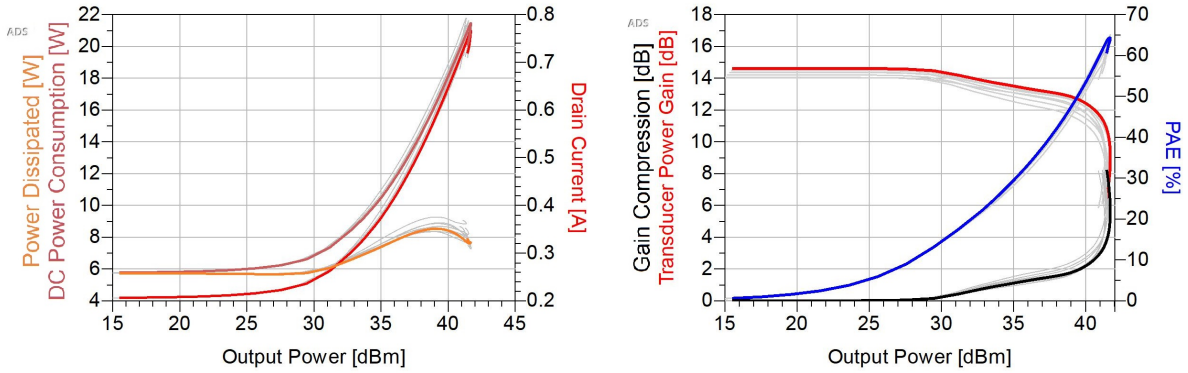


Figure 4.16: OMN impedance trajectory match for the desired load impedances from the OMN network in figure 4.15.

match, although within 1dB gain and a couple percentages of PAE. The large-signal characteristics of the stabilized transistor with the OMN are shown in figure 4.17. Compared to the plots in figure 4.8 the PAE has increased with five percentage points, the maximum drain current has reduced by 50mA and the DC power consumption has decreased by 1W, but the transducer power gain became less flat over the frequency band at the higher output powers and the variance of the saturated output power has increased a little.



(a) (b)

Figure 4.17: (a) Power Dissipated, DC Power Consumption and Drain Current, and (b) Transducer Power Gain, Gain compression and PAE of the stabilized transistor with OMN, for the frequency range 2.0-2.8GHz, highlighting the center frequency of 2.4GHz.

4.3.5 Harmonic Sourcepull

Now that we have a real network at the output of the transistor, a Harmonic Sourcepull (HSP) can be performed using the same simulation setup as for the HLP shown in figure A.4; where the *LoadpullTB* is replaced by the OMN. The same goals as during HLP are used during the optimization. The desired source impedances from the optimization are shown in figure 4.18 for the fundamental frequencies only, as the harmonic impedances had a negligible effect on the performance. Evidently the desired source impedances are spread widely over the smith chart and in the counter-clockwise direction, which sets the premise for an unattainable optimal source impedance match over the frequency band. Thus, a compromise must be made to accommodate a satisfactory performance. From the fundamental sourcepull contours in figure 4.19 through 4.21, the maximum PAE and maximum transducer power gain are located at similar source impedances. By comparing the optimal source impedances to a 50Ω termination, a roughly estimated difference of 1dB in transducer power gain and 5 percent PAE. Considering that the loadpull optimization was performed with a 50Ω source termination and that a compromise must be made between the optimal source impedances, the impedance trajectory of the IMN will probably pass within the proximity of the center of the smith chart in order to get the desired performance.

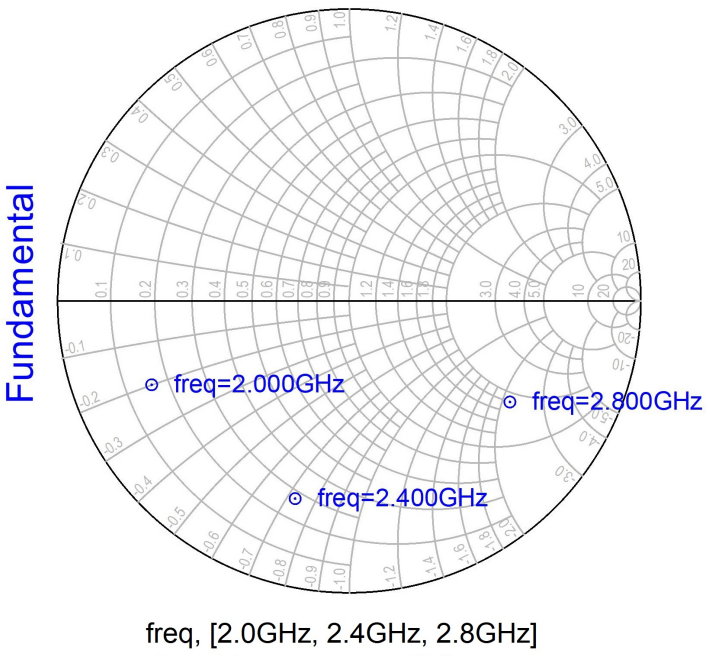


Figure 4.18: Desired source impedances of the of the driver stage.

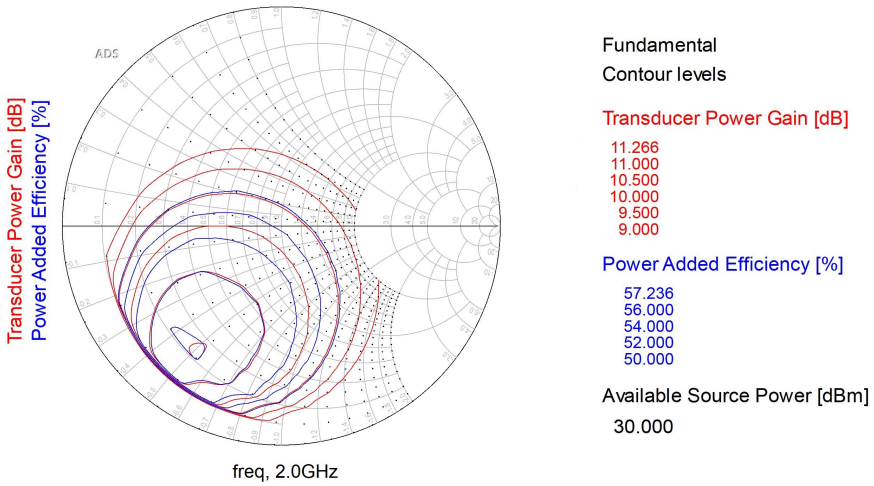


Figure 4.19: Fundamental sourcepull contours for 30dBm available source power at 2.0GHz.

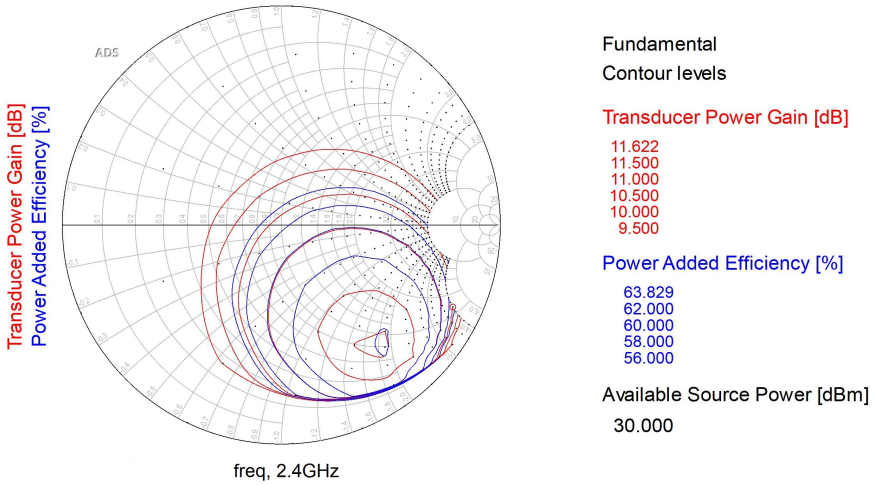


Figure 4.20: Fundamental sourcepull contours for 30dBm available source power at 2.4GHz.

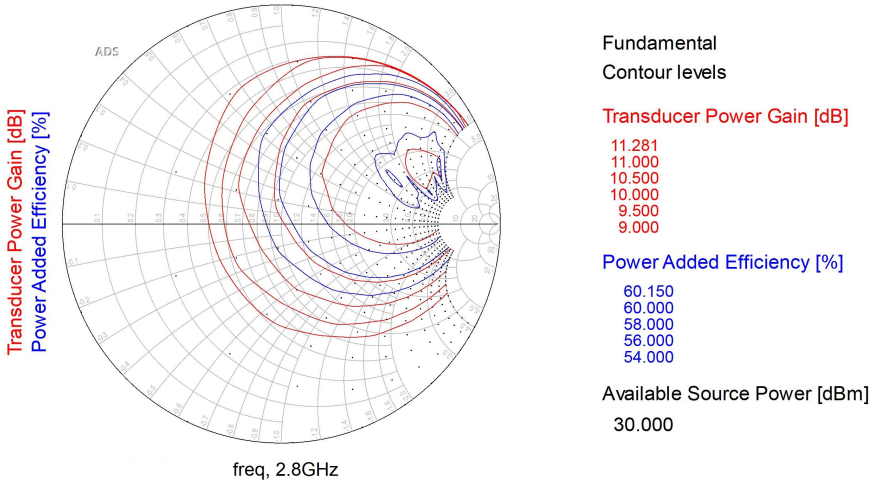


Figure 4.21: Fundamental sourcepull contours for 30dBm available source power at 2.8GHz.

4.3.6 Design of the Input Matching Network

The IMN is set up as shown in the simulation schematic in figure 4.22 and is designed to be as simple as possible with the intent of mainly providing bias and RF inputs, but also to provide some degree of impedance matching. The IMN was optimized using the harmonic balance simulation setup shown in figure A.3 in the appendix, where the GBN was set at a fixed distance from the transistor gate terminal. The transmission line to the GBN used the transmission line width of the GBN, and a tapered transmission line was used to match the width of the stabilization network transmission line. The IMN was optimized for gain flatness in the frequency band, for input powers of 17dBm and 32dBm, simultaneously. The outcome of the optimization is shown in the simulation schematic in figure 4.22 and the corresponding IMN impedance trajectory, along with the desired fundamental source impedances, is shown in figure 4.23. Noticeably the fundamental IMN impedances are confined to a small region near 50Ω in the inductive part of the smith chart, rather than closer to the desired source impedances in the capacitive part of the smith chart.

To see the operating class of the transistor we can look at the impedances presented in the internal nodes of the transistor as shown figure 4.24. The impedances reminds of an inverse class F where the fundamental has a real impedance, the second harmonic is open circuited and the third harmonic is short circuited, but where the fundamental impedances are shifted into the inductive half plane and the harmonic impedances are shifted into the capacitive half plane. Some impedances seem to be located outside of the smith chart, but this is most likely due to current sources within the model causing the appearance of negative resistance.

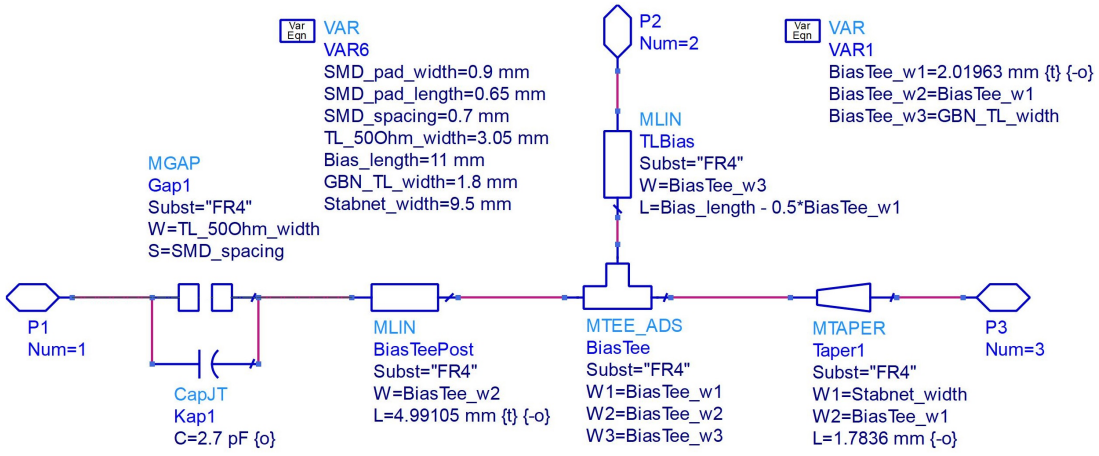


Figure 4.22: The simulation schematic of the power stage IMN.

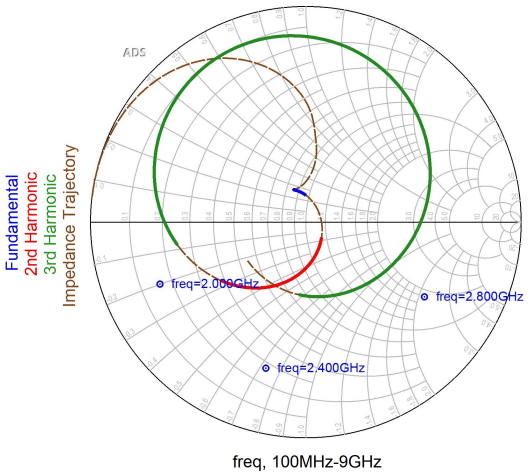


Figure 4.23: Impedance trajectory of the IMN of the power stage.

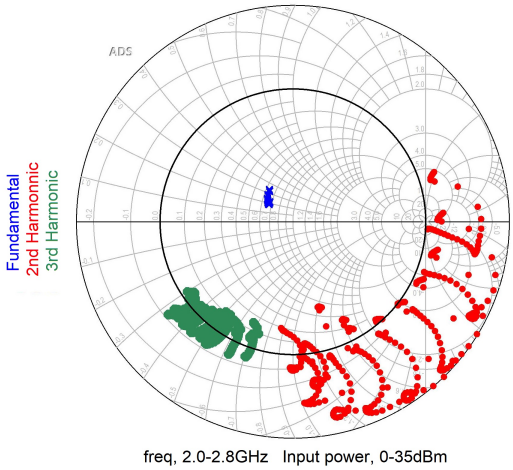
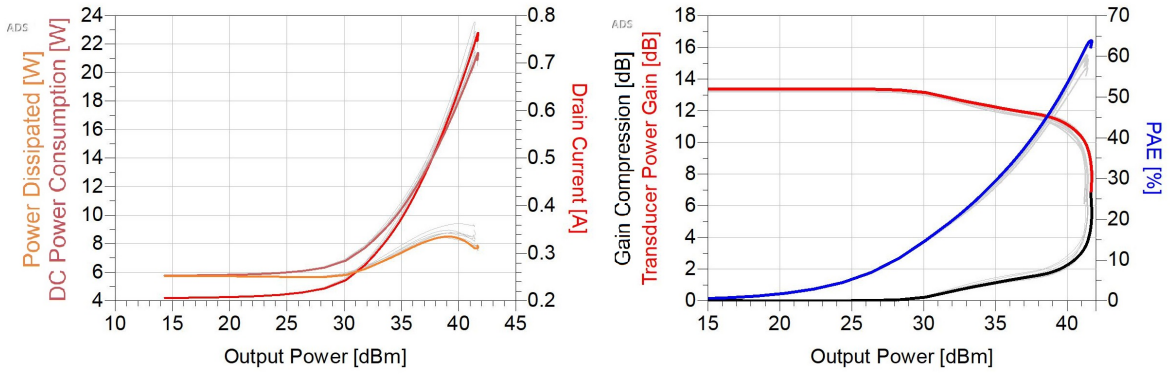


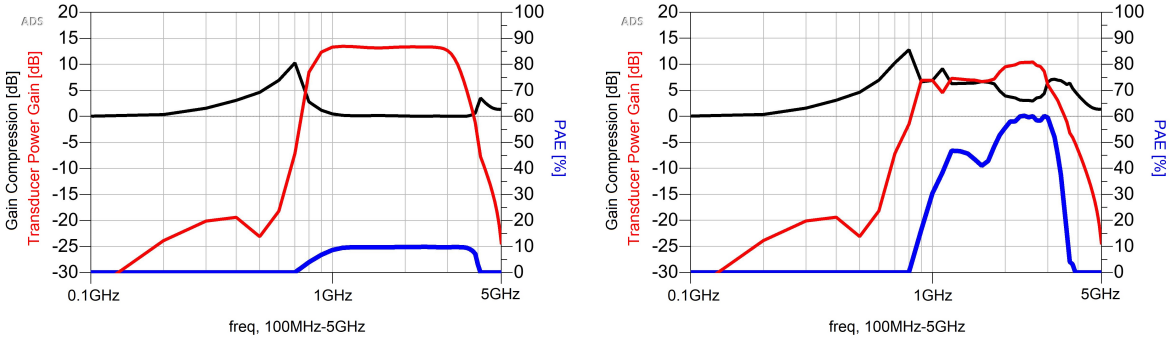
Figure 4.24: Impedances presented to the intrinsic nodes of the transistor.

From the large-signal characteristics shown in figure 4.25 we see that the transducer power gain has dropped to 13.35dB at the lower output powers, but deviates less than 0.5dB over the frequency band, up to the saturated output power. The mean saturated output power is greater than 41.5dBm, ranging from 41.2dBm to 41.7dBm; and the mean peak PAE is 61.25%, ranging from 57.2% at the edge of the frequency band to 64% in the center of the frequency band. The maximum drain current is 780mA and the maximum dissipated power is less than 9.4W. As shown in figure 4.26a, the transducer power gain is 13.5dB in the 1-3GHz range for linear operations (less than 28dBm output power), and at 41dBm desired output power the frequency band is in the 2.0-2.8GHz range with an efficiency of 60%. The resulting layout of the power stage is shown in figure 4.27.



(a) (b)

Figure 4.25: (a) Power Dissipated, DC Power Consumption and Drain Current, and (b) Transducer Power Gain, Gain compression and PAE of the power stage, for the frequency range 2.0-2.8GHz, highlighting the center frequency of 2.4GHz.



(a) (b)

Figure 4.26: The transducer power gain, gain compression and PAE for (a) 28dBm and (b) 41dBm desired output power, from 100MHz to 5GHz.

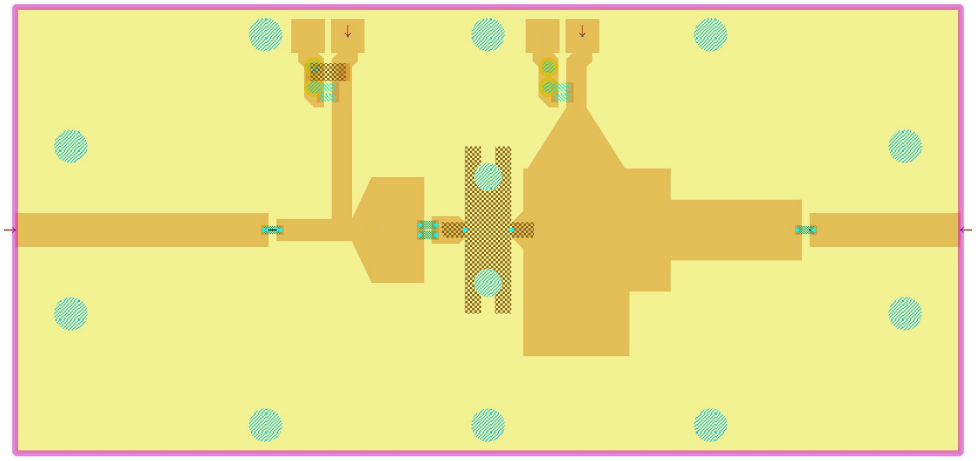


Figure 4.27: Layout of the Power stage.

4.4 Summary and discussion

In this chapter we went through the design process of the power amplifier stage, looking at stability, small-signal and large-signal characteristics. From figure 4.26 we can see that a much greater bandwidth was attained, expanding at frequencies below the intended frequency band. However, the expanded frequency band is only flat for linear operations. When the input power is greater than 28dBm the expanded frequency band collapses at the additional frequencies, but is not entirely attenuated. Hence, the additional frequency band is not optimized well and one could either extend the impedance matching to make the transducer power gain flat also in the extended frequency band at higher input powers, or one could restrict the impedance matching in order to attenuate the transducer power gain at the additional frequencies. By taking a closer look at the OMN impedance trajectory matching of the desired load impedances we can see an abrupt impedance change in the path at 2.0GHz, which may have resulted in a better than intended impedance match at the frequencies below 2.0GHz. By designing a matching network with only a single twirl as presented in the desired impedance trajectory in figure 4.14a without the extra twirls as in the established OMN, the transducer power gain could have been more similar to the desired gain.

Driver Amplifier stage design

Chapter 5

Driver Amplifier stage design

In this chapter we will go through the entire design process of the driver amplifier stage, from the characterization of the transistor to both small-signal and large-signal analysis and matching network design. The same design procedure as in the previous chapter will be used. Hence, the design choices and simulation results from the driver amplifier stage design will continuously be compared to the design choices and simulation results from the power amplifier stage design.

5.1 Transistor loadline analysis

The I-V characteristics of the CGH40006P transistor is simulated by using the simulation setup as shown in figure A.1 in the appendix, and the results are shown in figure 5.1. Superimposed on the I-V characteristics is the maximum power dissipation curve, given by the power dissipation de-rating curve in the datasheet [28] and noted in table 3.2. The driver stage is integrated into the same application as the power stage from the previous chapter, and thus uses the same rail voltage and quiescent voltage of $V_{DSQ} = 28V$. From the I-V characteristics it is evident that the knee voltage of the transistor is $V_{knee} = 5V$; the same as for the power stage. Hence, the voltage operating range is also the same. The maximum power dissipation is less than for the CGH40010F transistor thereby resulting in a lower maximum drain current. The I-V properties of the CGH40006P transistor for each current bias between class A and class B are shown in figure 5.2. To ensure that the driver stage operates linearly until the

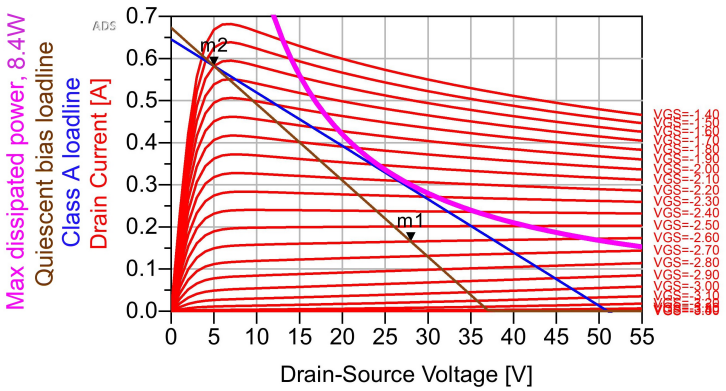


Figure 5.1: I-V Characteristics of the CGH40006P transistor with superimposed maximum power dissipation, class A loadline and loadline at the desired quiescent bias at marker m1.

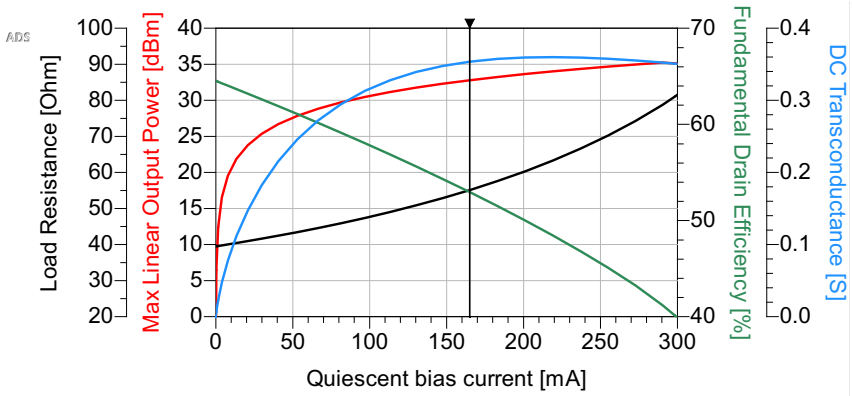


Figure 5.2: Maximum linear output power, fundamental drain efficiency and DC transconductance versus quiescent bias currents between class A and class B.

Table 5.1: I-V Properties of the CGH40006P transistor at the desired quiescent bias.

Property	Symbol	Min.	Q	Max.	Unit	Condition
Drain-Source Voltage	V_{DS}	5	28	51	V	
Drain Current	I_D	0	165	600	mA	
Gate-Source Voltage	V_{GS}	-3.40	-2.60	-2.25	V	$V_{DS} = 28V$
Loadline Resistance	R_{load}	38.074^B	52.873	76.667^A	Ω	$V_{DS} = 28V$
Max Linear Output Power	$P_{out,lin}$	-	32.781	35.378^A	dBm	$V_{DS} = 28V$
DC Power Consumption	P_{DC}	5.348^B	6.469	8.4^A	W	$V_{DS} = 28V, P_{out,max}$
Drain efficiency	η_D	41.1^A	53.3	64.5^B	%	$V_{DS} = 28V, P_{out,max}$
DC Transconductance	$g_{m,DC}$	0	0.354	0.36	S	$V_{DS} = 28V$

^{A}Class A operation, ^{B}Class B operation

power stage goes into saturation, the maximum linear output power must be greater than 30dBm. The desired quiescent current bias is set to the peak of the product of the properties ($P_{out,lin.max} \cdot \eta_D \cdot g_{m,DC}$) at 165mA shown by marker m1 in figure 5.1 and the vertical marker in figure 5.2. The I-V properties of the transistor operating at the desired quiescent bias are summarized in table 5.1. Noticeably the loadline resistance at the desired quiescent bias is close to 50Ω.

5.2 Stability analysis

5.2.1 Small-signal stability

The stability of the CGH40006P transistor can be evaluated in accordance with Rollet's stability conditions through the $K-\Delta$-test, and the geometric load and source stability factors, μ_{load} and μ_{source}. By using the S-parameter simulation setup shown in figure A.2 in the appendix, the stability factors at a specified bias can be calculated. The stability factors in figure 5.3 are calculated at the most unstable bias of the transistor; $I_{DQ} = 20mA$, and the corresponding stability circles for the frequency range are plotted in figure 5.4. From the plots we can see that the transistor is potentially unstable below 20GHz, except for a small frequency band at 3-6GHz. Hence a stabilization network is necessary to ensure unconditional stability. By comparing the stability factors and stability circles with the corresponding stability factors and stability circles of the CGH40010F transistor in figure 4.3 and 4.4 in the

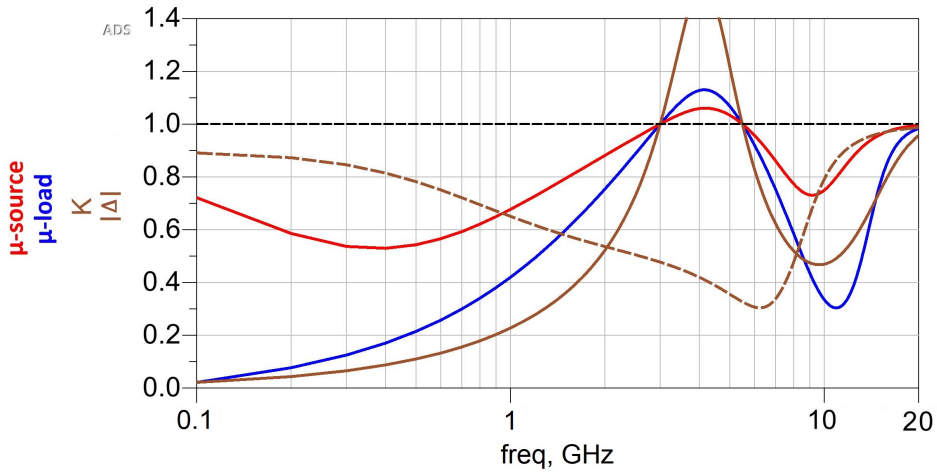
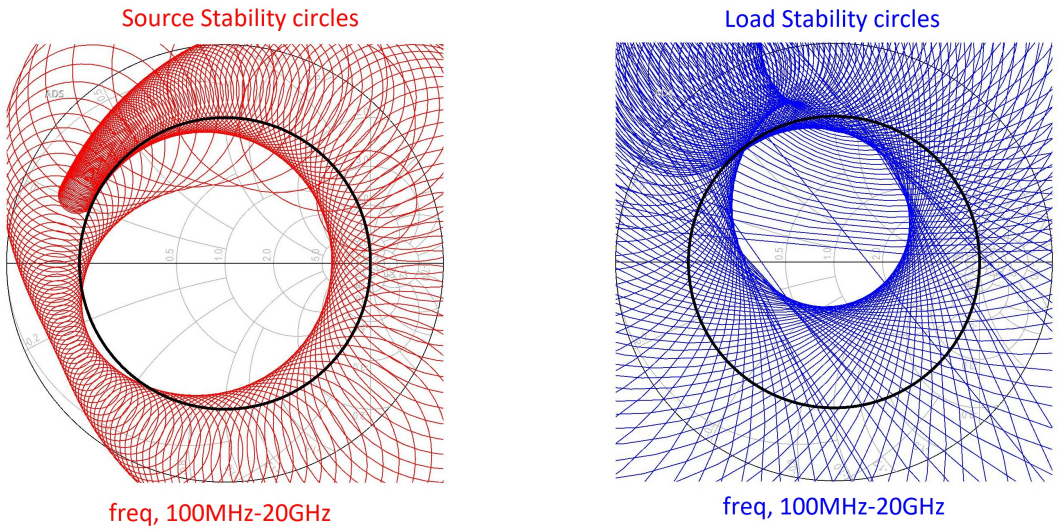


Figure 5.3: Stability factors of the CGH40006P transistor at the most unstable bias; $I_{DQ} = 20mA$, $V_{GSQ} = -3.11V$.



(a) (b)

Figure 5.4: The (a) source and (b) load stability circles at $I_{DQ} = 20mA$.

previous chapter, we see a very similar behavior. At sub-GHz frequencies the transistor is highly unstable and close to the 10-12GHz frequencies there is an apparent resonance. Considering the stability circles, both the radius of the stability circles and their protrusion in the smith chart are greater, but the center of the stability circles follow the same path; inductive instability at lower frequencies and high impedance instability at higher frequencies. Hence, by the same argumentation, a resistive network with a bypass capacitor at the gate terminal would suffice as a stabilization network.

5.2.2 Stabilization network

The stabilization network is set up as shown in the simulation schematic in figure 5.5. Since the transistor must be placed on top of a copper pad for connection to ground, the gate terminal tab must be bent down to make a connection with the transmission lines, as can be seen in figure 3.5b. To account for effects from this the rightmost transmission line in figure 5.5, is modeled as a transmission line trough air, with a width equal to the width of the gate terminal tab and a length equal to the approximate length of the tab to the first transmission line. Otherwise the simulation schematic is equivalent to the stabilization network of the power stage.

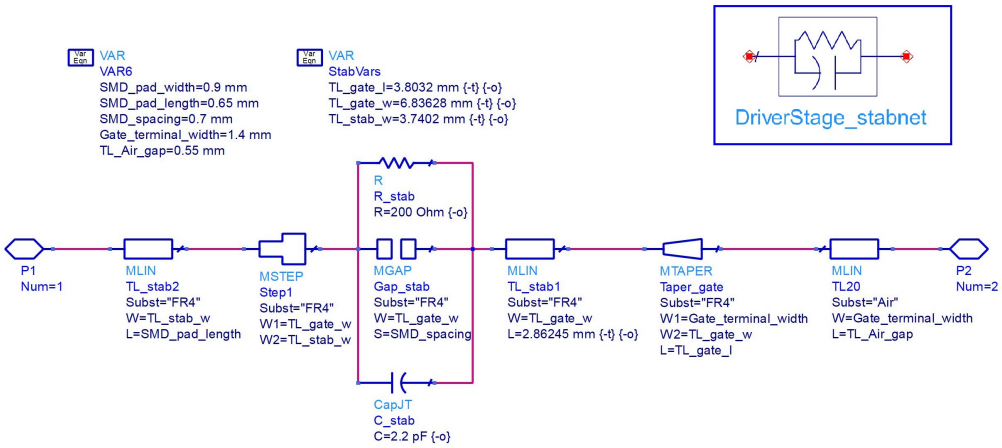
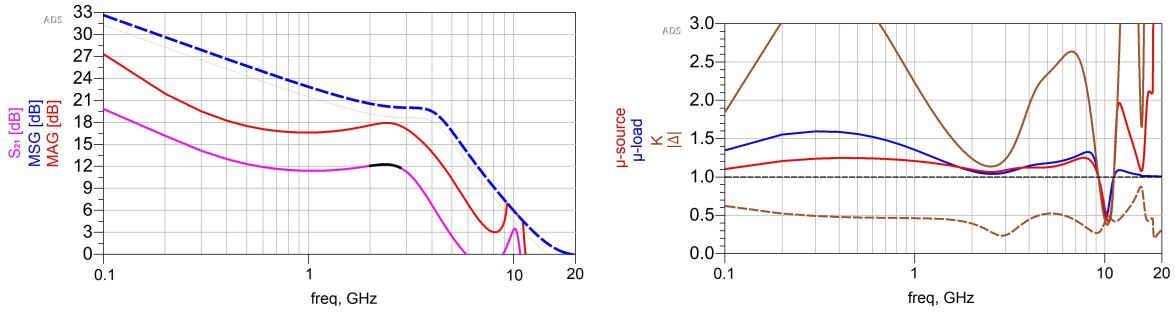


Figure 5.5: Simulation schematic of the stabilization network for the CGH40006P transistor.

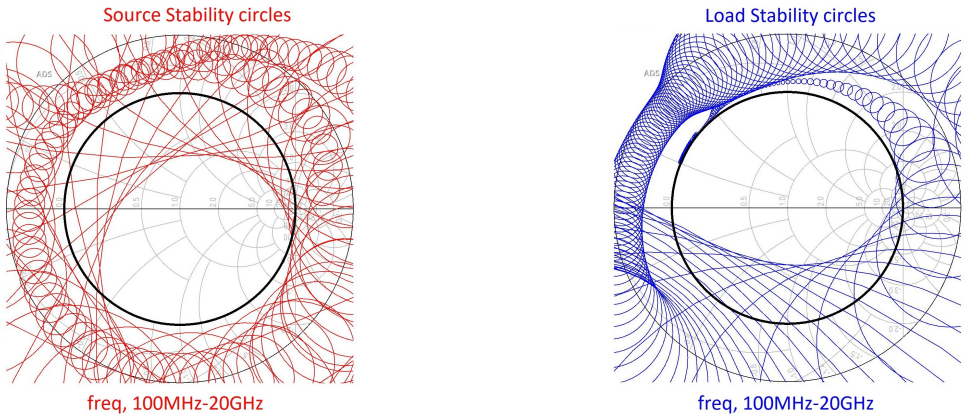
5.2.3 Stability and small-signal gain optimization

The simulation setup shown in figure A.2 was then used to optimize the stabilization network for stability over the whole frequency range and for maximum flat small-signal gain in the frequency band, while the load impedance was set to the corresponding loadline resistance of 52.873Ω. The geometric stability factors were restricted to be greater than 1 to ensure that the stability circles were outside the smith chart; and the K-factor was restricted to $K > 1.05$ to ensure that the MAG does not exceed the MSG, and to establish a minimum degree of stable gain. The small-signal gain, S_{21}, was subsequently maximized while maintaining its flatness in the frequency band. The result of the optimization is shown in figure 5.6a and the corresponding stability factors are shown in figure 5.6b. Evidently the transistor is unconditionally stable, except at 10GHz. However, we can ensure stability if we force the source and



(a) (b)

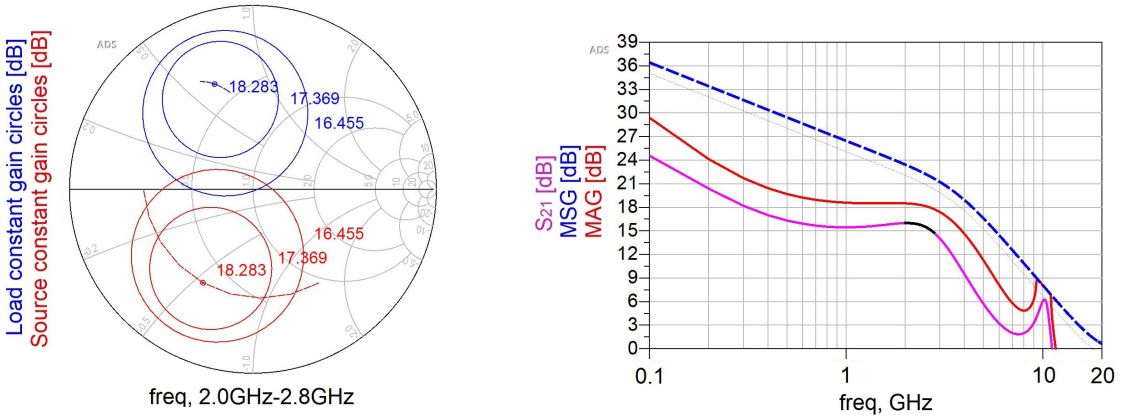
Figure 5.6: (a) Small-signal gain and (b) stability factors of the CGH40006P transistor with the optimized stabilization network at $I_{DQ} = 20mA$.



(a) (b)

Figure 5.7: The (a) source and (b) load stability circles at $I_{DQ} = 20mA$, for the transistor with stabilization network as shown in figure 5.5.

load impedances to remain in the stable regions of the smith chart by designing a proper IMN and OMN. Henceforth, we assume that is the case, and must check for this property in retrospect of the network designs. The stability circles are shown in figure 5.7, outlining the stable region of the smith chart. At the desired quiescent bias the small-signal gain is 14.770-15.983dB in the frequency band, and the MAG and MSG at the center frequency are 18.238dB and 22.528dB respectively, as shown in figure 5.8. The constant matched gain circles for the source and load at the center frequency, including the MAG for each frequency in the frequency band, are shown in the smith chart in figure 5.8. Noticeably the MAG load impedance match is confined within a relatively small region of the smith chart, while the MAG source impedance match traverse a more extensive region of the smith chart. Thus a



(a) (b)

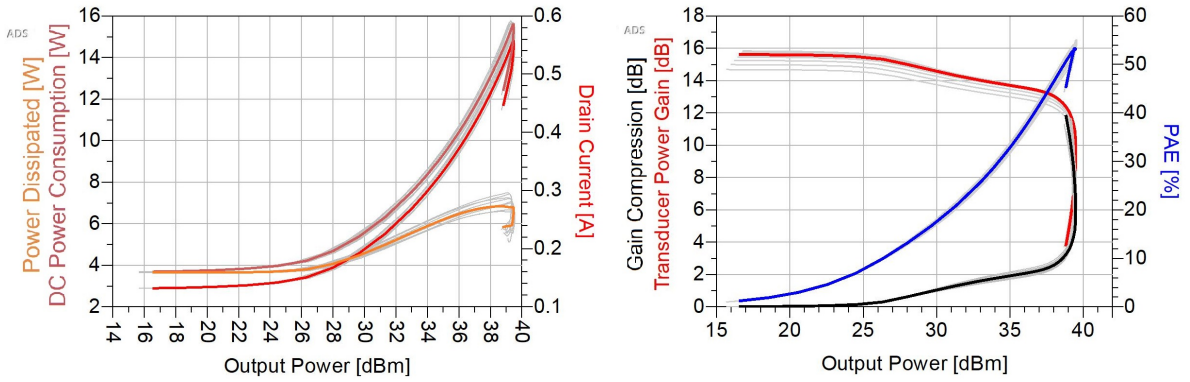
Figure 5.8: (a) Constant matched gain circles and (b) small-signal gain at $I_{DQ} = 165mA$.

good impedance match for the MAG over the frequency band can be achieved at the load, but will be more difficult to accomplish at the source.

5.3 Large-signal analysis

5.3.1 Large-signal characteristics

The large-signal characteristics of the stabilized transistor can be calculated by using the harmonic balance simulation setup shown in figure A.3 in the appendix; using the quiescent bias at $V_{DSQ} = 28V$ and $I_{DQ} = 165mA$, and setting the load impedance to the corresponding loadline resistance of 52.873Ω. The results of the simulation are shown in figure 5.9 and summarized in table 5.2.



(a) (b)

Figure 5.9: (a) Power Dissipated, DC Power Consumption and Drain Current, and (b) Transducer Power Gain, Gain compression and PAE of the stabilized transistor, for the frequency range 2.0-2.8GHz, highlighting the center frequency of 2.4GHz.

Table 5.2: Properties of the stabilized transistor in accordance with the large-signal characteristics in figure 5.9

Parameter	Symbol	Value	Unit
Saturated Output Power	P_{sat}	39.6	dBm
Transducer Power Gain	G_t	16.0	dB
Peak PAE	PAE_{max}	55	%
Maximum Drain Current	$I_{D,max}$	566	mA
Maximum DC Power Consumption	P_{DC}	15.8	W
Maximum Dissipated Power	P_{diss}	7.64	W

5.3.2 Harmonic loadpull

As with the power stage, the HLP simulation setup for the driver stage is shown in figure A.4, where the load impedance is set to the desired 50Ω-load and the reflection coefficients of the *LoadPullTB* component are optimized at the center and outer frequencies in the frequency band. When the source is terminated in 50Ω, the optimal fundamental and harmonic load impedances for maximum transducer power gain, PAE and delivered output power is as shown in figure 5.10, and the corresponding properties are shown table 4.3.

From figure 5.10 we observe that the optimal fundamental load impedances appear to traverse the smith chart horizontally in the counter-clockwise direction. The optimal fundamental load impedances for PAE ($Z_{opt.PAE}$) and power delivered ($Z_{opt.Pdel}$) have approximately equivalent resistances, but the $Z_{opt.PAE}$ have a more inductive reactance. Whereas the optimal fundamental load impedances for transducer power gain ($Z_{opt.Gt}$) are more resistive and reactances between the $Z_{opt.PAE}$ and $Z_{opt.Pdel}$. The optimal fundamental load impedances are relatively close to each other, and the optimal load impedance step size are relatively short, indicating that a good impedance match over a larger bandwidth can be achieved.

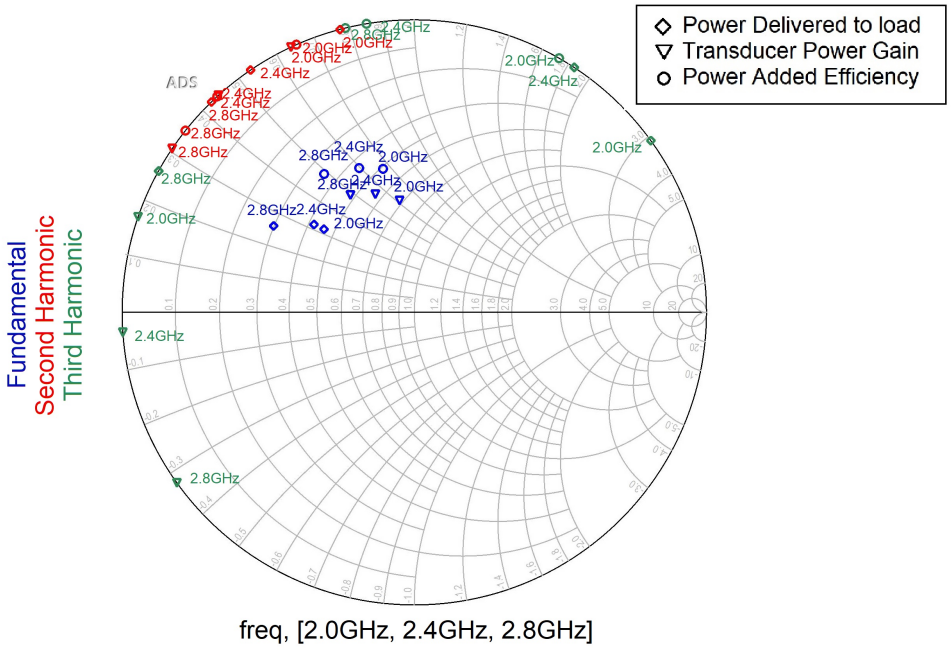


Figure 5.10: Optimal Harmonic Loadpull data for Power delivered, Transducer Power Gain and PAE at 2.0GHz, 2.4GHz and 2.8GHz.

The optimal second harmonic load impedances are in close proximity to each other and located radially outwards compared to the optimal fundamental load impedances. Thus, since the impedance trajectory of the OMN must follow Foster path, a second harmonic load impedance match would be easier to achieve if the $Z_{opt.Pdel}$ impedances are used, compared to the $Z_{opt.PAE}$. The optimal third harmonic load impedances for each property also seem to be close to each other, but the angle of the reflection coefficients seem to be quite sensitive to which optimal fundamental load impedances that are being used.

From table 5.3 we can see that the sensitivity of the transducer power gain is relatively low, with only 1.515dB maximum deviation, and likewise for the power delivered. Contrary, the sensitivity of the PAE are quite high, with a maximum deviation of 12.585 percentage points. From these data the optimization goal and restrictions are set to

$$G_t > 16dB; \qquad P_{sat} > 39.2dBm; \qquad max(PAE). \tag{5.1}$$

The desired load impedances from the HLP simulation using these optimization goals are shown in figure 5.11, and as expected the desired optimal impedances are close to the $Z_{opt.PAE}$ impedances. The corresponding properties are presented in table 5.4. The fundamental, 2nd and 3rd harmonic loadpull contours for the transducer power gain and PAE are shown in figure 5.12 through 5.14, where the samples not fulfilling the desired power delivered are highlighted, and the desired load impedances from the previous optimization are superimposed

Table 5.3: The Transducer Power Gain, PAE and Power delivered to the load, when the load impedances are matched to the optimal load impedances for the center and outer frequencies.

Parameter	Values			Unit	Optimization
Frequency	2.0	2.4	2.8	GHz	
Transducer Power Gain	**16.796**	**16.790**	**16.001**	dB	**Opt. Gain**
	16.735	16.760	15.950	dB	Opt. PAE
	16.150	16.282	15.275	dB	Opt. Pdel
Power Added Efficiency	73.259	74.588	74.705	%	Opt. Gain
	82.103	**82.755**	**83.153**	%	**Opt. PAE**
	70.568	72.898	71.822	%	Opt. Pdel
Power delivered	39.103	39.188	39.315	dBm	Opt. Gain
	39.218	39.211	39.301	dBm	Opt. PAE
	40.675	**40.596**	**40.568**	dBm	**Opt. Pdel**

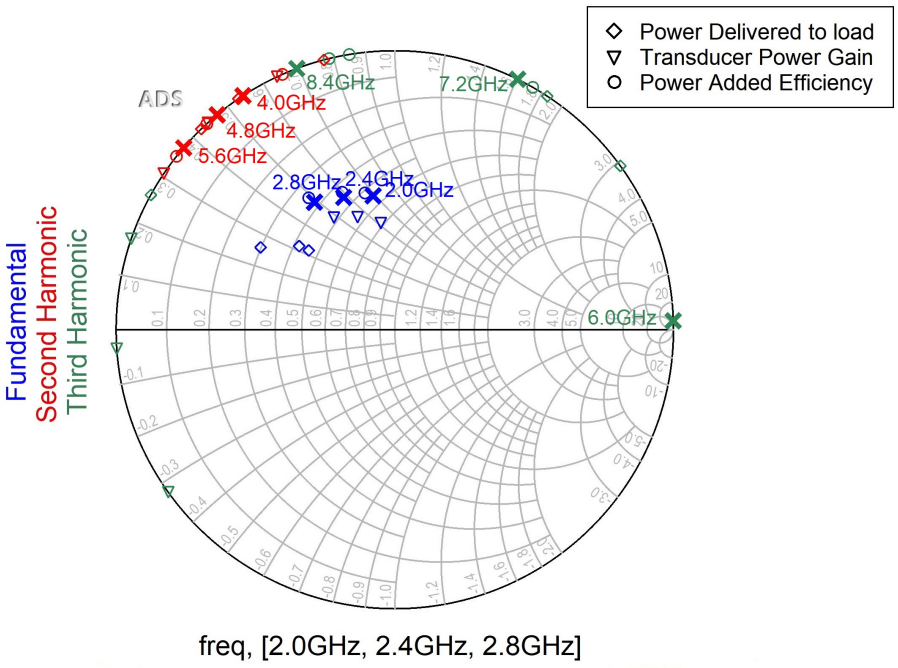


Figure 5.11: Desired load impedances, superimposed on the optimal impedances from figure 5.10.

Table 5.4: The Transducer Power Gain, PAE and Power delivered to the load, when the load impedances are matched to the desired load impedances for the center and outer frequencies.

Parameter	Values			Unit	Optimization
Frequency	2.0	2.4	2.8	GHz	
Transducer Power Gain	16.769	16.776	15.978	dB	Opt. desired
Power Added Efficiency	82.118	82.477	82.038	%	
Power delivered	39.195	39.323	39.328	dBm	

on the contour plot. During the fundamental loadpull the harmonic loads are terminated in the desired harmonic load impedances, and likewise for the fundamental and the other harmonic load impedance during the harmonic loadpulls. From the contour plots we observe that the fundamental PAE contours are primarily in the invalid regions of the smith chart, making design for both high efficiency and high saturated output power difficult. Additionally, the valid regions for the second harmonic load impedances are narrow at the edge of the smith chart, making the second harmonic load impedance match more difficult.

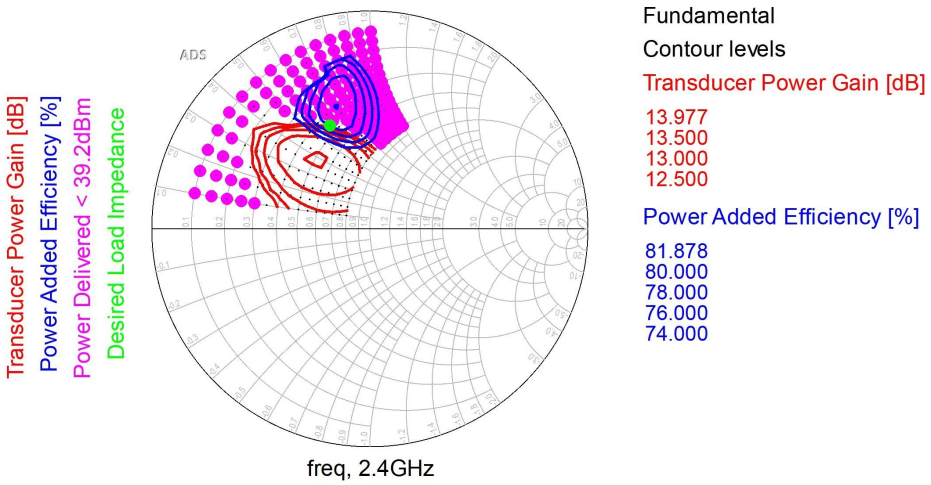


Figure 5.12: Fundamental loadpull contours for 39.2dBm desired power delivered at the center frequency, when terminated in the desired load impedances.

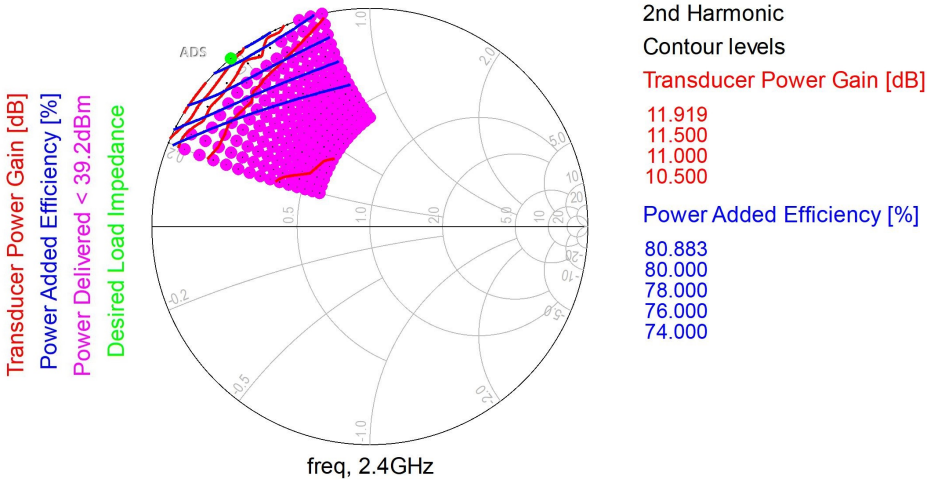


Figure 5.13: 2nd Harmonic loadpull contours for 39.2dBm desired power delivered at the center frequency, when terminated in the desired load impedances.

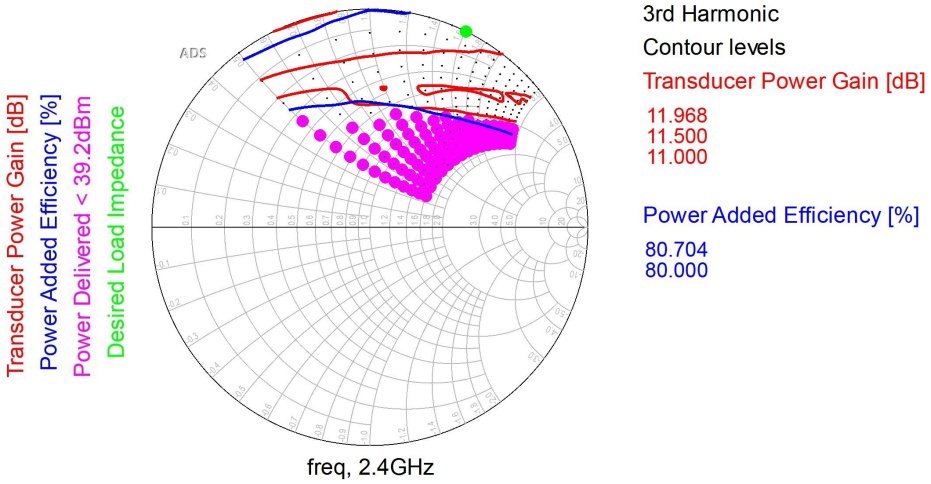
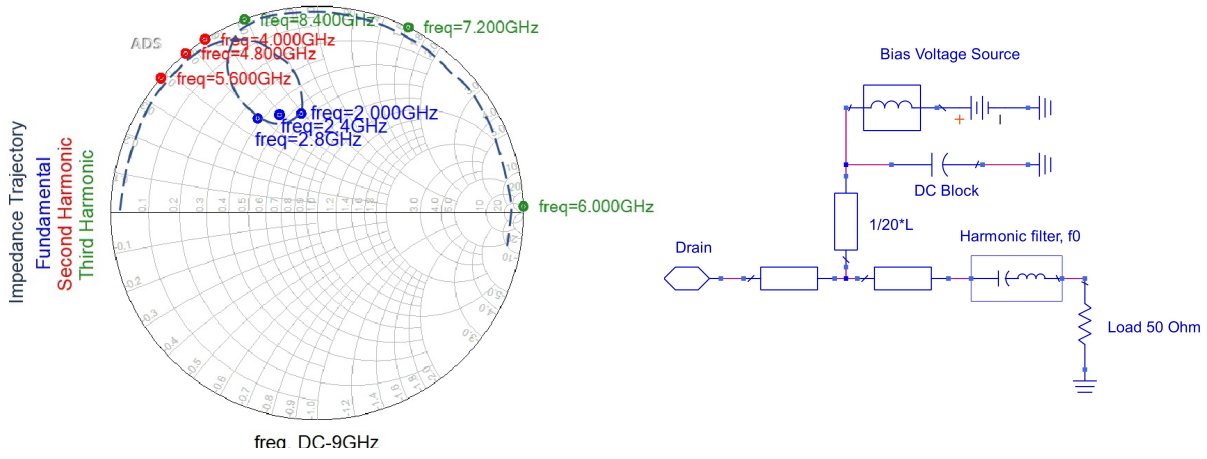


Figure 5.14: 3rd Harmonic loadpull contours for 39.2dBm desired power delivered at the center frequency, when terminated in the desired load impedances.

5.3.3 Output Network impedance trajectory

Now that the desired fundamental and harmonic load impedances, and the preferred sensitivity range, for the transistor are determined, the OMN can be designed according to these restrictions. By comparing the desired impedance trajectory for the driver stage with the desired impedance trajectory for the power stage in the previous chapter, we see that they are quite similar. Hence a similar structure for the driver stage OMN is desired.

The most important differences are the position of the twirl in the impedance trajectory, the shorter impedance trajectory path, and the counter-clockwise positioning of the desired second harmonic load impedances relative to the desired fundamental load impedances. The latter could be solved by introducing additional twirls in the impedance trajectory, or one can accept a slight mismatch in return for a less complex matching network. The rest can be solved by adjusting the length of the transmission line from the drain terminal and the transmission line to the bias network respectively. Regarding the preliminary design of the bias networks, the same design as described in the previous chapter is used, but the transmission line to the bias network is made shorter because of the shorter desired impedance trajectory.



(a) (b)

Figure 5.15: The (a) desired impedance trajectory and the (b) preliminary schematic, of the output matching network.

5.3.4 Design of the Output Matching Network

The OMN of the driver stage is set up as shown in figure 5.16, and compared to the power stage OMN in figure 4.15 the structure is the same, except for the leftmost transmission line through air. The DBN is fixed to a distance of 11mm from the drain terminal, the transmission line from the drain terminal tab is restricted to be greater than 1mm, and the taper angles are restricted to be less than 45 degrees.

The OMN is optimized using the network optimization simulation setup shown in figure A.5 in the appendix, where the distance between the OMN input impedance and the desired load impedances is minimized. The outcome of the optimization is shown in figure 5.16 and the corresponding impedance trajectory, along with the desired load impedances, is shown in figure 5.17. Evidently the second harmonic network impedances are shifted clockwise relative to the desired second harmonic load impedances as predicted, and the third harmonic network impedances are compressed towards the mean phase of the desired third harmonic load impedances in order to improve the third harmonic through match. The fundamental network impedances are also closely matched to the desired fundamental load impedances with a twirl match.

The large-signal characteristics of the stabilized transistor with the OMN are shown in figure 5.18. Compared to the large-signal characteristics of the stabilized transistor with matched load in figure 4.8, the transducer power gain has increased by 0.5dB; the maximum linear output power has increased from 25 dBm to 30 dBm; the peak PAE has increased

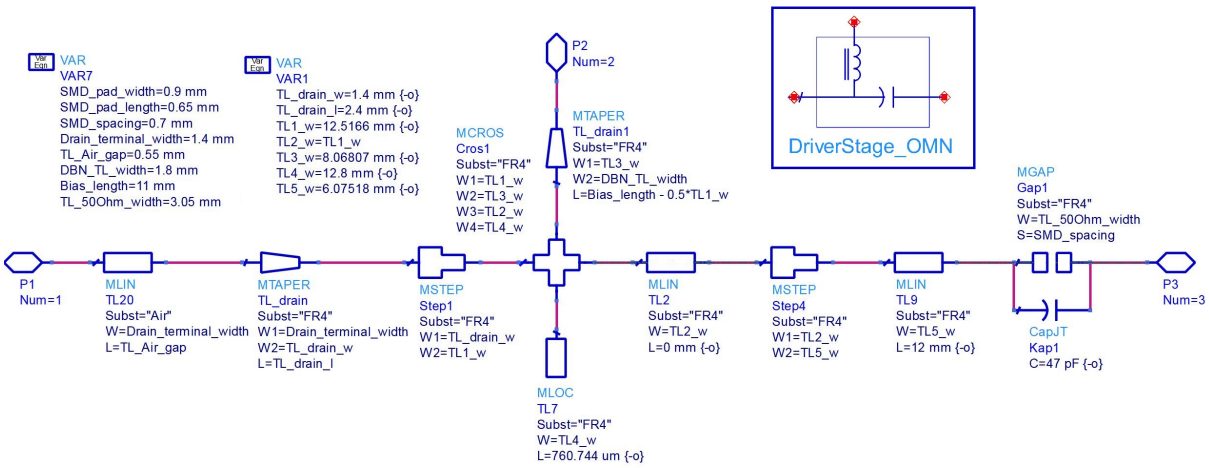


Figure 5.16: Schematic simulation model of the OMN.

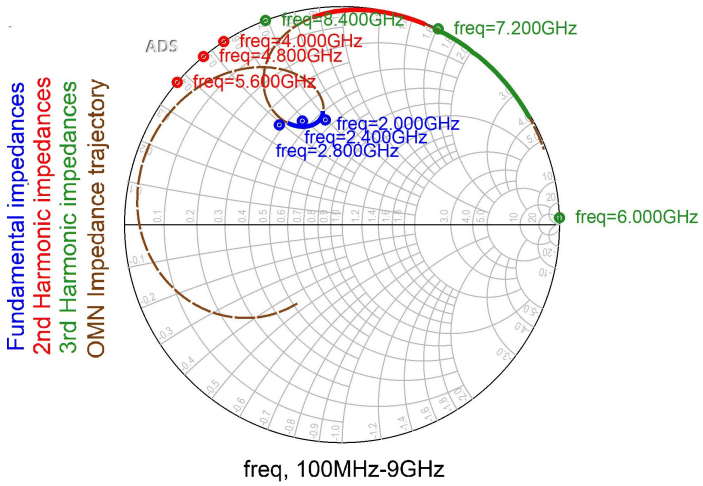
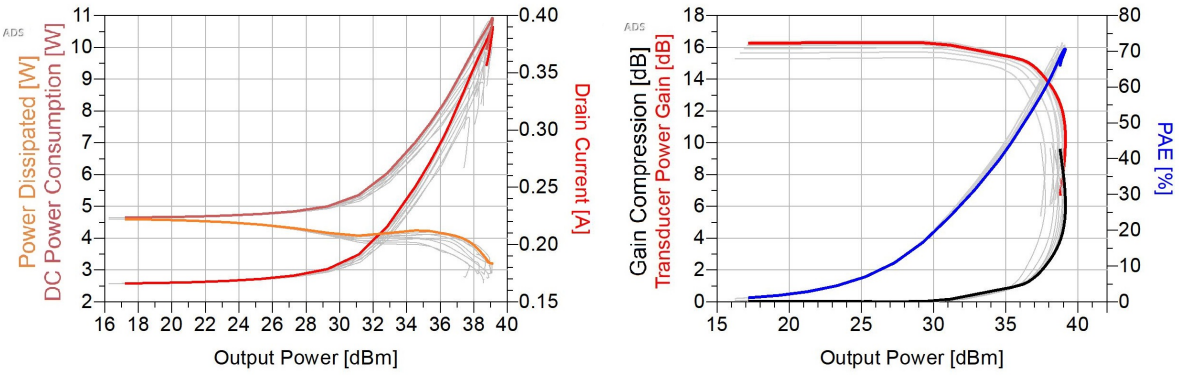


Figure 5.17: OMN impedance trajectory match for desired load impedances from the OMN network in figure 5.16.

from 54% to 70%; the peak drain current has decreased by 180mA; and the peak DC power consumption has decreased by 5W. However, the transducer power gain at the upper part of the frequency band is up to 1 dB less than the lower part of the frequency band, which reduces the gain flatness; the saturated output power now deviates up to 3dB from the desired output power; and the power dissipation has increased by 0.7W at the lower output powers. Noticeably the deviation of the PAE is much less than the deviation in the transducer power gain and the saturated output power, analogous to the fact that the desired load impedances are more closely matched to the $Z_{opt.PAE}$ impedances than the $Z_{opt.Pdel}$ and $Z_{opt.Gt}$ impedances.



(a) (b)

Figure 5.18: (a) Power Dissipated, DC Power Consumption and Drain Current, and (b) Transducer Power Gain, Gain compression and PAE of the stabilized transistor with OMN, for the frequency range 2.0-2.8GHz, highlighting the center frequency of 2.4GHz.

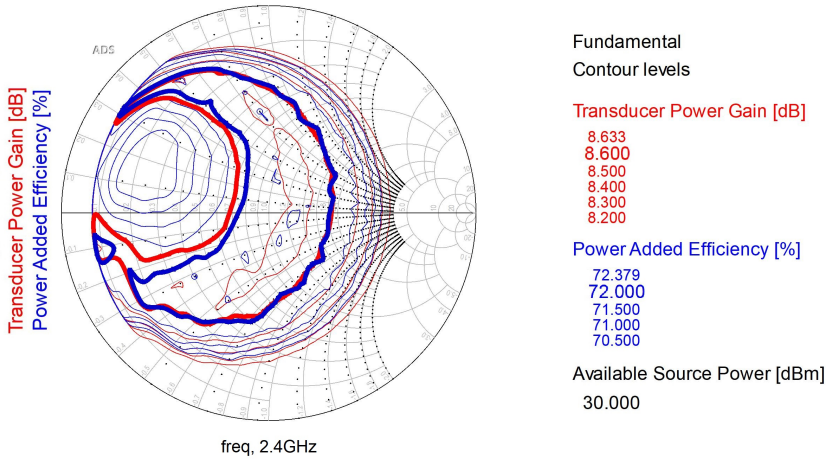


Figure 5.19: Fundamental sourcepull contours for 30dBm available source power at 2.0GHz.

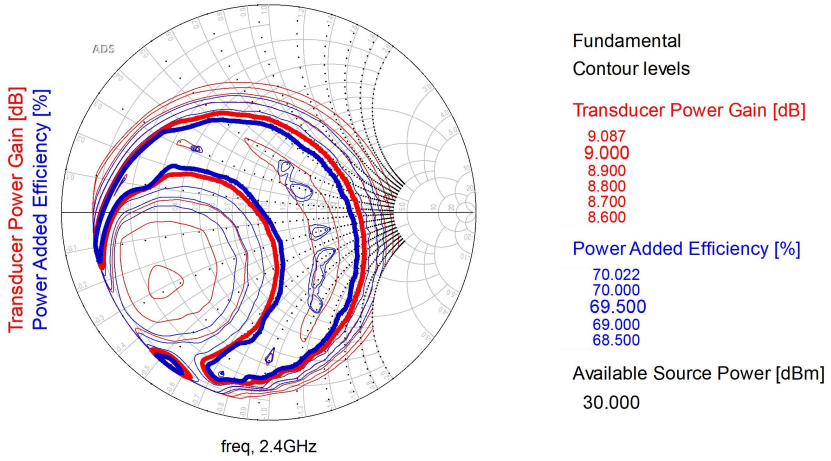


Figure 5.20: Fundamental sourcepull contours for 30dBm available source power at 2.4GHz.

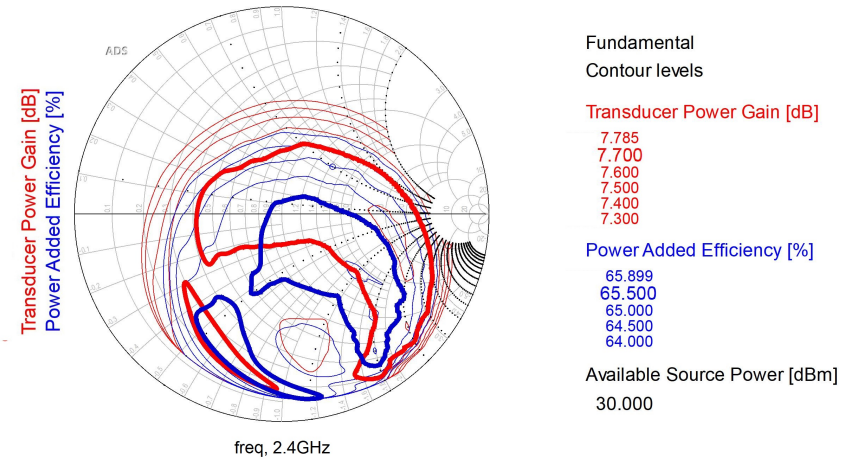


Figure 5.21: Fundamental sourcepull contours for 30dBm available source power at 2.8GHz.

5.3.5 Harmonic Sourcepull

By using the simulation setup shown in figure A.4 in the appendix and replacing the *Load-PullTB* component with the OMN, a HSP simulation can be performed. The same goals as during HLP were used during the optimization, but no decisive optimal load impedances could be found, as it changed for each optimization. By looking at the HSP contour plots for transducer power gain and PAE shown in figure 5.19 through 5.21, we can observe that it consists of several local poles. Hence, the optimization would converge to different local poles depending on the first guess of optimal impedance, thus explaining the indecisive behavior. A graphical evaluation to estimate the optimal source impedances could then be used, or one could optimize the IMN through other means.

5.3.6 Design of the Input Matching Network

Since the HSP was inconclusive in determining the optimal source impedances, the IMN could be optimized directly from the large-signal characteristics by using the harmonic balance simulation setup shown in figure A.3 in the appendix. The driver stage IMN was set up as shown in figure 5.22, where the GBN are fixed at 11mm from the gate terminal; the transmission line cross junction with the stabilization network is restricted to have the transmission line width of the stabilization network; and the transmission line to the GBN is restricted to have the transmission line width of the GBN. The transmission line stub is used as a supplement impedance match for the transmission line to the GBN as it is quite constrained, and the transmission line to the capacitor is used for the rest of the impedance matching.

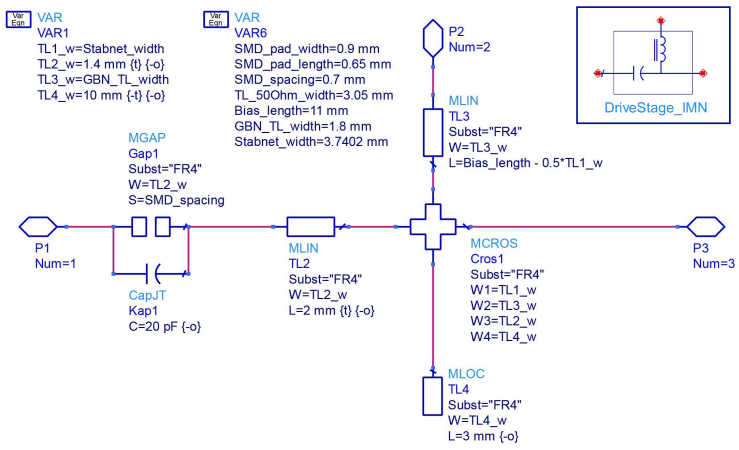


Figure 5.22: Simulation schematic of the driver stage IMN.

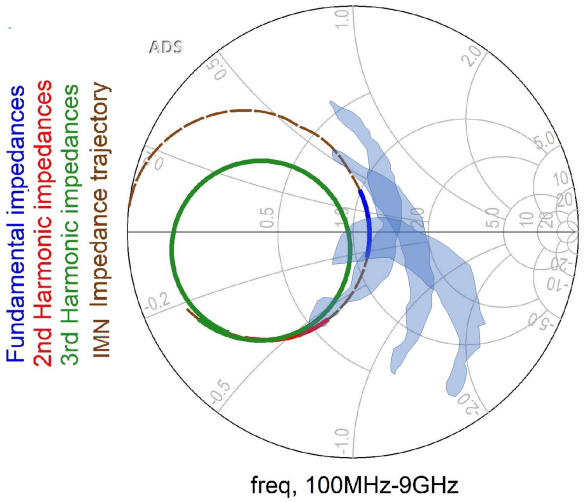


Figure 5.23: Impedance trajectory of the driver stage IMN, and superimposed optimal fundamental contour plots.

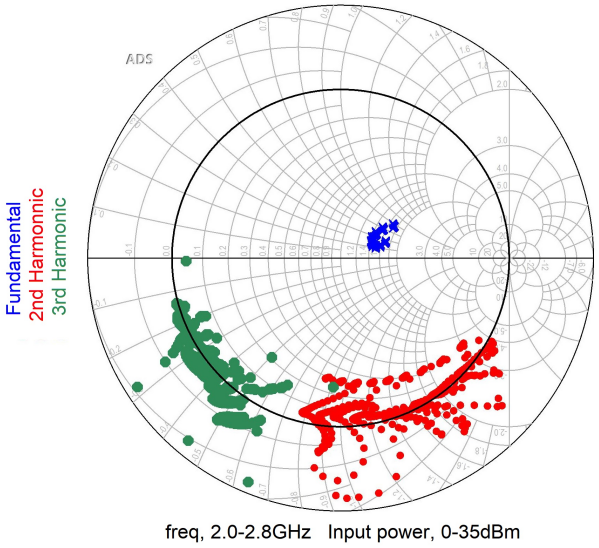


Figure 5.24: Caption

Evidently the IMN is designed to be as simple as possible, while providing some degree of impedance match.

The IMN was optimized for gain flatness in the frequency band, for input powers of 15dB and 21dBm, simultaneously. The outcome of the optimization is shown in the simulation schematic in figure 5.22 and the corresponding IMN impedance trajectory is shown in figure 5.23 with the optimal regions of impedances from the HSP contours. Noticeably the impedance match in the frequency band are close to but greater than 50Ω and are closely matched to the optimal regions of impedances. As with the power stage we can determine the class of operation by looking at the impedances presented to the internal nodes of the

transistor shown in figure 5.24. The impedances reminds of and inverse class F much like the impedances in the power stage, but with higher fundamental resistance and second harmonic reactance.

During the design of the stabilization circuit we assumed that the potential instability at 10GHz would be eliminated when designing the OMN and IMN for the driver stage. Thus, the stability must be reevaluated. By using the s-parameter simulation setup shown in figure A.2 and evaluating the stability of the entire driver stage, the stabilization factors were as shown in figure 5.25. Indeed the driver stage is unconditionally stable and a redesign is not required.

The characteristics of the matched driver stage are shown in figure 5.26. Compared to the characteristics of the stabilized transistor with OMN, the transducer power gain has dropped about 0.4dB, but deviates less than 0.3dB over the frequency band up to 31dBm output power; and less than 0.4dB up to 36dBm output power. The lowest saturated output power is 37.7dBm at a frequency of 2.8GHz, whereas the highest saturated output power is 39.05dBm at 2.4GHz. The mean peak PAE is 69%, the maximum drain current is 390mA and the maximum dissipated power is 4.6W. From figure 5.27a the transducer power gain is 15.6dB in the 1.5-2.8GHz range for linear operations (less than 30dBm output power) with a PAE at 20%, and at 36dBm desired output power the transducer power gain is 14.5dB in the 1.7-2.8GHz range with a PAE at 50%. The resulting layout of the driver stage is shown in figure 5.28.

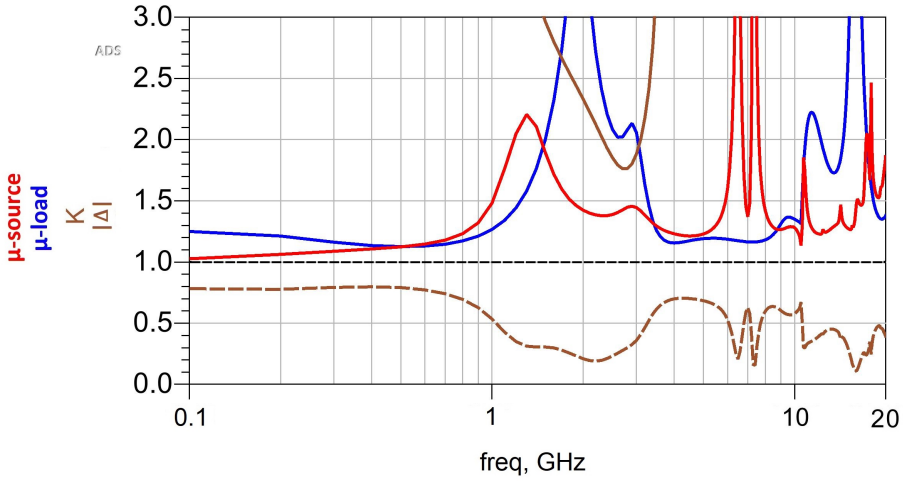
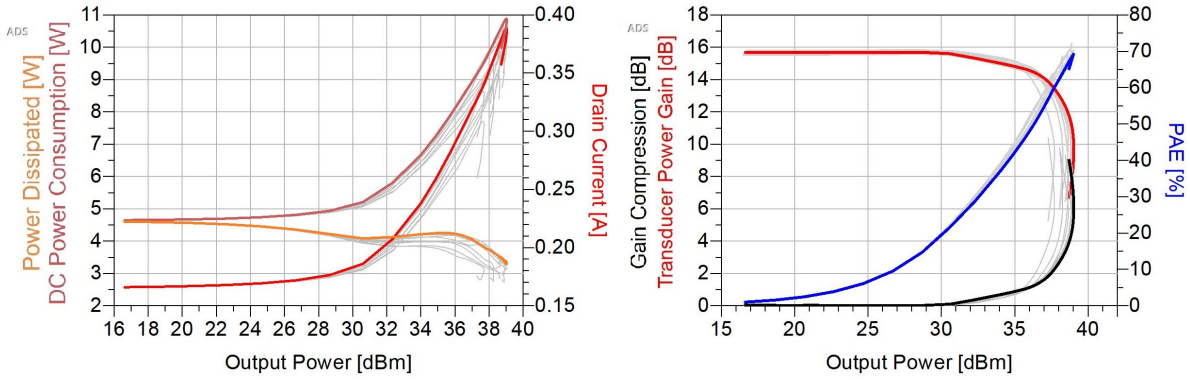
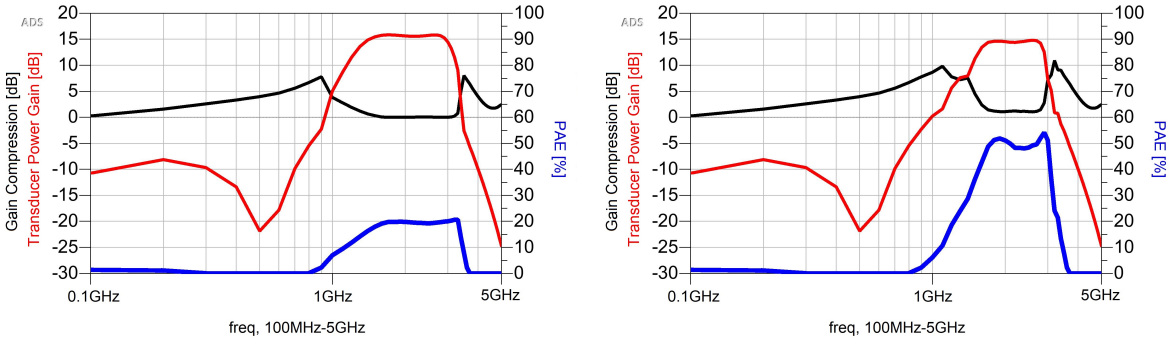


Figure 5.25: The stability factors of the entire driver stage, showing unconditional stability between 100MHz and 20GHz.



(a) (b)

Figure 5.26: (a) Power Dissipated, DC Power Consumption and Drain Current, and (b) Transducer Power Gain, Gain compression and PAE of the power stage, for the frequency range 2.0-2.8GHz, highlighting the center frequency of 2.4GHz.



(a) (b)

Figure 5.27: The transducer power gain, gain compression and PAE for (a) 30dBm and (b) 36dBm desired output power, from 100MHz to 5GHz.

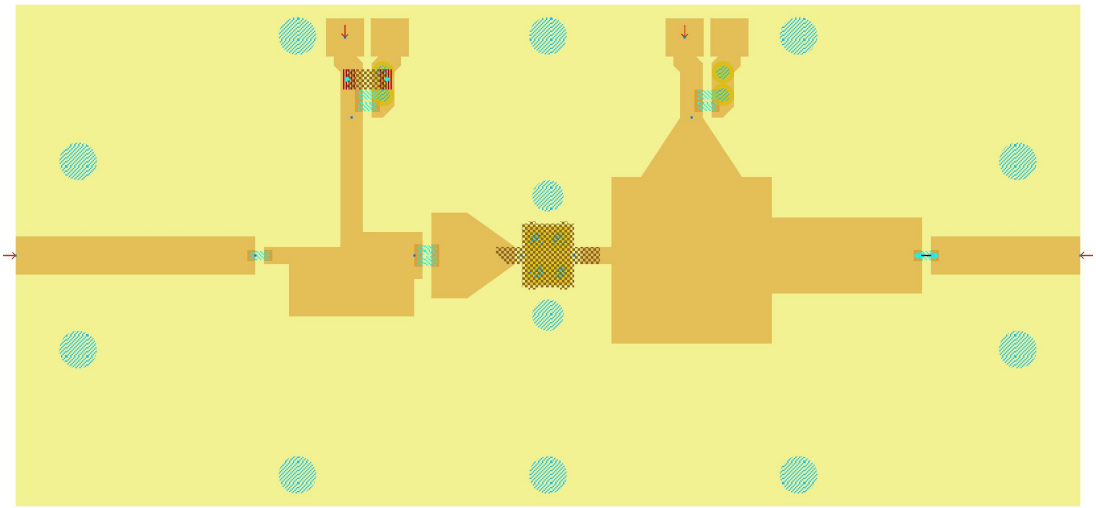


Figure 5.28: Layout of the Driver stage.

5.4 Summary and discussion

In this chapter we went through the design process of the driver amplifier stage, looking at stability and small-signal and large-signal characteristics, and comparing to the corresponding results from the power amplifier stage design. From figure 5.27 we can see that a much greater bandwidth was attained, expanding at frequencies below the intended frequency band, and that the transducer power gain remains flat over the entire bandwidth up to 35dBm output power. However, at larger output powers the transistor goes into saturation very differently and thus the bandwidth collapses. Looking back at figure 5.11 we chose desired load impedances that were close to the $Z_{opt.PAE}$, but we could have chosen impedance points closer to the $Z_{opt.Pdel}$ instead, which also would have made matching of the desired second harmonic load impedances easier. We would then have a flat gain also at larger output powers, but we would loose some 10% PAE. Since the primary goal of the driver stage is to have a flat gain until the power stage is saturated, there is only need for the bandwidth to to remain flat up to 31dBm output power. Hence, the bandwidth collapse over 35dBm would not be an issue.

Two-stage Amplifier design

Chapter 6

Two-stage Amplifier design

In this chapter we will take a look at the characteristics of the cascaded two-stage amplifier of the driver and power stage amplifiers from the previous chapters. An interstage network is then designed and optimized in order to improve the impedance match between the stages and thereby also the characteristics of the two-stage amplifier.

6.1 Cascaded two-stage amplifier

The single-stage amplifiers from the previous chapters can be cascaded into a two-stage amplifier, where the driver amplifier acts as the first stage and the power stage acts as the second stage. As both the driver and power amplifier are designed to fit within the design space of the aluminium plate, the entire design including the 50Ω transmission lines towards each connector input/output, is evaluated. In the junction between the two stages it is assumed that the 50Ω transmission lines are directly connected to each other, without using any connectors and wires. The large-signal simulation setup from figure A.3 is used to evaluate the characteristics of the cascaded two-stage amplifier, where the setup is modified as shown in figure 6.2. The results of the simulation of the cascaded two-stage amplifier are shown in the plots in figure 6.1, and are compared with the driver and power amplifier stages in table 6.1.

Most noticeable is the increased variance in the maximum power delivered, the transducer power gain and peak PAE. Additionally the maximum drain current of the driver stage, the maximum DC power consumption and the maximum dissipated power of the cascaded

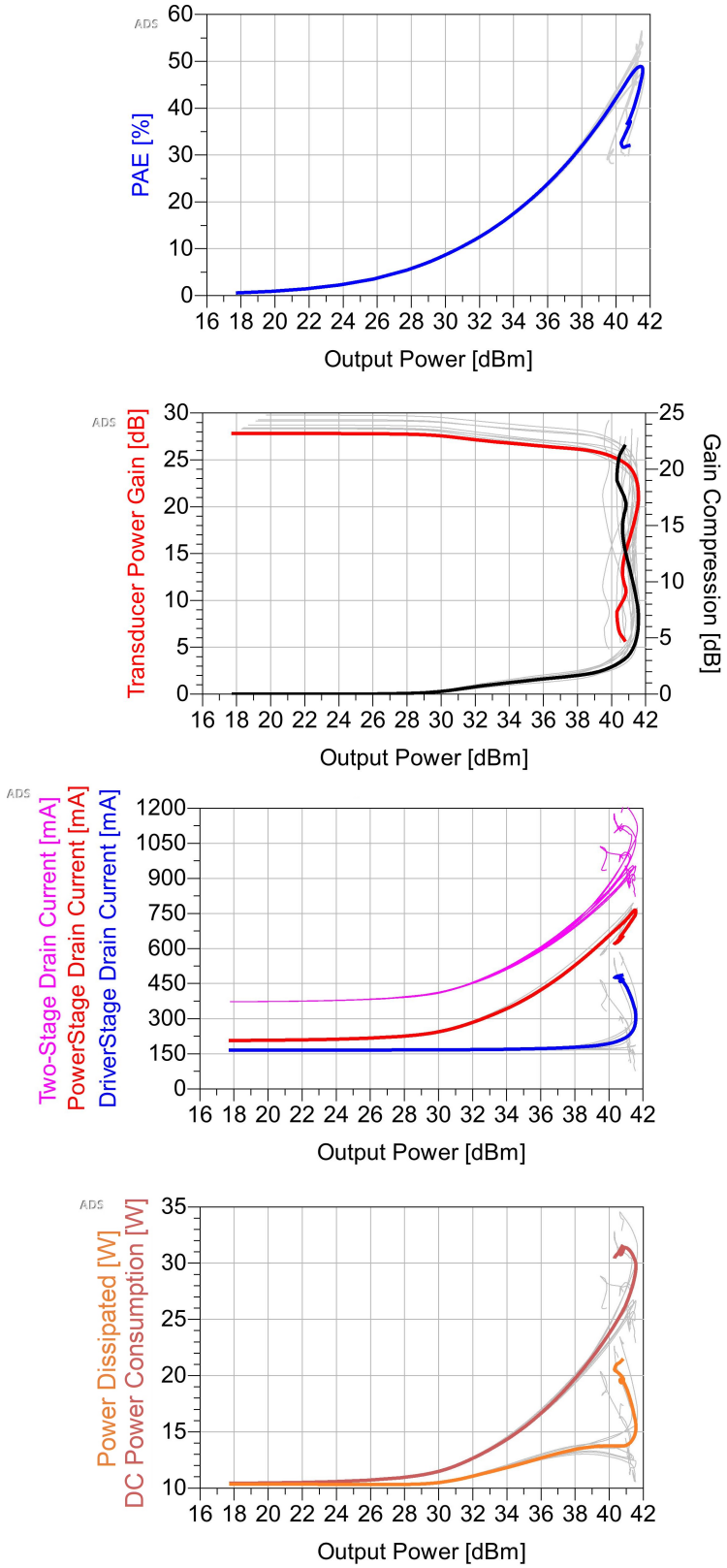


Figure 6.1: PAE, Transducer Power Gain, Gain compression, Drain Current, Power Dissipated and DC Power Consumption of the cascaded two-stage amplifier, for the frequency range 2.0-2.8GHz, highlighting the center frequency of 2.4GHz.

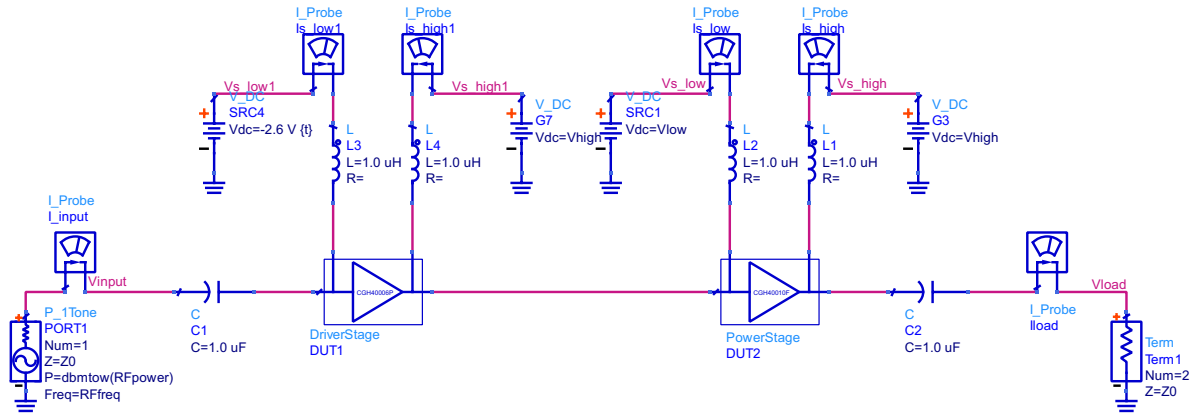


Figure 6.2: The modified simulation schematic of the setup in figure A.3 for large-signal evaluation of the cascaded two-stage amplifier.

amplifier have increased compared to the combination of the separate characteristics of the driver and power amplifier stage.

6.2 Interstage network design

In order to improve the characteristics of the cascaded two-stage amplifier the design of the driver and power stages can be combined by introducing an interstage network between the output of the driver stage and input of the power stage. The simplest way of introducing this kind of network, while using most of the established network design in order to minimize redesign, is to replace the two DC blocking capacitors with a single capacitor and an appropriate matching network. The simulation schematic of the interstage network used henceforth in this design is shown in figure 6.3. As with the IMNs, the interstage network was optimized using the large-signal simulation setup shown in figure A.3 in the appendix, modified for two stage simulation as shown in figure 6.2. Since the design of the driver and

Table 6.1: Comparison of the characteristics of the cascaded two-stage amplifier versus the driver and power stage amplifiers, in the frequency band 2.0-2.8GHz.

Parameter	Symbol	Driver stage	Power stage	Two-stage	Unit
Saturated Output Power	P_{sat}	37.6-39.0	41.4	41.2-41.7	dBm
Transducer Power Gain	G_t	15.5	13.1	27.8-29.8	dB
Peak PAE	PAE_{max}	69	60	45.6-56.5	%
Maximum Drain Current	$I_{D,max}$	390	791	585, 795	mA
Maximum DC Power Consumption	P_{DC}	10.9	22.15	34.6	W
Maximum Dissipated Power	P_{diss}	4.6	10.0	23.5	W

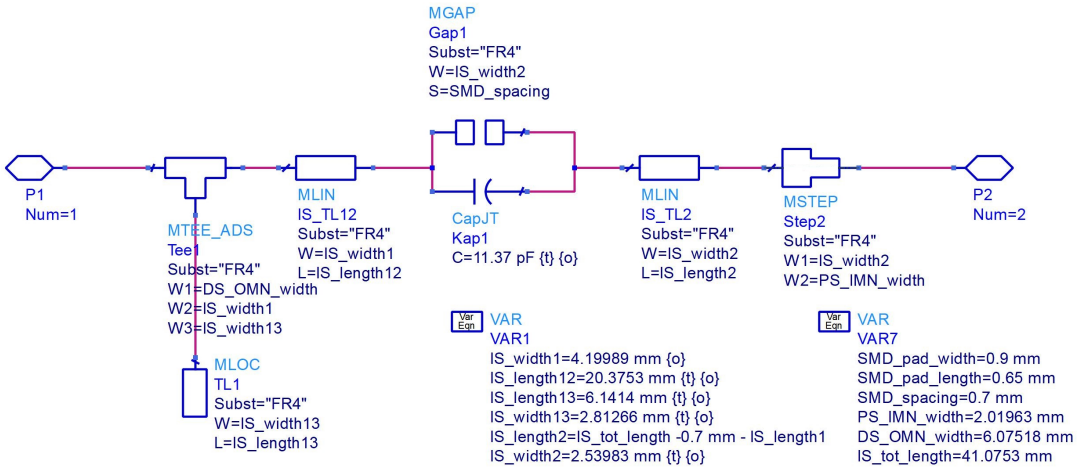


Figure 6.3: The simulation schematic of the interstage network.

power stages remain unmodified from the previous design, the distance between the transmission lines of the driver stage OMN and power stage IMN are fixed. Thus, the total length of the interstage network is also fixed. Therefrom, an open stub and the DC blocking capacitor is added, along with the intermediate transmission lines. Subsequently the positioning of the stub and capacitor, and the width of the transmission line segments are optimized. The outcome of the optimization is shown in figure 6.3, and a simulation schematic subcircuit overview of the two-stage amplifier is shown in figure 6.4 for reference.

The characteristics of the two-stage amplifier with the interstage network are shown in the plots in figure 6.5. Evidently the flatness of the transducer power gain has improved during the optimization, the PAE at the center frequency have increased and the saturated power variance has decreased. Although the PAE, drain currents, dissipated power and DC power consumption have the same tendencies as for the cascaded two-stage amplifier, the characteristics at the center frequency has improved.

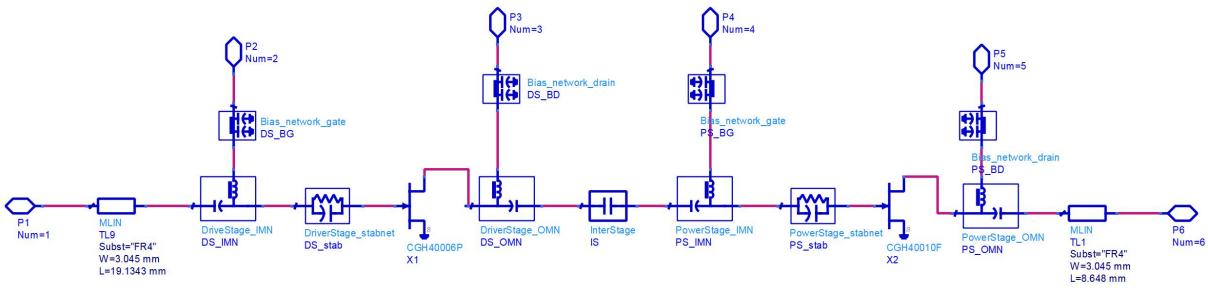


Figure 6.4: A simulation schematic subcircuit overview of the two-stage amplifier.

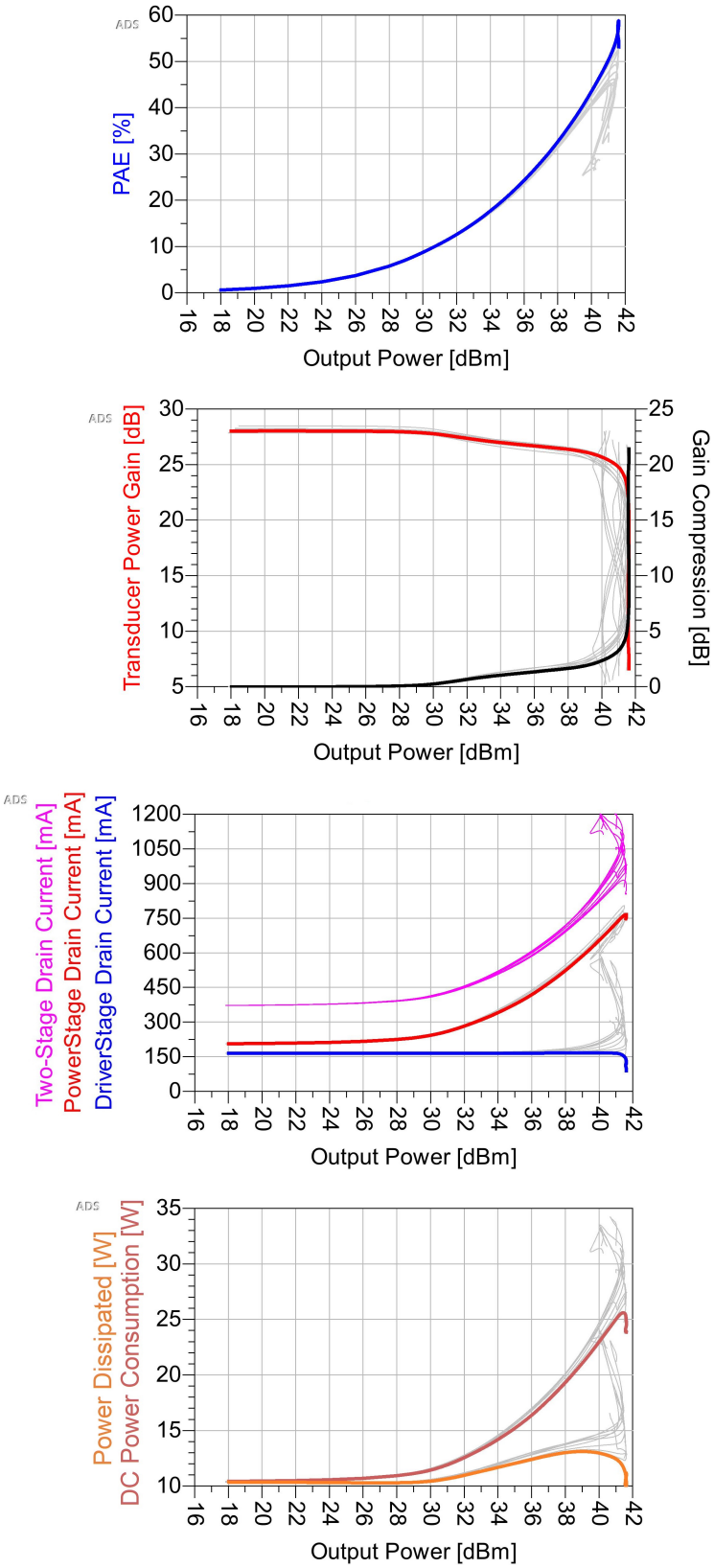
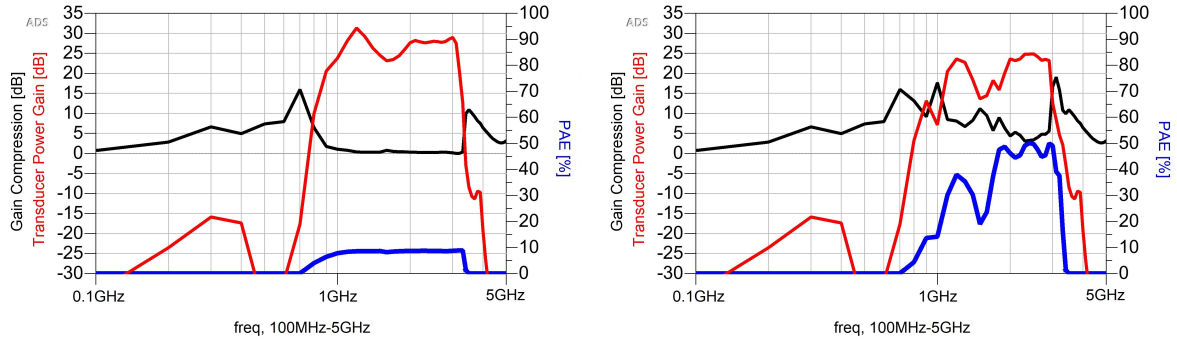


Figure 6.5: PAE, Transducer Power Gain, Gain compression, Drain Current, Power Dissipated and DC Power Consumption of the two-stage amplifier with interstage network, for the frequency range 2.0-2.8GHz, highlighting the center frequency of 2.4GHz.



(a) (b)

Figure 6.6: The transducer power gain, gain compression and PAE for (a) 30dBm and (b) 41dBm desired output power, from 100MHz to 5GHz.

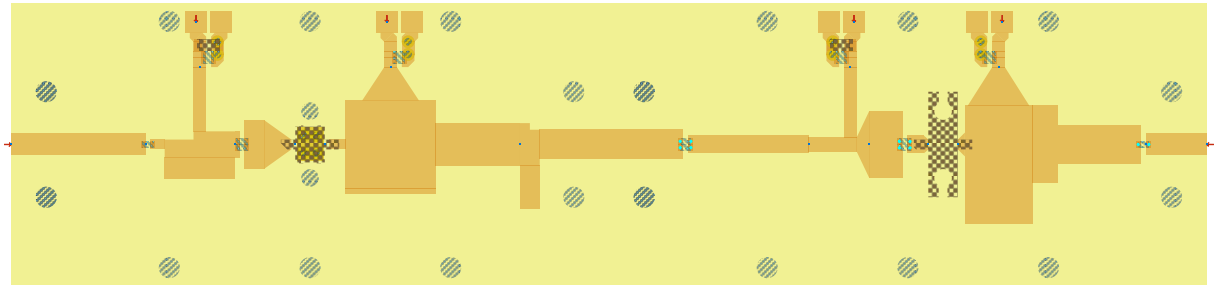


Figure 6.7: Layout of the two-stage amplifier with interstage network.

The transducer power gain, gain compression and PAE at 30dBm and 41dBm desired output power versus frequency are also shown figure 6.6. Evidently the transducer power gain at the frequency band 2.0-2.8GHz are relatively flat, with only 1.3dB and 1.6dB in gain ripple for the respective desired output powers. Some unintentional bandwidth down to 1GHz are also attained, but it has a huge dip of 4-10dB in transducer power gain at 1.6GHz. At 41dBm output power the transistor operates close to peak PAE and have a mean of 47.3% with an efficiency ripple of 5.6% in the frequency band 2.0-2.8GHz. As with the transducer power gain, some efficiency is attain down to 1GHz with a huge dip at 1.6GHz. The layout of the two-stage amplifier is shown in figure 6.7.

6.3 Summary and discussions

Considering the simple design method used to create the interstage network, several improvement could have been made to ensure an even better impedance match between the

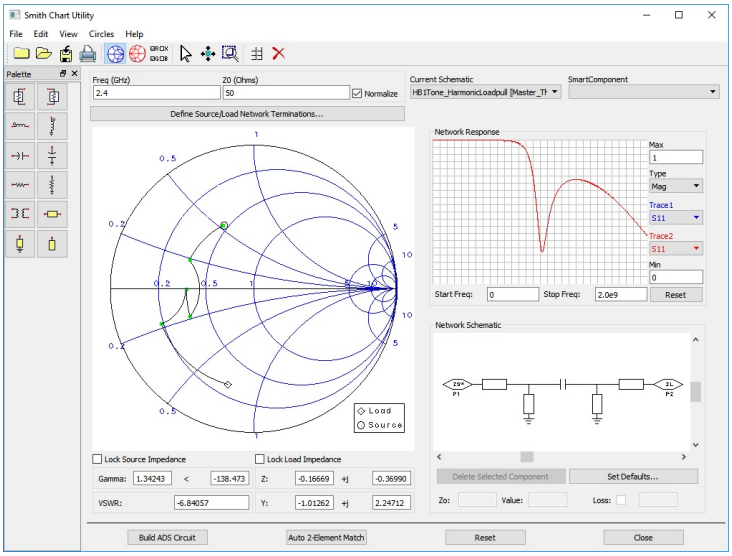


Figure 6.8: A quick interstage network design for the desired impedances at 2.4GHz using the smith chart utility in ADS.

transistor, to compress the overall design of the two-stage amplifier, and to ensure the stability of the design. However, as the time frame of the project were limited at this design stage and because of the restrictions in the design space, the fast and simple design method was chosen. The benefit of this method is that the characteristics of the cascaded two-stage amplifier and the two-stage amplifier with interstage network could be compared directly.

Full interstage matching network

Instead of using the already established design of the driver stage OMN and power stage IMN while designing the interstage network, one could create an entirely new interstage network design to match the drain terminal of the CGH40006P transistor directly to the stability network (or gate terminal) of the CGH40010F transistor. The desired input impedances at these nodes are already established in chapter 4 and 5 during the source- and loadpull. By using the source- and loadpull results and assuming the basic network design as shown in the network schematic of the smith chart utility tool in figure 6.8, a quick example of a the network impedance matching at 2.4GHz is shown in the smith chart in the same figure. The interstage network would be optimized by the same method as used in the previous chapters, by using the network optimization simulation setup shown in figure A.5 in the appendix to evaluate both the S11 and S22 parameters.

Stability

Another important property of the two-stage amplifier is to ensure that it's unconditionally stable. In chapter 4 and 5 the transistor stability were evaluated using the S-parameters, which is only valid when considering a network with one or none active components. If a network has multiple active components, as in the in the two-stage amplifier, the stability is not certain even though each stage is stable on its own. A method for evaluating the stability is by using the STAN circuit stability analysis tool [9, 10], which can identify the poles and zeros of the whole circuit and thereby determine the stability.

Measurements

Chapter 7

Measurements

In this chapter we will look at the measurement results from both the small-signal and large-signal measurements and compare these to the simulated results. The measurement setups are also shown.

7.1 Small-signal measurements

7.1.1 Measurement setup

For the small-signal measurements the E8364B PNA Series Network Analyzer [1] from Agilent Technologies are used with an auxiliary CPX200DP Dual DC Power Supply [2] from Aim-TTi as shown in figure 7.1. Two 10dB attenuators are also attached to port 2 of the network analyzer as it can only withstand a maximum input power of +30dBm.

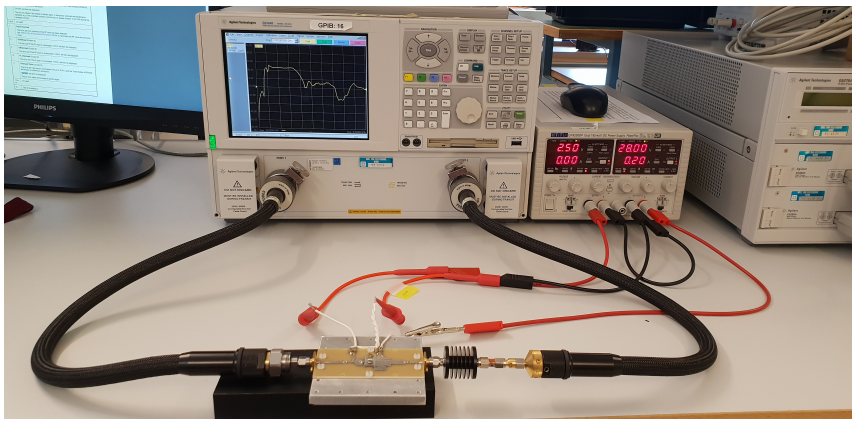


Figure 7.1: Measurement setup for small-signals, using a series network analyzer and a power supply.

7.1.2 Power stage amplifier characteristics

The small-signal measurement results of the power stage amplifier are shown in figure 7.2 and the simulated results are shown in figure 7.3 for comparison. The same flat gain of 12.5-13.2dB are present in both the measurement and simulation in the frequency band 1.0-3.0GHz, although a undesired higher gain peak is present at 1GHz in the measurements. Evidently an extra 1Ghz of bandwidth below the intended frequency band have been attained through the matching.

Both at approximately 500MHz and at 1GHz the same response is present, and we can also see some of the same tendencies at 4GHz and 7GHz. One possible source for this response could be the occurrence of oscillations, possibly due to the lower capacitance at the DBN. However, adding the Murata capacitor used in the GBN did alter the characteristic

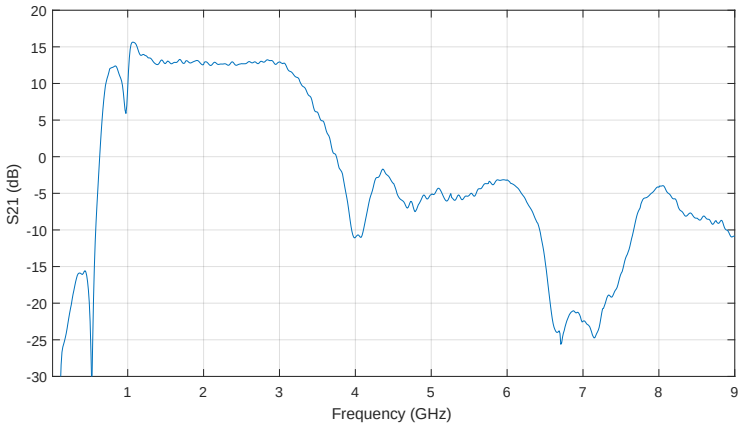


Figure 7.2: Measured small-signal gain of the power stage amplifier from 10MHz to 9GHz.

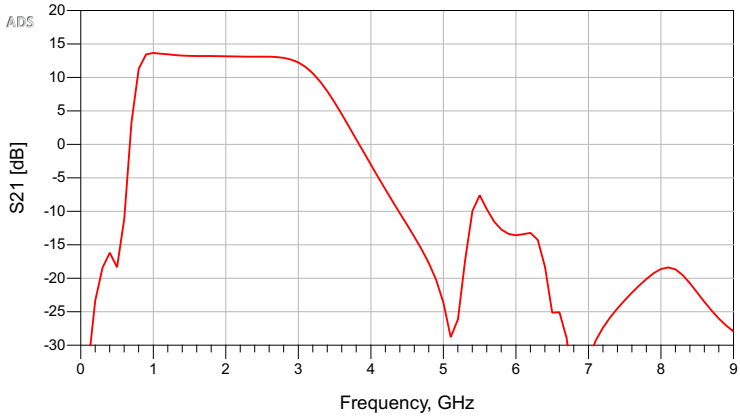


Figure 7.3: Simulated small-signal gain of the power stage amplifier from 10MHz to 9GHz.

to some degree, but the same response remained. Changing the impedances at different points on the transmission lines also did not affect the response. Thus, the last theory must be that the characteristics of either of the capacitors changes with frequency from capacitive to inductive and back again. By recollecting the design of the bias networks, some parallel combination of capacitors tended to make twirls at the left side of the smith chart at low frequencies. If this twirl is located close to the real axis and traverse both the capacitive and inductive half planes of the smith chart it would explain the response. From this hypothesis we can deduce that the bias network must have a twirl at the left side of the smith chart passing the real axis at 500MHz and 1GHz; then it passes the real axis at the right side of the smith chart at 4GHz; and again passes the real axis at the left side of the smith chart at 7GHz. Hence, changing the combination of capacitors could prevent the twirl and result in a characteristics more similar to the simulated characteristics.

7.1.3 Driver stage amplifier characteristics

The small-signal measurement results of the driver stage amplifier are shown in figure 7.4 and the simulated results are shown in figure 7.5 for comparison. The simulated results show a much flatter gain than what is achieved in the measurement results. As the simulations predict 15dB gain in the 1.4-3.0GHz band, the measurements show a frequency band of 1.0-2.7GHz with a maximum gain of 18dB at the edges and a minimum gain of 15dB at 1.8GHz. Noticeably the same response as with the power stage is present, where the twirl seems to be shifted relative to the twirl of the power stage. Hence, we've already discussed how to resolve

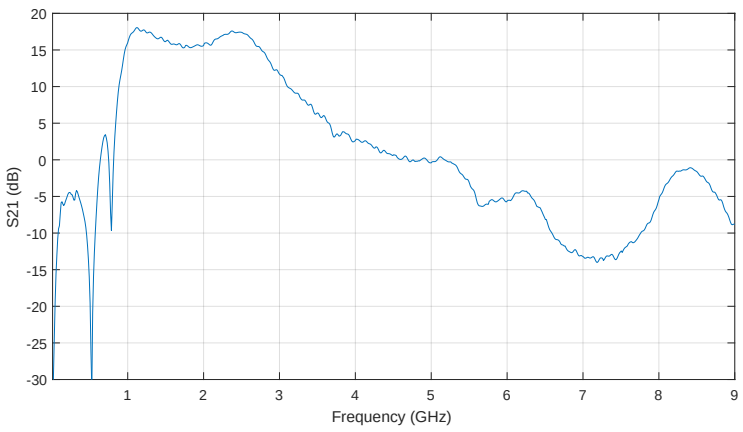


Figure 7.4: Measured small-signal gain of the driver stage amplifier from 10MHz to 9GHz.

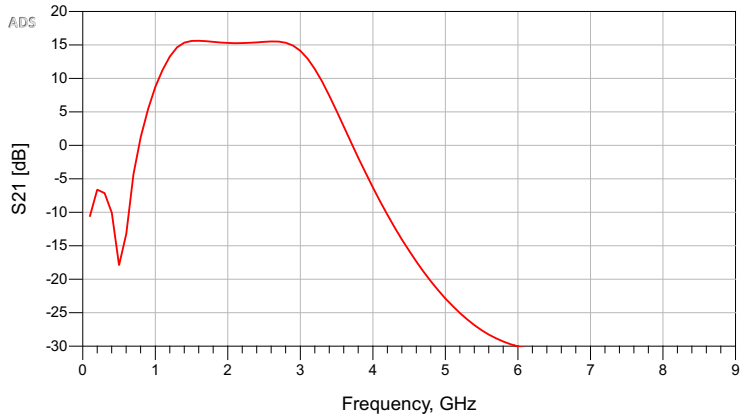


Figure 7.5: Simulated small-signal gain of the driver stage amplifier from 10MHz to 9GHz.

that problem. Another discrepancy between the measured and simulated results is the ripple in the extended frequency band. Recollecting the design of the stabilization network this typical characteristic were present depending on the combination of resistor and capacitor values. Hence, the ripples could be adjusted by changing the RC response of the stabilization network.

7.1.4 Two-stage amplifier characteristics

The small-signal measurement results of the two-stage amplifier are shown in figure 7.6 and the simulated results are shown in figure 7.7 for comparison. The simulation predicts a relatively flat small-signal gain of 27.9-29.0dB gain in the frequency band 2.0-3.0GHz. Some extra bandwidth is also attained below 2GHz with 4dB less gain and an undesirable peak of

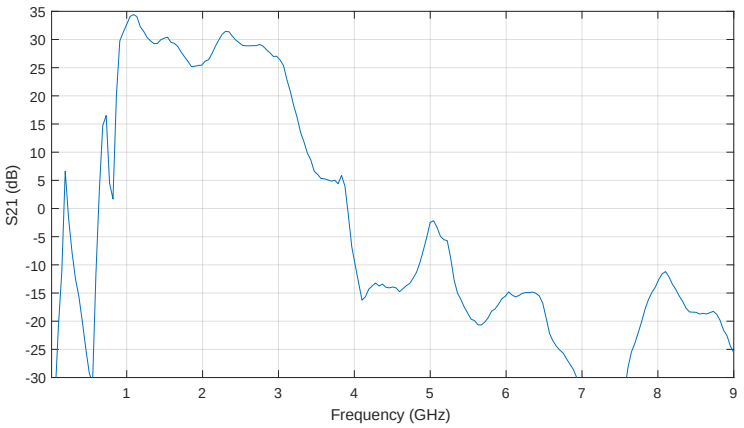


Figure 7.6: Measured small-signal gain of the two-stage amplifier from 10MHz to 9GHz.

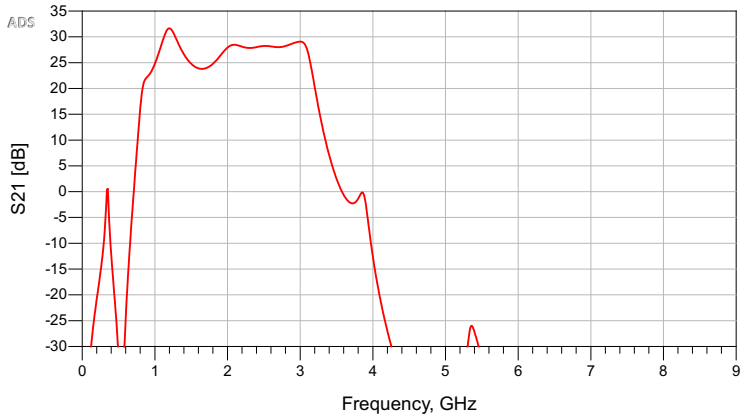


Figure 7.7: Simulated small-signal gain of the two-stage amplifier from 10MHz to 9GHz.

31.6dB at 1.2GHz. In the measurement results the gain flatness at 2.0-2.8GHz from the simulations is lost and the gain drop has moved from 1.8GHz up to 2.0GHz, which is undesirable. The gain peak at 1.2GHz has also increased by 3dB and moved down to 1GHz.

By comparing the results and the analysis of the power and driver stage with the two-stage we can see a very similar characteristics. The frequency band ripples of the driver stage, the 1GHz gain peak of the power amplifier, the bandwidth of both stages and the bias network twirl effects seem to be present also for the two-stage amplifier.

7.2 Large-signal measurements

7.2.1 Measurement setup

For the large-signal measurements an SMU200A Vector Signal Generator [25] is used in conjunction with an FSQ40 Signal Analyzer [24], both from Rhode&Schwarz, with different auxiliary power supplies (EL302Tv [3], EL302 [3], CPX200DP [2] and EL355TP [3]) from Aim-TTi, as shown in figure 7.8. Additional equipment in the setup are: a driver amplifier with 12.5dB gain in the 0.5-5.0GHz frequency band [22] designed by Morten Olavsbråten; an UIY-BCI5049B coaxial isolator [27] from UIY with 17dB minimum isolation in the 1.5-3.0Ghz range; a couple of model 5292 broadband high directivity couplers [20] from Narda with a minimum directivity of 28dBm and a nominal coupling of 13dB in the 1-18GHz range; a 5910_SMA-50-010 10W 10dB attenuator [14] from Huber+Suhner; and a T2516 25W 50Ω dummy load [21] from Narda-ATM. Additional fans and heatsinks are use to cool down the

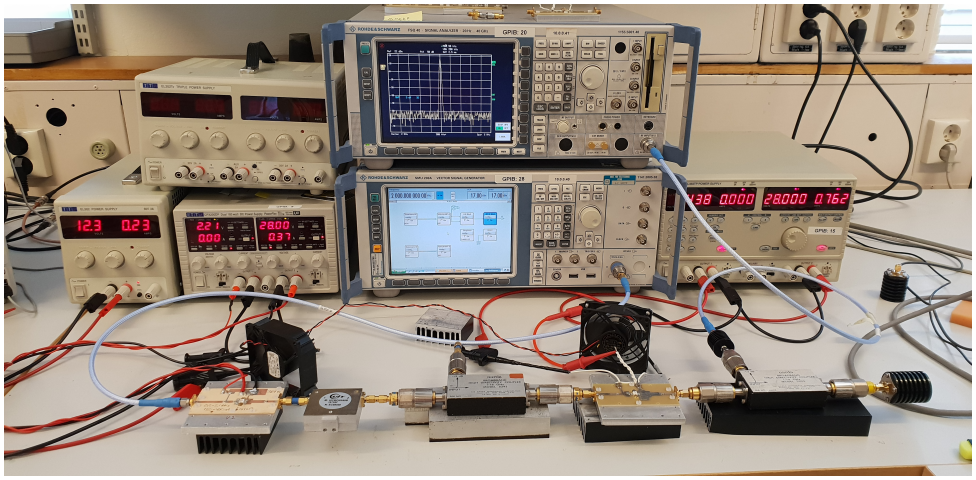


Figure 7.8: Measurement setup for large-signals, using a signal generator, a signal analyzer and some power supplies.

amplifiers, and a ML2438A power meter [4] from Anritsu is available if more accurate accurate power measurements are needed. The generator, analyzer and CPX200DP and EL355TP power supplies are connected via GPIB to a computer running each measurement script and plotting the results in MATLAB.

7.2.2 Calibration

In order to perform the measurement of the Device Under Test (DUT) only and not the whole setup, the measurements must be calibrated to the input and output reference planes of the DUT. This is achieved by measuring the whole setup and subtracting the effects of the input and output networks in MATLAB. Firstly, a measurement of the output network is performed and then a measurement of the input and output networks, connected with a through, is performed. These measurements are used as calibration sets to set the reference planes after a measurement of the whole setup is performed. The results from the calibration measurements are shown in figure 7.9 through 7.14, where the output power and transducer power gain versus frequency and input power; for the output network and through network are shown in figure 7.9-7.10 and 7.11-7.12 respectively. The characteristics of the input network are calculated from the measurement of the output network and through network and presented in figure 7.13-7.14.

We can observe that the output network has a 23 dB loss as expected (-13dB coupling and -10dB attenuation), with an increasing loss toward the frequency limit of the broadband

coupler at 1GHz. Noticeably the signal generator also seem to to have a limited output power at a minimum of 25dBm varying over 5dB in the 1.0-3.5GHz range. For the through network we can see the same trends from the output network in addition to frequency limitations of the isolator outside the 1.5-3.0GHz range. In the calculated results of the input network we can see that the amplifier operates linearly over the frequency band with 12.5dB transducer power gain, and the effects of the frequency limitations of the isolator and the power limitations of the signal generator is also present. From the calculations we can also see a measurement error of about 0.5dB.

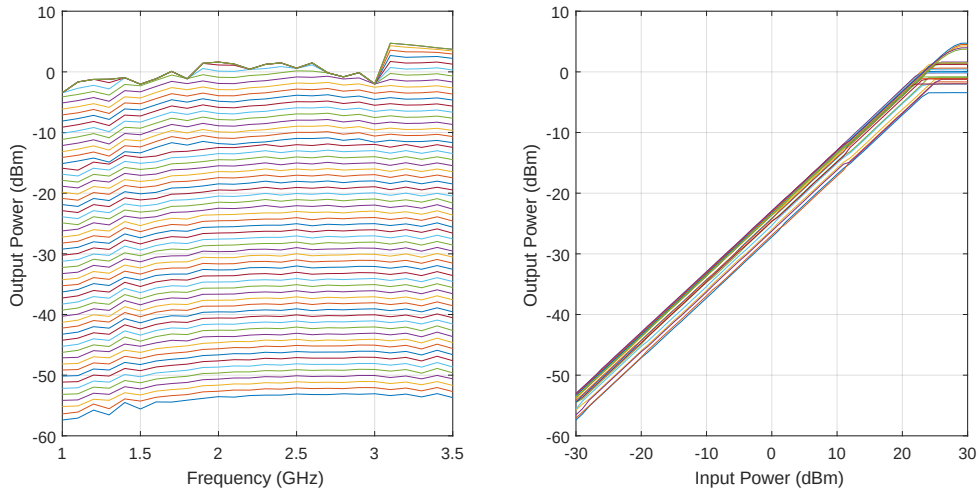


Figure 7.9: Measurements of the output power versus input power and frequency for the output network.

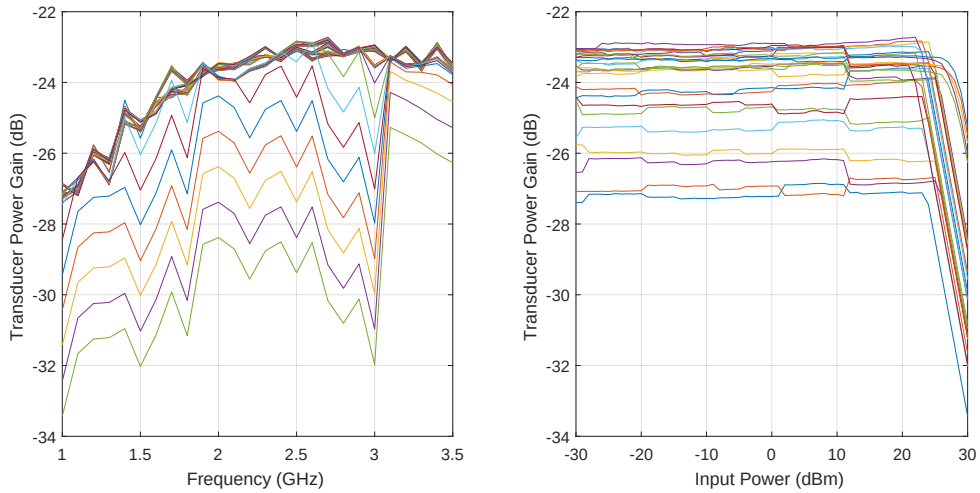


Figure 7.10: Measurements of the transducer power gain versus input power and frequency for the output network.

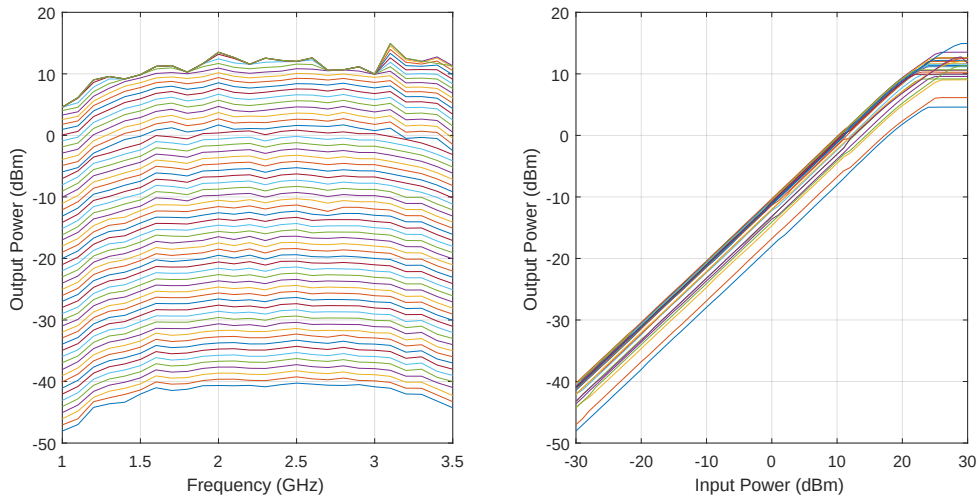


Figure 7.11: Measurements of the output power versus input power and frequency for the through network.

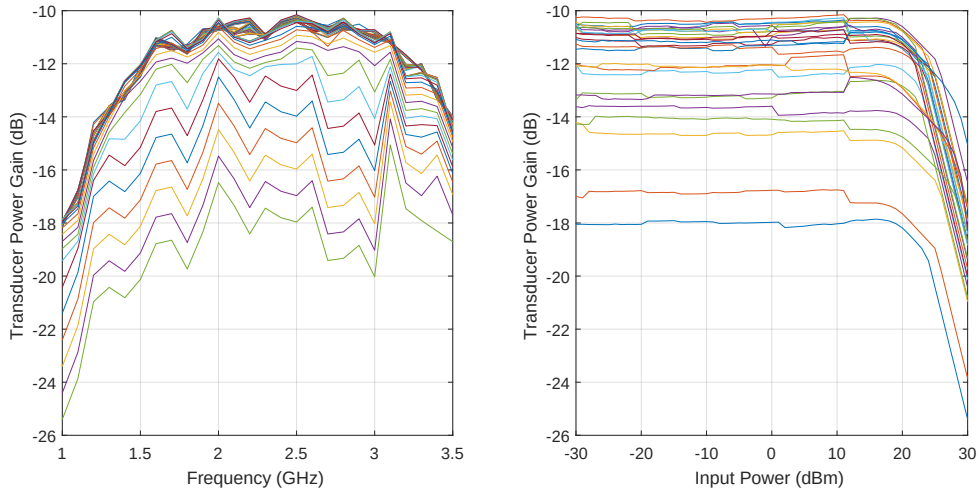


Figure 7.12: Measurements of the transducer power gain versus input power and frequency for the through network.

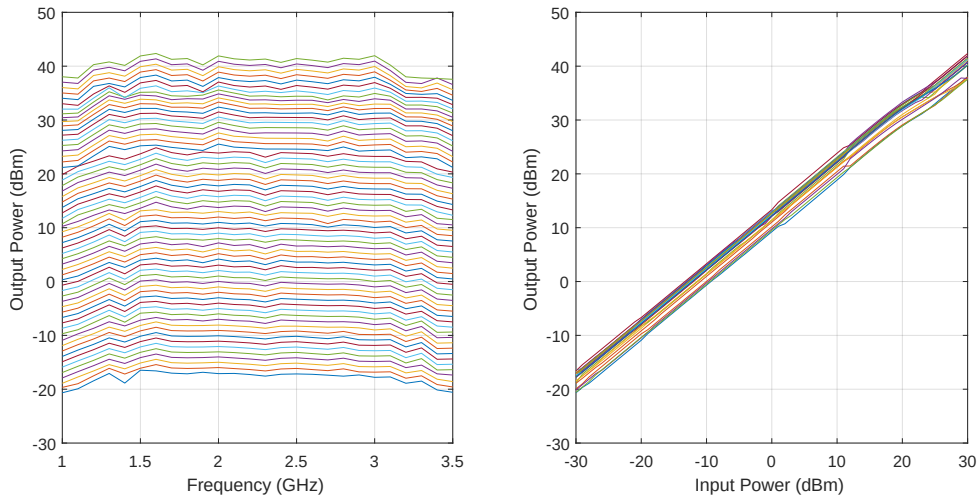


Figure 7.13: Measurements of the output power gain versus input power and frequency for the input network.

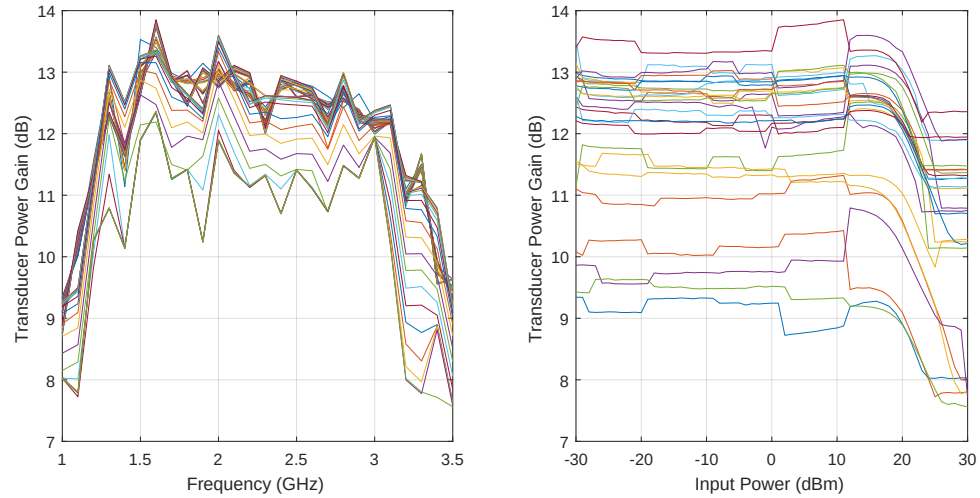


Figure 7.14: Measurements of the transducer power gain versus input power and frequency for the input network.

7.2.3 Measurement summary

The large-signal measurement results of the power amplifier stage, driver amplifier stage and the two-stage amplifier is added in appendix B.1, B.2 and B.3 respectively, and the key characteristics of the measurements are summarized in table 7.1 through 7.3 and shown in figure 7.15 through 7.17. The plots in the appendix show output power, transducer power gain, PAE, drain current, DC power consumption and power dissipation versus frequency and output power (the output power is plotted versus input power). The tables do not account for discrepancies in the measurements, so the reader is encouraged to compare the tables with the plots in the appendix for a more thorough analysis.

To conclude the power stage amplifier exhibit a mean transducer power gain of 13.5dB, a maximum linear output power of 25dBm, a mean saturated output power of 41.5dBm, and a mean peak PAE of 54% at a quiescent voltage bias of 28V and a quiescent current bias of 200mA. The driver stage amplifier exhibit a mean transducer power gain of 17.5dB, a maximum linear output power of 25dBm, a mean saturated output power of 37.8dBm, and a mean peak PAE of 55% at a quiescent voltage bias of 28V and a quiescent current bias of 165mA. The two-stage amplifier exhibit a mean transducer power gain of 29.8dB, a maximum linear output power of 25dBm, a mean saturated output power of 41.3dBm, and a mean peak PAE of 44.5% at a quiescent voltage bias of 28V and a quiescent current bias of 165mA and 200mA.

As a quick note to the reader in regards to the resonance responses discussed in the small-signal measurement section *7.1.2 Power stage amplifier characteristics*, some last-minute experiments with the bias network capacitors were performed in order to test the hypothesis stated. It showed that any of the parallel combination of the Murata and Johanson capacitors used created the resonance at specific frequency. Both the 15pF and 18pF seemed to have a resonance around 1GHz. Larger capacitance values moved the gain drop downwards in frequency and vice versa for smaller capacitances. From the datasheet of the R14S capacitors [15] we can see that the series resonance frequency is estimated to be at 3-4GHz at 16 mil-thick Rogers 4003C substrate, highly depending on the substrate.

Table 7.1: Properties of the power stage amplifier from the large-signal measurements.

Property	Symbol	Min.	Mean	Max.	Unit	Condition
Saturated Output Power	P_{sat}	38.41	41.55	43.10	dBm	
Max Linear Output Power	$P_{lin.max}$	-	25	-	dBm	
Transducer Power Gain	G_t	12.76	13.45	14.66	dB	$P_{del} < P_{lin.max}$
Max Power Added Efficiency	PAE_{max}	51.36	55.88	62.29	%	
Drain Current	I_D	146	200*	1043	mA	$*I_{DQ}$
DC Power Consumption	P_{DC}	4.09	5.6*	29.20	W	$*I_{DQ} \cdot V_{DSQ}$
Power Dissipation	P_{diss}	3.50	5.6*	13.42	W	$*P_{DC}$

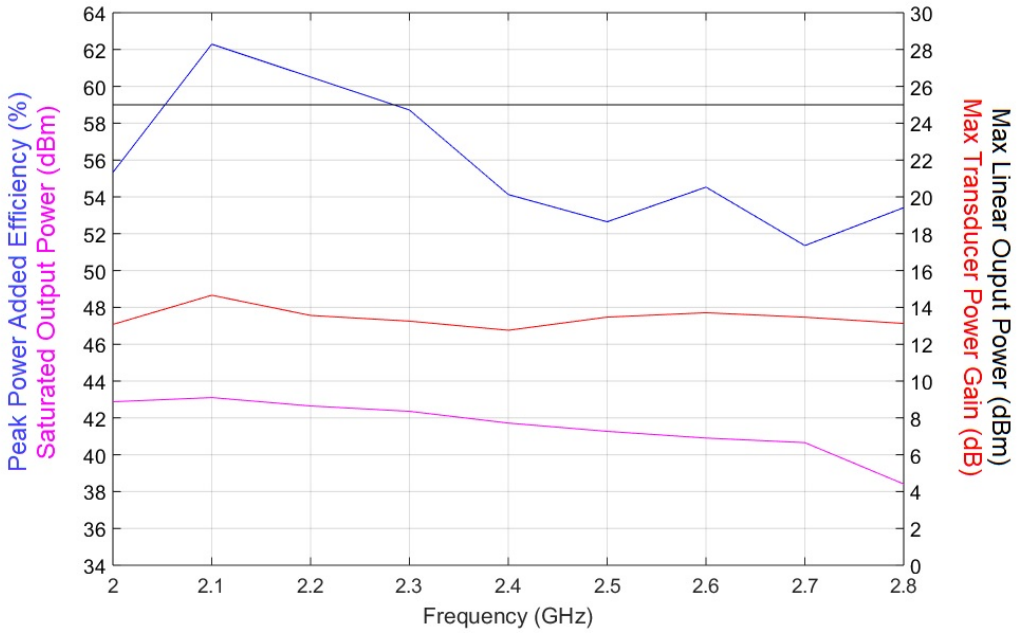


Figure 7.15: Measured performance of the power stage amplifier extrapolated from the corresponding plots in the appendix.

Table 7.2: Properties of the driver stage amplifier from the large-signal measurements.

Property	Symbol	Min.	Mean	Max.	Unit	Condition
Saturated Output Power	P_{sat}	35.59	37.80	40.75	dBm	
Max Linear Output Power	$P_{lin.max}$	-	25	-	dBm	
Transducer Power Gain	G_t	14.96	17.45	18.91	dB	$P_{del} < P_{lin.max}$
Max Power Added Efficiency	PAE_{max}	49.49	63.66	93.44	%	
Drain Current	I_D	0.07	165*	0.53	mA	$*I_{DQ}$
DC Power Consumption	P_{DC}	2.02	4.62*	14.92	W	$*I_{DQ} \cdot V_{DSQ}$
Power Dissipation	P_{diss}	0.43	4.62*	8.59	W	$*P_{DC}$

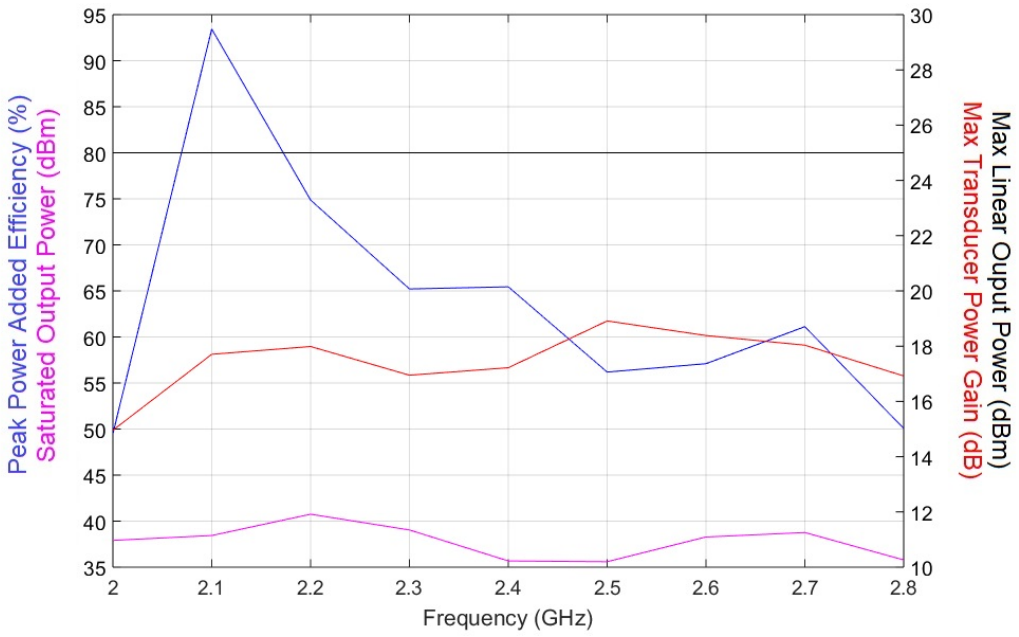


Figure 7.16: Measured performance of the driver stage amplifier extrapolated from the corresponding plots in the appendix.

Table 7.3: Properties of the driver stage amplifier from the large-signal measurements.

Property	Symbol	Min.	Mean	Max.	Unit	Condition
Saturated Output Power	P_{sat}	39.30	41.28	42.41	dBm	
Max Linear Output Power	$P_{lin.max}$	-	25	-	dBm	
Transducer Power Gain	G_t	25.31	29.84	32.71	dB	$P_{del} < P_{lin.max}$
Max Power Added Efficiency	PAE_{max}	37.41	44.45	52.44	%	
Drain Current						
Power Stage	I_D^{ps}	173.00	200*	1016.00	mA	$*I_{DQ}^{ps}$
Driver Stage	I_D^{ds}	83.00	165*	698.00	mA	$*I_{DQ}^{ds}$
Total	I_D^{ts}	341.00	365*	1662.00	mA	$*I_{DQ}^{ps} + I_{DQ}^{ds}$
DC Power Consumption						
Power Stage	P_{DC}^{ps}	4.84	5.6*	28.45	W	$*I_{DQ}^{ps} \cdot V_{DSQ}^{ps}$
Driver Stage	P_{DC}^{ds}	2.32	4.62*	19.54	W	$*I_{DQ}^{ds} \cdot V_{DSQ}^{ds}$
Total	P_{DC}^{ts}	9.55	10.22*	46.54	W	$*P_{DC}^{ps} + P_{DC}^{ds}$
Power Dissipation Total	P_{diss}	8.97	10.22*	31.69	W	$*P_{DC}$

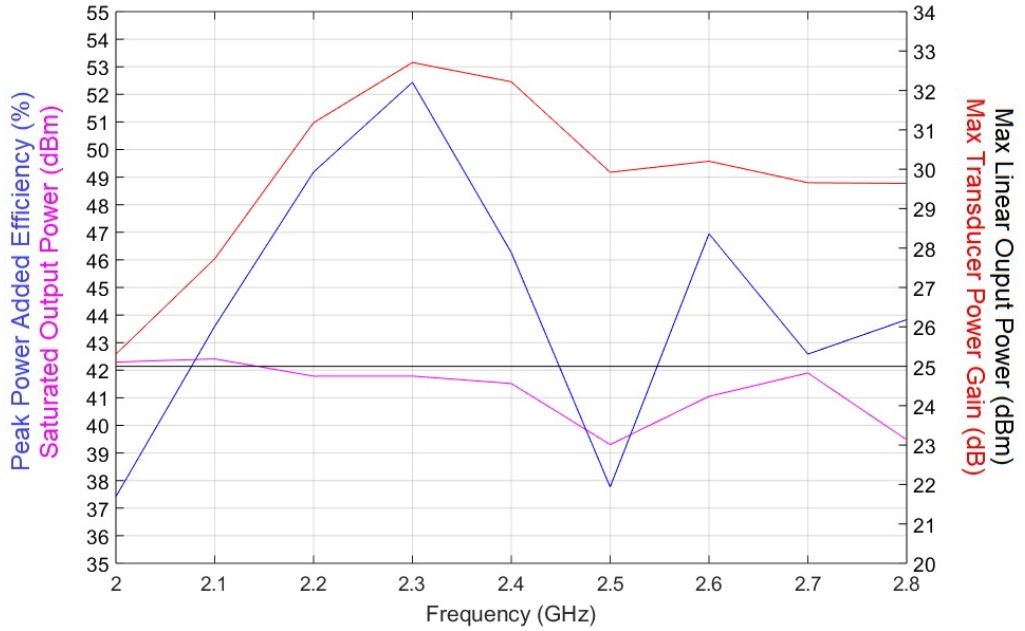


Figure 7.17: Measured performance of the two stage amplifier extrapolated from the corresponding plots in the appendix.

Discussion

Chapter 8

Discussion

Thesis summary

Throughout this master's thesis we have made a comprehensive analysis of the design process of a power amplifier. The steps in the design process have included a thorough loadline analysis, looking at linear output power, drain efficiency, transconductance and loadline resistance; a small-signal stability and gain analysis, using the S-parameters, Rollett's stability conditions and the geometric stability; and a large-signal analysis, using the harmonic load- and sourcepull techniques to find optimal impedances and performance contours.

The steps of the design process have included determination of quiescent operating bias, in order to decide the preliminary performance characteristics; determining the proper stabilization scheme, in order to satisfy the stability conditions and set the initial small-signal gain; a large-signal conformity analysis of the stabilized transistor, for affirmation of the large-signal analysis' correspondence to the small-signal and loadline analysis; a harmonic load- and sourcepull analysis, to find the optimal load and source impedances and the amplifiers sensitivity to mismatch; a network impedance trajectory optimization based on harmonic termination; and lastly a large-signal characterization of the power amplifier and layout generation. Additionally, the bias network must be determined either in advance or be designed as a part of the matching networks.

Small-signal gain and loadpull

During the design of the stabilization network, the small-signal gain was in part optimized for flatness within the frequency band. This would entail a very similar performance at the

optimal load impedances during loadpull, and the desired desired load impedances would be centered equivalently between each corresponding optimal load impedances. For example would the desired load impedance at 2.4GHz be centered in the middle of the the optimal impedances for power delivered and transducer power gain if the goals are weighted equally, and equivalently for 2.0GHz and 2.8GHz and other frequencies in the frequency band. Another approach is to create a higher peak in the small-signal gain in the frequency band and not consider the flatness as much, while ensuring a high and relatively flat MAG.The gain flatness of the amplifier would then be more dependant on the matching networks. During loadpull this would mean that the the desired load impedances e.g. would move away from the optimal load impedances for transducer power gain at a specific frequency if the small-signal gain at that frequency has peak. Hence, one could fine-tune the position of the desired load impedances as needed. The latter approach could however be very tedious and cumbersome, as one would need to iterate between the stabilization network optimization and loadpull optimization for each frequency in the frequency band.

Out-of-band desired load and source impedances

During the load- and sourcepull optimizations only three frequencies were used - the center and edge frequencies of the frequency band. One could argue that more of the in-band frequencies should have been evaluated, especially for broadband amplifiers, but for the most part using only these frequencies suffice. Evaluating the optimal impedances for multiple frequencies is also time consuming. Nevertheless, an evaluation of the out-of-band impedances could have been made to ensure e.g. a bandwidth only contained within the desired frequency band. The contour plots at these frequencies would especially be useful.

Simultaneous load- and sourcepull

The load- and sourcepull steps of the design process were in this thesis performed as separate parts. During loadpull the source were terminated in 50Ω, and during sourcepull the load was terminated in the OMN. Consequentially, when changing the source termination from 50Ω to the IMN, the optimal load impedances changes, and when changing the OMN the optimal source impedances changes again, resulting in an iterative design process. These loadpull and sourcepull could however be performed at the same time, thus finding a con-

vergent solution right away.

Two-stage amplifier stability

As discussed in chapter 6 the small-signal stability of each stage in a two-stage amplifier are not always sufficient to ensure stability of the whole amplifier. A more thorough stability evaluation of the amplifier should therefore have been made as discussed, but with limit time the two-stage amplifier had to be assumed stable which it was during the measurements.

Measurement accuracy

In the large-signal measurements we can see different measurement errors occurring resulting in larger variance in the samples, discontinuities and unreal performances. Especially the drain current measurements seem to be way off at some sample sets, which e.g. resulted in 95% PAE at one frequency and not the other frequencies for the driver stage amplifier. Other errors like the sudden steps in the transducer power gain for the power stage were also present. These errors could be minimized by remeasuring and updating the sample sets, but that would also have been time consuming process.

Loadpull measurements

In order to validate the loadpull and sourcepull simulations of the amplifiers, one could set up a loadpull and sourcepull measurements and evaluate the matching results. The simulation models in the PDK were assumed to be accurate models of the transistors and the measurements were confirmed at least a very close approximation, so the loadpull and sourcepull validation is left to a more in-depth characterization of the transistors themselves.

Iterative redesign

Although some experimentation with the surface-mount components were made, no detailed examination of the characteristics supplemented with simulations were performed. This trial-and-error method could somewhat have improved the characteristics of the amplifiers. However, from the experimentation that were performed it seemed that some iterative redesign would be appropriate to improve the circuit at the frequency band. A iterative

redesign is also tempting in order to use the entire extended frequency band, which would basically double the original bandwidth.

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Appendices

Appendix A

Simulation setups

A.1 Transistor I-V Characteristics

A.2 Network S-Parameters

A.3 Amplifier Large-signal Characteristics

A.4 Harmonic Load- and Sourcepull

A.5 Network Impedance Trajectory Optimization

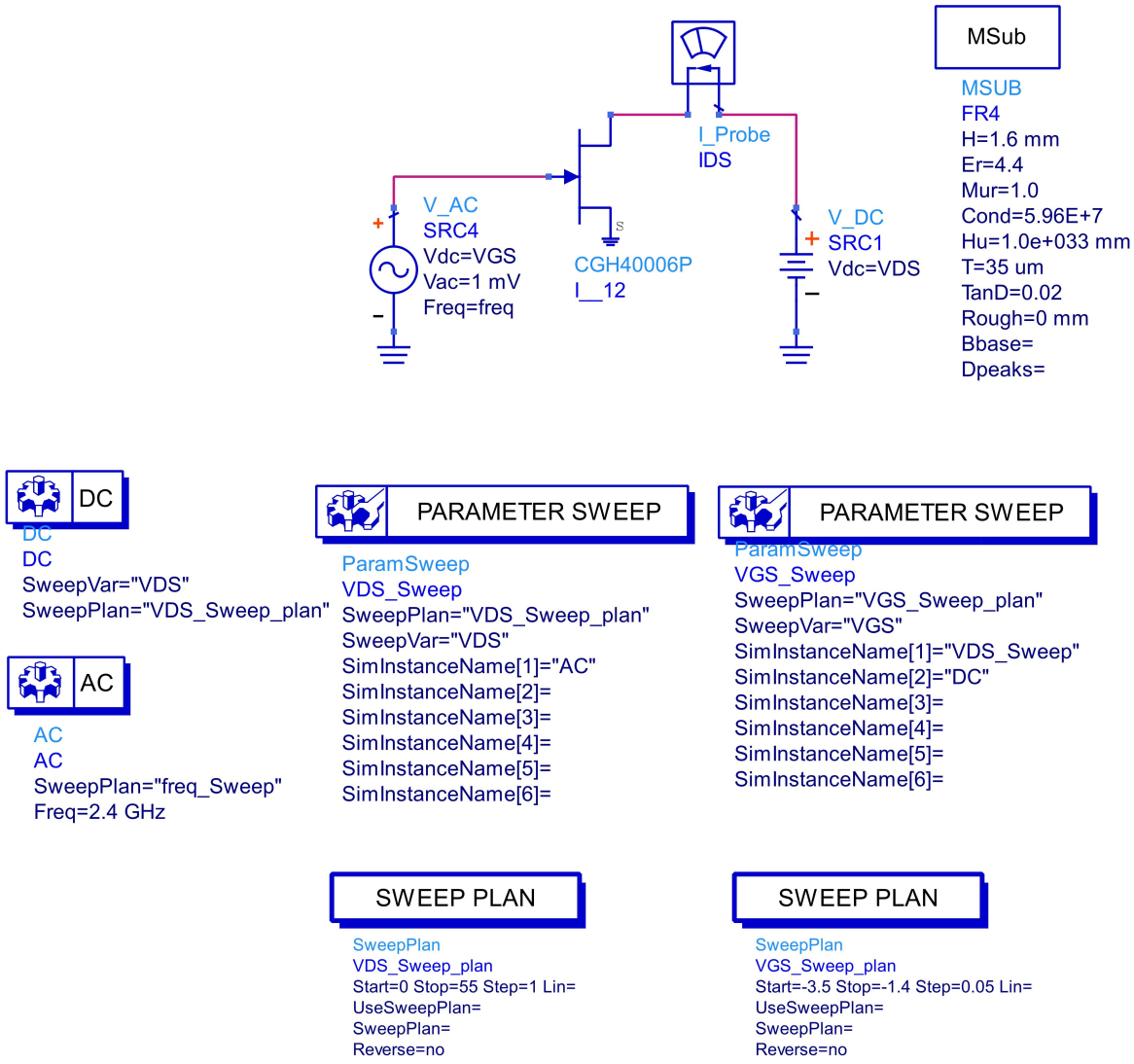

Figure A.1: The schematic simulation setup for calculating the I-V characteristics of a transistor and determine the properties of the transistor at different quiescent biases. Here, the CGH40006P transistor is evaluated for $0V \leqslant V_{DS} \leqslant 55$ and $-3.5V \leqslant V_{GS} \leqslant -1.4$ at DC operations and for a input signal at 2.4GHz.

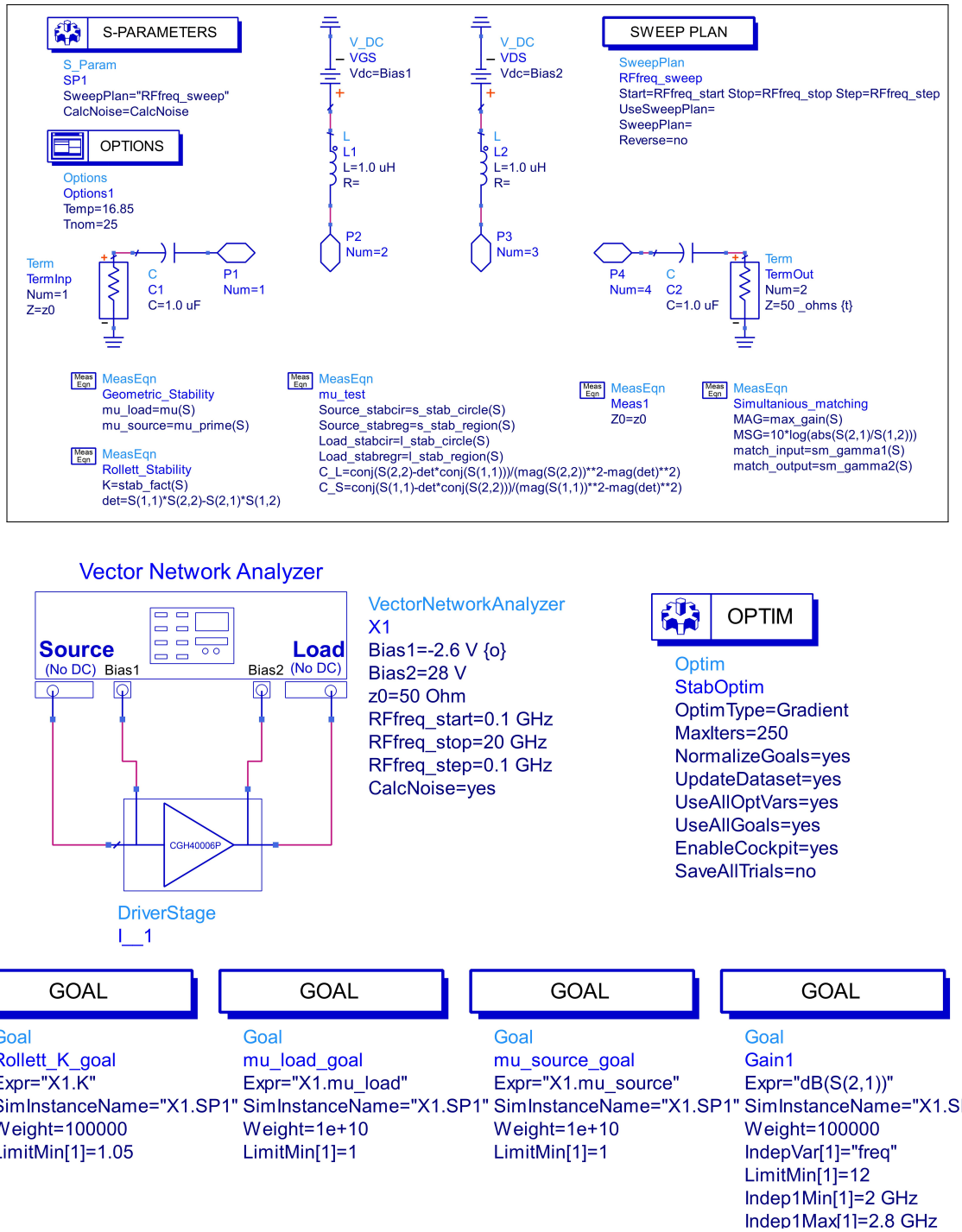

Figure A.2: The schematic simulation setup for calculating the S-parameters of a network, also showing the internal simulation schematic of the VNA. Here, the driver stage is evaluated at the quiescent bias from 100MHz to 20GHz, and the stability and small-signal gain optimization goals are shown.

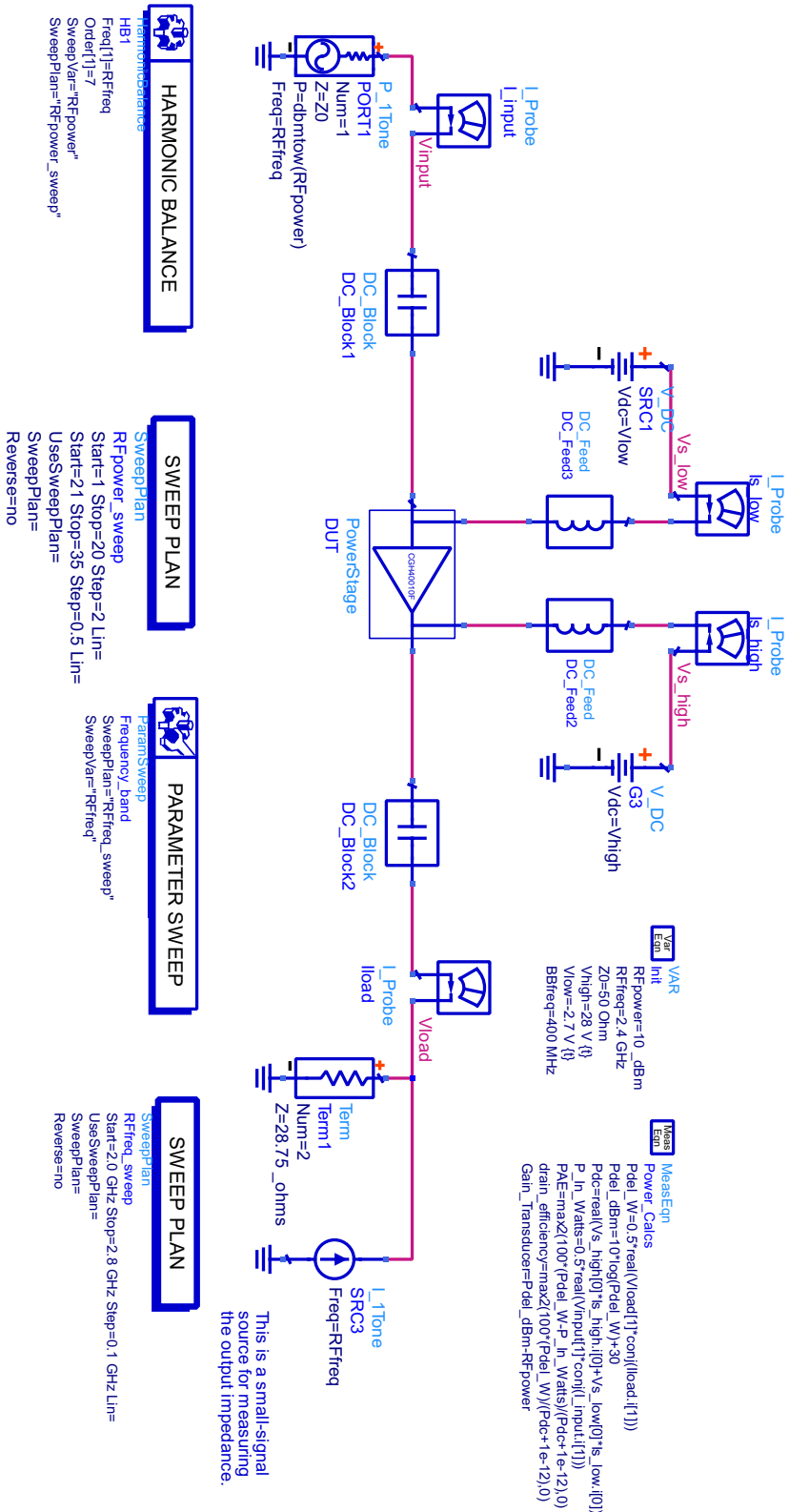

Figure A.3: The schematic simulation setup for calculating the large-signal characteristics of a an amplifier. Here, the power stage is evaluated at the quiescent bias for input powers from 0dBm to 35dBm in the frequency band (2.0-2.8GHz).

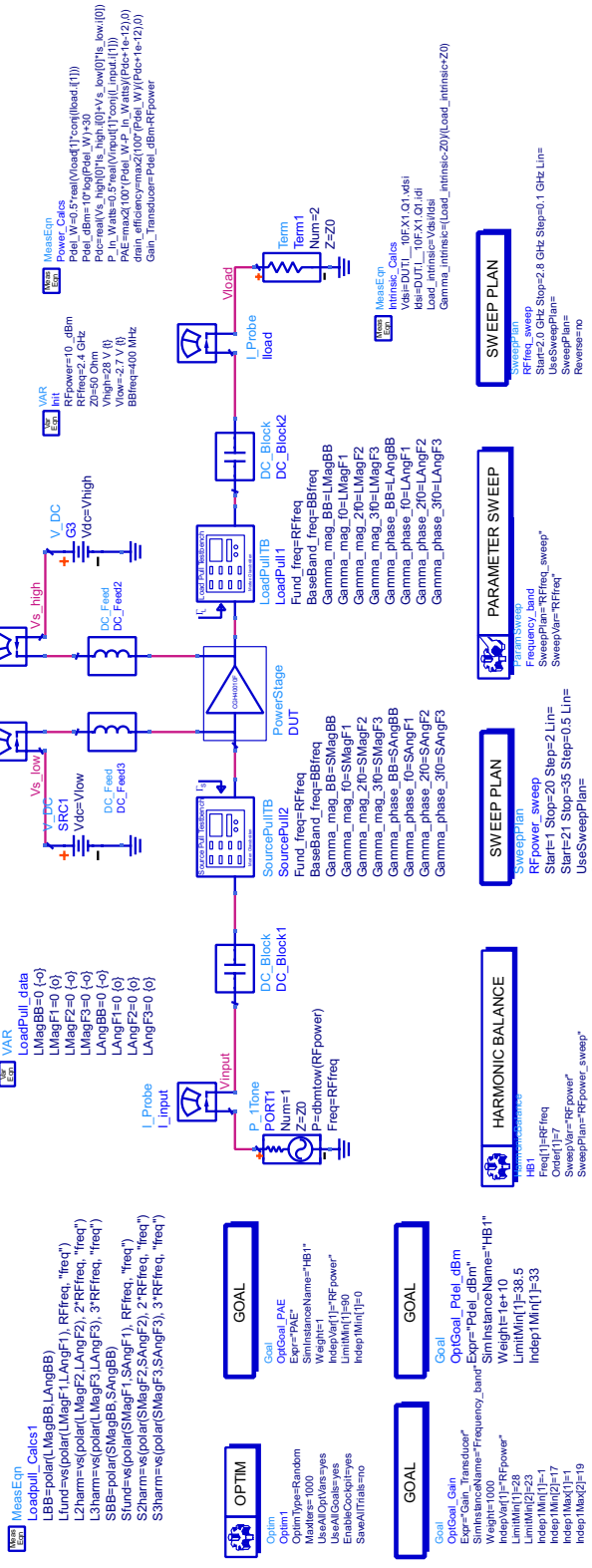

Figure A.4: The schematic simulation setup for performing harmonic load- and sourcepull of a network. Here, the power stage is evaluated at the quiescent bias for input powers from 1dBm to 35dBm at 2.4GHz. A large-signal simulation can also performed with this setup.

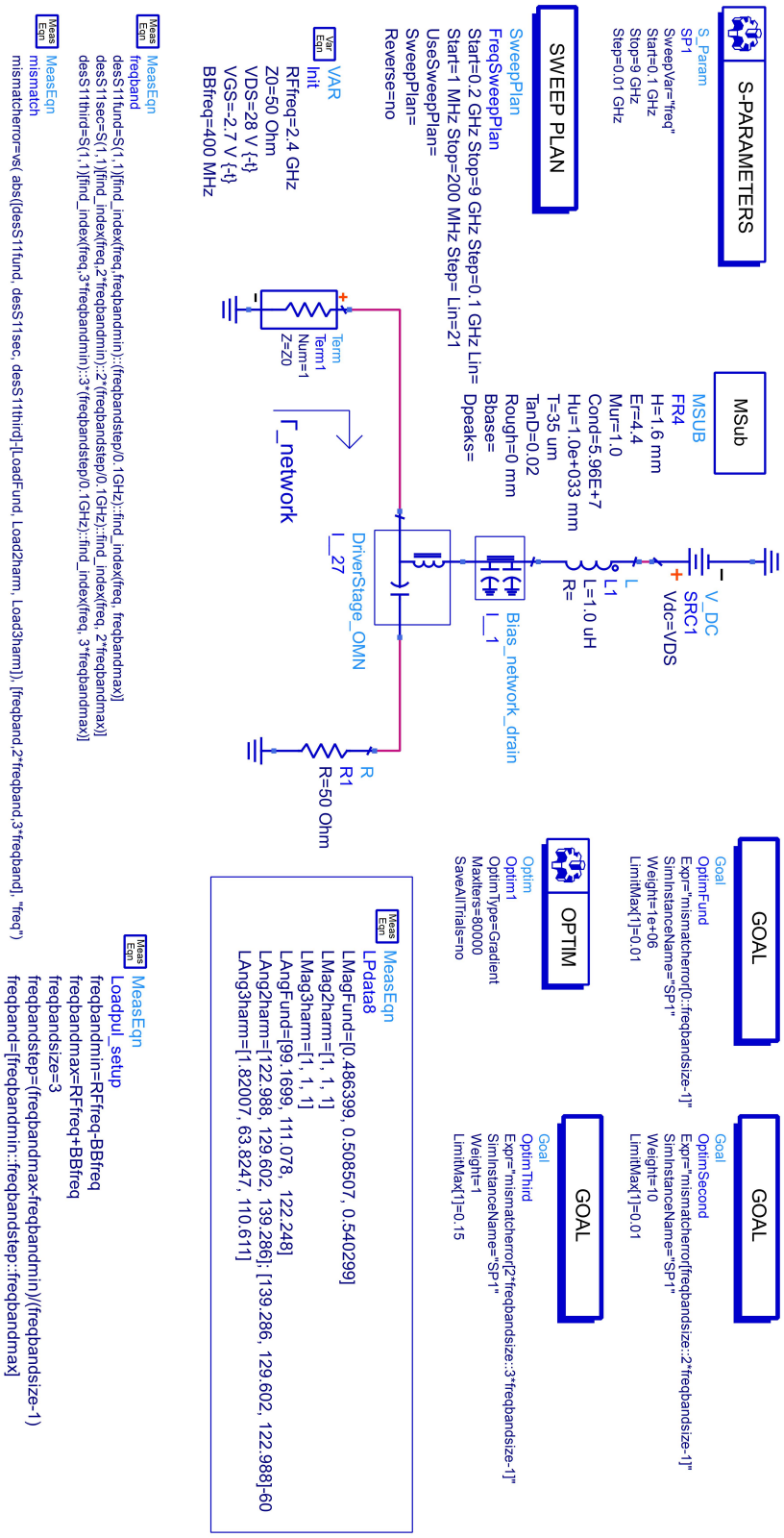

Figure A.5: The schematic simulation setup for optimization of the network input impedance. Here, the driver stage output matching network impedance trajectory is matched with the desired load impedances from the harmonic loadpull simulation.

Appendix B

Large-signal measurement results

B.1 Power stage amplifier

B.2 Driver stage amplifier

B.3 Two-stage amplifier

B.1 Power stage amplifier

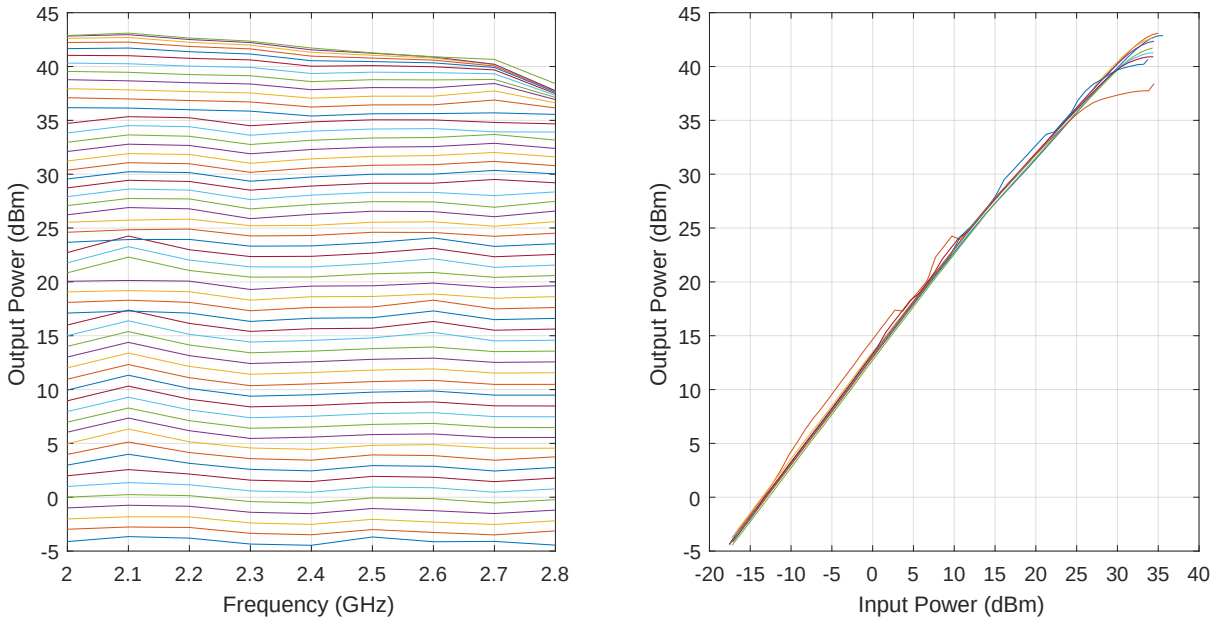

Figure B.1: Measurements of the output power gain versus input power and frequency for the power stage.

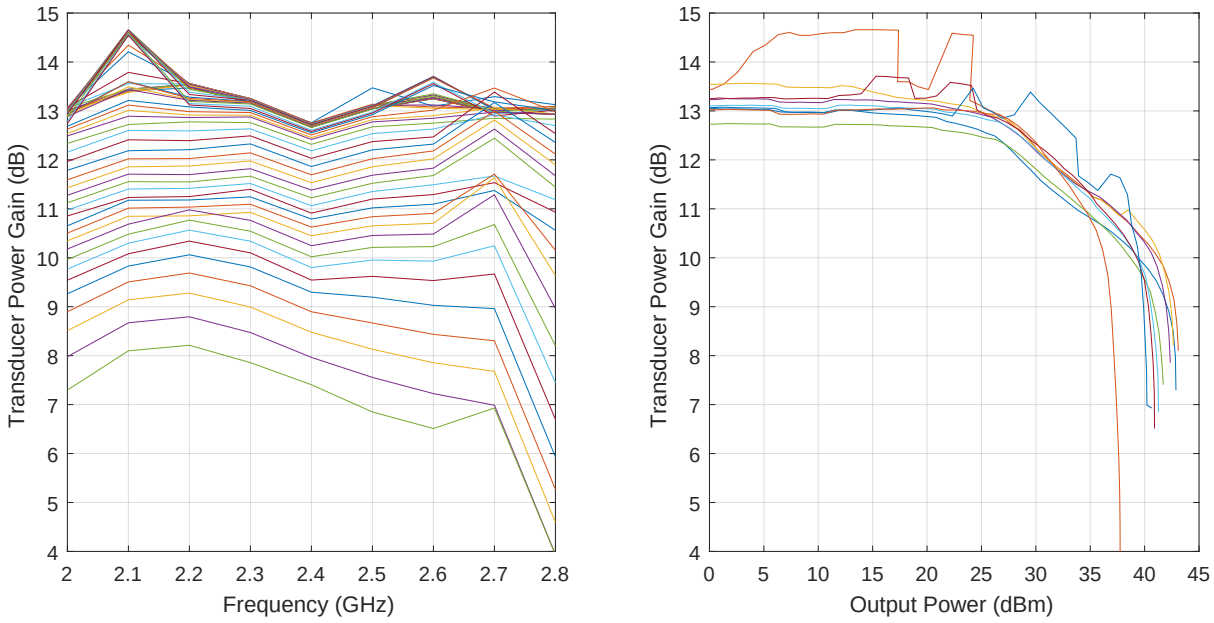

Figure B.2: Measurements of the transducer power gain versus input power and frequency for the power stage.

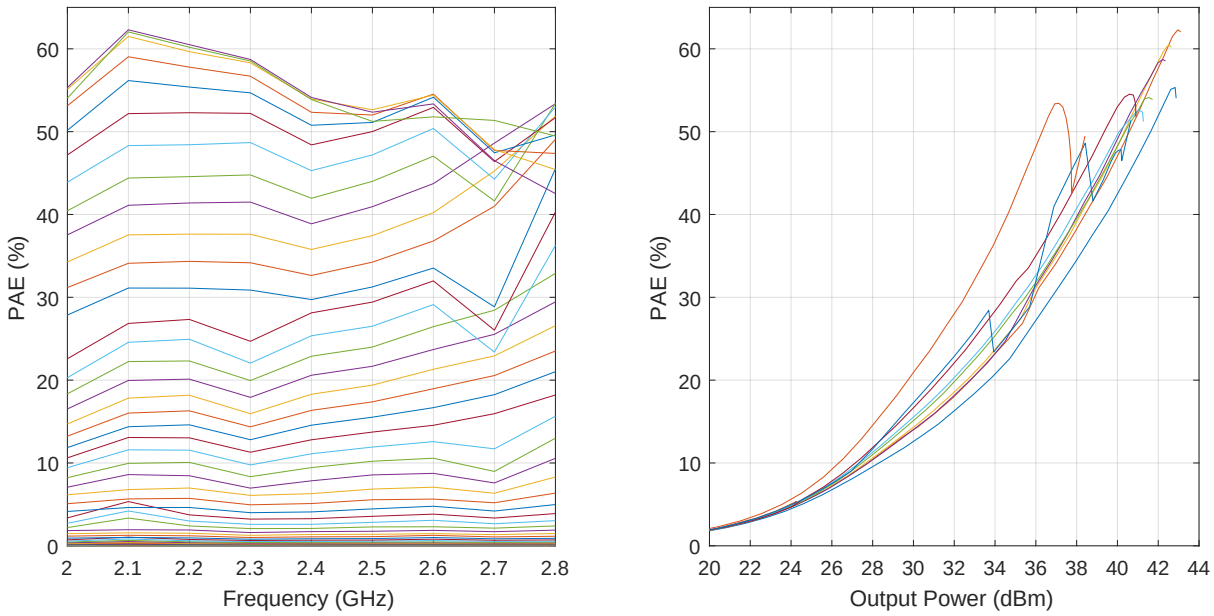

Figure B.3: Measurements of the PAE versus input power and frequency for the power stage.

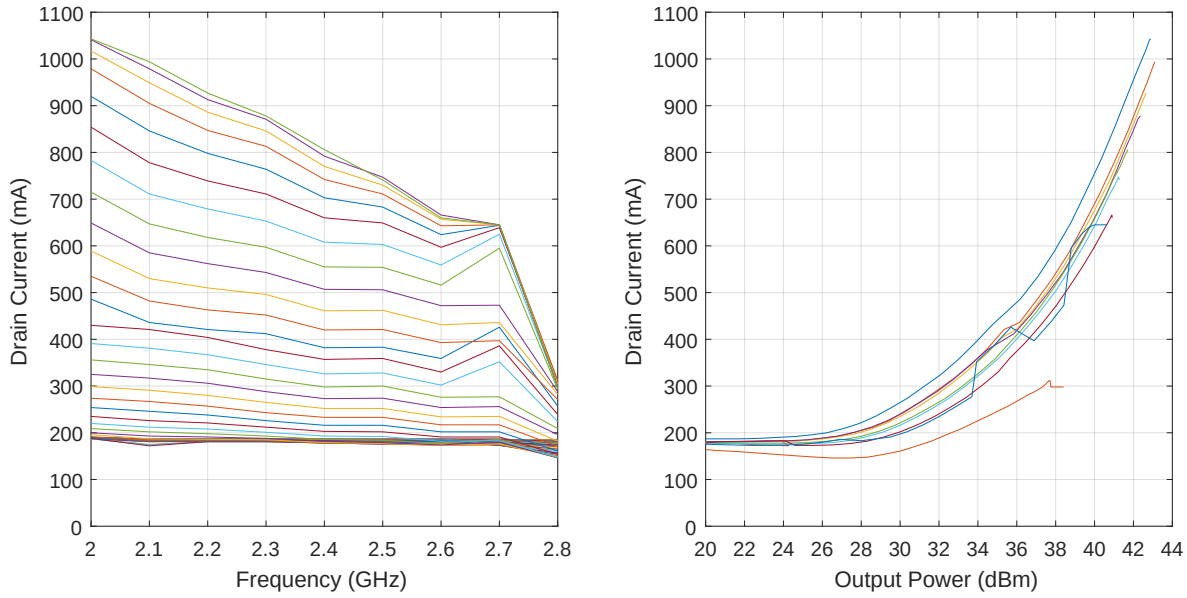

Figure B.4: Measurements of the drain current versus input power and frequency for the power stage.

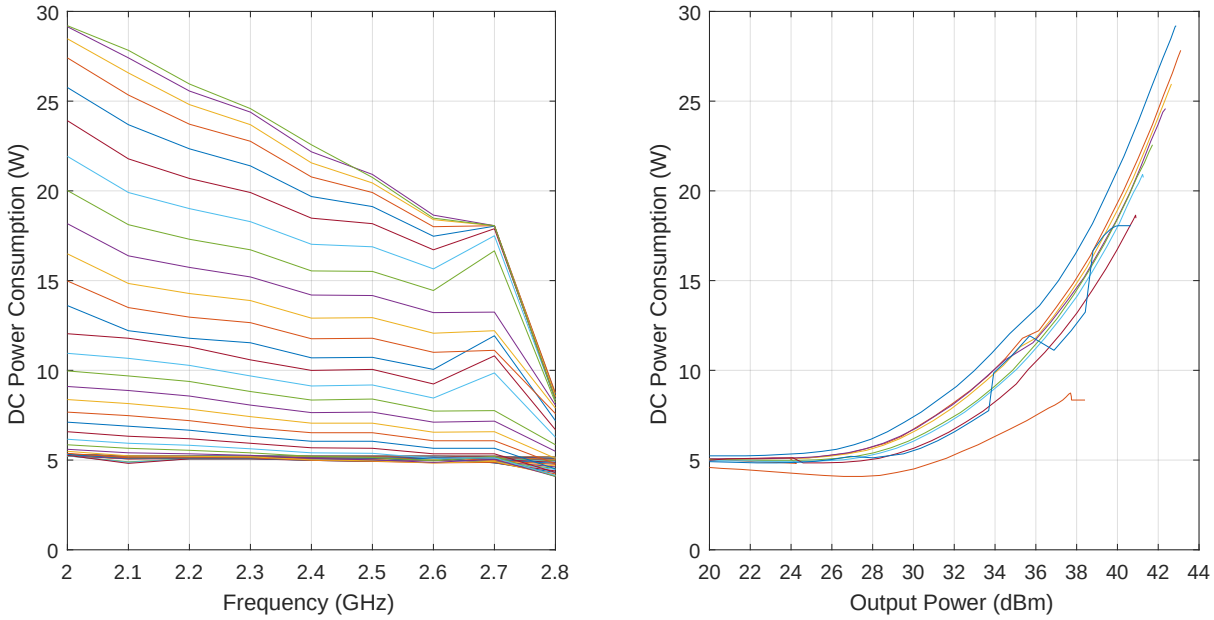

Figure B.5: Measurements of the DC power consumption versus input power and frequency for the power stage.

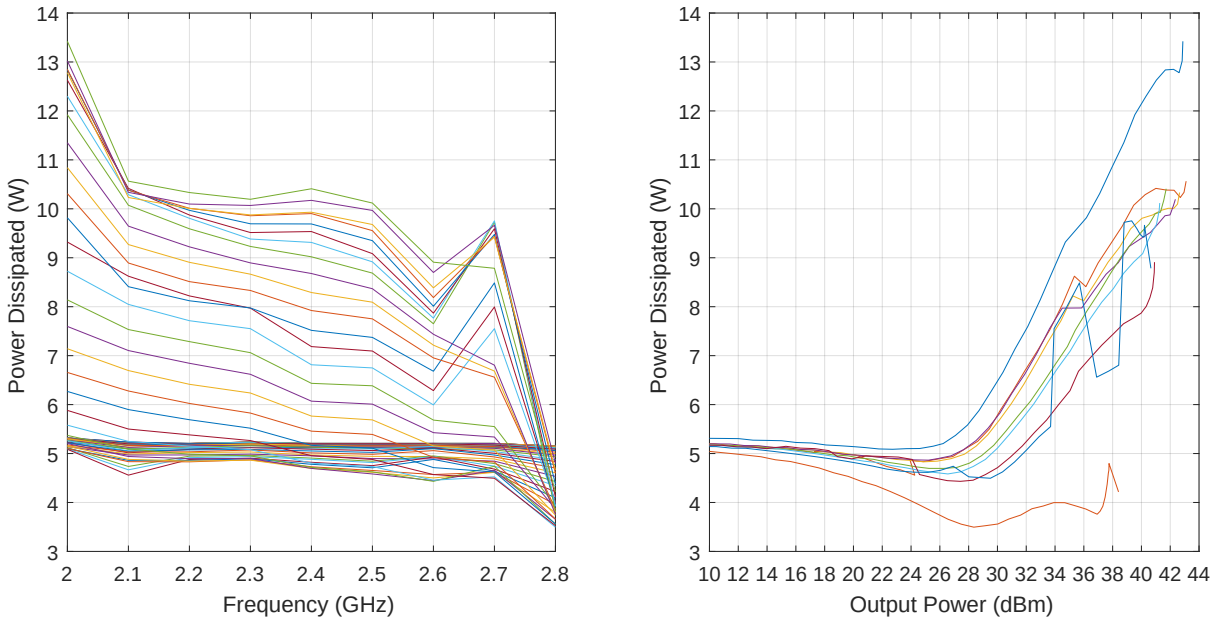

Figure B.6: Measurements of the power dissipated versus input power and frequency for the power stage.

B.2 Driver stage amplifier

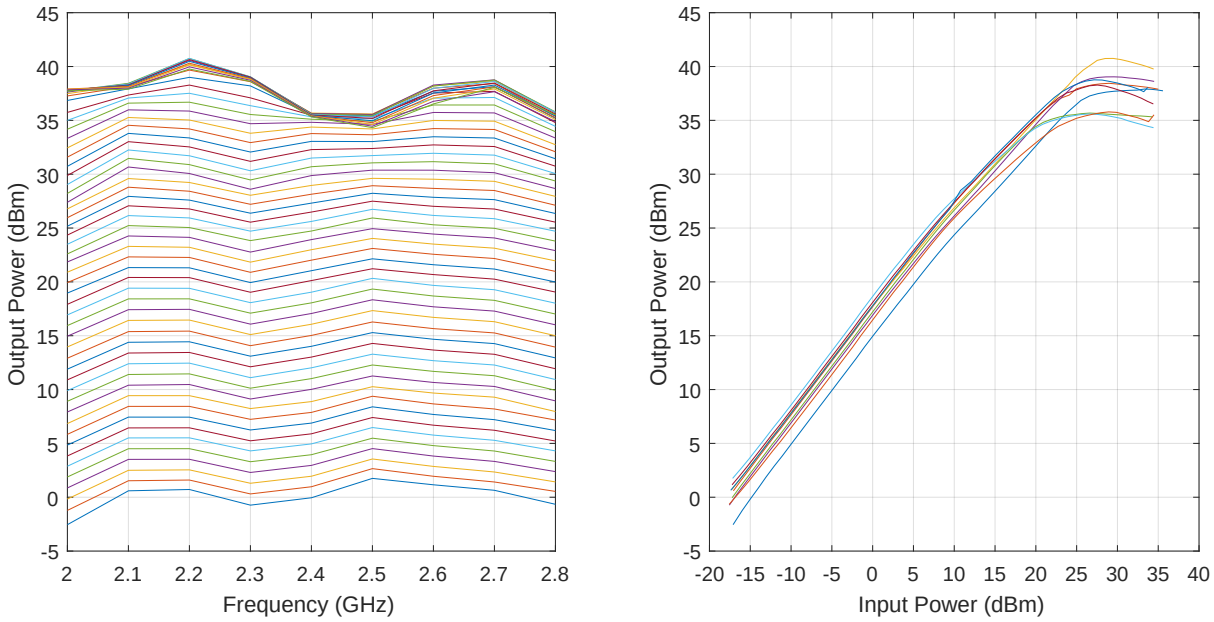

Figure B.7: Measurements of the output power gain versus input power and frequency for the driver stage.

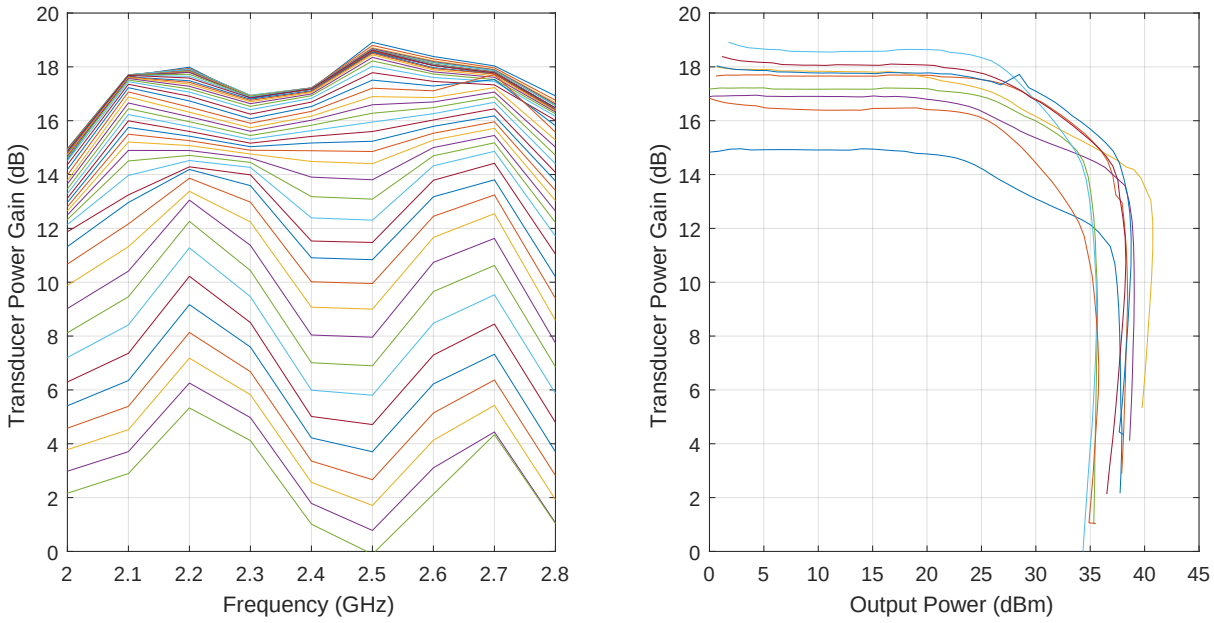

Figure B.8: Measurements of the transducer power gain versus input power and frequency for the driver stage.

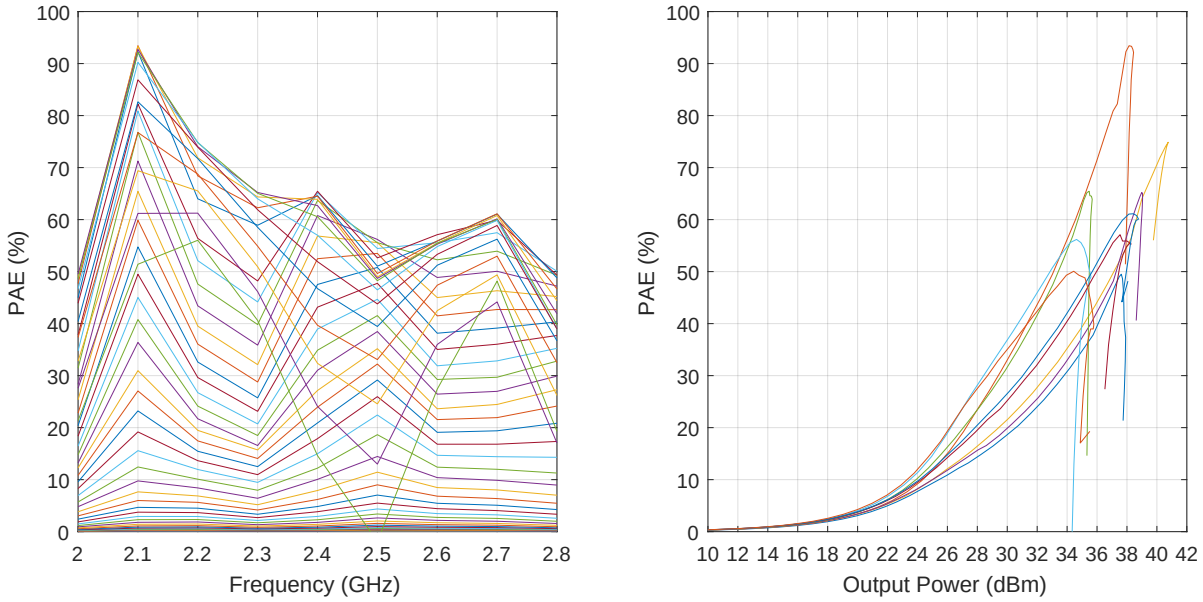

Figure B.9: Measurements of the PAE versus input power and frequency for the driver stage.

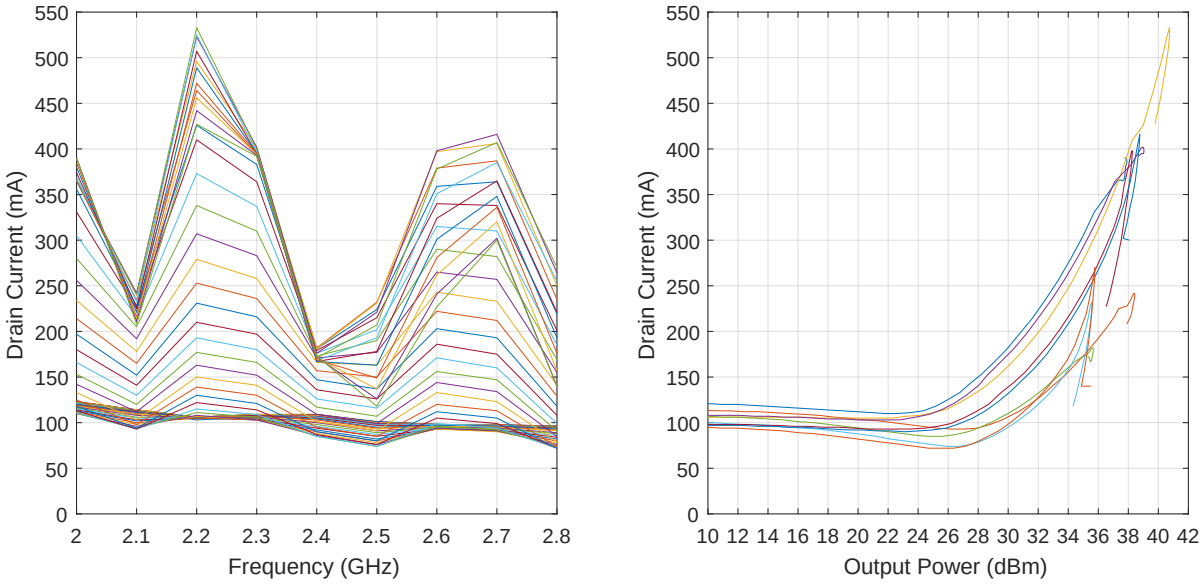

Figure B.10: Measurements of the drain current versus input power and frequency for the driver stage.

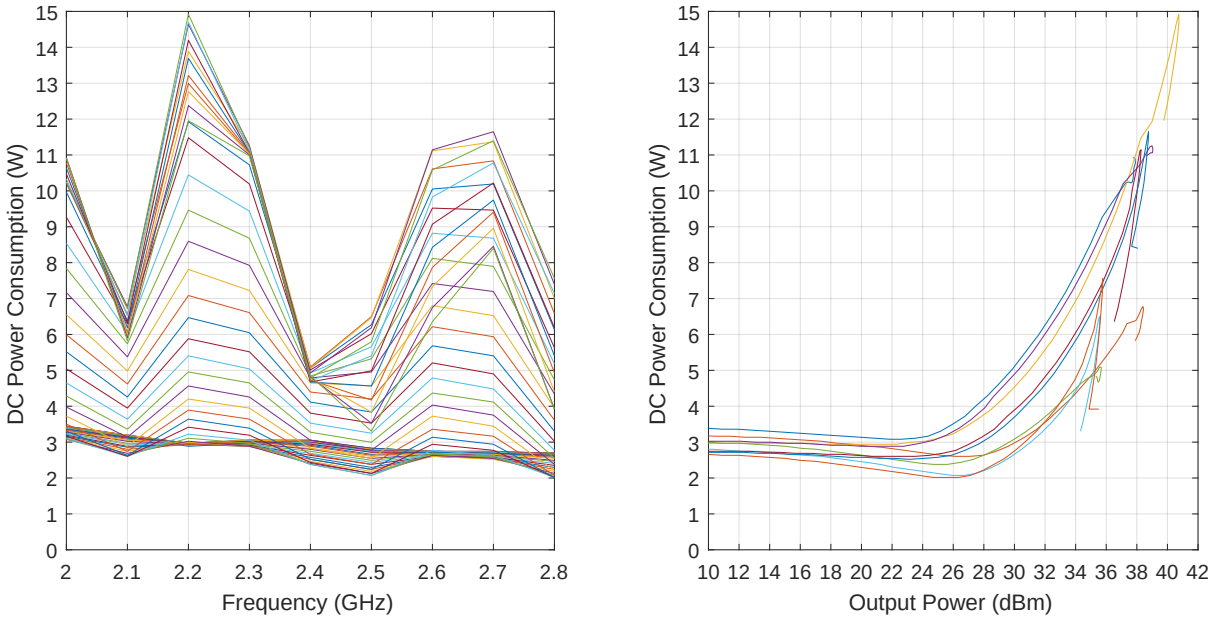

Figure B.11: Measurements of the DC power consumption versus input power and frequency for the driver stage.

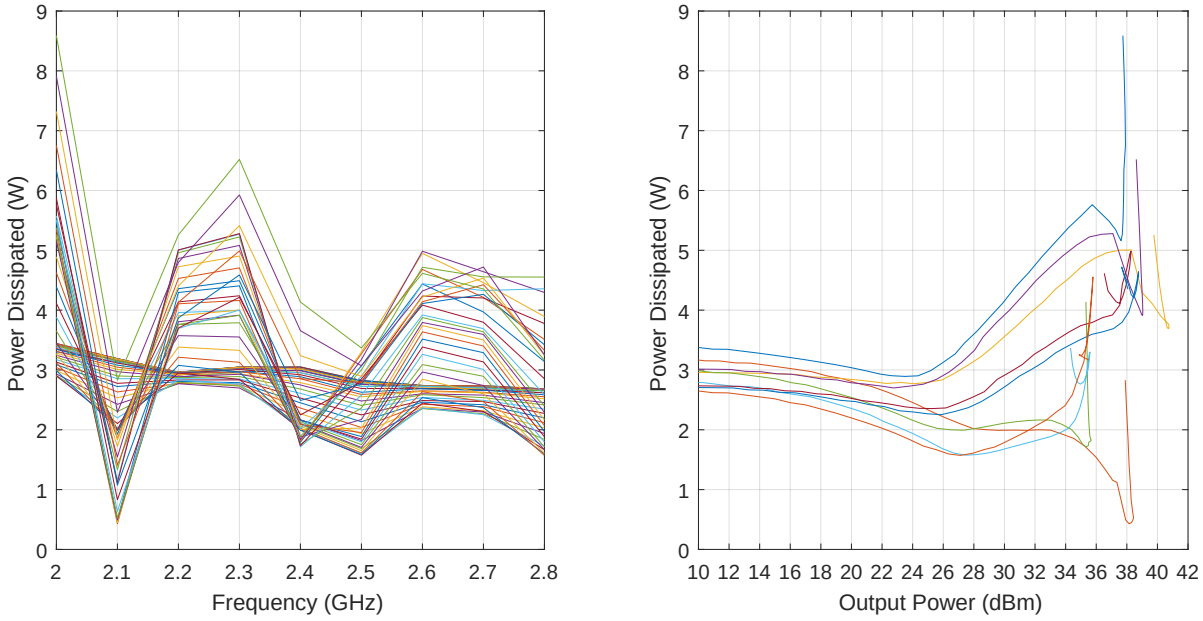

Figure B.12: Measurements of the power dissipated versus input power and frequency for the driver stage.

B.3 Two-stage amplifier

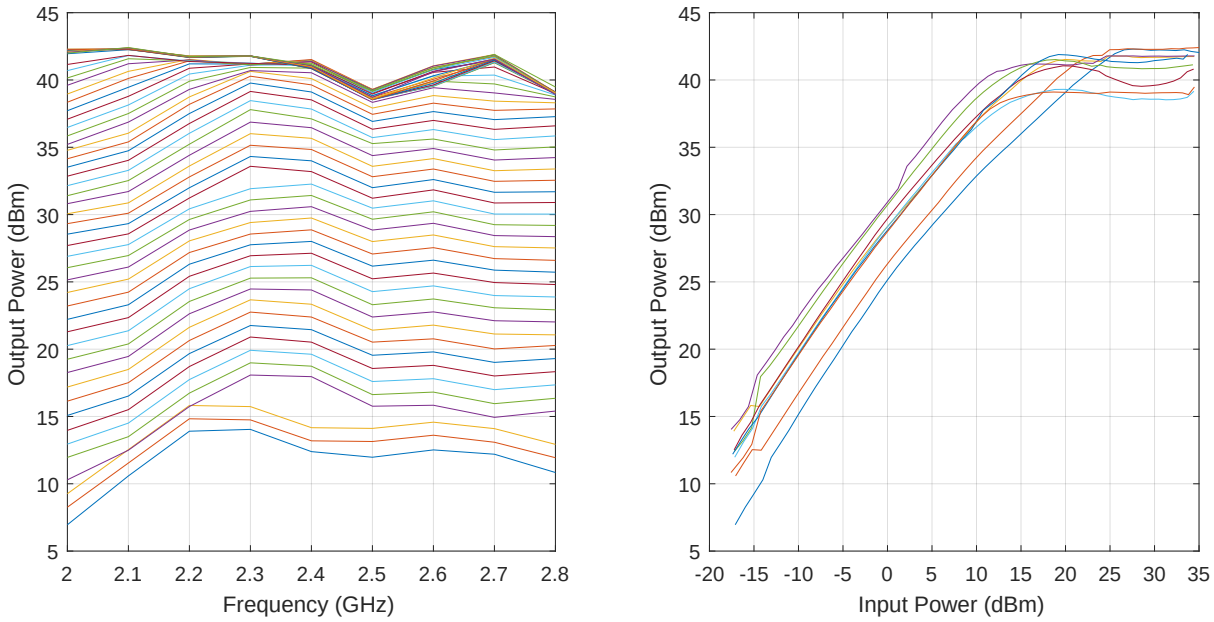

Figure B.13: Measurements of the output power gain versus input power and frequency for the two-stage.

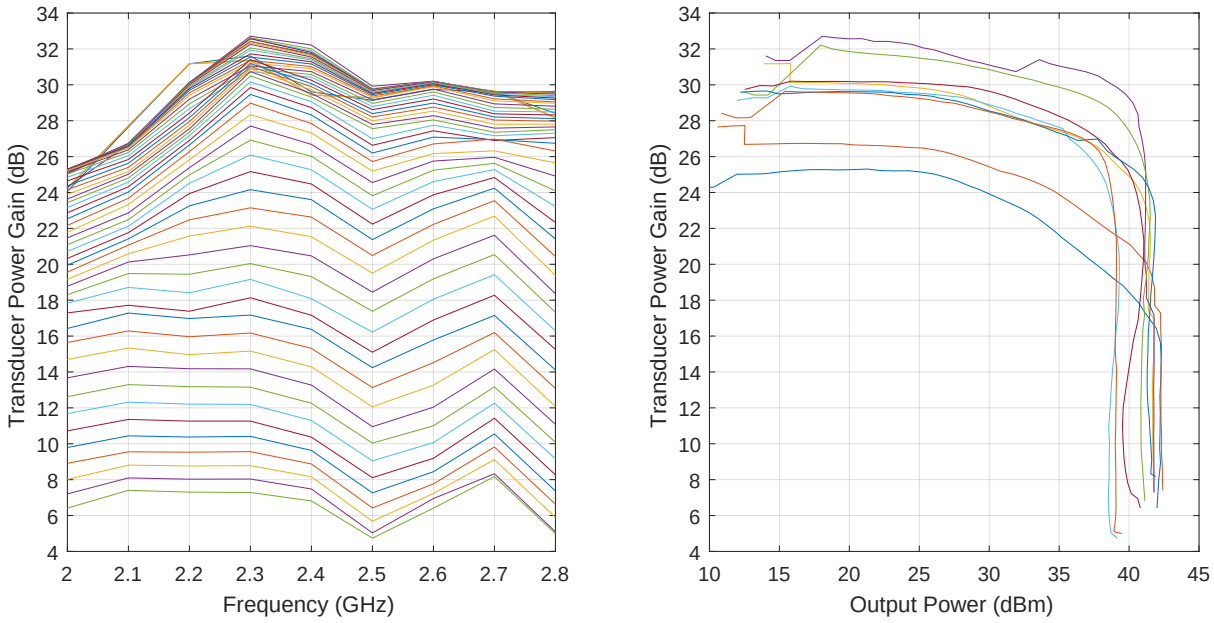

Figure B.14: Measurements of the transducer power gain versus input power and frequency for the two-stage.

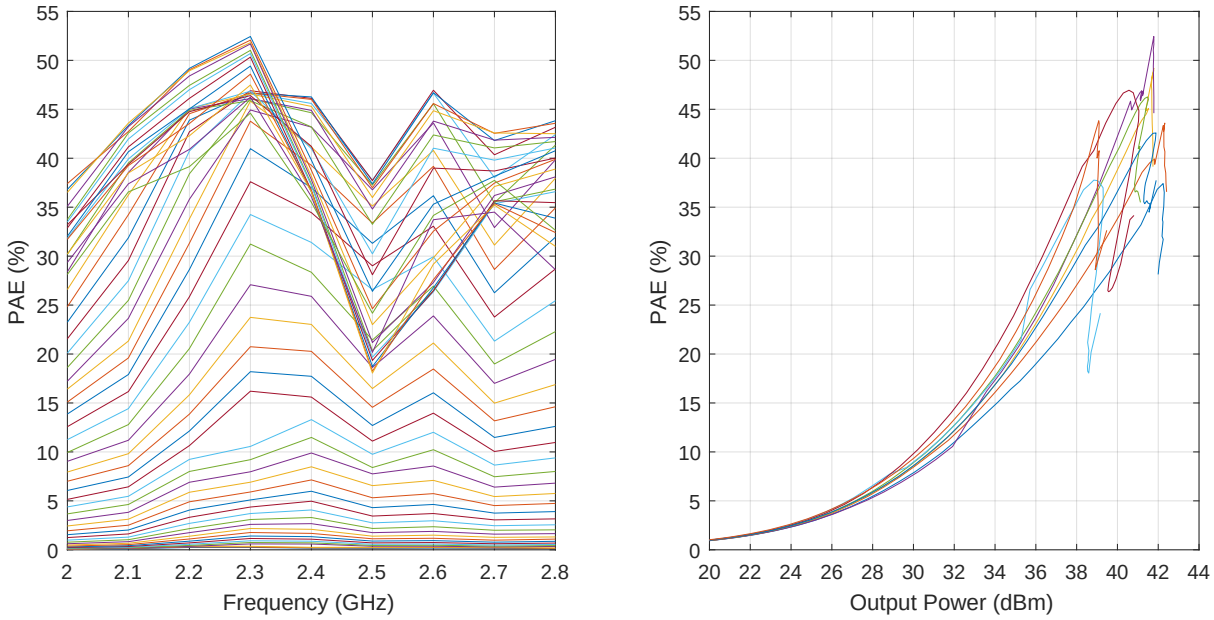

Figure B.15: Measurements of the PAE versus input power and frequency for the two-stage.

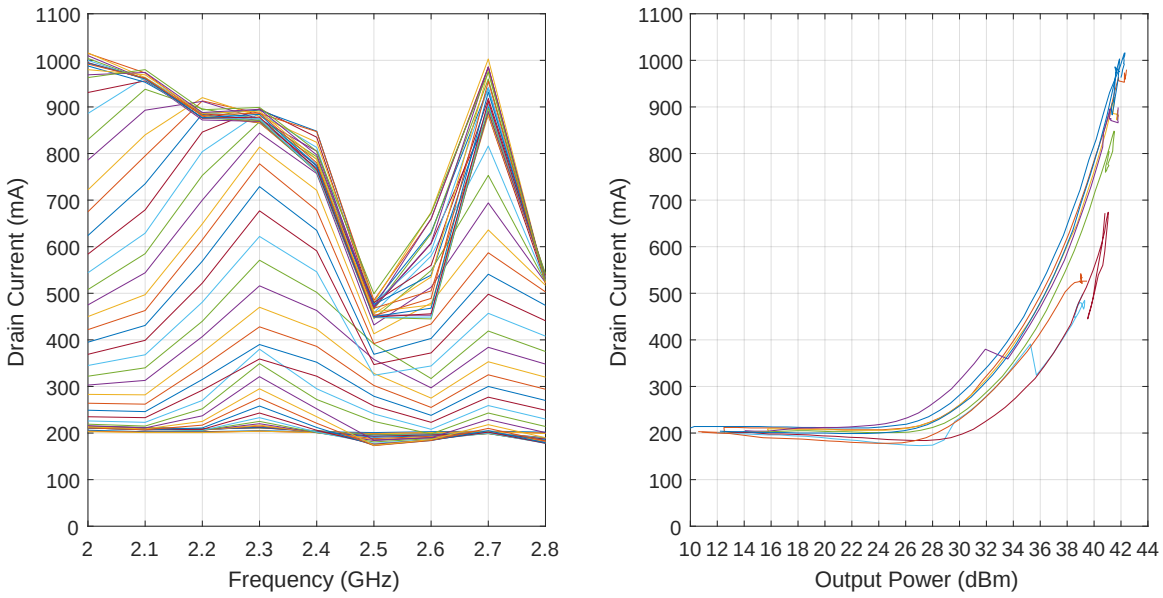

Figure B.16: Measurements of the power stage drain current versus input power and frequency for the two-stage.

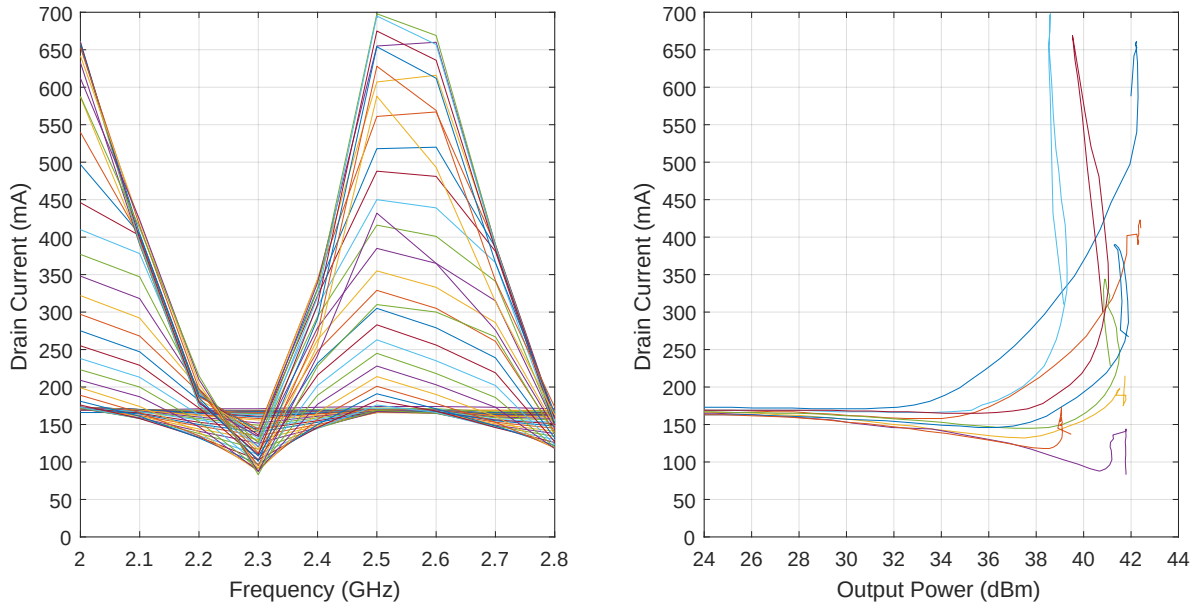

Figure B.17: Measurements of the driver stage drain current versus input power and frequency for the two-stage.

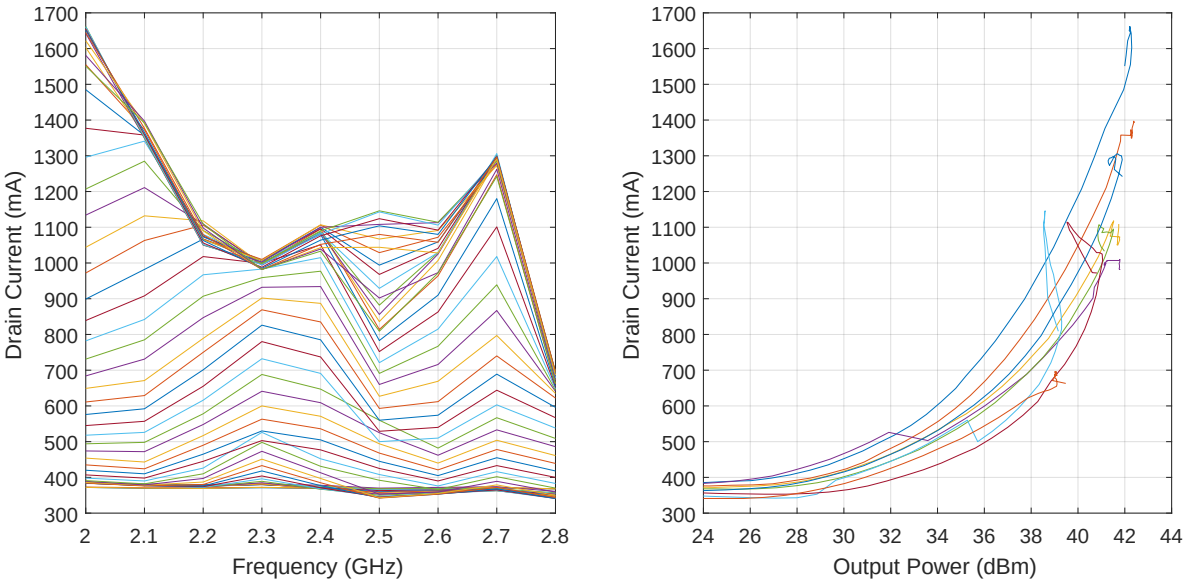

Figure B.18: Measurements of the total drain current versus input power and frequency for the two-stage.

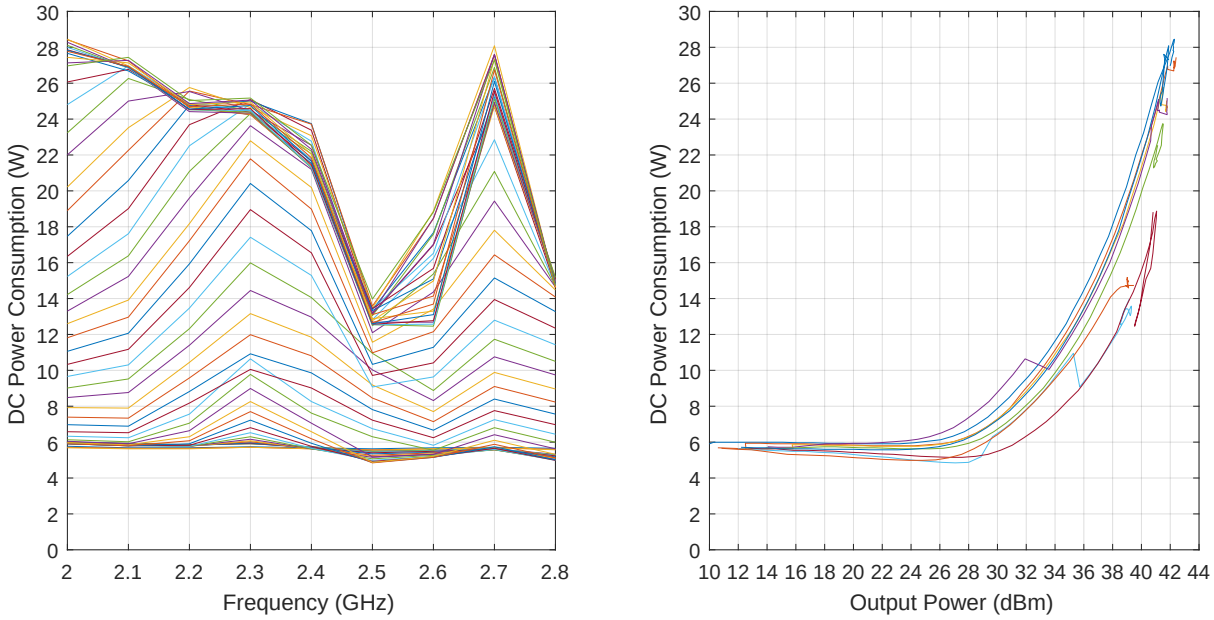

Figure B.19: Measurements of the power stage DC power consumption versus input power and frequency for the two-stage.

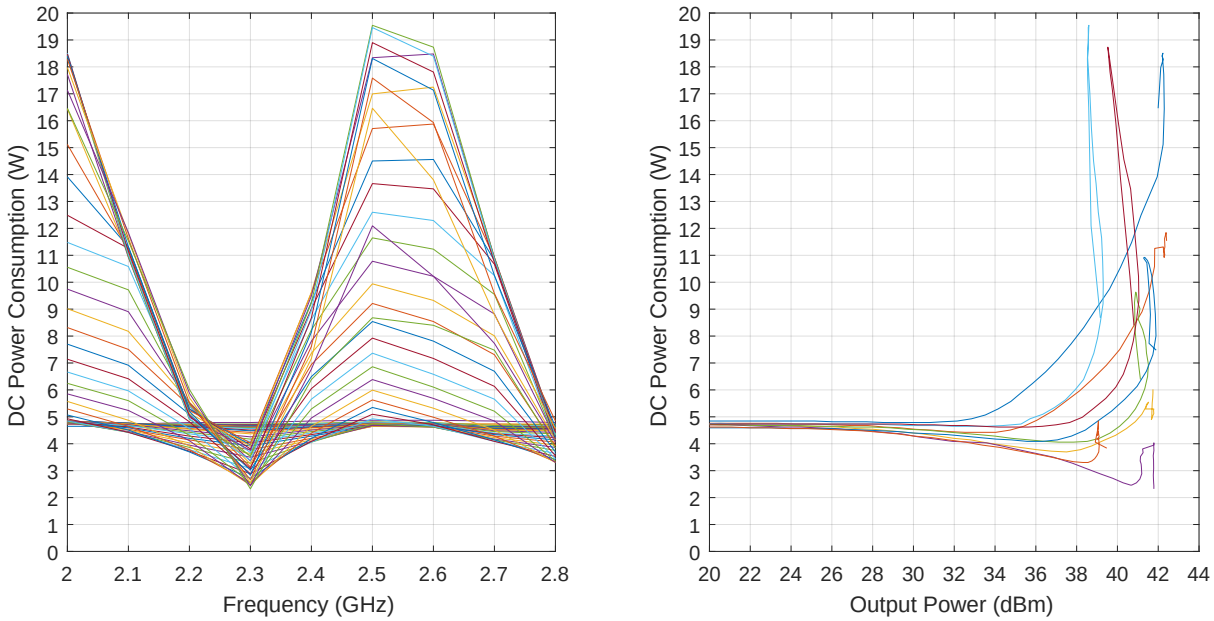

Figure B.20: Measurements of the driver stage DC power consumption versus input power and frequency for the two-stage.

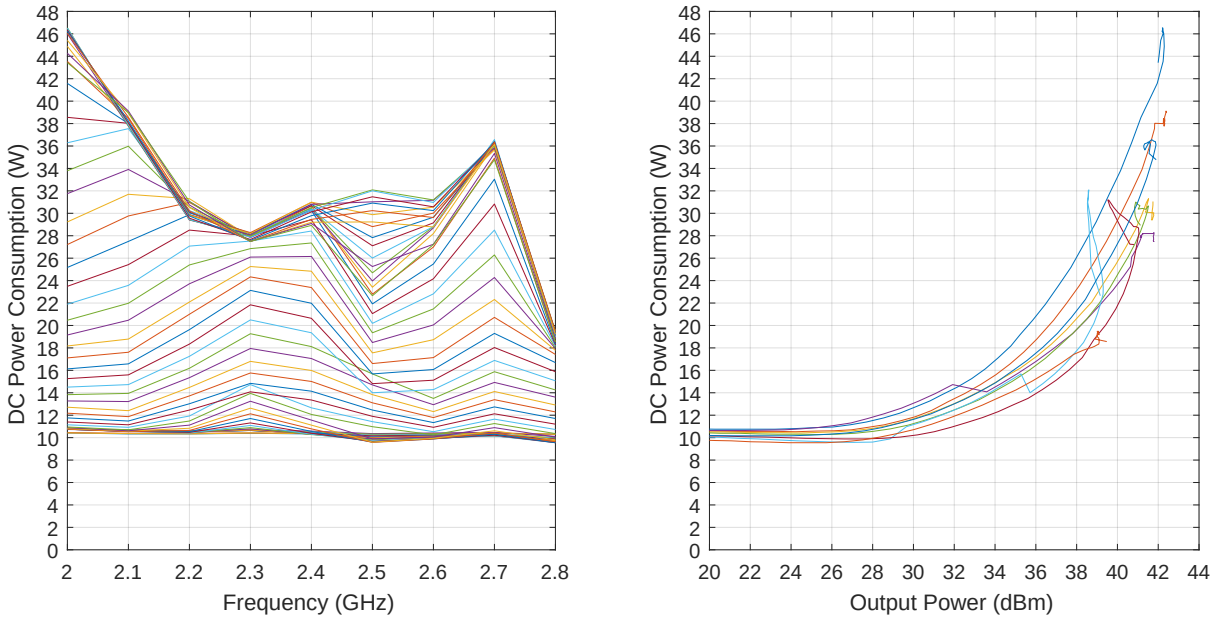

Figure B.21: Measurements of the total DC power consumption versus input power and frequency for the two-stage.

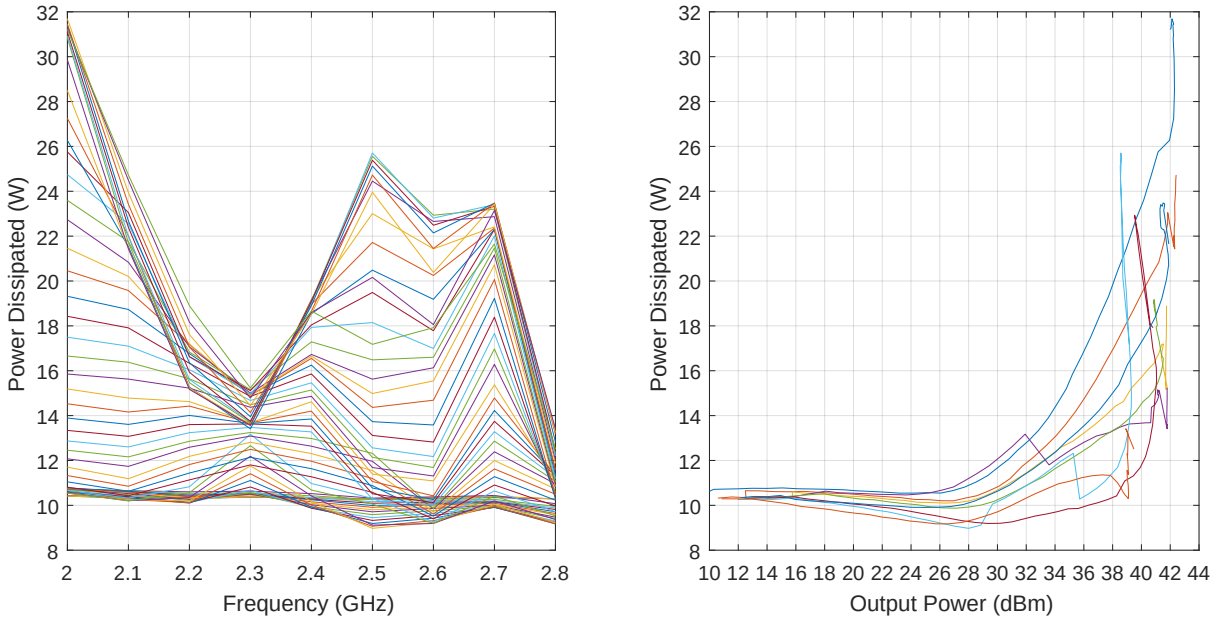

Figure B.22: Measurements of the total power dissipated versus input power and frequency for the two-stage.

Appendix C

Photos of the Amplifiers

C.1 Power Stage Amplifier

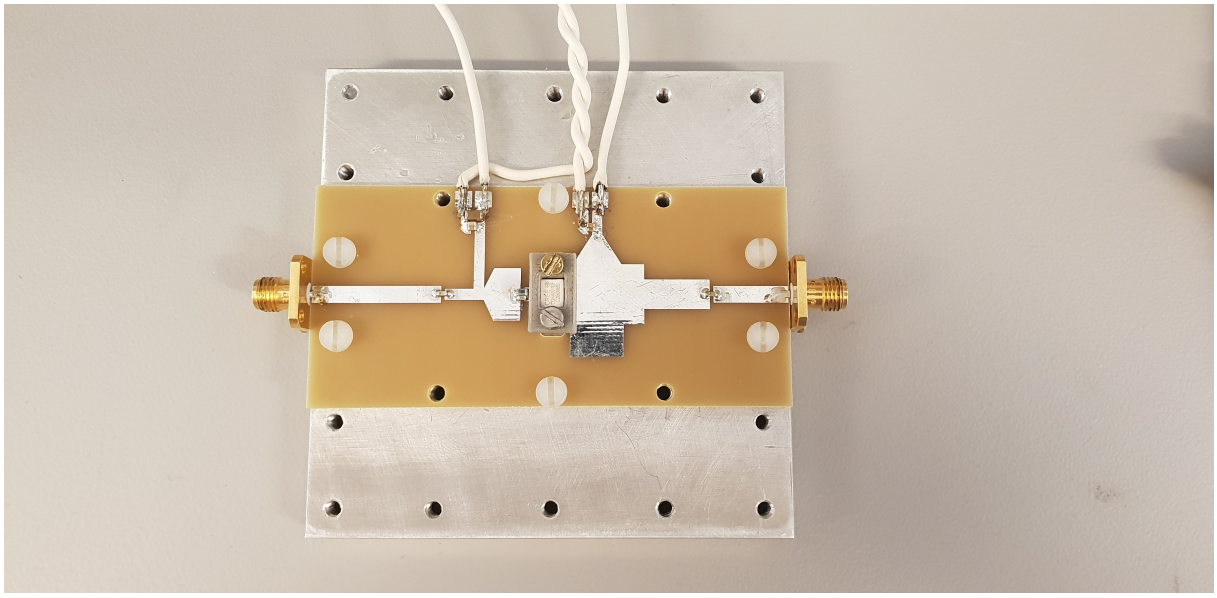

Figure C.1: Photo of the power stage amplifier with the CGH40010F transistor and clamp.

C.2 Driver Stage Amplifer

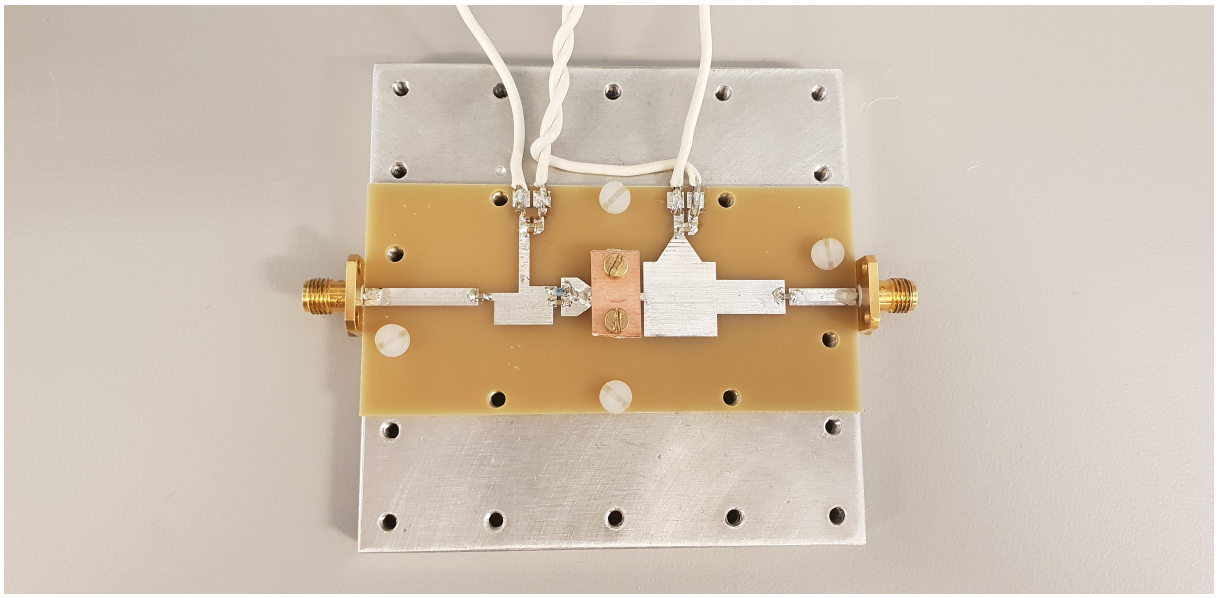

Figure C.2: Photo of the driver stage amplifier with the CGH40006P transistor and clamp.

C.3 Two-stage Amplifier

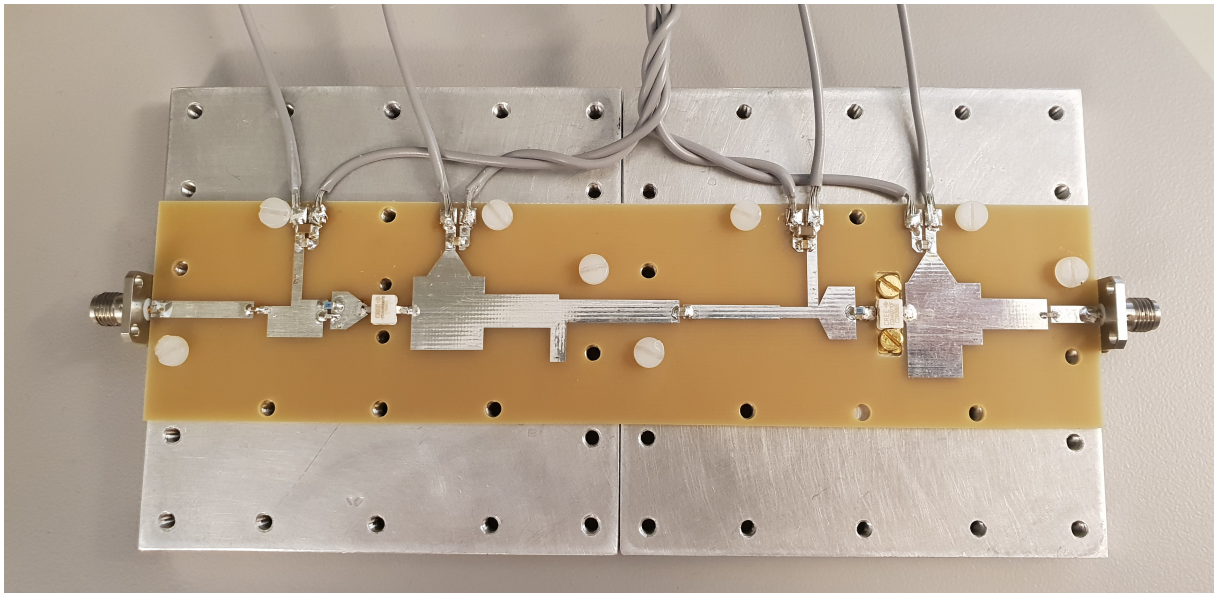

Figure C.3: Photo of the two-stage amplifier with both the driver and amplifier stages.