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Study and development of Solid State based Long Pulse Klystron Modulators for future Linear Accelerators at CERN

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Problem Description

Solid state based converter systems are under development for the next generation of linear accelerators at CERN. This project concentrates on the study and development of a high voltage pulsed power supply for klystron modulator systems. The project is based on the specific requirements of the projected LINAC-4, which requires a long pulse of -100 kV / 20 A. The load can be assumed purly resistive. The pulse time is 800 us with a repetition rate of 2 Hz.

The project should investigate existing state of the art solutions and possible new solution in this specialized field. Based on the research, one or two of the most suitable toplogies should be investigated further by accurate dimensioning and thorough simulations. Also the project should coincide with the already ongoing development of a prototype at CERN.

Assignment given: 15. January 2007
Supervisor: Tore Marvin Undeland, ELKRAFT

Abstract

A new Klystron modulator is to be developed as a part of the new Linear Accelerator (LINAC4) project that is currently running at CERN. The Klystron modulator is required to supply a pulsed output voltage of -100 kV / 20 A with a repetition rate of 2 Hz and a pulse length of 800 μs. In addition to this, the Klystron modulator must also handle arcing in the Klystron, and allow for no more than 10 J of energy to be dissipated in the arc in such a case.

This thesis studies possible solid state based topologies that could be relevant for the Klystron modulator. A single switch topology, based on a 12 kV IGCT switch and a pulse transformer, is studied in detail and developed as a full scale prototype. Preliminary test results indicate that this will provide a satisfactory solution that meets the requirements.

A second topology based on the Parallel Resonant Converter (PRC) was studied in detail through analysis and simulations. This showed to be a promising solution that could be an improvement compared to the single switch topology. The PRC is fully controllable and thus offers a flexible solution that can meet various demands. The topology also showed very good arc handling capabilities, and the PRC can be configured to protect the Klystron by its natural response.

Preface

This report is the master thesis and final part of the Masters course *Energy and Environmental Engineering* at NTNU, the Norwegian University of Technology and Science. This thesis is written for CERN through their technical student program.

This master thesis is a continuation of the project work submitted December 2006. To make this thesis a complete and independent document, some parts of the project report have been included with only minor changes. This applies to the Introduction and some parts of Chapter 4. The State of the Art study in Chapter 3 is a condensed version of the one given in the project report.

This thesis consists of just below 30 000 words which amount to less than 60 effective pages of text. All the work, analysis, and assembly described in this thesis are performed by the writer himself, unless specifically stated otherwise.

Acknowledgements

I wish to thank Prof. Tore Undeland and Dr. Frédérick Bordry for their effort in making the exchange to CERN possible. I also wish to thank Dr. Carlos de Almeida Martins for his continuous supervision during my work, and for always being forthcoming with me and answering all kinds of questions.

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Chapter 1

Introduction

1.1 CERN

CERN, The European Organization for Nuclear Research, is a European physics laboratory located on the border between France and Switzerland just outside Geneva. The laboratory is houses a large complex of underground particle accelerators, the largest is 27 km in circumference, which makes the CERN complex the world's largest physics machine. [3]

In general the experiments start by creating a beam in one of the linear accelerators. The beam then proceeds through several energy increasing steps in the different accelerator rings. Finally the beam is collided in one of the detectors; ATLAS, Alice, LHCb, or the CMS. The latest developments at CERN are the LHC machine and detectors which have scheduled start of operation during the 2008. [22]

1.2 Linear Accelerator

The first step in the CERN complex is the Linear Accelerator, often referred to as LINAC. The LINAC is located directly after the particle source and is responsible for the initial acceleration. Today there are two operational LINACs at CERN, the LINAC2 proton accelerator and the LINAC3 heavy ion accelerator. LINAC2 is about 40 years old and is scheduled to be replaced by the new LINAC4. [14] [1] Pulsed power technology, under study by this work, has a relevant application on this kind of accelerators as it will be explained later.

1.2.1 Basic Principle

The basic principle of a Linear Accelerator consists in applying a voltage between two metal objects, usually plates as shown in Figure 1.2. This generates an electric field, which in turn accelerates charged particles to-

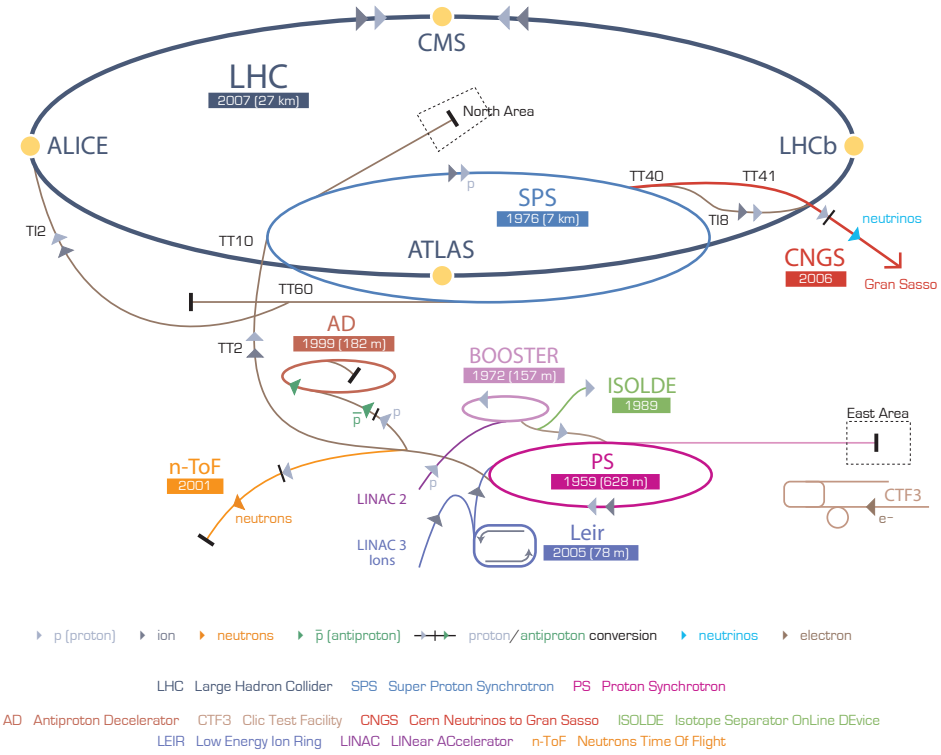


Figure 1.1: The CERN Complex

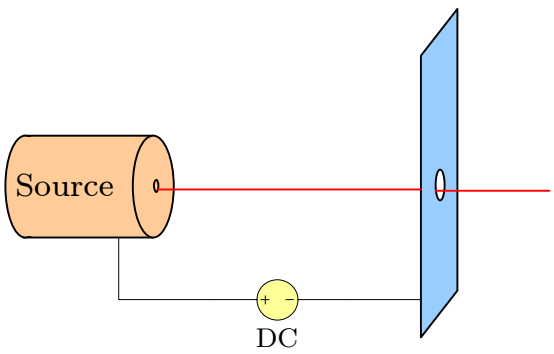


Figure 1.2: Single stage LINAC

wards the collector plate. A hole in the center of the collector plate allows the accelerated particles to escape without colliding with the plate. The accumulated kinetic energy gain in the particle is given by Equation 1.1:

$$W_e = qU \tag{1.1}$$

As stated by Equation 1.1, the accelerated energy of a given charged particle is dependent upon the applied voltage. There are practical limits to the voltage that can be obtained and voltage levels over 1 MV must be considered impractical due to HV effects and technological limitations. This limits the practical maximum energy level for this configuration to the order of 1 MeV.

To achieve higher energy levels, a more suitable solution is a configuration that consists of several plates in succession, as shown in Figure 1.3. By alternating the voltage between the plates in phase with the particle movement, the particle will always see an unidirectional field. Thus the particle will accelerate and accumulate energy while traveling through the stack of plates.

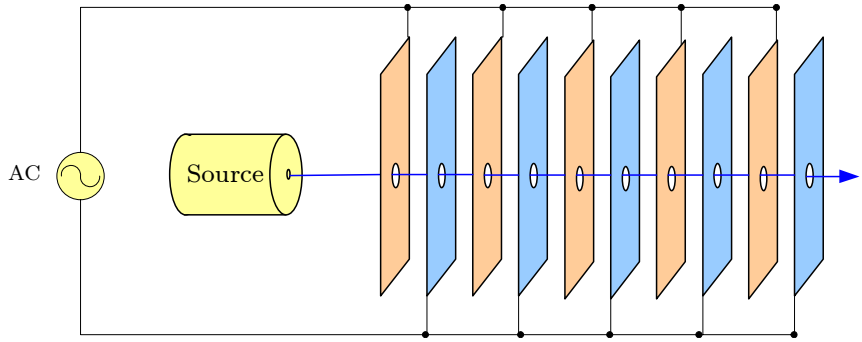


Figure 1.3: Multi-stage LINAC

Due to the inhomogeneous field, the accumulated energy must be calculated with the integral stated in Equation 1.2.

$$W_e = \int_{s_1}^{s_2} q\vec{E}\, d\vec{s} \tag{1.2}$$

In the ideal case the applied voltage is a perfect square wave accurately in phase with the particle. In this case the accumulated energy between two plates can be calculated with the same equation as for the single plate configuration above. Hence the total accumulated energy gain is given by Equation 1.3.

$$W_e = qU\,(n-1) \tag{1.3}$$

Here n is the total number of plates. This equation clearly shows the advantage of the stacked configuration. The challenge with the multi-stage

LINAC is that to keep the size down, the applied frequency has to be in the gigahertz range.

1.2.2 Managing Gigahertz Frequencies

In practical terms the ideal square wave voltage pulses will be difficult to generate, given the higher harmonics that are required to form the square shaped waveform. The LINACs therefore rely on sinusoidal waveforms. However, the task of applying a sinusoidal voltage of several gigahertz at the plates is very challenging. At present there are no existing solid state switches or other conventional voltage source topologies that can handle these frequencies and power levels. If such a configuration were possible, the connection to the plates and the plates it self would lead to heavy RF radiation and power loss, as stated by Maxwell's equations. Hence conventional AC converters at these frequencies are generally not feasible.

One solution to achieve high frequency voltages is to exploit the linkage between RF waves and electrical fields to the opposite of the issue above. By injecting RF energy with the right frequency and phase into a suitable RF cavity, it is possible to achieve the desired voltage. The RF waves must be generated by some kind of RF tube.

Through history solid state technology has successively replaced RF tube technology at successively higher frequencies and power levels. The gigahertz frequency domain is therefore often viewed as the last frontier of the RF tube technology. However, the RF tubes still have to be polarized by an electrical power source. At this level modern power electronics combined with the most recent developments in power semiconductors plays an increasingly important role.

1.2.3 Current LINACs at CERN

The current LINACs at CERN utilize the mentioned RF-to-Voltage relationship. Figure 1.4 shows the first stage of the LINAC3. The ions are injected from the right and accelerated through the rings. The rings are equivalent to the plates in the earlier examples. The big pipes supporting the rings are the waveguides. LINAC3 delivers 4.2 MeV/n when accelerating $^{208}_{53}\mathrm{Pb}^{+}$ [4]. In general terms this corresponds to a total 873.6 MeV per unit charge. (4.2 MeV multiplied with the 208 nucleus of a Pb53 atom) When compared to the single plate configuration it can be seen that this configuration improves the energy factor by three orders of magnitude.

1.3 Klystron

The Klystron can be viewed as an electrical-to-RF power converter and is the best suited RF tube for LINACs. The Klystron emits accurate, co-

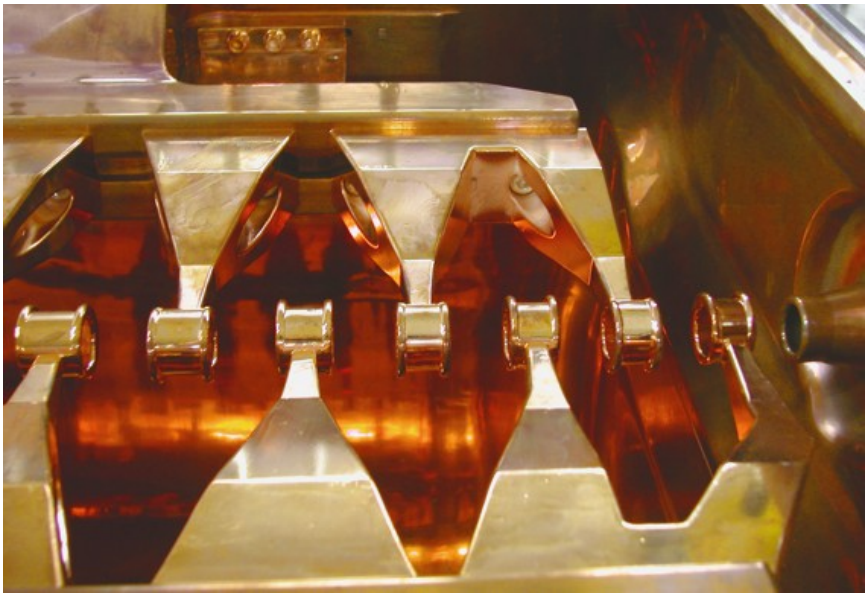


Figure 1.4: LINAC3 - first stage

herent, microwave energy up to several gigahertz, and also has high power capabilities. The one used in the LINACs is a *two-cavity Klystron amplifier*, as shown in Figure 1.5.

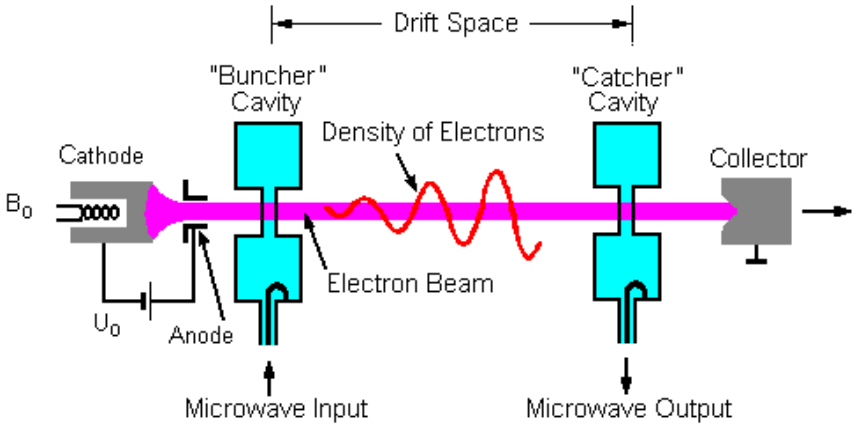


Figure 1.5: Two-cavity Klystron

In the two-chamber Klystron, an electron beam from the cathode of an electron gun is injected into a resonant cavity. The free electrons are generated by a source consisting of a filament heated to several thousand degrees. The Klystron is polarized by an electrical voltage source applied between the collector and the cathode terminals. The collector is connected to body

ground. The electron beam is constrained by an axial magnetic field and is accelerated through a connecting passage, called a *drift tube*, to a second resonant chamber. While passing through the first chamber the electron beam is velocity modulated, often referred to as *periodically bunched*, by the weaker RF signal. The negative electrons are attracted by the positive collector placed after the second resonant chamber. As the bunched electrons enter the second chamber they induce standing electromagnetic waves at the same frequency as the input signal. The signal induced in the second chamber is much stronger than that in the first. The energy required to amplify the weak RF input signal is drawn from the polarization current.

In a simplified way the Klystron can be compared to a BJT transistor as shown in Figure 1.6. A high voltage bias is required between the cathode and the collector to accelerate the electrons through the drift tube. This bias voltage can be compared to the BJT collector-emitter voltage. On the RF input a RF control signal is injected. The RF output will emit an electromagnetic high power wave similar to the input, but heavily amplified. Hence the RF input can be compared to the base current of a BJT. The emitter current can be compared to the RF output.

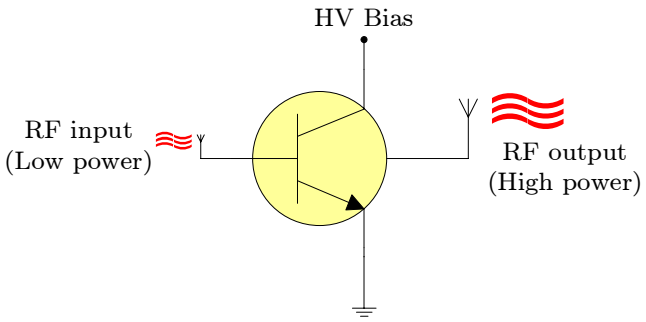


Figure 1.6: Klystron equivalent

The electron beam flowing trough the Klystron represents a constant flowing current from the HV bias to ground. This current represents a power loss in the Klystron, and to mitigate the loss, the bias voltage should only be applied when Klystron operation is required. This is typically when a particle beam is accelerated in the LINAC. Since Klystrons often are required to excite pulsed RF power, this requires a pulsed bias voltage. A pulsed bias voltage source is often referred to as a *Klystron modulator*. Since the Klystron is ground connected on the collector, the bias voltage always has to be negative.

Chapter 2

Objective

The objective of this thesis is to study and participate in the development of solid state based Klystron modulators for the LINAC4 project.

2.1 Klystron Modulator Requirements

The LINAC4 will inject hadron bunches into the PS booster (shown in Figure 1.1) with a repetition rate of 2 Hz. The accelerating time for each bunch is 600 μs. [14] This leads to the requirements for the Klystron modulator shown in Table 2.1:

Parameter	Value	
Output voltage	-100	kV
Output current	20	A
Pulse duration	800	μs
Pulse repetition rate	2	Hz
Maximum rise/fall-time	100	μs
Maximum arc energy	10	J
Voltage droop tolerance ($<$ 10 kHz)	1	%
Voltage ripple tolerance ($>$ 10 kHz)	0.1	%
Maximum reverse voltage	3	%
Supply voltage (3 ph)	400	V
Lifetime	100 000	h

Table 2.1: Klystron modulator requirements

The LINAC4 project is to be built in several stages. The first stage is projected to be finished during the end of 2007, and requires only one Klystron modulator. The second stage is scheduled to take place during 2008-2012 and requires 16 modulators. The third and final stage during 2012-2016 will require 45 modulators.

The Klystron modulator project should take advantage of the long time frame of the LINAC4 project and do continuous development in parallel with the project. Since there is a short deadline for the first modulator, the development therefore becomes a dual part project. The first part is to deliver the first modulator in time for stage 1. The second part deals with the projected future modulators. Since there are several years until these have to be delivered, there is time for resource and development into more advanced systems.

Currently, all the required modulators are rated with the specifications listed in Table 2.1. However, this has been subject to changes, and a future universal modulator that is to be used in all Klystron applications should be flexible on amplitude, pulse length and pulse repetition rate. A projected extension of LINAC4, the *Super Conducting Proton LINAC* (SPL), will require pulse frequencies in the area of 50 Hz.

The objective of this thesis involves both parts of the modulator project. Firstly the work should focus on the modulator system required for early delivery. A project of developing a prototype is already started and this thesis coincides with this work. Secondly the work should focus on finding the optimal solution for future Klystron modulators.

To address this, the thesis is organized as follows:

- **State of the Art - Chapter 3**
  The existing solutions using the best available technologies are explored in the state of the art analysis. This builds a foundation for the further work, and the selection of the optimal system.

- **Prototype work - Chapter 4-6**
  This part focuses on the prototype solution that is to be delivered during 2007. The work incorporates analysis, development, assembly and testing.

- **Future solutions - Chapter 7**
  Based on the state of the art analysis, a system that may be more suitable in future systems is selected and studied in detail in this part.

Chapter 3

State of the Art

This chapter presents the latest available technology in pulsed power that can be relevant for a Klystron modulator. Since the entry of the thyristors during the sixties, solid state based technology has taken over for the RF tube technology in an increasing number of applications. Solid state systems have shown to be advantageous over the tubes in most qualities and are usually superior on the qualities of size, cost, efficiency, reliability and maintenance. Thus solid state based converters are viewed as generally advantageous over the older switching technologies [17]. A study of more than 50 technical papers on solid state based systems resulted in a selection of four interesting topologies that are subjects for further study. These are the *single switch converter*, the *Marx generator*, the *direct modulator* and the *resonant converter*. In the following, these topologies are examined and compared with the Klystron modulator requirements.

3.1 Single Switch Topology

The simplest solution for a pulsed converter is a circuit where the voltage source is directly connected to the load through a switch as shown in Figure 3.1.

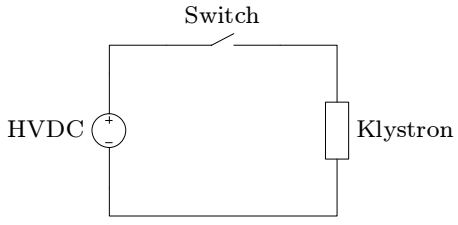


Figure 3.1: General single switch configuration

The challenge with running such a circuit at 100 kV is to obtain a switch that can handle the voltage level. Today there are still no existing solid state

modules that can single handedly operate anywhere near 100 kV. Currently the maximum available voltage rating of IGBT modules are about 6 kV [21] [12]. Switches that shall handle higher voltages therefore have to be based on arrays of several serial connected switches. Based on this technique, voltage levels up to 200 kV [15] have been reached, but the technology is complicated and expensive. Because of the complexity of the system, and the price level, applications based on this technology are rare.

One way to avoid the high switching voltage is to insert a transformer between the switch and the load. For instance a ten times reduction of the voltage will completely change the situation and allow for a wider range of available switches. However, to keep a satisfactory square shape of the pulse, a specially designed pulse transformer is required.

The common power source for such applications is a capacitor bank connected to a standardized capacitor charger. However, a challenge with the capacitor bank is the voltage droop that will occur as the pulse energy is quickly extracted. This problem can easily be solved by adding capacitors until the droop is within the accepted range. Alternatively some means of compensation system can be used. Since the accepted droop for the Klystron modulator is only 1 %, and some voltage droop also must be expected in the pulse transformer, it is expected that a compensation system would be advantageous.

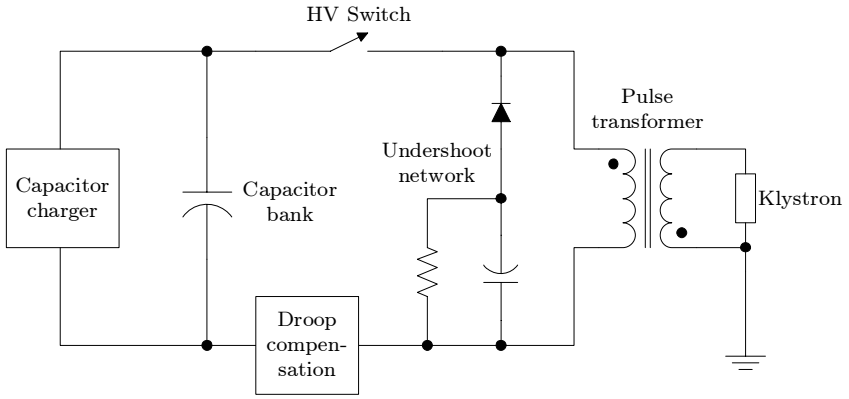


Figure 3.2: Suitable Klystron modulator configuration

Figure 3.2 shows the single switch based configuration that is most suitable as a Klystron modulator. The converter consists of a low number of components and is simple to control. The circuit is totally controlled by the switch, and a pulse is generated simply by turning the switch on and off. This makes the single switch topology the solution that can be brought most quickly into operation. However, the few, but exclusive components used in the circuit are both expensive and have to be tailor made for the application. The availability of such components is limited.

3.1.1 Existing Systems

Fermi National Accelerator Laboratory (Fermilab), in Batavia near Chicago, and DESY, the largest German particle physics laboratory, have cooperated in developing a solid state based Klystron modulator. The modulator is based on an 8x serial stack of 3.3 kV IGBTs to achieve a total switch voltage of 12 kV. [11]. To compensate for capacitor voltage droop the modulator is equipped with a *bouncer*. The bouncer is discussed in detail in Chapter 5.

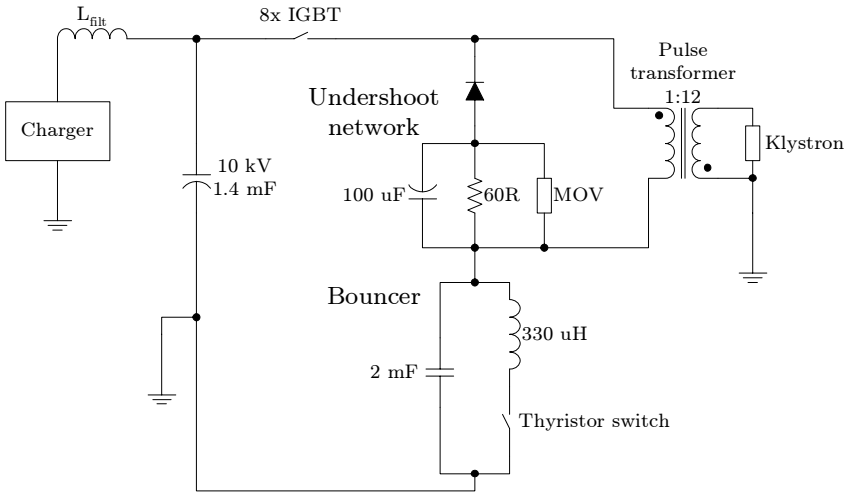


Figure 3.3: Klystron modulator developed by Fermilab and DESY

3.1.2 Summary of the Single Switch Topology

The single switch topology is the quickest approach to obtain a working Klystron modulator due to its simplicity. A project of developing a full scale prototype was therefore undertaken ahead of this thesis work because of the short deadline for the first modulator. Much of the work on this thesis is therefore based on the development of the single switch converter.

However simple, the single switch converter is also a rigid and expensive solution that allows for little flexibility. The pulse transformer has to be specially designed to the pulse length and pulse power, the switch must be tailor made to the voltage and current level, and the eventual correction bouncer must be fine tuned to fit the load perfectly. In addition to this, the high price level suggests that there might be other better solutions that should be developed with time.

3.2 Marx Generator

A Marx generator is a type of electrical circuit first described by Erwin Marx in 1924, whose purpose is to generate a high voltage pulse. It is extensively used for simulating the effects of lightning during high voltage and aviation equipment testing. The concept of a Marx generator is to slowly charge a stack of capacitors in parallel to a given voltage. Upon firing of the pulse, the capacitors are reconnected in series, usually by spark gaps configuration. The Marx generator will then ideally generate an output pulse with a voltage equal to the individual cell voltage times the number of cells. [6]

When using a spark gap configuration it is impossible to stop the discharging process. The discharge will continue until the capacitors are almost completely discharged, hence it is impossible to produce a flat-top pulse with a classic Marx generator.

With the latest advances in solid state technology it is possible to create a more controllable Marx generator based on solid state switches. This will sacrifice some of the steep voltage edge offered by the spark gap since the rising edge will be restricted by the solid state switches. However, for applications with less demanding rise time, the blunter edges help reducing EMC problems.

When using several solid state switches in series, it is crucial to secure the switches so that imbalances between the individual switches cannot lead to undesirable voltages. In Marx generators the voltage will be always be evenly distributed due to the distribution of capacitors. However, if a switch fails to close, it will be exposed to almost the full output voltage. This can easily be avoided by inserting bypass diodes in the cells as showed in Figure 3.5.

An example of a suitable solid state based Marx generator is given in Figure 3.5. For faster charge time and reduced loss, the resistors from the classical configuration are replaced with common mode filters. A common mode filter has low impedance for differential mode current and high impedance for common mode current. This corresponds well to the requirements of the Marx generator since the charge current will appear as a differential mode current, while the leak current during discharge only will flow trough one leg of the common mode filter, and thus appear as a common mode current.

This Marx configuration is not very reliable since a failing capacitor or switch may bring down the entire converter. This can be avoided by introducing a second switch in the charging loop as shown in Figure 3.6. The converter can then be equipped with several spare modules which can be switched in upon failure. Also the second switch can be utilized to improve the charging process so that a balanced capacitor voltage is quickly obtained.

Ideally there are no limits to the number of serial connected modules, but in reality stray capacitances between the components, the charging current,

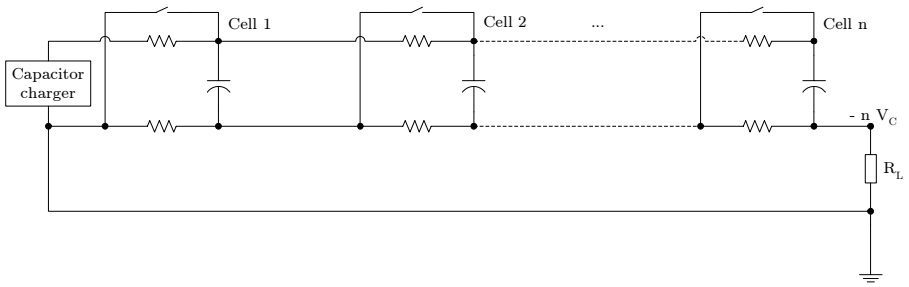


Figure 3.4: General Marx generator

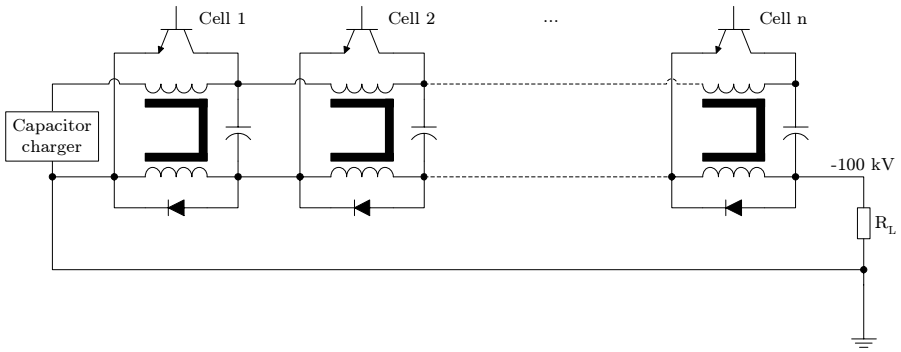


Figure 3.5: Solid state based Marx generator

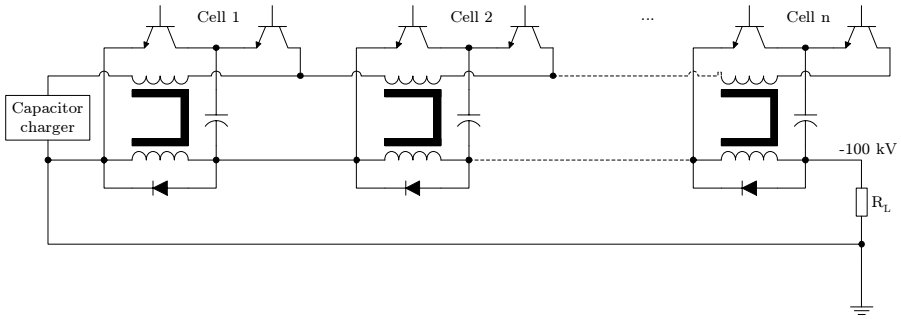


Figure 3.6: Extended Marx generator

and practical considerations limit the total number of cells.

3.2.1 Voltage Droop Compensation

If the Marx generator is operated autonomously, there will be a voltage droop on the output caused by the capacitor discharge. However, the Marx generator offers a possibility to compensate this internally. If the generator is equipped with a surplus of cells, the extra cells can be fired sequentially during the pulse so that they compensate the droop. The ripple caused by firing a new cell will equal the cell voltage. Thus this method of compensation is most useful when the Marx generator consists of a high number of cells so that the ripple is low in respect to the total voltage. The ripple can be reduced by adding an output filter.

To demonstrate this method a simulation of a 55-cell, 100 kV system has been performed. To make the simulation as authentic as possible, 100 pF stray capacitance to ground has been added on all cells. The stray capacitances will be given by the geometrical configuration of the converter and are hard to estimate on a general basis. 100 pF is probably a bit overstated and serves as a safe estimate. Also an inductor is added to as output filter. The complete simulation circuit is shown in Figure 3.7.

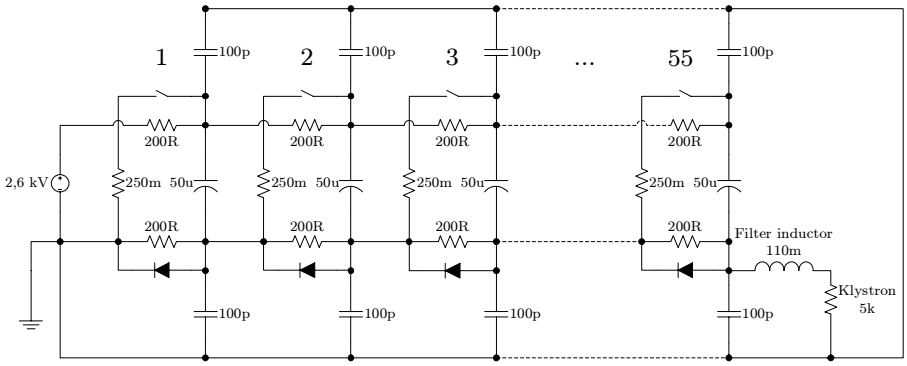
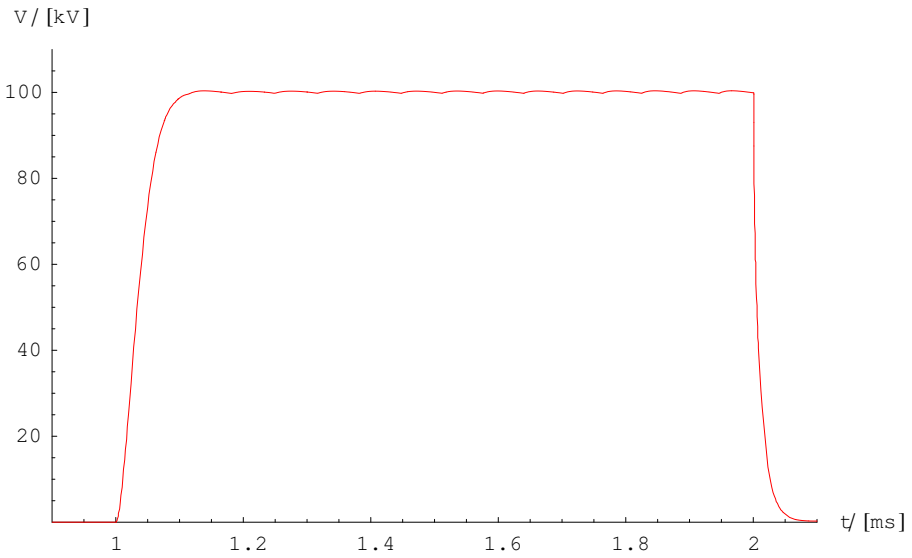


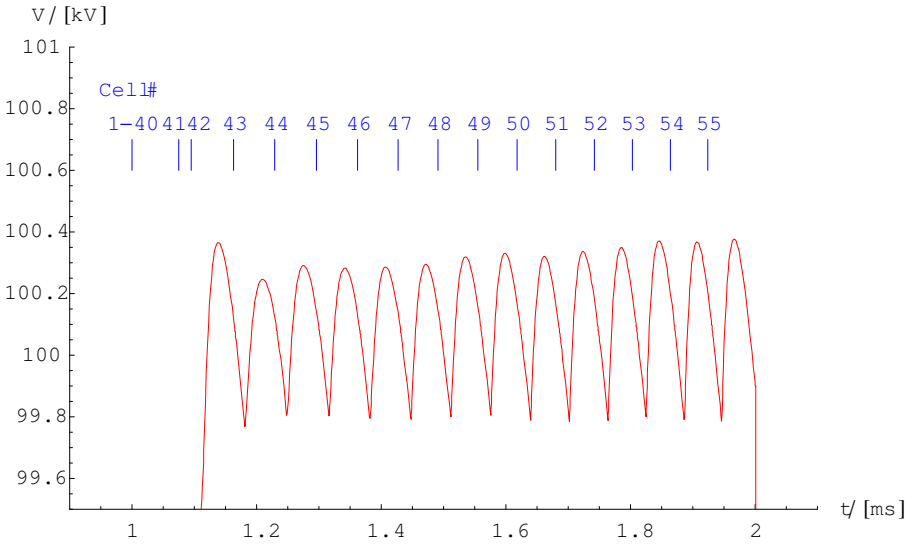
Figure 3.7: Simulated Marx generator

On pulse startup, 40 cells are fired to reach 100 kV. The last 15 cells are distributed through the pulse to compensate the droop. Figure 3.8(a) shows the output pulse. The slow 57 μs rise time is mostly caused by the output filter, and is well within the 100 μs requirement. Figure 3.8(b) shows a zoom on the flat-top. The firing times of the cells are indicated in blue.

The allowed output ripple is 0.1 % which corresponds to 100 V. This requirement is heavily violated, as the ripple is close to 600 V. The ripple can be reduced by either increasing the filter or by increasing the number off cells. Since the number of cells is already high, and the filter is already limiting the performance, this compensation method is probably not suitable for systems with tight ripple requirements.



(a) Output



(b) Output - zoomed on flat-top

Figure 3.8: Marx generator simulation results

3.2.2 Existing Systems

At *Stanford Linear Accelerator Center* (SLAC), a 500 kV Solid State Marx Generator is under development. [16] The converter is based on the double switch topology described earlier. The second switch is utilized actively to control the charging cycle of the capacitors, to avoid excessive inrush currents, and to achieve equal voltage in all the cells. The converter is divided into sub modules, each consisting of 12 cells with an output voltage of 18 kV. This results in a DC-link voltage of only 1.5 kV on each IGBT module, and avoids the use of the expensive high voltage modules. One sub module is shown in Figure 3.9. The low charging voltage also simplifies the general design. The problems with capacitive coupling on the driving signals are solved by keeping the driving boards at or near the cell potential and communicating the driving signals by standard wireless network (WLAN).

At SLAC the required output pulse is very short and requires a short rise time. This makes the stray capacitance of the system important and restricts the physical geometry. Generally the generator should be kept small to reduce the capacitive area. Currently a long pulse version is also under development at SLAC.

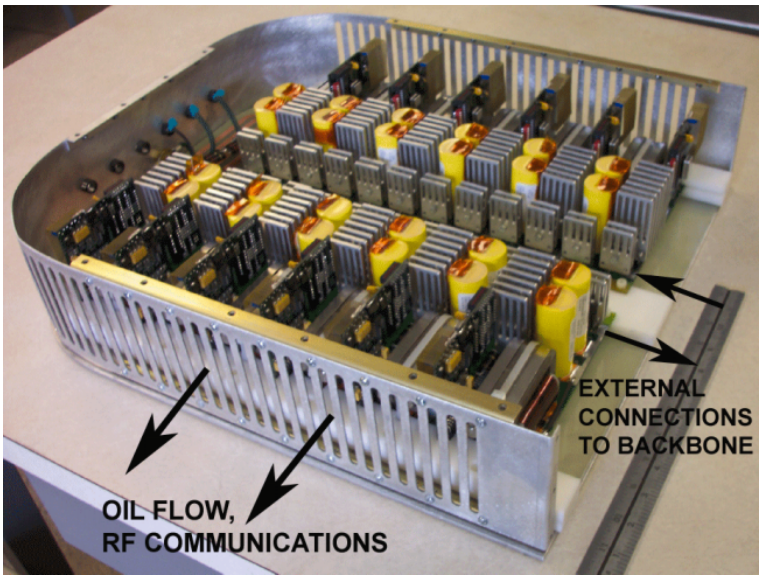


Figure 3.9: One sub-module from the SLAC modulator

3.2.3 Summary Marx Generator

Two properties with the Marx generator restrict the flexibility of the system. Firstly the high number off cells that are required to achieve adequate voltage amplification makes the system vulnerable since it has to consist of

a long serial connected chain of components with a non-zero failure probability factor. Redundancy can be added to the system so that it can be reliable, but still, breakdown of modules must be expected. Failing modules adds to maintenance and is not desirable.

Secondly the distribution of modules and IGBT-drivers over the whole potential specter is a source for trouble. As the generator is fired, all modules move from the charge potential around 2 kV to the different potential steps from 2-100 kV. Since there will be some stray capacitance in the control circuit there will be interference into the control system as the pulse is fired. The driver and control circuitry must be carefully designed so that this does not affect operation.

Also the possibility for compensation is less favorable due to the strict ripple requirements for the Klystron modulator. Thus, the only advantage of the Marx generator is the avoidance of transformers. Given the high level of research and development that will be required to construct such a system, the Marx generator is probably not a good solution for a Klystron modulator.

3.3 Direct Modulator

The direct modulator topology is based on solid state switches connecting the load to a voltage source through a transformer. The switches are alternated quickly after a given pattern, usually PWM, to achieve the desired output waveform. The galvanic insulation offered by the transformer allows for serial connection of several modules to increase the output voltage.

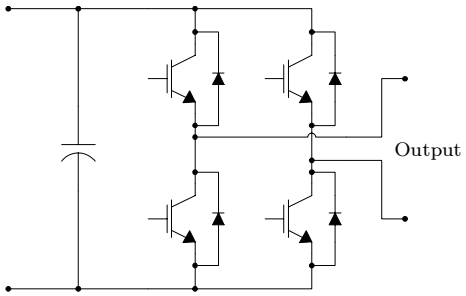


Figure 3.10: 4 quadrant IGBT converter

The converter in Figure 3.10 allows full 4 quadrant operation and is the most versatile configuration. If the application does not require operation in all quadrants, the converter can be simplified by removing some switches and diodes. The Klystron may only require one quadrant operation depending on the transformer configuration selected. In this case a freewheeling diode should also be included to deal with inductive effects in the circuit.

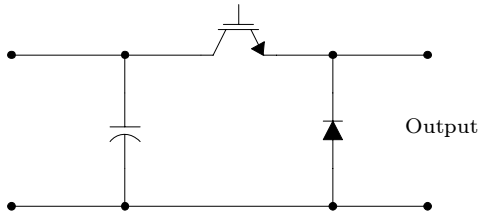


Figure 3.11: 1 quadrant IGBT converter

Direct converters are often operated by *Pulse Width Modulation* (PWM), where the switching frequency is kept constant. The converter is then controlled by altering the *duty cycle*, which is the relationship between on time and off time. Another common control method is to compare the output directly with the reference signal and control on the polarity from this. When the output is below the reference, the switch is on and vice versa. To avoid runaway switching when the output is close to the reference, a suitable hysteresis band has to be added to the system. Thus this method is often referred to as *hysteresis control*.

PWM control requires a more complicated algorithm to generate the control signals. A common way is to compare the reference signal to a triangle waveform alternating at the switching frequency. When the reference signal is higher than the triangle waveform, the switch is on, and vice versa. Figure 3.12 shows 1-quadrant converter running PWM at 20 kHz. 3.12(a) shows the reference signal and the triangle waveform. 3.12(b) shows the corresponding output.

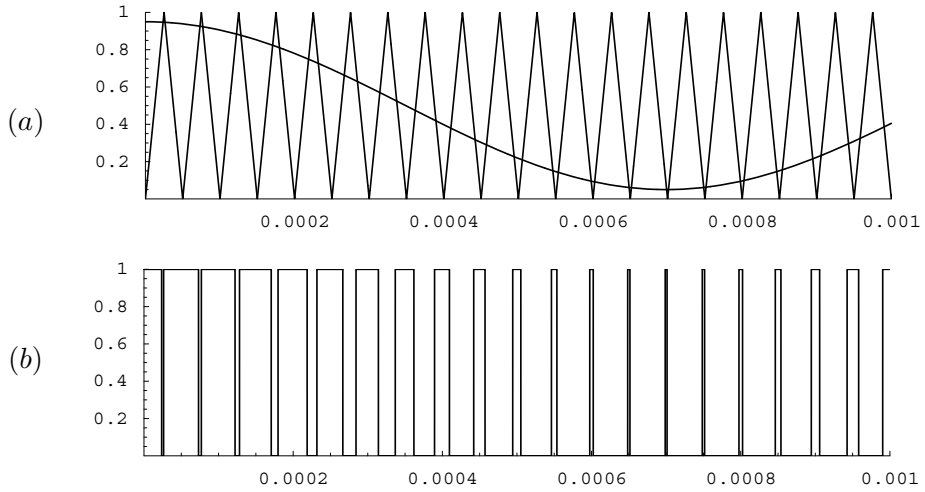


Figure 3.12: PWM control

3.3.1 Switching Loss

To keep output ripple low, and to achieve good controllability of the pulse, the switching frequency should be kept as high as possible. To keep the number of serial connected cells down, the switches also have to operate close to their maximum power rating. In this mode of operation the switching loss will be significant. For instance 1700V / 480A IGBT modules manufactured by Semikron [2] has given a full cycle switching loss of 280 mJ when operated at their nominal condition of 1200V / 300A. With a switching frequency of 20 kHz, which only allows for 16 cycles during the output pulse, the switching loss will be 5.6 kW during the pulse. Since the pulse duty cycle is very low, the average switching loss will be close to 10W and easily manageable. But the thermal shock that will occur during each pulse may be problematic for the switch in terms of lifetime. Also the module given here is among the fastest available. Modules with higher voltage ratings will have higher switching times and thus aggravate the problem. The switching loss is therefore a subject that should be carefully studied when building such a system. To achieve a reliable system, substantial oversizing of the transistors will probably be required.

3.3.2 Transforming

To reach high voltage, both transforming and serial connection of several modules will be required. Since the converter will be controlled by feedback loops, the quality requirements on the transformer output are low. It is not important if the pulses on the output exactly match the pulses on the input since the output will be filtered down. But the transformer is required to have low core losses, both magnetically caused by hysteresis, and electrically caused by eddy currents. Thus the core configuration is significant with such a topology. All the examples given here are meant to be used in serial connections of several modules through inductive adding.

The transformer can be operated either with DC condition or with zero-DC condition. If the configuration is based on the one quadrant topology, the output will have a significant DC component. In this case the transformer core has to be sized to hold the full pulse like the pulse transformer discussed in Section 3.1. However, if the converter is based on the 4-quadrant H-bridge topology, the input can operated with zero-DC conditions. The required pulse time for the transformer is then reduced from 800 μs to 50 μs given a switching frequency of 20 kHz. This allows for a 16-fold reduction of the transformer core area and allows for substantial decreases in cost and size on the transformer. Since the transformer output will be alternating with zero DC conditions, an output rectifier bridge must be included as shown in Figure 3.14

A third possibility is to put the transformer on the input. This is the

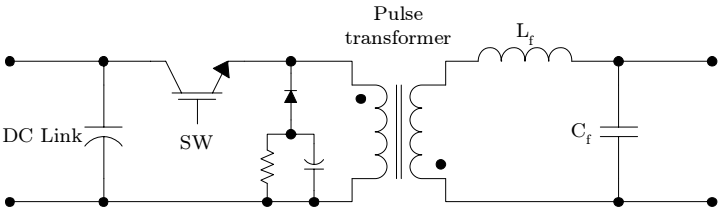


Figure 3.13: Basic DC-transformer configuration

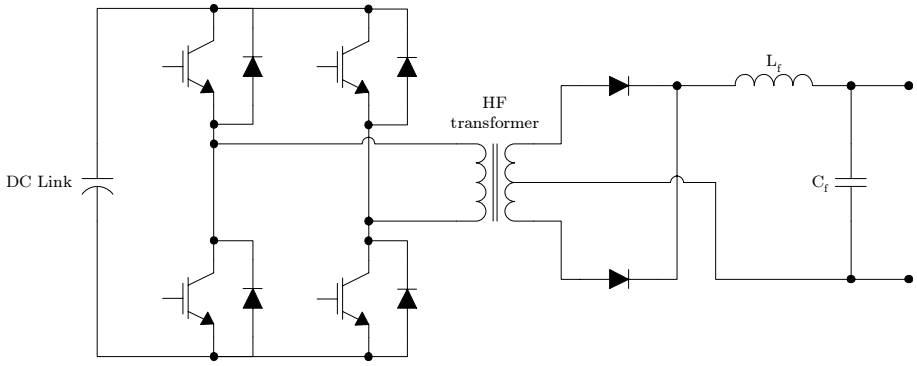


Figure 3.14: HF transformer configuration

solution that is chosen at ITER as described in Section 3.3.4. The advantage with this solution is that the transformer will not have to handle the pulse power, but can charge the capacitors at average power. The drawback is that the maximum output voltage of a converter is restricted by the transistor voltage ratings. Voltage can easily be increased by serial connection of modules, but to reach high voltages the number of modules has to be high. Also stray capacitance between the switches and ground will cause interference on the driving signals as the modules shift in potential. This was also discussed for the Marx generator in Section 3.2.

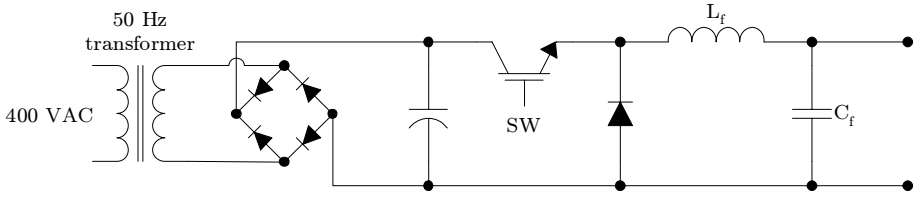


Figure 3.15: Pre transformer configuration

3.3.3 Step-up Converter

Another possibility based on present technology is the buck-boost converter [17]. The buck-boost converter allows for a regulated output voltage while also offering voltage amplification. A pure boost converter could deliver higher output voltage, but is unable to disconnect the load during pulse-off and would thus require a second switch.

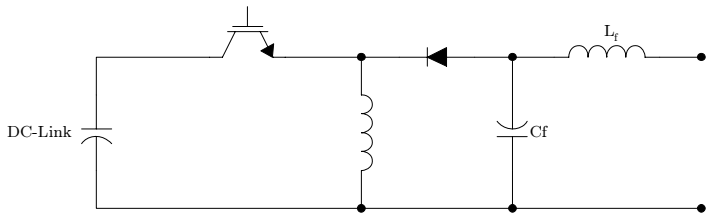


Figure 3.16: Buck-Boost converter

The buck-boost converter has a negative output in respect to input ground. The Klystron requires negative voltage, and initially this may seem to be an advantage. But the output voltage has to be further stepped up, either through inductive adding of several modules or through a pulse transformer. In both cases the output will be decoupled from the ground potential and the polarity of the output will not matter.

The buck-boost converter can operate in the same configuration as the direct PWM proposed above, except for the advantage of higher output voltage. But there are also some drawbacks in respect to the direct connected solution:

- To achieve a significant step-up ratio the duty cycle has to be close to 100%. This results in high di/dt and high ripple on the output.
- To remove the ripple on the output heavy filtering is required. The energy contained in the filter can make the converter vulnerable in case of an arc.

3.3.4 Existing Systems

At ITER, the fusion research program in Cadarache, France, a converter based on this principle is projected to supply a 170 GHz, 2 MW gyrotron. [7] The gyrotron is used as a part of the plasma heater system to control instabilities in the plasma. The required time constants for the power supply to stabilize the system are short and require the resultant switching frequency to be in the range of 700 kHz. This is achieved by using a serial connection of 50 modules. The modules are galvanicly insulated from the grid by a transformer with 50 separated secondary windings. This allows for the modules to be serial connected and can be viewed as an inductive

adder system where the adding takes place before the converter. The ITER gyrotron is a capacitive load, and to perform the desired operation, two quadrant operation is required. Each module is operated with a switching frequency of 14 kHz.

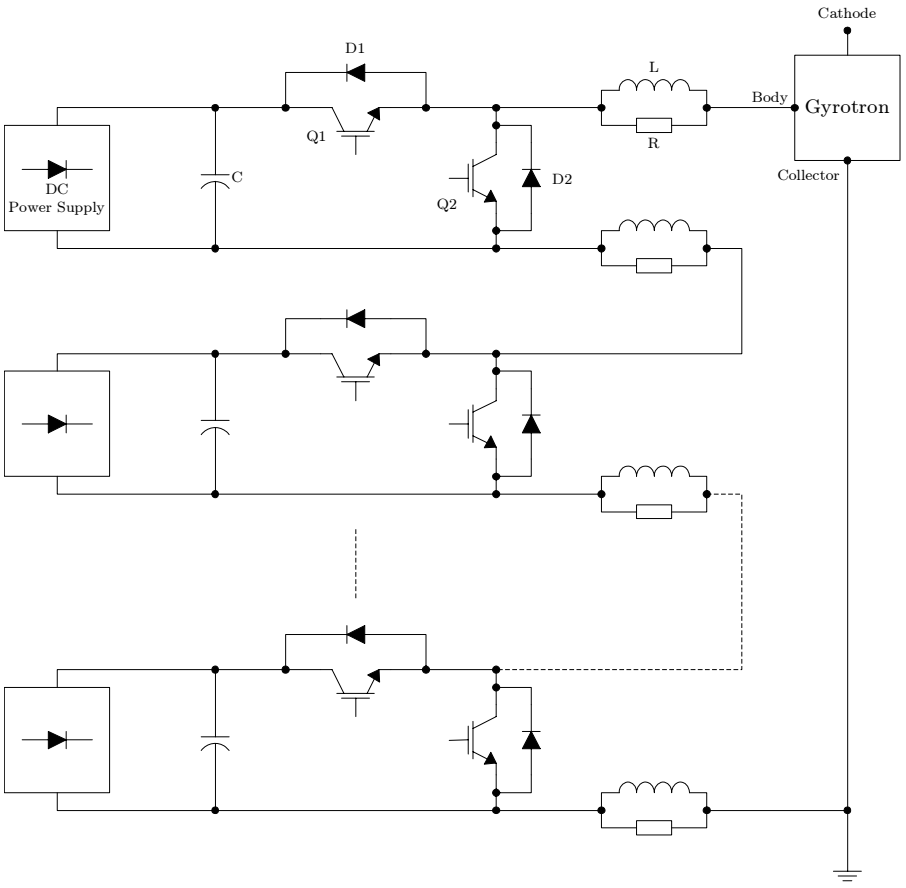


Figure 3.17: Gyrotron modulator at ITER

The paper on this power supply presents a successful test using only 5 modules. The paper concludes on creating the full scale system, but it is not known if this has been successful. [7]

3.3.5 Summary Direct Modulator

The advantage of the direct modulated converter is that it has the ability to control the output. With several serial connected modules it is possible to achieve good regulation capabilities for the output pulse with around 100 samples resolution. Also the system can achieve high rise and fall times. It can be equipped with a surplus of modules so that the system is redundant.

Depending on the configuration, it is also possible to avoid pulse trans-

formers. Inductive adding makes it possible to interleave the switching schemes of the modules, which significantly increases the resultant output ripple frequency and reduces the ripple amplitude. The fast switch and response time should also make the converter able to handle the arc requirements of the Klystron.

The main drawbacks are the switching loss and the high number of cells required to reach 100 kV. The buck-boost configuration has an advantage over the one quadrant converter when it comes to output voltage. However, the configuration will produce a saw tooth like current and will have poor average current factor in respect to the one quadrant converter. These considerations must be taken into account and evaluated in respect to the application.

3.4 Resonant Converter

The resonant converter can be viewed as an extension of the direct modulator topology. A resonant circuit consisting of a capacitor and an inductor is connected between the load and the H-bridge. One of the benefits with the resonant converter is that it may allow for *soft switching*. Soft switching is when the switching occurs with close to zero current or voltage. This can substantially reduce the switching losses and may therefore be an interesting solution for the Klystron modulator. However, the resonant circuit also places some significant limitations on the converter. Due to the resonant circuit, the output will have a large quasi-sinusoidal AC component on the output. It is therefore difficult to modulate arbitrary waveforms with the resonant converter. The usual application where the resonant converter is used is constant DC/DC converters where the output is rectified and filtered. This will also be the most probable configuration for a Klystron modulator. The control of the system is quite complicated compared to the direct modulator topology and it can be demanding to obtain the soft switch condition.

There are mainly two different resonant converter configurations that may be relevant for a Klystron modulator, the *parallel resonant converter* (PRC) and the *serial resonant converter* (SRC). [17, p.253]

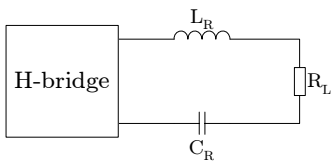


Figure 3.18: SRC

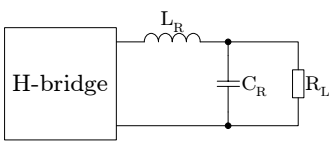


Figure 3.19: PRC

The properties of the two converters are quite different. The important

difference between the topologies in respect to the Klystron modulator is the amplification capabilities. The PRC has the ability to amplify the voltage, whilst the SRC at maximum can achieve unity. For the Klystron modulator the amplification capability is a welcome feature since the 100 kV output voltage requires extensive voltage amplification. Also the PRC works well with transformers since the leakage inductance and stray capacitance of the transformer can be incorporated as a part of the resonant circuit. The SRC on the other hand will always be vulnerable to the transformer parasitics since its inverse construction makes the resonant circuit work against the transformer.

When operating close to resonance, the SRC approaches voltage source characteristics, while the PRC approaches current source characteristics. Since the load can be assumed purely resistive, this is of little importance. In the short circuit case however, the PRC have a better response since the current source characteristics will deny excessive over currents. Depending on the operating frequency, the SRC will also limit the short circuit current, but not as effective as the PRC. Since all the differences of the two configurations are in favor to the PRC, this is chosen as the preferred choice for the Klystron modulator.[13]

When operating resonant converters, the response of the resonant circuit has to be respected and attended to. For instance PWM operation of a resonant converter will not give the desired result. Two common ways to operate the resonant converter is with frequency control and with phase control. The duty cycle should always be 50% so that the resonant circuit operates with zero DC conditions. This is especially important when operating the PRC with a transformer so that DC currents are avoided in the transformer.

Figure 3.20 shows the frequency response of a PRC with resonance frequency of 20 kHz. The response is plotted for several Q-factors which correspond to different resistive loads. High Q means that the load has high impedance compared to the resonant circuit. The frequency response plot shows the two crucial points mentioned earlier:

1. The PRC can offer voltage amplification when configured correctly

2. When the PRC is short circuited, which corresponds to a decrease in Q-factor, the output voltage sees natural attenuation

It can also be seen from Figure 3.20 that as the voltage amplification increases, the frequency sensitivity of the output voltage increases. Thus there are limits to how much amplification can practically be obtained. A factor of 3 seems to be a good compromise.

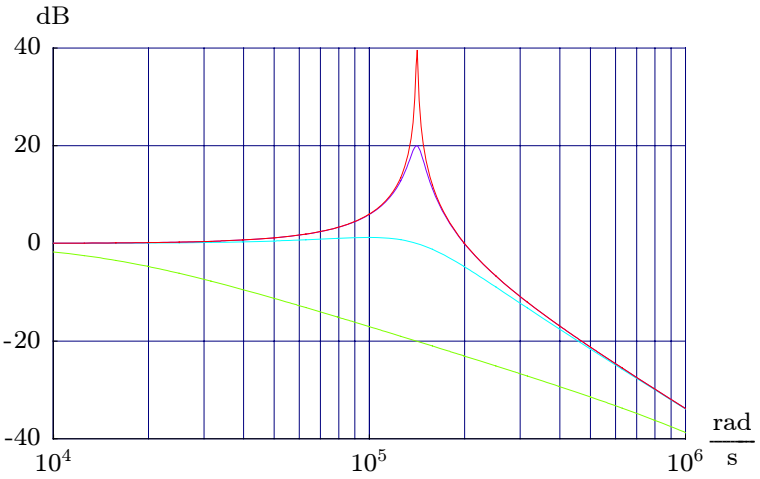


Figure 3.20: Frequency responce of 20 kHz PRC at different Q-factors
Red: Q=100, Violet: Q=10, Cyan: Q=1, Green: Q=0.1

3.4.1 Existing Systems

Los Alamos National Laboratory in USA, best known for the nuclear developments through the Manhattan project, has developed one of the first high voltage pulse converters based on resonant technology. The converter is supplying high power Klystrons in the particle accelerators at Oak Ridge National Laboratory (ORNL). One converter is also in temporarily use at Stanford Linear Accelerator Center (SLAC).

Figure 3.21: Los Alamos National Laboratory

The advantages of resonant converters in these applications are the possibilities for high switching frequencies, and thus fast feedback voltage regu-

lation, low energy in the high voltage circuit and high efficiency. Several converters with different ratings have been constructed, but they are all based on the same principle. The configuration is module based which makes it easy to scale the system to desired current and voltage rating through serial or parallel connection of modules.

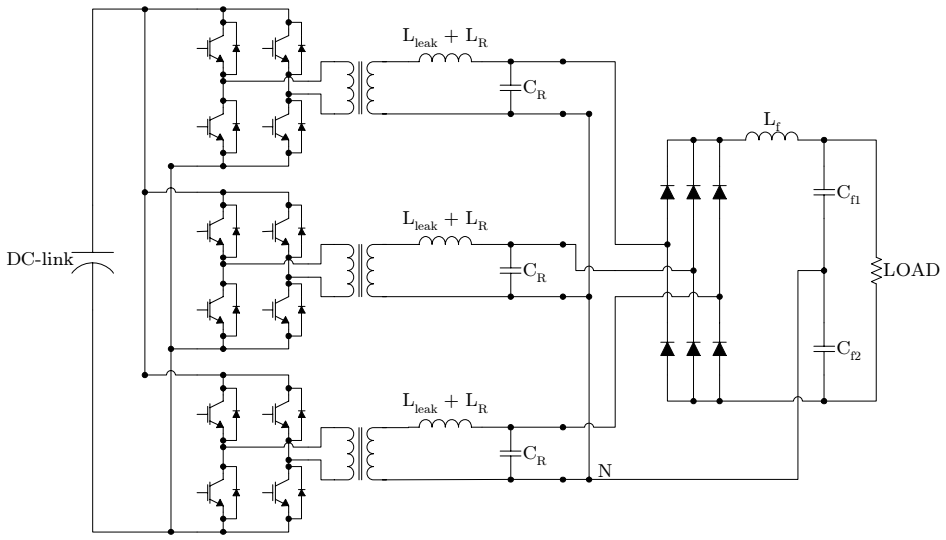


Figure 3.22: PRC based converter developed by Los Alamos

The basic configuration is based on three separately excited resonant circuits as shown in Figure 3.22. The circuits are star connected on the output to form a normal 3-phase system. This makes it possible to use 3-phase calculus to analyze the system. The first converter built was rated 10 A @ 25 kV for a 1-2 ms pulse. [5] Later, power converters have been built with power ratings increased by orders of magnitude. The Spallation Neutron Source [20] is powered by a 11 MW resonant converter at 80 kV. The average power is 1.1 MW.

3.4.2 Summary Resonant Converter

The PRC looks like a promising topology for the Klystron modulator. It can offer voltage amplification and short circuit protection. Also it can be constructed as a modular based converter, and when operated with soft switching, the converter can be operated with both high power and high repetition rate. The PRC should be further investigated as a possible future Klystron modulator.

Chapter 4

Single Switch Topology

The CERN prototype that is under development is based on the single switch topology. In this chapter the topology is studied in detail and the theory of importance is addressed. The chapter examines the different aspects of the single switch topology and successively goes through the circuit by addressing, among others, the energy storage, the switch, and the pulse transformer. In the end the more general concepts for a full scale system are discussed. Most subjects are both discussed in a general manner and in the special case of the Klystron modulator.

4.1 Energy Storage

The peak-to-average power factor in pulsed applications is often high. As can be calculated from the requirements in Chapter 2, the Klystron modulator has a peak-to-average factor of 625. It is rarely feasible to size the upstream grid infrastructure for the full pulse power when the average power is so low. Also the implications of running a high power pulsed system directly on the grid would be extensive in the case of flicker and other disturbances. These applications therefore usually rely on an intermediate energy storage that can charge at average power and discharge at peak power. In normal pulsed applications that are not operating close to the extremes, capacitive energy storage is usually the most suitable solution.

The required pulse energy can be calculated by Equation 4.1. Here V_O and I_O are the pulse voltage and current, T_{pulse} is the pulse duration and η represents the efficiency of the converter. A calculation based on the values given in Chapter 2, and based on a total converter efficiency of 0.90 results in a required pulse energy of 1.8 kJ.

$$W_{pulse} = \frac{V_O \cdot I_O \cdot T_{pulse}}{\eta} \tag{4.1}$$

The energy stored in a capacitor of capacitance C is directly dependent on the capacitor voltage and is given as $W_C = 1/2CV^2$. A total energy

extraction from the capacitor therefore implies a full discharge down to zero voltage. Since this seldom leads to good operation, the capacitor should be oversized so that the voltage droop is kept within a specified tolerance. Equations 4.2 to 4.4 gives the required capacitance as function of the pulse energy and the accepted voltage droop. The accepted droop is denoted as d and is given in per unit.

$$W_{pulse} = \Delta W_C = \frac{1}{2}CV_1^2 - \frac{1}{2}CV_2^2 \tag{4.2}$$

$$V_2 = V_1\,(1-d) \tag{4.3}$$

$$C = \frac{2W_{pulse}}{V_1^2\,(2d-d^2)} \tag{4.4}$$

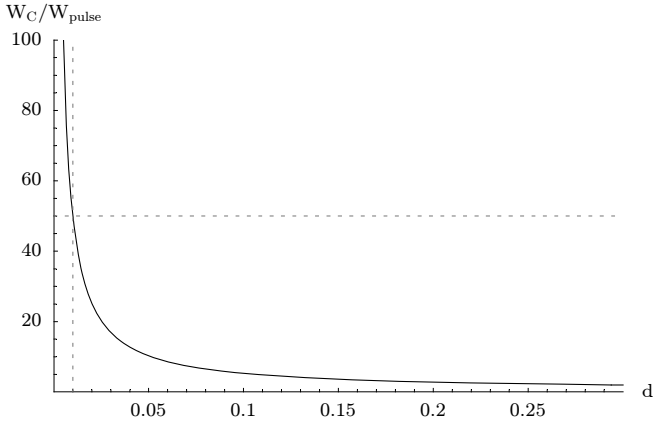


Figure 4.1: Capacitor oversizing factor

Figure 4.1 shows the general relationship between the capacitor over sizing factor and the accepted voltage droop. The maximum accepted voltage droop for the Klystron modulator is 1 %, and as indicated by the graph this requires a 50 times over sizing factor.

Depending on the total energy requirement, and the configuration, it may be feasible to reduce the size of the capacitor and compensate the exceeding voltage droop by a separate compensation circuit. This is a question of size, costs and development. Given the strict droop requirement for the Klystron modulator, a compensation system will be advantageous. The design of this is discussed in detail in Chapter 5.

4.2 Switch Technology

Available solid state switches can be divided into two families; the full controlled switches and the thyristors. The thyristors are unable to turn off a

flowing current and are dependent on natural commutation in the circuit to switch off. Thyristors generally have higher ratings, are more robust and are easier to control than the other types of switches. The thyristor is therefore usually the preferred choice in AC applications where natural commutation occurs. In some non-commutating applications where the use of thyristors is strongly desired it is possible to force commutation by external circuitry, such as a *pulse forming network* [18]. The savings are however usually outweighed by the additional circuitry, and these configurations are rare.

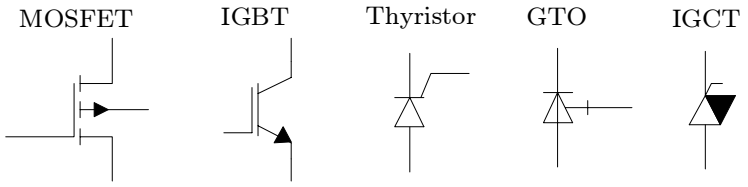


Figure 4.2: Some transistor switches

Since the Klystron requires switch-off capabilities the thyristor is unsuitable. The commonly used full controlled solid state switch devices are IGBT, IGCT, GTO and MOSFET. The abbreviations denote respectively: *Insulated Gate Bipolar Transistor*, *Insulated Gate Controlled Thyristor*, *Gate Turn Off thyristor* and *Metal-Oxide-Semiconductor Field-Effect Transistor*.

The GTO is an extended version of the thyristor that can be switched off. Like the thyristor the GTO has high power rating, but has a long switch-off time compared to the other devices. The IGCT has slightly higher ratings than the IGBT, but requires more complicated driving systems. IGCTs are only manufactured by ABB and usually come with an on-board driver to deal with the driver difficulties. MOSFET is the fastest switch and can operate at switching frequencies up to 1 MHz, but have poor power ratings. Because of the high variety of available systems and the less demanding driver requirements, the IGBT is the most popular and versatile solid state technology. It is usually the preferred choice for full controlled switching. The high power rating and quick switching speed required in the Klystron modulator suggests that the circuit should be based on either IGBTs or IGCTs.

4.2.1 Voltage Increase by Serial Connection

Currently the maximum available voltage rating on IGBTs is around 6 kV. [21]. A common way to reach higher switching voltages than the voltage rating of the solid state modules is to connect several modules in series. The resulting total operating voltage will then ideally be the individual voltage rating times the number of modules in the series chain.

However, to develop a reliable serial connected switch is not an easy task.

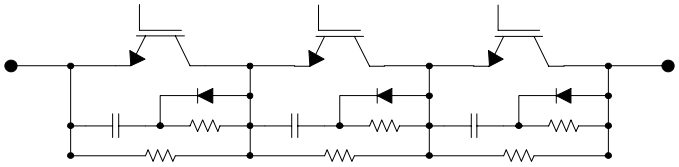


Figure 4.3: Serial IGBT chain

The low resistance and the varying voltages over the solid state switches make them vulnerable to over voltage due to imbalances in the system. The overloading capabilities of solid state switches are low, so there is little margin to play with. The challenging part is usually to keep the voltage balanced between the switch modules during the switch transients. With the high switching speed of current modules, the timing accuracy and precision required is demanding.

Development of a good serial connected switch system is a long and demanding process. Applications that require high switching voltages and are to be produced in low quantities are usually based on ready made switch systems supplied by companies that have worked out these issues.

4.3 Snubbers

The circuit that incorporates the switch always includes some small inductance linked to the physical size and geometry of the system. Given the fast switching speed of modern power electronics, this inductance may cause problems for the switch. As the switch is about to turn off, and the load current is quickly to be brought down to zero, an over voltage caused by the inductance will add to the already present voltage. The over voltage is given as $L\,di/dt$, and is thus proportional to the switching speed of the switch times the inductance present in the circuit. This over voltage may be critical for the switch, and in most configurations *snubbers* are included to protect the switch. The simplest snubber configuration is a RC circuit that is connected in parallel with the switch. A more effective configuration is the DRC snubber which also incorporates a diode. This configuration is shown in Figure 4.4.

The principle of the snubber is to allow for a continuous flow in the load current when the switch is turned off and the switch current is quickly halted. The initial voltage of the snubber capacitor is zero, and as the capacitor voltage builds up, the load inductor current is braked down in a controlled manner.

When dimensioning the DRC snubber several considerations have to be taken. The size of the capacitor is the most important factor. The capacitor has to be large enough to hold the necessary inductive energy without causing over voltage on the switch. But it is also important to note

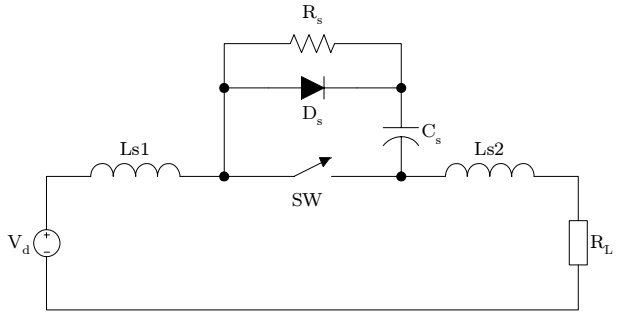


Figure 4.4: Switch protected with DRC-snubber

that the energy held by the capacitor in each switching cycle will be lost, so that the capacitor should not be sized larger than required.

When a suitable capacitance is selected, the resistor must be dimensioned. The purpose of the resistor is to slowly discharge the capacitor upon switch-on. The resistor should be chosen so that the discharge current is not endangering the switch. Secondly it must be sized so that the snubber capacitor is completely discharged before the switch-off occurs. Based on this it can be seen that the snubber should be tailor made for the specific application.

In a circuit with a purely resistive load, the system can easily be evaluated analytically. It is the switch-off that is important when dimensioning the snubber, and a simplified circuit to analyze this event specifically is given in Figure 4.5.

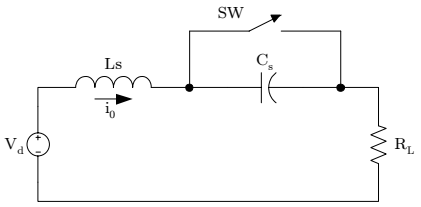


Figure 4.5: Simplified circuit suitalbe for analysis

Before switch-off the circuit operates at steady state with zero capacitor voltage and inductor current equal to the load current. After switch-off the circuit is simplified to a serial connection consisting only of linear components. The circuit can then be analyzed by Kirchhoff's voltage law.

$$V_d + L\frac{di}{dt} + iR + \frac{1}{C}\int i\,dt = 0 \tag{4.5}$$

$$L\,i''(t) + R\,i'(t) + 1/C\,i(t) = 0 \tag{4.6}$$

$$L\lambda^2 + R\lambda + 1/C = 0 \tag{4.7}$$

$$\zeta = \frac{R}{\sqrt{L/C}} \tag{4.8}$$

ζ represents the damping of the system where $\zeta > 1$ is an overdamped system and $\zeta < 1$ gives an underdamped system. If the system is overdamped, the switch voltage can never climb above the source voltage, which gives a safe configuration. If it necessary to reduce the snubber power loss, the snubber design can be moved slightly into the underdamped area. The peak voltage over the switch will then exceed the source voltage, and such a design must be carefully fitted to the circuit.

4.4 Pulse Transformer

All general transformers can handle pulses if the pulse is kept within the voltage rating of the transformer, and within the voltage-time integral limitations of the magnetic of the core. However, general transformers have substantial parasitics and energy carrying elements in them which may not affect normal operation, but can have a great negative impact when operated with pulses. This results in output pulse distortion.

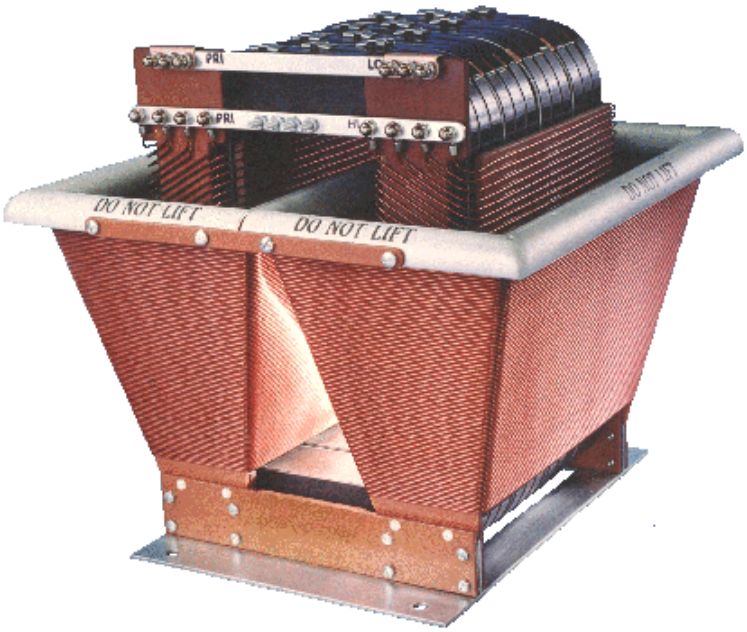


Figure 4.6: Pulse transformer

Pulse transformers are designed specifically to handle square pulses and are precisely constructed to reduce pulse distortion. It is impossible to achieve ideal transforming and some distortion always occurs. Figure 4.6 shows a typical pulse transformer. A transformer equivalent circuit that is suitable for pulse transformer analysis is shown in Figure 4.7.

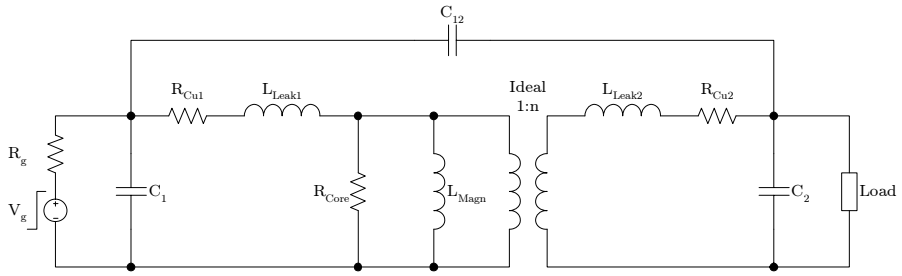


Figure 4.7: Transformer equivalent suitable for pulse analysis

It is important to note the capacitive connection between the primary and secondary, which corrupts the decoupling effect of the transformer. It is caused by the capacitive coupling between the primary and secondary winding and is possible to eliminate by using shielded coaxial cable on the windings. The extra shielding complicates the cable insulation and results in increased size, cost and complexity. For high voltage applications the shielding may be very impractical.

It is possible to transform the circuit to a simplified equivalent with all parasitics referred to the primary, as showed in Figure 4.8. A crucial observation in relation to this is to note that the secondary leakage inductance, as seen from the primary, is given by Equation 4.9 [6]. This relationship contributes to restrict the maximum possible step-up ratio which usually is in the low tens.

$$\acute{L}_{leak2} = L_{leak2} \cdot n^2 \tag{4.9}$$

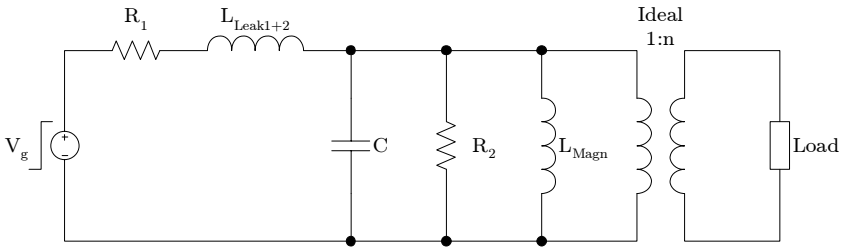


Figure 4.8: Transformer equivalent referred to the primary

When the pulse transformer is pulsed with an ideal square pulse on the input, the output pulse distortion can be described by the standard

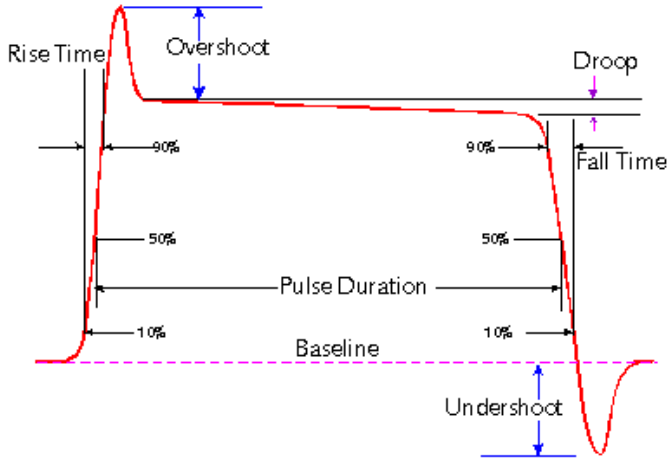


Figure 4.9: Typical output waveform

model for square pulse distortion as shown in Figure 4.9. The 800 μs pulse time required by the Klystron is considered as a long pulse in relation to pulse transformers. The capacitive couplings are usually small compared to the leakage inductances and influence most on short pulses. It is therefore expected that the overshoot and ringing imposed by the capacitive effects will be short and of little importance for the Klystron modulator. On the other hand, the leakage inductances and the magnetizing current will be significant. The distortion from these is described separately in the following subsections.

4.4.1 Delayed Rise Time

The effect of the leakage inductance on the pulse is increased rise time. The issue can be studied in detail by considering the simplified equivalent circuit in Figure 4.10. Here the leakage inductances are combined and referred to the primary. The other parasitics are neglected as they have little influence on the rise time. The load is assumed purely resistive and is also referred to the primary. The simplified model represents a first order circuit and can be analyzed accordingly.

$$\tau = \frac{L_{eq}}{\acute{R}_{load}} \tag{4.10}$$

$$v_R(t) = v_{C0}\left(1 - e^{-\frac{t}{\tau}}\right) \tag{4.11}$$

$$t_{rise} = t_{90} - t_{10} = \tau\left(\ln 0.9 - \ln 0.1\right) \approx 2.2\tau \tag{4.12}$$

$$t_{rise} \approx 2.2 \frac{L_{eq}}{\acute{R}_{load}} \tag{4.13}$$

The Klystron requires a 700 μs flat-top polarization voltage and increased rise time leads to a prolonged input pulse, higher energy requirement and reduced efficiency. The converter specifications define the maximum rise time to 100 μs. If the step-up ratio is assumed to be 10 this gives $\acute{R}_{load} \approx 50\Omega$ and leads to a maximum allowable leakage inductance of 2.2 mH referred to the primary. A comparison by other pulse transformers with these ratings suggests that this can easily be achieved.

4.4.2 Voltage Droop

The increasing magnetizing current during the pulse will cause a gradually increasing voltage droop due to the winding resistance. In normal operation the magnetizing current is increasing linearly with the voltage-time integral of the pulse, but if the magnetizing current is allowed to enter the saturation region, there will be a runaway effect that will cause a severe voltage droop. This is undesired and the transformer should be designed to avoid core saturation during normal operation. The magnetizing current is governed by Faradays law of induction, reproduced in Equation 4.14.

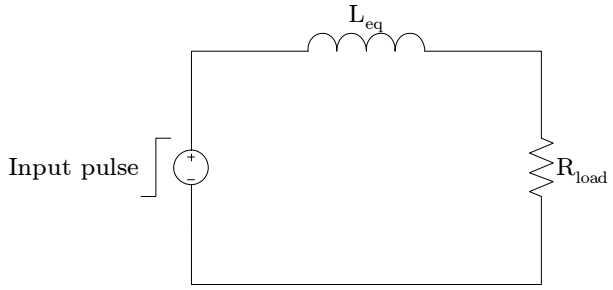


Figure 4.10: Equivalent circuit for rise time calculations

$$e = N \frac{d\Phi}{dt} \tag{4.14}$$

$$e = N \cdot A \frac{d\Phi}{dt} = k \cdot \mu_r \cdot A \frac{di}{dt} \tag{4.15}$$

If it is assumed that the transformer core has a maximum allowable threshold flux, Equation 4.15 states that a longer pulse will require a larger core area. This relationship gives the rule of thumb for pulse transformers which states that the transformer cost increases proportional with the voltage-time integral.

4.4.3 Undershoot

At the end of the pulse the magnetizing current is running at its maximum. When the voltage source is disconnected, the primary side usually acts like an open circuit. If there is no undershoot network installed in the circuit, the magnetizing current will discharge trough the load by running a reverse current, thus causing an undershoot. This effect is taken advantage of in such circuits as the fly back converter [14]. However, in devices that cannot handle negative currents the back swing can be damaging if not handled properly. The Klystron has diode characteristics due to the unidirectional electron flow and must be protected for undershoot.

One way to handle the undershoot is to insert a freewheeling diode which will prevent negative output voltages. However, this can be problematic in repetitive pulse applications since the discharging time constant will be very high and the magnetizing current can keep on flowing for a long time. It is important to completely discharge the magnetizing current before next pulse is fired to avoid current build up and saturation. The dilemma is that the negative voltage required to discharge the magnetizing current also will appear on the secondary side, but upscaled according to the step-up ratio. This relationship makes it impossible to completely avoid the undershoot and also participates in limiting the possible step-up ratio.

It could be possible to reduce this effect by placing a diode in series with the load so that the load is protected against the negative voltage. To be sure that the undershoot voltage is subjected to the diode a resistor should also be put in parallel with the load. It is desired to keep the number of components on the high voltage side down due to the isolation issues, and it is preferable to handle the undershoot on the primary side.

Usually the undershoot can be handled by adding a parallel connected capacitor and resistor in series with the freewheeling diode as shown in Figure 4.11.

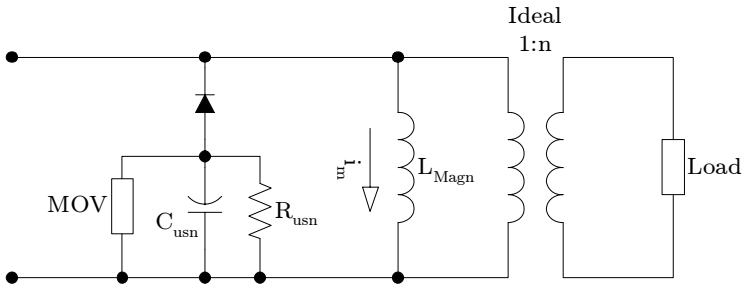


Figure 4.11: Tranformer with undershoot network

This allows the major part of the magnetizing energy to be transferred to the undershoot capacitor, in order to be slowly discharged through the resistor. The undershoot network should be designed to meet the requirements

of the application. A MOV can be included to serve as extra protection for over voltages. For the Klystron, the duration of the reverse voltage is unimportant as long as it is kept within the required limits. The undershoot network should be sized accordingly.

4.5 Inductive Adder

As discussed earlier the pulse transformer step-up ratio has its limitations and step-up ratios over a few tens are generally not practical. One way to further increase the voltage without violating this is to utilize inductive adding. This principle works by serial connection of several galvanicly decoupled modules as suggested in some of the topologies in Chapter 3. An example of inductive adding is shown in Figure 4.13. The advantage of an inductive adder is that, except from the secondary winding to ground coupling, no components are exposed to the full output voltage. Each stage can be controlled individually, and except for adding stray capacitance to the system, there are no limitations to the number of stages. The inductive adder can very well be realized by normal transformers and pulse transformers. It is possible to utilize inductive adding with a single transformer by adding several primary windings. A pulse transformer configuration consisting of 5 primaries would bring the switch voltage down to 2.4 kV and thus eliminate the need for stacked switch configurations. An example of this configuration is shown in Figure 4.12.

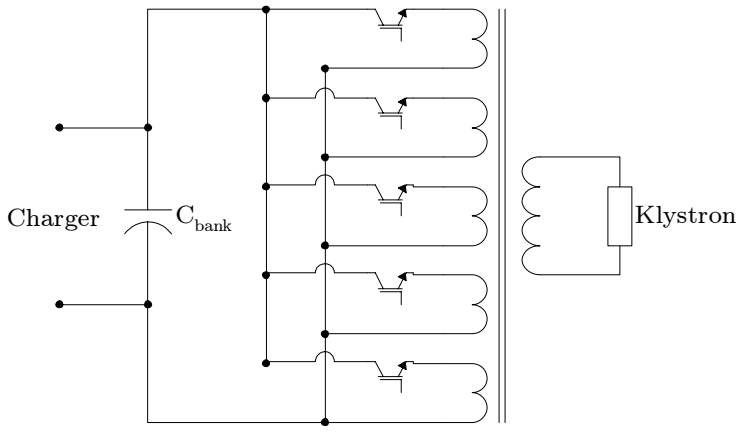


Figure 4.12: Pulse transformer with multiple primary windings

More exotic solutions are the one winding system where a single turn of high voltage cable is guided through the center of several toroidal transformers. This concept is used in the fast kickers at SLAC [9] and showed in Figure 4.13. However, this is not practical for long pulses.

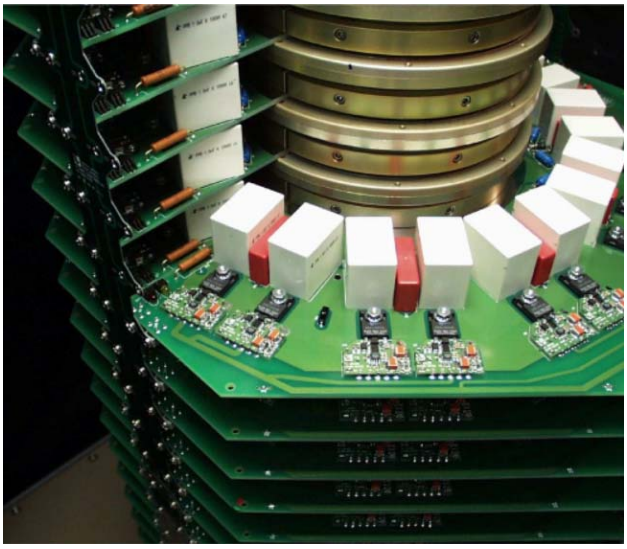


Figure 4.13: One winding inductive adder
The beam in the center is the one-turn secondary winding while the stack of toroidal primary windings can be seen around.

4.6 Modular Configuration

It is possible to create modular configurations consisting of several single switch converters to increase the ratings. One single switch converter can be considered as a module. By serial connecting the pulse transformer output of several modules it is possible to increase the output frequency, amplitude and pulse time:

- **Increased Frequency**
  The power ratings of the pulse transformer limits the output frequency. By operating several modules with interleaving, the output frequency can be increased with the multiple of interleaved modules. This is illustrated in Figure 4.14(a) and 4.14(b).

- **Increased Amplitude**
  The output amplitude is limited both by the voltage-time integral of the transformer core and the transformer insulation. The core limitation can be overcome by firing several serial connected modules simultaneously. The total output voltage can then be multiplied by the number of modules as shown in Figure 4.14(c) and 4.14(d). However, the insulation rating of the transformer cannot be amplified by this method and will be a limiting factor.

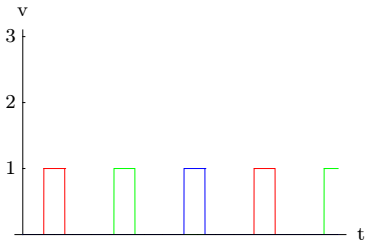
- **Increased pulse time**
  The pulse time is also limited by the voltage-time integral of the core.

By utilizing several modules the individual pulse voltage can be lowered so that the pulse time can be increased without violating the core ratings. This is shown in Figure 4.14(e) and 4.14(f).

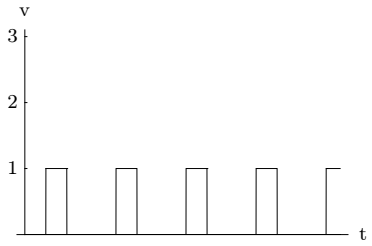
It can therefore be possible to meet various requirements with the single switch topology through modular configurations. The drawback with this method is that it requires several pulse transformers.

4.7 Summary

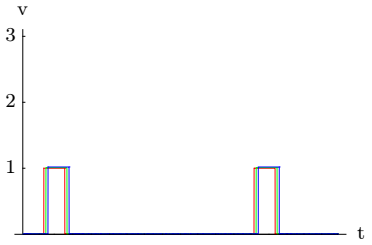
In this chapter the different aspects of the single switch topology was studied and the necessary analytical principles were derived. The work done in this chapter serves as a basis for the dimensioning and design done in Chapter 5 and 6.



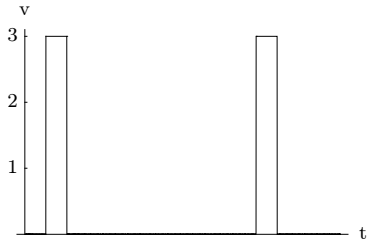
(a) Frequency increase - Module



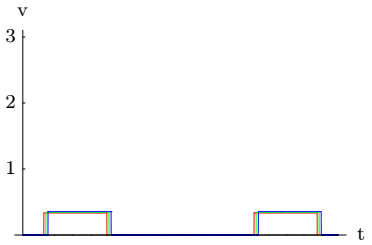
(b) Frequency increase - Sum



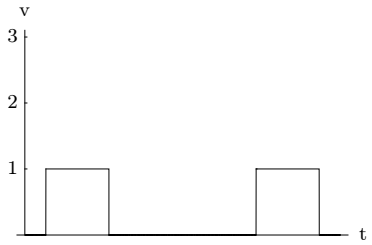
(c) Amplitude increase - Module



(d) Amplitude increase - Sum



(e) Pulse time increase - Module



(f) Pulse time increase - Sum

Figure 4.14: Modular configurations

Chapter 5

The Bouncer

Pulse applications that rely on a capacitor bank as voltage source requires voltage droop compensation if a constant output voltage is to be obtained. The bouncer, also referred to as the *passive bouncer* is probably the simplest way to perform voltage droop compensation in pulsed applications. It relies on a simple resonant circuit to supply the required compensation voltage. In the following sections the governing principles of the bouncer are analyzes in detail. Based on the analysis, a bouncer prototype is dimensioned and built.

5.1 Mode of Operation

The bouncer is incorporated into the circuit on the low voltage side after the load as shown in Figure 5.1. Initially both the main switch and the thyristor are open. The bouncer capacitor is charged with a positive voltage according to the polarity defined in Figure 5.1. When an output pulse is to be produced, the bouncer thyristor is fired ahead of the main pulse so that the capacitor starts to discharge through the inductor. The goal is to

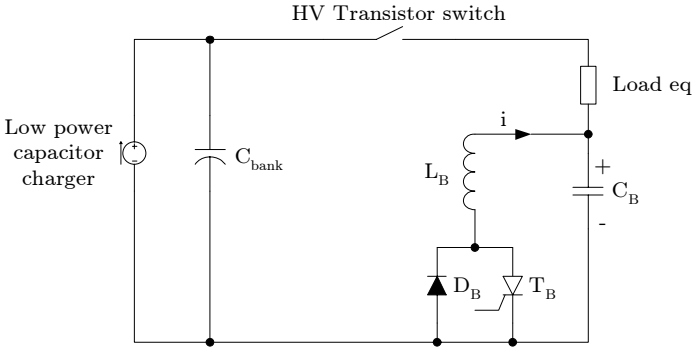


Figure 5.1: Single switch topology with bouncer

design the system so that the linear part of the sinusoidal capacitor voltage coincides with the output pulse. The bouncer will then compensate the close to linear voltage droop in the capacitor bank.

As the bouncer capacitor voltage approaches zero, the inductor current will reach its peak and thus force a negative voltage on the capacitor. Ideally the zero crossing of the capacitor voltage should occur at the center of the output pulse. After the pulse has ended the inductor current will continue to force a negative charging of the capacitor until the inductor current reaches zero. At the inductor zero current crossing the bouncer thyristor will close and the diode will open. The negative capacitor voltage will then charge back to the corresponding positive voltage through the bouncer inductor.

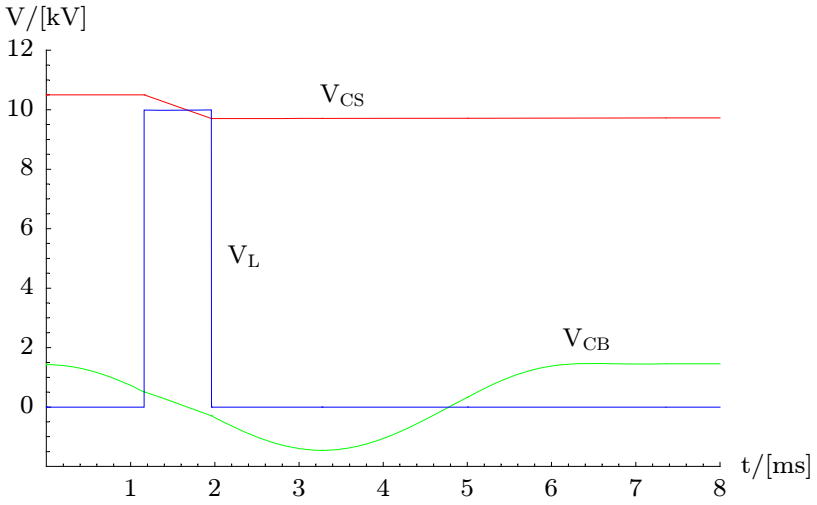
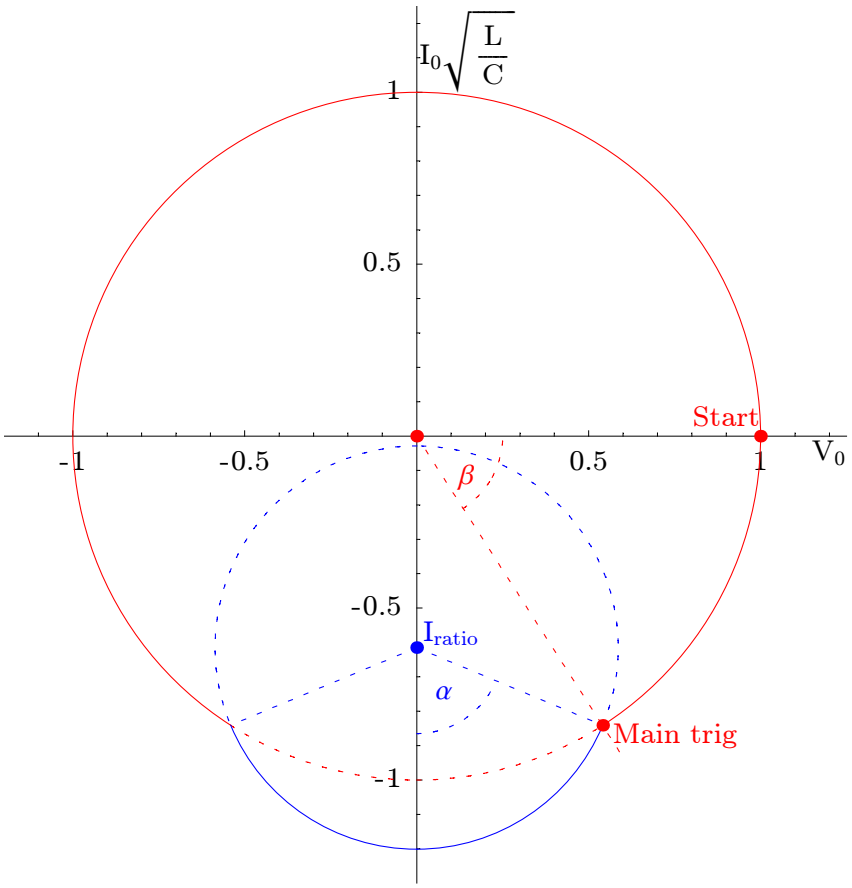


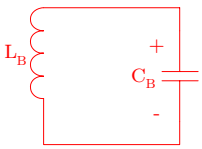
Figure 5.2: Time plot of bouncer operation

Figure 5.2 shows a simulation of the bouncer operation. The red line shows the voltage in the capacitor bank. During the output pulse, shown in blue, there is a voltage droop in the capacitor bank. The bouncer voltage, as given by the green line, can be seen to match the capacitor bank voltage during the pulse. The bounder voltage is subtracted from the capacitor bank voltage and the resulting output flat-top is well compensated.

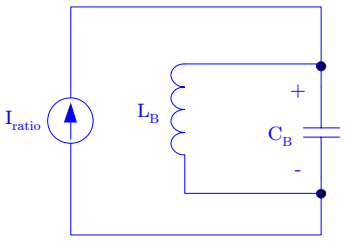
The bouncer operation can analyzed by utilizing *phase plane analysis* [10] where the capacitor voltage and inductor current is plotted as a time based parametric plot. This method is explained in detail in Appendix A. The phase plane plot for the bouncer is shown in Figure 5.3(a). The operation can be divided into two sections, the operation during pulse-on and the operation before and after the pulse. During the pre- and post pulse operation the bouncer can be viewed as a free motion resonant circuit as showed in Figure 5.3(b). When the pulse is fired, the bouncer is subjected to the load current as shown in Figure 5.3(c). Since the load current can be



(a) Phase plane plot of bouncer operation



(b) Equivalent circuit, pulse off



(c) Equivalent circuit, pulse on

Figure 5.3: Bouncer phase plane analysis

assumed constant, the resonant circuit will still operate in free motion, but with different DC conditions. The angle α, marked in 5.3(a), is given by the pulse length.

If the bouncer is to be operated in repetitive mode, it is crucial that the circuit is designed so that the pulse is symmetrically divided by the zero voltage line. This is true for the plot in Figure 5.3(a). As can be seen from the phase plane plot, any deviation from the symmetrical case will lead to an end capacitor voltage different from the initial voltage. The bouncer will thus not be in steady state.

The simulation shown in Figure 5.2 is based on a bouncer with high level of stored energy compared to the compensated energy. It will be shown later that the bouncer should be designed with as low energy storage as possible to reduce costs and dimensions. Since a reduction in bouncer energy will reduce the output quality, the design must be a compromise between quality and costs.

5.2 Theoretical Analysis

Analytical expressions for the bouncer can best be derived from phase plane analysis. An important factor is the relationship between the peak bouncer inductor current and the load current. This is denoted I_{ratio} and defined by Equation 5.1. The peak conditions are defined as operation without load current, as given by the complete red circle in Figure 5.3(a).

$$I_{ratio} = \frac{I_{load}}{\hat{I}_{Lb}} \tag{5.1}$$

In the phase plane, the peak inductor current and peak capacitor voltage are both defined as unity for the free motion condition. The intersection point between the free motion condition and the pulse-on condition is crucial for defining the bouncer and is denoted (x_{is}, y_{is}). The free motion circle is defined by the equation $x^2 + y^2 = 1$. By defining the angle α as given in Figure 5.3(a), the intersection point can be calculated by Equation 5.2 and 5.3. α is a quality parameter and defines how large part of the sine wave that is to be used as compensation. A smaller α gives better linearity but heavier bouncer requirements. The optimum α value is derived later.

$$y_{is} = x \tan \alpha + I_{ratio} \tag{5.2}$$

$$x_{is} = \frac{-I_{ratio} \cot \alpha - \sqrt{1 - I_{ratio}^2 + \cot^2 \alpha}}{1 + \cot^2 \alpha} \tag{5.3}$$

When that the intersection point is known, the β angle can be found. β is an expression for the required time delay between triggering of the bouncer

and the output pulse. The relationship between angle and time in the phase plane is given by the resonant frequency of the bouncer, ω_0. Thus the delay time t_d is given by Equation 5.5.

$$\beta = \arctan \frac{y_{is}}{x_{is}} \tag{5.4}$$

$$t_d = \arctan \frac{\beta}{\omega_0} \tag{5.5}$$

From this the required resonant frequency can be calculated from the pulse time T_{pulse}:

$$\omega_0 = \frac{2\alpha}{T_{pulse}} \tag{5.6}$$

The required inductor and capacitor value for the bouncer can be derived from the resonant frequency by taking the energy distribution into consideration. As can be seen from Figure 5.3(a), the peak inductor energy must equal the peak capacitor energy:

$$\omega_0 = \frac{1}{\sqrt{LC}} \tag{5.7}$$

$$W_{Cb} = W_{Lb} \tag{5.8}$$

$$\frac{1}{2}C\hat{V_{Cb}}^2 = \frac{1}{2}L\hat{I_{Lb}}^2 \tag{5.9}$$

$$\hat{V}^2 = \hat{I}^2\sqrt{\frac{L_b}{C_b}} \tag{5.10}$$

The peak capacitor voltage $\hat{V}_{Cb}$ can be calculated from the required compensation voltage V_{comp}. When taking into consideration that the intersection point between the pulse-on mode and the free motion mode for the bouncer is given by (x_{is}, y_{is}), the compensation voltage can be found from Equation 5.11

$$V_{comp} = 2x_{is}\hat{V}_C \tag{5.11}$$

Now that $\hat{V}_{Cb}$ and $\hat{I}_{Lb}$ are known the capacitor and inductor value can be found:

$$L = \frac{\hat{V_C}}{\hat{I_L}\omega_0} \tag{5.12}$$

$$C = \frac{\hat{I_L}}{\hat{V_C}\omega_0} \tag{5.13}$$

The relationship between the required compensation voltage and the size of the capacitor bank is given by Equation 5.15:

$$\Delta W_{pulse} = \frac{1}{2} C_{bank} \left\{ \left(V_d + \frac{V_{comp}}{2} \right)^2 - \left(V_d - \frac{V_{comp}}{2} \right)^2 \right\} \tag{5.14}$$

$$C_{bank} = \frac{\Delta W_{pulse}}{V_d V_{comp}} \tag{5.15}$$

The energy difference can be found from the allowed voltage droop. These equations govern the operation of the bouncer. Next, the required parameters for a specific application will be discussed.

5.3 Dimensioning

When fitting the bouncer to a specific application there are four values that have to be specified:

- Pulse length
- Voltage droop that is to be compensated
- Load current
- Maximum allowed flat-top deviation

5.3.1 α value

α is a quality factor for the bouncer, and is defining how large part of the sinusoidal output voltage that is to be considered usable for compensation. Thus, the α angle is directly linked to the flat-top deviation. Since the pulse time will be short compared to the time constant of the capacitor bank, the voltage droop can be considered linear. Figure 5.4 shows some examples of different α values. It can be seen from the figure that $\alpha = \pi/6$ gives a good linear approximation. With higher values the deviation becomes more significant.

The total flat-top deviation can be directly calculated as a function of α by Equation 5.16. Figure 5.5 shows the total deviation ϵ as a function of α for a circuit with 10% droop before compensation. As can be read of the graph, the marginal α-value to keep the deviation below 1% is 1.29 radians. Given that the voltage droop will deviate some from the linear case, and that there will be some voltage droop and ripple from the pulse transformer, the final α-value should include some extra margin.

$$\epsilon = \frac{V_{comp}}{V_{pulse}} \cdot \frac{\sin\left(\arccos\frac{\sin\alpha}{\alpha}\right) - \frac{\sin\alpha}{\alpha}\arccos\left(\frac{\sin\alpha}{\alpha}\right)}{\sin\alpha} \tag{5.16}$$

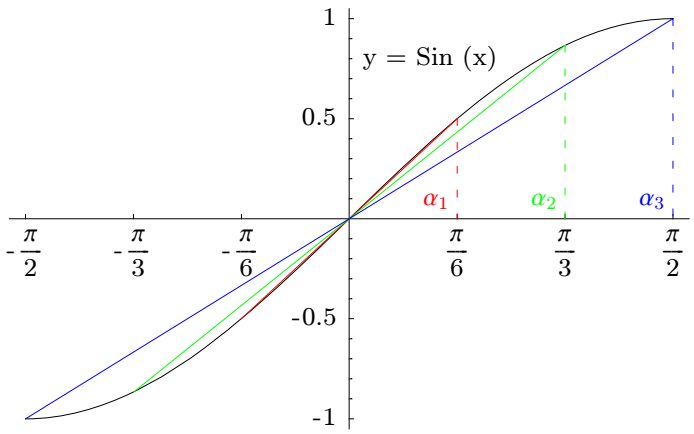


Figure 5.4: Different α values

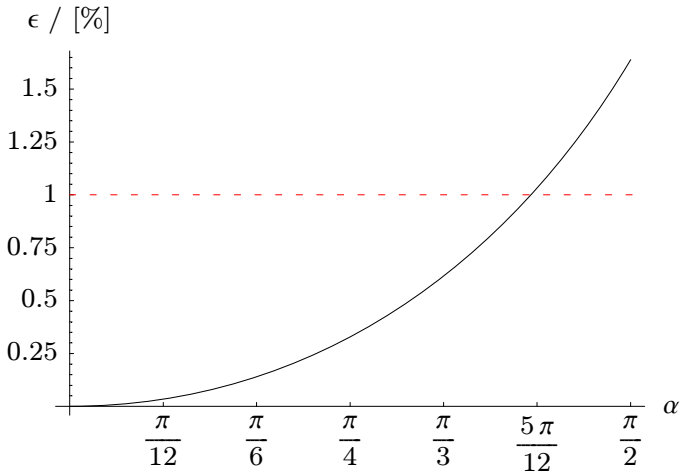


Figure 5.5: Flat-top deviation as function of α

5.3.2 Inductance value L_b

For long pulse applications that operate with a pulse time in the order of 1 ms, the total required energy is the dimensioning factor for the circuit. In contrast, power will typically be the dimensioning criteria for short pulse applications. It is most practical to use a normal copper wound iron inductor for this kind of application, and since these have substantially lower energy density than capacitors, the inductor becomes the dimensioning component for the system. The system should therefore be designed with the smallest possible inductor. An important parameter that has great impact on the required inductor energy is I_{ratio}. An algorithm to calculate the required inductance and inductance energy was developed and is attached in Appendix E. The results are shown in Figure 5.6 and 5.7.

The required inductor core volume is the most important factor for the inductor price. Since the core volume is proportional with the inductor energy, the required peak inductor energy becomes the interesting parameter. As can be seen from Figure 5.7, the inductor energy is at its lowest for I_{ratio} values between 0.6 and 0.9.

5.4 Transient Analysis

During start-up the bouncer has to be charged to the requred initial capacitor voltage by some means. There are three ways to reach the steady state condition:

1. Charging by external network
2. Natural internal charging
3. Forced internal charging

It is desirable to avoid any external circuitry to perform the initial charging process. The two internal charging methods are performed by using the existing circuit. The natural charging process is performed by simply operate the bouncer as if it was operating in steady-state. In this case the bouncer will slowly approach the steady state condition. The required number of cycles to reach steady state depends on I_{ratio}. Natural charging with three different values of I_{ratio} are showed in Figure 5.8(a), 5.8(c) and 5.8(e).

The forced charging process is performed by operating the bouncer in the most effective way during startup. It can be seen from phase plane analysis that the fastest charging can be achieved by firing the bouncer thyristor simultaneously with the output pulse until the bouncer is completely charged. As for the natural charging case, the required number of cycles for the forced charged case is heavily dependent on I_{ratio}. Forced charging will always be faster than natural charging. Three examples of forced charging are showed

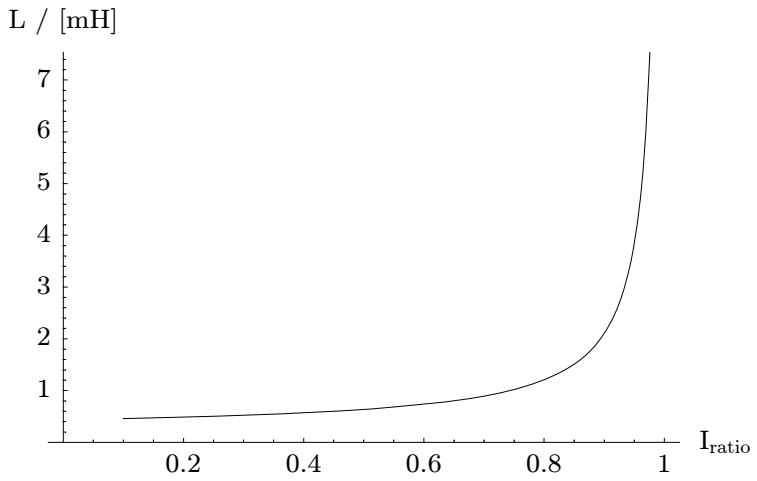


Figure 5.6: Requred inductance as function of I_{ratio}

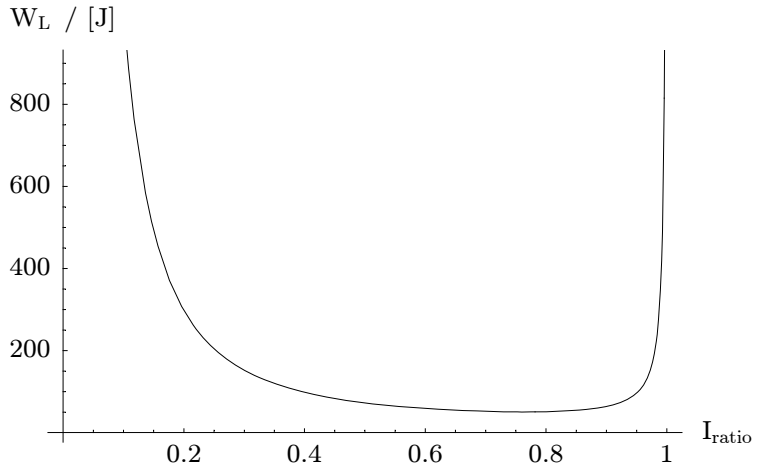


Figure 5.7: Inductance energy as function of I_{ratio}

in Figure 5.8(b),5.8(d) and 5.8(f). The forced charging should be stopped when the steady state condition is reached. This is not done in the examples shown in the figures.

As can be seen from the figures, the first charge cycle is equal for both natural and forced charging. The reason for this is that the initial capacitor voltage is zero, so that when the bouncer is fired ahead of the pulse the first time, nothing happens. These calculations are based the assumption that the thyristor is still open when the main pulse is fired. As will be shown in section 5.4.1, this is not necessarily the case.

It can be seen from Figure 5.8(e) and 5.8(f) that the bouncer actually is charged *above* the steady-state level on the first cycle. This can be avoided by firing the bouncer thyristor with a delay after the main pulse. The overcharging case also suggests that there is a value of I_{ratio} between 0.5 and 0.7 that allows for a direct charging to the steady-state voltage on the first cycle.

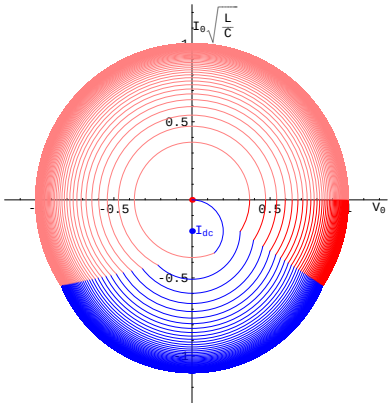
5.4.1 Open Bouncer Thyristor

A typical thyristor firing circuit usable for single pulses consists of an amplifier and a 400 μs pulse transformer. Given that the first pulse may be fired without any voltage over the capacitor, the thyristor may fail to close. Depending on the delay time between the bouncer firing and the output pulse, there is a possibility that the bouncer thyristor will be open when the output pulse is fired. The result is that the bouncer capacitor is connected in series with the load, and may suffer excessive charging. This must be considered when designing the control structure.

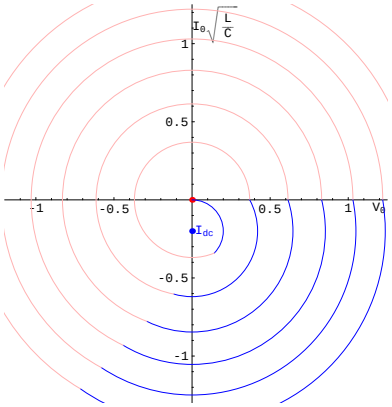
5.5 Operation and Control

Based on the findings in section 5.4, the charge process should be controlled so that the bouncer is fired simultaneously with the main switch. One solution is to obtain this is to use feedback control so that the delay time is regulated in respect to the capacitor voltage. This can also solve the open thyristor problems. The regulation process should be based on feedback from the capacitor voltage. Since the delay time can only be altered ahead of a bouncer run, the regulator has to operate in discrete steps. The best way to do this is probably to calculate the time delay for the next run when the current run has ended and the voltage in the bouncer capacitor is constant. This requires an algorithm that can calculates the required time delay from the true voltage and a given reference.

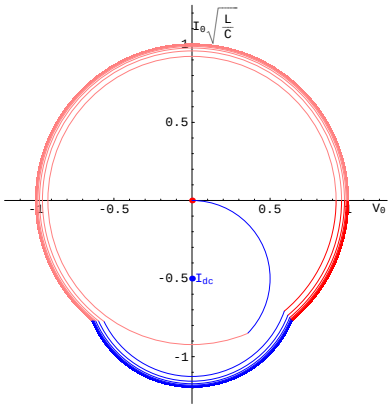
Figure 5.9 shows the regulation case in the phase plane with the noteworthy angles and lines marked in. The total energy in the resonant circuit is proportional to the distance from the origin. When the bouncer is operating in free motion (red line) the total energy, $W_L + W_C$, is always constant.



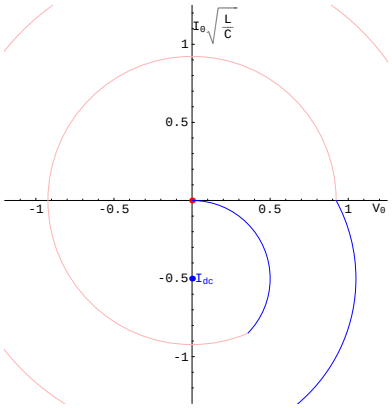
(a) natural, $I_{ratio} = 0.2$



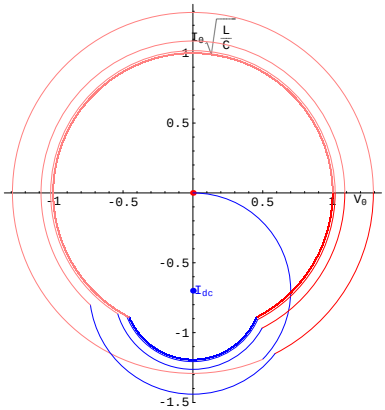
(b) forced, $I_{ratio} = 0.2$



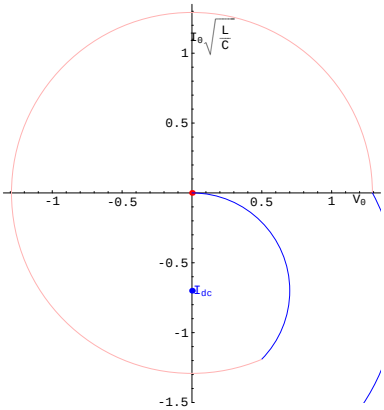
(c) natural, $I_{ratio} = 0.5$



(d) forced, $I_{ratio} = 0.5$



(e) natural, $I_{ratio} = 0.7$



(f) forced, $I_{ratio} = 0.7$

Figure 5.8: Bouncer transient analysis

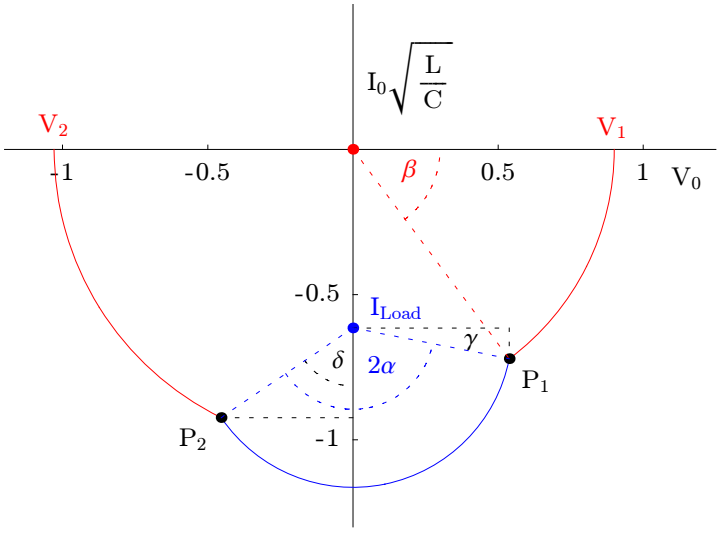


Figure 5.9: Error correction showed in the phaseplane

As the main pulse fires, the load current starts to flow through the bouncer (blue line) and the total energy changes. After the pulse has ended, the bouncer is again operating in free motion with constant energy. Hence the energy change in the bouncer can be found by considering the change in radius from P_1 to P_2 marked in Figure 5.9. Since all the bouncer energy will end up as voltage in the capacitor, the total energy is an expression of the end capacitor voltage. In the example shown in Figure 5.9, the bouncer starts off with a voltage of $0.9\,V_0$ and ends with a voltage just above V_0.

P_1 can easily be found by Equation 5.17. P_2 is derived from Equation 5.18-5.21 where R_2 denotes the radius of the blue arc shown in Figure 5.9. The angles α, β, γ and δ are shown in Figure 5.9.

$$\vec{P_1} = V_1\,[\cos\beta, -\sin\beta] \tag{5.17}$$

$$R_2 = \sqrt{{P_{1x}}^2 + (P_{1y} - I_{Load})^2} \tag{5.18}$$

$$\gamma = \arctan\frac{P_{1y} - I_{Load}}{P_{1x}} \tag{5.19}$$

$$\delta = \frac{\pi}{2} - 2\alpha - \gamma \tag{5.20}$$

$$\vec{P_2} = [R_2\,\sin\delta\,,\; R_2\; -\cos\delta - I_{Load}] \tag{5.21}$$

$$V2 = |\vec{P_2}| \tag{5.22}$$

It is desired to find a solution of Equation 5.22 on the form $\beta(\alpha, I_{Load}, V_1, V_2)$. It is possible to find an analytical solution for the equation, but solution showed to be to complex to be practical. Instead the equation should be linearized.

5.6 Bouncer Prototype

A full scale prototype of the bouncer is to be built for testing together with the prototype Klystron modulator. The initial goal is to keep the output voltage within the 1% criteria when the capacitor bank consists of two 106 μF capacitors in parallel. The pulse length is defined as 800 μs. To have some safety margin the bouncer requirements are calculated with a flat-top deviation of 0.8%. The α angel that defines the usable part of the voltage sine wave from the bouncer, is calculated according to Section 5.3.1, which gives 64°.

Next, the I_{ratio} must be determined. In principle it should be calculated from the inductor energy relationship to find the least energy demanding configuration. This relationship is shown in Figure 5.7. However, for the case of the prototype, it is desired with dimensions such that it can rely mostly on components in stock at CERN. It is found that with $I_{ratio} = 0.50$, the configuration coincides with available capacitors. No suitable inductors were found in stock and the inductor will therefore have to be custom made. This adds some degrees of freedom to the dimensioning process. It was decided to order an inductor that could work both with $I_{ratio} = 0.50$ and a more optimal value of $I_{ratio} = 0.61$. Values above 0.61 will bring the bouncer closer to the point where the bouncer may be overcharged on the first cycle and it was desired to avoid this with some safety margin.

The characteristic values for the two configurations are calculated by the Mathematica script shown in appendix E, and the two resulting configurations are listed in Table 5.1.

Par	$I_{ratio} = 0.50$	$I_{ratio} = 0.61$
C_B	220μF	500μF
$\hat{V}_C$	650 V	720 V
L_B	500μF	750μH
$\hat{I}_L$	500 A	400 A
t_d	300μs	300μs

Table 5.1: Bouncer prototype configuration

5.6.1 Simulation

A simulation was ran with the $I_{ratio} = 0.61$ configuration to confirm the parameters. Three different configurations were tried out as listed in Table 5.2. The basis for the simulation is shown in Figure 5.10. The parameters for the pulse transformer is based on data provided by the company from which the transformer has been ordered.

Simulation	Bouncer	Pulse transformer	Flat-top deviation
Sim1	YES	NO	0.82 %
Sim2	NO	YES	6.69 %
Sim3	YES	YES	0.62 %

Table 5.2: Simulation configurations

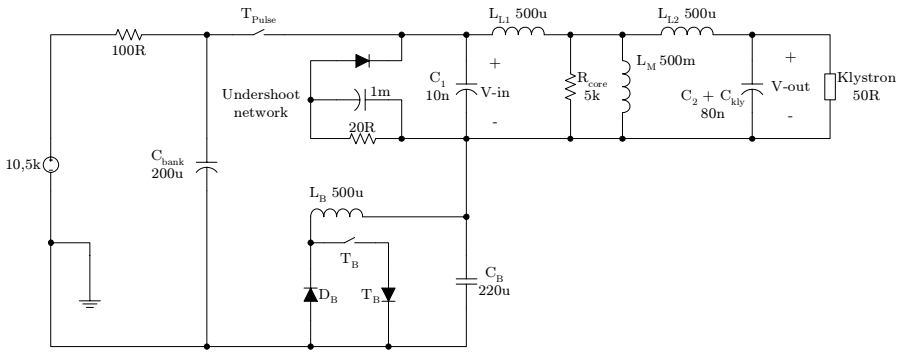


Figure 5.10: Simulation circuit

Figure 5.11 and 5.12 show the resulting waveforms from the simulations. *Sim1* is very close to the expectations from the theoretical analysis that showed a deviation of 0.80 %. The difference is believed to be caused by the linearization of the capacitor bank voltage droop.

In *Sim3* the pulse transformer is included in the circuit. It was not expected that the pulse transformer would improve the deviation. It is believed that this is caused by the increased rise time which results in less voltage-time load on the bouncer.

5.6.2 Assembly of Bouncer Prototype

The bouncer prototype was initially based on the $I_{ratio} = 0.50$ configuration, but prepared for a quick change to $I_{ratio} = 0.61$. The thyristor-diode stage is realized with old, heavily oversized, components that were available in stock. This is not expected to influence on the system in any significant degree. The exact components used, and their ratings, are listed in Table 5.3. The bouncer circuit is shown with all power components in Figure 5.13.

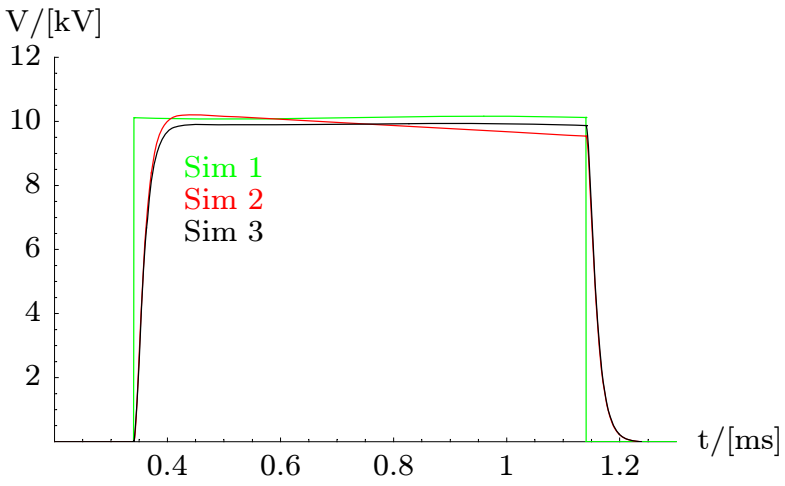


Figure 5.11: Simulations with bouncer

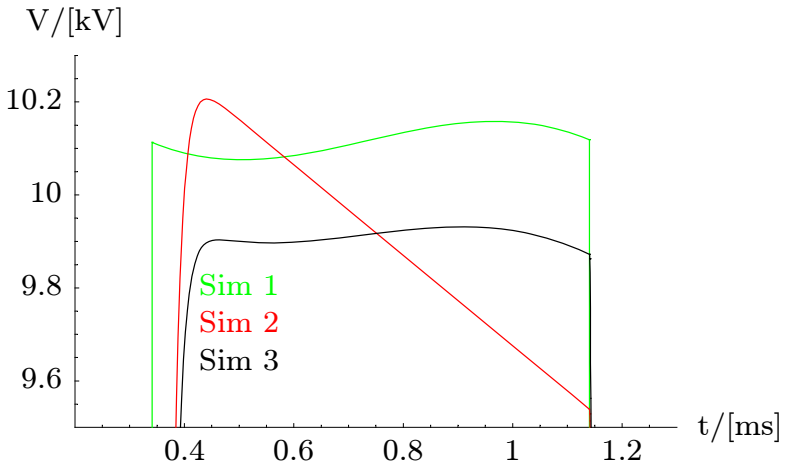


Figure 5.12: Simulation with bouncer - zoomed

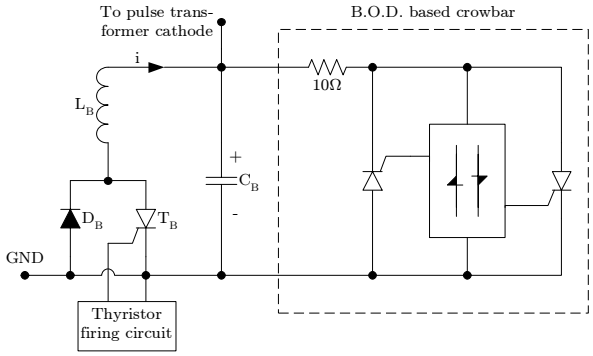


Figure 5.13: Bouncer protype circuit

Comp.	Brand/No	V	$\hat{V}$	I	$\hat{I}$
C_B	TPC/FFVI6A0227K	700 V	1.05 kV	100 A	∞
L_B	Tramo ETV	-	3 kV	35.3 A	500 A[1]
T_B	Westcode/N32-CH36	1.9 kV	3.6 kV	1.13 kA	14.3 kA[2]
D_B	AEI / DS912SM33	3.3 kV	3.7 kV	600A	3kA
T_{crowb}	Westcode/N32-CH36	1.9 kV	3.6 kV	1.13 kA	14.3 kA[2]

Table 5.3: Bouncer prototype components

As discussed in Section 5.4.1 and 5.4, any abnormal triggering of the bouncer thyristor can lead to excessive capacitor voltages. To protect the bouncer capacitor, a crowbar is included in the circuit, as showed in Figure 5.13. This crowbar is based on two thyristors connected in anti-parallel that are triggered directly by the capacitor voltage through a *Brake Over Diode* [3] (BOD) based network. The BOD network is a standardized configuration developed by CERN and is used in a large number of applications. The BOD network selected has a threshold voltage of 900 V. This provides sufficient protection for the capacitor while also allowing for good flexibility in the circuit.

Firing of the bouncer thyristor is achieved by feeding the thyristor gate with a low power pulse. Usually a pulse transformer is connected after the firing circuit to isolate it from the high voltage circuit. The firing circuit for the bouncer was based on a ready made pulse transformer board developed at CERN. The board has to be supplied with a 400 μs pulse on the input. It was desired to supply the pulse with a standard pulse generator. To achieve the required pulse power, an amplifying circuit had to be provided between the pulse generator and the pulse transformer. This was not available and had to be built separately. The amplifier was designed based on existing systems and is shown in Figure 5.14. The assembly was built on a veroboard that can be seen in Figure 5.15.

Figure 5.15 shows the complete and assembled bouncer.

5.6.3 Bouncer Test

To verify the assembly a test run was done with the prototype bouncer. The bouncer capacitor was charged to the specified initial voltage and the bouncer was fired in a stand-alone configuration without the load and power supply. The inductor current and capacitor voltage was measured with an oscilloscope. The results are shown in Figure 5.16.

[1] 500 A in 500 μH mode, 400 A in 750 μH mode

[2] 10 ms non-repetitive surge

[3] The brake over diode can be viewed as hybrid between a thyristor and a zenerdiode. The result is a self-trigged thyristor that triggers when the forward voltage exceeds the threshold level.

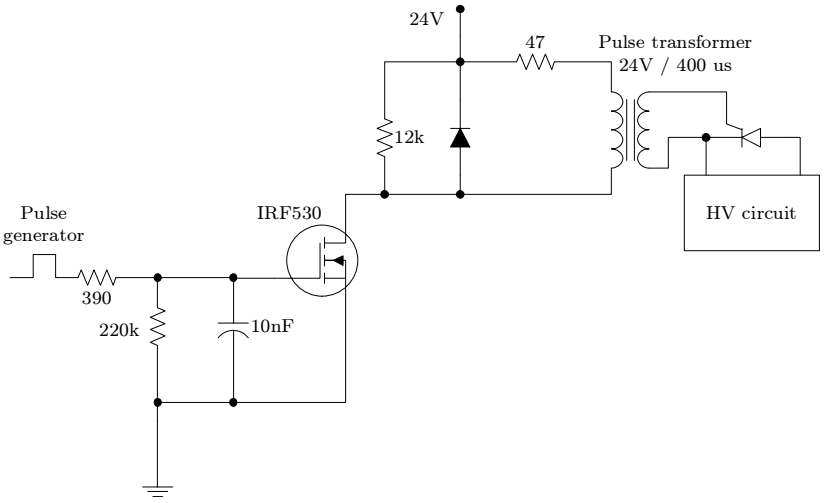


Figure 5.14: Firing circuit for bouncer thyristor

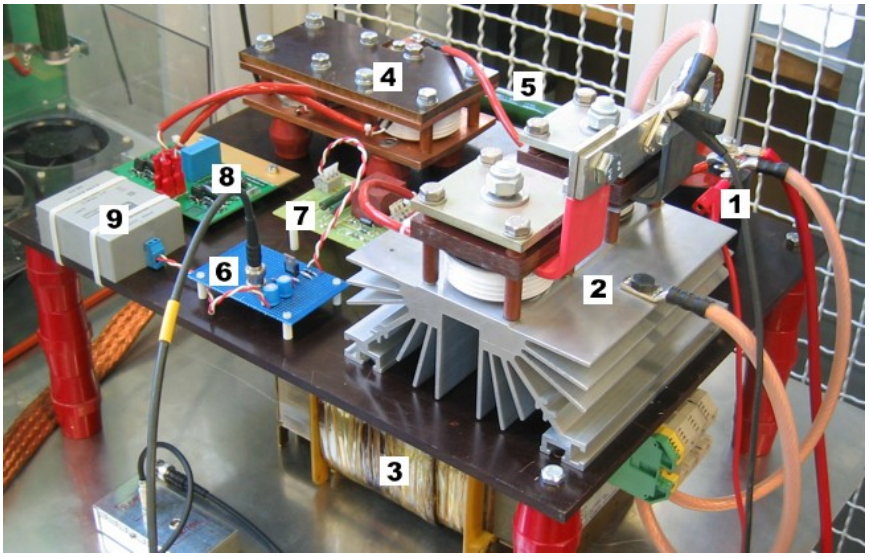


Figure 5.15: Bouncer prototype
(1) Capacitor C_B, (2) Thyristor/Diode assembly, (3) Inductor L_B, (4) Crowbar thyristors, (5) Crowbar resistor, (6) Firing pulse amplifier, (7) Firing pulse transformer, (8) BOD firing network, (9) 24V power supply

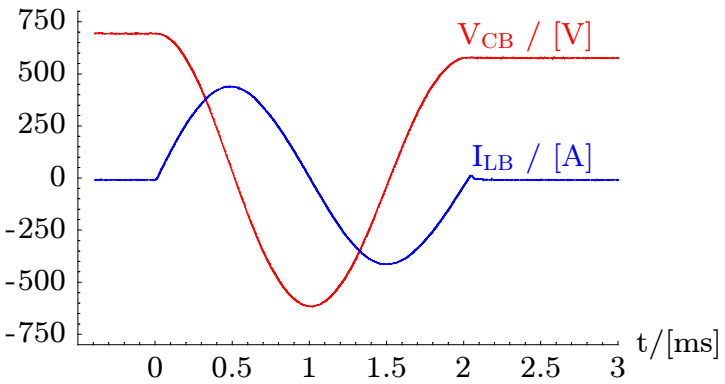


Figure 5.16: Test with prototype bouncer

As can be seen from the figure there is a voltage loss in the capacitor from the initial to the final voltage. This is caused by series resistance in the circuit and by the pn junction voltage over the thyristor and the diode. The voltage droop is larger than the calculated results and was measured to 118 V with an initial voltage of 700 V. The bouncer resistance was measured to 56 mΩ by DC-current measurement, below the 100 mΩ expected. However, the cable junctions and connections showed to have a significant resistance that had been neglected in the simulations.

For stable operaton, the initial voltage must equal the final voltage. The easiest way to compensate the loss is to reduce the bouncer time delay. However, this will also reduce the performance of the bouncer since the optimum area of the sinusoidal bouncer voltage will be shifted away from the output pulse. This performance loss can be compensated by oversizing the bouncer.

There is another possible solution to the problem. If a large resistor is placed in parallel with the switch, a leakage current will flow through the circuit and charge the capacitor. The resistor can be sized to compensate the capacitor loss. A parallel resistor will also help the problems with an open thyristor as discussed in Section 5.4.1. The charging process of the bouncer capacitor is given by Equation 5.23. Equation 5.23 gives the required time constant, and by inserting the repetition time constant for the output pulse (500 ms), the required parallel resistance can be found directly. In the equations V_s are the voltage in the capacitor bank and V_{C1} and V_{C2} are the initial and final bouncer capacitor voltages respectively.

$$V_{C2} = V_{C1} + (V_S - V_{C1}) \left(1 - e^{-\frac{t}{\tau}}\right) \tag{5.23}$$

$$\tau = -\frac{t}{\ln 1 - \frac{V_{C2} - V_{C1}}{V_S - V_{C1}}} \tag{5.24}$$

$$R = \frac{-\frac{T_{rep}}{\ln 1 - \frac{V_{C2}-V_{C1}}{V_S-V_{C1}}}}{C} \tag{5.25}$$

Since the bouncer capacitor holds a low voltage compared to the capacitor bank, the charging resistor will hold most of the voltage. Thus the efficiency of the charging will be low. A rough example based on the equations above suggest a charging resistor in the area of 200 kΩ. With a capacitor bank voltage at 10 kV this will result in a constant power loss of about 500 W. Depending on the application, this waste energy may be accepted. In the case of the Klystron modulator the loss could quickly become uneconomical since it is foreseen to have a total time in operation of several years. Hence, it is probably a better solution to oversize the bouncer accordingly.

5.7 Summary

The bouncer has been studied in detail and analyzed theoretically. Based on the analysis, a bouncer prototype was dimensioned and built. In Chapter 6 the bouncer prototype is included in the Klystron modulator setup for full system testing.

Chapter 6

Laboratory Setup

As a proof of concept, and as an initial test bench for the prototype components, a temporary lab setup was assembled with the single switch topology. The pulse transformer had not yet arrived in time for this setup so the configuration consisted only of the primary side components. A resistive dummy load was included as an equivalent for the Klystron and the pulse transformer. Since the undershoot network was expected to handle the inductive effects of the pulse transformer, no inductance was included in the load equivalent. The power circuit thus only consisted of the capacitor bank, the switch and the dummy load.

6.1 Assembly of High Voltage Lab

Due to the high number of development projects currently running at CERN, the availability of technicians was limited. The assembly and design of the lab setup was therefore done as a part of this thesis work.

6.1.1 Power Circuit

The power components used in the lab setup was mainly borrowed from the prototype that is under development, except for the safety discharger and the dummy load. In the following, the power components are described in detail.

Capacitor Charger

A *TECHNIX High Voltage Power Supply* rated 15 kV / 1000 mA is used as a capacitor charger. It can be controlled both on voltage and current, and has a dynamic response in the area of 50 ms. It is also internally EMC shielded so that noise inflicted on the high voltage side will not spread to the grid. The power supply was ordered specifically for the prototype, and will be remote controlled by the central controller. Fortunately the power

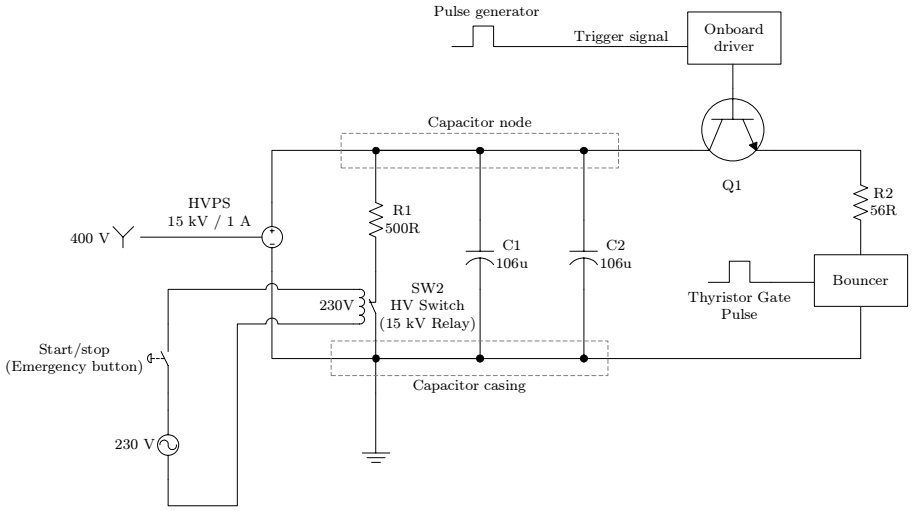


Figure 6.1: Lab setup

supply is also equipped with manual potentiometers that allow for direct control of the output. The charger can be seen to the right in Figure 6.2.

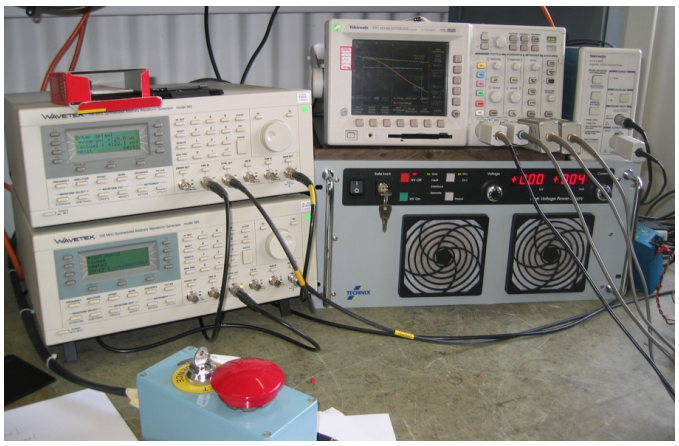


Figure 6.2: Input control
Left: Two pulse generators - Right: Capacitor charger and oscilloscope - Bottom: Emergency stop button

Capacitor Bank

The capacitor bank, shown in Figure 6.3, consists of two parallel connected 106 μF capacitors. The nominal DC voltage rating is 14.5 kV and the maximum allowed DC peak voltage is 21.75 kV. The capacitors are manufactured by APX and have model number DLIFMC1MF1066.

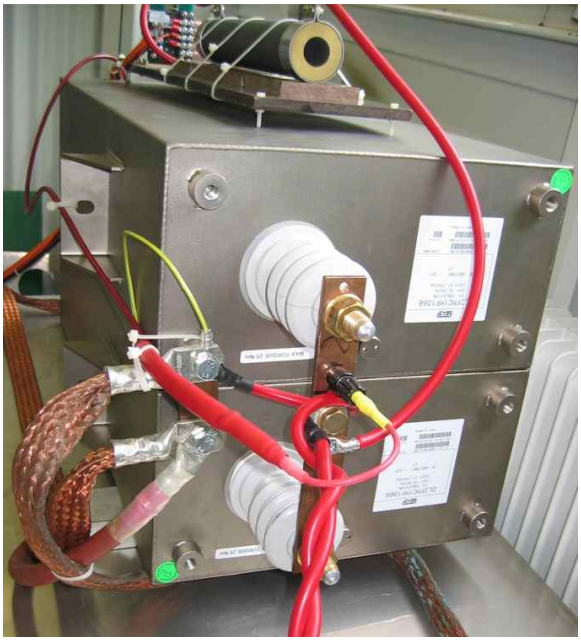


Figure 6.3: Capacitor bank

Safety Discharger

The safety discharge relay consists of a 500 Ω HV resistor in series with a 15 kV relay. The relay is controlled by a 230 V input and is of the type *normally-closed*. The time constant of the system is about 100 ms which ensures quick discharge of the system. The safety discharger is showed in Figure 6.4. The relay is also equipped with micro switches that monitor the operation. These are used to halt the power supply when the relay is closed.

Load Equivalent

Initially the load equivalent was based on high voltage resistors specifically ordered for the purpose. They where however not able to handle the pulse energy, and broke already at low voltage. As a substitute 5x 12 Ω resistors rated 700 W / 5 kV where ordered. 4 or 5 of these would provide a resistance of around 50 Ω with sufficient ratings. Unfortunately only 3 resistors were available for quick delivery. Instead 8x10 Ω rated 150 W / 2 kV where used in a serial/parallel connection to make up for the shortage. This adds up to a total resistance of 56 Ω.

Since the resistors will operate at around 5 kW, which is slightly above their power rating, a plexiglas duct with cooling fans was mounted around the resistors to blow the heat out of the closed lab setup. The resistors were mounted on a insulating plate that could handle high temperatures. The

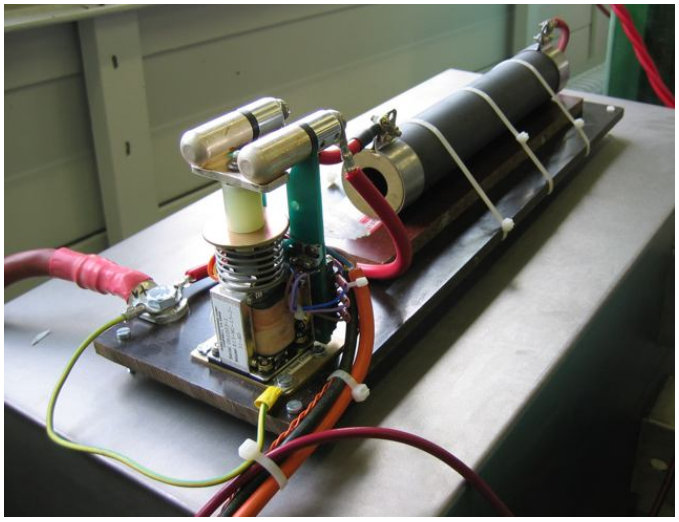


Figure 6.4: Safety discharge circuit

setup can be seen in Figure 6.6.

To allow for measurements of the output voltage with low voltage measurement equipment, a voltage divider was added in parallel with the last resistor stage of the dummy load. The total ratio of the voltage divider is 1:101.2. The complete resistor configuration is showed in Figure 6.5.

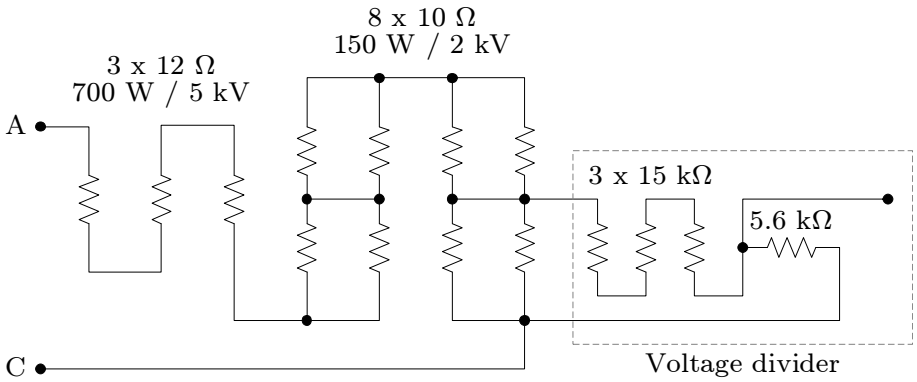


Figure 6.5: Load equivalent circuit

Switch

3 different switches are tested. These are the 4xIGCT switch, the 7xIGCT switch and the Behlke switch, described under their respective sections.

Figure 6.6: Resistor assembly

Pulse Generators

Advanced waveform generators are used to control the switch and the bouncer. The signals required are simple pulses, and normally it would be possible to generate such signals with a standard signal generator. However, the large difference between pulse-on time and pulse-off time places high accuracy requirements on the generator since they usually are digital and run on a single timer. The waveform generator Wavetek 395 that was available at CERN was found suitable for the job. The two pulse generators are shown in Figure 6.2.

The pulse generators are configured so that one controls the bouncer thyristor and the other controls the switch. The bouncer pulse generator operates in 2 Hz repetitive mode with a pulse width of 400 μs. The switch pulse generator is operated in single pulse mode and is configured with a time delay T_d and a pulse width T_{pulse}. It is set up so that it is triggered by the bouncer pulse generator. The triggering of the switch pulse generator is done with a separate signal from the bouncer pulse generator so that the switch can operated without operating the bouncer. With this configuration there is no redundancy in the system and the timer values can easily be adjusted. The control pulses are shown in Figure 6.7.

6.1.2 Safety Measures

The lab setup can operate up to 15 kV and must be designed so that all safety requirements are met for this voltage level.

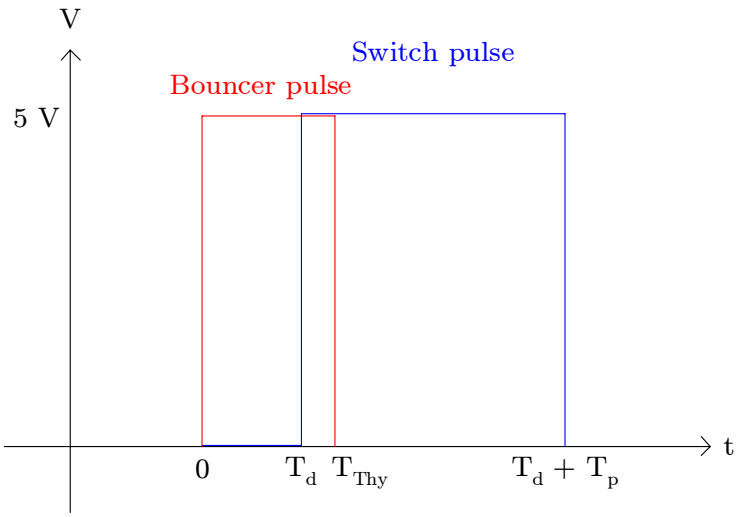


Figure 6.7: Control pulses

Figure 6.8: HV Lab setup

Ground Plane

The conducting ground plane is one of the most important safety measures. The whole lab area is placed on top of copper/aluminum plates which are connected directly to a safety ground loop located in the building. In case of an accident or a flash-over in the circuit, the ground plane reduces the risk of currents spreading outside the lab area.

Safety Discharger

The safety discharger is operated by the emergency stop button so that the capacitor can quickly be discharged. It only handles the capacitor bank. The other capacitors in the circuit may still hold voltage after the safety discharger has been engaged. This must be taken care of by other measures.

Safety Insulation

The configuration has to be made so that it is impossible for a person to reach any part on the high potential. This is achieved by shielding the whole lab setup in a plexiglas cage. The cage was built from large plexiglas plates which where cut into suitable pieces and mounted together with insulating nuts and bolts. The plexiglas used has a dielectric breakdown strength of about 30 kV/mm. The thickness of the plates is 4 mm and gives good protection from the 15 kV potential. The plexiglas cage also protects the lab personnel in case of an electrical explosion in the setup. The assembly can be seen in Figure 6.8.

Earth Rod

Two safety earth rods were included to allow for safety grounding of the high voltage components. All parts not directly connected to ground should be safety discharged with the safety rod as a step in the procedure of declaring the lab setup safe. The tip of the earth rods is directly connected to the earth plane. The rod it self is made of a insulated material and is approved for 45 kV.

Discharge Procedure

A discharge procedure for the setup was made and consists of the following steps:

1. Press the emergency button and ensure that the power supply interlocks, and that the capacitor bank voltage drops to zero.
2. Run the switch and the bouncer in 2 Hz repetitive mode for at least 10 sec to ensure complete discharge of the snubber capacitors and the bouncer capacitor.

3. Touch all the capacitors in the circuit with the earth rod.

4. Secure the earth rod on the capacitor bank to ensure that no voltage may enter the circuit.

When this procedure is fulfilled, the lab setup can be deemed safe.

Area Restriction

As further protection, an area of about 4 meter radius around the lab was sealed off to deny entry of persons not concerned with the experiment. The access through the fence was made such that it automatically shut down the HV circuit when opened. This area restriction is in accordance with French safety requirements for HV installations.

Visual Warning

A yellow warning sign was connected to the safety discharge relay so that it flashed when the discharge relay was open. This serves as a warning to both the personnel working in the lab and those outside.

Insulation Testing

The full circuit, except for the capacitor bank, was tested with a non-destructive insulation tester to ensure adequate insulation. The switch was tested up to its peak voltage while the other components in the system where tested up to the maximum rating of the tester at 30 kV.

6.2 ABB 4xIGCT Switch

During the lab setup assembly the switches ordered for the experiment had not yet arrived. To advance the test process, an old switch from a previous experiment was brought in. The tests with this switch were done with a qualitative approach to confirm the basic operation of the setup. No specific test procedure was followed.

6.2.1 The Switch

The ABB4 switch is configured much like the ABB7 switch described in Section 6.4 and will not be described in detail here. The ABB4 switch is rated as given in Table 6.1.

The switch is internally protected by both DRC snubbers and MOVs. The MOV assembly can be seen in front of the switch in Figure 6.9. The resistors and capacitors forming the snubbers can be seen on the left side of the switch. The upper snubber diode is also partly visible. On the left the

V_{nom}	6.0	kV
$\hat{V}$	8.5	kV
V_{MOV}	8.0	kV
I_{nom}	1.0	kA
$\hat{I}$	1.2	kA

Table 6.1: ABB 4xIGCT switch ratings

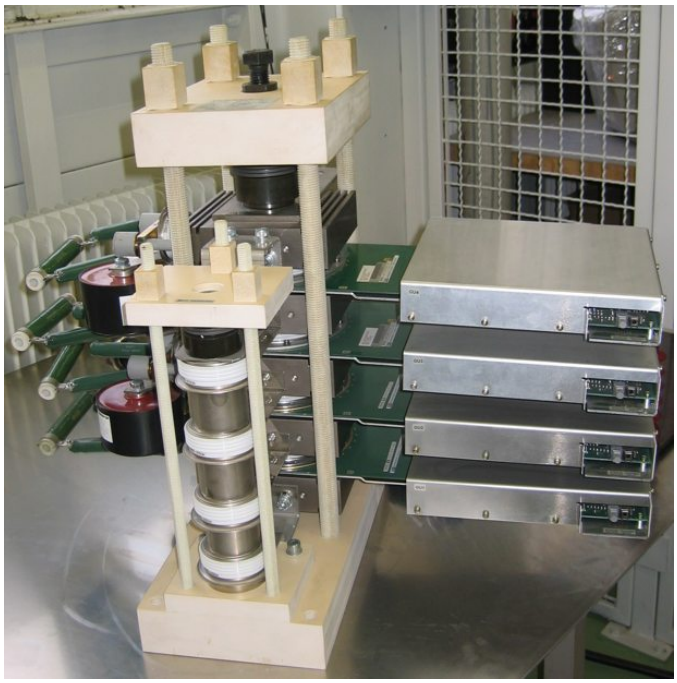


Figure 6.9: 4xIGCT ABB switch

IGCTs are visible in the center clamp of the switch. The drivers are located in the aluminum boxes to the right.

Unfortunately one of the power supplies for the drivers where broken so that one of the IGCT stages had to be bypassed. This reduced the voltage ratings of the switch by 25 %. The switch was therefore not brought above 5.5 kV. Most of the testing was performed at 5 kV.

6.2.2 Configuration

The tests were performed without the bouncer so that the power part of the circuit only consisted of the capacitor bank, the switch and the load. The wires to and from the load were twisted all the way from the capacitor bank to the load to reduce the stray inductance in the circuit. With this configuration the total inductance was believed to be within the handling

capabilities of the snubber.

6.2.3 Results

The testing started with trying out the performance of the safety discharger. The discharge resistor was of the same brand as the ones initially used in the load, and for unknown reasons it broke already when subjected to 1.5 kV. The load resistors managed 2.5 kV before they also broke. The resistors were replaced with a different brand as described in Section 6.1.1. The reason for failure was not investigated further, but is believed to be caused by the resistors not handling the high power of the pulse due to inadequate internal heat transfer. The pulse energy was well within the ratings of the resistors.

With the resistors replaced, the rest of the tests were successful. The system was run at 2 Hz repetitive mode with 800 μs pulse width up to 5.5 kV, showing the desired result. Different configurations were tried out for the measurement on the high voltage side. The most favorable solution was thought to be a set of 20 kV high voltage probes manufactured by Tektronix, but unfortunately they showed poor results in pulsed mode. A second solution that was tried was a 1 kV differential probe directly connected on the last resistor in the serial chain. During these initial tests the voltage divider described in section 6.1.1 was not yet implemented.

Figure 6.10 shows a result plot comparing the two measurement methods. Since the test is done without bouncer the voltage droop in the capacitor is visible on the output.

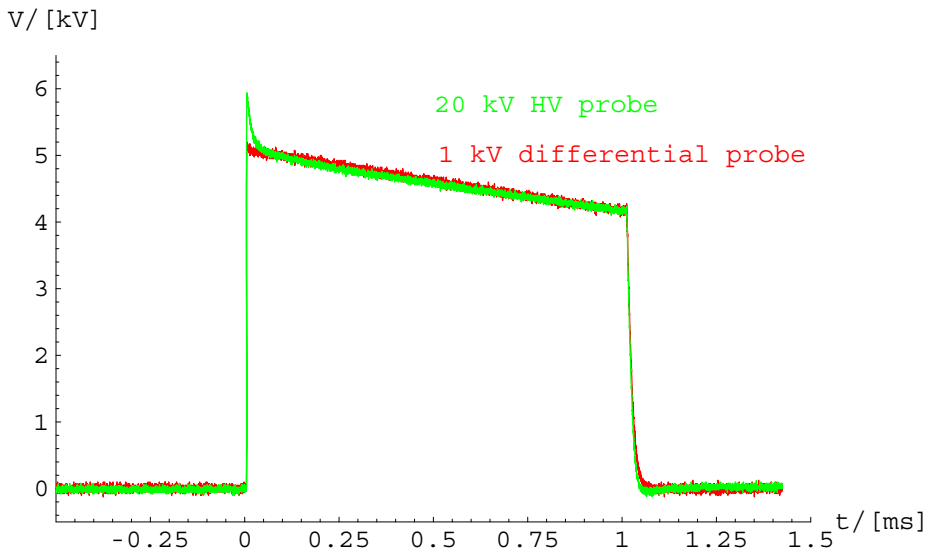


Figure 6.10: Comparison of probes

Since the operation of the HV probe was so poor it was desired to base further tests on the 1 kV differential probe. The differential probe can handle 1 kV between the terminals and a maximum of 1.3 kV between any of the terminals and ground. Since the bouncer may lift the low end of the load equivalent up to 900 V the load voltage must be scaled down so that the measurement voltage is kept within the 1.3 kV limit. This resulted in the voltage divider described in section 6.1.1.

6.3 Behlke Fast Transistor Switch

A German company named Behlke after the founder Frank Behlke, has specialized on producing high power switches based on low power transistors. The switches are made as large matrixes of serial and parallel connected transistors. Since the switch time of regular transistors are directly linked to the power rating, it is possible to achieve faster operation with low power transistors. In collaboration with Behlke, one of their switches was tested out in the lab.

6.3.1 Background

The availability of fully controllable switches above 10 kV is limited and is dominated by a few leading companies. This makes the market for these kinds of switches more like an oligopoly, and the price level is accordingly high. Also it is difficult to find suitable of-the-shelf switches in this voltage range, and the products often have to be tailor made with further increases in costs.

Since the Behlke switches are smaller, cheaper, and faster, and are supplied with numerous different ratings, it would be interesting to test them out.

The switch most suitable for our application is a 18 kV / 2 kA IGBT based switch. It has a switch-on time of 65 ns which is fast compared to other available switches in the same voltage range. The switch speed is handy in many military applications and can be used for military purposes. To avoid security issues, models that are made for export include a driver delay of at least 1 μs. This is also the case for the system used at CERN since it is foreseen that some of the future Klystron modulator development will be done in collaboration with non-European countries.

6.3.2 Configuration

Little is known about the specific design of the Behlke switch, except for that it consists of a large number of low power IGBTs. The switch and its driver is fully encapsulated. It is equipped with four connectors:

- HV Positive

- HV Negative
- Ground
- 4 pin Lemo connector with the following pins:
  1. Trigger signal (TTL, 3-5 V)
  2. Signal ground
  3. 5 V supply (<600 mA)
  4. Fault signal (5 V, low on fault)

The switch is not equipped with an internal snubber so this had to be provided externally. The snubber was designed as a compromise between the guidelines specified in Section 4.3 and the availability of components at CERN. The resistor was realized as a serial connection of 11x4.7 Ω resistors resulting in a total resistance of 51.7 Ω. The capacitor chosen was rated 250 nF. This led to a heavily oversized snubber and resulted in an unnecessarily high power loss. But given the slow switching frequency of 2 Hz, this is not of importance. The snubber was mounted as close to the terminals as possible to minimize the stray inductance. The snubber assembly can be seen in Figure 6.11. The capacitor is the white plastic box to the left. The large copper bars connected to the capacitor are used for safety discharging of the capacitor with the earth rod.

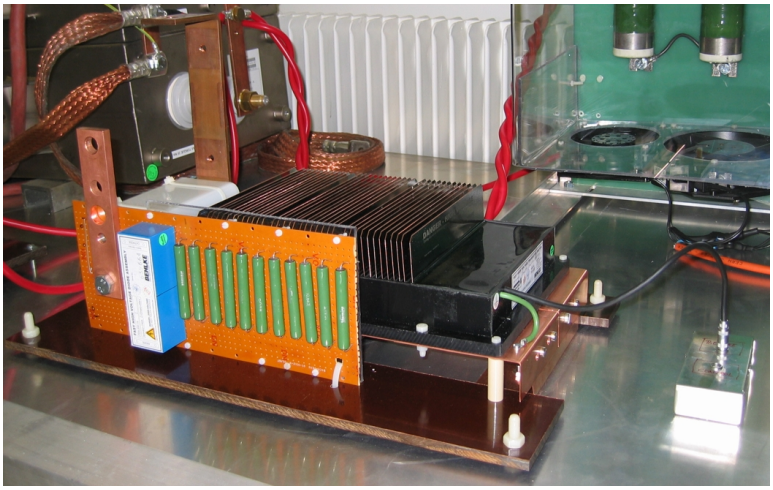


Figure 6.11: Behlke switch

6.3.3 Testing

The testing was based on the lab setup as described in Section 6.1, but without the bouncer. The test was supposed to be done in collaboration

with Behlke, but unfortunately they were not able to participate. There was little information available on the necessary precautions to be taken when assembling and operating the switch, so this was done in the best manageable way.

A plastic box with the interface connectors for the Behlke switch was assembled and connected in the circuit. The 5 V input was supplied by a stabilized DC supply suitable for the purpose.

The test was started by firing single pulses at low voltages. The operation looked good and the voltage was slowly increased. At about 5 kV the operation started to show problems. Sometimes when the pulse was fired the pulse was aborted after just a few microseconds. The problem was investigated by measuring the trigger signal at different points in the circuit. When measured close to the switch it could be seen that there was much interference on the signal from the power side of the system. Figure 6.12 shows the input trigger signal as measured on the switch input and the resulting output voltage. At t=0, about 1.5 μs after the trigger signal goes high, the switch closes. The interference from the switch-on violently distorts the trigger signal with voltages that exceed the input range by far. The voltage peaks showed in the graph are limited by clipping in the scope and is probably even higher than the 9 V indicated. It is believed that these oscillations either trigged the switch protection system or that the switch responded to the low voltage parts of the trigger voltage. In any case the noise led to early opening of the switch.

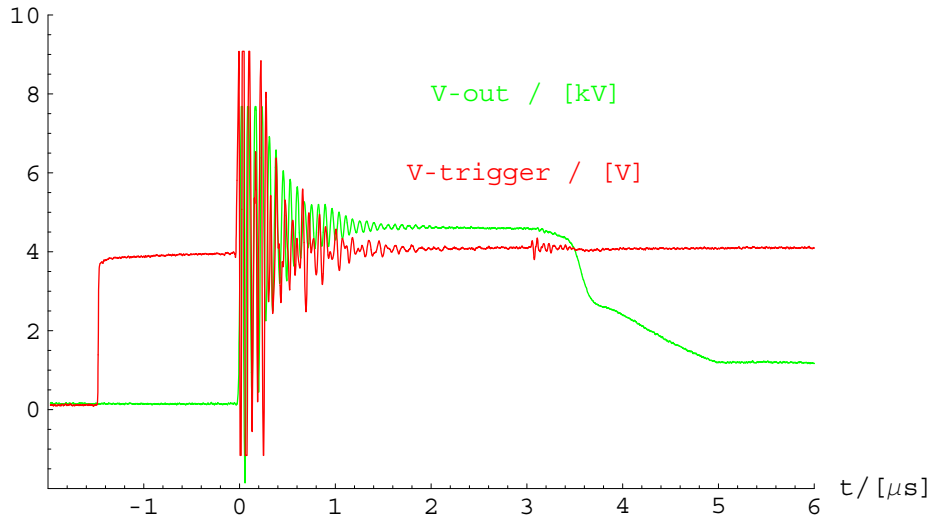


Figure 6.12: Trigger signal interference

The interference was thought to mainly be caused in the plastic box close to the switch. (this cannot be seen in Figure 6.11 since the picture is taken

from the improved setup described later) Inside the plastic box the trigger signal runs unshielded for a couple of centimeters from the input coaxial cable to the shielded output cable. Given that the plastic box is close to the high voltage circuit, and given the powerful electric field change that is caused by the high dv/dt (close to 200 kV/μs) this is probably the cause of the induced voltage in the trigger circuit. To help the problem, the plastic box was temporarily shielded with conductive copper tape. Also, the earth cable from the switch was shortened down from the initial configuration. This reduced the interference somewhat and allowed for steady operation of the switch up to 12 kV. However, the noise levels present in the system were still far above what could be accepted in a permanent solution.

The signal was carried from the pulse generator to the plastic interface box by single shielded coaxial cable. Since the shielding of the cable also is used as a return conductor, this may pick up noise and contribute to the interference.

The output pulse at full voltage is showed in Figure 6.13. Since the test was done without bouncer the capacitor voltage droop is directly visible on the output.

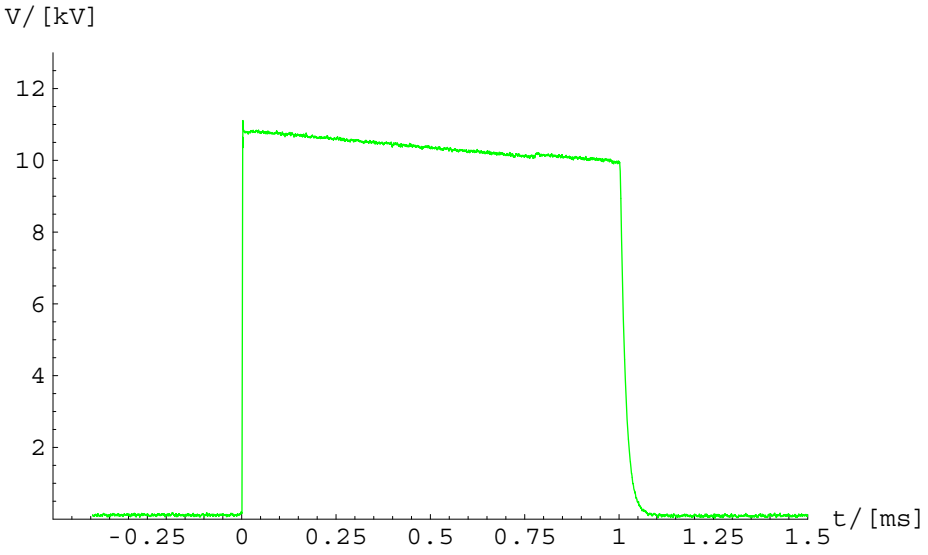


Figure 6.13: Behlke switch operating at full voltage

The switch was ran in 2 Hz repetitive mode at 12 kV for about 15 minutes. When the test was stopped the switch looked good, but for unknown reasons the switch failed to operate after this. It is possible that the noise induced in the trigger signal from the power stage destroyed the driver.

6.3.4 Improved Setup

To deal with the EMC problems in a more effective way the switch assembly was changed according to instructions given by Behlke. The plastic interface box was abandoned in favor of a fully shielded system. Also the coax cables were exchanged with shielded twisted pair cables. The trigger circuit was isolated from the shielding of the cable, and the cable shielding was connected to ground at both ends. Additionally an elevated ground plane made of copper plates was assembled under the switch to improve the earth connection. The new metal box and the elevated ground plane can be seen in Figure 6.11. The TP cable is not connected in this picture. The assembly was done with a new switch of the same type while the broken one was returned to Behlke for inspection. It was decided that further tests would have to be done with Behlke present. Representatives from Behlke were however not available to participate in the near term and the Behlke switch was postponed for now.

The Behlke switch is an interesting system, but due to the EMC issues and the fragility of the switch it was decided to wait with further testing with this system and proceed with the ABB switch.

6.4 ABB 7xIGCT Switch

The lab setup was changed to the new ABB7 switch upon arrival. The ABB7 switch is a serial stack of 7xIGCT's and is rated as specified in Table 6.4. Cosmic rays break down and reduce the performance of the solid state modules over time. To ensure a reliable system in the long run, the switch has to be heavily oversized. This causes the large difference between the peak ratings and the nominal ratings.

V_{nom}	12.0	kV
$\hat{V}$	31.5	kV
I_{nom}	300	A
$\hat{I}$	9	kA[1]

The driver boards and the driver power supplies for the IGCTs are on the same voltage potential as the corresponding IGCT. This gives some isolation issues since the driver and the power supply will float at full voltage when the switch is closed. The power supplies are therefore supplied through isolation transformers. The drivers are integrated in the switch and require no further preparations. The power supplies and the transformers on the other hand are large and bulky and have to be assembled in accordance with the potential issues. It is difficult to avoid a space demanding assembly, and

[1] Non-repetetive

as can be seen from Figure 6.14 the configuration is bulky. The installation was assembled by a CERN technician as a part of the prototype assembly described in Section 6.9.

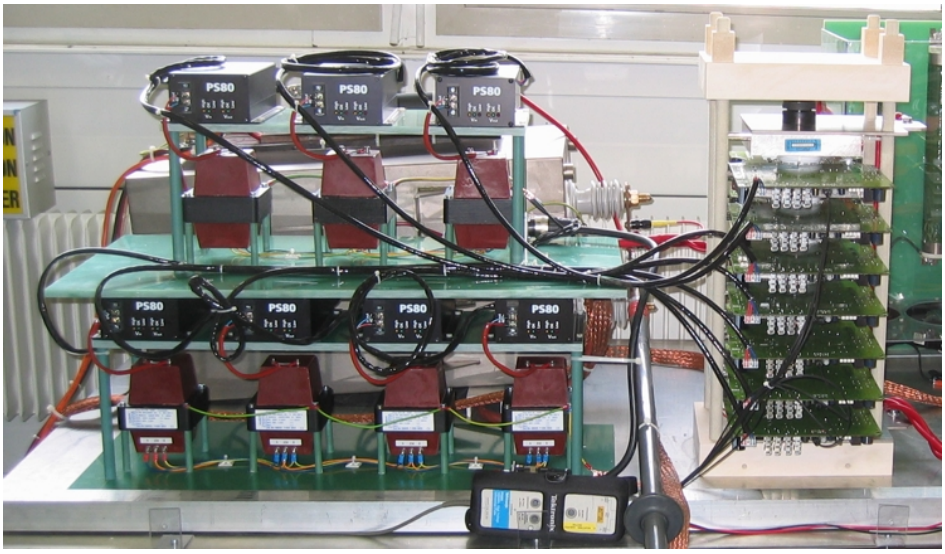


Figure 6.14: ABB 7xIGCT switch fully assembled

Figure 6.14 shows the full switch assembly with the transformer/power supply configuration to the left and the switch to the right. The black cables crisscrossing in the switch assembly are the power cables from the power supplies to the drivers. Tests with a high voltage insulation tester showed that the cable insulation was not sufficient to safely hold the full voltage. Heavy partial discharging was detected at 15 kV. This can lead to problems when the switch is open and the IGCTs are distributed on different potentials. To lessen the strain, the cables were arranged so that they are in the same order as the potential difference. Thus the strain on each cable cannot exceed the distributed voltage over the IGCTs, which is below 2 kV.

The switch is optically triggered to avoid insulation problems with the trigger signals. There is a separate optical fiber for each IGCT stage which triggers the IGCTs individually. The optical signals are provided by a divider that is triggered electrically and provides the seven optical signals. The optical fibers can be seen near the lower left corner of the switch in Figure 6.14. The use of optical signals also reduces the risk of EMC related problems since the electrical parts of the trigger system can be kept at a distance.

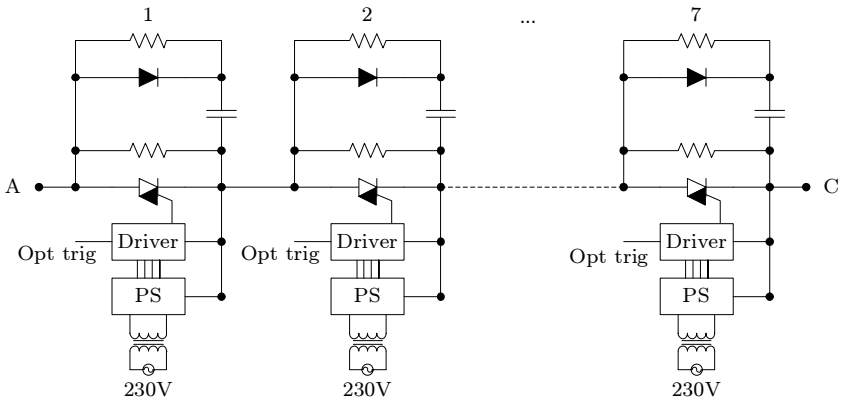


Figure 6.15: Sketch of ABB7

6.4.1 Snubbers

The switch is provided with powerful DRC snubbers equally distributed over the IGCT stages as shown in Figure 6.15. Also a set of balancing resistors are provided to ensure equally distributed voltage over the separate stages when the switch is off. This adds a leakage current of some milliamperes to the system when the switch is open. The leakage current is not important in respect to the power loss, but it will cause charging of the bouncer capacitor when the switch is open. During operation this is an advantage since it helps replenish the lost energy in the bouncer as described in Section 5.6.3. However, if the modulator is left idle for a longer period, the charging will lead to an over voltage in the bouncer that will fire the bouncer crowbar. Since it is foreseen that the modulator will be subjected to long idle periods, measures should be taken to avoid the problem. The simplest solution is to insert a parallel resistor in the bouncer that will carry a current equal to the leakage current at nominal voltage.

6.5 Commissioning

With the assembly of the ABB7 switch complete, the lab setup was ready for full system testing. To ensure correct assembly and operation, the testing was started with a commissioning where the system initially was ran on the lowest possible voltage. This should be non-destructive and allow for early detection of any failures or erroneous assembly. Next, the voltage was increased slowly towards rated voltage to verify the system. The commissioning with the full procedure and results are provided in Appendix B.1.1. The commissioning was successful and the lab setup was cleared for full scale testing.

6.6 Bouncer Optimizing

The first step for full system testing was to optimize the bouncer so that further testing could be based on one specific bouncer configuration. The bouncer must be tuned on three parameters; time delay, capacitor value and inductor value. A suggestion for the parameters was given by the calculations of Chapter 5. This part focuses on fine tuning of the parameters to compensate for practical deviation not accounted for in the theoretical analysis.

The bouncer inductor was designed for configuration 1 and 3 as specified in Table 6.6. A third test case based on maximum inductance and maximum capacitance was tested on request. This test case is referred to as configuration 2.

#	C_B/μF	L_B/μH	V_{rated}	$\hat{I}_{rated}$
1	220	500	700	500
2	220	750	700	400
3	150	750	700	400

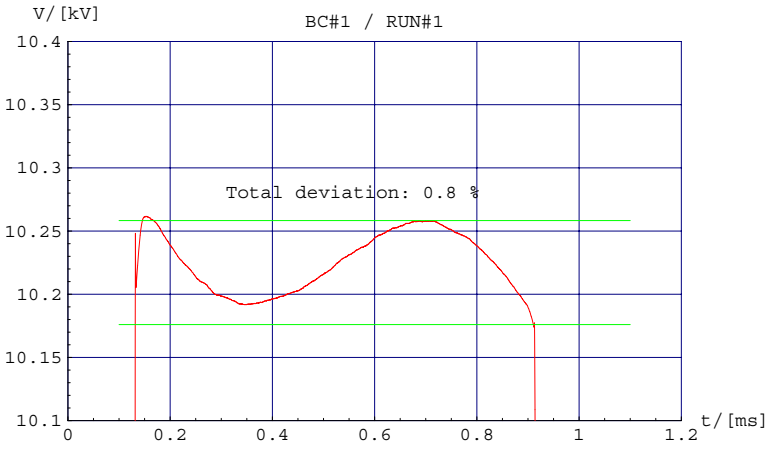
Table 6.2: Bouncer configurations

The bouncer optimizing was performed by running series of tests with varying time delays for the three different configurations. The complete test table and results are attached in appendix B.2. The time delays are restricted by the digital resolution of the waveform generators. This influenced on the selected time delays.

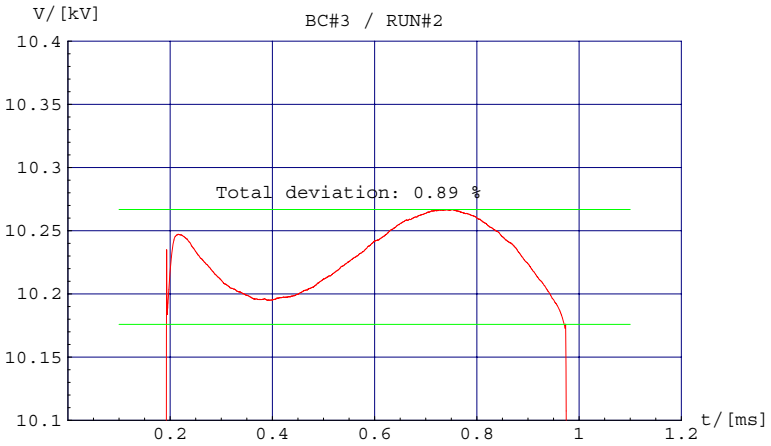
In general, configuration two showed poor results as expected due to inductor saturation. This is because the capacitor holds more energy than the rated energy for the inductor. Configuration 1 and 3 showed close to equal performance and the best results from these test runs are shown in Figure 6.16.

Configuration 1 ended up with slightly better performance than configuration 3. However, the bouncer is stretched to its maximum with the inductor operating slightly in saturation. The configuration has little room for maneuvering, and if the complete solution should require a higher voltage to compensate for pulse transformer droop it would be unable to comply. As can be seen from Figure 6.16(a) the end voltage is far below the start voltage, which means that the bouncer is not able to fully compensate the droop. If this is compared to configuration 3 given in Figure 6.16(b) it can be seen that this configuration has better compensating capabilities and is not yet at its full power. The full result sets are attached in Appendix 6.6.

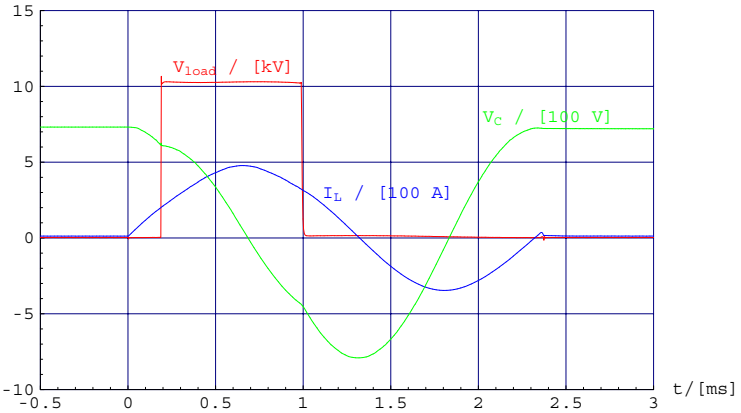
Note that the maximum point at the voltage wave in Figure 6.16(a) is not defined by the highest peak to the left, but by the second highest peak in the middle. This is because the pulse transformer is not expected to have



(a) Best case bouncer config 1



(b) Best case bouncer config 3



(c) Best case config 3 - Full results

Figure 6.16: Results from bouncer optimizing

reached the full output at this instant in the full configuration.

Based on this, bouncer configuration 3 with 170 μs delay time was decided to be the best setup.

6.7 Quantitative Testing

With the bouncer tuned in, a conclusive test run of the performance was carried through. The full results are attached in Appendix B.3. The final pulse is shown in Figure 6.17 with the flat-top deviation of 0.9 %

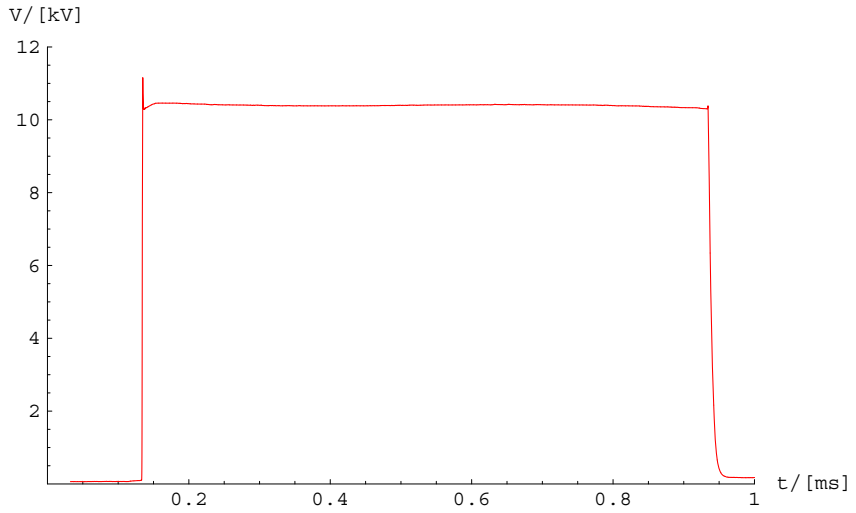


Figure 6.17: Full pulse

The rise time and fall time was measured to 0.41 μs and 9.6 μs respectively. This is calculated between the 10 % and the 90 % level. Especially the rise time is fast given the high ratings of the system. However, if the transients are measured from the point where the trigger signal is toggled, the result is quite different. The delay from the trigger edge to the execution of the change is about 5 μs. This is of little importance for the system in normal operation since it will not affect the lost transient energy. The delay can easily be compensated in the central trigger system.

However, if the switch is to quickly respond to an arc in the Klystron, the fall time becomes very important. A zoom on the falling edge is shown in Figure 6.18. It is difficult to predict exactly how the arc will behave during the transition from full arc voltage down to the low voltage level. The final arc voltage will typically be around 100 V, which results in low power. The leakage inductance of the pulse transformer is expected to be 100 mH referred to the secondary. If the arc voltage is neglected, this will result in a current rise of 1 A / μs. If one considers the example were it

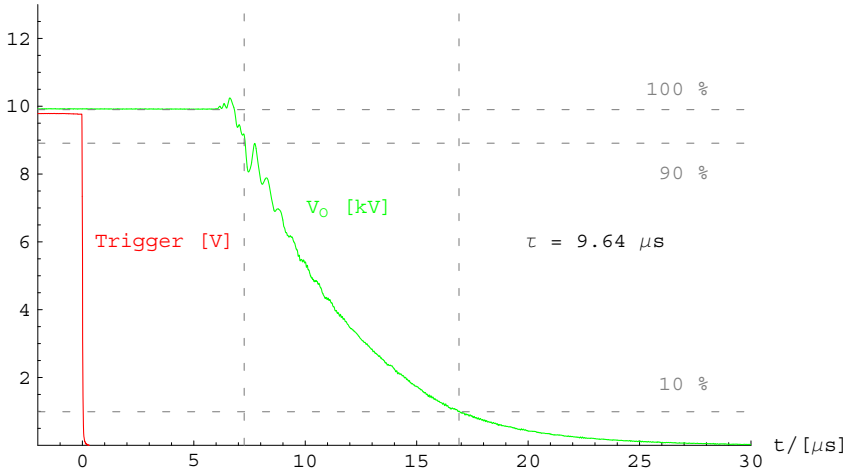


Figure 6.18: Falltime analysis

takes 50 μs from the arc fires until the switch is open, the average current will be 45 A and result in 4.5 kW of arc power. In this time frame it should be possible to protect the Klystron sufficiently. The fall time delay of the switch is therefore not critical.

It is important to notice that if the system fails to detect the arc and the switch is left closed, the load current could rise close to 1 kA. This would most certainly destroy the Klystron.

6.8 Measurements and Precision

The oscilloscope used in the tests has a resolution of 8 bits. This corresponds to 1/256 or 0.39%. Additionally, noise either in the measurements or the signal processing reduced the resolution with several multiples of the least significant bit. To achieve the desired measuring precision, it was necessary to take several steps to improve the signal quality. The oscilloscope is equipped with a hardware based averaging function that can improve the precision. Averaging is a powerful method of removing random noise. It is important to notice that the function will also remove non-periodic signals that are not coupled with the trigging of the scope. The only interest in the bouncer optimizing measurements is the fluctuating sinusoidal flat-top. This will be triggered equally for every sequence and the averaging function should be a good solution to improve the measurement. When averaging, the scope automatically increases the resolution to 10-12 bits depending on the number of averaged acquisitions. Figure 6.19 shows the effect of averaging with 128 acquisitions compared to the raw signal.

The horizontal resolution of the scope is very high with 10.000 measurement points provided for a single measurement and allows for post-

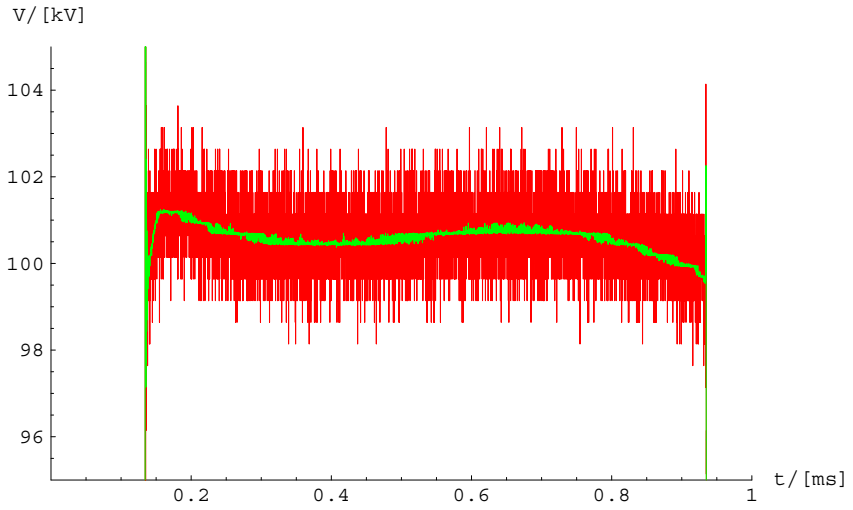


Figure 6.19: Effect of averaging

processing of the results. To further smooth the results to those shown in the results graphs *moving average* was used. The moving average calculation was performed as specified by Equation 6.1 - 6.3.

$$\vec{d} = [l_1, l_2, l_3, \cdots, d_i] \tag{6.1}$$

$$\vec{a} = [a_1, a_2, a_3, \cdots, a_i] \tag{6.2}$$

$$a_k = \frac{1}{s+1} \sum_{n=k}^{k+s} d_n \tag{6.3}$$

The dataset of results is denoted $\vec{d}$. A new vector containing the averaged results is denoted $\vec{a}$. The elements in vector $\vec{a}$ are given by Equation 6.3 where s is the number of samples contained in the moving average. $s = 200$ was found to give the desired results and was used in the bouncer optimization.

Based on these techniques it was possible to achieve precise results showing the exact flat-top fluctuation based on measurements with more than 2 % noise. However, it is important to note that these measurements cannot be conclusive in respect to the ripple requirements. If there existed high frequency ripple on the output this would have been filtered down by the averaging techniques. There is however no reason to expect such ripple since no non-linear operations occurs during the pulse.

6.9 Prototype

The CERN prototype that is to supply the first stage of the LINAC4 project has been developed in parallel with this thesis work. The development and assembly has been done by CERN engineers and technicians, except for the bouncer, which is based on this thesis work. The prototype is based on the lab setup components, including the pulse transformer to reach the full output voltage of 100 kV. It also includes the necessary interface components that are required to communicate with the control center and to receive status signals from the Klystron. Since the prototype was not finished in time for this thesis work, it will not be dealt with in detail. Some results from the commissioning are presented.

6.9.1 Power Circuit

The prototype is more complex than the lab setup circuit with protection circuitry, and measurement, and control parts. The active part of the power circuit however, is much like the lab setup, but including the pulse transformer as shown in Figure 6.20. The pulse transformer was manufactured by Stangenes, one of the very few suppliers of pulse transformers. It is rated -120 kV / 20 A / 800 μs.

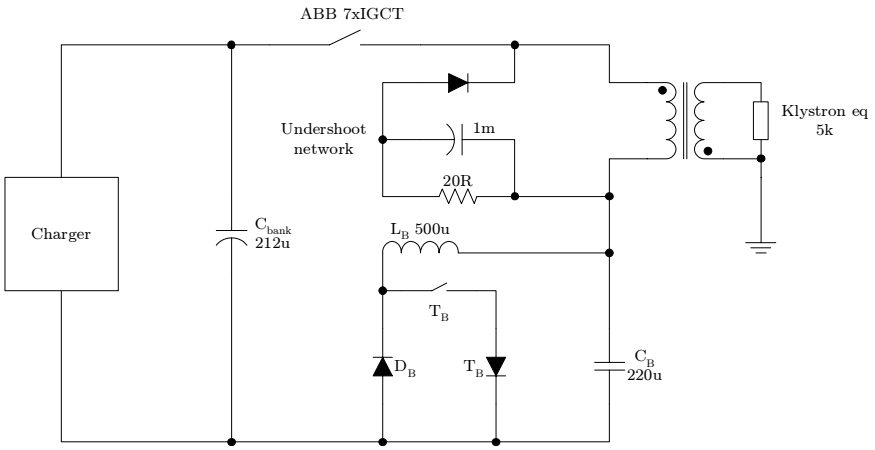


Figure 6.20: Prototype power circuit

6.9.2 Prototype Results

The initial commissioning of the prototype was done with the ABB 4xIGCT switch. This was done in the initial testing in case of a fatal error that could break the switch. However, this restricts the primary side voltage to 6 kV. During the finalization of this thesis work the prototype was still operating

with the ABB 4xIGCT switch. Results are therefore restricted to 57 kV. The flat top at 57 kV is shown in Figure 6.21.

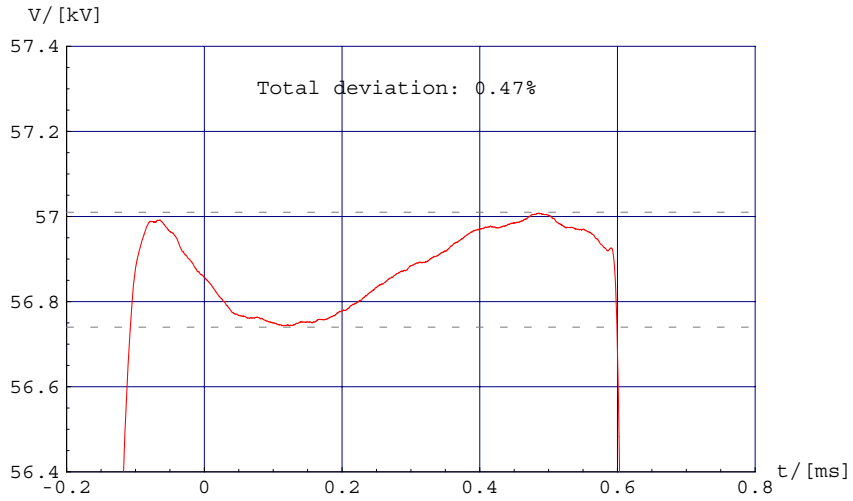


Figure 6.21: Prototype operation at 57 kV - Flat-top zoom

As can be seen from the figure, the voltage droop is well within the requirements. The bouncer is not operated at its full voltage, so some deterioration must be expected when the bouncer approaches saturation. However, the result shows slightly better performance than what was expected from the calculations. The test therefore confirm the simulation discussed in Section 5.6.1 on page 54. It can therefore be expected that the prototype will operate well within the requirements also at full voltage. This gives some safety margin in case of increased output voltage requirements due to voltage drops in the circuit.

6.10 Summary

Testing of the first stage of the Klystron modulator prototype has been performed by bringing the configuration up to its full voltage at 12 kV. The tests were successful and showed that the configuration was within the specifications. Also preliminary tests with the full prototype were performed and showed successful results. Full voltage testing with the prototype still remains.

Chapter 7

The Parallel Resonant Converter

The analysis of state of the art technologies in Chapter 3 indicated that the parallel resonant converter (PRC) looked like the most promising solution for future Klystron modulators. Features like flexibility in amplitude, pulse length and frequency, and the inherent short-circuit protection, makes the PRC interesting for further studies. In this chapter the PRC is studied in detail with both steady state analysis and dynamical analysis. The required frequency analysis to obtain a functional system is performed, and a specific configuration for the Klystron modulator is suggested. Finally a full simulation of a possible modulator is provided. The full system is thoroughly tested through simulations, both in normal operation and with arcing.

7.1 General Concept

The parallel resonant converter is usually configured like the circuit shown in Figure 7.1. As could be seen from the bode plot in Figure 3.20 on page 25, the resonant converter can both amplify and attenuate the output voltage. In theory there is no limit to the amplification, but since the transistor currents and the converter rise time increase with the amplification, there are practical limitations.

The PRC can be seen to be operating in three different modes, depending on the frequency: [13]

1. **Far below resonance**
   When operated far below the resonance frequency, the converter will operate in *discontinuous conduction mode* (DCM). During DCM the resonant capacitor voltage drops to zero for some time intervals. This causes the output rectifier to short circuit so that load is bypassed for the discontinuous intervals. DCM always occurs when $f_s < 0.5 f_0$,

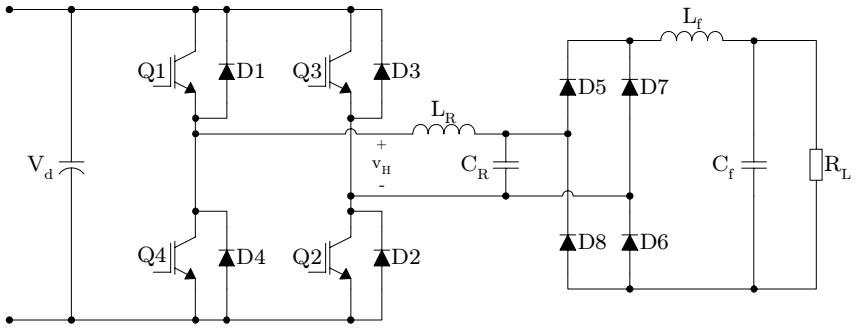


Figure 7.1: Typical DC/DC resonant converter

but may also occur close to resonant frequency due to heavy loading. Here, f_s is defined as the switching frequency while f_0 denotes the resonance frequency. The converter operates naturally with complete soft switching in DCM; however, no amplification is possible.

2. **Below resonance**
   When operated just below resonance, the PRC operates in *continuous conduction mode* (CCM). This allows for both amplification and attenuation, depending on the frequency. However, it is not possible to achieve complete soft switching.

3. **Above resonance**
   Above resonance the converter operates in CCM and can both amplify and attenuate. In normal operation the PRC cannot achieve complete soft switching. Nevertheless, with a specific configuration including loss-less snubbers it is possible to approach the complete soft switching condition.

To offer the required bandwidth the PRC has to operate at high frequencies. The switching loss will typically be the limiting factor when pushing for high switching frequencies. Depending on the pulse repetition rate, thermal cycling may add to the problem and reduce the transistor lifetime. It is therefore viewed as crucial to achieve complete soft switching for the Klystron modulator. Since it is also desired to utilize the amplification possibilities of the converter it is advantageous to operate above resonance. This is in accordance with other similar systems. [5], [8], [19].

7.1.1 Operating Voltage

The operating voltage for the converter must be seen in respect to the transistor switches that are to be used. The given power level for the converter suggests that high power IGBTs should be used. However, the time response impairs with increasing ratings, and it is important to keep the switching

time down to allow for high frequency operation. IGBTs with voltage ratings of 1700 V and below are significantly faster than those rated 3300 V and above. 1700 V IGBTs are therefore viewed as the best choice for the PRC. To have some safety margin the DC-link voltage should not exceed 1100 V with this configuration. With some capacitor voltage droop this adds to a required voltage amplification factor of about 100. It is difficult to achieve this order of amplification with the high power required with a single converter. A better approach is to use an output transformer with the PRC and connect several PRC converters in series in an inductive adder configuration. A configuration consisting of 5 modules is a suitable solution and allows for:

- Transformer step-up ratio around 10
- IGBT currents below 1 kA
- Low output ripple with interleaving of the modules

An extra module may also be included to add redundancy to the system. In this case the system can be very reliable.

When operating with several serial connected converters they should be interleaved to reduce the output ripple. When operating with interleaving the converter outputs are phase shifted as illustrated in Figure 7.2. This will reduce the output ripple with several tens of dB.

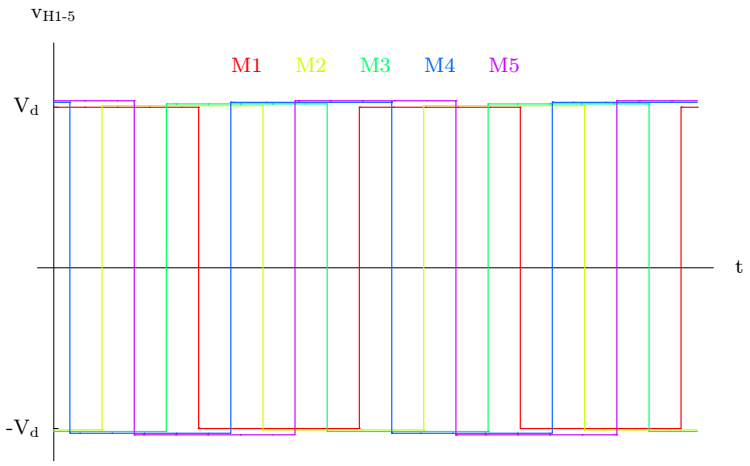


Figure 7.2: Interleaving of modules

7.2 Analysis of the PRC

If one consider the PRC given in Figure 7.1, and assumes the capacitor voltage V_d and the resulting load current I_0 to be constant through a switching

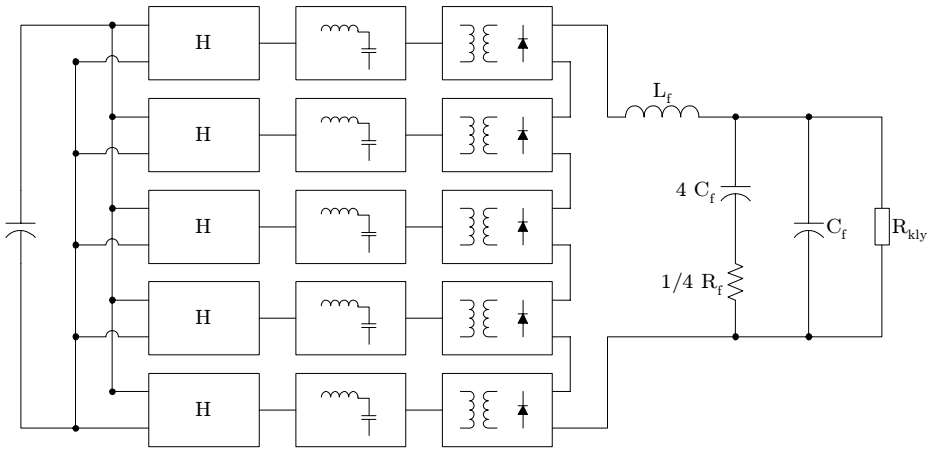


Figure 7.3: 5 stage PRC converter

cycle, the circuit can be simplified to the one given in Figure 7.4. Here the input voltage will switch between V_d and $-V_d$ due to the H-bridge switching. The H-bridge is assumed to operate with a duty cycle of 0.5 since this result in zero DC operation. Since the resonant capacitor will alternate between positive and negative voltages, the rectifier will commutate to result in a load current that alternates between I_O and $-I_O$. Hence, the converter will operate in 4 states as given in Table 7.1.

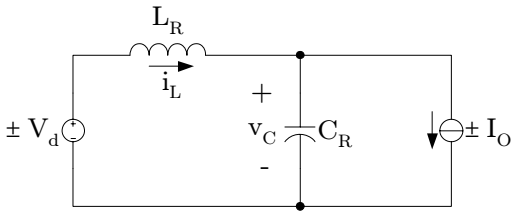
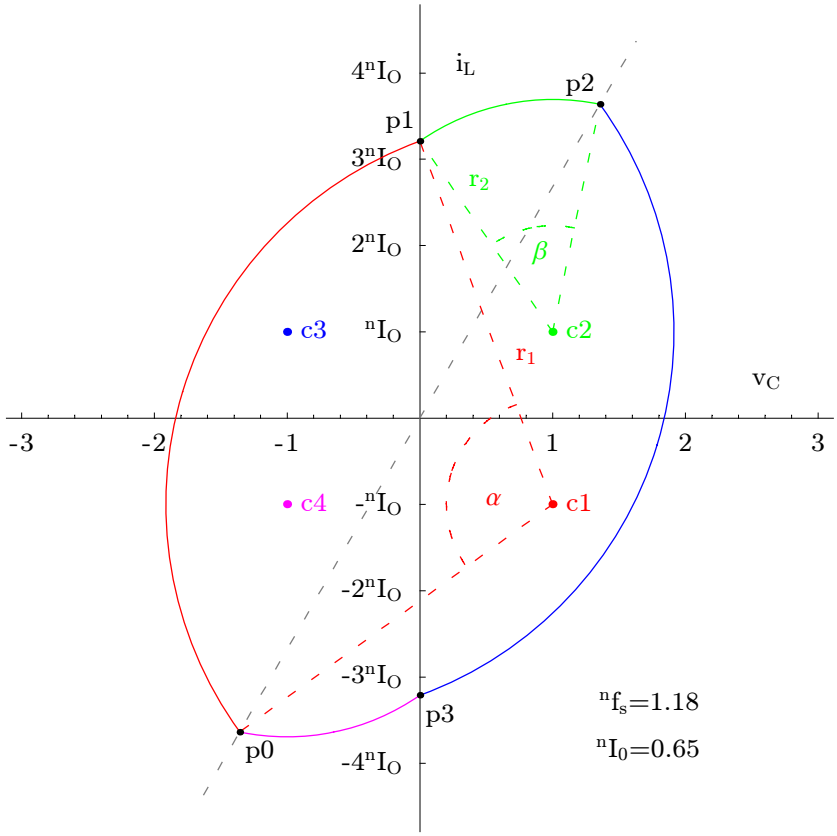


Figure 7.4: Simplified equivalent

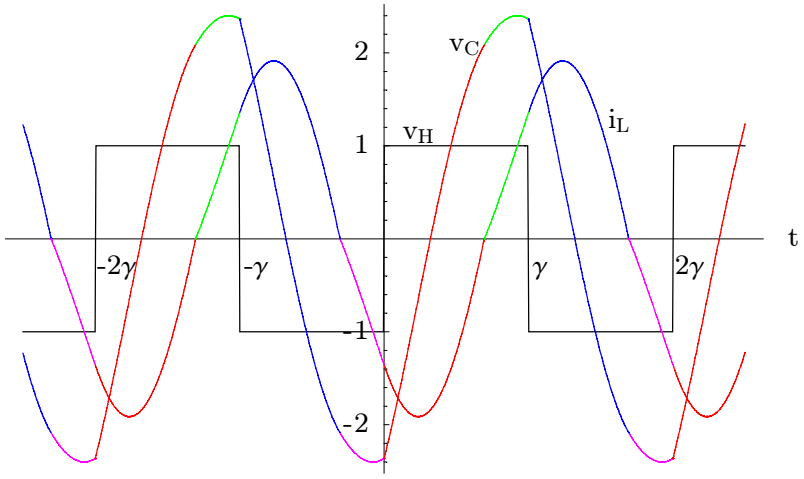
State	V_H	I_{Load}
c1	V_d	I_O
c2	V_d	$-I_O$
c3	$-V_d$	$-I_O$
c4	$-V_d$	I_O

Table 7.1: Resonant converter states

With this simplification, and by using phase plane analysis, the PRC operation can be derived analytically. The process described here is inspired by the work of R. Erickson as described in his book *Fundamentals of Power Electroncis* [13].



(a) Phase plane plot



(b) Time plot

Figure 7.5: Resonant converter operating in CCM

If one considers the phase plane analysis given in Figure 7.5(a) it can be seen that, to operate in steady state, the converter must operate in a closed loop where the end point equals the start point (p0). If the converter operates with zero DC voltage and current, which is the desired case when operating with a transformer on the output, the negative voltage cycle will be symmetrical to the positive voltage cycle. This is indicated by the diagonal dashed line in the figure. The angles α and β given in the figure is defined as the H-bridge diode conduction angle and the H-bridge transistor conduction angle respectively. As given in Equation 7.1, γ is defined as the angle of a half cycle. The angles given in the phase plane is proportional to time as given by Equation 7.2. Deductible from this is that when the converter is operating at resonant frequency, $\gamma = \pi$. Above resonant frequency $\gamma < \pi$ and below $\gamma > \pi$.

$$\gamma = \alpha + \beta \tag{7.1}$$

$$t_{angle} = angle \cdot \omega_0 \tag{7.2}$$

When considering the output voltage it can be seen that this is positive in the second and third period of the cycle. If the filter is considered ideal, the output voltage V_O will equal the average resonant capacitor voltage ${}^*V_C$ over one half period. The notation ${}^*V_x$ refers to the average voltage over one half period starting in point 1 and ending in point 3 as specified in Figure 7.5(a). V_H denotes the H-bridge output voltage.

$$V_O = {}^*V_C = \frac{1}{t_\gamma} \int_{t_\alpha}^{t_\alpha + t_\gamma} v_C(t)\ dt \tag{7.3}$$

$${}^*V_L = \frac{1}{t_\gamma} \int_{t_\alpha}^{t_\alpha + t_\gamma} v_L(t)\ dt \tag{7.4}$$

$${}^*V_H = \frac{1}{t_\gamma} \int_{t_\alpha}^{t_\alpha + t_\gamma} v_H(t)\ dt\ = V_d \left(\frac{\beta - \alpha}{\omega_0} \right) \frac{1}{t_\gamma} \tag{7.5}$$

By applying Kirchhoff's voltage law in integral form, one can find an expression based on the averaged voltages as shown in Equation 7.6.

$$V_O = {}^*V_C = {}^*V_H - {}^*V_L \tag{7.6}$$

As can be seen from the phase plane, the inductor end current does not equal the initial current. The average inductor voltage will therefore be non-zero and is defined as given by Equation 7.7. Note that the magnitude of the end current equals the initial current.

$${}^*V_L = \frac{1}{t_\gamma} 2 I_{L1} L \tag{7.7}$$

Substitution of Equation 7.7 and 7.5 into Equation 7.6 yields Equation 7.8:

$$V_O = \frac{1}{t_\gamma}\left(V_d\frac{\beta-\alpha}{\omega_0} + 2I_{L1}L\right) \tag{7.8}$$

It is easier to understand the operation of the PRC when one considers the load parameters in respect to the resonant circuit parameters. This is achieved when working with normalized parameters. Normalized values are denoted equally to their respective scaled values, but with a super-scripted n in front, as indicated by Equation 7.9. The normalization parameters are defined by Equations 7.10 - 7.14.

$${}^nV_x = \frac{V_x}{V_{basis}} \tag{7.9}$$

$$V_{basis} = V_d \tag{7.10}$$

$$I_{basis} = I_O \tag{7.11}$$

$$f_{basis} = \frac{1}{2\pi\omega_0} \tag{7.12}$$

$$R_0 = \frac{1}{\sqrt{L/C}} \tag{7.13}$$

$$\omega_0 = \frac{1}{\sqrt{LC}} \tag{7.14}$$

$$\phi = \frac{\beta-\alpha}{2} \tag{7.15}$$

Normalization of Equation 7.8 yields Equation 7.16.

$$\frac{{}^nV_O\gamma}{2} = \phi + {}^nI_{L1} \tag{7.16}$$

By geometrical analysis of the phase plane, the closed form solution of the system can be found. Equation 7.17 defines the relationship between the load current and output voltage for different frequencies. It can be seen from the phase plane that ϕ has to be positive below resonance and negative above resonance. At resonance $\phi = 0$. When ϕ is known, the conditions p0 and p1 shown in the phase plane can be found by Equations 7.18 - 7.20. The subscripts 0 and 1 refers to the condition in point 0 and 1 in the phase plane.

$$\cos(\pm\phi) = \cos\frac{\gamma}{2} + {}^nI_O\,\sin\frac{\gamma}{2} \tag{7.17}$$

$$^{n}I_{L1} = -\frac{\sin\varphi}{\cos\frac{\gamma}{2}} \tag{7.18}$$

$$^{n}I_{L0} = -\left(^{n}I_{O}^{2} - 1\right)\tan\frac{\gamma}{2} \tag{7.19}$$

$$^{n}V_{C0} = -\frac{^{n}I_{O}\sin\varphi}{\cos\frac{\gamma}{2}} \tag{7.20}$$

By substituting Equation 7.18 into Equation 7.16 the closed form solution for the output voltage is found:

$$^{n}V_{O} = \left(\frac{2}{\gamma}\right)\left(\phi - \frac{\sin\phi}{\cos\frac{\gamma}{2}}\right) \tag{7.21}$$

By solving Equation 7.17 in respect to $^{n}I_{O}$ and plotting this parametrically together with Equation 7.21, the different load conditions can be visualized. The resulting plot is shown in Figure 7.6. It is only valid for the continuous conduction mode shown with black lines. The red lines indicate the boundary CCM and DCM.

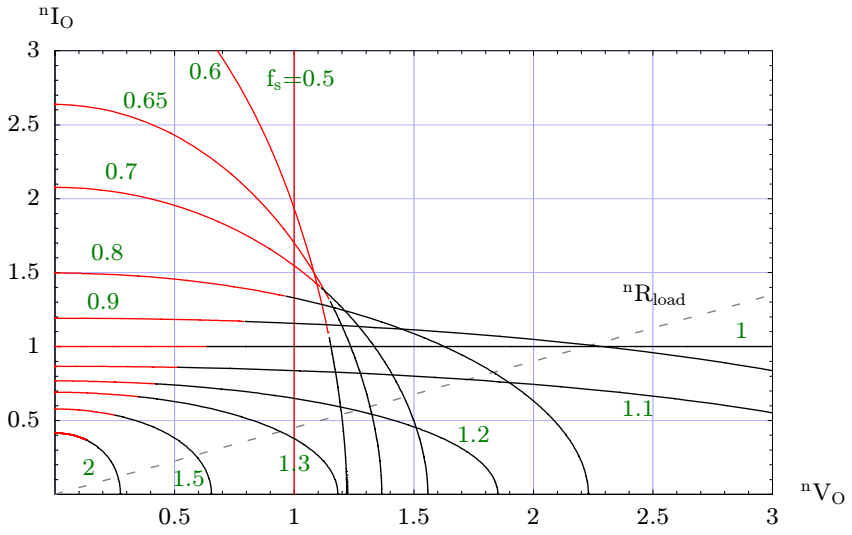


Figure 7.6: Operation characteristics of the PRC

For the Klystron modulator it is desired to operate with high output voltages. As can be seen from the example load line given in Figure 7.6, the output voltage gets more sensitive to frequency changes as one moves into the high amplification area to the right.

To find the required switching frequency for a given load condition, ϕ in Equation 7.21 can be substituted with Equation 7.17 to form Equation 7.22. However, the equation proved to be difficult to solve analytically. Instead

a simple Newton-Raphson iterative algorithm was used instead as shown in Equation 7.23.

$$ {}^{n}V_O = \frac{2\left(\sec\frac{\gamma}{2}\sqrt{1-\left(\cos\frac{\gamma}{2}+{}^{n}I_O\sin\frac{\gamma}{2}\right)^2}-\arccos\cos\frac{\gamma}{2}+{}^{n}I_O\sin\frac{\gamma}{2}\right)}{\gamma} \tag{7.22} $$

$$ \gamma_1 = \gamma_0 - \frac{{}^{n}V_O(\gamma_0)}{{}^{n}V_O{}'(\gamma_0)} \tag{7.23} $$

Based on these equations the operation point for the resonant converter can be calculated. Note that a normalization point for the load current has to be selected for the system. This gives some freedom in the system design and is discussed in the next section.

7.3 Converter Design

The requirements for the PRC, and its corresponding chosen parameters, are listed in Table 7.2. Initially it was desired to operate the converter with an amplification factor of 3 so that the transformer ratio could be scaled down below 10. Also it was desired to operate the converter at 20 kHz. However, simulations of the system indicated that this configuration would be too slow and thus not be suitable for a pulse modulator.

Number of modules	5	
Input voltage, V_D	1.1	kV
Max capacitor bank voltage droop	10	%
Max resonant amplification	2	
Max switching frequency, f_s	40	kHz
Required output voltage, $5\,V_O$	100	kV
Required output current, I_O	20	A
Load resistance	5	kΩ
Transformer step-up ratio, n	10	

Table 7.2: PRC configuration

The PRC has been chosen to operate above resonant frequency based on the principle discussed in Section 7.1. As a part of the design, the normalized load current ${}^{n}I_O$ has to be selected. As can be seen from Figure 7.6, ${}^{n}I_O$ is restricted to be below 1 when operating above resonance. The peak inductor current is inversely linked to ${}^{n}I_O$, so that to keep the peak current down ${}^{n}I_O$ should be selected as high as possible. However, as discussed earlier, the sensitivity to frequency increases as ${}^{n}I_O$ approaches unity, and there must be a compromise between these. In addition to this, some safety margin

must be added to allow for deviations from in the resonant circuit. Three values for ${}^nI_O$ have been tried out, 0.6, 0.75, 0.9. The results are shown in Table 7.3. The voltage amplification as seen from the converter will not be constant due to the capacitor bank voltage droop. Based on the specification the normalized start voltage is 1.8, while the end voltage is 2.

	V_d [kV]	${}^nV_O$	${}^nI_O$	${}^nf_s$	f_s [kHz]	$\hat{I_L}$ [A]	$\hat{V_C}$ [kV]
1_{high}	1.1	1.8	0.60	1.145	40.00	665	3.16
1_{low}	0.99	2.0	0.60	1.133	39.59	726	3.15
2_{high}	1.1	1.8	0.75	1.106	40.00	647	3.20
2_{low}	0.99	2.0	0.75	1.098	39.73	707	3.18
3_{high}	1.1	1.8	0.90	1.052	40.00	630	3.23
3_{low}	0.99	2.0	0.90	1.049	39.90	688	3.21

Table 7.3: Design results for three different cases

When evaluating the strain on the transistor switches, the inductor current is what counts since the inductor current always flows through the H-bridge. The capacitor voltage on the other hand is of little importance since the H-bridge never will be subjected to voltages above V_d. To minimize the transistor currents, ${}^nI_O = 0.9$ is selected.

When ${}^nI_O$ and ${}^nf_s$ are known, the converter components are easy to size by Equations 7.23-7.27.

$$R_0 = {}^nI_O \frac{V_{d-low}}{I_O} \tag{7.24}$$

$$f_0 = \frac{f_{s-max}}{{}^nf_{s-max}} \tag{7.25}$$

$$L = \frac{R_0}{2\pi f_0} \tag{7.26}$$

$$C = \frac{1}{2\pi f_0 R_0} \tag{7.27}$$

The qualtiy factor (Q-factor) for the resonant circuit is given by Equation 7.28.

$$Q = \frac{R_L}{n^2\, R_0} \tag{7.28}$$

7.3.1 Phase Control

So far the resonant converter has only been discussed in respect to frequency control. It is also possible to control the converter by altering the phase shift between the H-bridge legs while running at a constant frequency. The result

of a phase shift is that the typical square wave output also includes a portion of zero voltage. By adjusting the amount of zero voltage, the converter can be controlled in amplitude. The phase shift is defined in Figure 7.7. An example of the total H-bridge output when operated with a phase shift can be seen in Figure 7.17(a).

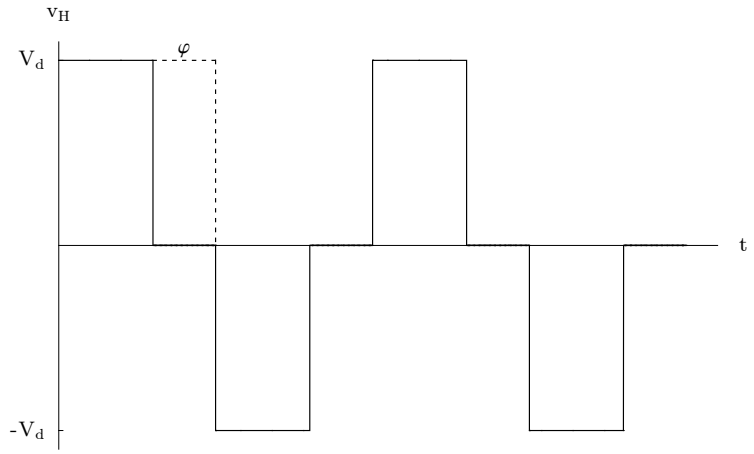


Figure 7.7: H-brigde output voltage with phase shift control

The fundamental of the H-bridge voltage can be calculated by Fourier analysis as shown in Equation 7.29. When operated at resonant frequency the output waveforms will be purely sinusoidal and the output voltage can simply be calculated by multiplying the fundamental input voltage with the amplification factor of the resonant stage. Phase control at resonant frequency is thus an easy approach to control the resonant converter.

$$h_1 = \frac{4}{\pi} \int_{\varphi/2}^{\pi/2} V_d \sin(\omega t)\ d(\omega t) = \frac{4}{\pi} \cos\left(\frac{\varphi}{2}\right) \tag{7.29}$$

When the H-bridge is operated with phase shifts, the response of the two legs is no longer symmetrical. The legs are usually distinguished by denoting them as the *leading leg* and the *lagging leg*. The leading leg is the leg that receives the control signal first. The lagging leg receives the same control signal after a delay angle φ has passed.

7.3.2 Soft Switching

Soft switching is achieved when the transistors are switching with either zero current or zero voltage across the transistor. The two cases are referred to as *zero voltage switching* (ZVS) and *zero current switching* (ZCS). The switching loss in a soft switching transistor will be close to zero.

In frequency controlled operation above resonance, both legs of the H-bridge will undergo zero current switching at turn-on. This can be seen from

the phase plane plot in Figure 7.5(a). The transistor current starting in p1 and p3 starts due to commutation in the output rectifier when the transistor is already open. However, both legs undergo hard switches during turn-off as can be seen in p0 and p2.

In the case where the resonant converter is operated at resonant frequency with phase shift control the situation changes somewhat. The leading leg undergoes hard turn-off whilst the lagging leg undergoes hard turn-on. Thus soft switching is still lost for all devices. [22]

However, if one operate with a combination of frequency control and phase shift control it is possible to move closer to complete soft switching. The phase shift between the fundamental of the H-bridge voltage v_H and the inductor current i_L is defined as ψ. If the H-bridge is operated with a phase shift φ so that $\varphi = \psi/2$, the lagging leg will achieve ZCS during turn-off.

The leading leg will still undergo hard turn-off. But since the output current is negative during turn-on, the switch current cannot start to flow until the switch voltage is brought up to zero and the diode blocks. This allows for inserting a loss-less snubber consisting only of a capacitor over the leading leg transistors. During the turn-off the capacitor will keep the voltage close to zero so that ZVS is achieved. This mode of operation can be seen in Figure 7.17 on page 106. The capacitor must be sized so that the transistor voltage is kept sufficiently low during the turn-off transition. On the same time it must not be larger than that it manages to discharge completely before turn-on. A capacitor value of 800 nF was experimentally found to work well.

To ensure that soft switching is achieved in a practical configuration with the expected irregularities, the turn-off should not rely on the calculated phase-shift, but should be executed by measuring the zero crossing of the inductor current. Since the inductor current is close to sinusoidal it should be possible to make this measurement without noise or distortion problems.

The turn-on at the leading leg must be controlled so that the opening is delayed after the capacitor discharge. Since the inductor current is running negative at this point the timing of this delay is not critical as long as the transistor is not opened with voltage present in the snubber capacitor. The safest way to control the delay is by measuring the capacitor voltage.

7.3.3 Filtering

The high frequency ripple tolerance of the Klystron modulator is 0.1 % and demands for heavy filtering. A calculation with ideal sinusoidal waveforms of a 5 stage resonant converter without filter shows a ripple of 5 % at 400 kHz frequency, as shown in Figure 7.8. The ripple frequency equals the switching frequency times the number of phase shifted modules times 2. The last factor is caused by the rectification.

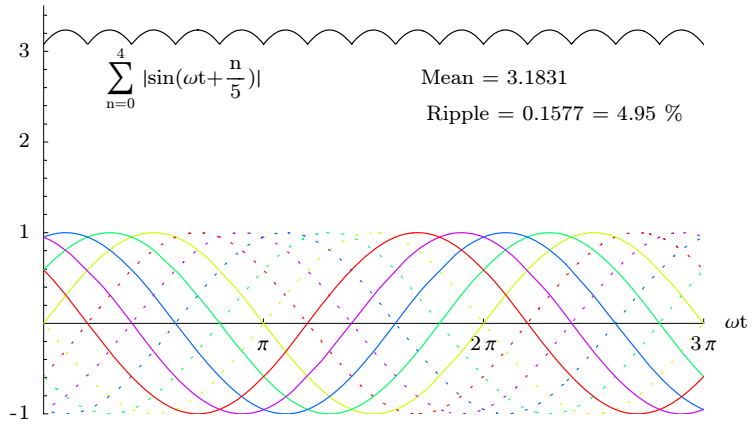


Figure 7.8: Ideal output voltage

The ripple calcualtion was confirmed by a full system simulation.

To have a safety margin it is desired to filter down the ripple to at least 0.05 %. This requires a ripple attenuation of 100 times or 40 dB. Thus the filter must attenuate at least 40 dB at 400 kHz frequency. In the same time the filter must also allow for sufficient bandwidth. In normal PWM converter design the cut off frequency of the filter can be sized to meet the desired bandwidth. The bandwidth may also be improved slightly beyond the bandwidth of the filter by active feedback compensation. The converter is usually so fast that it can be considered ideal in this case.

The resonant converter on the other hand is quite slow, and the converter itself is the most limiting factor in the system. The converter can therefore only be relied on for active damping to a limited degree. A second order filter can ideally achieve 40 dB attenuation per decade, which means that the cut-off frequency could be placed somewhere just below 40 kHz. Simulations indicate that a PRC with the specified design has a bandwidth closer to 4 kHz. It is therefore a good solution to design a filter with much higher bandwidth than the converter, and make it rely on passive damping. The filter can then be taken out of the equation when designing the control.

A standard second order filter that is widely used in power converters is shown in Figure 7.9. Since the four damped capacitor legs are connected in parallel they can be equated to one leg.

Since the filter is consisting of both a damped and an undamped part the analysis is not straight forward. As a starting point the damping resistance was set to zero and the corresponding undamped system was dimensioned with a resonance frequency of 30 kHz. The relationship between the inductor and capacitor value was chosen so that the stored amount of energy at DC conditions was equally distributed. Not surprisingly the filter showed a poor frequency response with high resonance. Further tuning of the filter

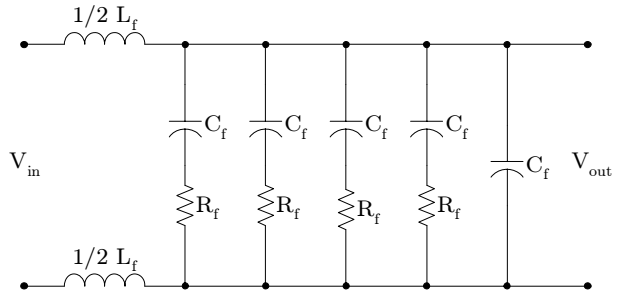


Figure 7.9: 2 order output filter

was done by simulations in MathCAD. Table 7.4 shows the final values that showed the desired performance. The full frequency analysis with bode plots is attached in Appendix C.

L_f	20	mH
C_f	1	nF
R_f	60	kΩ

Table 7.4: Final filter values

For simplicity the full system simulation is based on a single filter placed on the output. In a practical setup it may be preferable to distribute the filter over the PRC modules to improve the modularity. This can be done without changing the performance and will also reduce the required voltage ratings for the filter components.

7.3.4 Control Analysis

As a part of the control analysis, the dynamical properties of the converter have to be found. The analytical approach to this showed to be beyond the scope for thesis. Instead the dynamics were found empirically through simulations.

A 5 stage PRC converter with 2x amplification and 40 kHz switching frequency showed a natural step-response with a time constant of about 40 μs. The transient waveform showed a close fit to the first order exponential function on form $C\left(1-e^{-\frac{t}{\tau}}\right)$. The Laplace transformation of this function gives the one pole transfer function given in Equation 7.30.

$$h_v(s) = \frac{1}{1+T_1 s} \tag{7.30}$$

Given the simple one-pole converter dynamics, the basic PI controller shown in Figure 7.10 will probably be sufficient.

$$h_u(s) = K_p \frac{1 + T_i s}{T_i s} \tag{7.31}$$

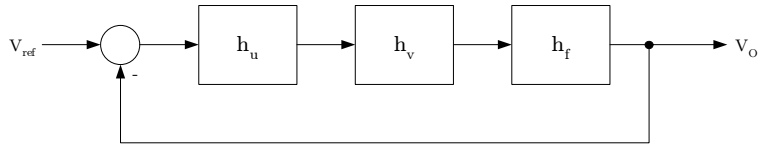


Figure 7.10: Converter with PI-regulator

The integral time was chosen to equal the converter time constant since this gives the best compensation for a single pole system.

Initially the K_p was sized on the basis of frequency analysis after the standard stability criteria. The full frequency analysis with bode plots is attached in appendix C.

Since the frequency response was based on a simplification of the system, the final tuning had to be done with full system simulations. It was aimed for an overshoot that stayed just within the 1 % criteria.

In the final simulation this was achieved with $T_i = 40\mu s$ and $K_p = 1$.

7.4 Simulation design

With the converter and the regulator fully designed a full simulation was developed. The simulation was done in *Saber*, which is a powerful simulation tool for mixed signal analysis. Power converters operate with a combination of analog and digital signals which is demanding for most simulator software. The simulation was ran on one of the available computer clusters at CERN.

7.4.1 PRC power circuit

The simulation is based on the third case in Table 7.3. The corresponding specified parameters are given in Table 7.5.

The simulation was configured as a 5 stage serial connected system as shown in Figure 7.3. The modules share the same capacitor bank and output filter as shown in the figure. Each module is configured as shown in Figure 7.11. Some of the simulations were based on a slightly different rectifier bridge configuration, but this did not affect the results.

7.4.2 IGBT Controller

It was desired to make an IGBT controller interface that could handle both variable frequency and variable phase shift simultaneously. Also the interface must handle the interleaving of the modules so that the output is distributed as shown in Figure 7.8. This showed to be complicated since

Parameter	Symbol	Value	
Number of modules		5	
Capacitor bank	C_{bank}	20	mF
Initial capacitor bank voltage	V_{d1}	1.1	kV
Characteristic resistance	R_0	4.455	
Resonance frequency	f_0	38.023	kHz
Resonance inductor	L_R	18.65	μH
Resonance capacitor	C_R	940	nF
Transformer turn ratio	n	10	
Filter inductor	L_f	20	mH
Filter capacitance	C_f	1	nF
Filter resistance	R_f	60	kΩ

Table 7.5: PRC simulation dimensions

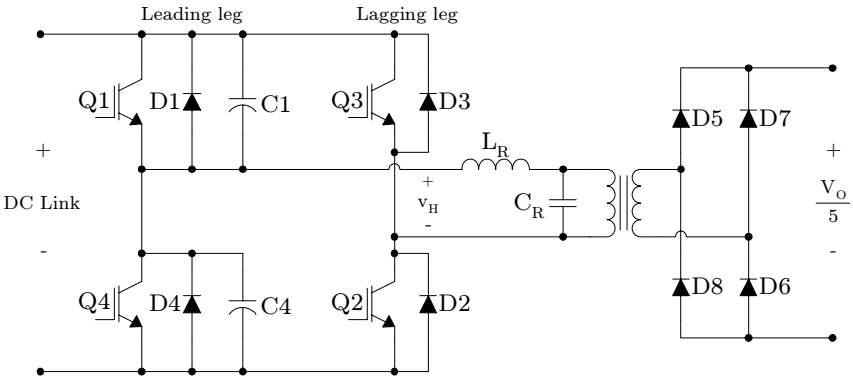


Figure 7.11: Simulated power circuit module

the timing of both phase shifts are frequency dependent. The problems were overcome and the solution finally decided on was based on a series of integrators where the reference frequency is integrated by time. As the integrator reaches a given threshold level specified by the phase shift, the trigger signal is given. The integrators operate at double frequency so that the same integrator can provide both on and off signals. A feedback connected SR-latch on the output allows for the on and off signals to be transformed into the desired square waves.

The block diagram for the IGBT driver is shown in Appendix D. Since the process is completely analog, except from the latching output, the response time is short and allows for immediate changes. Frequency changes that are performed during a switch period will influence on the current switch period and will be completely executed on the next switching period. The IGBT controller is demonstrated in Figure 7.12. Sinusoidal signals are subjected on the frequency and phase input as shown in the lower part. The upper part shows the resulting control signals for the 10 IGBT legs. The two IGBTs in each leg are driven by the same signal, but with inverted responses. Also a dead time generator was included to avoid short circuiting the H-bridge.

7.4.3 Regulator Interface

The regulator output is given in the interval 0-1. Since the IGBT controller requires leveled signals for phase and frequency, the regulator output must be converted. As an initial approach the frequency was directly linearized so that 1 gave the resonant frequency and 0 gave 45 kHz. The phase was calculated directly from the frequency signal by Equation 7.32 [22].

$$\psi = \arctan\left[QF\left(F^2 + \frac{1}{Q^2} - 1\right)\right] \tag{7.32}$$

$$\varphi = \frac{10}{\pi}\psi \tag{7.33}$$

The feedback measurement of the regulator is scaled down so that 100 kV gives unity. When the pulse ends, the regulator is bypassed and the IGBTs directly switched off. The voltage reference, V_{ref} is therefore always set to unity.

7.4.4 Module Balancing

It was quickly discovered during the simulations that the 5 modules where not operating in perfect unity as expected. There were slight differences in output voltage between the modules which lead to sub-harmonic ripple on the output. When one consider the initial conditions for the modules, it is not surprising that differences occur. Upon initial startup the first module

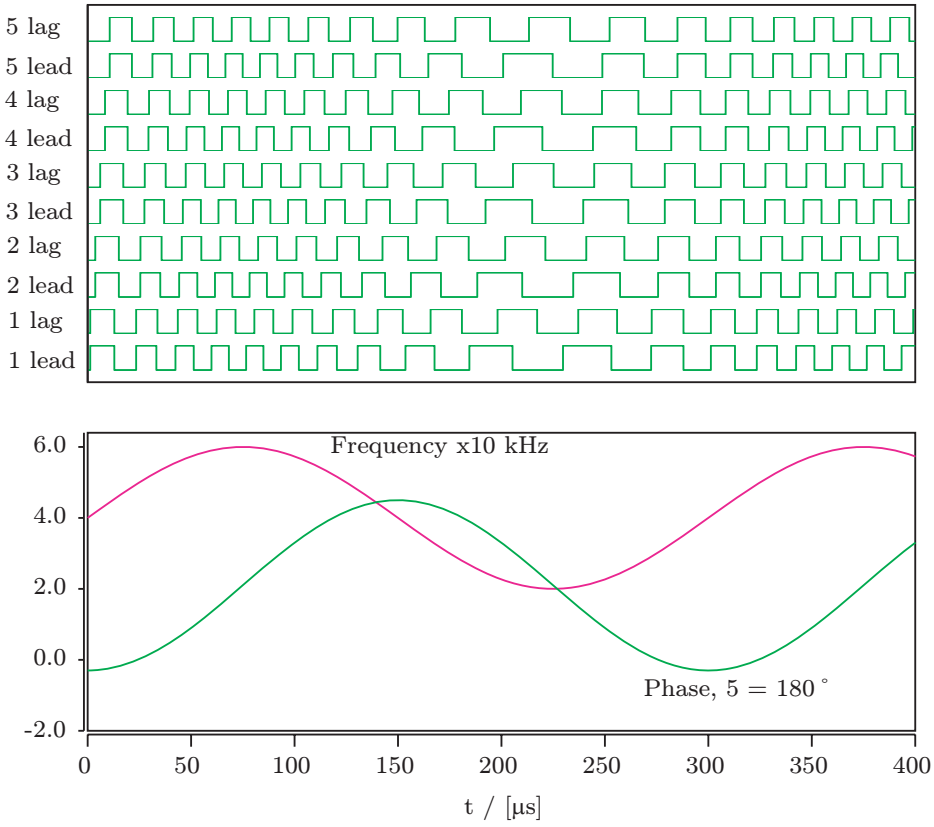


Figure 7.12: IGBT Control signals

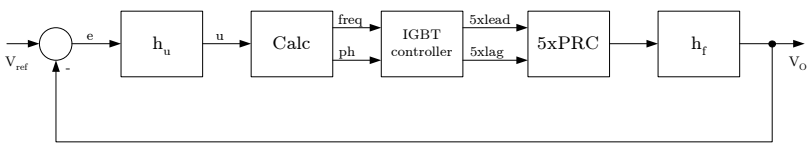


Figure 7.13: Regulator interface

will fire the first pulse without any voltage present in the system and thus see the full load impedance. However, when module number five is fired the other modules will have built up the capacitor voltages so that the fifth module only see about one fifth of the load impedance. This causes different responses and thus different voltages in the modules.

When the converter is ran in open loop, the imbalance dies off after time. But the constant altering of the operation taking place when ran in closed loop sustain the imbalance. The imbalance leads to ripple far above the tolerance and must be reduced.

An internal compensation loop was established to handle the problem. The voltage was measured on each module and compared to the average module voltage. To avoid ripple, the measurements were based on the positive and negative peak voltage in the resonant capacitor. The difference between the individual voltage and the average voltage was used as a direct feedback signal into the phase control of the modules. With the compensation it was possible to bring the converter output close to the ideal case. Figure 7.15 shows the uncompensated output compared with the compensated one.

A simplified block diagram of the control principle is shown in Figure 7.14.

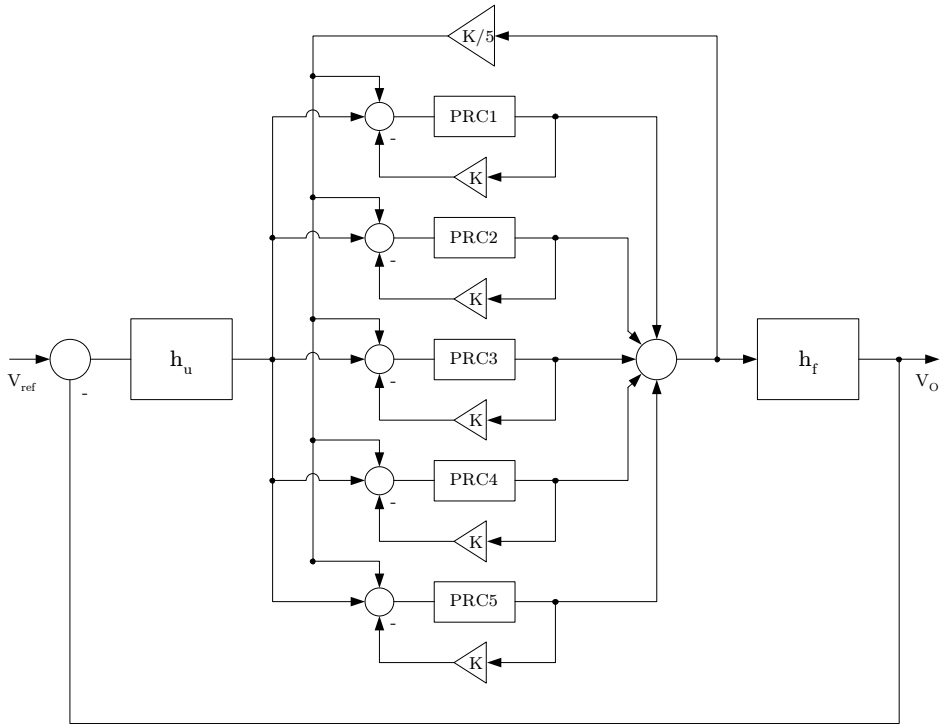


Figure 7.14: Control diagram with balance control

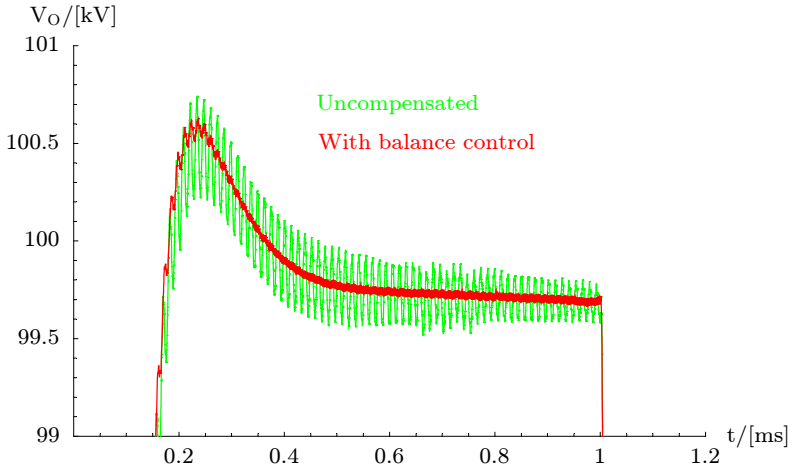


Figure 7.15: Sub-harmonic ripple

7.5 Pulsed operation

The output voltage from the converter in pulsed mode is shown in Figure 7.16. Figure 7.16(b) shows that the converter has reached the 1 % droop margin after 168 μs.

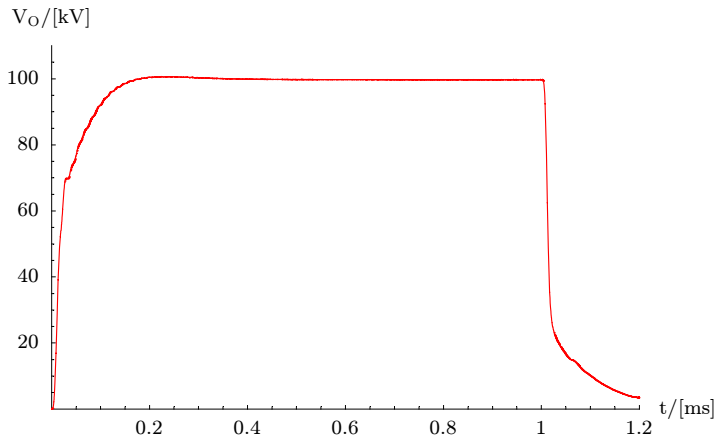
Figure 7.16(c) shows the general output ripple. In the ideal case the 35 V / 400 kHz ripple that is visible should be the only ripple. But since there still is some module imbalance there is a sub-harmonic ripple running at around 10 V / 80 kHz. This sum up to a total ripple of 45 V which is well within the requirement.

7.5.1 Soft Switching

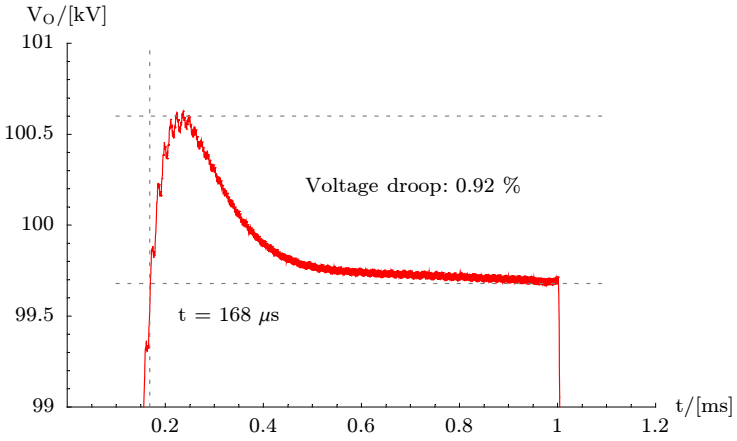
Figure 7.17 shows the resonant circuit and the operation of the two transistor legs. It can be seen that soft switching is obtained in both legs. The slow moving voltage over the transistors of the leading leg is caused by the snubber capacitors charging and discharging.

7.5.2 Control Improvements

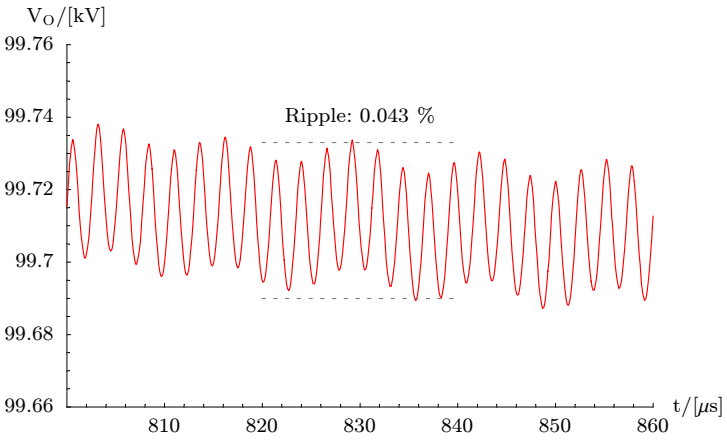
The achieved rise time of 168 μs is higher than the 100 μs requirement. It is also higher than the theoretical rise time of 70 μs, and the possibilities for improvements should be investigated. Figure 7.18(a) shows a comparison between the open loop step response and the closed loop step response. In the open loop case the output reaches 100 kV in 70 μs. Due to the dynamics in the system, one cannot expect to reach 100 kV in 70 μs and then keep the overshoot within the 1 % band. However, by trying different reference steps in open loop it was found that the converter quickly can drive large



(a) Output voltage

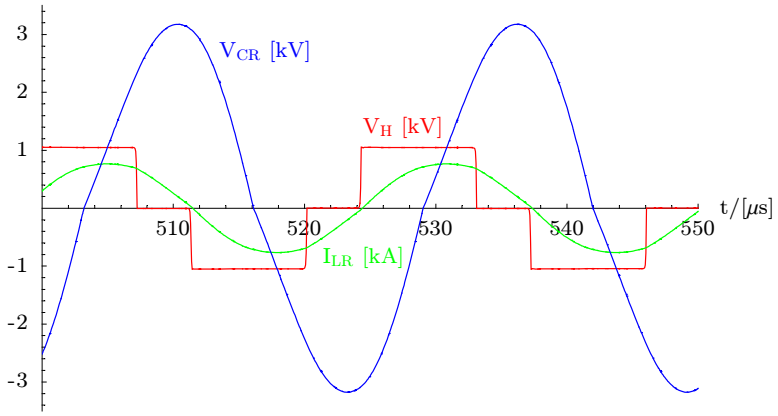


(b) Output voltage droop

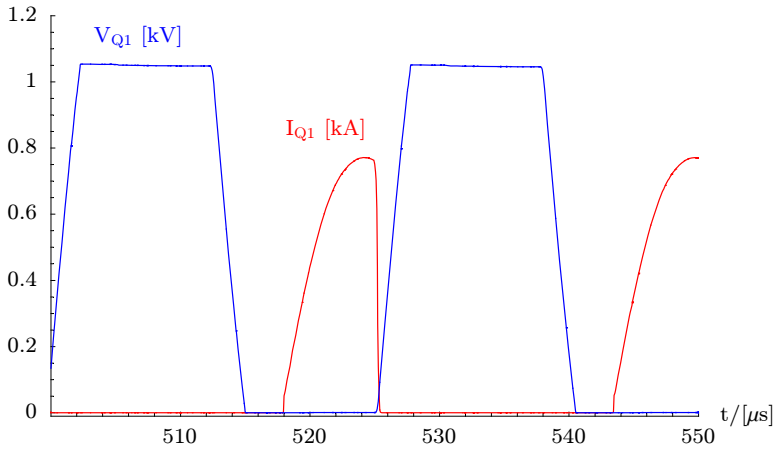


(c) Output voltage ripple

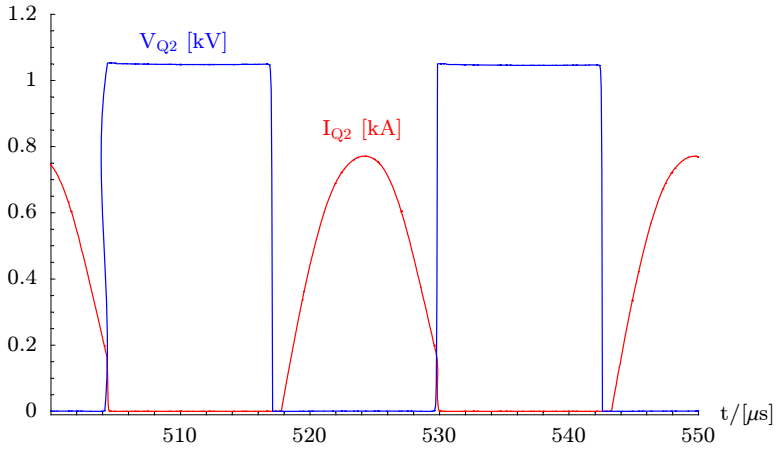
Figure 7.16: PRC Simulated output voltage



(a) Resonant circuit conditions



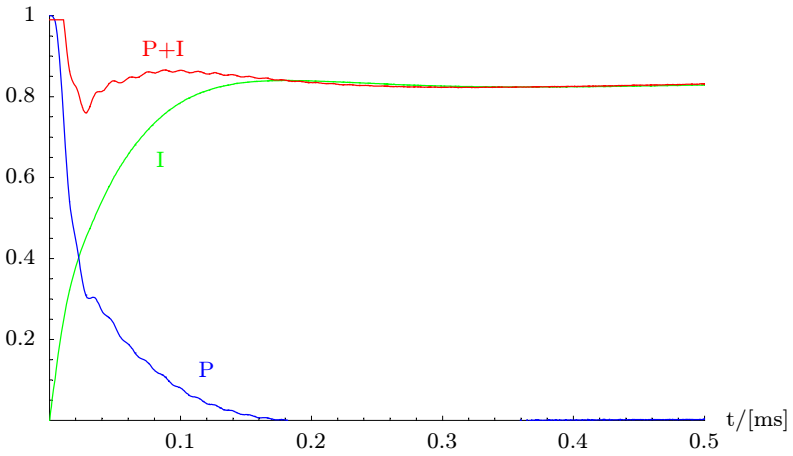
(b) Leading leg



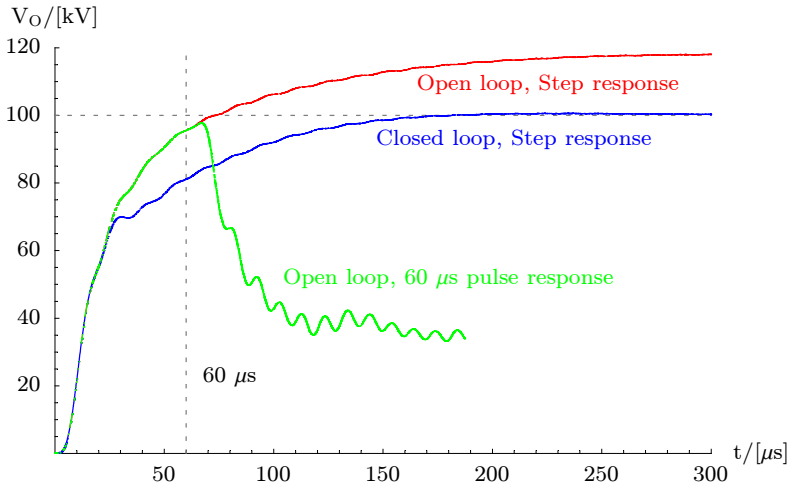
(c) Lagging leg

Figure 7.17: Soft switching

steps in the output, except from that there is a time delay of about 10 μs through the converter. This is illustrated by the green line in Figure 7.18(a) where the open loop regulator is subjected to a 60 μs pulse. This delay will reduce the speed of the control loop and is in a large part responsible for the slowed control system. The different parameters of the controller in closed loop is shown in Figure 7.18(b). It can be seen that the integrator works to slow to exploit the full potential of the system.



(a) Regulator variables



(b) Closed loop vs open loop response

Figure 7.18: Regulator analysis

One way to increase the speed of the regulator is to measure the converter response earlier in the system. For instance an inner control loop based on the inductor current will be able to increase regulator bandwidth. A system

with an inner feedback loop is shown in Figure 7.19. In the figure the original PRC, described by the transfer function h_v is divided into the two sub-systems h_{v1} and h_{v2}. This allows for using two regulators h_{u1} and h_{u2}. Since the PRC operates with alternating conditions, some signal processing will be required to obtain a steady measurement signal. One possible way to quickly obtain a steady signal is to perform a half-cycle moving average.

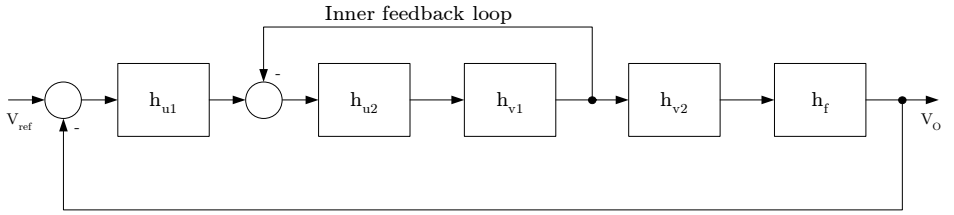


Figure 7.19: PRC with inner feed-back loop

Since the converter operation is very predictable, another possibility to reduce the rise time is to run the converter in open loop during the transient period with a reference signal that has been calculated on beforehand. However, this is less flexible and may not be desired if the system is to be used for different applications.

7.6 Arc Response

The converter response to an arc in the Klystron is very important since this must be expected during operation. The are two key issues in arc operation. Firstly the converter it self must be able to handle the situation without damaging voltages or currents. Secondly the converter must not allow a dangerous amount of energy to enter the arc. The maximum allowed energy is 10 J.

The simulation of the arc was performed by adding an equivalent circuit for the arc as shown in Figure 7.20 to the already developed PRC simulation. When the arc is established, it is expected to operate with voltage source characteristics at around 100 V. To have some safety margin, the simulation is based on a 200 V arc since this will lead to higher arc power. The converter response was not affected by the increase.

7.6.1 Converter Operation upon Arcing

The PRC is expected to have good short circuit handling capabilities due to the natural attenuation in the resonant circuit. A full simulation was performed with the arc condition, resulting in the waveforms shown in Figure 7.21. The arc is trigged at t = 0. The waveforms are plotted for all 5 modules. It can be seen from Figure 7.21(a) that the resonant capacitor

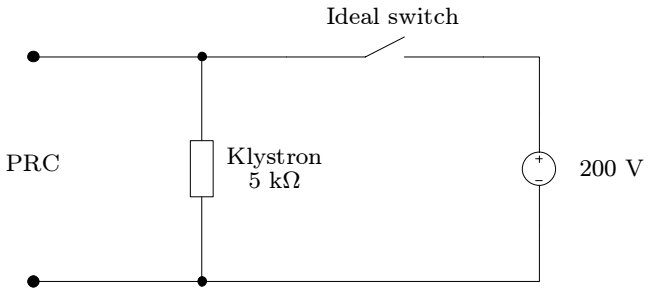


Figure 7.20: Arc equivalent

voltage quickly drops towards zero. This causes the converter to enter DCM where the rectifier bridge is short circuited for some periods of time during the switching cycles. The performance of the PRC during the arc condition is poor, and almost no energy passes through the rectifier bridge. Figure 7.21(b) and 7.21(c) shows the inductor currents and the IGBT currents respectively. It can be seen that the currents actually are reduced from their nominal level during arc conditions. The converter is thus well protected form the arc.

7.6.2 Deposited Arc Energy

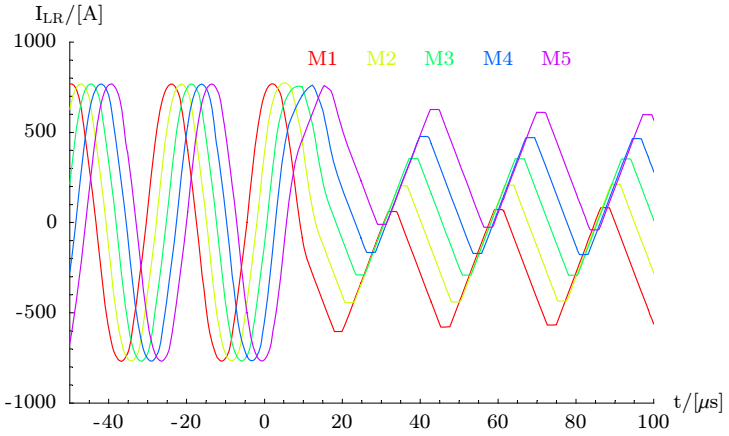
To find the energy dissipation in the arc, the problem is evaluated in two steps. Firstly the amount of energy that is present within the components of the PRC that will be transferred to the arc is calculated. Secondly the supplied power from the PRC when operating in steady state conditions with an arc is considered in Section 7.6.3.

All the energy in the filter must be expected to be transferred to the arc. The filter energy can be calculated from the DC conditions. The filter branch with the capacitor and the series resistor is a little more complicated since a large part of the capacitor energy will be dissipated in the resistor. The capacitor voltage and current will follow the basic natural step response as shown in Equations 7.34 and 7.35. The deposited arc energy can be found by integrating the capacitor current multiplied with the arc voltage as shown in Equation 7.36. The results are shown in Table 7.6.

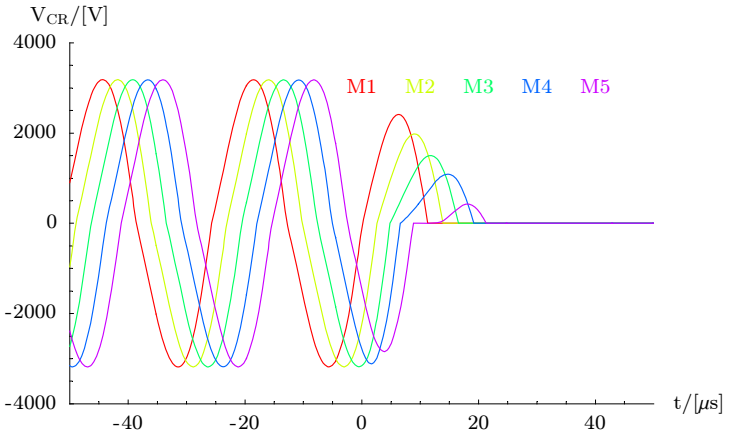
$$v_C = (V_0 - V_{arc})\, e^{-\frac{t}{\tau}} + V_{arc} \tag{7.34}$$

$$i_C = C\frac{dv_C}{dt} \tag{7.35}$$

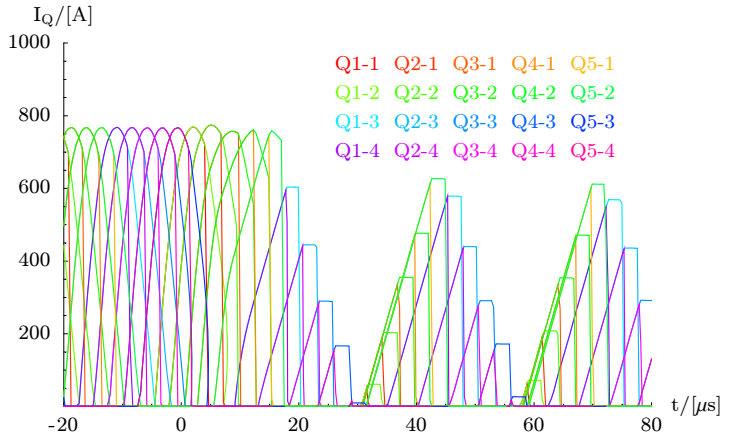
$$W_{arc} = \int_0^\infty i_C \cdot V_{arc}\, dt = C\, V_{arc}\, (V_0 - V_{arc}) \tag{7.36}$$



(a) Resonant inductor current



(b) Resonant capacitor voltage



(c) Transistor current

Figure 7.21: PRC arc response

It is difficult to predict the exact PRC response and the energy movements in the circuit during the transient arc response. However, if one considers the resonant capacitors, it can be seen that they fall very quickly towards zero. The energy transfer from the PRC can be assumed neglectable after the capacitor discharge for this short transient analysis. As the PRC enters the arc condition, all the energy released from the PRC is expected to be transferred to the filter inductor. The voltage and current waveform for the inductor is shown in Figure 7.22. If the arc voltage is assumed neglectable compared to the nominal output voltage, the total energy transfer from the PRC to the arc can be calculated from the current change in the filter inductor. The total arc energy balance is showed in Table 7.6.

Filter inductor L_f	4	J
Filter capacitor C_f	5	J
Filter C+R branch $4C_f + 1/4R_f$	80	mJ
PRC resonant circuit	35.69	J
Total arc energy	44.77	J

Table 7.6: Arc energy

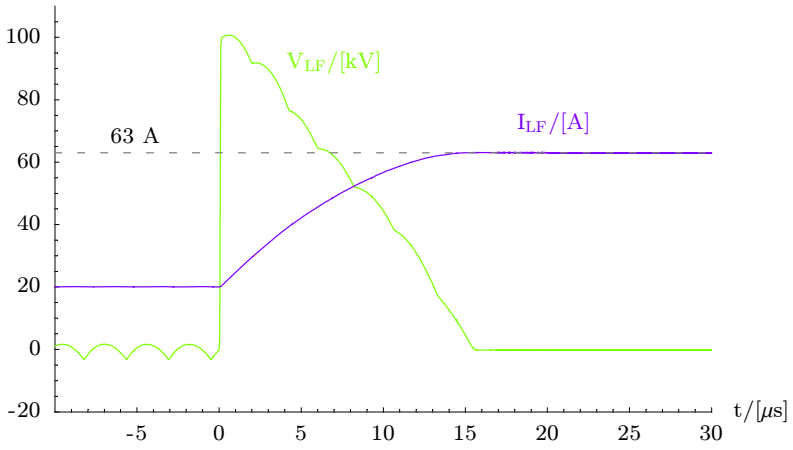


Figure 7.22: Filter inductor during arc transient

It can be seen that the capacitor branch including the resistor only contributes with an insignificant amount of energy compared to the single capacitor, even though the initial energy in the branch is 4 times the single capacitor. This is caused by the large voltage difference between the arc and the initial capacitor voltage. Most of the energy is therefore dissipated in the resistor. As can be seen from Equation 7.36 this energy loss is not related to the value of the resistance, only the voltage difference. Since there will be some series resistance in the circuit, the same effect can also be expected

for the single capacitor. Also the polarization mechanisms in the capacitor are expected to dissipate some energy in such a quick discharge. However, the simplified arc transition will not be true and a lot more energy may be transferred during the arc transient.

The inductor energy will be transferred slowly to the arc due to the low arc voltage. Most of the energy should therefore be expected to end up in the arc.

As can be seen from Table 7.6, the arc energy exceeds the limit with several multiples. However, this is not problematic since it will be easy to substantially reduce the arc energy. A 100 Ω resistor placed in series with the load would hold a significantly larger voltage than the arc and dissipate most of the energy. Additionally a MOV can be placed in parallel with the filter inductor to dissipate some of the energy transferred from the PRC. The energy calculations for the PRC therefore are very promising.

7.6.3 Steady State Arc Power

The steady state power was found by running the resonant converter with the arc condition until it had stabilized in steady state. The steady state current showed to be 34 A which gives 6.8 kW for a 200 V arc. This corresponds to 147 μs per joule of arc energy. Thus the timing from the arc is detected to the PRC is shut down is not critical. Depending on the arc energy found in the previous section, it may not be necessary to shut down the converter at all upon arcing.

7.7 Transformer Considerations

The simulation has been based on an ideal transformer connected after the resonant circuit as shown in Figure 7.11. A real transformer will have leakage inductance, magnetizing inductance, and stray capacitance, which will influence on the system. One of the benefits with the PRC is that if the circuit is configured correctly, the transformer parasitics can be incorporated as a part of the resonant circuit. The equivalent circuit of a transformer with all components refered to the primary was given in Figure 4.8 on page 33. If the transformer is connected between the inductor and the capacitor in the resonant circuit, as shown in Figure 7.23, the transformer inductance and capacitance will be incorporated as a part of the resonant circuit. The transformer parasitics can then be subtracted from the resonant circuit components. If the transformer is designed correctly the resonant inductance may even be avoided altogether. In this case the transformer must handle the full voltage steps from the H-bridge.

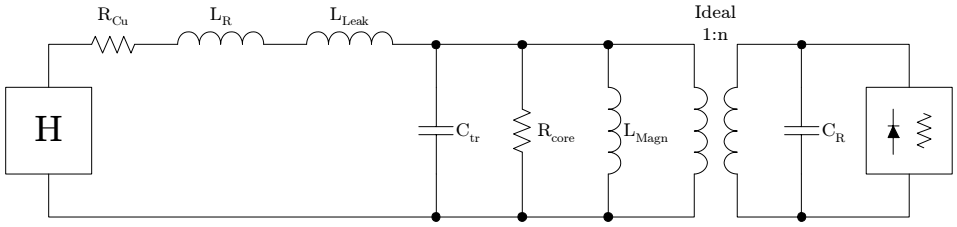


Figure 7.23: PRC transformer configuration

7.8 Summary

The resonant converter has been found to be an interesting topology for the Klystron modulator. It can be capable of supplying the pulse within the required limits, and it also has very good arc handling capabilities. In addition to this, the topology is flexible with its module based configuration, and can be scaled to meet varying demands. The modularity also opens for adding redundancy to the system, thus creating a reliable modulator. The PRC will be especially interesting for the 50 Hz SPL if it is realized, since it will be difficult to operate the single switch topology at this frequency.

However, the topology is complicated to implement and requires a large number of processes and measurements to be continuously monitored. A large investment on the development of the control system and the transformer must be foreseen. The high transforming frequency and the high secondary voltage may show to be challenging. The topology also requires the IGBTs to be run close to their maximum switching frequency, with the problems this involves.

Chapter 8

Conclusion

The prototype tests have shown to be successful and the Klystron modulator works in full accordance with the theoretical modeling. It has not yet been brought up to its full voltage of 100 kV, but have been tested up to 57 kV. However, since all the critical components of the system have been tested at full voltage, except from the pulse transformer, there is no reason to expect problems at full voltage. The only possible major problem that is foreseen is breakdown of the transformer insulation. The company that manufactured the transformer has long experience with high voltage components and insulation breakdown is very unlikely. It is therefore expected that the Klystron modulator project will show to be successful on quality, ratings, and time of delivery.

8.1 Future Klystron Modulators

A proof of concept of the Parallel Resonant Converter has been created through simulations, showing to be very promising. The PRC shows good controllability, flexibility, and high efficiency. Most of the requirements are meet with a good safety margin. The arc handling capabilities of the converter are excellent with a natural response that automatically protects the Klystron.

However, the PRC also shows some challenges that might show to be difficult to achieve in the practical setup. The long time constant of the PRC requires the transistor switching frequency to be operated above normal levels for the converter to meet the rise time requirement. The simulations were operated at 40 kHz. With the soft switching opportunities that the PRC offers this should not be problematic in relation to switching loss in the transistors, but a control system operating at this frequency may show to be difficult to implement. Moreover, the high switching frequency will lead to strict requirements and high stresses on the transformer. Because of this the transformer may show to be difficult to manufacture within reasonable

cost and development.

The single switch topology can also meet various demands through different configurations of serial connected module systems. The drawback with the topology is that it relies on a pulse transformer which is expensive and hard to obtain. The pulse transformer will often be the bottle neck in producing such a system and also restricts the flexibility of operation. Both step-up ratios above 10, and multiple primary configurations, are hard to obtain. The topology therefore has to rely on expensive high voltage switches. The single switch topology must also include a reliable arc detection system since early detection of the arc is crucial to offer sufficient protection for the Klystron.

It therefore viewed as advantageous to investigate further the PRC topology, and keep the single switch topology as a backup solution. Development of the PRC must be expected to be a costly and time consuming process. However, if such a development is successful, the PRC may show to be a flexible and efficient solution that can be used in numerous pulsed high voltage applications worldwide for years to come.

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Appendix A

Phase Plane Analysis

Phase plane analysis is a simple method for transient analysis of resonant circuits. The key to the method is the fact that oscillating LC circuits undergo cyclical oscillations. When plotted in the V / I plane, where I is scaled by the factor $\sqrt{L/C}$, the oscillations can be as perfect circles or arcs. The center of the circle is defined by the DC conditions and the radius is given as an initial condition.

The circuit that are to be analyzed with phase plane analysis should be converted to a circuit consisting only of DC sources like the example showed in Figure A.1. Based on the circuit, the phase plane diagram can be drawn as a circle with center $(V_{DC}, I_D C)$. The radius is given as the distance the center to the initial condition. The circle represents the true voltage/current relationship for the inductor current i_L and the capacitor voltage v_C. The traveled angle is given as time multiplied with the resonant frequency, $\alpha = t\,\omega_0$. It is important to note that the way the polarities are defined in Figure A.1 which results in the positive time direction to be clockwise.

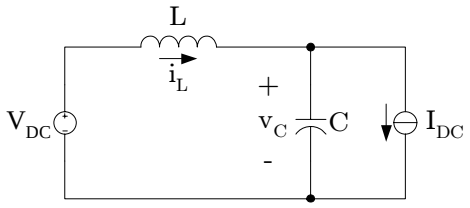


Figure A.1: Circuit suitable for phase plane analysis

As an example the following circuit operating after in the conditions given in Table A are considered.

In state 0 the system is completely dead without any voltage or current. When the system is switched over to state 1 the initial condition is therefore zero. The DC conditions are as given by the state. Hence, the system will

State	V_{DC}	I_{DC}	(v_{ic}, i_{ic})	Cycles
0	0	0	-	-
1	-1	1	$(0, 0)$	several
2	1	-1	$(-2, 0)$	partial
3	1	1	$\left(1, \sqrt{10} - 1\right)$	several

Table A.1: Operating conditions for example circuit

operate along a circle with center $(-1, 1)$. The radius of the circle is the distance between the initial condition and the center, and is $Sqrt2$. The system is stable in the state and will continue the run clockwise around the circle until the DC conditions are changed.

After some cycles in state 1 the system is switched over to state 2 at the zero current crossing. After the change, the initial condition has to equal the end condition of state 1. The DC conditions however, immediately switches and brings the system over to the second arc with a different center and radius. In the example the system is only allowed to stay in state 2 for a short time before it is switched over to state 3.

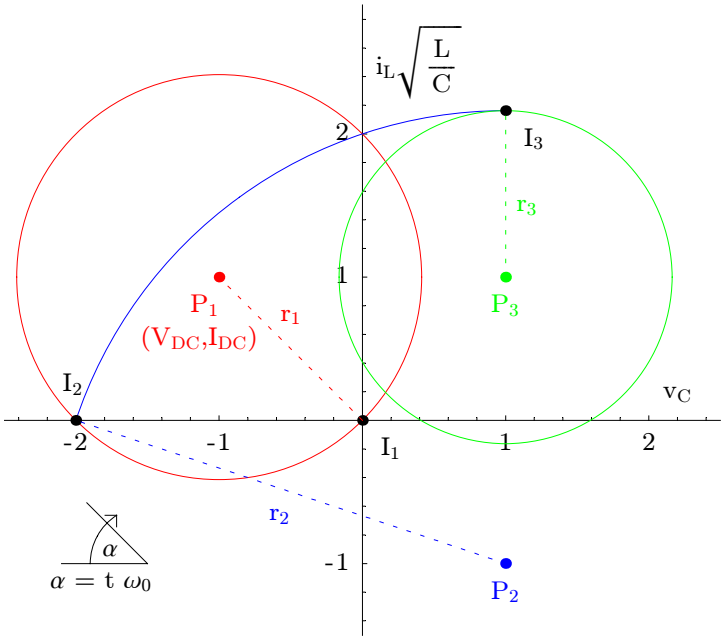


Figure A.2: Phaseplane analysis example

The method requires a non-resistive system. It is also possible to express damped systems with phase plane analysis. For instance, in the underdamped case, the curve will spiral towards the center until it enters steady DC operation. However, the simple method of deriving the operational conditions only works with non-damped systems.

Appendix B

Testresults with ABB 7xIGCT switch

B.1 Commissioning

As an initial verification of the assembly, setup, and mode of operation, a series of basic qualitative function tests were performed. The testprocedure is attached in its original form.

B.1.1 Verification of assembly

Test the basic assembly. Confirm correct assembly and mode of operation for the system by testing at lowest possible voltage. Bouncer is short-circuited and out of operation. Maximum voltage for the test is 1 kV. The test can be performed without safety shielding.

No	Voltage	Observe/Measure	Result
1	100-200 V	Confirm correct operation of capacitor discharger (Ross relay) by activating it and measuring the capacitor voltage	pass
2	100-200 V	Confirm full opening of the switch by measuring the voltage over the switch	pass
3	100-200 V	Confirm correct load configuration by measuring the load current with a current probe	pass
4	1 kV	Measure the full pulse and ensure that the general operation looks good	pass
5	1 kV	Measure the overshoot at switch off and ensure it is within the safe range	pass
6	1 kV	Measure switch off time and compare with specifications	pass
7	1 kV	Measure switch on time and compare with specifications	pass
8	1 kV	Control EMC intrusion on probes by measuring capacitor voltage during switch on	pass

Table B.1: Commissioning - Part 1

B.1.2 Full voltage testing

Increase voltage gradually to the full voltage while measuring switch off overshoot and EMC intrusion on measurements. All safety precautions has to be taken for this test.

No	Voltage	Observe/Measure	Result
1	3 kV	Measure the full pulse and ensure that the general operation looks normal	pass
2	3 kV	Measure the overshoot at switch off and ensure it is within the safe range	pass
3	5 kV	Measure the full pulse and ensure that the general operation looks normal	pass
4	5 kV	Measure the overshoot at switch off and ensure it is within the safe range	pass
5	7.5 kV	Measure the full pulse and ensure that the general operation looks normal	pass
6	7.5 kV	Measure the overshoot at switch off and ensure it is within the safe range	pass
7	12 kV	Measure the full pulse and ensure that the general operation looks normal	pass
8	12 kV	Measure the overshoot at switch off and ensure it is within the safe range	pass
9	12 kV	Control EMC intrusion on probes by measuring capacitor voltage during switch on	pass
10	12 kV	Run at 2 Hz repetetive mode for 20-30 sec and ensure that the general operation looks normal	pass

Table B.2: Commissioning - Part 2

B.1.3 Bouncer commissioning

Connect the bouncer and test the operation

No	Voltage	Observe/Measure	Result
1	1 kV	Ensure that the bouncer thyristor is trigged and that the bouncer is operating is operating correctly by measuring capacitor voltage and inductor current	pass
2	3 kV	Check for normal operation by measuring capacitor voltage and inductor current	pass
3	3 kV	Test the bouncer with first pulse issues / missing thyristor trigging / wrong trigging of thyristor. Specifically check capacitor charging with short/no time delay. Ensure that undesirable over voltages are avoided by safety crowbar	pass
4	5 kV	Check for normal operation by measuring capacitor voltage and inductor current	pass
5	7.5 kV	Check for normal operation by measuring capacitor voltage and inductor current	pass
6	12 kV	Check for normal operation by measuring capacitor voltage and inductor current	pass
7	12 kV		pass
8	12 kV	Tune in the time delay so that the bouncer capacitor voltage is stable at 650-700V in repetitive mode. Run the system in repetitive mode for 20-30 sec and ensure normal operation	pass

Table B.3: Commissioning - Part 3

B.2 Bouncer optimalisation

Three different bouncer configuration, based on the available inductor, are tested for different operation parameters to find the optimal solution. Due to limitations in the sampling of the pulse generator, the delay time are given as discrete steps allowed by the pulse generator.

#	C_B/μF	L_B/μH	$\hat{V}_{rated}$	$\hat{I}_{rated}$
1	220	500	700	500
2	220	750	700	400
3	150	750	700	400

Table B.4: Bouncer configurations

B.Conf	Run #	Delay [μs]	$\hat{I_L}$ / [A]	$\hat{V_C}$ / [V]
1	1	109.9	596	638
1	2	116.0	580	631
1	3	122.1	564	620
1	4	128.2	552	609
1	5	134.3	540	599
1	6	140.4	529	587
1	7	146.5	516	579
1	8	152.6	504	567
1	9	158.7	492	557
2	1	244.1	508	671
2	2	250.2	494	666
2	3	256.3	476	656
2	4	262.5	464	646
2	5	268.6	456	637
2	6	274.7	452	631
2	7	286.9	435	610
3	1	158.7	520	759
3	2	170.9	492	741
3	3	177.0	480	731
3	4	183.1	472	720
3	5	189.2	460	708
3	6	195.3	453	696
3	7	201.4	440	685
3	8	213.6	424	663
3	9	225.8	408	642
3	10	238.0	392	623

Table B.5: Bouncer optimalisation runs

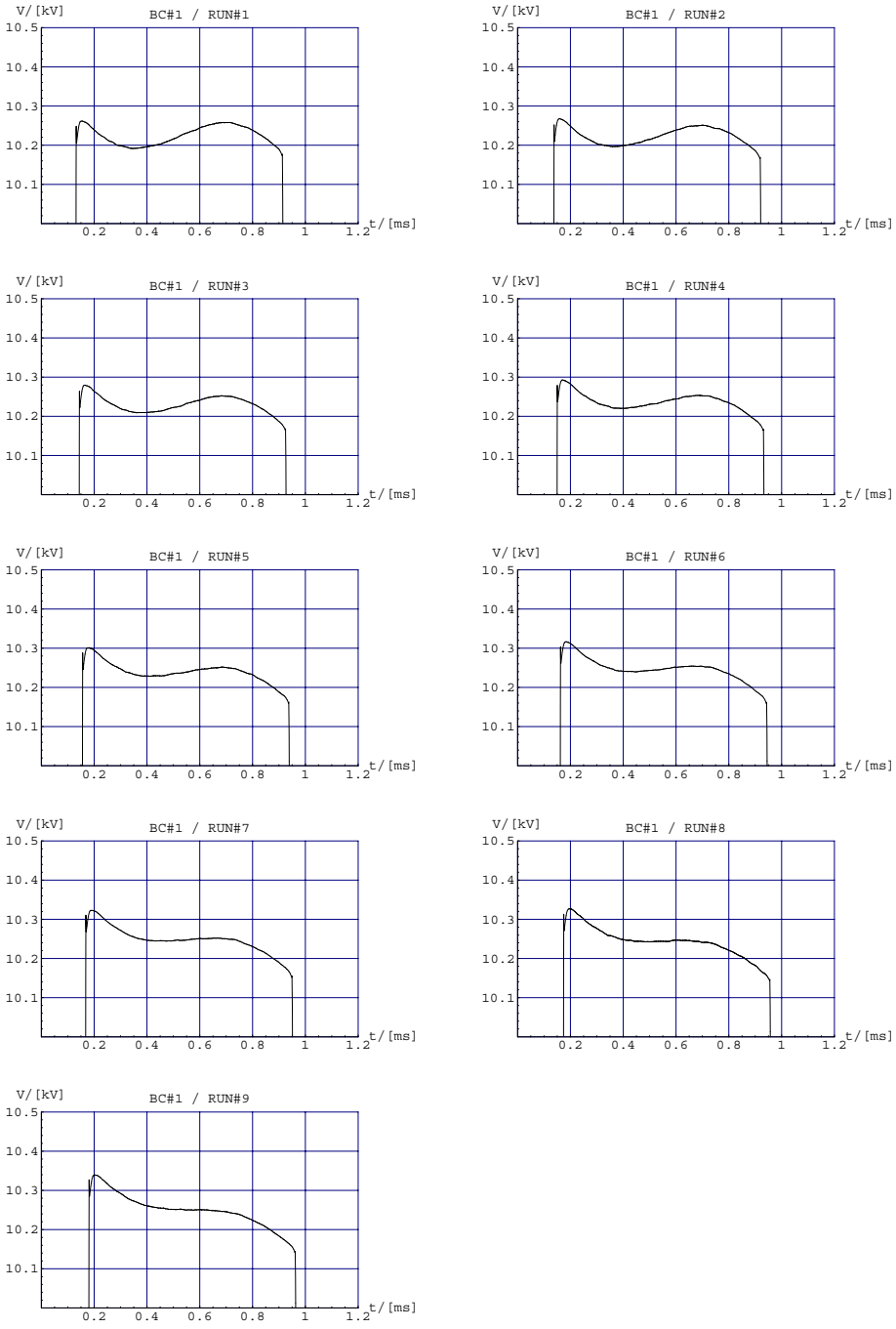


Figure B.1: Flat-top visualisation, bouncer configration 1

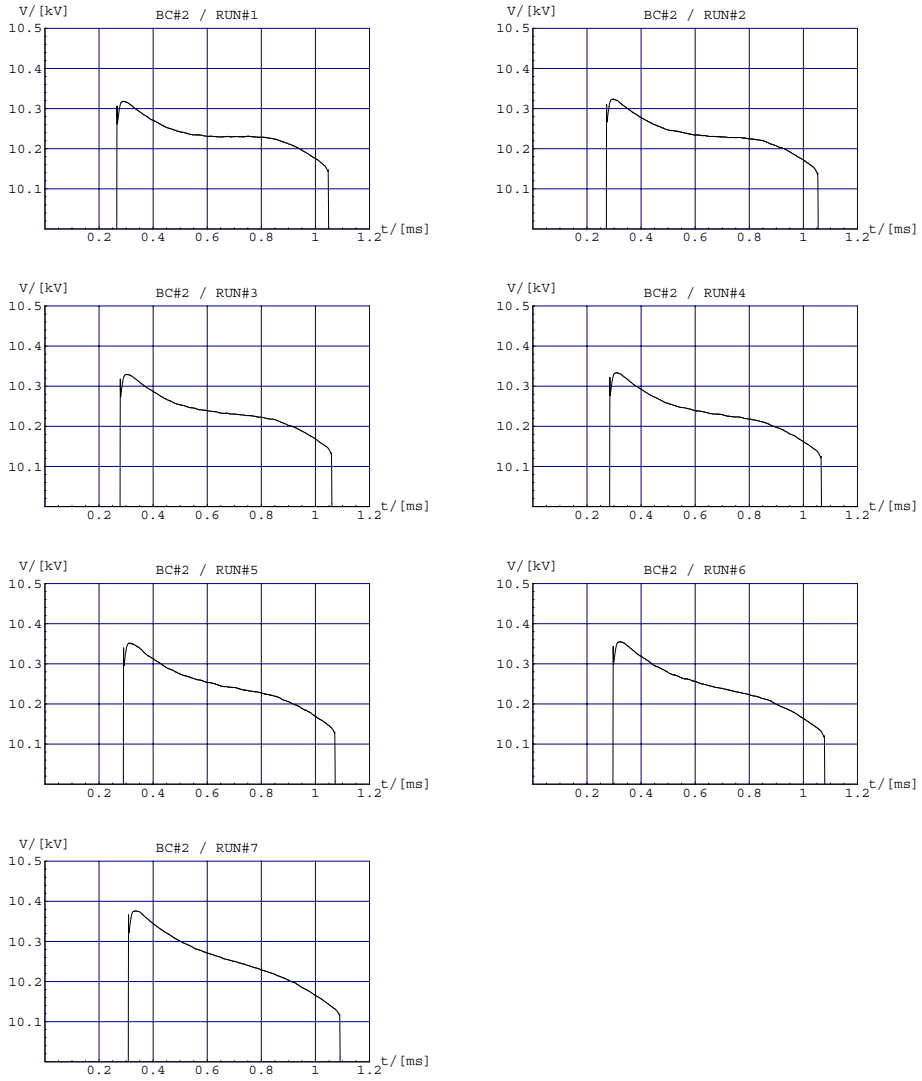


Figure B.2: Flat-top visualisation, bouncer configration 2

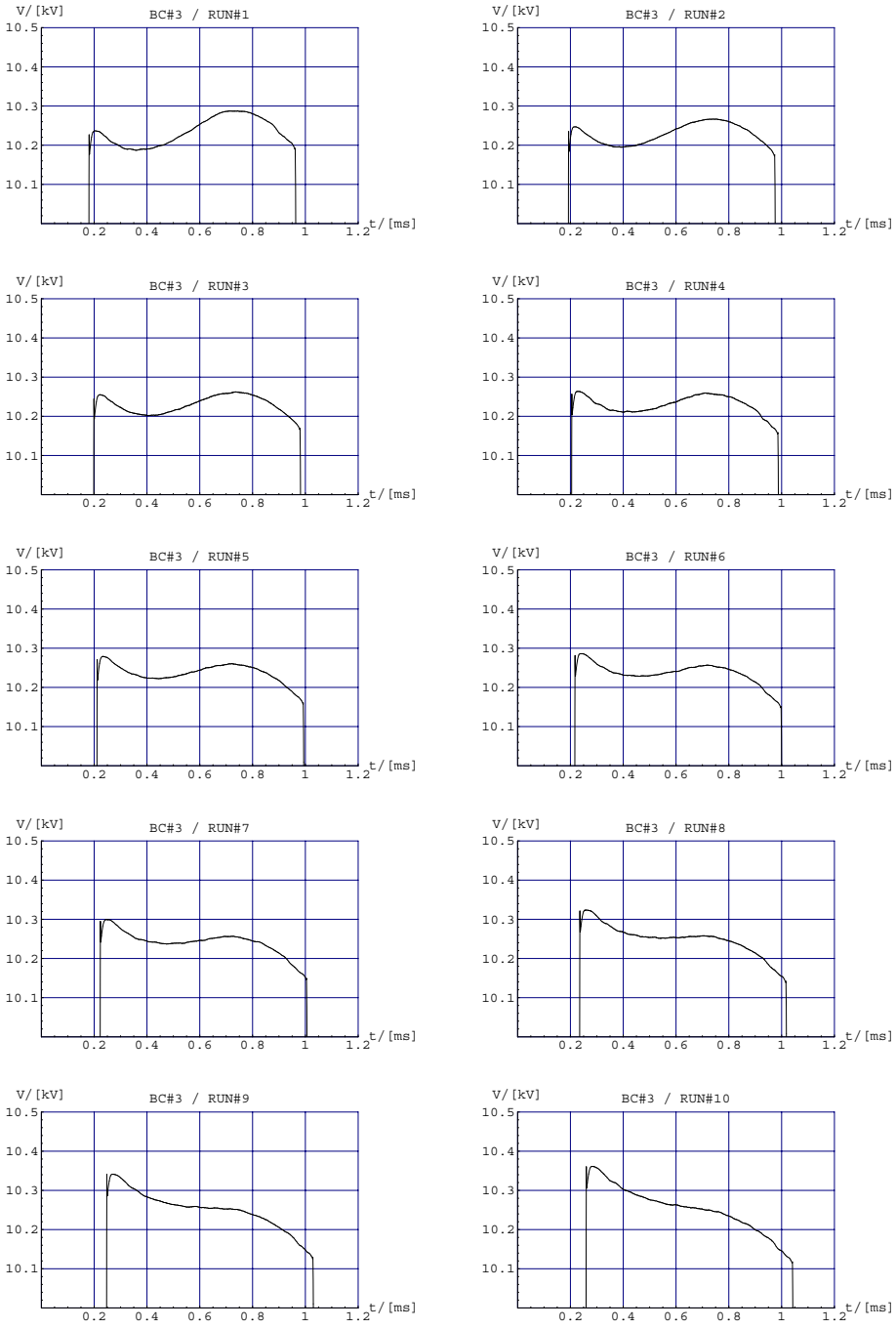


Figure B.3: Flat-top visualisation, bouncer configration 3

B.3 Quantitative tests

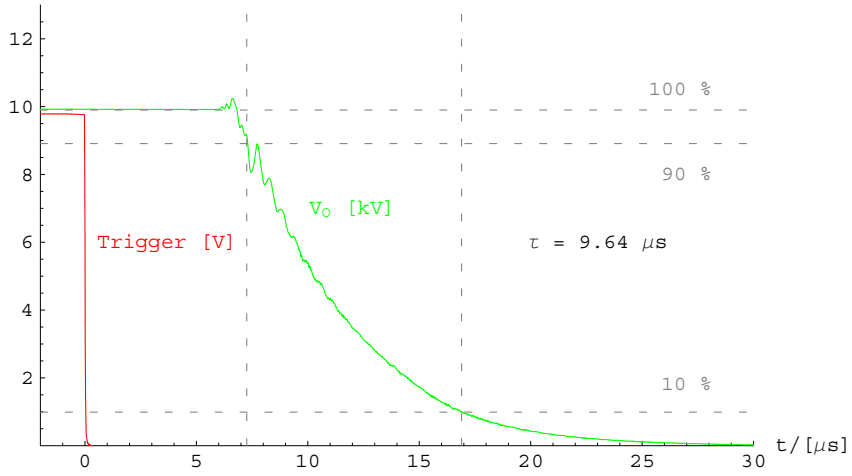


Figure B.4: Fall time

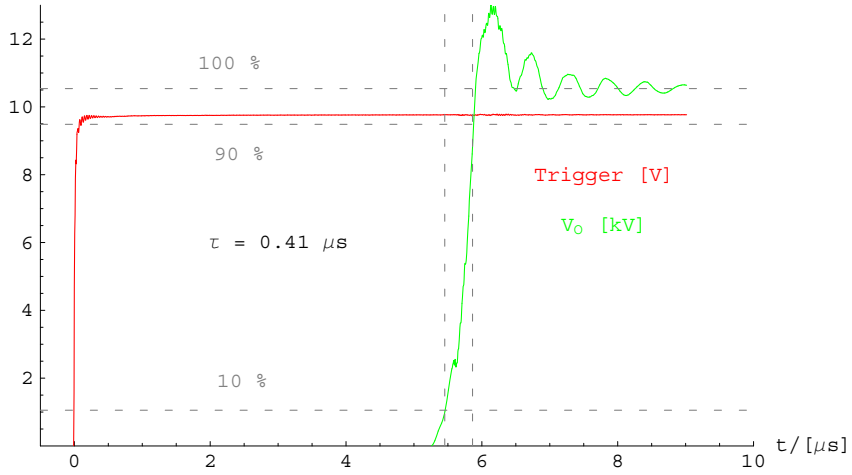


Figure B.5: Rise time

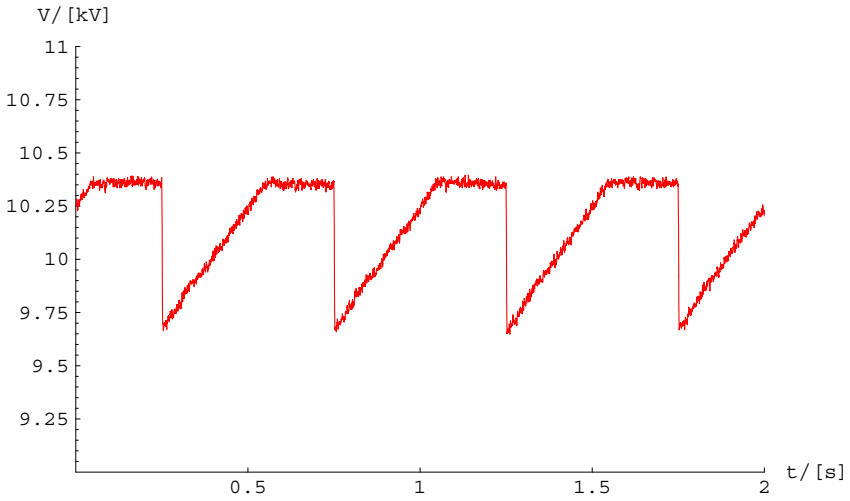


Figure B.6: Charge cycle

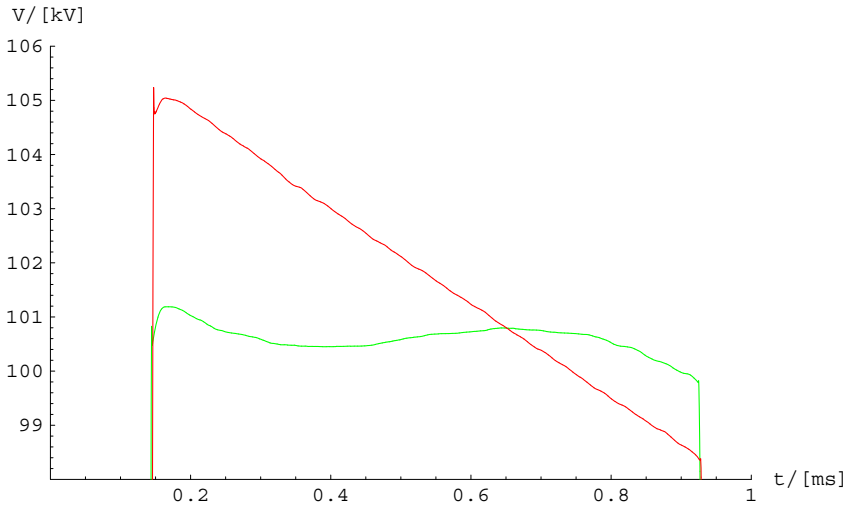


Figure B.7: Effect of the bouncer

Appendix C

PRC Frequency analysis

Input parameters

$Rkly := 5000$ $T1 := 40 \cdot 10^{-6}$ T1 = Converter time constant

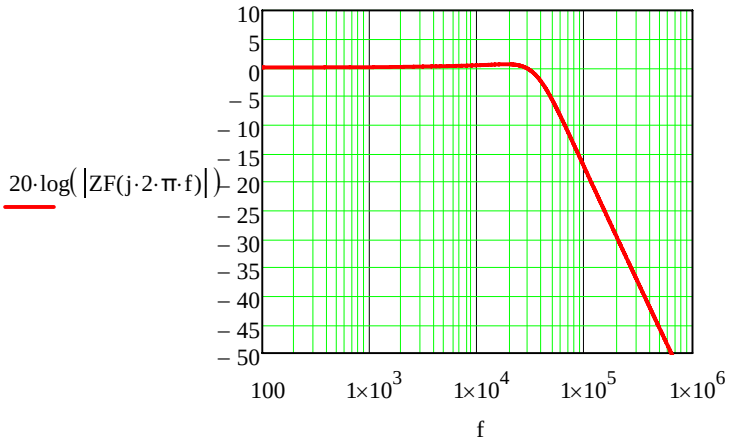
$Lkly := 10 \cdot 10^{-6}$

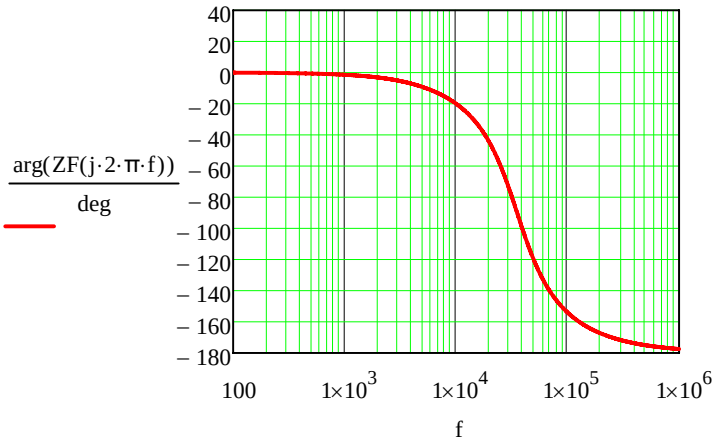
Filter transfer function and filter parameters

$Cf := 1 \cdot 10^{-9}$ $Lf := 20 \cdot 10^{-3}$ $Rf := 60 \cdot 10^{3}$

$$ZC(s) := \frac{\frac{1}{s \cdot Cf} \cdot \left(\frac{1}{s \cdot 4Cf} + \frac{Rf}{4} \right)}{\frac{1}{s \cdot Cf} + \frac{1}{s \cdot 4 \cdot Cf} + \frac{Rf}{4}} \qquad ZCA(s) := \frac{ZC(s) \cdot (Rkly + s \cdot Lkly)}{ZC(s) + Rkly + s \cdot Lkly}$$

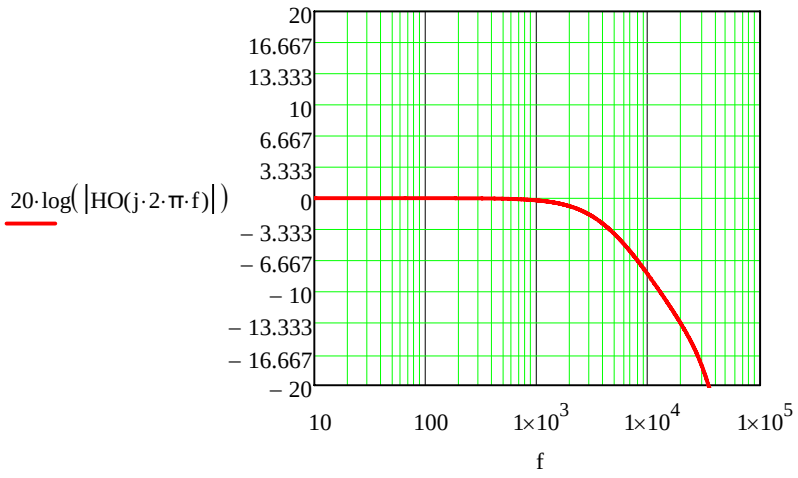
$$ZF(s) := \frac{ZCA(s)}{ZCA(s) + s \cdot Lf}$$

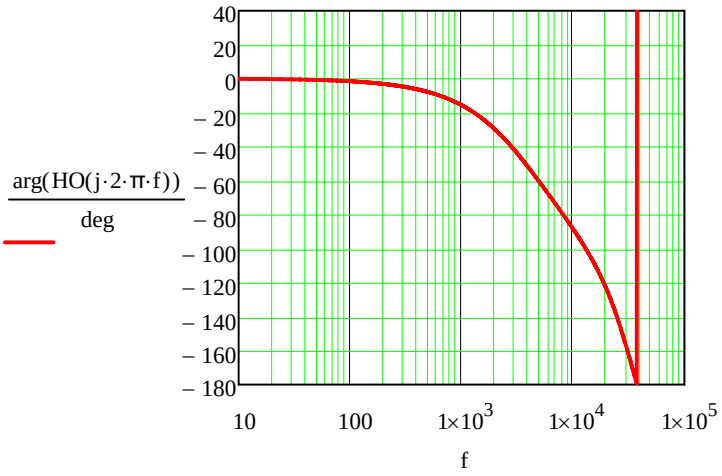




Transfer function including filter and converter

$$Hv(s) := \frac{1}{1 + T1 \cdot s} \qquad HO(s) := ZF(s) \cdot Hv(s)$$



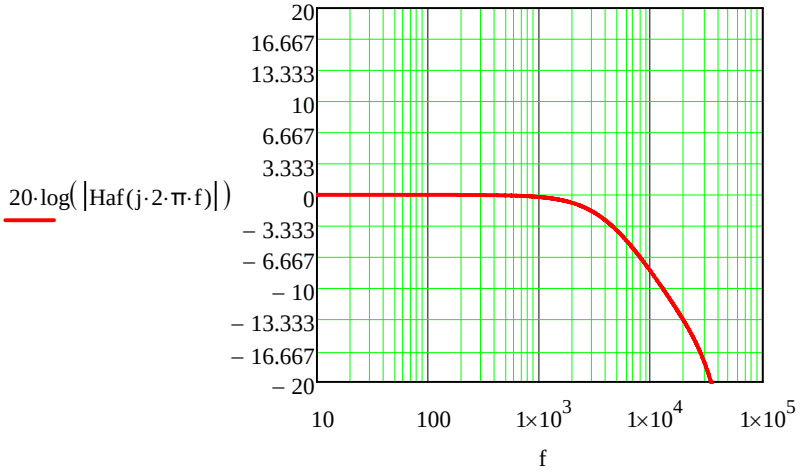


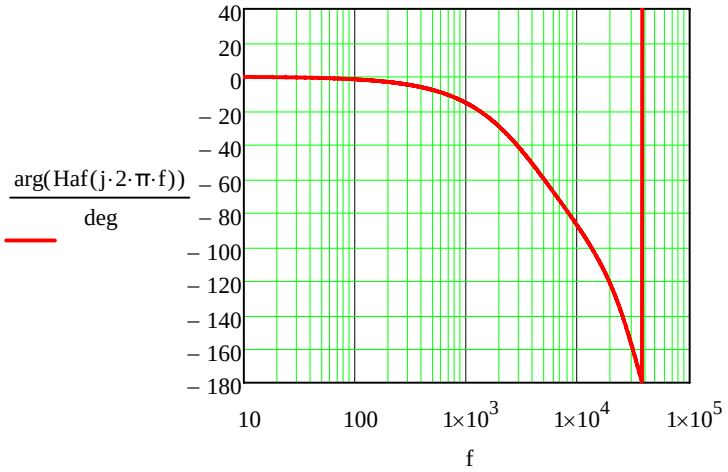
The bode plot is dominated by the converter response. The asymptote in the phase plot is caused by a plotrange from -180 to 180 degrees and simply means that the phase angle is below 180 degrees.

Transfer function including active damping feedback loop

$$KCRI := 0 \qquad ZCRI(s) := \frac{KCRI}{\frac{Rf}{4} + \frac{4}{s \cdot Cf}}$$

$$Haf(s) := \frac{Hv(s) \cdot ZF(s)}{1 + Hv(s) \cdot ZF(s) \cdot ZCRI(s)}$$

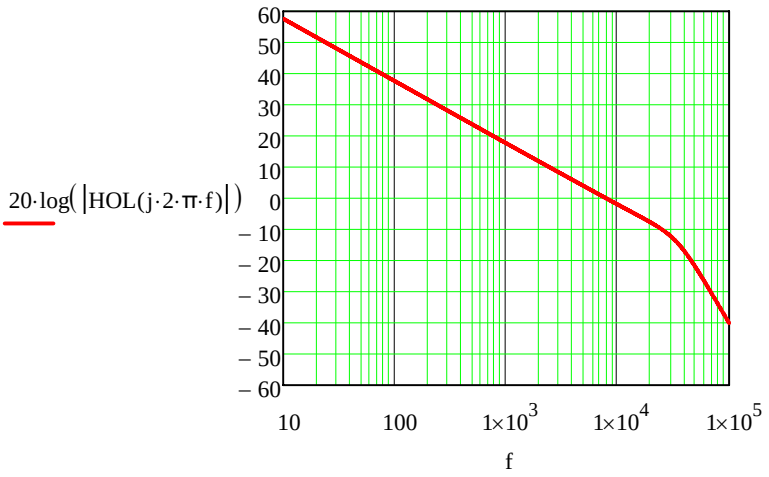


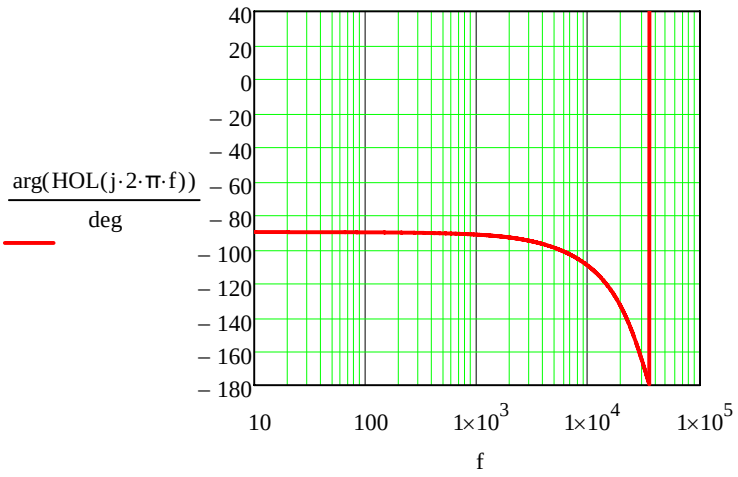


The active damping done by measuring the capacitor current in the damped capacitor and subtracting this from the signal fed to the converter. This is a common way of performing active damping in power converter systems, but due to the slow converter respnse the effect showed to be very limited. The gain of this feedback was therefore set to zero.

PI Controller - Open loop

$Kp := 1.9 \qquad Ti := 40 \cdot 10^{-6} \qquad Hu(s) := Kp \cdot \frac{1 + Ti \cdot s}{Ti \cdot s} \qquad HOL(s) := Haf(s) \cdot Hu(s)$

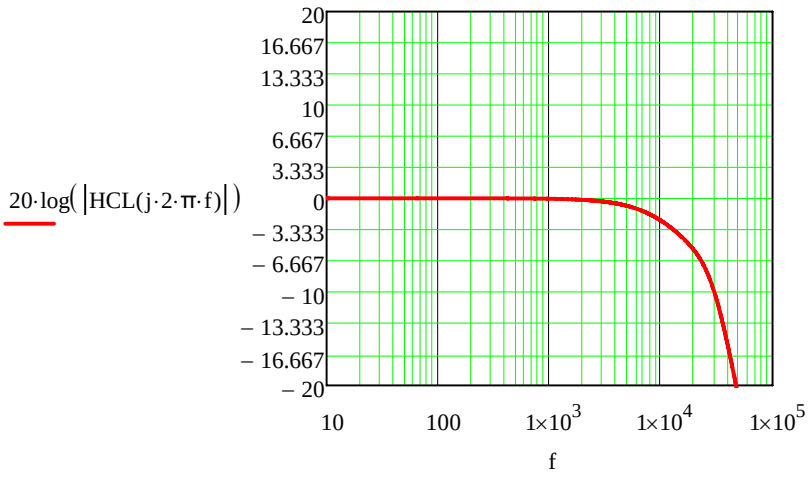


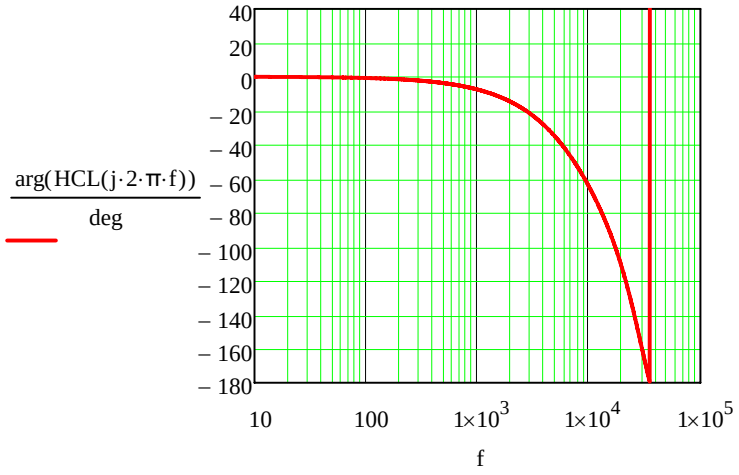


Open loop bode plot with PI controller showing a very safe configuration with 80 degrees phase margin and 15 dB gain margin

PI Controller - Closed loop

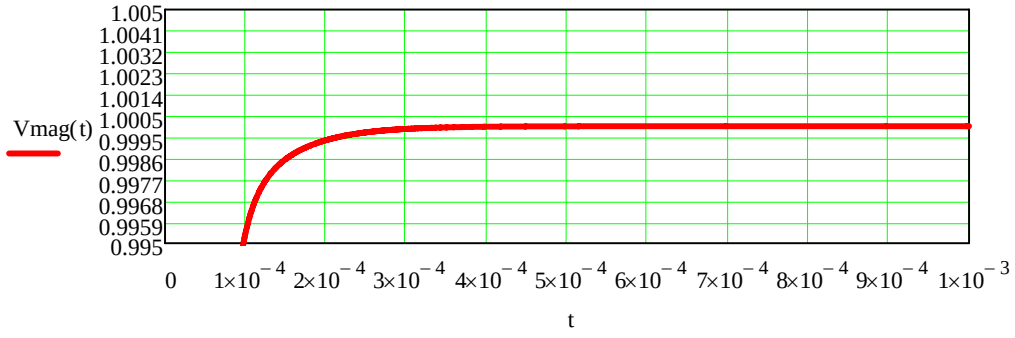
$$HCL(s) := \frac{HOL(s)}{1 + HOL(s)}$$

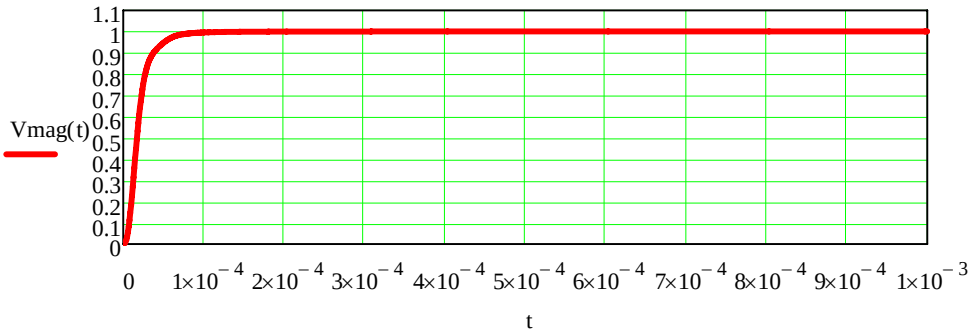




Step response

$$\text{Vmag}(t) := \frac{\text{HCL}(s)}{s} \left| \begin{array}{l} \text{invlaplace}, s, t \\ \text{simplify} \end{array} \right. \rightarrow 2.3599772244940214297\text{e-}21 \cdot e^{-83333.333333333333333 \cdot t} + 2.77$$



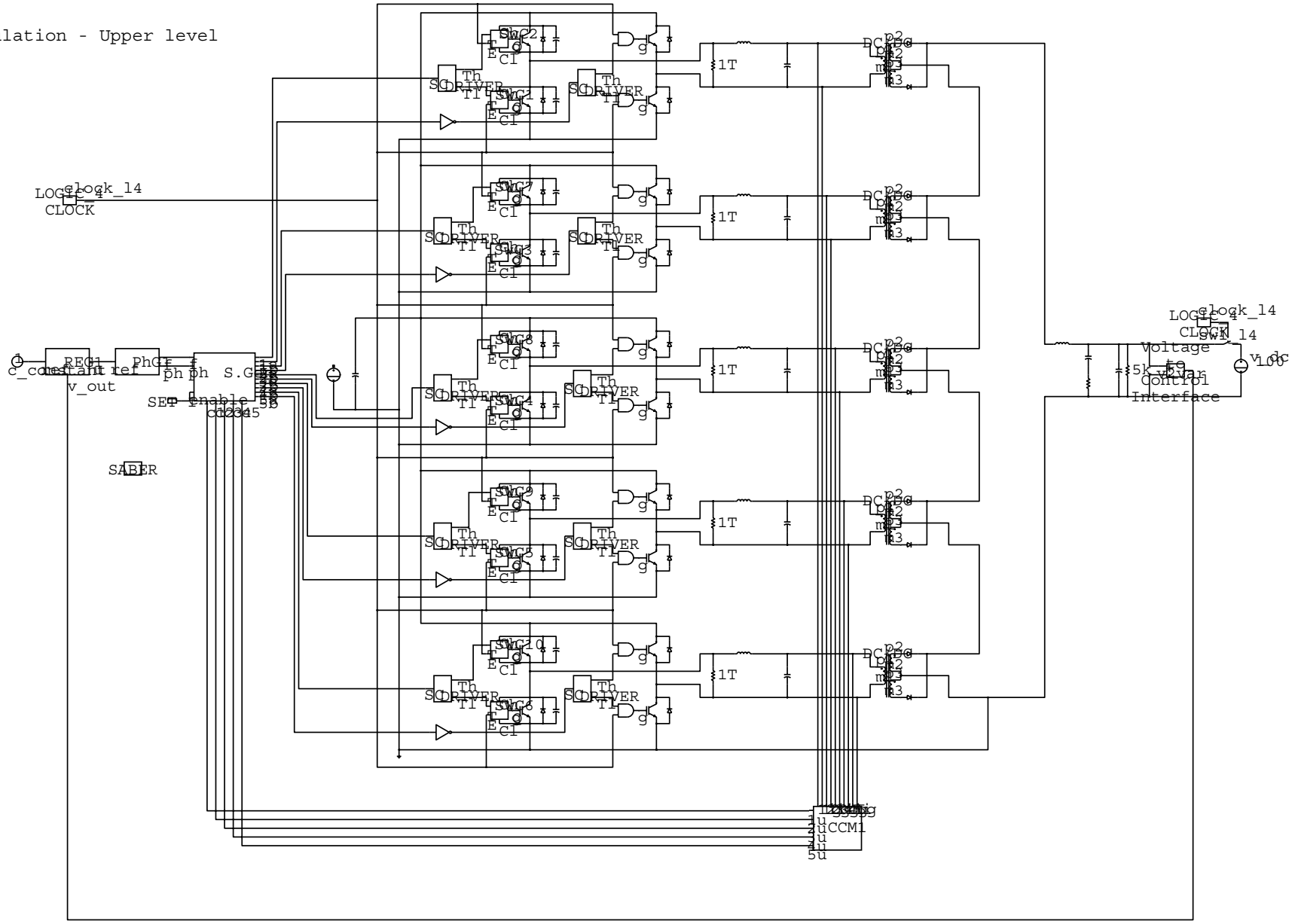


The step response indicates a much quicker system than the 40 us time constant observed in simulations. This is because converter saturation is included in this simulation.

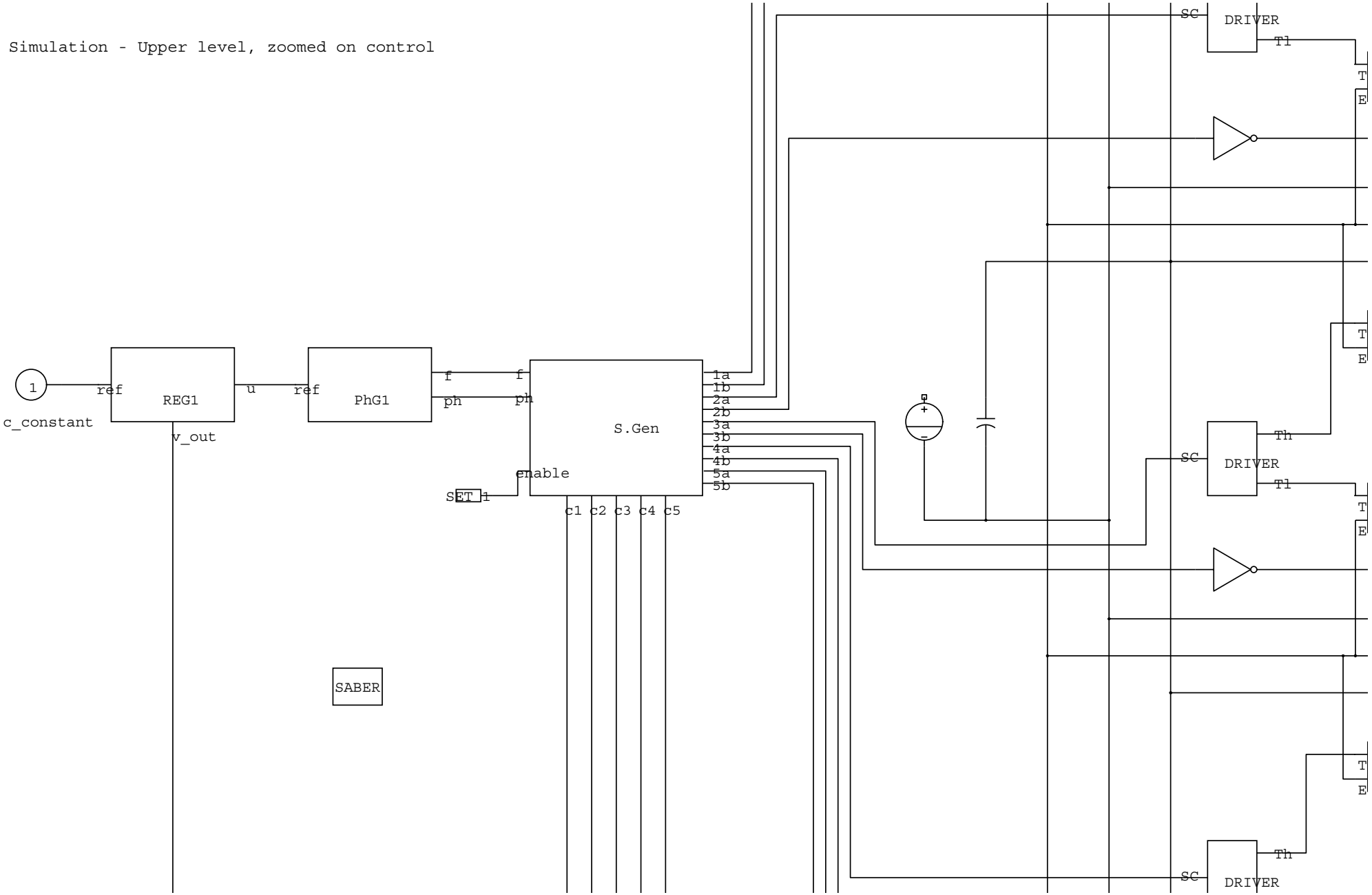
Appendix D

PRC Saber Simulation

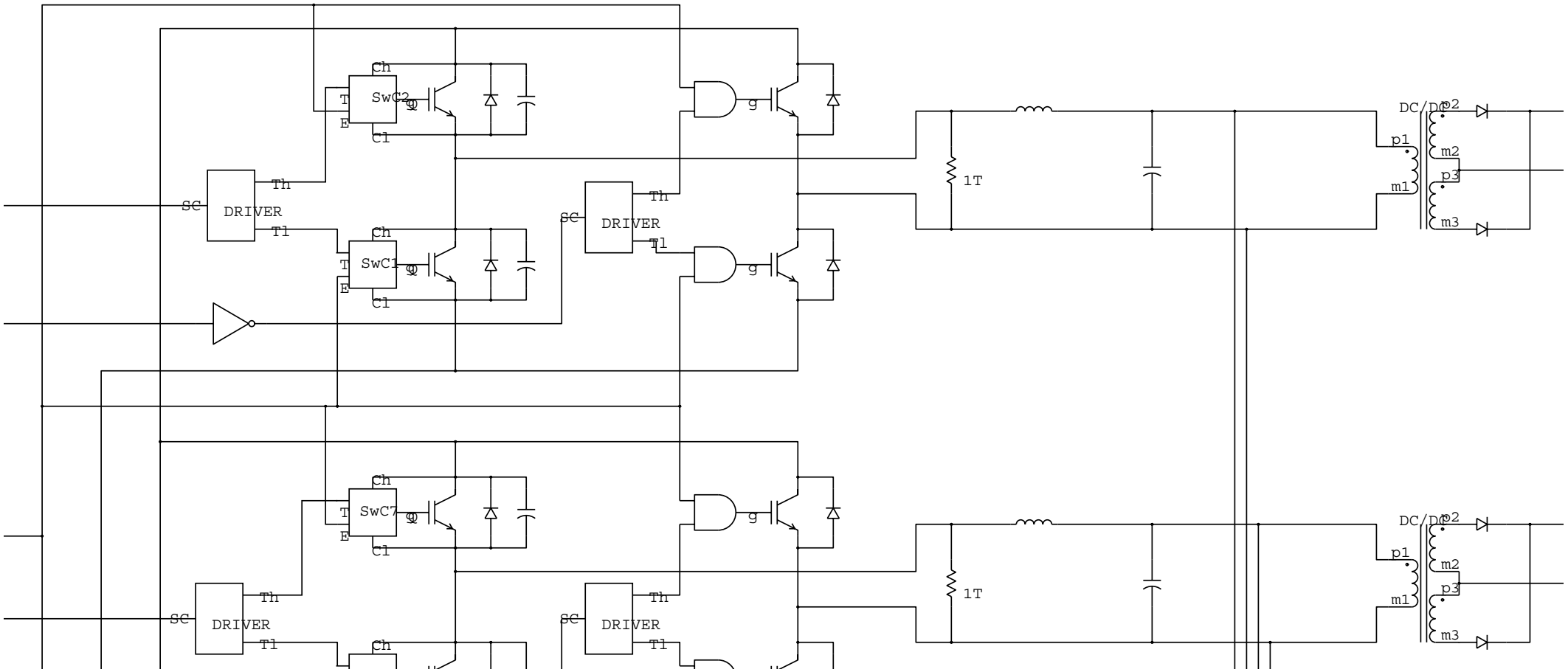
PRC Simulation - Upper level

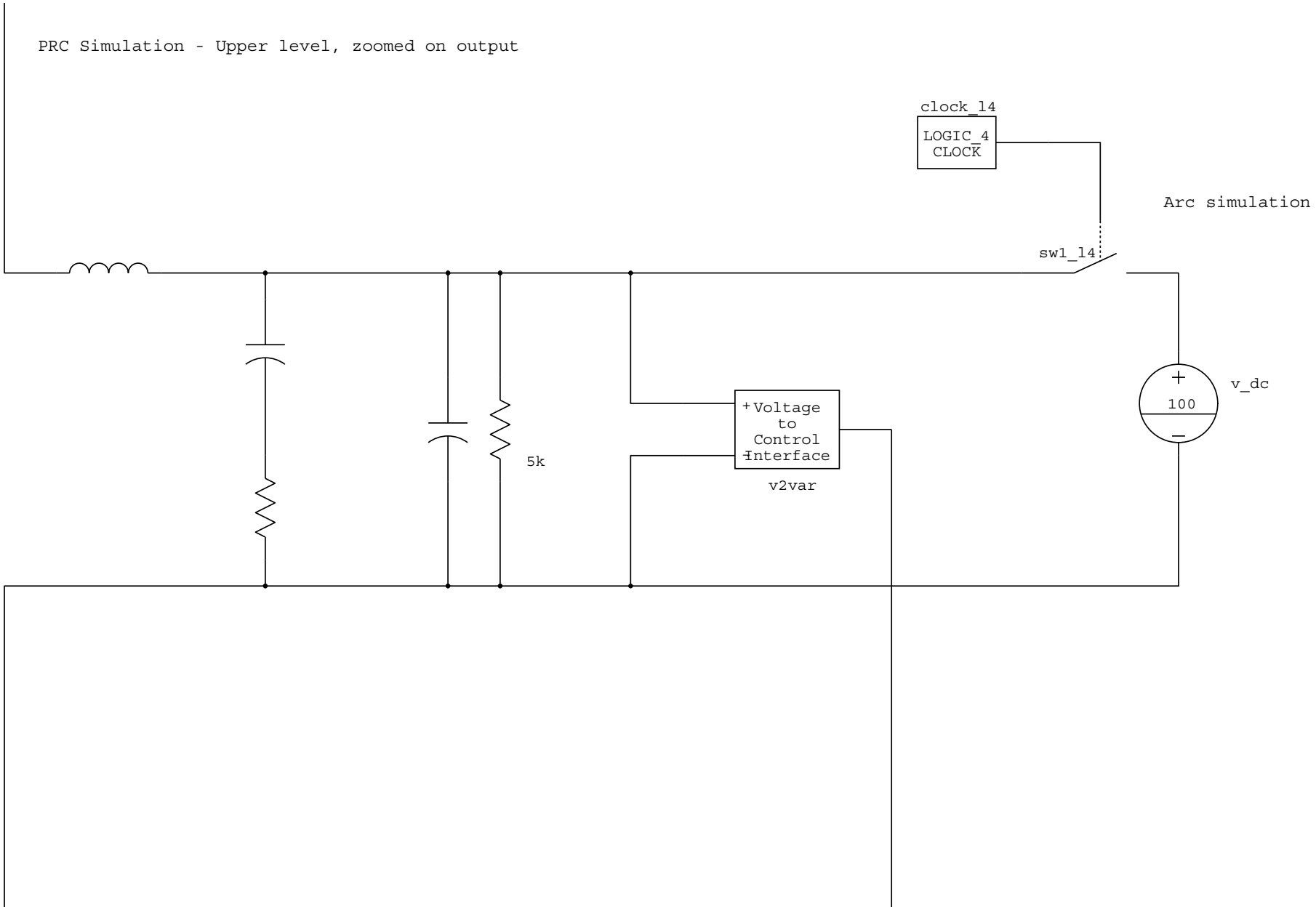


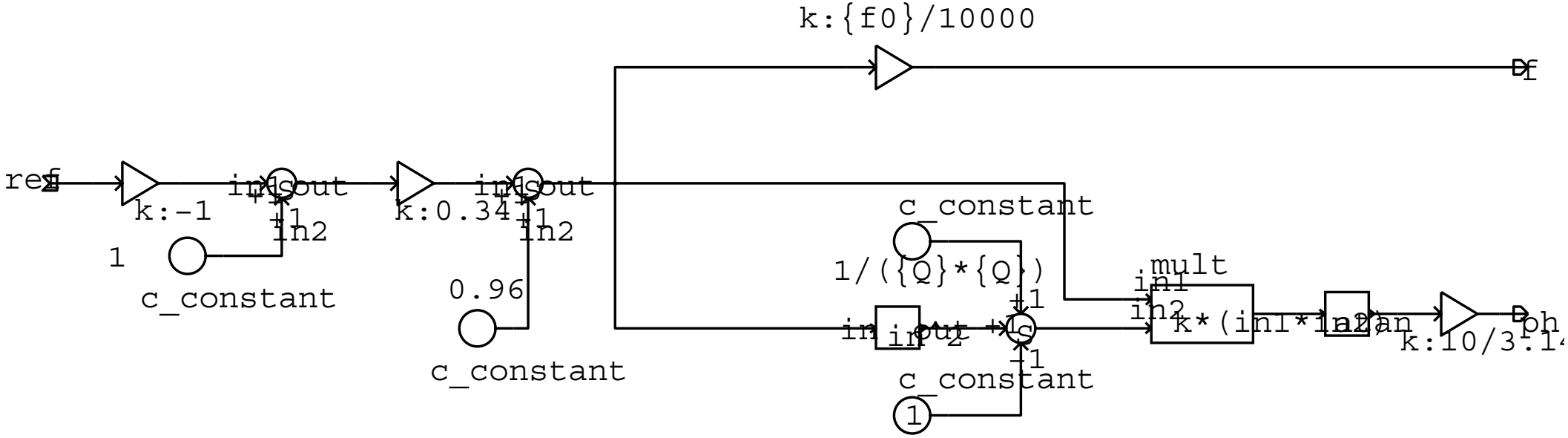
PRC Simulation - Upper level, zoomed on control

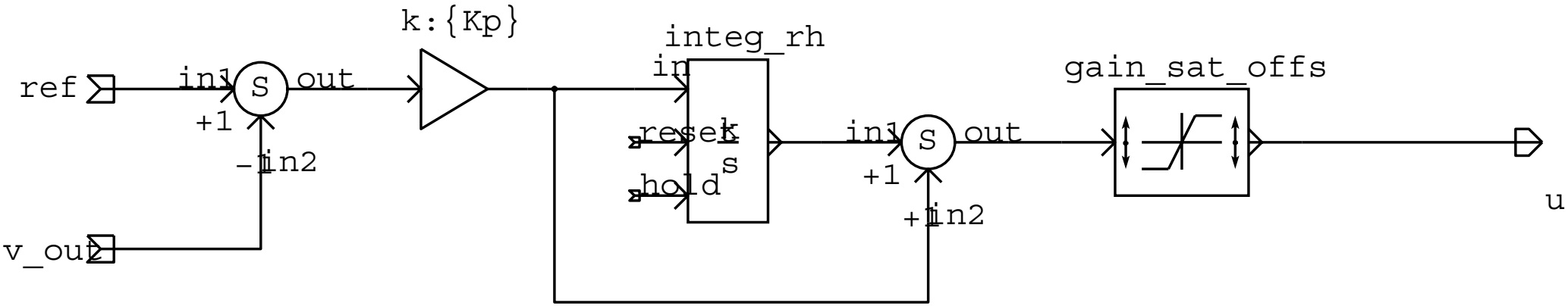


PRC Simulation - Upper level, zoomed on module 1



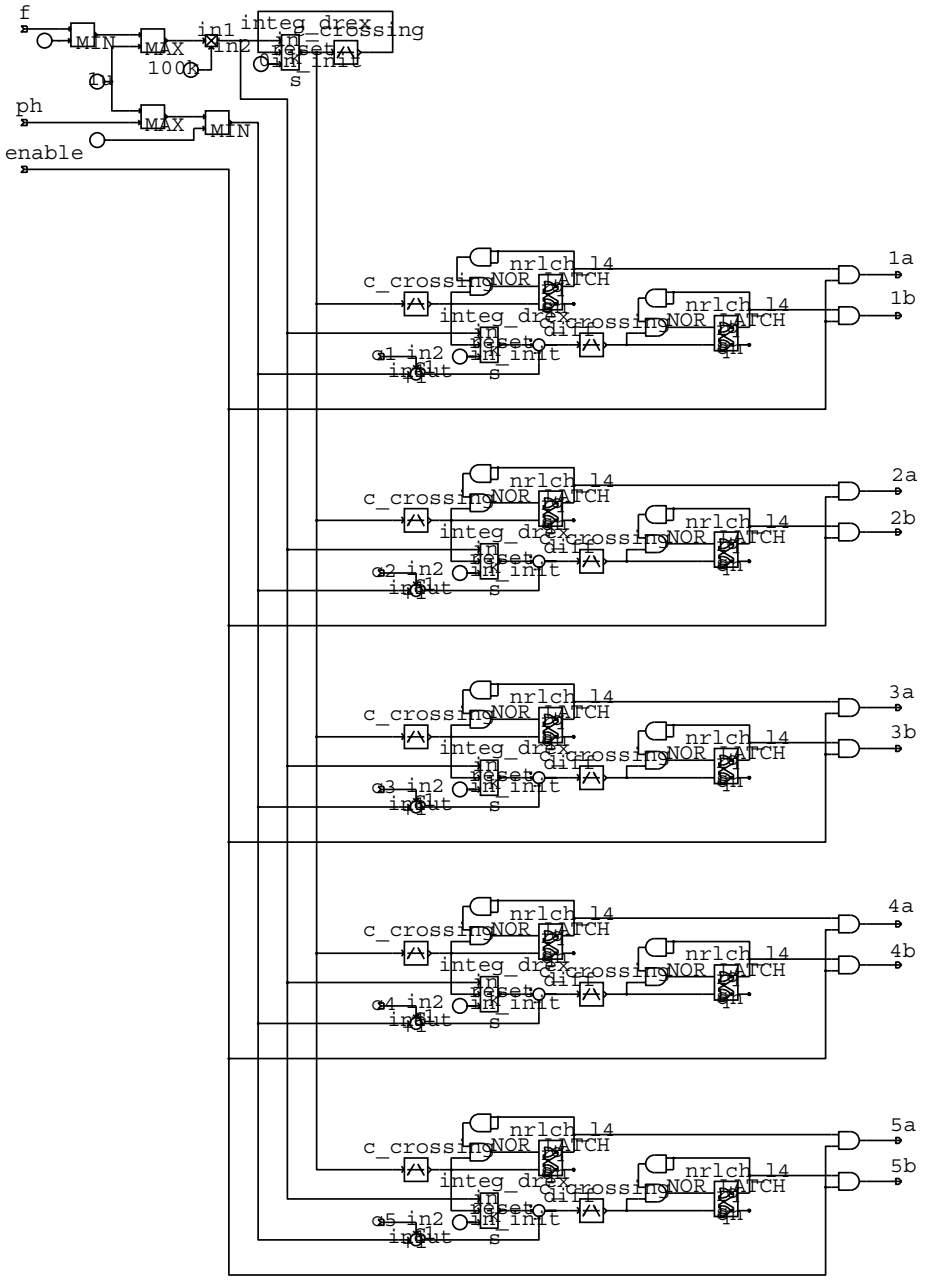

PRC Simulation - Upper level, zoomed on output
clock_14
LOGIC_4
CLOCK
Arc simulation
sw1_14
5k
+ Voltage
to
Control
Interface
v2var
+
100
−
v_dc


k:{f0}/10000
f
ref
k:-1
in1
out
+1
+1
in2
1
c_constant
k:0.34
in1
out
+1
+1
in2
0.96
c_constant
c_constant
1/({Q}*{Q})
in1
out
+1
+1
in2
c_constant
1
mult
in1
in2
k*(in1*in2)
k:10/3.1
ph

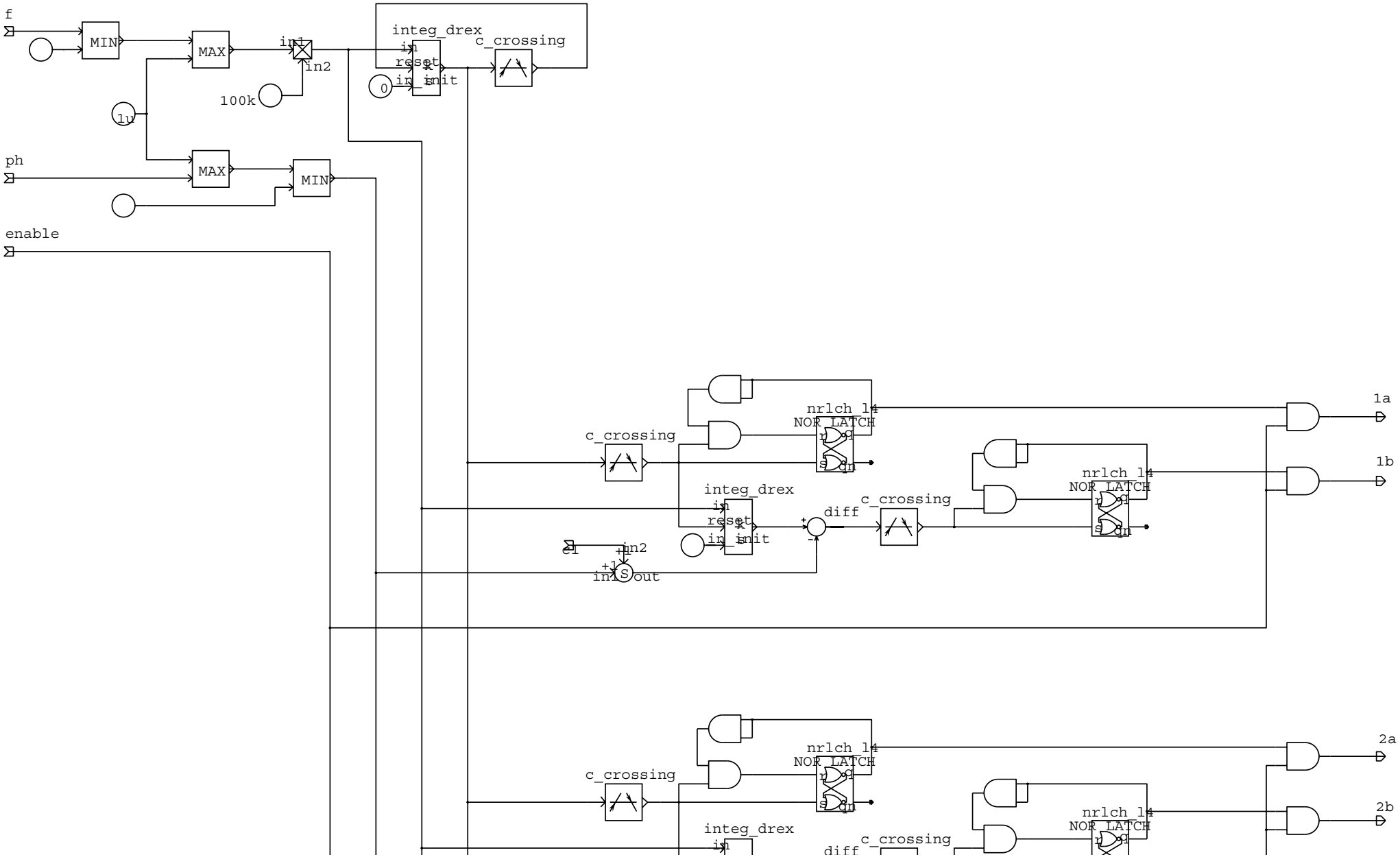

ref
v_out
in1
+1
S
out
-1
in2
k:{Kp}
integ_rh
in
reset
hold
k
s
in1
+1
S
out
-1
in2
gain_sat_offs
u

PRC Simulation -

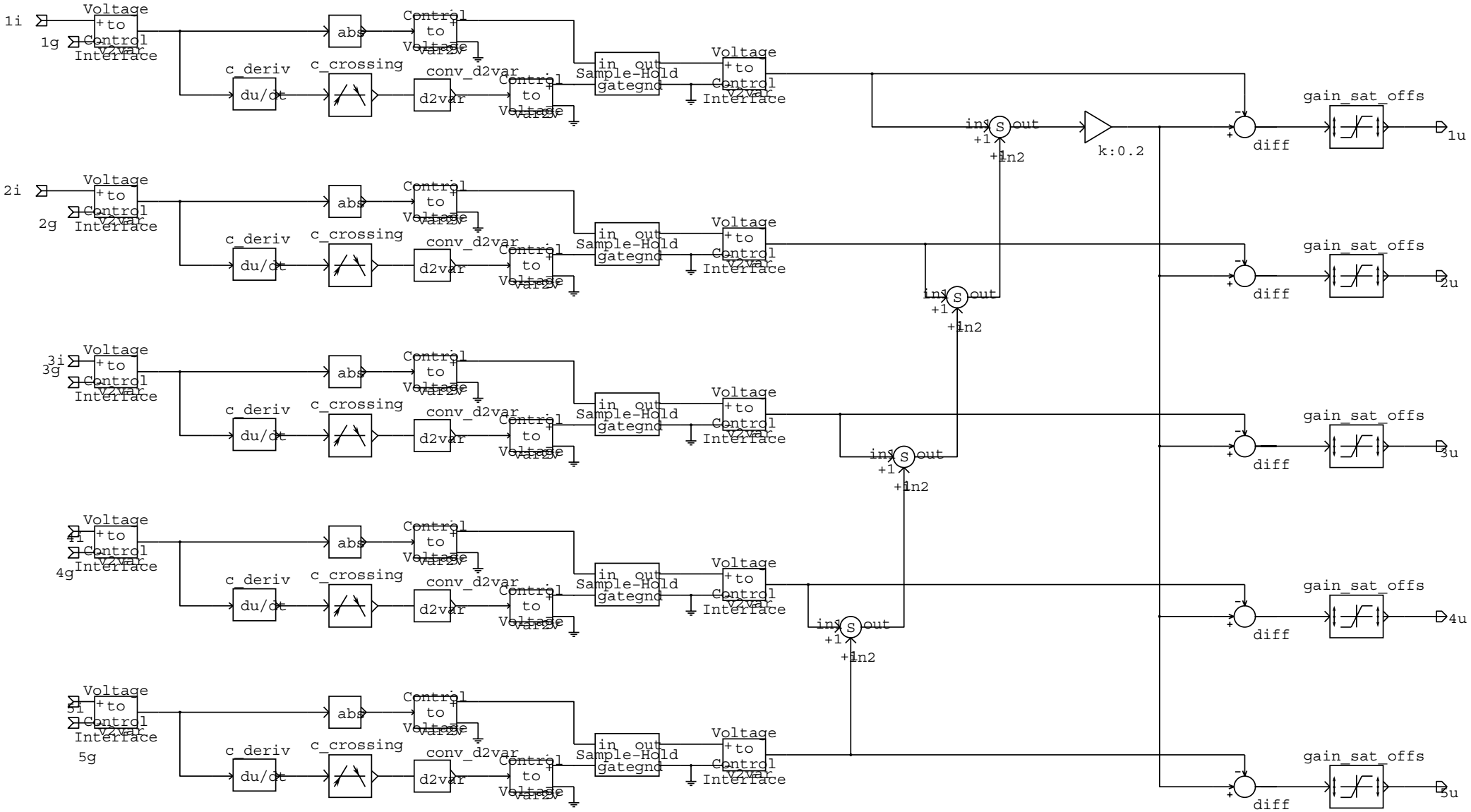
IGBT Firing signal block



PRC Simulation - IGBT Firing signal block, zoomed top



PRC Simulation - Balance control block



Appendix E

Mathematica Bouncer Scripts

Description

I nput

Idc = DC current def : 20
Iratio = Idc / I0 def : (1 / 2)
Vnom = Nominal pulse voltage
CES = Capacitive Energy Storage, def : 212 * 10^-6
Rload = Load equivalent referred to primary, def : 50
T = Pulse length, def : 800 us
Verr = Total error tolerance, def : 0.01
Corr = Unlinearity correction factor, def : 0.04

Other variables

(xa, ya) = First intersection point
α = Tolerance angel for liear area def : (π / 6)
β = Intersection angel referred to center circle
r2 = radius of inner circle
L = Bouncer inductor value, henry
C = Bouncer capacitor value farad
td = Timedelay between triggers
τ = Time constant for capacitor / load circuit
Vcomp = Required compensating voltage def : 10000
Null

Input data

```
T = 800 * 10^-6;
Idc = 200;
Iratio = 0.615;
Vnom = 10^4;
Verr = 0.008;
Rload = 50;
CES = 212 * .97 * 10^-6;
Corr = 1.04;
```

Functions

```
VpulseLin[t_] :=
  If[(t - Floor[t / 0.5] * 0.5) ≥ T, 0, Vnom + Vcomp / 2 - Vcomp / T * (t - Floor[t / 0.5] * 0.5)];

VpulseExp[t_] := If[(t - Floor[t / 0.5] * 0.5) ≥ T,
   0, (Vnom + Vcomp / 2) * E^(-(t - Floor[t / 0.5] * 0.5) / τ)];

VpulseSin[t_] :=
  If[(t - Floor[t / 0.5] * 0.5) ≥ T, 0, V0 * r2 * Sin[ω0 * (t - Floor[t / 0.5] * 0.5) - α]];

ϵ[al_] := -(Sin[al] / al * ArcCos[Sin[al] / al] - Sin[ArcCos[Sin[al] / al]]) / Sin[al];
```

Calculus

```
τ = Rload * CES;
Vcomp = Vnom (1 - E^(-T / τ)) * Corr;
α = alpha /. FindRoot[ϵ[alpha] * Vcomp / Vnom == Verr, {alpha, Pi / 4}];

(*Eq=Solve[{x^2+y^2==1,y==-Iratio-x*Tan[Pi/2-α]},{x,y}]*)
```

$$xa = \frac{-\text{Iratio}\,\text{Cot}[\alpha] + \sqrt{1 - \text{Iratio}^2 + \text{Cot}[\alpha]^2}}{1 + \text{Cot}[\alpha]^2};$$

```
ya = -Iratio - xa * Tan[Pi / 2 - α];
r2 = √(xa^2 + (ya + Iratio)^2);
β = ArcTan[Abs[ya] / Abs[xa]];
ω0 = 2 α / T;
V0 = Vcomp / (2 xa);
I0 = Idc / Iratio;
Lb = V0 / (ω0 I0);
Cb = I0 / (ω0 V0);
td = β / ω0;
Ipeak = (Iratio + r2) * I0;
```

Results

```
Print[""];
Print["Output:"];
Print["L: ", EngineeringForm[N[Lb]]];
Print["C: ", EngineeringForm[N[Cb]]];
Print["V₀: ", EngineeringForm[N[V0]]];
Print["I₀: ", EngineeringForm[N[I0]]];
Print[""];
Print["Ipeak: ", EngineeringForm[N[Ipeak]]];
Print["Vcomp: ", EngineeringForm[N[Vcomp]]];
Print[""];
Print["td: ", EngineeringForm[N[td]]];
Print["ω₀: ", EngineeringForm[N[ω0]]];
Print["f: ", EngineeringForm[N[ω0/(2π)]]];
Print["α: ", EngineeringForm[N[α*180/Pi]]];
Print[""];
Print["WC: ", EngineeringForm[N[(V0^2*Cb)/2]]];
Print["WL: ", EngineeringForm[N[(Ipeak^2*Lb)/2]]];
Print[""];
```

```
Output:

L: 753.549×10^-6

C: 153.849×10^-6

V₀: 719.719

I₀: 325.203


Ipeak: 390.636

Vcomp: 778.502


td: 340.273×10^-6

ω₀: 2.93695×10^3

f: 467.43

α: 67.3099


WC: 39.8466

WL: 57.4946
```

Phase plane plot

```
Show[Graphics[ {
    {
     RGBColor[1, 0, 0],
     Circle[{0, 0}, 1, {-Pi/2 + (Pi/2 - β), 3/2 Pi - (Pi/2 - β)}],
     Dashing[{0.005, 0.015}],
     Circle[{0, 0}, 1, {3/2 Pi - (Pi/2 - β), 3/2 Pi + (Pi/2 - β)}],
     {PointSize[.015], Point[{0, 0}]},
     {PointSize[.015], Point[{1, 0}]},
     Text["β", {.3, -.1}],
     Text["Start", {.9, .05}],
     Text["Main trig", {xa + .2, ya}],
     Circle[{0, 0}, 0.25, {-β, 0}],
     Line[{{0, 0}, {xa * 1.1, ya * 1.1}}]
    },
    {
     RGBColor[0, 0, 1],
     Circle[{0, -Iratio}, r2, {3/2 Pi - α, 3/2 Pi + α}],
     Dashing[{0.005, 0.015}],
     Circle[{0, -Iratio}, r2, {-Pi/2 + α, 3/2 Pi - α}],
     Circle[{0, -Iratio}, 0.25, {-Pi/2, -Pi/2 + α}],
     Line[{{0, -Iratio}, {xa, ya}}],
     Line[{{0, -Iratio}, {-xa, ya}}],
     {PointSize[.015], Point[{0, -Iratio}]},
     Text["α", {.05, -Iratio - .2}],
     Text["Idc", {.08, -Iratio}]
    },
    {
     RGBColor[0, 0, 0],
     Text["I₀√(L/C) ", {.15, 1.12}],
     Text["V₀", {1.2, -.05}]
    }
   },
   PlotRange → {{-1.2, 1.25}, {-1.3, 1.25}},
   Axes → Automatic,
   AspectRatio → Automatic
  ]];
```

Flattop visualisation

```
Plot[{VpulseExp[t] + VpulseSin[t], 10050, 9950}, {t, -.0001, .001},
  PlotRange → {{-.0001, .001}, {9900, 10100}}, AxesOrigin → {-.0001, Automatic}];
```

Inductance requirements

```
T_cycle = .500;
T_bouncer = 1 / (ω0 / (2 Pi));
I_L = Sqrt[1 / T_cycle ∫_0^T_bouncer (Ipeak Sin[ω0 t])^2 dt];

Print["Inductance:"];
Print["L: ", EngineeringForm[N[Lb]]];
Print["Î_L: ", EngineeringForm[N[Ipeak]]];
Print["I_L: ", EngineeringForm[N[I_L]]];
```

```
Inductance:
L: 753.549×10^-6
Î_L: 390.636
I_L: 18.0682
Inductance:
L: 849.644×10^-6
Î_L: 369.075
I_L: 17.0709
```

α - accuracy

```
Plot[Sin[t], {t, -Pi/2, Pi/2},
  Ticks → {{-Pi/2, -Pi/3, -Pi/6, Pi/6, Pi/3, Pi/2}, Automatic},
  TextStyle → {FontFamily → "cmr8"},
  Epilog → {
    Text["y = Sin (x)", {Pi/8, .8}],
    Red,
    Dashing[{}],
    Line[{{-Pi/6, Sin[-Pi/6]}, {Pi/6, Sin[Pi/6]}}],
    Dashing[{0.01, 0.025}],
    Line[{{Pi/6, Sin[Pi/6]}, {Pi/6, 0}}],
    Text["α1", {Pi/6 - .1, .1}],

    Green,
    Dashing[{}],
    Line[{{-Pi/3, Sin[-Pi/3]}, {Pi/3, Sin[Pi/3]}}],
    Dashing[{0.01, 0.025}],
    Line[{{Pi/3, Sin[Pi/3]}, {Pi/3, 0}}],
    Text["α2", {Pi/3 - .1, .1}],

    Blue,
    Dashing[{}],
    Line[{{-Pi/2, Sin[-Pi/2]}, {Pi/2, Sin[Pi/2]}}],
    Dashing[{0.01, 0.025}],
    Line[{{Pi/2, Sin[Pi/2]}, {Pi/2, 0}}],
    Text["α3", {Pi/2 - .1, .1}]
   }
 ];

Plot[100 * ϵ[al] * Vcomp / Vnom, {al, 0, Pi/2},
  TextStyle → {FontFamily → "cmr8"}, AxesLabel → {"α", "ϵ / [%]"},
  Epilog → {
    Dashing[{0.01, 0.025}],
    Red,
    Line[{{0, 1}, {1.65, 1}}]
   }
 ];
```

Inductance energy

```
Lb3D[Iratio_] := (Vcomp / (2 (-Iratio Cot[α] + Sqrt[1 - Iratio^2 + Cot[α]^2]) / (1 + Cot[α]^2))) / (ω0 I0);

Ipeak3D[Iratio_] := (Iratio + Sqrt((((-Iratio Cot[α] + Sqrt[1 - Iratio^2 + Cot[α]^2]) / (1 + Cot[α]^2))^2 +
        ((-Iratio - (((-Iratio Cot[α] + Sqrt[1 - Iratio^2 + Cot[α]^2]) / (1 + Cot[α]^2)) * Tan[Pi / 2 - α]) + Iratio)^
         2)) * Idc / Iratio;

Plot[.5 * Lb3D[a] * Ipeak3D[a]^2, {a, 0.1, 1},
  TextStyle → {FontFamily → "cmr8"},
  AxesLabel → {"I_ratio", "W_L / [J]"}
 ];
Plot[Lb3D[a] * 1000, {a, 0.1, 1}, PlotRange → {Automatic, {0, Lb * 10000}},
  TextStyle → {FontFamily → "cmr8"},
  AxesLabel → {"I_ratio", "L / [mH]"}];
```

Transient analysis

Natural charge cycle

```
Clear[R1old];
PktA = {R1old Cos[-β], R1old Sin[-β]};
R2 = Sqrt[PktA[[1]]^2 + (PktA[[2]] + Iratio)^2];
γ = π / 2 + ArcSin[(-Iratio - PktA[[2]]) / R2];
PktB = {R2 Cos[π / 2 - 2 α - γ], R2 Sin[π / 2 - 2 α - γ] - Iratio};
R1new = Sqrt[PktB[[1]]^2 + PktB[[2]]^2];
R1next[R1last_] := R1new /. R1old → R1last;


R1 = 0;
Show[
  Graphics[
   {
    {
     RGBColor[0, 0, 0],
     Text["I_0 Sqrt[L/C] ", {.15, 1.12}],
     Text["V_0", {1.2, -.05}],
     RGBColor[0, 0, 1],
     {PointSize[.015], Point[{0, -Iratio}]},
     Text["I_dc", {.08, -Iratio}],
     RGBColor[1, 0, 0],
     {PointSize[.015], Point[{0, 0}]}
    },
    Table[
     {
      PktA = {R1 Cos[-β], R1 Sin[-β]};
      R2 = Sqrt[PktA[[1]]^2 + (PktA[[2]] + Iratio)^2];
      γ = π / 2 + ArcSin[(-Iratio - PktA[[2]]) / R2];
      PktB = {R2 Cos[π / 2 - 2 α - γ], R2 Sin[π / 2 - 2 α - γ] - Iratio};

      RGBColor[1, 0, 0],
      Circle[{0, 0}, R1, {-β, 0}],
      RGBColor[0, 0, 1],
      Circle[{0, -Iratio}, R2, {-γ - 2 α + π / 2, -γ + π / 2}],

      R1 = Sqrt[PktB[[1]]^2 + PktB[[2]]^2];
      λ = ArcSin[PktB[[1]] / R1] + 3 π / 2;

      RGBColor[1, .5, .5],
      Circle[{0, 0}, R1, {0, λ}]
     },
     {k, 0, 200, 1}
    ]
   },
   PlotRange → {{-1.2, 1.25}, {-1.3, 1.25}},
   Axes → Automatic,
   AspectRatio → Automatic
  ]
 ];
```

Forced charge cycle

```
R1 = 0;
Show[
  Graphics[
   {
    {
     RGBColor[0, 0, 0],
     Text["I₀√(L/C)", {.15, 1.12}],
     Text["V₀", {1.2, -.05}],
     RGBColor[0, 0, 1],
     {PointSize[.015], Point[{0, -Iratio}]},
     Text["I_dc", {.08, -Iratio}],
     RGBColor[1, 0, 0],
     {PointSize[.015], Point[{0, 0}]}
    },
    Table[
     {
      PktA = {R1 , 0};
      R2 = Sqrt[PktA[[1]]^2 + (PktA[[2]] + Iratio)^2];
      γ = π / 2 + ArcSin[(-Iratio - PktA[[2]]) / R2];
      PktB = {R2 Cos[π / 2 - 2 α - γ], R2 Sin[π / 2 - 2 α - γ] - Iratio};

      RGBColor[0, 0, 1],
      Circle[{0, -Iratio}, R2, {-γ - 2 α + π / 2, -γ + π / 2}],

      R1 = Sqrt[PktB[[1]]^2 + PktB[[2]]^2];
      λ = ArcSin[PktB[[1]] / R1] + 3 π / 2;

      RGBColor[1, .7, .7],
      Circle[{0, 0}, R1, {0, λ}]
     },
     {k, 0, 5, 1}
    ]
   },
   PlotRange → {{-1.2, 1.25}, {-1.3, 1.25}},
   Axes → Automatic,
   AspectRatio → Automatic
  ]
 ];
```

Full charge on one natural cycle

```
R1FNC =
  Sqrt[IratioFNC^2 * (1 + Sin[2 αFNC - π / 2])^2 + IratioFNC^2 * Cos[2 αFNC - π / 2]^2];

Result = IratioFNC /. Solve[R1FNC == 1, {IratioFNC}];
IratioOptFnc[alphavar_] := Result[[2]] /. αFNC → alphavar;

Plot[IratioOptFnc[x], {x, Pi / 6, Pi / 2},
  AxesOrigin → {0, .5}, PlotRange → {{0, 2}, {.5, 1}},
  Ticks → {{π / 12, 2 π / 12, 3 π / 12, 4 π / 12, 5 π / 12, 6 π / 12}, Automatic},
  AxesLabel → {"α", "Iratio"}];
```

Current graphs

```
IpeakCG = 500;
iLCG[t_] :=
  If[(t - Floor[t / 0.5] * 0.5) ≥ 2 π / ω0, 0, IpeakCG * Sin[ω0 * (t - Floor[t / 0.5] * 0.5)]];

Plot[iLCG[t], {t, 0, .01}, PlotLabel → "Inductor current - Close view",
  AxesLabel → {"t / sek", "i / A"}, Ticks → {Automatic, {-500, -250, 0, 250, 500}}];

Plot[iLCG[t], {t, -0.01, 1.1}, PlotLabel → "Inductor current - Overview",
  AxesLabel → {"t / sek", "i / A"}, Ticks → {Automatic, {-500, -250, 0, 250, 500}},
  AxesOrigin → {-.01, 0}, PlotPoints → 100];
```

Control Analysis

```
R1 = .9;
βca = β * .93;

Show[
  Graphics[
   {
    {
     RGBColor[0, 0, 0],
     Text["I₀√(L/C)", {0.2, 0.244783}],
     Text["V₀", {1.15, -.1}],
     RGBColor[0, 0, 1],
     {PointSize[.015], Point[{0, -Iratio}]},
     Text["I_Load", {0.15, -0.548215}],
     RGBColor[1, 0, 0],
     {PointSize[.015], Point[{0, 0}]}
    },
    Table[
     {
      PktA = {R1 Cos[-βca], R1 Sin[-βca]};
      R2 = Sqrt[PktA[[1]]^2 + (PktA[[2]] + Iratio)^2];
      γ = π / 2 + ArcSin[(-Iratio - PktA[[2]]) / R2];
      PktB = {R2 Cos[π / 2 - 2 α - γ], R2 Sin[π / 2 - 2 α - γ] - Iratio};

      RGBColor[1, 0, 0],
      Circle[{0, 0}, R1, {-βca, 0}],
      RGBColor[0, 0, 1],
      Circle[{0, -Iratio}, R2, {-γ - 2 α + π / 2, -γ + π / 2}],

      R1 = Sqrt[PktB[[1]]^2 + PktB[[2]]^2];
      λ = ArcSin[PktB[[1]] / R1] + 3 π / 2;

      RGBColor[1, 0, 0],
      Circle[{0, 0}, R1, {Pi, λ}]
     },
     {k, 0, 0, 1}
    ],
    {
```

```
    Black,
    {PointSize[.015], Point[PktA]},
    {PointSize[.015], Point[PktB]},
    Text["P₁", {0.631544, -0.8}],
    Text["P₂", {-0.55, -1.00}],

    Dashing[{0.005, 0.015}],
    Line[{{0, -Iratio}, {PktA[[1]], -Iratio}}],
    Line[{{PktA[[1]], -Iratio}, PktA}],
    Text["γ", {0.40764, -0.653}],

    Circle[{0, -Iratio}, 0.2, {Pi / 2 - 2 α - γ + 2 Pi, 3 Pi / 2}],
    Text["δ", {-0.05, -0.73}],

    Red,
    Line[{{0, 0}, PktA}],
    Circle[{0, 0}, 0.3, {-βca, 0}],
    Text["β", {0.192825, -0.072}],
    Text["V₁", {0.89268, 0.0725715}],
    Text["V₂", {-1.03075, 0.0811201}],

    Blue,
    Circle[{0, -Iratio}, 0.28, {Pi / 2 - 2 α - γ + 2 Pi, Pi / 2 - 2 α - γ + 2 Pi + 2 α}],
    Line[{{0, -Iratio}, PktA}],
    Line[{PktB, {0, -Iratio}}],
    Text["2α", {0.1, -0.748092}]
   }
  },
  PlotRange → {{-1.2, 1.25}, {-1.3, 0.5}},
  Ticks → {{-1, -.5, .5, 1}, {-1, -.5}},
  Axes → Automatic,
  AspectRatio → Automatic,
  TextStyle → {FontFamily → "cmr8"}
 ]
];
```

Export

```
Export["G:\\Users\\j\\jonasb\\02_Master\\Thesis\\MathematicaOUT\\oi.eps",
 %%, ImageSize → 400]
```

```
G:\Users\j\jonasb\02_Master\Thesis\MathematicaOUT\oi.eps
```

Appendix F

Mathematica PRC Scripts

Input

```
γ = π / 1.18;
J = 0.65;
```

Definition of variables

```
ω0 = 1;

Rad = Range[4];
Ang = Partition[Range[8], 2];
Cent = {{1, -J}, {1, J}, {-1, J}, {-1, -J}};
CurveCol =
  {RGBColor[1, 0, 0], RGBColor[0, 1, 0], RGBColor[0, 0, 1], RGBColor[1, 0, 1]};
```

Definition of functions

```
Repetetive[t_, T_] :=
  t - T * Floor[t / T];

S[t_] :=
  Repetetive[t, 2 γ * ω0];

VPlot[t_] :=
     Rad[1] * Cos[Ang[1, 1] - ω0 t] + Cent[1, 1]          ω0 t ≤ α
    Rad[2] * Cos[Ang[2, 1] - ω0 t + α] + Cent[2, 1]      α ≤ ω0 t ≤ α + β
   Rad[3] * Cos[Ang[3, 1] - ω0 t + α + β] + Cent[3, 1]   α + β ≤ ω0 t ≤ 2 α + β
  Rad[4] * Cos[Ang[4, 1] - ω0 t + 2 α + β] + Cent[4, 1]     2 α + β ≤ ω0 t

IPlot[t_] :=
     Rad[1] * Sin[Ang[1, 1] - ω0 t] + Cent[1, 2]          ω0 t ≤ α
    Rad[2] * Sin[Ang[2, 1] - ω0 t + α] + Cent[2, 2]      α ≤ ω0 t ≤ α + β
   Rad[3] * Sin[Ang[3, 1] - ω0 t + α + β] + Cent[3, 2]   α + β ≤ ω0 t ≤ 2 α + β
  Rad[4] * Sin[Ang[4, 1] - ω0 t + 2 α + β] + Cent[4, 2]     2 α + β ≤ ω0 t

HPlot[t_] :=
   1       ω0 t ≤ α
   1    α ≤ ω0 t ≤ α + β
  -1  α + β ≤ ω0 t ≤ 2 α + β
  -1    2 α + β ≤ ω0 t

MT[gamma_] := 2 / gamma (-ArcCos[Cos[gamma / 2] + J Sin[gamma / 2]] -
      Sin[-ArcCos[Cos[gamma / 2] + J Sin[gamma / 2]]] / Cos[gamma / 2]) - M_target;
MTD2 = D[MT[gamma2], gamma2];
MTD[gamma_] := MTD2 /. gamma2 → gamma;
```

Calculations

$$\varphi = \begin{cases} -\text{ArcCos}[\text{Cos}[\gamma/2] + J\,\text{Sin}[\gamma/2]] & \gamma < \pi \\ \text{ArcCos}[\text{Cos}[\gamma/2] + J\,\text{Sin}[\gamma/2]] & \gamma \geq \pi \end{cases};$$

$$\alpha = \frac{\gamma}{2} - \varphi;$$

$$\beta = \frac{1}{2}(\gamma + 2\varphi);$$

```
JL1 = -Sin[φ] / Cos[γ / 2];
JL0 = -(J^2 - 1) Tan[γ / 2];
MC0 = -J Sin[φ] / Cos[γ / 2];
M = (2 / γ) (φ - Sin[φ] / Cos[γ / 2]);

Rad[[{1, 2}]] = {Sqrt[1 + (-J - JL1)^2], Sqrt[1 + (+J - JL1)^2]};
Rad[[{3, 4}]] = Rad[[{1, 2}]];
PointPos = {{MC0, JL0}, {0, JL1}, -{MC0, JL0}, -{0, JL1}};
PointPosLabel = {{-1, 1}, {-1, 1}, {1, -1}, {1, -1}};

MC1 = 1 + Sqrt[r2^2 - (JL1 - J)^2];

Ang[[{1, 2}]] = {
   {ArcTan[(JL0 - J) / (1 + MC0)] + Pi, ArcCos[(JL1 + J) / Rad[[1]] + Pi / 2},
   {Pi - ArcSin[(JL1 - J) / Rad[[2]], Pi - ArcSin[(JL1 - J) / Rad[[2]] - β}
  };
Ang[[{3, 4}]] = Ang[[{1, 2}]] - Pi;
```

$$\text{RadMax} = \begin{cases} \text{Rad}[[1]] & \text{Rad}[[1]] \geq \text{Rad}[[2]] \\ \text{Rad}[[2]] & \text{Rad}[[1]] < \text{Rad}[[2]] \end{cases} + .2;$$

```
PlRng = {RadMax, RadMax / J};
```

Phaseplane plot

```
Show[
  Graphics[
   {Table[{
      CurveCol[[i]],
      PointSize[0.02],
      Point[Cent[[i]]],
      Circle[Cent[[i]], Rad[[i]], {Ang[[i, 2]], Ang[[i, 1]]}]}]
     , {i, 4}
    ],
    {RGBColor[0, 0, 0],
     Text["I0√(L/C) ", {.75, J PlRng[[2]] - .45}],
     Text["V0", {PlRng[[1]] - .5, .35}]}},
   PlotRange → {{-PlRng[[1]], PlRng[[1]]}, {-J PlRng[[2]], J PlRng[[2]]}},
   Ticks → {Automatic, {{-6 J, "-6J"}, {-5 J, "-5J"},
      {-4 J, "-4J"}, {-3 J, "-3J"}, {-2 J, "-2J"}, {-J, "-J"}, {J, "J"},
      {2 J, "2J"}, {3 J, "3J"}, {4 J, "4J"}, {5 J, "5J"}, {6 J, "6J"}}},
   Axes → Automatic,
   AspectRatio → Automatic
  ]
 ];
```

Phaseplane plot with references

```
(Pi / 1.1 - J = 0.8)

Show[
  Graphics[
   {Table[{
      CurveCol[[i]],
      PointSize[0.01],
      Point[Cent[[i]]],
      Circle[Cent[[i]], Rad[[i]], {Ang[[i, 2]], Ang[[i, 1]]}],
      Text["c" <> ToString[i], {Cent[[i, 1]] + 0.2, Cent[[i, 2]]}]
     }
     , {i, 4}
    ],
    {Black,
     Text["i_L", {.35, J PlRng[[2]] - .45}],
     Text["v_C", {PlRng[[1]] - .5, .30}],
     Text[" ^n I_0=" <> ToString[J], {1.70, -2.5}],
     Text[" ^n f_s=" <> ToString[N[Round[100 * π / γ] / 100]], {1.7092, -2.15}],
     Dashing[{0.01, 0.025}],
     Gray,
     Line[1.2 {{-MC0, -JL0}, {MC0, JL0}}],

     Red,
     Line[{Cent[[1]], {-MC0, -JL0}}],
     Line[{Cent[[1]], {0, JL1}}],
     Circle[Cent[[1]], 0.8, {Ang[[1, 2]], Ang[[1, 1]]}],
     Text["α", {0.557572, -0.607134}],
     Text["r_1", {0.805382, 0.483229}],

     Green,
     Line[{Cent[[2]], {MC0, JL0}}],
     Line[{Cent[[2]], {0, JL1}}],
     Circle[Cent[[2]], 0.8, {Ang[[2, 2]], Ang[[2, 1]]}],
     Text["β", {0.904506, 1.25}],
     Text["r_2", {0.45, 1.8}],

     Table[{
       Black,
       Point[PointPos[[i]]],
       Text["p" <> ToString[i], (PointPos + PointPosLabel * 0.15)[[i]]]
      }, {i, 4}
     ]
    }},
   PlotRange → {{-PlRng[[1]], PlRng[[1]]}, {-J PlRng[[2]], J PlRng[[2]]}},
   Ticks → {Automatic, {{-6 J, "-6^n I_0"}, {-5 J, "-5^n I_0"}, {-4 J, "-4^n I_0"},
      {-3 J, "-3^n I_0"}, {-2 J, "-2^n I_0"}, {-J, "-^n I_0"}, {J, " ^n I_0"},
      {2 J, "2^n I_0"}, {3 J, "3^n I_0"}, {4 J, "4^n I_0"}, {5 J, "5^n I_0"}, {6 J, "6^n I_0"}}},
   Axes → Automatic,
   AspectRatio → Automatic,
   TextStyle → {FontFamily → "cmr8", FontSize → 10}
  ]
 ];
```

Boundary conditions

```
Fvec = {0.5, 0.6, 0.65, 0.7, 0.8, 0.9, 1, 1.1, 1.2, 1.3, 1.5, 2};
FPos = {{0.85, 2.87}, {0.62914, 2.84711}, {0.379992, 2.65515}, {0.278298, 2.17522},
  {0.218976, 1.62674}, {0.202549, 1.2947}, {2.87149, 1.10}, {2.43929, 0.570918},
  {1.75, 0.40}, {1, 0.200693}, {0.52, 0.18}, {0.142706, 0.173269}};
PlotVec = Range[{Length[Fvec], Length[Fvec]}];
For[k = 1, k ≤ Length[Fvec],
 γbc = π / If[Fvec[[k]] == 0.5 || Fvec[[k]] == 1, Fvec[[k]] + 0.000001, Fvec[[k]]];
 PlotVec[[1, k]] = ParametricPlot[{2 / γbc * (φ - Sin[φ] / Cos[γbc / 2]),
    (Cos[φ] - Cos[γbc / 2]) / Sin[γbc / 2]}, {φ, If[γbc ≥ Pi, -π, -1] *
     ArcCos[1/2 Sin[γbc/2]] (2 Cot[γbc/2] - Sin[γbc] + Sqrt[4 Sin[γbc/2]^2 + Sin[γbc]^2])],
    If[γbc ≥ Pi, 1, π] * ArcCos[1/2 Sin[γbc/2]]
        (2 Cot[γbc/2] - Sin[γbc] + Sqrt[4 Sin[γbc/2]^2 + Sin[γbc]^2])]
   },
   PlotPoints → 1000, PlotRange → {{0, 3}, {0, 3}}, PlotStyle → Red];

 PlotVec[[2, k]] =
  ParametricPlot[{If[γbc ≥ π / 0.54, 10, 0] + 2 / γbc * (φ - Sin[φ] / Cos[γbc / 2]),
    (Cos[φ] - Cos[γbc / 2]) / Sin[γbc / 2]}, {φ, If[γbc ≥ Pi, 1.01, -4 π] *
     ArcCos[1/2 Sin[γbc/2]] (2 Cot[γbc/2] - Sin[γbc] + Sqrt[4 Sin[γbc/2]^2 + Sin[γbc]^2])],
    If[γbc ≥ Pi, π, -ArcCos[1/2 Sin[γbc/2]]
        (2 Cot[γbc/2] - Sin[γbc] + Sqrt[4 Sin[γbc/2]^2 + Sin[γbc]^2])]]
   },
   PlotPoints → 1000, PlotRange → {{0, 3}, {0, 3}}];
 k++;
]

Show[
  Graphics[{
    Red,
    Table[PlotVec[[1, i, 1]],
     {i, 1, Length[Fvec]}],
    Black,
    Table[PlotVec[[2, i, 1]],
     {i, 1, Length[Fvec]}],
    RGBColor[0, 0.5, 0],
    Table[Text[Fvec[[i]], FPos[[i]]], {i, 2, Length[Fvec]}],
    Text[" f_s=0.5", {1.01, 2.8}]
   }],
  TextStyle → {FontFamily → "cmr8", FontSize → 10},
  AxesLabel → {" V_0", " I_0"},
  Frame → True
 ];
```

Boundary conditions2

```
JCritFunc[γinn_] := -1 / 2 Sin[γinn] + Sqrt[Sin[γinn / 2] + 1 / 4 Sin[γinn]];
φfunc[γinn_, Jinn_] := If[γinn < π, -1, 1] * ArcCos[Cos[γinn / 2] + Jinn Sin[γinn / 2]];
Mfunc[γinn_, φinn_] := (2 / γinn) (φinn - Sin[φinn] / Cos[γinn / 2]);
ParametricPlot[
 {Mfunc[γnow, φfunc[γnow, JCritFunc[γnow]]], JCritFunc[γinn]}, {γnow, π, 2 π}]
N[JCritFunc[3]]
N[φfunc[4, JCritFunc[4]]]
```

Sine plot

```
pp = Plot[{VPlot[S[t]], IPlot[S[t]]}, {t, -2.5 γ, 2.5 γ}, PlotPoints → 1000,
   Ticks → {{{-2 γ, "-2γ"}, {-γ, "-γ"}, {γ, "γ"}, {2 γ, "2γ"}}, Automatic}];
pp2 = Plot[HPlot[S[t]], {t, -2.5 γ, 2.5 γ}];
LabelTags = {{-2 γ, "-2γ"}, {-γ, "-γ "}, {γ, "γ  "}, {2 γ, "2γ "}};
Show[{
  Graphics[{
    Text[" iL", {4.25, 1.26693}],
    Text[" vC", {1.45, 2.1}],
    Text[" vH", {0.55, 1.15}],
    Black,
    pp2[[1]],
    Black,
    Table[Text[LabelTags[[i, 2]], {LabelTags[[i, 1]] + 0.4, -0.3}], {i, 1, 4}]


   }],
  {pp /. Line[l : {_, __}] :> ({
         CurveCol⟦1⟧    S[#1⟦1, 1⟧] < α
         CurveCol⟦2⟧   S[#1⟦1, 1⟧] < α + β
         CurveCol⟦3⟧  S[#1⟦1, 1⟧] < 2 α + β
         CurveCol⟦4⟧  S[#1⟦1, 1⟧] < 2 α + 2 β
        , Line[#1]} &) /@ Partition[l, 2, 1]
  }},
 TextStyle → {FontFamily → "cmr8", FontSize → 10},
 Axes → True, Ticks → {None, Automatic},
 AxesLabel → {"t", None}
];
```

4 - Stage PRC

```
Plot[
  Abs[VPlot[S[t - 0 * 1 / 4 γ]]] +
   Abs[VPlot[S[t - 1 * 1 / 4 γ]]] +
   Abs[VPlot[S[t - 2 * 1 / 4 γ]]] +
   Abs[VPlot[S[t - 3 * 1 / 4 γ]]]

  , {t, -2 γ, 2 γ}, PlotPoints → 100, PlotRange → {{-2 γ, 2 γ}, {0, 10}},
  Ticks → {{{-γ, "-γ"}, {γ, "γ"}}, {{2.5, "Vd"}}}];
```

Dimensioning

```
Gam = Range[2];
xN = 3;
count = 0;
Mtarget = 2.4;
While[Not[MT[xN] < 0 + 10^-6 && MT[xN] > 0 - 10^-6] && count < 100,
 xN = xN - MT[xN] / MTD[xN];
 count++;
]
Gam[[1]] = xN;

xN = 3;
count = 0;
Mtarget = 3;
While[Not[MT[xN] < 0 + 10^-6 && MT[xN] > 0 - 10^-6] && count < 100,
 xN = xN - MT[xN] / MTD[xN];
 count++;
]
Gam[[2]] = xN;
FreqN = Pi / Gam;
Ft = 20;
Freq = {Ft, Ft * FreqN[[2]] / FreqN[[1]]};
{Gam, FreqN, Freq}
M

MCpeak = If[JL0 > J, Sqrt[(MC0 + 1)^2 + (J - JL0)^2] - 1, Sqrt[1 + (JL1 - J)^2] + 1];
JLpeak = If[MC0 < 1 && JL0 > 0, JL0, J + Sqrt[(JL1 - J)^2 + 1]];
{MCpeak * 1.1, MCpeak * 0.88}
JLpeak * 200
```

```
{2.10509, 1.68407}

480.099
```

Export

```
Export["G:\users\j\jonasb\02_Master\Thesis\MathematicaOUT\SumOut.gif"
, %, "GIF", ImageSize → 300];
```