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Fundamentals of Grid Connected Photo-Voltaic Power Electronic Converter Design

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Master of Science in Energy and Environment
Submission date: June 2007
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Problem Description

The goal of this master thesis is to design a power electronic converter for use with solar power systems. The converter is meant to be used in the renewable energy laboratory at NTNU. It should be focused on the overall system, and the design should therefore be made with basic solutions in order to make the complexity low. In order to make this design, a literature study giving an overview of photo-voltaic systems and the power electronic converters used should be made. The study shall focus on both the hardware configurations, but also the control of these systems. To verify the theoretical studies made, simulations and experimental tests of the system should be made.

Assignment given: 22. January 2007
Supervisor: Lars Einar Norum, ELKRAFT

ACKNOWLEDGEMENTS

In this report the efforts of obtaining a masters degree in *electrical power engineering* at the *Norwegian University of Science and Technology* (NTNU) is concluded. The project which deals with the electrical conversion of power from solar panels was initiated by my supervisor Lars Norum at the department of *electric power conversion*. The project is a part of the integration of solar power in the renewable energy laboratory at NTNU, and hopefully it can contribute giving some basic understanding of the processes involved in the power conversion.

The first formulation of the scope for this project was very widely defined, and this gave me the opportunity to influence the extent and the content of the work in a large degree. At first the assignment was supposed to have a major focus on control of photo-voltaic converters, but because there was need for a DC-DC converter, the design and construction of this also became a large part of the thesis.

During the work with this thesis there has been several people who has helped me when things stopped up and given me a different point of view of things. I would first of all like to thank my supervisor Lars Norum for giving me good ideas and helping me formulate the thesis. When things stopped up in the laboratory i got lots of helpful tips from PhD student Pål Andreassen, so a big thanks to him for letting me bother him with all sorts of strange problems. I would also like to thank my fellow students at the department for support and encouragement during the last 6 months.

Last but not least I have to give a great thanks to my girlfriend Inger who has been home with our son Emre during my work with this thesis. You have been a great support, and you have given me the freedom to spend the time I needed on this thesis. So thanks for coping with almost being a single parent for the last few months of this work.

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ACRONYMS

ADC - Analog to Digital Converter

CB-PWM- Carrier Based PWM

CC - Current Control

CCM - Continuous Conduction Mode

CV - Constant voltage

DCM - Discontinuous Conduction Mode

DPWM- Discontinuous modulation PWM

DSP - Digital Signal Processor

FFT - Fast Fourier Transform

GI - Generalized Integrators

GUI - Graphical User Interface

HF - High Frequency

INC - Incremental conductance

LF - Low Frequency

MPP - Maximum Power Point

MPPT - Maximum Power Point Tracking

NDZ - Non Detection Zone

PCC - Point of Common Coupling (The point where a local EPS is connected to an area EPS)

PLL - Phase Lock Loop

PR - Proportional Resonant

PV - Photo Voltaic

PWM - Pulse Width Modulation

P&O - Perturb and observe

STC - Standard Test Conditions

SVM - Space Vector Modulation

SVPWM- Symmetrical SVM

VC - Voltage Control

VSI - Voltage Source Inverter

ZCD - Filtered Zero Cross Detection

ZSS - Zero Sequence Signal

PARAMETER DEFINITIONS

C_f - LCL filter capacitance

I_{SC} - PV short circuit current

L_i - LCL filter inverter side inductance

L_g - LCL filter grid side inductance

m_a - modulation ratio $\left(\hat{V}_{control}/\hat{V}_{tri}\right)$

n - transformer winding ratio

R_d - LCL filter damping resistance

V_{DC} - DC-link voltage

V_{MPP} - PV voltage at maximum power point

V_{N0} - Voltage between inverter neutral and load neutral

V_{OC} - PV open circuit voltage

V_{PV} - Voltage of the PV module

ABSTRACT

In this master thesis the basic theory of *grid connected photo-voltaic systems* is explained, giving an introduction to the different aspects of system design. Starting with a look at the standards concerning grid connection of *distributed resources,* and working its way through how the *photo-voltaic cells* work, to how *photo-voltaic modules* with *electrical converters* can be arranged. Some different converter topologies suitable for use with photo-voltaics are found, and based on these topologies, solutions for how to control these converters have been examined. These controls involve methods for utilizing the maximum power from solar panels, methods for synchronizing with the grid and methods for current and voltage control.

Based on this theory a system model is made, including an *isolated current fed full bridge DC-DC converter* in cascade with a *three phase full bridge DC-AC converter* having a *LCL filter* as grid interface. This model is simulated in Simulink and experiments are made on a laboratory setup, where focus has been on the control system. Therefore linear system models of the control system has been made, and these have formed a basis for the optimization of the control systems. The simulations have been made using *Simulink*, and the control system for the converters has been implemented in two *DSP's*, one for each converter.

The design and construction of the DC-DC converter has been made in this thesis, but it showed out to be more complicated then first assumed. Because of this, too little time was spent in the design of the circuit and too much time was spent on testing and correcting errors. It ended with a non-functional converter, and therefore the experiments made had to be done without the DC-DC converter. However the report shows that the *isolated current fed full bridge DC-DC converter* is a promising topology in *photo-voltaic* systems, and should be investigated closer.

It is found in the simulations and experiments made, that the system models derived give a dynamic response close to the real, and are suitable for giving a basic understanding of the system dynamics and for optimizing the control system. The control system consists of a *maximum power point tracker* which effectively finds the point where the *photo-voltaic modules* delivers the highest power, and in order to synchronize to the grid voltage a *phase locked loop* is used, which locks the converter output to the grid voltage in less then 10ms. In order to control the power flow into the grid, current control in a *rotating reference frame* locked to the grid voltage is used. This has simplified the control since it gives DC-values stationary, and has made it possible to separately control the active and reactive power flow.

Most of the tests made in the simulations and experiments have been made with operating conditions close to ideal. In order to verify how the system handles varying operating conditions, and to see if it coincides with the requirements in the standards, more extensive testing should be made of the system. This includes testing with varying irradiance of the solar panels, grid disturbances and grid failures.

1 INTRODUCTION

This master thesis deals with the connection of *photo-voltaic* power sources to the *electrical grid*. Today photo-voltaics has become one of the major renewable energy sources in the world, and in order to utilize the energy from this power source, electrical converters is needed. This study is meant as an introduction to the design of *grid connected photo-voltaic electrical power converters*, and it has been written for the Department of Electric Power Engineering at NTNU.

The study shall give an overview of the different aspects of designing an electrical converter. By taking the reader through the basics of what characterizes a photo-voltaic system and which requirements is put upon such a system, the report aims on giving a fundamental understanding of how to supply the energy from the solar panels into an electrical grid. The theory shall then be put to the test by finding a representative system model, and then simulating it and test it on an experimental setup.

Chapter 2 introduces photo-voltaic systems and has focus on the characteristics of solar cells, and how they are arranged. Standards dealing with the interconnection of PV power sources and the electrical grid are reviewed, and the last part of this chapter describes different converter topologies, with filters and temporary storage alternatives.

Chapter 3 describes different ways to control the converters. Methods for utilizing the maximum power from the solar panels, methods for controlling the energy flow into the grid is explained, and some methods for synchronizing the converter output with the grid voltage is presented. An introduction to islanding detection is given, and to the implementation of a digital control system is also given. Last in this chapter it is explained how to optimize the control systems used in this thesis.

Chapter 4 gives a description of the system used in the simulations and the laboratory setup used in this project. It describes what sort of control, and which hardware have been used. Based on this models for the control system is found based on linear system theory, and the control systems are optimized using the methods described in chapter 3.

Chapter 5 and 6 describes the results of the simulations and the experiments which have been made. The tests have focus on verifying the models made of the control system, but also a harmonic analysis will be made in order to verify the quality of the power delivered to the grid.

Chapter 7 concludes the thesis with a discussion of the most important aspects of this thesis, and ends up with a conclusion and suggestions for further work

2 OVERVIEW OF PHOTO VOLTAIC SYSTEMS AND CONVERTERS

In the resent years there has been a large increase in the interest for renewable energy. This is due to an increasing need for energy, increasing power prices and the need for more environmental friendly power sources. A consequence of this is an enormous amount of new renewable energy projects. Renewable energy sources are often small (compared to traditional energy production), and they are often spread around the utility network, therefore they are often termed *distributed resources*, and includes sources like solar, wind and wave power.

Solar power generated from *photo-voltaic* (PV) cells is gaining increased importance as a renewable source due to advantages such as the absence of fuel cost, little maintenance and no noise and wear due to absence of moving parts. So in theory this is an ideal power source, but in practice there are several problems that needs to be addressed. There is still a high installation cost, low energy conversion efficiency and issues concerning the interaction with other systems.

The energy from PV panels is in the form of DC-current, and in order to utilize this energy in the grid, the current must be transformed into AC-current. The most convenient way to to this is by the use of *electric power converters*. Using these converters as a grid interface for PV panels is not a new technology, and much of the same technology is used in e.g. fuel cell converter, wind power converters and also converters for motor drives. Even though they use much of the same technology, there are always some special considerations for the different cases.

In this chapter the standards concerning the connection of *distributed resources* to the grid, and which requirements this has on the system design is examined. Next the characteristics of *photo-voltaic* power will be introduced, and different converter and solar panels structures will be shown.

2.1 Grid connection standards

Before designing a converter for grid connection of *photo-voltaic* power sources, an overview of which rules and regulations one must follow in order to be allowed to connect to the grid should be investigated. These rules will however not be the same all over the world. Depending on the grid type there are different considerations to be made in each country, and therefore there will always be some adaption to the demands from the local utilities. The demands from the local utilities are usually based on a national standard or international standard which deals with the interconnection of distributed resources. These standards are often very similar, but they might have some variations in the degree of limitations and in the definitions used. By looking at the standards from two of the major international standardisation organizations listed below, an overlook of the most important demands and limitations can be found.

- *International Electrotechnical Commission* - IEC

- *Institute of Electrical and Electronics Engineers* - IEEE

When developing a PV system there is a risk that even though all current standards are followed, there are new ones released before or right after the product is released, and the product will become outdated. A major goal when designing a new converter is to make it compatible with current standards, but also future standards. Below is a list of the most recent standards of interest from IEC and IEEE.

- *IEEE Std 1547-2003* [1]: Standard for Interconnecting Distributed Resources with Electric Power Systems
- *IEC 61727 Second Edition 2004-12* [2]: Photovoltaic (PV) systems - Characteristics of the utility interface.

IEEE has also released a recommended practice document especially for grid connection of photovoltaic cells, this states mostly the same as [1]

- *IEEE STD 929-2000* [3]: Recommended Practice for Utility Interface of Photovoltaic (PV) Systems

2.1.1 Converter requirements

Based on the international standards mentioned above a list of requirements for the design of a converter can be made. Below is a list of requirements which should be followed when designing a converter in order to make it coincide with the standards.

Grounding

It should be possible to connect the negative pole of the PV panels to ground.

Power Quality

The quality of the power provided by the PV system for the on-site loads and the power delivered to the utility is governed by practices and standards addressing voltage, DC-injection, flicker, frequency, distortion/harmonics and power factor. These parameters must, unless otherwise is specified, be measured at the *point of common coupling* (PCC).

1. Voltage

   Grid connected PV systems do not normally control the voltage of the connected grid, they merely inject current into it, therefore there is usually not any active voltage control. On the other hand there has to be a certain voltage operating range where the inverter is allowed to work, in order to detect abnormal utility conditions and prevent islanding mode. The inverters response to abnormal voltages is specified in table 2.1.

Table 2.1 - Voltage operating range

Voltage[a]	Maximum trip time[b]
$V < 50\%$	0,1s
$50\% \le V < 85\%$	2,0s
$85\% \le V \le 110\%$	Continuous operation
$110\% < V < 135\%$	2,0s
$135\% \le V$	0,05s

a. Limits are in % of the nominal voltage at PCC in RMS.
b. Trip time refers to the time between the abnormal condition occurring and the inverter ceasing to energize the utility line.

Within the specified trip times the inverter must cease to energize the grid, but the PV control circuits shall remain connected to the grid to allow sensing of the electrical conditions. The latter for use by a reconnection feature. Unless the voltage is measured at the PCC, the voltage drop between the inverter and the PCC must be taken into considerations. For further information on voltage operating range see *IEC 61727* §5.2.1 and *IEEE 929* §4.1

2. DC-injection

The inverter shall not inject DC current >0.5% of rated inverter output current into the utility AC interface under any operating condition. For further information on DC-injection see *IEC 61727* §4.4 and *IEE 929* §5.2

3. Flicker

Only IEC 61727 gives specific limits for flicker, thus these will be used. This standard states that the amount of flicker must comply with *IEC 61000-3-3* §4 and *IEC 61000-3-5*. The flicker limits stated in these standards are approximately equal, so the limits in table 2.2 can be used for all system sizes. For the calculation of the amount of flicker the reader is referred to the standards.

Table 2.2 - Flicker limits

Limits P_{st}[a]	Limits P_{lt}[b]
≤ 1.0	≤ 0.65

a. P_{st} is the short term flicker indicator. This is the flicker severity evaluated over a short period (i minutes), where P_{st}=1 is the conventional threshold of irritability

b. P_{lt} is the long term flicker indicator. This is the flicker severity evaluated over a long period (a few hours) using successive P_{st} values.

4. Frequency

The PV system must operate in synchronism with the grid voltage. If the frequency deviates outside of the specified condition, the converter shall cease to energize the grid within a specified time. The allowed operating frequency and trip time differs between countries, and thus these limits will have to be adjustable. The default limits will be according to *IEC 61727* §5.2.2, which states that when the utility frequency is outside $\pm 1\,\mathrm{Hz}$ of the rated frequency, the system shall cease to energize the utility within 0,2s. If the utility returns to normal operating frequency within this time, the converter does not have to cease energizing the utility line.

The limits for North America can be found in *IEEE 929* §4.3, and states that the frequency operating range is between 59.3 - 60.5Hz, and the converter should cease to energize the utility within 6 cycles (0.1s). For further information on the frequency limits see *IEC 61727* §4.5 and *IEEE 929* §4.3.

5. Distortion/Harmonics

It is desirable to have low levels of current and harmonic distortion in the grid, in order to decrease the potential for adverse effects on connected equipment. In the standards this is regulated through limits in allowed current distortion. The allowed current distortion limits the converter is allowed to inject into the grid is given in table 2.3. For further information on the harmonic limits see *IEC 61727* §4.6 and *IEEE 929* §4.4.

Table 2.3 - Harmonic current limits

Harmonic order h (odd harmonics)[a]	Distortion limits[b]
THD	5%
3rd through 9th	<4.0%
11th through 15th	<2.0%
17th through 21st	<1.5%
23rd through 33rd	<0.6%
above 33rd	<0.3%

a. Even harmonics are limited to 25% of the odd harmonic limits above.
b. All limits are given as percent of the rated fundamental current component

6. Power factor

The converter shall have a power factor according to table 2.4, but in some situations there is a need for the inverter to supply reactive power. Therefore the inverter should have the ability to regulate the output power factor. For further information on the power factor limits see *IEC 61727* §4.7 and *IEEE 929* §4.5.

Table 2.4 - Power factor limits

Output of converter[a]	Power factor
>10%	>0.85(lagging)
>50%	>0.9(lagging)

a. In percent of rated output

Anti-Islanding

A non-islanding inverter is defined as an inverter that ceases to operate within a certain time after the islanding occurs, but based on measurements it is not easy to define a set of limitations defining exactly when an islanding situation occurs. The definition of when an islanding situation occurs has been defined differently in the standards from IEC and IEEE.

1. *IEC 61727*:

   A utility distribution system is islanded when it is out of the normal operation specifications for voltage and/or frequency. When this situation occurs, the PV system must cease to energize the utility within 2 s of loss of utility.

2. *IEEE 929* (definition of non islanding inverter):

   An inverter that will cease to energize the utility line in ten cycles or less when subjected to a typical islanded load in which either of the following is true:

   a) There is at least a 50% mismatch in real power load to inverter output (that is, real power load is <50% or >150% of inverter power output).

   b) The islanded-load power factor is < 0.95 (lead or lag).

   If the real-power-generation-to-load match is within 50% and the islanded-load power factor is > 0.95, then a non-islanding inverter will cease to energize the utility line within 2 s whenever the connected line has a quality factor of 2.5 or less.

Neither of these limits are adequate for determining when a islanding situation occurs in every possible situation, but to be able to satisfy the standards the to last definitions should be used. It should however be noted that in *IEC 61727* it is stated that the issues of non-islanding inverter is the subject of another standard under consideration. So one should be aware that these requirements may change, and become stricter.

Reconnection

When an out-of-bounds utility event occurs, in which the inverter has ceased to energize the utility line, the inverter shall not reconnect before the frequency and voltage have been maintained within the specified limits for at least 5 min. After these 5 min. The inverter shall automatically reconnect to the utility.

2.2 Solar Cell Characteristics

Energy sources deliver energy in many forms, some mechanical with conversion to electrical, some with conversion of chemically stored energy to electricity, and some produce energy directly as electrical energy. The latter is the case when producing energy with solar cells, where the energy is delivered as DC current. The photo voltaic cells have a special *current-voltage* (I-V) characteristic which must be taken into consideration when designing a PV power system. Defining this characteristic is a short circuit current I_{sc} and an open circuit voltage $V_{oc.}$ This characteristic varies with irradiance and temperature, and in figure 2.1 it is shown how this current voltage relationship changes as the irradiance decreases.

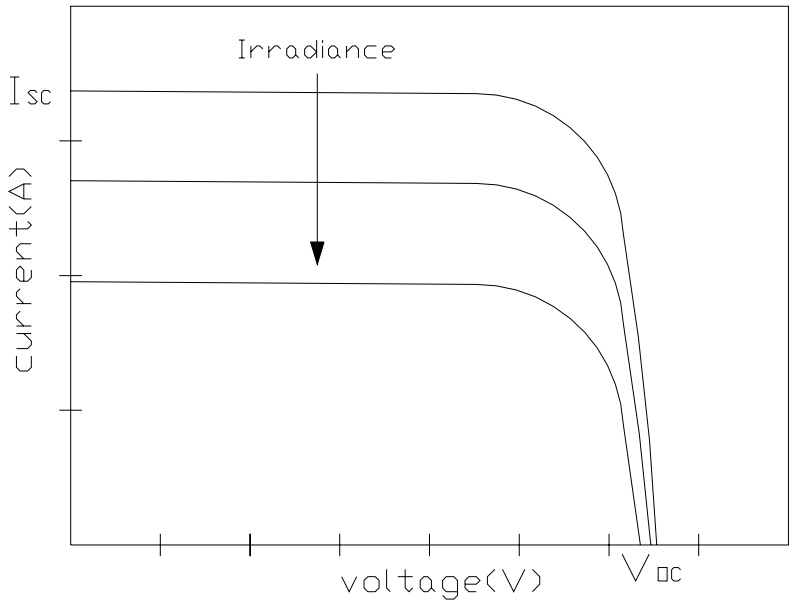

Figure 2.1: I-V characteristic of a solar cell as irradiance decreases

As can be seen from the figure, it is mostly the current which is affected by the change in irradiance, and thus the voltage variation due to changes in irradiance is usually neglected. The response to temperature changes is somewhat different, and is shown in figure 2.2

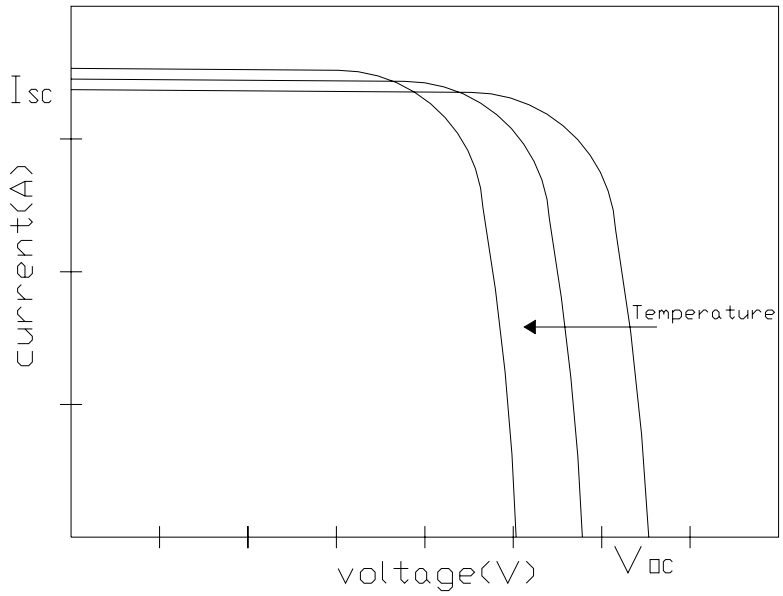

Figure 2.2: I-V characteristic of a solar cell as temperature increases

As the figure shows the open circuit voltage is largely dependent on the temperature, whereas the current is only slightly dependent, therefore the current change due to temperature variations is usually neglected. In a practical calculation, the voltage variation with temperature of a module or a string consisting of n_c cells in series, is often sat equal to:

$$\frac{dV_{OC}}{dT} = -2.3 \cdot n_c[\mathrm{mV}/^{\circ}C] \qquad (2.1)$$

It can be seen from the I-V characteristic that when drawing power from a solar cell, it is most beneficial to work in the region where the product of current and voltage is at its highest, and thus delivers the highest output power. The *power-voltage* (P-V) characteristic is shown in figure 2.3.

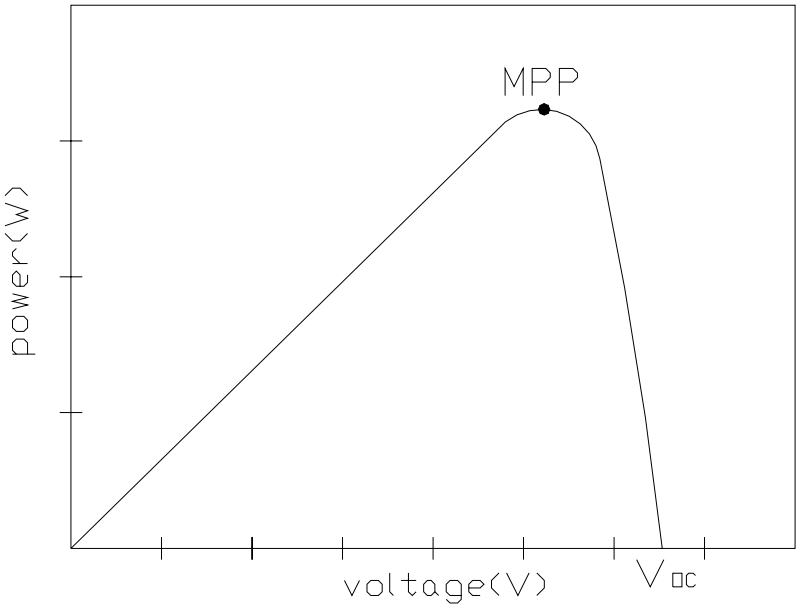

Figure 2.3: P-V characteristic of a solar cell

As seen from the figure it is important to deliver power at the voltage which gives the highest power, or else the power output end thus the efficiency of the system will rapidly decrease. This point on the curve giving the highest power, is commonly referred to as the *maximum power point* (MPP). It is now important to recognize that the power is depending on both the current and the voltage, and therefore the MPP will be largely depending on both irradiance and temperature.

2.2.1 PV panel modelling

In order to simulate the behaviour of a specific solar panel, there have been made different mathematical models in the literature, which can be used to make theoretical models. These models will only be approximations to the behaviour of the panels, and the accuracy of the models depend on how many internal phenomena are considered. The equations shown below are rather simple and does not give a high degree of accuracy, but they will give an understanding of the basic behaviour of the solar cells. The definition of the different variables in the equations is found at the end of this chapter.

The cell temperature is a function of the ambient temperature and the irradiance, and is given in Kelvin.

$$T_{cell} = T_a + \frac{NOCT - 20}{800} \cdot G \tag{2.2}$$

In eq (2.3) the changes in short circuit current due to temperature and irradiance is shown.

$$I_{SC} = I_{SC\_STC}\left(1 + \alpha_I \cdot \left(T_{cell} - T_{STC}\right)\right)\frac{G}{G_{STC}} \tag{2.3}$$

In eq (2.4) it is assumed that the change in open circuit voltage due to changes in irradiance are so small they can be neglected, therefore the open circuit voltage is only a function of temperature.

$$V_{OC} = V_{OC\_STC}\left(1+\alpha_V \cdot (T_{cell} - T_{STC})\right) \tag{2.4}$$

The output current of a solar cell is the light induced current minus the diode current, as can be seen from the equivalent circuit of a PV cell shown in the figure below.

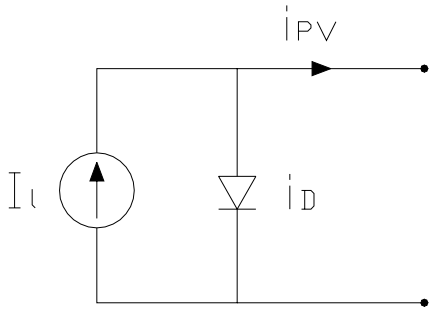

Figure 2.4: Equivalent circuit of a photo.voltaic cell

The light induced current is the same as the short circuit current, and the PV cell output current is then given in (2.5)

$$i_{PV} = I_l - i_D = I_{SC} - I_0\left[\exp\left(\frac{qv_{PV}}{kT_{cell}}\right) - 1\right] \tag{2.5}$$

Based om (2.5) the dark saturation current I_0 can be found by setting i_{PV}=0 and v_{PV}=V_{OC}, as shown in (2.6).

$$I_0 = I_{SC}\left[\exp\left(\frac{qV_{OC}}{kT_{cell}}\right) - 1\right]^{-1} \tag{2.6}$$

By using (2.5) the PV voltage from one cell can also be found.

$$v_{pv} = \frac{k\ln\left(1 - \frac{i_{PV} - I_{SC}}{I_0}\right)}{qT} \tag{2.7}$$

A ideal I-V curve would be rectangular, but in practice this is not so. The “Fill Factor” (FF) describes how close the I-V curve is to the ideal one, and is defined as

$$FF = \frac{P_{MPP}}{V_{OC} I_{SC}} \tag{2.8}$$

Based on these equations a complete model of the PV panels can be made. This model can then be implemented in a simulation program and used for simulation of PV-panels. Another use of these models or other models for that sake, is in the control of a DC-power source used as a PV simulator. A converter of this type can be an alternative to field testing of PV-panels and of converters. With this converter one will also be able to do repeatable tests, and simulations of all sorts of operating conditions. Some examples of such converters are given in [4,5]. Below is a list of the different parameters found in the equations presented in this section.

k_I - Temperature coeffisient of I_{SC}
k_V - Temperature coeffisient of V_{OC}
k_P - Temperature coeffisient of P_{MPP}
G - iirradiance [W/m^2]
I_{SC} -Short circuit current
I_0 - Dark saturation current
k = 1.3806 10^{-23} J/K (Boltzmann constant)
MPP - Maximum Power Point
NOCT - Normal Operating Cell Temperature [°C]
n_s - nr of cells in series in one panel
n_{ps} - nr of panels in series
n_{sp} - nr of strings in parallel
P_{MPP} - Power at MPP
q = 1.6 10^{-19} C (Electron charge)
STC - Standard Test Condition (G=1000W/m^2, T=25°C, AM1.5)
T_a - Ambient temperature [K]
T_{cell} - Cell temperature [K]
G – irradiance [W/m^2]
V_{OC} - Open circuit voltage

2.3 Solar panel and converter configurations

Throughout the history of solar panels there has been several ways of arranging the solar panels have been tried. How they are arranged has an effect on which type of converter which should be used, and this will in turn influence the cost and efficiency of the system. Figure 2.5 (from [6]) shows a historical overview of the different panel configurations of panels and converters used in the past, present and future.

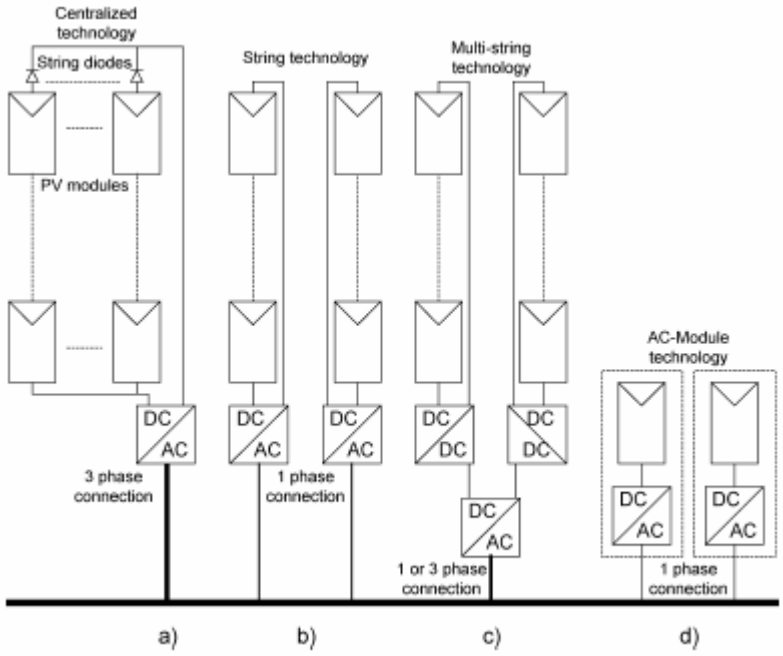

Figure 2.5: Historical overview of PV converters. (a) Past centralized technology. (b) Present string technology. (c) Present and future multi-string technology. (d) Present and future AC-module and AC cell technologies.

In [6] a review of different configurations is presented, and a summary of this is presented here. In this section the abbreviation MPPT is used a lot, which stands for *maximum power point tracker* and is described in chapter 3.1.

Centralized Converters

This is an old technology, and is based on the connection of a large number of PV modules to the converter (see figure 2.5a)). The advantage of this configuration is the need for few converters, which give low loss in the power conversion stage, and the possibility to connect several modules in series to achieve a sufficiently high input voltage and then avoid further amplification. However the drawbacks are more severe, with limitations such as the use of high-voltage DC-cables between the PV modules and the converter, power losses due to centralized MPPT, mismatch losses between the PV modules, losses in the string diodes[1], and a non flexible design where the benefits of mass production cannot be reached.

String Converters

As seen in figure 2.5 b), the string converter is a reduced version of the centralized converter, where only one single string is connected to each converter. In this configuration one can also gain the advantage of high input voltage, if a sufficiently amount of PV modules are connected in series. If the input voltage is to low, then the use of a transformer, or a DC-DC converter can be used to boost the voltage. Since there is only one

1. *String diodes are used to prevent current from one string to enter another string.*

string, the use of string diodes[1] is not necessary, and it allows individual MPPT tracking of each string. The mismatch losses are also reduced, but not eliminated. All in all this configuration increases the overall efficiency when compared to the centralized converter, and it will reduce the price, due to possibility for mass production.

Multi-String Converters

The multi-string converter in figure 2.5 c), is a further development of the string converter, and has many of the advantages of both the centralized converter and the string converter. In this configuration there is one DC-DC converter with separate MPPT tracking for each input, all connected to the same inverter. This is beneficial since the MPPT can be controlled individually for each string, and a plant can be realized with less components than the string converter. This gives a flexible design with high efficiency, and will probably become standard where centralized and string converters are used today.

AC-Module Converters

With this configuration one PV module is integrated with the converter in one electrical device, as shown in figure 2.5 d). By incorporating the PV module and the converter into one device, the possibilities of creating a module based “plug and play” device arises, and it can than be used by persons without any knowledge of electrical installations. In this configuration the mismatch losses between the PV modules is removed, and it is possible to optimize the converter to the PV module, and thus also allowing individual MPPT of each module. Since there will be need for more devices then with the previous mentioned configurations, it will give the benefit of large scale production, and thus lower prices. On the other hand the input voltage will become low, requiring high voltage amplification, which may reduce the overall efficiency.

2.4 Converter topologies

The converters for all the panel configurations presented in 2.3, are based on the same basic topologies. In [7] a schematic of the fundamental PV converter topologies is presented, this is shown in the figure below.

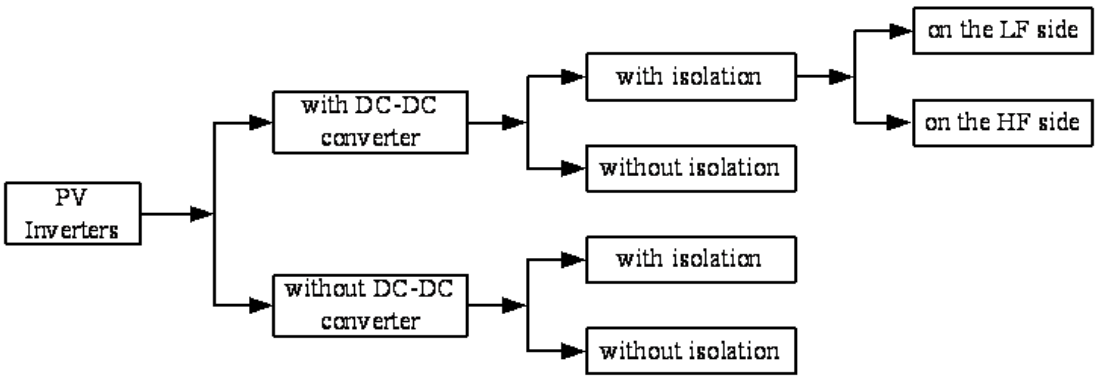

Figure 2.6: PV converter topologies [7]

A seen in the figure, there are three major parts an converter can be constructed of. First there is the *DC-AC converter* (inverter), a *DC-DC converter* and *transformer* (galvanic isolation) and. The different parts are described in [6,7,8], and is summarized in the following paragraphs.

2.4.1 Transformer

The transformer has to major functions in the circuit, to amplify the voltage and to gain galvanic isolation between the PV modules and the grid. There are two basic ways to connect the transformer, one is by embedding it in a *high frequency* (HF) DC-DC converter, or connecting a *low frequency* (LF) transformer on the grid side. The latter is in newer converters often avoided because of increased size, weight and prize. So in modern converters there is a tendency towards using HF transformers.

The galvanic isolation is often needed in order to ground the PV system properly. This grounding sometimes involves connecting the negative terminal of the PV array(s) to ground, and in transformerless systems this might become a problem. Especially in one-phase systems with neutral to line connection, where the inverter is already grounded on the grid side. Galvanic isolation can also, if mounted on the low frequency (LF) side, prevent DC-current from entering the connected grid. This can however be solved by using improved measuring equipment, which is able to detect small DC-currents.

Some standards demand that the PV modules shall be grounded and monitored by faults, while others only demand equipment ground (grounding of frames and other metallic parts) in the absence of galvanic isolation. There is usually not any direct demands for galvanic isolation in the standards, but it is often the only, or the easiest way to achieve system grounding and/or to prevent the injection of DC-currents. Transformerless topologies are also very interesting because they can offer higher efficiency and reduced cost, but more research is needed to be done in order to minimize the leakage current and ensure safety and panels reliability

If using a transformer the question will be where to place it, on the high frequency (HF) or the low frequency (LF) side? The LF transformer is more expensive, larger and heavier, but the design is more simple then if a HF transformer is used.

2.4.2 DC-DC converter

PV converters with DC-DC converter is termed *dual stage*, and in this topology the DC-DC converter will handle the MPPT (see chapter 3.1) and some voltage amplification if needed. Most converter structures only have one DC-DC converter, but multi string converters will have two or more.

The output of the DC-DC converter will depend on the inverter used at the grid interface. If the inverter is controlling the grid current by means of pulse width modulation (PWM), or bang-bang (hysteresis) operation, then the output of the DC-DC converter can be a pure DC voltage. The inverter can also switch at line frequency, and then the output of the DC-DC

converter can be a current, modulated to follow a rectified sine wave, thus the inverter will unfold the rectified sine wave into a full sine wave. According to [6] the latter solution can give a high efficiency if the nominal power is low, but if the power is high, it is advisable to operate the inverter in PWM mode, and thus the output of the DC-DC converter will be a pure DC voltage.

The choice of DC-DC converter depends mainly on the use of HF transformer, and amplification range. When there is no transformer, a buck, boost, buck-boost or variants of these can be used, and if a HF transformer is used, a forward, push-pull, flyback, half-bride, full-bridge or other variants can be applied. Because there is usually a need for galvanic isolation the ones with a HF transformer is the most interesting.

The forward and the flyback converters are typically used for low power applications (up to approximately 250w for the flyback), because of low utilization of the magnetic components due to unidirectional core excitation. There are ways to improve the power handling capabilities of these converters, but this will not be handled here. These topologies are therefore best suited for small AC-module converters, or other low power designs.

For medium power applications, converters with bidirectional core excitation are preferred, because they utilize the magnetic components better. The push-pull, half-bridge and full-bridge converters are examples of the latter. In [7] three different topologies with bidirectional transformer excitation has been considered, with “max efficiency” as optimization criteria. These topologies are usually used for applications at 750W or more, and the three topologies are:

- *Full bridge isolated boost DC-DC converter* (FB)
- *Single-inductor boost push-pull converter* (SIC)
- *Dual-inductor boost push-pull converter* (DIC)

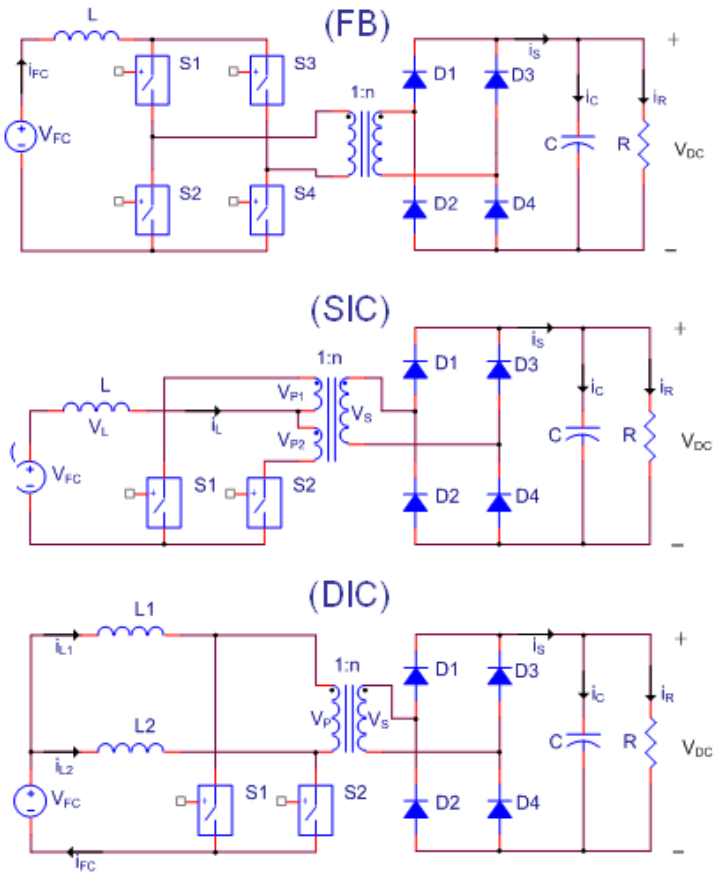

Figure 2.7: The full bridge isolated boost (FB), the single-inductor boost push-pull (SIC) and the dual-inductor boost push-pull (DIC) DC-DC converter [7].

The results of the comparison is shown in the tables presented below.

Table 2.5 - Comparison of DC-DC converters ([7])

Parameter	Full-Bridge	SIC	DIC
Number of switches	4	2	2
Number of Boost Inductor	1	1	2
Transformer	1 primary coil	2 primary coils	1 primary coil
Switch peak voltage	V_{DC}/n	$2*V_{DC}/n$	V_{DC}/n
Switch rms current			
Boost inductor current	I_{FC}	I_{FC}	$I_{FC}/2$
Inductor current ripple frequency	$2f_S$	$2f_S$	f_S
Trafo peak volt- ampere	$(V_{DC}/n)*I_{FC}$	$(V_{DC}/n)*I_{FC}$	$(V_{DC}/n)*I_{FC}/2$
Duty-cycle	0.69	0.69	0.38

Table 2.6 - Loss comparison dc-dc converters ([7])
(Full bridge is reference, with loss in pu)

Loss types	Full-Bridge	SIC	DIC
P_{SW}, switch	1	~1	~0.5
P_C, switch	1	~0.5	~0.61
P_{COPPER}, transf	1	~1	~0.5
P_{CORE}, transf	1	~1	~1
P_{COPPER}, inductor	1	~1	~0.64
P_{CORE}, inductor	1	~1	~2.65

The comparison concludes that the full bridge isolated boost DC-DC converter is advantageous as it uses the same power stage as the grid inverter (proven technology), and it is more suitable for applications with higher input voltages. Whereas the push-pull DC-DC converters are more suitable for applications with low input voltage, and the topology with dual-inductor yields in slightly higher efficiency as single-inductor topology.

The *full bridge isolated boost DC-DC converter* is also called a *current fed full bridge converter.* In [26] it is compared to the *voltage fed full bridge converter*, which is based on the same converter but with different input circuitry. The current fed converter has a inductor at the input and therefore has a *boost* characteristic, whereas the voltage fed has no inductor and therefore has a *buck* characteristic. In this thesis they are compared with each other with respect to their suitability for use with fuel cells, but the results are interesting also for photo-voltaic systems. It is here concluded that the current fed converter has a 1-2% higher efficiency compared the voltage fed converter, which is due to lower semiconductor losses. In the voltage fed converter it is also shown that the transformer leakage inductance has a great influence on the dimensioning of the converter, and that it limits the maximum output to input voltage ratio or the operating frequency of the converter. This is not a problem in the current fed, but it will need a clamping circuit for the energy stored in the transformer leakage inductance.

2.4.3 DC-AC inverter

The DC-AC converter is the most fundamental part of the PV converter, and can be made as one- or three-phase. A single phase converter is the most common solution for small residential converters up to approximately 5-6 kW, but the use of a three-phase converter has some advantages. First of all the power will be distributed equally in all three phases, and unlike single-phase inverters, the three-phase inverter will under balanced load conditions have a constant instantaneous load power (see figure 2.8). The latter will remove the need for capacitive storage elements under the balanced load conditions, but control techniques that deal with unbalanced three-phase condition can be needed.

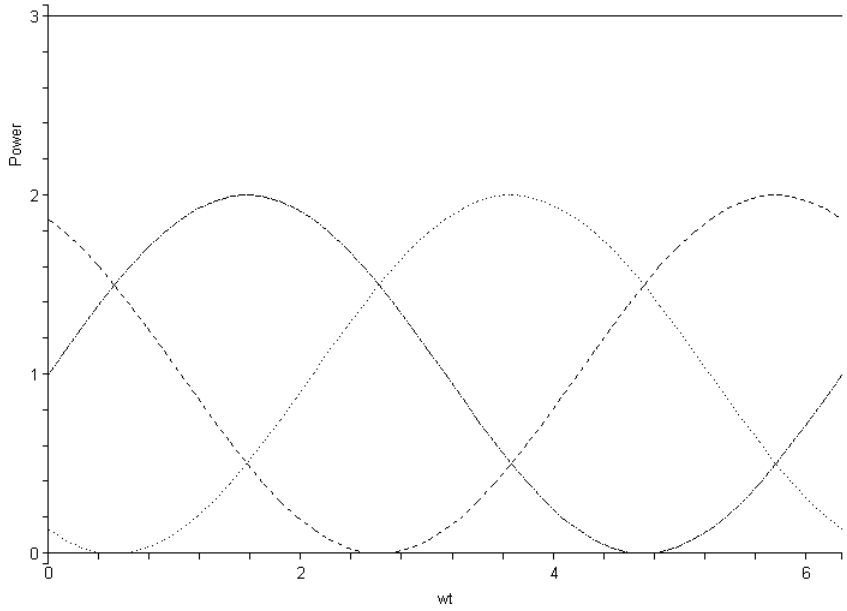

Figure 2.8: The instantaneous power in the three phases, and the sum of these powers as the solid line

The inverters used for grid interfacing of the PV panels are usually voltage source inverters (VSI's), but current source inverters (CSI) are also used. Since the PV modules are current sources, a capacitor has to be added in parallel when using a VSI, in this way the inverter sees a voltage source.

This thesis is based on a three-phase converter, and the most commonly used topology is the full bridge VSI (two level), but it is also possible to use more advanced multilevel inverters (three levels or more). Some of the most common is described in [9], like the diode clamped multilevel inverter, the flying capacitor structure, and series H-bridge multilevel inverter. It is also possible to use a line commutated inverter, but it gives poor power factor and power quality, and is seldom used.

By using a full bridge VSI as shown in figure 2.9, a near sinusoidal current can be produced and harmonic distortion can be lower than by using a line commutated inverter. The level of harmonic distortion is depending on the switching frequency, and the modulation technique used (see chapter 3.3.2).

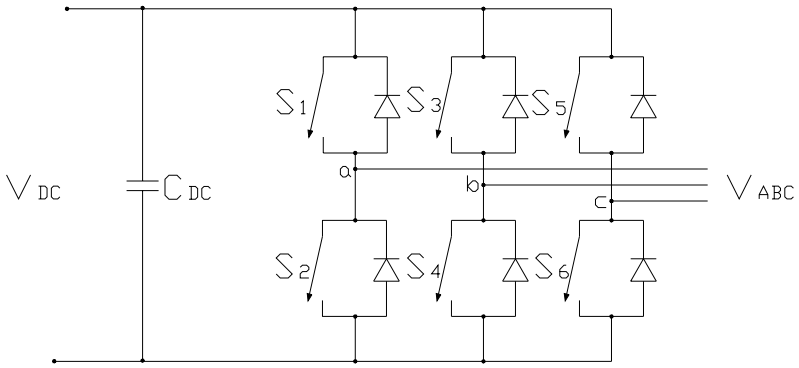

Figure 2.9: Full bridge VSI

By using a multilevel inverter, advantages such as improved power quality and electromagnetic compatibility (EMC), lower switching losses, and higher voltage capability can be achieved. The main disadvantages of this technique is that a larger number of switching semiconductors are required for lower-voltage systems and the small voltage steps must be supplied on the DC side either by a capacitor bank or multiple PV modules configured to create voltage steps. Multilevel inverters are most often used in larger PV systems, and it is an area of much research.

2.5 Grid filter topologies

Injection of power from the PV system to the grid is typically done through a VSI. Harmonics in the output voltage of the inverter is usually attenuated by connecting a filter between the VSI and the grid in order to cope with the power quality requirements of the utility. Improvements in the reactive power export to the grid is also constrained by the filter parameter. The most common filters used for this purpose are reviewed in this chapter

2.5.1 L-filter

The degree of which the harmonic content is attenuated depends on the filter used. A first order filter consisting of one inductor in series with the mains is the most commonly used filter. This is because the filter is easy to make, and it has no resonance problems as higher order filters may have. The major drawback of this filter is the size of the inductor needed to achieve a reasonable attenuation of the current harmonics. So with an attenuation of 20dB per decade over the whole frequency range, this filter is most efficient when used with high frequency PWM converters.

2.5.2 LC and LCL-filter

Higher order filters consisting of combinations of inductors and capacitors, can give a better attenuation of the harmonics, but they also make the design more complex. The most common higher order filters are the second order LC filter and the third order LCL filter. In grid connected systems the LC filter is seldom used, since the resonance frequency of the

filter will vary with the inductance value of the grid. Instead by using a correctly designed LCL filter this problem is reduced, because the resonance frequency is mostly depending on the filter components. The LCL filter will also give a better attenuation than a LC filter given the same size.

The dynamic control of the inverter is more difficult when using a LCL filter compared to using a simple L filter. With the LCL filter two more poles and two more zeroes are introduced compared two the simple L filter. So care must therefore be taken when designing the controller, and the additional poles and zeroes can make the system unstable if not proper damping is introduced.

Damping

Damping of the LCL filter resonance can be either active using the converter, or passive using elements like resistors, capacitors and inductors. Several different methods for passive damping has been proposed ([10]), from a simple resistor in series with the capacitor, to more complex circuits including resistors, capacitors and inductors in series or parallel with the condensator. When a resistor is introduced in the circuit, there will be some increase in the losses, how much depends on the configuration. One should also be aware that some of the configurations might introduce resonance frequency shifts, and lower attenuation at higher frequencies compared to the undamped LCL filter.

Several different approaches to active damping has been proposed in the literature. These methods often require the measurement of the capacitor voltage and/or currents, but other methods using estimated values have also been used. The use of active damping removes the losses associated with passive damping, but it increases the complexity of the control and might introduce other problems if not correctly designed.

In the figure below a LCL filter with a simple passive damping resistor in series with the filter capacitor is shown.

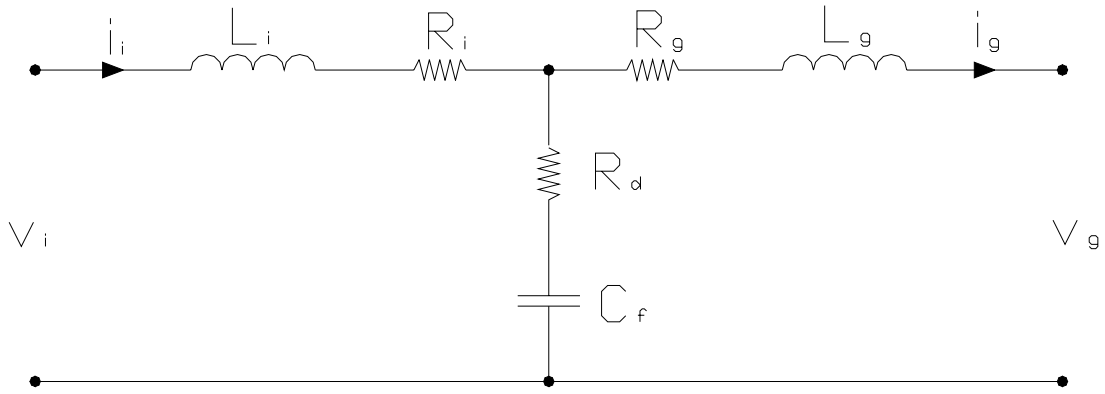

Figure 2.10: LCL filter model with damping and inductor resistance

2.6 Temporary storage

In some applications temporary storage of the produced energy might be needed for several reasons. If the system is connected to a weak grid, some extra capacity might be useful to stabilize the grid during short periods of high power consumption, and to increase the short circuit capabilities of the grid. The temporary storage might also be used as a UPS, where a part of the load will be supplied by the PV system if the grid is disconnected. There is also the case where the PV system is working as a standalone system, but this is not of interest here. There are several different technologies for storing the produced energy, but for grid connected systems some sort of battery storage is the most common.

3 CONTROL OF PHOTO-VOLTAIC CONVERTERS

Almost all of the converters found in the previous chapter are active converters with controllable switches. These can be controlled in various ways in order to achieve a desired effect. In this chapter some control methods which are of interest in PV systems are presented. An introduction to the implementation of a control system in a DSP is also given. In order to optimize the control systems, some methods for the optimization of the various controls is also given.

3.1 Maximum power utilization of photo voltaic power sources

To utilize the maximum power produced by the solar cell at all times, the regulation system has to be equipped with a *maximum power point tracker* (MPPT). This is a device which *tracks* the voltage at where the maximum power is utilized at all times. It is usually implemented in the DC-DC converter, but in systems without a DC-DC converter the MPPT is included in the DC-AC inverter control. Several methods have been developed for this purpose, and the most well known are presented here, with their major advantages and drawbacks (from [7,11]).

3.1.1 Constant voltage (CV)

This algorithm is based on the fact that the MPP voltage changes only slightly with varying irradiance. The MPP voltage is expressed as the ratio between V_{MPP}/V_{OC}, where V_{MPP} is the voltage at the point of MPP, and V_{OC} is the open circuit voltage. This ratio is depending on the solar cell parameters, but a commonly used value is 76%. By momentarily setting the current to zero, this algorithm is allowed to measure the open circuit voltage V_{OC}, and then calculate V_{MPP}. The drawbacks of this algorithm is the loss off energy when the load is disconnected, and the MPP is not always located at 76%.

3.1.2 Perturb and observe (P&O)

This is the most commonly used algorithm for MPP tracking, and is based on *perturbing* the voltage and *observing* the dP/dt. The direction of the derivative shows if the voltage is to high or to low, and the voltage can thus be decreased or increased until the MPP is reached, and thus the derivative is zero. Because this algorithm is based on perturbation, there will always be some oscillations even when the MPP is reached. In figure 3.1 a flow chart from [7] describing the P&O algorithm is presented.

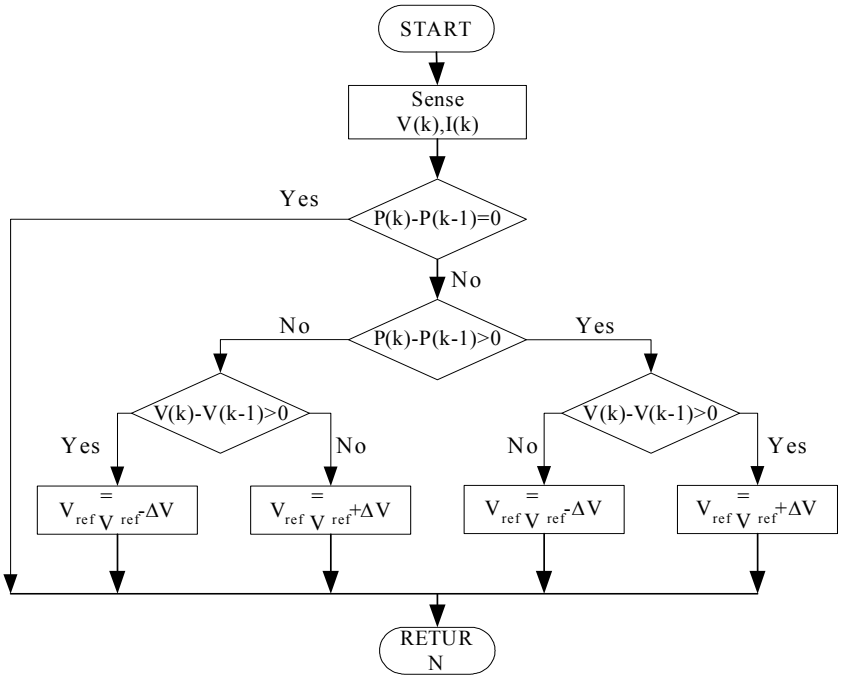

Figure 3.1: Flow chart of the P&O algorithm [7]

3.1.3 Incremental conductance (INC)

In the incremental conductance algorithm the drawbacks of the P&O algorithm with oscillations around MPP is removed. This is done by using the PV array's *incremental conductance* to compute the sign of $\mathrm{d}P/\mathrm{d}t$ without perturbations. In [7] it is shown that

$$P = VI \Rightarrow \frac{dP}{dV} = I + V\frac{dI}{dV}$$
$$At\ MPP: \frac{dP}{dV} = 0 = I + V\frac{dI}{dV} \Rightarrow \frac{dI}{dV} = -\frac{I}{V} \qquad (3.1)$$

Based on these equations the algorithm can determine if the MPP is reached, and stop perturbing the operating point. One disadvantage of this technique is the increased complexity compared to the P&O algorithm, and In figure 3.2 a flow chart from [7] describing the INC algorithm is presented.

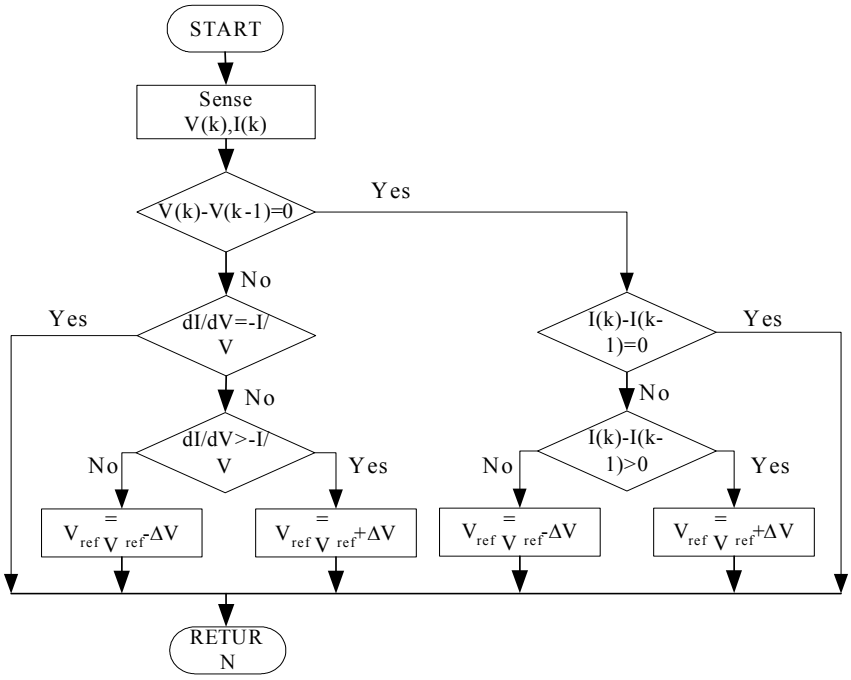

Figure 3.2: Flow chart of the INC algorithm [7]

3.1.4 Parasitic Capacitance (PC)

In every solar cell there is a *parasitic capacitance*, and this capacitance is used to determine the MPP. The parasitic capacitance technique uses the switching ripple to perturb the array. To account for the parasitic capacitance, the average ripple in the array power and voltage, generated by the switching frequency is measured and then used to calculate the array conductance. Then the incremental conductance algorithm is used to determine in which direction the operating point of the MPPT has to be moved. It can be seen that this is a refinement of the INC technique, and is thus at least as complex. A disadvantage of this method is the size of the parasitic capacitance is very small in each module, and thus it only comes into play in larger systems with several modules in parallel. There is also a problem when there are large input capacitors on the DC-DC converter, as these might overshadow the effect of the parasitic capacitance.

3.1.5 Efficiency of the MPPT techniques

Even though *incremental conductance* and *parasitic capacitance* is more complex than the other to methods, all the methods presented here are designed to be implemented in low cost systems with low computational capacity. Results presented in [11] indicates the efficiency of the three first methods, these are reproduced in table 3.1:

Table 3.1 - Efficiency of the MPPT methods [11]

	CV	P&O	INC
Array	88.1%	96.5%	98.2%
Simulator	92.7%	97.2%	98.5%

These results indicate that CV has a low efficiency, and the difference in efficiency between P&O and INC is small, but both have high efficiency. How the parasitic capacitance compares to these methods is unknown, but since it is a refinement of the INC method, one can assume an efficiency of the INC or even slightly better.

3.2 DC-DC Converter Control

The DC-DC converter is controlling the DC-link voltage, and in most cases trying to keep it at a constant voltage, but in the case when the DC-DC converter is used for MPPT, it's main purpose will be to operate the PV system at it's MPP. Therefore the feedback to this system is the PV panel power, not the DC-link voltage. So in the case where the DC-DC converter is controlled by an MPPT, the current drawn by the DC-AC converter will decide the DC-link voltage.

In the MPPT algorithms it is usually assumed that the duty cycle is the controlled variable, but it is also possible to have the peak switch current as the controlled variable. In the literature (described briefly in [12], and more in depth in [30]), these controls are described with feedback of the DC-link voltage, which is not the case when using an MPPT. Then the power is feed back to the MPPT, and the control of the DC-link voltage becomes an open loop control. The principal of these to techniques when using an MPPT as the controller is shown in the two figures below

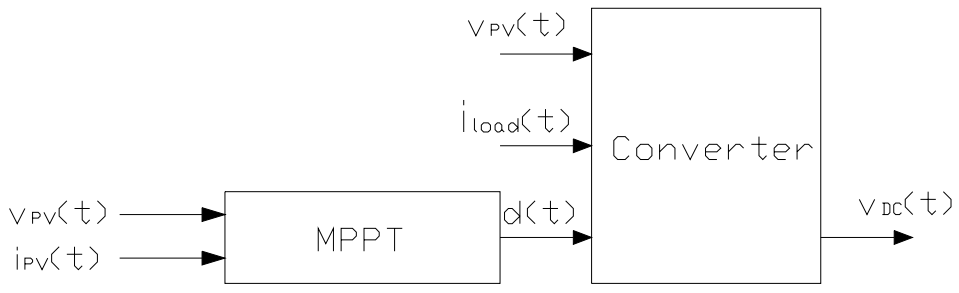

Figure 3.3: Direct duty-cycle control strategy for DC-DC converter

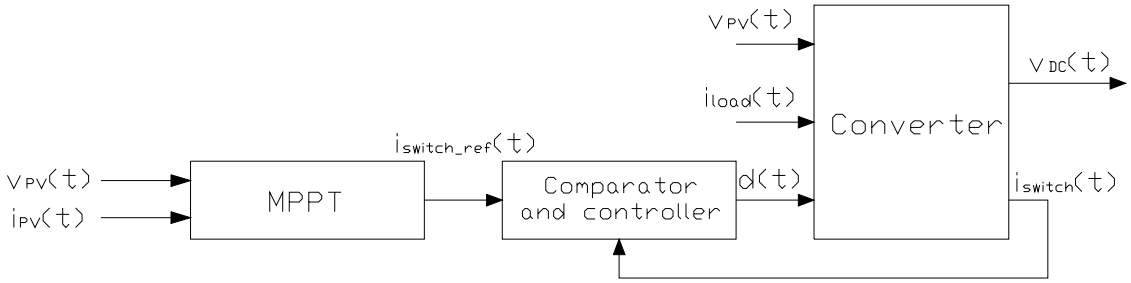

Figure 3.4: Peak switch current control strategy for DC-DC converter

By using the peak switch current control strategy there can be seen some advantages compared to the direct duty-cycle control, like better protection of the switches by limiting the current to acceptable levels and transformer saturation problems due to DC-bias tend to disappear. The drawbacks of this strategy is the need for an extra current sensor, and the control system must be able to accurately switch at the instant the current reaches the threshold current. It also has a susceptibility to noise, and therefore some filtering of the feedback is required which will introduce a delay.

3.3 DC-AC Converter control

In order to control the DC-AC converter inverter there are to major control strategies, *current control* (CC) and *voltage control* (VC). Where current control is the most common way to control grid connected VSI's. A current controller has the advantage of being less susceptible to voltage phase shifts and to distortion in the grid voltage, thus it reduces the harmonic currents to a minimum. Whereas voltage control can result in overloading of the inverter due to small phase errors, and large harmonic currents may occur if the grid voltage is distorted. If operated in standalone mode, voltage control would be a natural choice, but when operated in grid connected mode, current control is the most robust control. Therefore only *current controlled VSI's* (CC-VSI) will be considered here.

Some of the control schemes presented in this chapter will involve the use of transformations between the 3-phase system and different two-phase systems, therefore the concept of transformation is described first.

Common to all the control strategies described in this chapter is a clearly separated current error compensation and voltage modulation part (PWM modulation). This concept allows one to exploit the advantages of open-loop modulators separate from the current error compensation loop, and therefore this is described next.

In the last chapters three different current control methods are described. The first two are described in [7,12,13,14,], where the first is a PI controller using a rotating reference frame, the second is a proportional resonant (PR) controller using a stationary reference frame.

The third method is described in [15], which is a state feedback controller working in a rotating reference frame. Other control strategies like hysteresis and dead-beat control has also been reported ([15,16]), but these methods will not be discussed further in this thesis.

3.3.1 Transformations

In order to avoid controlling three current/voltages separately, transformations from a three-phase system to different two-phase systems have been made. These are based on the fact that in a balanced three-phase system there are only two independent current/ voltages, thus the third current/voltage can be expressed by the other two. These systems are often referred to as reference frames, where the frame is the axis system of the transformed system.

Stationary reference frame (Clarke transform)

When a three-phase system is transformed into a two-phase system, this is often called a abc to $\alpha\beta$ (or $\alpha\beta 0$ when the zero vector is used) transform, or a transform into the *stationary reference frame*. Both the three-phase and the two-phase system is said to be stationary, because the axes is locked in one position, but the term *stationary reference frame* usually refers to a two-phase stationary reference frame.

The transformation is made by applying the Clarke transformation in eq (3.2), where the three-phase quantities must be phase values, i.e not line values. By inverting the coefficient matrix, the three-phase quantities can be found as a function of the two-phase quantities.

$$\begin{bmatrix} X_\alpha \\ X_\beta \\ X_0 \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \cdot \begin{bmatrix} X_a \\ X_b \\ X_c \end{bmatrix} \tag{3.2}$$

The transformation can be thought of as a change of coordinate system, from a three axis (phase) system to a two axis (phase) system as shown in figure 3.5. It can be seen from the abc system that only two phases is needed to express the vector X_{abc}, and thus it can be expressed in the $\alpha\beta$ system as the vector X_{ab} without any loss of information. In the figure ω is the angular speed of the vector, and θ is the instantaneous angle of the vector. If X is the grid voltage, then ω represents the grid frequency, and θ represents the instantaneous phase angle.

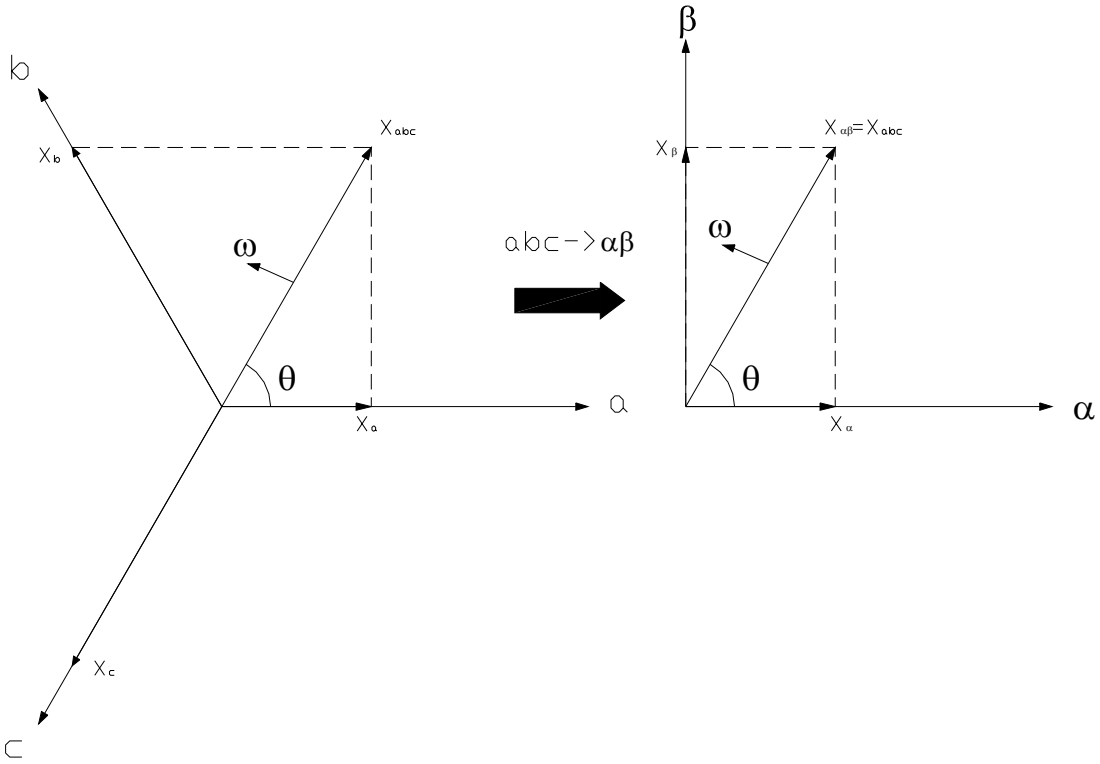

Figure 3.5: Abc to αβ transformation

Usually the three-phase quantities are assumed symmetrical, and thus the zero-sequence component can be ignored. When there is no zero-sequence component the instantaneous active and reactive power is given by eq (3.3) and (3.4). The factor 3/2 is introduced in order to have the power from all three phases.

$$p_{\alpha\beta} = \frac{3}{2}\left(v_\alpha i_\alpha + v_\beta i_\beta\right) \tag{3.3}$$

$$q_{\alpha\beta} = \frac{3}{2}\left(v_\beta i_\alpha - v_\alpha i_\beta\right) \tag{3.4}$$

Synchronous reference frame (Park transform)

In this system the axis system is no longer locked, and rotates following an arbitrary vector, hence the term “synchronous reference frame”. It is sometimes also termed the dq system (or dq0 if zero-vector is used).

This transformation is widely used in motor drives, where the axis system follows for instance the rotor position or rotor flux. In grid connected inverters it is most common to lock the axis system to a voltage or current (usually the grid voltage). In figure 3.6 the d-axis is locked to the vector X_{ab}, and therefore $X_d=X_{ab}$ and $X_q=0$. The axis system will then rotate with an angular speed of ω, and have an instantaneous angle of θ (referred to the stationary system).

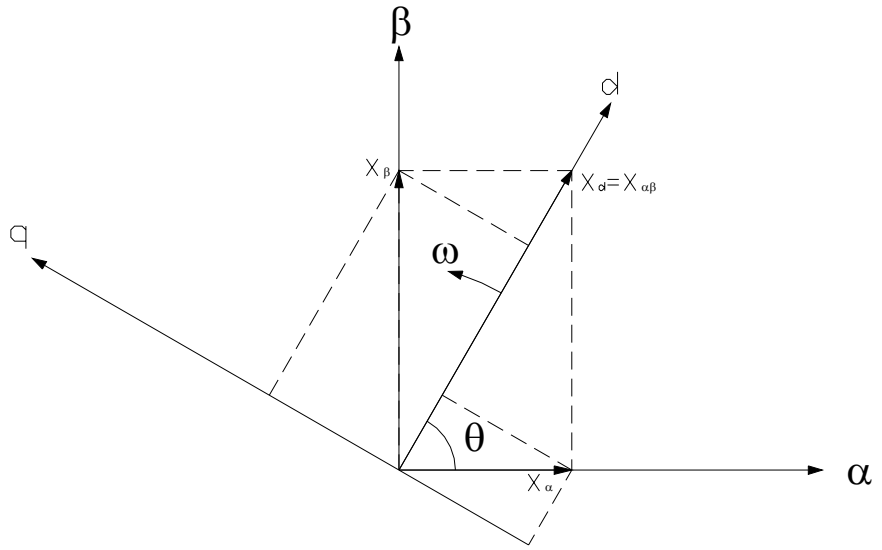

Figure 3.6: αβ to dq transformation

The transformation is made using the Park transformation shown in eq (3.5), where the stationary quantities can be found as a function of the synchronous quantities by inverting the coefficient matrix.

$$\begin{bmatrix} X_d \\ X_q \\ X_0 \end{bmatrix} = \begin{bmatrix} \cos(\theta) & \sin(\theta) & 0 \\ -\sin(\theta) & \cos(\theta) & 0 \\ 0 & 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} X_\alpha \\ X_\beta \\ X_0 \end{bmatrix} \tag{3.5}$$

θ - Instantaneous phase angle

If the dq-axis system is locked to the grid voltage, the axes will rotate with the frequency $2\pi f_g$, and the dq values will become DC-values stationary. If it is still assumed that the three-phase quantities are symmetrical, then the zero-sequence component is still zero, and the active and reactive power is given by eq (3.6) and (3.7)

$$p_{dq} = \frac{3}{2}\left(v_d i_d + v_q i_q\right) \tag{3.6}$$

$$q_{dq} = \frac{3}{2}\left(v_q i_d - v_d i_q\right) \tag{3.7}$$

These equations assume that both the voltage and the current is transformed into the dq-system using the same reference frame. When the reference frame is oriented at the voltage vector, then the d-axis current will represent current in phase with the voltage, and thus it represents the *active power* in the circuit. The q-axis current will then represent current which is out of phase with the voltage, and thus it represents the *reactive power* in the circuit.

It should be noted that other versions of the Park transform exists, and in these the orientation of the dq-axis on the X_{ab} vector might differ. This can for instance lead to having the active power controlled by the q-axis, but only the transform given by eq (3.5) will be used throughout this text.

3.3.2 Pulse Width Modulation (PWM)

The PWM modulators are open-loop voltage controllers, and the most common methods for PWM modulation is *carrier based PWM (CB-PWM), space vector modulation (SVM)* and *random PWM*. The fundamental difference between these methods are described in [31], and a summary of the operation in the linear modulation range is presented.

Carrier Based (CB-PWM)

CB-PWM is the basic and most common way to modulate the switching signals. This method can be divided into to methods, *sinusoidal PWM* and *CB-PWM with zero sequence signal (ZSS)*. With sinusoidal PWM, three reference sinusoidal signals are compared to a triangular wave generating logical signals controlling the switches. Whereas the ZSS method is based on the sinusoidal PWM, with the addition of a zero sequence signal of third harmonic frequency. The injection of the third harmonic is not producing phase voltage distortion or affecting load average currents. It does however extend the linear region of operation, reduce the average switching frequency and reduce the current harmonics.

The ZSS method can be further divided into continuous and discontinuous modulation (DPWM), where the most well known method of continuous modulation is the method with sinusoidal ZSS, but also triangular ZSS is used. A ZSS amplitude of 1/4 of the fundamental corresponds to the minimum of output current harmonics, and with 1/6 it corresponds to the maximum linear range. Discontinuous modulation is formed by unmodulated $60°$ segments (converter power switches do not switch) phase shifted from 0 to $\pi/3$, and can reduce the average switching frequency and switching losses, but has higher harmonic content at lower modulation ratios. The maximum output voltage in the linear region for the sine PWM and the PWM with ZSS is

$$V_{LL\_sine} = \frac{\sqrt{3}}{2\sqrt{2}} V_{DC} = 0.612 \cdot V_{DC}$$
$$V_{LL\_ZSS} = \frac{1}{\sqrt{2}} V_{DC} = 0.707 \cdot V_{DC} \qquad (3.8)$$

The principle of the generation of switch signals is shown in figure 3.7, where a triangular carrier signal is compared to sinusoidal signals representing the phase voltages. If the sinusoidal is larger than the carrier wave, then switch turns on, and if less it turns off.

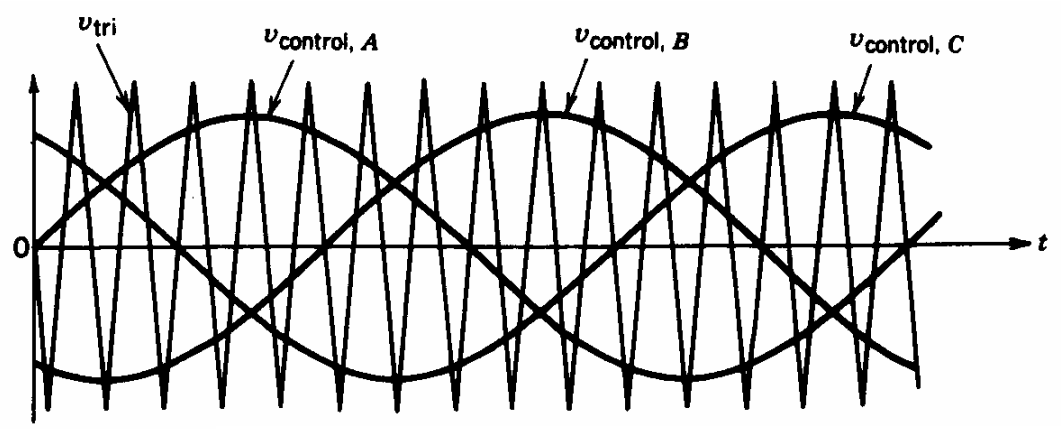

Figure 3.7: Generation of Carrier Based PWM signals [31]

Space Vector Modulation (SVM)

SVM is a method based on space vector representation of the converter AC-side voltages, and it is shown in [31] that the difference between SVM an CB-PWM is only the treatment of the three-phase quantities. CB-PWM operates in terms of three-phase natural components, whereas SVM uses an artificial vector transformation. With a three-phase two level inverter there are eight possible switching states, made up of six active and two zero switching states. There are several different methods for creating the switching pattern, the only difference between them is the placement of the zero vectors. The different switching states is shown in the figure below.

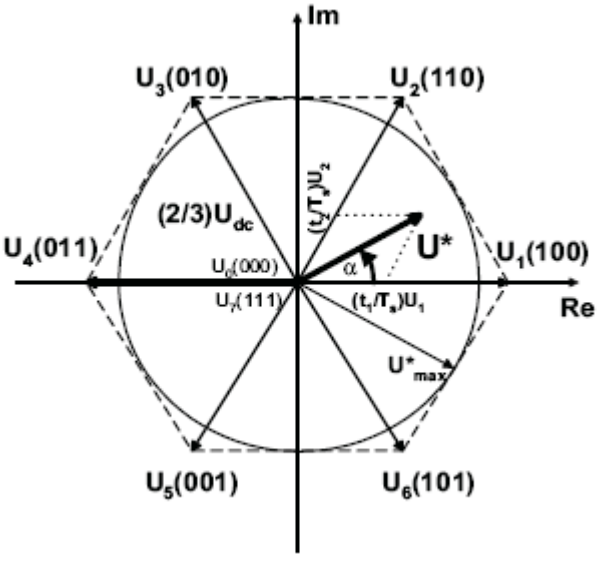

Figure 3.8: Space vector representation of output voltage. [31]

The most popular method is the three-phase SVM with symmetrical placement of zero vectors (SVPWM). This method corresponds to CB-PWM with triangular ZSS of 1/4 amplitude, and has almost equal harmonic content as CB-PWM with sinusoidal ZSS. It is

easy to implement in a microprocessor, and is therefore the natural choice of SVM. Two other techniques for SVM is vector modulation with V_{N0}=0 (voltage between converter neutral and grid neutral=0, equal to sine PWM), and vector modulation with third harmonic (equal to CB-PWM with sinusoidal ZCC), but these are easier to achieve with CB-PWM. Two-phase SVM is another method which is equivalent with the discontinuous CB-PWM with ZSS(DPWM). This method will have only one zero state per sampling time, and therefore a simple calculation, but is best used at high modulation ratios. The maximum line voltage with the SVPWM and also the two-phase PWM is

$$V_{LL\_SVPWM} = \frac{1}{\sqrt{2}} V_{DC} = 0.707 \cdot V_{DC} \tag{3.9}$$

There is also a variant of SVM called adaptive SVM (ASVM), which combines different SVM techniques into one universal solution. This method gives full control range including overmodulation and six-step operation (square wave operation) and higher efficiency of the inverter, but the inverter will only mostly operate in the upper linear area of modulation, therefore this method is not of interest.

The generation of the switch signals is for the SVM based on a mathematical approach, which can easily be implemented into a microprocessor. For details on this the reader is referred to [31] where this is described in detail.

Random PWM

Random PWM is based on randomly varying the switching period, and thus creating harmonics more evenly distributed throughout the frequency spectrum. This has advantages as reducing the acoustic noise, and compliance with standards defining limits for emission of conducted and radiated EMI may be obtainable with less filtering and shielding efforts. The implementation of random modulation is strongly dependent on the hardware used for the PWM, and the distribution of harmonics is not well defined as it is for fixed carrier period PWM.

3.3.3 PI Controllers

PI controllers can be applied both in the *stationary* ($\alpha\beta$) or *synchronous* (dq) reference frame, but by applying them to the dq system there will be DC currents stationary, and the PI compensators are able to reduce the stationary error of the fundamental to zero. This is not the case with PI controllers working in the $\alpha\beta$ system, where there is an inherent tracking error of phase and amplitude. Therefore current control in a synchronous (rotating) reference frame, using PI controllers is the typical solution in 3-phase grid connected inverters.

An advantage of current control in the dq system is individual control of active and reactive power by orienting the dq frame on the grid voltage (see chapter 3.3.1). Where the active power is controlled by the d-axis current and the reactive power is controlled by the q-axis

current. Some well known drawbacks of this method is the need for many transformations, decoupling in three-phase converters, and limitations in compensating the low harmonics in order to comply with power quality standards. In its general form the PI controller is defined as

$$H_{PI}(s) = K_p \frac{1 + T_i s}{T_i s} \tag{3.10}$$

If harmonic compensation (see 3.4) is desired, it is possible to add harmonic compensators with the same method as described above, but now using reference frames rotating at the desired harmonic frequency.

3.3.4 PR controllers

The proportional resonant (PR) controller is a new type of controller described in [7,12,13,14]. In this approach the PI DC-compensator is transformed into an equivalent AC-compensator (using the transforms described in 3.3.1), thus giving the same frequency response characteristics in the bandwidth of concern. By using this method the complexity of the calculations will be reduced, and the cross couplings are removed. The PR controller is defined as

$$H_C(s) = K_P + K_1 \frac{s}{s^2 + \omega^2} \tag{3.11}$$

In combination with the PR controller it is often added a harmonic compensator (HC). The harmonic compensator consists of a sum of generalized integrators (GI), which are tuned to have almost infinite gain at different frequencies, called resonant frequencies. Outside these frequencies the GI's have almost no attenuation. This is an interesting feature of the GI, because it does not affect the dynamics of the PR controller outside the tuned frequency. Thus one can add as many GI as needed without affecting the overall system dynamics. The harmonic compensator is defined as

$$H_h(s) = \sum_{h=3,5,\ldots} K_{Ih} \frac{s}{s^2 + (\omega \cdot h)^2} \tag{3.12}$$

This combination of PR controllers and harmonic compensators, can be tuned to react to the fundamental frequency for a good regulation, and tuned to harmonic frequencies in order to compensate them (see 3.4).

3.3.5 State feedback controller

In the methods described above where the control processes have a mathematical description in the form of transfer functions, it is not possible to observe and control all of the internal phenomena involved in the control process. Therefore the state space method

is gaining more and more attention, because this method provides a uniform and powerful representation in the time domain of multivariable systems of arbitrary order with linear, nonlinear, or time varying coefficients. There exist different ways to write the state space equations, but one way described in [32] is

$$\begin{aligned}\dot{\mathbf{x}}(t) &= \mathbf{A}\mathbf{x}(t) + \mathbf{B}\mathbf{u}(t) \\ \mathbf{y}(t) &= \mathbf{C}\mathbf{x}(t) + \mathbf{D}\mathbf{u}(t)\end{aligned} \tag{3.13}$$

$\mathbf{x}(t)$: State vector
$\mathbf{u}(t)$: Input vector
$\mathbf{y}(t)$: Output vector
A: State coupling matrix
B: Input coupling matrix
C: Output coupling matrix
D: Input to output coupling matrix

With this system description also the initial conditions are easy to implement, and the state feedback controller can work in both stationary and synchronous reference frame. When using this method the poles of the closed loop system can be placed in predetermined locations in the s-plane (or z-plane when discretized), and thus controlling the characteristics of the response of the system.

Also with this method harmonic compensation (see 3.4) can be achieved, by including a model of the system at the desired harmonic frequency.

3.4 Harmonic compensation

Nonlinear loads have become a large part of the load profile of the grid nowadays. These loads draw currents with a harmonic spectrum where the harmonic above the fundamental becomes distinctive. When these currents go through the impedances of the grid, they create voltage harmonic drops which deteriorate the grid voltage. This deterioration of the grid voltage will affect all the grid connected equipment, and if the harmonics are sufficiently large, it can lead to damage or deterioration of this equipment. It can therefore be understood that this situation is undesirable, and some sort of compensation is needed in order to keep the harmonics at a low level.

The classical solution to this problem is installing passive filters, but these filters have some drawbacks. The source impedance will strongly affect the compensation characteristics, and they are susceptible to undesirable series and parallel resonance with source and load. In order to alleviate these problems active filters have become more and more interesting, because they are flexible and have the ability to adapt to varying situations. An active filter can be a VSI programmed to deliver currents at the desired harmonic frequencies (harmonic compensation), and thus reduce the harmonic voltage drops. Which means that any grid connected VSI can be used as an active filter.

In order to compensate for any harmonic drawn by the load, the harmonic currents needs to be isolated and their phase and amplitude must be known. This can for instance be achieved using filtering or some FFT algorithm. Once the harmonic current is known, it can be compensated using for example one of the methods described about current control in chapter 3.3.

3.5 Grid synchronisation

The inverter delivers current to the grid, and the synchronization of the current with the grid voltage is important to:

- deliver power at a power factor within the limits in the standards, or within limits given by the utility if there is need for reactive power compensation.
- reduce the harmonic current content, by applying a “clean” reference current.
- minimize the grid connection transients.

In [7,18] several methods for grid synchronization are presented. These are summarized here, discussing their major advantages and disadvantages.

3.5.1 Filtered Zero Cross Detection (ZCD)

With this method the *zero-crossing* of the voltage is registered, and the phase angle is calculated. The method is easy to implement and uses little computational capacity, but the technique has several drawbacks. Since the technique is based on zero-crossing detection, the phase angle is only updated two times per period of the grid voltage frequency, and therefore the dynamic performance of this technique is low. Also filtering has to be applied in order to detect the zero-crossing of the fundamental frequency, and therefore a delay is introduced. This can be avoided using special high order predictive filter without delay, but then the complexity becomes very high.

3.5.2 Filtering of grid voltages

By filtering the grid voltage in different reference frames, such as the two-phase stationary or the synchronous frame, the phase angle can be extracted directly using the arctangent function. The filtering is done in either the stationary frame, or in the synchronous where there are DC-components. The arctangent function is always applied to the stationary frame, thus giving the instantaneous phase angle. Therefore when the filtering is done in the synchronous frame, the signal must be transformed back into the stationary frame before applying the arctangent function.

In [18] it is reported improved performance over the zero-crossing method, but the technique encounters some difficulties in extracting the phase angle when grid variations and or faults occur in the network. Another drawback of this method is the use of filtering, since most filter types introduces a delay, the calculated phase angle will lag the real phase angle.

3.5.3 Phase Lock Loop (PLL)

A *phase lock loop* (PLL) produces an output signal which synchronizes in phase and frequency with the input signal, using a negative feedback loop. The PLL controls the internal signal such that, the error in phase between input and output is kept to a minimum, and the frequency is equal at input and output. A basic PLL circuit often consists of three components, a *phase detector*, a *loop filter* and a *voltage controlled oscillator*. This basic circuit is shown in figure 3.9.

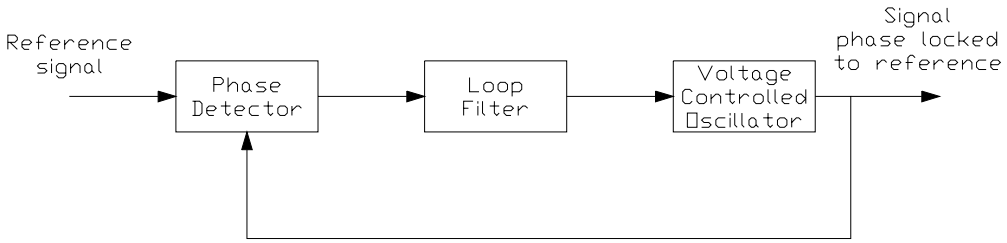

Figure 3.9: A basic PLL circuit

The phase detector is implemented by transforming the voltages into the dq system. By using the phase locked angle in the dq transformation, the phase difference between the reference signal and the phase locked signal can be extracted by applying the arctangent function. This gives the exact phase difference, but the phase difference can also indirectly be found by recognizing that the phase difference is zero when V_q equals zero. In three-phase systems the transformation is easy to implement, but in single phase systems there is only one voltage, so the orthogonal component of the voltage has to be found artificially.

The loop filter can be some sort of regulator, which brings the phase error to zero. This is usually a PI regulator, but also higher order regulators can be used. A higher order system increases the dynamics of the system and enhances the filtering capabilities, but it also increases the complexity. When choosing the controller order, one must weigh what is most important of the latter. When using a PI controller, this gives a second order system, and then the PLL bandwidth and damping factor can be set using linear system theory.

After the loop filter, which output is the frequency, a voltage controlled oscillator is applied. This is usually a simple integrator, which gives the phase locked angle as output. With the PLL no delays are introduced, so the phase locked angle will be in phase with the grid angle.

A schematic model based on one presented in [7] is shown in figure 3.10, and shows the basic principle of a phase lock loop with its transformations of the three-phase voltages. In this loop the arctan2 function is applied as the phase detector, giving the exact phase difference.

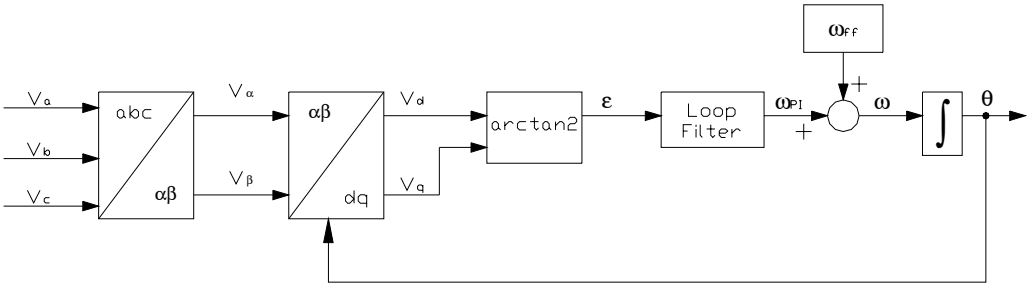

Figure 3.10: Schematic of a phase lock loop (PLL) with transformations

This algorithm has better rejection of grid harmonics, notches and any other kind of disturbances then the previous methods, but during grid unbalancing further improvements has to be done. In the case of a unsymmetrical voltage fault, the second harmonics produced by the negative sequence will propagate through the PLL and become reflected at the output. This means that in order to alleviate this problem, the zero-sequence signal has to be filtered out, thus the PLL is only estimating the phase angle of the positive sequence signal.

3.5.4 Adaptive PLL

In [18] a more advanced PLL structure is described, based on a adaptive algorithm. In this method three PLL systems is used, one for each phase. Where there are three control units that individually control the frequency, phase angle and voltage magnitude of the grid voltage. This gives precise information about each phase, and therefore this method is suitable for grid monitoring, and thus islanding detection (see chapter 3.6) and safety improvements. The disadvantage of this structure can be the large algorithm needed to implement the controllers (3x3 controllers in this case, but it can be less in other structures), and a moving average filter that is involved in the controllers which is computationally heavy but very precise.

3.6 Anti Islanding

Islanding can be defined as the continued operation of a distributed generation unit while the mains are tripped due to fault conditions or for maintenance purposes (from[19]). Unintentional islanding of the PV system is not desirable because it can damage equipment which remains connected to the inverter, and it can lead to dangerous situations since the grid may be assumed deenergized. It is also a problem if the supply system is reconnected, because then the PV system is likely to be out of phase, and large currents can be injected into the PV system.

A non islanding inverter is defined as an inverter that ceases to operate within a certain time after an islanding situation has occurred. In order to detect the islanding situation, different algorithms can be implemented in the inverter control. In [20] these algorithms are divided into two major groups: remotely controlled (communication based) and locally

built-in detection schemes. This survey is dealing with the inverter as a locally controlled device, so the communication based detection schemes are of no interest here. The local detection schemes can be further divided into two groups, active and passive.

3.6.1 Passive

The passive methods are based on local measurements, and the most common methods are

- Frequency limitations
  - Magnitude change
  - Rate of change
  - Phase shift
- Voltage limitations
- Power
  - Change of active power
  - Change of reactive power
  - Power factor (P/Q) and (df/dP) indices
- Harmonic content changes

These methods are usually easy to implement and they work without affecting the overall system, unless the limits are to strict and the inverter trips without being in islanded mode. One of the main limitations with these methods is that each of the methods have operating regions where they are not able to detect an islanding situation within the given time limits. This region is called the non-detection zone (NDZ). The impact of these zones are usually neglicible, but they can in some cases (particularly during balanced load conditions, when the load matches the power produced by the inverter) become a problem. Often combinations of these methods are used in order to reduce the NDZ.

3.6.2 Active

In these method disturbances is injected into the supply system in order to locally detect islanding conditions based on system responses. The most common methods are based on one of the following principles.

- Impedance measurement
- Voltage variation
- Frequency variation
- Output power variation

One of the advantages of these methods is increased ability to detect islanding even during balanced load conditions, and thus decrease or even remove the NDZ. One of the main problems with the active methods, is the interference of the disturbances introduced by

multiple distributed resources connected to the same grid, and other side effects can also be found depending on the method. Not much experience has been gained with these methods yet, but this is an area of growing research activity.

3.7 Digital Signal Processing

In todays control of converters and drives it is mostly digital controllers which are used. The use of digital controllers is convenient when implementing new control systems, since the control can be programmed and uploaded into a digital controller. Thus it is easy to make changes to the control, and problems with non ideal analog components is removed. On the other hand when using a digital control system then everything is in the discrete domain, which means one must change the system models and the way of thinking into the discrete domain. The focus in this chapter is on the implementation of the control system into a DSP.

3.7.1 DSP program

The control program of a DSP is often written in the high level language like C or C++, and sometimes pieces of assembly code might be used for special purposes. In order to have the code readable it is important to organize the code in a logical manner. In C++ the program code can be organized in a structure where each specific function is given its own class, and on a higher level it can be organized in separate files. In this way the code is easier to read and it becomes easier to change the code at a later time. This can also make it easier to test different algorithms, since it is then possible to change one function without making changes to the rest of the code.

Interrupts

In a continuous system the calculations are continuous, but in the DSP the calculations are executed at fixed (discrete) intervals. These intervals are called interrupts, and each interrupt is started when a defined event occurs. The interrupts may be executed at the same frequency, but they can be phase shifted, or they can run at different frequencies. In the DSP there are a set of predefined triggers for the interrupt, and each interrupt has a priority based on the event that triggered it. The priority means that if two interrupts are pending, then the one with the highest priority will be executed first.

All the algorithms needed to run the converter is executed in the interrupts. Which algorithms that are executed in the different interrupts, depend on how fast they must executed, and if some of the algorithms need to be phase shifted to one and another. An example is the controllers which will usually be driven at the switching frequency in order to have the fastest possible response, while the ADC (Analog to Digital Converter) can be executed at the same frequency, but 180 degrees phase shifted in order to have the measurements ready before the calculations start. In this way the calculations will have fresh measurements, but will not be delayed by the measuring.

Superior Control

In order to make everything run when it should run, and make sure things are not executed if they are not intended to, some superior control is needed. This superior control can involve a state machine which will have a set of defined states the system can be in. The state machine will handle the transaction between the different states, and make sure no illegal state transactions occur. In each state the superior control has defined which algorithms that are allowed to run, and there is also some logic which tells when it is allowed to or must leave that state.

An example of a superior control with a state machine is shown in figure 3.11, this shows in principle how the superior control works. The triangles in the figure represent the state machine, and the squares represent the events which will occur in each state. The different states can briefly be described as follows.

DSPERROR - This is the state the system is operated in once a serious system error occurs. The system will here be disabled, and must be manually restarted.

DSPRESET - The system is transferred here when the user or the system needs to reset the system for some reason. In this state the system is disabled, and once the system is disabled it is automatically transferred to the next state.

VALUESINIT - In this state the initial values for the measurements is sat, and offset values for the ADC is found. When this is done the system is automatically transferred to the next state

CONVINIT - In this state the converter hardware is initialized if needed. When this is done the system is automatically transferred to the next state

CONVCTRLINIT - In this state the initial values for the control system is sat. When this is done the system is automatically transferred to the next state

CONVREADY - When the superior control has reached this state everything should be initialized properly, and the converter should be ready to start. The system will be in this state until the user sets a start bit. In this state it is also made sure that none of the system variables is changed from their initial values before the system is started.

CONVRUNNING - When the system reaches this state, the converter starts running. All algorithms concerning the operation of the converter is executed in this state. The system will be in this state until the user sets the stop bit, or until a system error occurs and the system is sat in the error state.

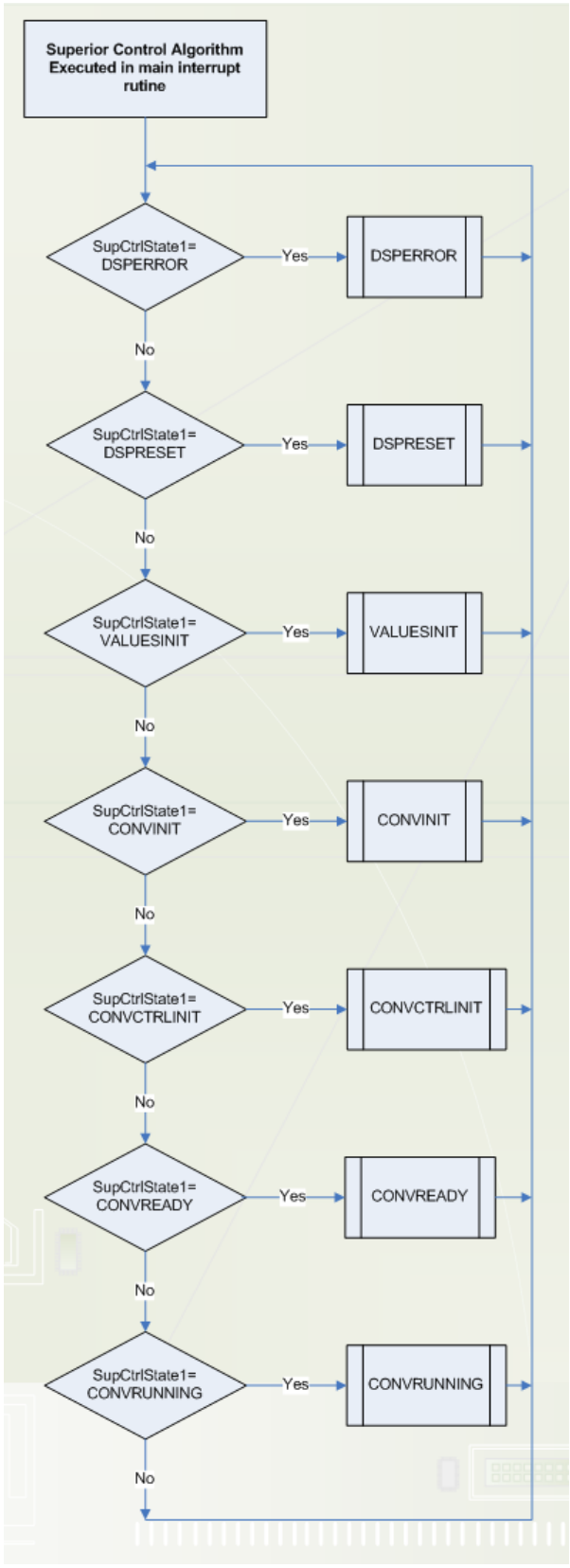

Figure 3.11: Flow chart of superior control with state machine

3.7.2 Measurements and analog to digital conversion

In a DSP the measured values has to be sampled before they can be used in any calculations, and this is done using a *analog to digital converter* (ADC). When using an ADC it is important to adjust the offset of the measurements before the measurements begin. If this is not done, one can risk having a shift in the measured value compared to the actual value, and in a three phase measurement it can lead to the measured values having a phase unbalance, even though the real values don't.

According to the sampling theorem the sampled signal should not contain frequencies above half the sampling frequency in order to avoid *aliasing*. In order to avoid this the most common solution is to use an anti aliasing filter to remove higher frequencies before it is sampled. This filter should then have a corner frequency of

$$\omega_c \leq \frac{\omega_s}{2}$$

By using an analog filter to avoid anti aliasing, a phase delay is introduced in the measurement, and the circuit is more complicated and expensive due to the extra filters. Therefore it is desirable to avoid these filters if possible.

A method called *synchronous sampling* [17,22] is a much used method in digital drives in the industry. With this method the ADC is synchronized at the top or bottom peak of the triangular PWM carrier signal. In this way the ADC conversion is made at an instant when the switching harmonic currents are negligible. This gives a measurement which is close to its averaged value, and with negligible ripple. Thus the need for an anti aliasing filter is reduced, and is therefore not needed for the measurements.

3.7.3 Discretization

In order to analyse the system in the discrete domain, the continuous models will have to be transformed into discrete models. There are several methods available for this, some based on numerical integration and some on numerical derivation. Two of the most basic methods used are the *Euler's forward* and *backward* numerical integration methods, which are first order transformations, meaning that they utilize only one sample per sampling interval in the calculations. These methods are quite accurate when the sampled signal has a frequency which is much lower than the sampling frequency, but the accuracy decreases as the sampling frequency approaches the frequency of the sampled signal.

Another method based on numerical integration called the *trapezoidal method* (also called the *bilinear transformation* or *Tustin's method*) is much used. This is a second order transformation, which means it uses two samplings during each sampling interval. Therefore this method is more accurate, and will not be as frequency dependent as the Euler methods, and will therefore be the preferable method. The transformation from the s-plane to the z-plane is achieved by inserting the relation in eq (3.14), into the continuous time model.

$$s = \frac{2}{T_s}\frac{z-1}{z+1} \tag{3.14}$$

When the system is transformed into the z-plane it is a small step left in order to implement it in a computer algorithm. It can be transformed into the discrete time domain by introducing the z-operator as a time shift operator, where z means a positive time shift and 1/z means a negative time shift. The transfer function can then be used on discrete time input and output values by using the relations shown in (3.15). The resulting expression will be a difference equation, which can easily be implemented in a computer algorithm. It should be noted that this is not the mathematically correct way, but it yields the correct answer in an easy manner.

$$\begin{aligned} zx[k] &= x[k+1] \\ z^{-1}x[k] &= x[k-1] \end{aligned} \tag{3.15}$$

3.7.4 Discrete filtering

The measured values might be in need for some filtering in order to remove unwanted frequency components from the measurements before they are processed in the DSP. Therefore some kind of filtering might be necessary, and in order to avoid the drawbacks of the analog filters, a digital filter implementation will be more appropriate.

There are lots of filtering techniques available, from simple first order to complex higher order filters. If it is not necessary to have a very sharp cutoff, a simple first order filter will usually do an appropriate job. Therefore only the implementation of this filter will be found here. Based on the continuous model of a first order filter as shown in (3.17), the z-transformation can be applied and a computer based algorithm can easily be found.

$$H_F(s)\frac{1}{1+sT_F} \tag{3.16}$$

The bilinear transformation is found by substituting (3.14) into (3.16)

$$H_F(z) = \frac{T_s + z^{-1}}{(T_S + 2T_F) + (T_S - 2T_F)z^{-1}} \tag{3.17}$$

Next the time shift operator z is used as shown in (3.15), and a difference equation is found.

$$y[k] = a_1 x[k] + a_2 x[k-1] + b_1 y[k-1] \tag{3.18}$$

$$a_1 = a_2 = \frac{T_S}{2T_F + T_S}$$
$$b_1 = \frac{T_F}{2T_F + T_S} - \frac{T_S}{2T_F + T_S}$$

The difference equation in (3.18) can then easily be implemented in a computer algorithm, and if the sampling frequency is high compared to the corner frequency, the filter constant can be used from the continuous model.

3.7.5 Discrete PI Regulator

Several places in the control algorithm there will be a need for PI regulators. In (3.19) the transfer function of a PI regulator is shown.

$$\mathrm{H_{PI}}(s) = K_P \frac{1 + T_i s}{T_i s} \tag{3.19}$$

In order to use this in a computer algorithm it must be discretized. By using the same procedure as with the discretization of the filter, the z-transformed model and a difference equation can be found.

$$H_{PI}(z) = \frac{\left(K_P T_S + 2K_P T_I\right) + \left(K_P T_S - 2K_P T_I\right) z^{-1}}{2T_I - 2T_I z^{-1}} \tag{3.20}$$

The difference equation of this is the same as found in (3.18), but with these coefficients

$$a_1 = \frac{K_P T_S}{2T_I} + K_P$$
$$a_2 = \frac{K_P T_S}{2T_I} - K_P$$
$$b_1 = 1$$

3.8 P&O algorithm optimization

Since the efficiency of the INC and P&O algorithm is so close, and the P&O algorithm is much easier to implement it will be analysed further. In order to have the efficiency of the algorithm as high as possible, the algorithm would in an ideal case have an indefinitely small duty cycle step, and be executed indefinitely often. This however is not possible because of the characteristics of a real system. Their will be noise, time delays of different sorts and changes in operating conditions which has to be considered. Therefore the minimum step size and duty cycle which can be used without risking to “confuse” the algorithm should be calculated.

3.8.1 Minimum time step

A disadvantage of the P&O algorithm is a tracking error which might occur during rapid changes of the solar irradiance. According to [24] the error occurs when the change in irradiance during one sampling interval is larger and in the opposite direction of the power change due to the duty cycle modulation. This will "confuse" the MPPT, and it will adjust the duty cycle in the opposite direction. In order to reduce the risk of confusing the MPPT during these changes, the sampling interval of the P&O algorithm should be sat as low as possible without causing instability. In [23] it is stated that the system sampling interval should be sat according to the converter's dynamics, so that after each duty-cycle perturbation the system is allowed to reach the steady state operation before the next perturbation. If the sampling is sat lower than this, the MPPT might become "confused" by the PV array + converter transient behaviour.

In order to find the time at which the system has reached steady state one has to look at the system model. It is shown in [23] that the array power is proportional to the PV voltage squared, as shown in (3.21). Therefore by finding a model for the control to PV-array voltage, one can calculate the time before the transients caused by the control perturbation has reached a certain value. When the system has reached this value, the MPPT can safely run without being confused by the system dynamics.

$$\hat{p}(t) = -\frac{v_{pv}^2(t)}{R_{MPP}} \tag{3.21}$$

Where R_{MPP} is the steady state equivalent resistance of the PV load at the quiescent operating point, where it is assumed that the operating point is in the vicinity of the MPP. This relation is given in (3.22)

$$R_{MPP} = \frac{V_{MPP}}{I_{MPP}} \tag{3.22}$$

The sampling interval can now be found by defining a region around the steady state value of $\hat{p}(t)$ which must be reached before a new sampling is allowed.

3.8.2 Minimum duty cycle step

When the sampling time of the algorithm is found, it is the duty cycle step size which will appoint the speed of the MPPT. A larger step size gives a faster response, but more steady state ripple and thus higher steady state loss. The minimum step size is constrained by the maximum possible change in irradiance between each sampling. By using a to small step size, the chance of confusing the MPPT during rapid changes in irradiance gets bigger. In [24] a criteria for avoiding the confusion of the MPPT is found.

$$\left|\Delta P_d\right| > \left|\Delta P_S\right| \tag{3.23}$$

The criteria in (3.23) states that the change in PV power due to the perturbation of the duty-cycle must be larger than the change in PV power due to irradiation during one sample period. In [24] eq (3.23) can be expanded and an equivalent expression is found (see [25] for explanation of the right hand side).

$$\left|\left(\frac{1}{2}\frac{\partial^2 i_{pv}}{\partial^2 v_{pv}}\bigg|_{MPP} V_{MPP} - \frac{1}{R_{MPP}}\right)\right|(H_0 \cdot \Delta d)^2 > V_{MPP} K |\Delta S| \tag{3.24}$$

Where H_0 is the DC gain of the system (4.2) and K is a material constant. For further detail on this the reader is referred to [24] and [25].

3.9 PLL PI controller Optimization

When choosing the controller parameters for the PLL, a closed loop design which gives fast tracking and good filtering characteristics should be pursued. These two requirements cannot be required simultaneously, because they are inconsistent. So a trade of between these two parameters must be made.

In a PLL using a PI regulator the closed loop control loop will be a second order transfer function. According to [21] the Wiener method is the most widely used optimization method, and for a second order loop the transfer function is according to this method given as

$$H_{PLL}(s) = \frac{\sqrt{2}\omega_n s + \omega_n}{s^2 + \sqrt{2}\omega_n s + \omega_n{}^2} \tag{3.25}$$

Where closed loop bandwidth can be found by the use of the stochastic information of the signal and noise, and by the Wiener method it is given as

$$\omega_n^2 = \Delta\omega\lambda\sqrt{\frac{2P_S}{W_0}} \tag{3.26}$$

$\Delta\omega$: Deviation of the frequency
P_S : Input signal power
W_0 : Input noise spectral density
λ : Lagrangian multiplier which determines the relative proportions of the noise and transient error

It is however concluded in [21] that it is very difficult to estimate the stochastic information of the noise, and this relation does not provide the optimum result under the distorted waveform. Therefore *empirical trade-off* will be used instead. As mentioned before both good filtering and fast tracking response is desired, where a low bandwidth gives a good filtering effect whereas a high bandwidth gives faster tracking response, so both cannot be

fully achieved. Errors caused by phase unbalancing and harmonics can be reduced by using a low bandwidth, but by choosing a to low bandwidth the dynamic performance of the PLL can become to low.

If the compromise between filtering and dynamic response when using the PI controller is not acceptable under distorted utility conditions, other methods such as higher order PLL or other techniques should be considered.

3.10 Voltage and current controller optimization

Two controller optimization methods which are thorougly described in [35] will be used for the voltage and current controllers of the inverter. Both these optimization methods are based on modulus hugging, also called frequency response magnitude shaping. The modulus hugging aims on bringing the modulus (absolute value) of the frequency characteristic as close to the value of 1 over as wide a frequency range as possible, from zero and upwards. By using modulus hugging, the result will always be control loops which give stable operation. Therefore no further investigations of the stability of these control loops is necessary.

3.10.1 Modulus optimum

The modulus optimum criteria can be used for processes containing several small time constants, or systems having 1 or 2 large time constants and several small. It can be proved that if the small time constants are small compared to the integrating time constant of the controller, then the higher order products of the small time constants does not contribute to the overall behaviour. Therefore the small time constants are added together and seen as one equivalent time constant T_{eq}.

The type of controller needed to achieve the modulus hugging depends on the which of these three systems which is to be controlled.

1. <u>System with several small first order delays</u>

   An integrating (I) controller as shown in (3.27) is suitable for this system.

$$H_I(s) = \frac{1}{sT_I} \tag{3.27}$$

   This gives an open loop transfer function for the system as shown in eq (3.28) (small t's are used for the small time constants)

$$H_1(s) = \frac{1}{sT_I} K_S \frac{1}{1+st_1} \frac{1}{1+st_2} \frac{1}{1+st_3} \cdots = \frac{1}{sT_I} K_S \frac{1}{1+sT_{eq1}} \tag{3.28}$$

   The closed loop transfer function with this controller is then

$$M_1(s) = \frac{K_S}{K_S + sT_I + s^2 T_I T_{eq1}} \tag{3.29}$$

When optimized using modulus optimum, the controller parameter becomes

$$T_I = 2K_S T_{eq1} \tag{3.30}$$

2. System with one large and several small first order delays

For this system a proportional-integral (PI) controller as shown in (3.31) is suitable. This is because the PI controller contains a phase advance which then can be used to compensate (cancel) the phase delay caused by the large time constant. If the phase delay is not compensated, the large time constant must be added to the small time constants and will make the control response slow. This will be shown by the following equations.

$$H_{PI}(s) = K_P \frac{1 + sT_I}{sT_I} \tag{3.31}$$

With this controller the open loop transfer function for the system becomes as shown in eq (3.32) (small t's are used for the small time constants)

$$H_2(s) = K_P \frac{1 + sT_I}{sT_I} \frac{1}{1 + sT_1} \frac{1}{1 + st_1} \frac{1}{1 + st_2} \cdots \tag{3.32}$$

If the large time constant is compensated by the PI phase advance (pole-zero cancellation) by setting $T_I = T_1$, the transfer function becomes as shown in (3.33).

$$H_2(s) = K_P \frac{1}{sT_I} K_S \frac{1}{1 + sT_{eq2}} \tag{3.33}$$

The closed loop transfer function with this controller is then

$$M_2(s) = \frac{K_P K_S}{K_P K_S + sT_I + s^2 T_I T_{eq2}} \tag{3.34}$$

When optimized using modulus optimum, the controller parameter becomes

$$\begin{aligned} T_I &= T_1 \\ K_P &= \frac{T_1}{2K_S T_{eq2}} \end{aligned} \tag{3.35}$$

3. System with two large and several small time constants

For this system a proportional-integral-derivate (PID) controller as shown in (3.36) is suitable. This is because the PID controller contains two phase advances which can be used to compensate (cancel) the phase delay caused by the large time constants, similar to the system with one large time constant. By compensating the two largest time constant, the speed of the control loop is determined by the sum of the small time constants. It could be possible to compensate more of the time constants in order to make the control response even faster, but that would make the loop very sensible to disturbances and it will be hard to achieve stable control.

$$H_{PID}(s) = K_P \frac{(1+sT_I)(1+sT_D)}{sT_I} \tag{3.36}$$

With this controller the open loop transfer function for the system becomes as shown in eq (3.37) (small t's are used for the small time constants)

$$H_3(s) = K_P \frac{1+sT_I}{sT_I} \frac{1}{1+sT_1} \frac{1}{1+sT_2} \frac{1}{1+st_1} \frac{1}{1+st_2} \cdots \tag{3.37}$$

If the large time constants are compensated by the PID phase advances (pole-zero cancellation) by setting $T_I=T_1$ and $T_D=T_2$, the transfer function becomes as shown in (3.38).

$$H_3(s) = K_P \frac{1}{sT_I} K_S \frac{1}{1+sT_{eq3}} \tag{3.38}$$

The closed loop transfer function with this controller is then

$$M_3(s) = \frac{K_P K_S}{K_P K_S + sT_I + s^2 T_I T_{eq3}} \tag{3.39}$$

When optimized using modulus optimum, the controller parameter becomes

$$\begin{aligned} T_I &= T_1 \\ T_D &= T_2 \\ K_P &= \frac{T_1}{2K_S T_{eq3}} \end{aligned} \tag{3.40}$$

It can be seen from the closed loop transfer functions of these systems, that after compensating for the large time constants, the systems end up as similar second order transfer functions. Therefore it can be said that any system which can be compensated or simplified in such a way that it gives a closed loop transfer function as shown in equation (3.41), can be compensated using modulus optimum.

$$M_{MO}(s) = \frac{\omega_0^2}{s^2 + 2\zeta\omega_0 s + \omega_0^2} \tag{3.41}$$

The generalized design criteria to achieve modulus hugging is

$$\zeta = \frac{1}{\sqrt{2}} \tag{3.42}$$

The frequency response of a modulus optimized control loop is shown in figure 3.12.

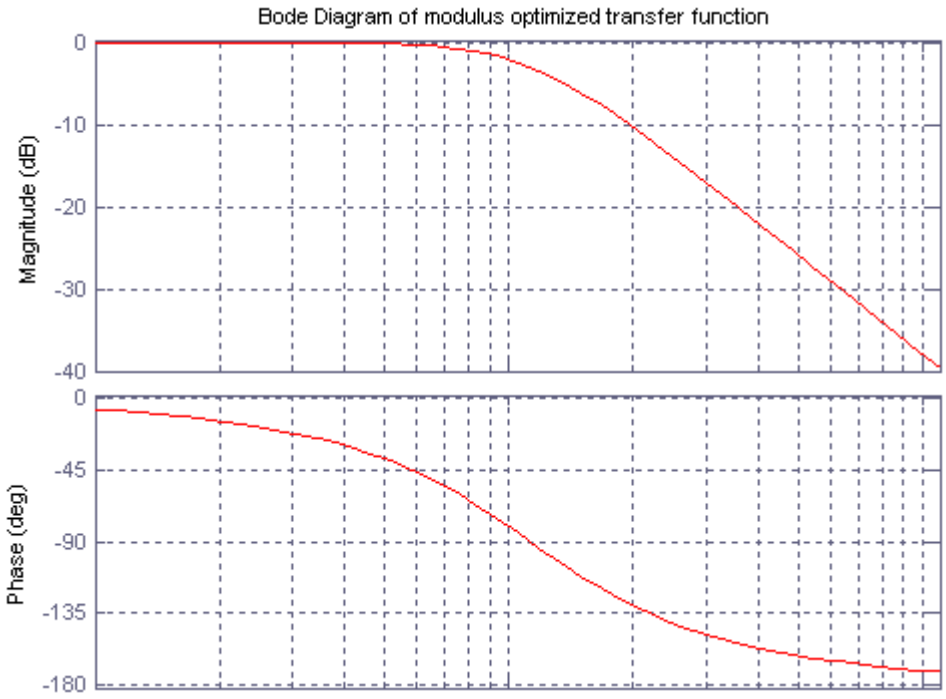

Figure 3.12: Frequency response of a modulus optimized control loop.

The step response of a modulus optimized control loop is shown in figure 3.13. This has a rise time of $4.7T_{eq}$, a maximum overshoot of 4.3% above the final steady state value, and the time used to reach the steady state within E2% (settling time) is $8.4T_{eq}$.

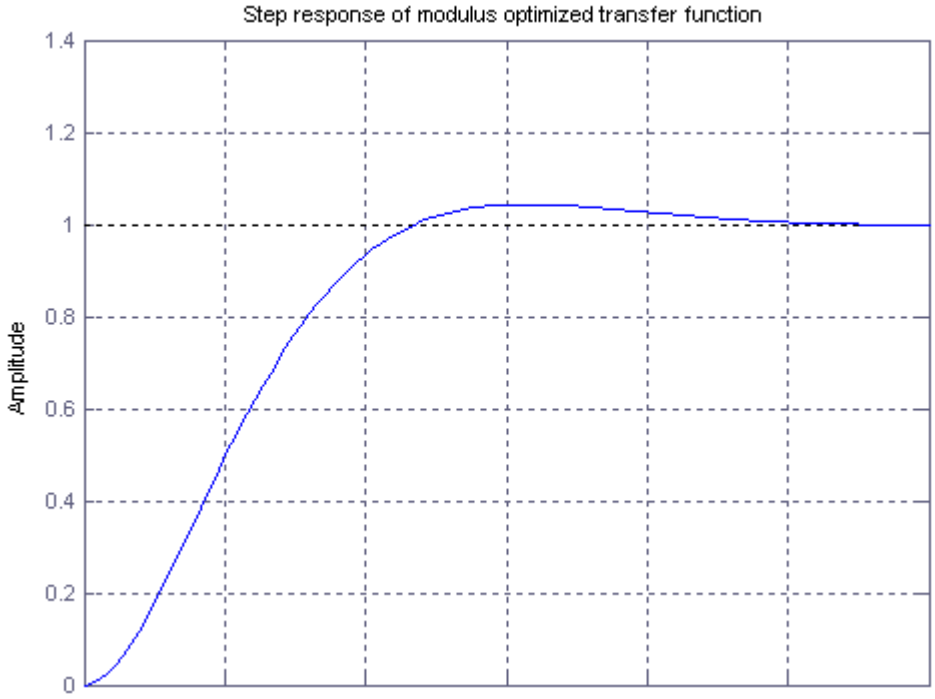

Figure 3.13: Step response of modulus optimized control loop

3.10.2 Symmetrical optimum

If the system to be controlled also involves an integrator, modulus optimum criteria can not be used. This is because compensation is not possible, since the integration of the controller will be added to the integration of the controlled system, which in turn will lead to oscillation of the controlled variable. Therefore another method to achieve modulus hugging has to be used, which is called symmetrical optimum.

As with the modulus optimum, the type of controller needed to achieve symmetrical optimum optimization depends on the system.

4. System with one integrating element and several small first order delays

   This system will need a PI controller (eq (3.31)), because a phase advance is needed in order to overcome the effect of the integrating element. This gives a system with the open loop transfer function in eq(3.43), which can be optimized by symmetrical optimum

$$H_4(s) = K_P \frac{1+sT_I}{sT_I} K_S \frac{1}{sT_S} \frac{1}{1+st_1} \frac{1}{1+st_2} \frac{1}{1+st_3} \cdots = K_P \frac{1+sT_I}{sT_I} K_S \frac{1}{sT_S} \frac{1}{1+sT_{eq4}} \tag{3.43}$$

   Since compensation of this function only leads to oscillation, the closed loop transfer function is found directly.

$$M_4(s) = \frac{K_P K_S (1 + sT_I)}{K_P K_S + sK_P K_S T_I + s^2 T_I T_S + s^3 T_I T_S T_{eq4}} \tag{3.44}$$

When optimized with symmetrical optimum, the controller parameters become

$$\begin{aligned} T_I &= 4T_{eq4} \\ K_P &= \frac{T_S}{2K_S T_{eq4}} \end{aligned} \tag{3.45}$$

5. System with one integrating element, one large and several small first order delays

With this system a PID controller (eq (3.36)) is needed in order to compensate the large delay. The open loop transfer function of this system is

$$H_5(s) = K_P \frac{(1 + sT_I)(1 + sT_D)}{sT_I} K_S \frac{1}{sT_S} \frac{1}{1 + sT_1} \frac{1}{1 + st_2} \frac{1}{1 + st_3} \cdots \tag{3.46}$$

After compensating and adding together the small time constants, the transfer function becomes.

$$H_5(s) = K_P \frac{1 + sT_I}{sT_I} K_S \frac{1}{sT_S} \frac{1}{1 + sT_{eq5}} \tag{3.47}$$

Giving the closed loop transfer function

$$M_5(s) = \frac{K_P K_S (1 + sT_I)}{K_P K_S + sK_P K_S T_I + s^2 T_I T_S + s^3 T_I T_S T_{eq5}} \tag{3.48}$$

This is the same as for the system without one large time delay, so the controller parameters become similar.

$$\begin{aligned} T_I &= 4T_{eq4} \\ T_V &= T_1 \\ K_P &= \frac{T_S}{2K_S T_{eq4}} \end{aligned} \tag{3.49}$$

6. System with only first order delays, where one is at least for times as large as the remainder

   With a system of this type, the large time delay can be approximated as an integrator. The larger the time delay is compared to the remainder, the more correct this assumption becomes. If this system is designed according to the symmetrical optimum criteria, the transient response will be somewhere between that of symmetrical optimum and modulus optimum. If the large time constant is equal four times the remainder, the modulus optimum transient response is achieved, if it becomes larger it will approach symmetrical optimum.

It can be seen from the closed loop transfer functions of these systems, that after compensating for the large time constant, the systems end up as similar third order transfer functions. As with the modulus optimum, it can be said that any system which can be compensated or simplified in such a way that it gives a closed loop transfer function as shown in eq (3.50), can be compensated using symmetrical optimum.

$$M_{SO}(s) = \frac{b_0 + sb_1}{a_0 + sa_1 + s^2a_2 + s^3a_3} \tag{3.50}$$

Here $a_0=b_0$ and $a_1=b_1$, and if this equation is analysed in order to achieve modulus optimum, then these design criteria can be found.

$$\begin{aligned} a_1^2 &= 2a_0a_2 \\ a_2^2 &= 2a_1a_3 \end{aligned} \tag{3.51}$$

The frequency response of a symmetrical optimized control loop is shown in figure 3.14.

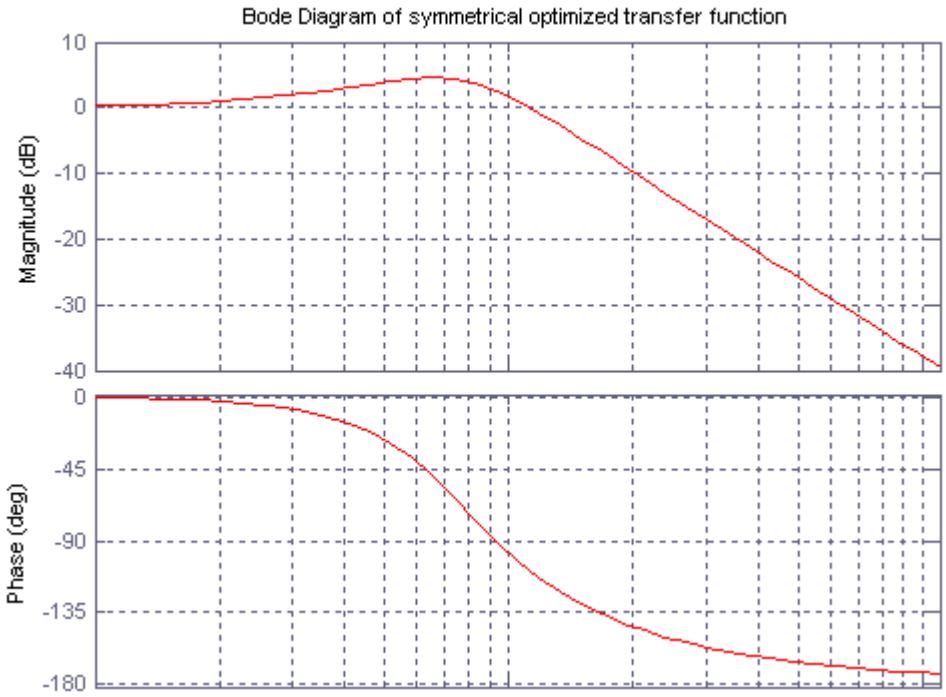

Figure 3.14: Frequency response of asymmetrical optimized control loop

The step response of a symmetrical optimized control loop is shown in figure 3.15. This has a rise time of $3.1T_{eq}$, a maximum overshoot of 43.4% above the final steady state value, and the time used to reach the steady state within E2% (settling time) is $16.5T_{eq}$.

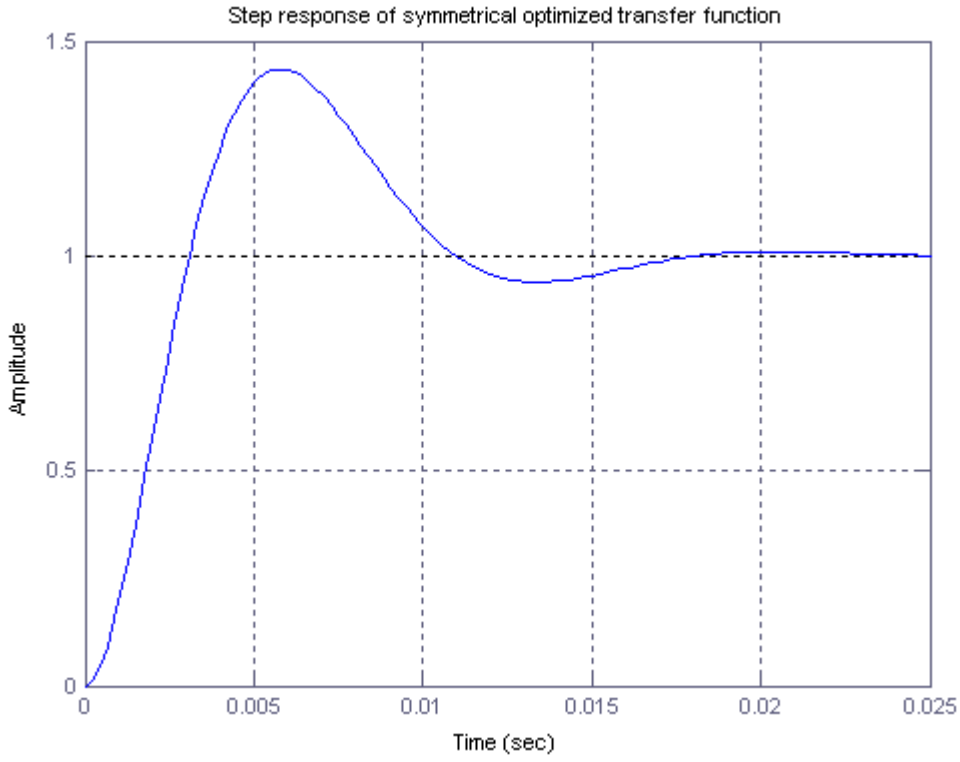

Figure 3.15: Step response of symmetrical optimized control loop

4 SYSTEM DESCRIPTION, MODELLING AND OPTIMIZATION

In this thesis a system is designed in order to demonstrate some of the theory described. The system setup is based on the topologies and control methods shown in the first chapters. Since most of these methods are well known and are not so complex, it has made it easier to design and construct a complete system. If it shows out at a later time that more advanced control is needed, these can easily be implemented at a later time when the system is up and running.

The system has been made first of all to test the different control methods, and therefore it has not been designed to be a high efficiency system. However the control system has been optimized with the methods described in chapter 3.10.

4.1 Converter topology and control description

In the setup for this assignment a *multi-string inverter* with a DC-DC converter and a DC-AC converter will be used. For the DC-DC converter the *current fed full bridge converter* with a *HF transformer* will be used, and for the DC-AC converter an ordinary *3-phase full bridge VSI* with an *LCL filter* as the grid interface will be used. The basic topology is shown in figure 4.1.

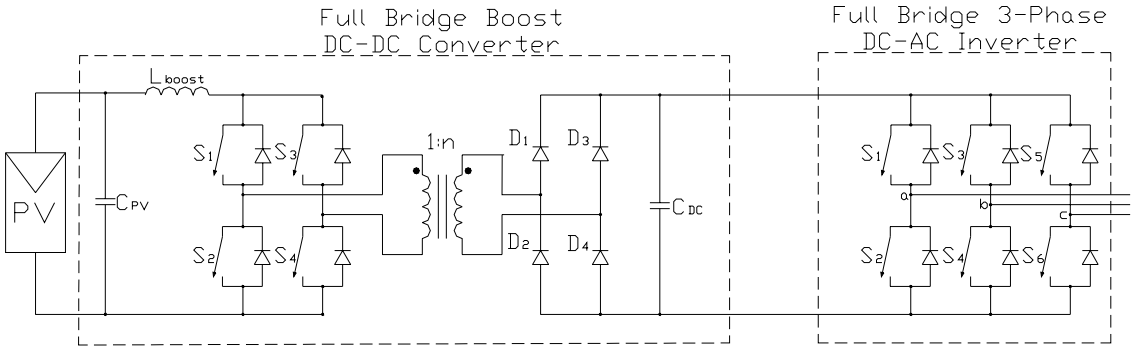

Figure 4.1: The basic converter topology

The control of the DC-DC converter will be a *P&O MPPT* which utilizes the direct duty cycle control, and the DC-AC converter will be *current controlled* by PI regulators in a *synchronous reference frame*. By locking the reference frame to the grid voltage, the d-axis current will represent the active power, and the q-axis current the reactive power. In order to synchronize with the grid a *PLL with a PI regulator* will be used, and in order to detect *anti islanding*, passive methods complying with the requirements stated in chapter 2.1.1 will be implemented. Pulse width modulation of the switch signals will be made based on *SVPWM*, but other methods can also be implemented in order to test the difference.

In this setup no harmonic compensation will be implemented, and there will not be any temporary storage since the system will always be connected to the grid.

4.1.1 DC-DC converter values

Because the DC-DC converter topology was not available as a laboratory converter, a new one had to be constructed. Since this converter type is not so common, models for the converter is not easily available in the literature, so therefore a steady state model and a dynamic model based on small ripple AC modelling is derived in appendix 1. Based on the steady state model, the converter is rated in appendix 3, and the rated values found are presented in the table below.

Table 4.1 - DC-DC Converter component values

Component	Value
Input capacitor	330µF
Boost inductor	1.0mH
DC-link capacitor	165µF

The operating conditions of the DC-DC converter is shown in figure 4.2.

Table 4.2 - DC-DC operating conditions

Name	Value
Switching frequency	50kHz
DC-link voltage	600V
Input voltage	170-350 V
Input current[a]	0.5-5 A
Transformer ratio	1.4
Duty cycle limits[a]	0.12-0.58

a. Lower limit is based on keeping the converter operating in continuous mode

The switching devices will be mosfets in the inverter side and fast diodes on the rectifier side of the converter.

4.1.2 DC-AC converter and LCL filter values

An IGBT converter which is designed for laboratory use at NTNU SEfAS will be used as the DC-AC converter. But LCL filter which is used as a grid interface has to be buildt especially for this setup. The rating of this filter can be found in appendix 3. The component values of the filter and the DC-AC converter are presented in the table below, and the converter operating conditions is shown in table 4.4.

Table 4.3 - DC-AC Converter and LCL filter component values

Component	Value
DC-link capacitor	3300µF
Inverter side inductance L_i	4.3mH
Filter capacitance C_f	0.68µF
Grid side inductance L_g	2.0mH
Damping resistor R_d	10Ω

.

Table 4.4 - DC-AC converter and LCL filter operating conditions

Name	Value
Switching frequency	20kHz
DC-link voltage	600V
Output voltage	0-400V RMS
Current limit pr leg	25A (at 20kHz)
Pulse width modulation	0-100%
Resonance frequency f_{res}	5224Hz

4.1.3 Laboratory setup

A schematic of the laboratory setup is shown in figure 4.2, and a equipment specification is listed in table 4.5.

Table 4.5 - Equipment in laboratory setup

Type	Brand	Model	#
Current transducer	LEM	LAH 25-NP	1
Current transducer	LEM	LA 205-S	3
Voltage transducer	LEM	LV 25-600	5
Controller card	NTNU/SEfAS	TMS 320 F2812	2
Measuring board	NTNU/SEfAS	v1.0	1
Variable DC power supply	Sorensen	DLM 300-10E	1
DC power supply	Traco Power	TXL 060-0533T	2

The controller cards used are based on the Texas Instruments TMS320F2812, which is a 16/ 32bits, 150MHz DSP micro controller. The card utilizes a Xilink XC95288XL CPLD as gate expansion. The DC-link has also been equipped with a charging circuit in order to avoid large inrush currents when connecting the grid. The current and voltage measurements are made with LEM current and voltage transducers, and when the DSP card is extended with the external measurement card it can handle eight LEM modules. The DSP has a buildt in 12bit analog to digital converter which can maximum handle 16 channels per conversion.

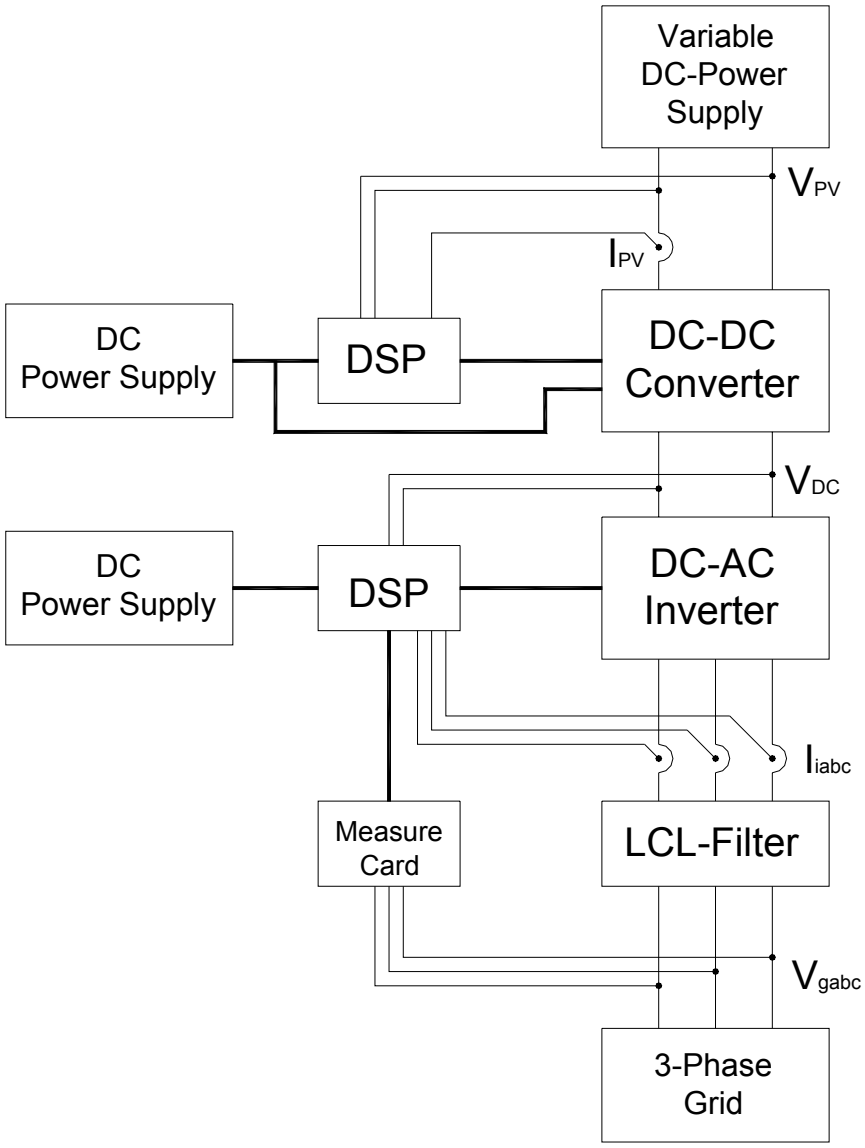

Figure 4.2: Schematic of laboratory setup

4.2 P&O Maximum Power Point Tracker optimization

Minimum time step

In the appendix 1 a small signal AC model was developed for the DC-DC converter. This model gives a third order system, and can be difficult to analyse analytical. In order to simplify this model it is assumed that the DC-link is stiff, therefore the AC variations in the DC-link is zero. With this simplification the transfer function becomes as shown in (4.1).

$$H_{vpvd} = \frac{\hat{v}_{pv}(s)}{\hat{d}(s)} = -\frac{\frac{1}{C_{pv}L_b}\left(I_L R_{on} + \frac{V_{DC}}{n}\right)}{s^2 + s\left(\frac{R_{on}}{L_b} + \frac{R_{on}D_m}{L_b}\right) + \frac{1}{C_{pv}L_b}} \tag{4.1}$$

This is a typical 2nd order transfer function, and can be analysed using well known methods. Equation (4.1) can be written as

$$H_{vpvd} = \frac{\hat{v}_{pv}(s)}{\hat{d}(s)} = \frac{\mu\omega_0^2}{s^2 + 2\omega_0\zeta s + \omega_0^2} \tag{4.2}$$

Where

$$\mu = -\left(I_L R_{on} + \frac{V_{DC}}{n}\right)$$

$$\omega_0 = \sqrt{\frac{1}{C_{pv}L_b}}$$

$$\zeta = \frac{\sqrt{C_{pv}}R_{on}(1+D_m)}{\sqrt{L_b}}$$

The step response of the PV voltage then becomes

$$\hat{v}_{pv}(s) = \frac{\mu\omega_0^2}{s^2 + 2\omega_0\zeta s + \omega_0^2}\frac{\hat{d}(s)}{s} \tag{4.3}$$

Transformed into the time domain the step response becomes

$$\hat{v}_{pv}(t) = \mu\Delta d\left(1 - \frac{1}{\sqrt{1-\zeta^2}}e^{-\zeta\omega_0 t}\cos\left(\sqrt{1-\zeta^2}\,\omega_0 t - \arcsin(\zeta)\right)\right) \tag{4.4}$$

The sampling interval can now be found by defining a region around the steady state value of $\hat{p}(t)$ which must be reached before a new sampling is allowed. The steady state value and the region is defined in (4.5) and (4.6) respectively.

$$\hat{p}(t) \underset{t\to\infty}{=} -\frac{\mu^2 \Delta d^2}{R_{MPP}} \tag{4.5}$$

$$\left[-\frac{(1+\varepsilon)\mu^2 \Delta d^2}{R_{MPP}}, -\frac{(1-\varepsilon)\mu^2 \Delta d^2}{R_{MPP}} \right] \tag{4.6}$$

Where ε gives the allowed deviation from the steady state value, and in this case a deviation of 10% giving ε = 0.1 is assumed to be adequate. Based on (4.4) to (4.6) it is shown in [23] that the time T_ε before $\hat{p}$ is confined within the region in (4.6) can be approximated as

$$T_\varepsilon \cong -\frac{1}{\zeta\omega_0}\ln(\varepsilon) \tag{4.7}$$

Based on the chosen component values T_ε becomes 9.3ms. To be on the safe side the sampling time is then chosen to be T_{S_MPPT} = 10ms.

Minimum duty cycle step

The minimum duty cycle step has been calculated based on eq (3.24). The calculated value became close to 16μs, which would make the MPPT algorithm very slow. There is also a possibility that this equation is not evaluated correctly since there are so many factors involved. In order to have a faster process a step size of $\Delta d = 0.001$ will be used.

4.3 Phase Locked Loop PI Regulator

4.3.1 Model

A model of the three-phase PLL is shown in the figure below

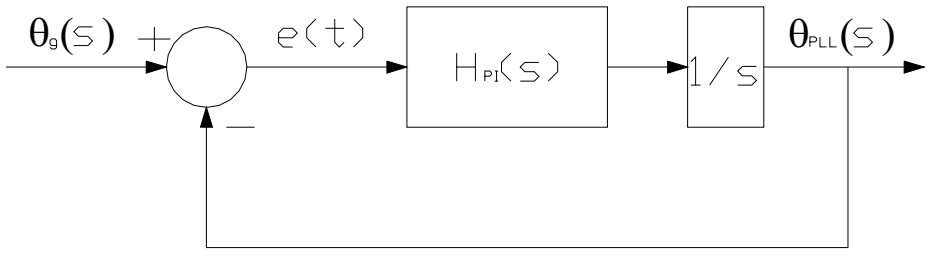

Figure 4.3: PLL model

The PI regulator is the same as in eq (3.10), and then the closed loop transfer function with the grid angle as input and the PLL angle as output becomes as shown in (4.8), and the phase error is found in (4.9).

$$M_c(s) = \frac{\theta_{PLL}}{\theta_g} = \frac{K_p s + \frac{K_p}{T_i}}{s^2 + K_p s + \frac{K_p}{T_i}} = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{4.8}$$

$$M_\varepsilon(s) = \frac{\varepsilon}{\theta_g} = \frac{s^2}{s^2 + K_p s + \frac{K_p}{T_i}} = \frac{s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{4.9}$$

$$\omega_n = \sqrt{\frac{K_p}{T_i}}$$
$$\zeta = \frac{K_p}{2\omega_n} = \frac{\sqrt{K_p T_i}}{2}$$

4.3.2 Optimization

Based on the optimization criteria found in chapter 3.9, the second order loop parameters must satisfy

$$\omega_0 \geq 2\pi f_g \text{ (lower gives good filtering, higher gives good tracking response)}$$
$$\zeta = \frac{1}{\sqrt{2}} \tag{4.10}$$

In order to achieve both good filtering and a fast tracking response, the undamped resonance frequency is sat to 628 rad/s (twice the grid frequency), giving these regulator parameters.

$$K_P = 890$$
$$T_i = 0.0023$$

The parameters are calculated according to a continuous system, and this can be done if the sampling time of the discrete system is less then the fastest time constant of the physical process. In this case the process is a pure integrator, and the time constant of the regulator is much larger than the sampling time constant (T_s=50µs).

By using the bilinear transform, which involves substituting eq (3.14) into (4.8) and (4.9) and rearranging, gives the system in discrete form as shown in (4.11) and (4.12).

$$M_c(z) = \frac{\left(-4T_S\zeta\omega_0 + T_S^2\omega_0^2\right)z^{-2} + \left(2T_S^2\omega_0^2\right)z^{-1} + \left(4T_S\zeta\omega_0 + T_S^2\omega_0^2\right)}{\left(4 - 4T_S\zeta\omega_0 + T_S^2\omega_0^2\right)z^{-2} + \left(-8 + 2T_S^2\omega_0^2\right)z^{-1} + \left(4 + 4T_S\zeta\omega_0 + T_S^2\omega_0^2\right)} \tag{4.11}$$

$$M_e(z) = \frac{4z^{-2} - 8z^{-1} + 4}{\left(4 - 4T_S\zeta\omega_0 + T_S^2\omega_0^2\right)z^{-2} + \left(-8 + 2T_S^2\omega_0^2\right)z^{-1} + \left(4 + 4T_S\zeta\omega_0 + T_S^2\omega_0^2\right)} \tag{4.12}$$

In figure 4.4 the frequency response of the PLL transfer functions is plotted, and in figure 4.5 the bode diagram of the disturbance rejection is shown. In figures 4.6 and 4.7 the step response and a pole-zero plot of the function is shown. It can be seen that the discrete system shows similar response as the continuous system at frequencies lower than approximately 5kHz.

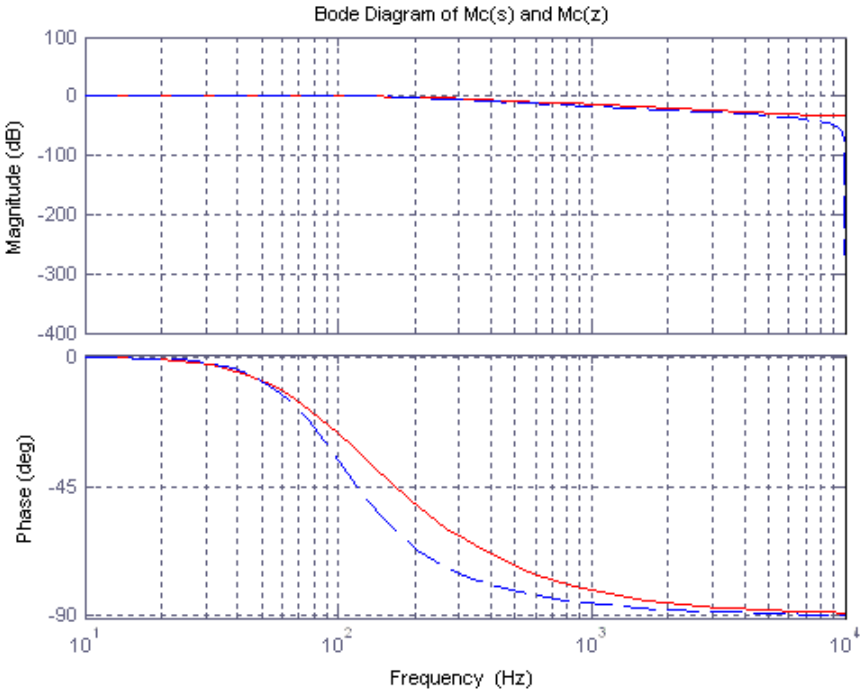

Figure 4.4: Bode plot of transfer function between input and output
Blue dotted: Discretized system
Red continuous: Continuous system

From figure 4.5 it can be seen that disturbances with frequency above twice the grid frequency (100Hz) is filtered.

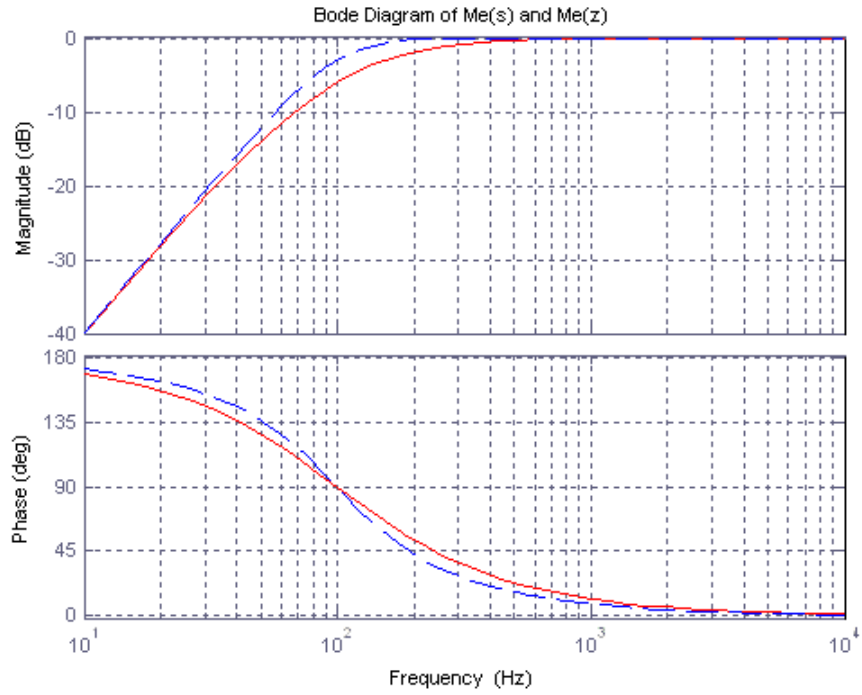

Figure 4.5: Bode plot of transfer function between input and error
Blue dotted: Discretized system
Red continuous: Continuous system

From the step response the time used to reach the steady state within E2% (settling time) is found to be approximately 10ms.

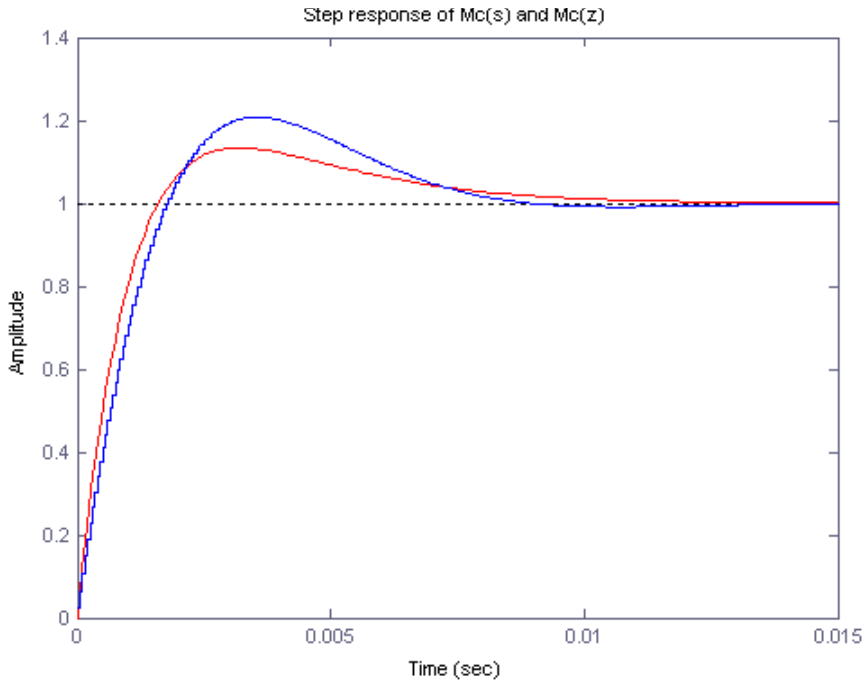

Figure 4.6: Step response of the continuous and the discrete transfer function, $M_C(s)$ and $M_C(z)$
Blue: Discretized system
Red: Continuous system

All poles and zeroes are inside the unit circle, and therefore the PLL control loop will show stable performance.

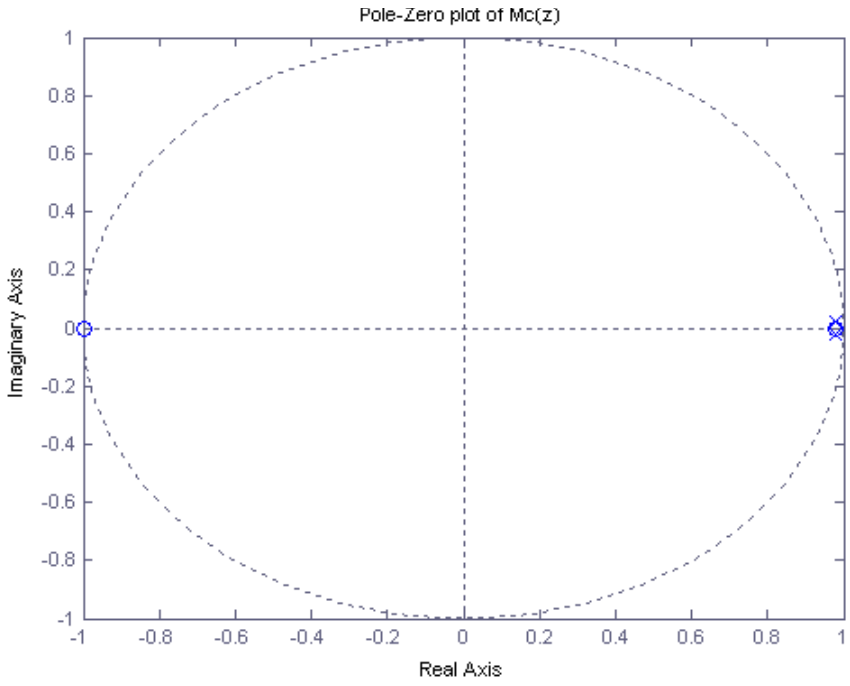

Figure 4.7: Pole-zero plot of the discrete transfer function $M_C(z)$

4.4 Current Regulator

The current regulator is found in the inner control loop of the DC-link voltage regulator. These are actually two regulators, one for the d- and one for the q-axis. Both of these regulators are working on the same system model, and it is adequate to estimate the parameters of one of them.

4.4.1 Model

The current control loop for the d-axis can be modelled as shown in figure 4.8 (similar for q-axis).

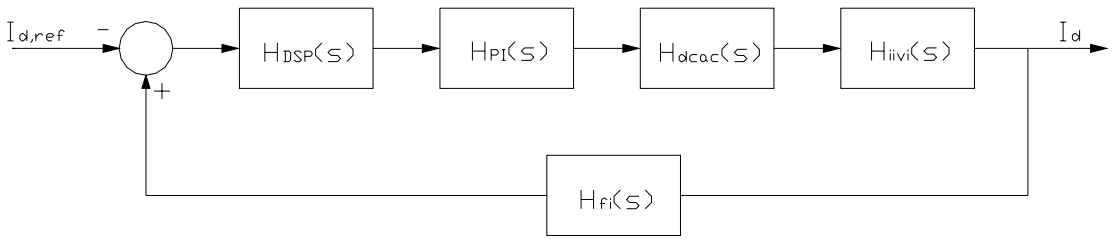

Figure 4.8: D-axis current control loop (similar for q-axis).

In this model all non-linearities and noise in the output voltage is ignored for simplicity. The blocks in the figure are described as follows.

H_{DSP} - Represents the time delay caused by the DSP, as it needs some time to do calculations and because of the way signals are sampled. The time delay caused DSP will be a minimum of half the switching period, that is 25µs.

$$H_{DSP}(s) = \frac{1}{1 + T_{DSP}s} \tag{4.13}$$

H_{dcac} - Represents the time delay caused by the inverter, because the desired output voltage from the inverter will be the time average over one switching period. It will take approximately half the switching period from a new voltage reference is applied until it is averaged over the load, thus the time delay becomes 25µs.

$$\mathrm{H}_{\mathrm{dcac}}(s) = \frac{1}{1 + T_{dcac}s} \tag{4.14}$$

H_{fi} - In order to reduce unwanted noise in the measurement a first order digital filter with a corner frequency of 3 kHz will be used, which gives a delay of 333µs

$$\mathrm{H}_{\mathrm{fi}}(s) = \frac{1}{1 + T_{fi}s} \tag{4.15}$$

H_{PI} - Represents the PI regulator (eq(3.19))

H_{iivi} - Represents a transfer function of the LCL filter, and will describe how the inverter output current reacts to a change in output voltage from the inverter.

A model of the filter is shown in figure 2.10, and based upon this a mathematical model of the filter in the dq reference frame has been derived. This result is shown in eq (4.16), and the derivation can be found in appendix 2.

$$\begin{bmatrix} \frac{di_{id}(t)}{dt} \\ \frac{di_{iq}(t)}{dt} \\ \frac{di_{gd}(t)}{dt} \\ \frac{di_{gq}(t)}{dt} \\ \frac{dv_{cd}(t)}{dt} \\ \frac{dv_{cq}(t)}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{R_i + R_d}{L_i} & \omega & \frac{R_d}{L_i} & 0 & -\frac{1}{L_i} & 0 \\ -\omega & -\frac{R_i + R_d}{L_i} & 0 & \frac{R_d}{L_i} & 0 & -\frac{1}{L_i} \\ \frac{R_d}{L_g} & 0 & -\frac{R_g + R_d}{L_g} & \omega & \frac{1}{L_g} & 0 \\ 0 & \frac{R_d}{L_g} & -\omega & -\frac{R_g + R_d}{L_g} & 0 & \frac{1}{L_g} \\ \frac{1}{C_f} & 0 & -\frac{1}{C_f} & 0 & 0 & \omega \\ 0 & \frac{1}{C_f} & 0 & -\frac{1}{C_f} & -\omega & 0 \end{bmatrix} \begin{bmatrix} i_{id}(t) \\ i_{iq}(t) \\ i_{gd}(t) \\ i_{gq}(t) \\ v_{cd}(t) \\ v_{cq}(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L_i} & 0 & 0 & 0 \\ 0 & \frac{1}{L_i} & 0 & 0 \\ 0 & 0 & -\frac{1}{L_g} & 0 \\ 0 & 0 & 0 & -\frac{1}{L_g} \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} v_{id}(t) \\ v_{iq}(t) \\ v_{gd}(t) \\ v_{gq}(t) \end{bmatrix} \tag{4.16}$$

From this model it can be seen that the d- and q- axis of the currents are dependent, so a decoupling should be used in order to simplify the model. In order to simplify the model further the capacitor voltage can also be fed forward. Since the capacitor voltage is not measured it can not be fed forward directly. There are two alternative ways of doing this, one is to feed forward the grid voltage and assume that the difference between this and the capacitor voltage is handled by the integrator in the controller. The other solution is to estimate the capacitor voltage, based on the grid voltage and the inverter current. Assuming one of these two feed forward methods will be used, the model of the LCL filter can be simplified.

Based on the mathematical model in (4.16), the converter output current can be expressed as in eq (4.17) and (4.18), where the feed forward terms are marked with colours. The blue colour indicates the cross coupling between the d- and q-axis, and the red colour indicates the filter capacitor voltage. The capacitor voltage also includes the damping resistor, in order to make the error less by using the grid voltage as feed forward instead.

$$L_i \frac{di_{id}(t)}{dt} = R_d\left(i_{gd}(t) - i_{id}(t)\right) - v_{cd}(t) + v_{id}(t) - R_i i_{id}(t) + \omega L_i i_{iq}(t) \tag{4.17}$$

$$L_i \frac{di_{iq}(t)}{dt} = R_d\left(i_{gq}(t) - i_{iq}(t)\right) - v_{cq}(t) + v_{iq}(t) - R_i i_{iq}(t) - \omega L_i i_{id}(t) \tag{4.18}$$

Collecting the feed forward terms into a single term gives the equations (4.19) and (4.20).

$$v_{idII} = R_d\left(i_{gd}(t) - i_{id}(t)\right) - v_{cd}(t) + \omega L_i i_{iq}(t) \tag{4.19}$$

$$v_{iqII} = R_d\left(i_{gq}(t) - i_{iq}(t)\right) - v_{cq}(t) - \omega L_i i_{id}(t) \tag{4.20}$$

By applying the feed forward terms, the model gets simplified to the to equations (4.21) and (4.22).

$$L_i \frac{di_{id}(t)}{dt} = v_{id}(t) - R_i i_{id}(t) \tag{4.21}$$

$$L_i \frac{di_{iq}(t)}{dt} = v_{iq}(t) - R_i i_{id}(t) \tag{4.22}$$

These to equations are similar, and will have the same transfer function. The transfer function of the LCL filter with the decoupling becomes

$$H_{iivi}(s) = \frac{i_{id}(s)}{v_{id}(s)} = \frac{i_{iq}(s)}{v_{iq}(s)} = \frac{1}{sL_i + R_i} = \frac{1/R_i}{1 + T_{iivi}s} \tag{4.23}$$

Using measured values for the inductances (se chapter 4.1.2), the time constant becomes.

$$T_{iivi} = \frac{L_i}{R_i} = \frac{4.45mH}{1.8\Omega} = 2.47ms$$

4.4.2 Optimization

The T_{iivi} time constant is much larger then the rest of the time constant, so this can be seen as a system of one large and several small time constants. Therefore modulus optimum with a PI controller can be used as an optimization criteria, as is described in chapter 3.10.1. The model in figure 4.8 is therefore reduced by adding together the small time delays, giving the model in figure 4.9.

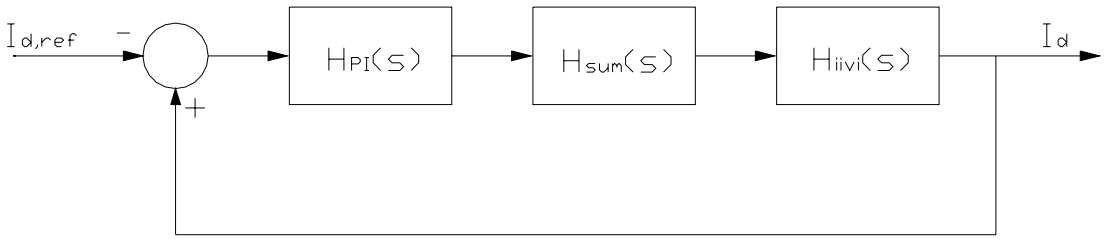

Figure 4.9: Reduced current control model

Where the sum of the time delays is defined in eq (4.24)

$$H_{eqi}(s) = \frac{1}{1+(T_{DSP}+T_{dcac}+T_{fi})s} = \frac{1}{1+T_{eqi}s} \tag{4.24}$$

Giving the equivalent time delay.

$$T_{eqi} = T_{DSP} + T_{dcac} + T_{fi} = 25\mu s + 25\mu s + 333\mu s = 383\mu s$$

The sum of these time constants is approximately four times larger then the sampling time constant T_s, and therefore only a small error will occur if the parameters are designed after the continuous system. The open loop transfer function of this system then becomes

$$H_{id}(s) = K_P \frac{1+T_i s}{T_i s} \cdot \frac{1}{1+T_{eqi}s} \cdot \frac{1/R_i}{1+T_{iivi}s} \tag{4.25}$$

In order to compensate the pole from the large time delay, the phase advance from the PI regulator is used. This leads to an integral time which is equal the large time constant, giving the closed loop transfer function

$$M_{id}(s)=\frac{H_{id}}{1+H_{id}}=\frac{K_P\dfrac{1/R_i}{T_i s\left(1+T_{eqi}s\right)}}{1+K_P\dfrac{1/R_i}{T_i s\left(1+T_{eqi}s\right)}}=\frac{K_P/R_i}{T_i s\left(1+T_{eqi}s\right)+K_P/R_i}=\frac{K_P}{T_i T_{eqi}R_i}\frac{1}{s^2+\dfrac{1}{T_{eqi}}s+\dfrac{K_P}{T_i T_{eqi}R_i}} \tag{4.26}$$

Which can be recognized as a second order function on the form of (3.41), giving

$$\omega_0=\sqrt{\frac{K_P}{T_i T_{eqi}R_i}} \tag{4.27}$$

$$\zeta=\frac{1}{2}\sqrt{\frac{T_i R_i}{K_P T_{eqi}}} \tag{4.28}$$

By using the modulus optimum criteria the damping factor ζ is sat equal to $\sqrt{1/2}$, giving the closed loop transfer function the value 1 between zero frequency and as high a frequency as possible. The controller parameters now become.

$$T_i=T_{iivi}=2.47ms$$
$$K_P=\frac{T_i R_i}{2T_{eqi}}=5.8$$

The system is discretized by applying the bilinear transform to eq (3.41), giving the discrete transfer function in (4.29).

$$M(z)=KT_S^2\omega_0^2\frac{z^{-2}+2z^{-1}+1}{\left(4-4T_S\zeta\omega_0+T_S^2\omega_0^2\right)z^{-2}+\left(-8+2T_S^2\omega_0^2\right)z^{-1}+\left(4+4T_S\zeta\omega_0+T_S^2\omega_0^2\right)} \tag{4.29}$$

In figure 4.10 the bode diagram of the continuous system and the discretized system is plotted. From the diagram it can be seen that the discrete system behaves as a continuous system up to approximately 5kHz, this proves that the approximation of the system as continuous was correct. It can also be seen from the magnitude plot that the magnitude has the value 1 up to a high frequency, as it should using the modulus optimum criteria.

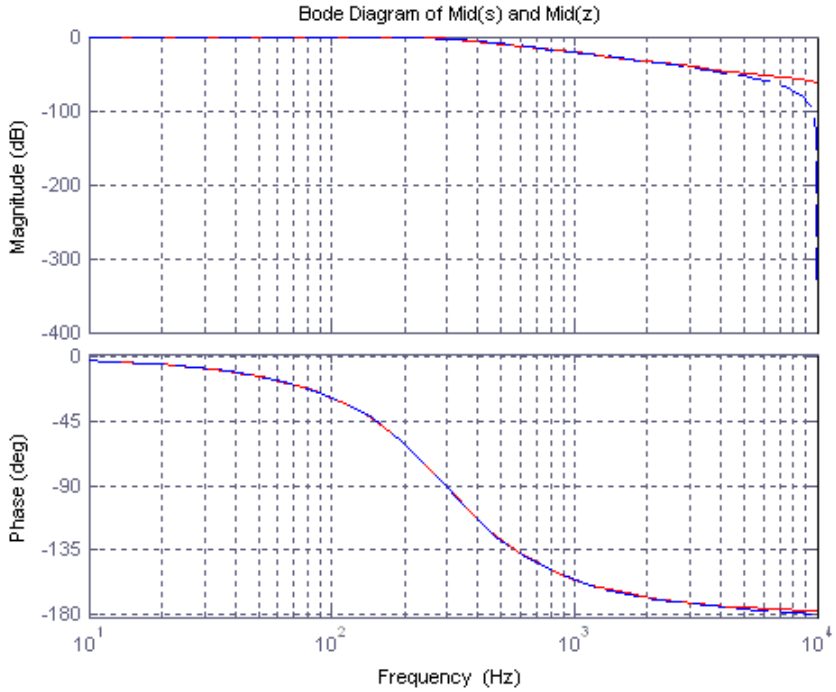

Figure 4.10: Bode diagram of continuous and discretized closed loop models of the inner control loop
Blue dotted: Discretized system
Red continuous: Continuous system

In figure 4.11 the step response of the system in discrete and continuous form is shown. It can here be seen that the response of the discrete system follows the continuous system.

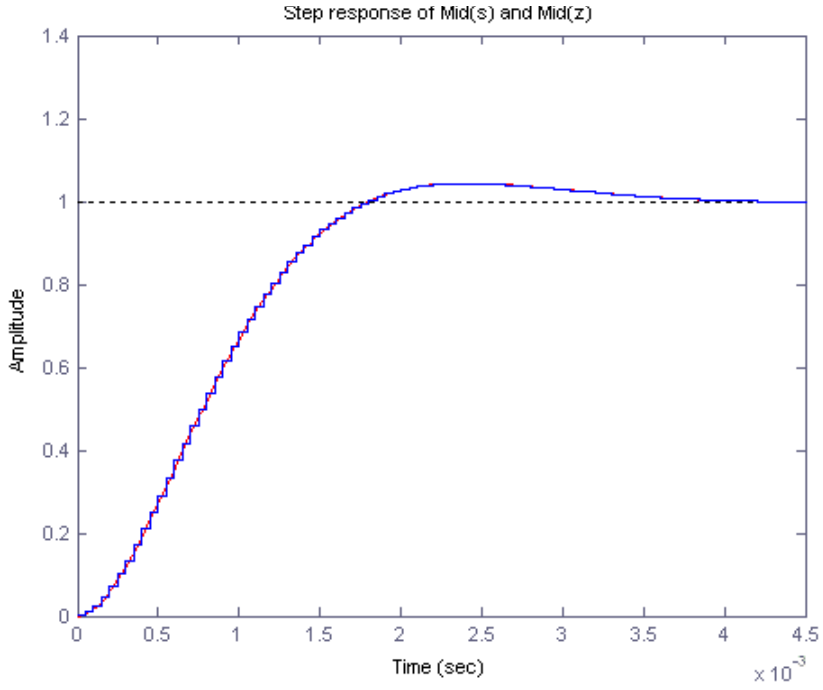

Figure 4.11: Step response of the discrete and the continuous time model of the inner control loop

In figure 4.12 a pole zero-plot of the discretized system is plotted. This shows that the poles of the closed loop lies inside the unit circle, and therefore the system is stable as predicted when using modulus hugging optimization.

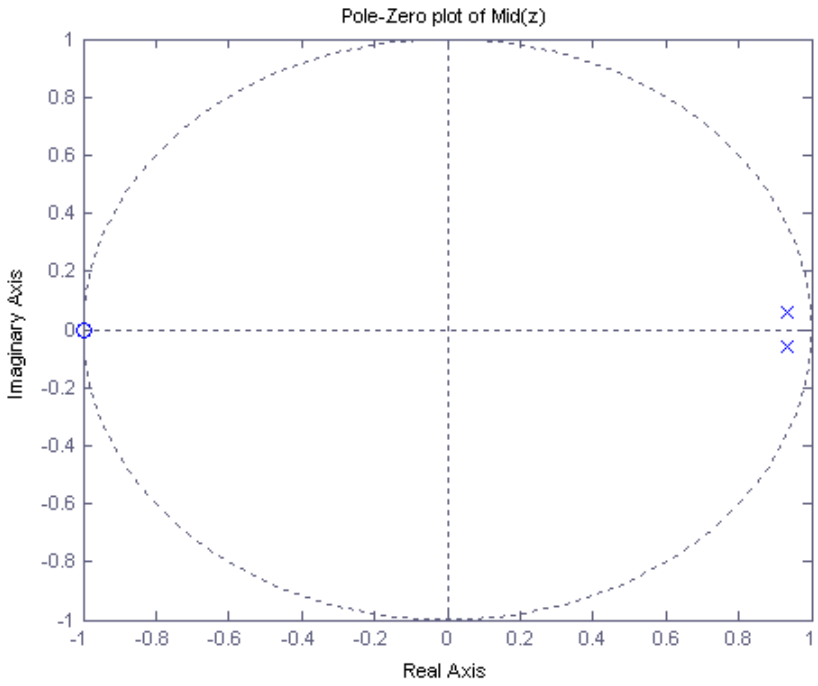

Figure 4.12: Pole-zero plot of the discretized closed loop system

4.5 Voltage controller

The voltage controller is found in the outer control loop of the DC-link voltage control. The output from this regulator is the reference to the d-axis current controller in the inner control loop.

4.5.1 Model

The DC-voltage controller is found in the outer control loop, and is shown in the figure below

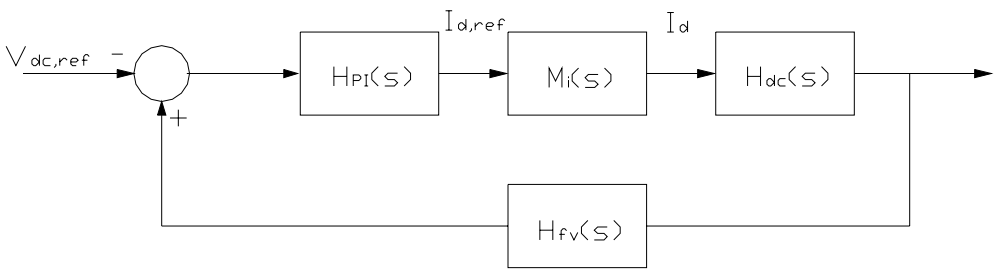

Figure 4.13: DC-link voltage control loop

H_{fi} - In order to reduce unwanted noise in the measurement a first order digital filter with a corner frequency of 3 kHz will be used, which gives a delay of 333µs.

$$H_{fv}(s) = \frac{1}{1 + T_{fv}s} \tag{4.30}$$

H_{PI} - Represents the PI regulator (eq (3.19))

M_{id} - Represents the d-axis current controller, and in order to use the symmetrical optimum criteria, the system should be approximated as a first order system. This can be justified knowing that the outer control loop must be slower than the inner control loop. Based on eq (3.41), the inner control loop transfer function can be rewritten as follows.

$$M_{id}(s) = K\frac{1}{\frac{1}{\omega_0^2}s^2 + \frac{2\zeta}{\omega_0}s + 1} \tag{4.31}$$

At frequencies below ω_0

$$\frac{1}{\omega_0^2}s^2 \ll 1$$

And the system can be approximated as the first order function in eq (4.32).

$$M_{id}(s) = \frac{1}{\frac{2\zeta}{\omega_0}s + 1} = \frac{1}{4\zeta^2 T_{sum}s + 1} = \frac{1}{4\left(\frac{1}{\sqrt{2}}\right)^2 T_{sum}s + 1} = \frac{1}{1 + 2T_{sum}s} \tag{4.32}$$

The difference between the approximation and the 2.order system is shown in figure 4.14, and it can here be seen that the approximation is correct at low frequencies.

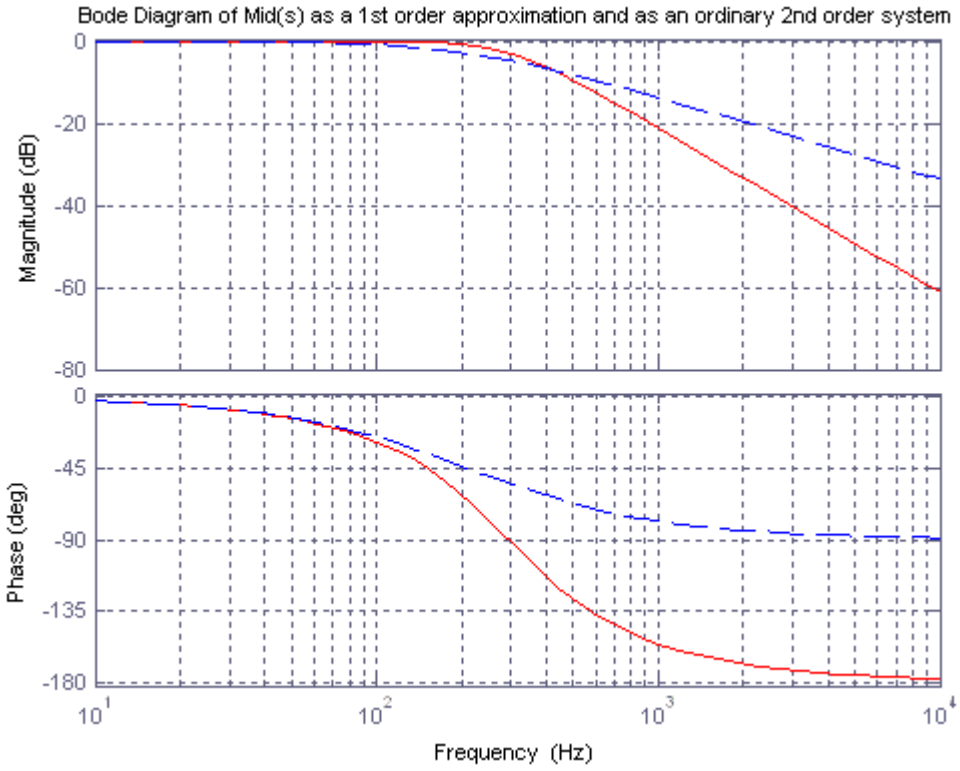

Figure 4.14: Bode diagram of the 1.order approximation compared to the 2.order original system
Red: 2.order original system
Blue: 1.order approximation

H_{DC} - Represents the transfer function between the d-axis current and the DC-link voltage. The DC-link voltage will vary with the DC-link current according to the following transfer function

$$H_{DC}(s) = K_{DC}\frac{1}{C_{DC}s} \tag{4.33}$$

The constant K_{DC} is a constant relating the d-axis current to the dc-current. The currents can be related knowing the power balance in eq (4.34), and the relation between the dc-link voltage and the d-axis voltage. The latter relation is derived in (4.35)

$$V_{DC}I_{DC} = \frac{3}{2}V_d I_d \tag{4.34}$$

$$\begin{aligned} V_{ab} &= \frac{\sqrt{3}}{2\sqrt{2}}V_{DC}m_a \\ V_d = \hat{V}_\alpha &= \hat{V}_a = \frac{\sqrt{2}}{\sqrt{3}}V_{ab} = \frac{1}{2}V_{DC}m_a \end{aligned} \tag{4.35}$$

By combining (4.34) and (4.35), the relation between the currents is found in (4.36).

$$K_{DC} = \frac{I_{DC}}{I_d} = \frac{3}{2}\frac{V_d}{V_{DC}} = \frac{3}{2}\frac{1}{2}\frac{V_{DC}}{V_{DC}} m_a = \frac{3}{4} m_a \tag{4.36}$$

$0 \le m_a \le 1$ with sinusoidal CB-PWM

$0 \le m_a \le 2/\sqrt{3}$ with SVM or CB-PWM with third harmonic injection

Assuming SVPWM is to be used, and in order to generate a voltage close to the grid voltage a modulation ratio close to maximum will be used most of the time. Therefore the constant relating the DC-link current and the d-axis current becomes.

$$K_{DC} = \frac{3}{4} m_{a,\max} = \frac{3}{4}\frac{2}{\sqrt{3}} = \frac{\sqrt{3}}{2} \approx 0.87$$

4.5.2 Optimization

The voltage control system contains two phase delays where both are of the same order, and can be summed together as one time constant. The system then satisfies the symmetrical optimum criteria where there is one integrator, several time constants and a PI regulator. The open loop transfer function of the voltage control system can now be written as

$$H_{DC}(s) = K_P K_{DC} \frac{1+T_i s}{C_{DC} T_i s^2} \frac{1}{1+(2T_{eqi}+T_{fv})s} = K_P K_{DC} \frac{1+T_i s}{C_{DC} T_i s^2} \frac{1}{1+T_{eqv} s} \tag{4.37}$$

$$T_{eqv} = 2T_{eqi} + T_{fv}$$

Giving the closed loop transfer function in (4.38). If compared to eq (3.50) it can be seen that it satisfies the symmetrical optimum criteria.

$$M_{DC}(s) = \frac{H_{DC}(s)}{1+H_{DC}(s)} = K_P K_{DC} \frac{T_i s + 1}{C_{DC} T_i T_{eqv} s^3 + C_{DC} T_i s^2 + K_P K_{DC} T_i s + K_P K_{DC}} \tag{4.38}$$

According to the symmetrical optimum criterion the parameters can now be found

$$T_i = 4T_{eqv} = 4.4ms$$
$$K_P = \frac{1}{2}\frac{C_{DC}}{K_{DC} T_{eqv}} = 1.72$$

By inserting the controller parameters into eq (4.38), an equation called the standard equation for the symmetrical optimum is obtained

$$M_{DC}(s) = \frac{1 + 4T_{eq}s}{8T_{eq}{}^3 s^3 + 8T_{eq}{}^2 s^2 + 4T_{eq}s + 1} \tag{4.39}$$

In figure 4.15 a bode diagram of the model is shown, where the continuous model is compared to a discretized model. The system is discretized using the c2d function in Matlab with the sampling time T_S.

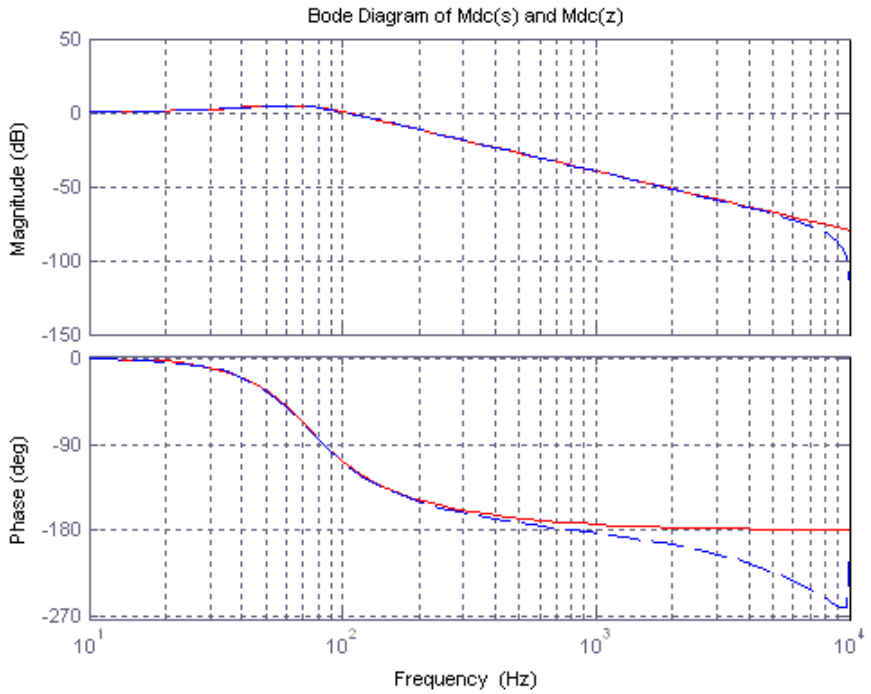

Figure 4.15: Bode plot of the continuous and discrete voltage control loop
Red continuous: Continuous system
Blue dotted: Discrete system

The step response of the optimized loop is similar to the one shown in figure 3.15, and it can be seen that the step response is equal for the discretized and the continuous system.

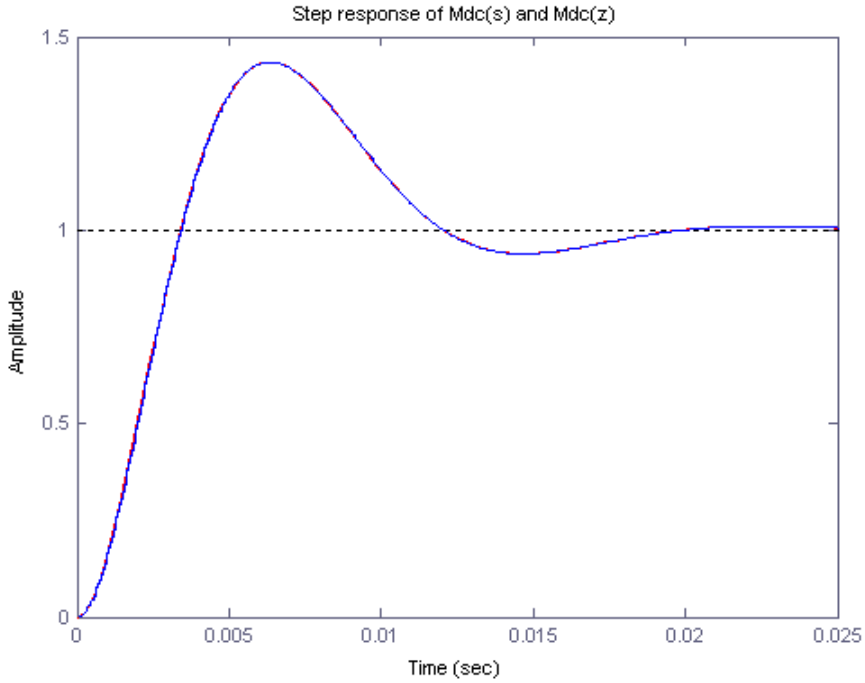

Figure 4.16: Continuous and discrete step response of the voltage control loop

As expected also all the poles are inside the unit circle as it should when using a modulus hugging technique.

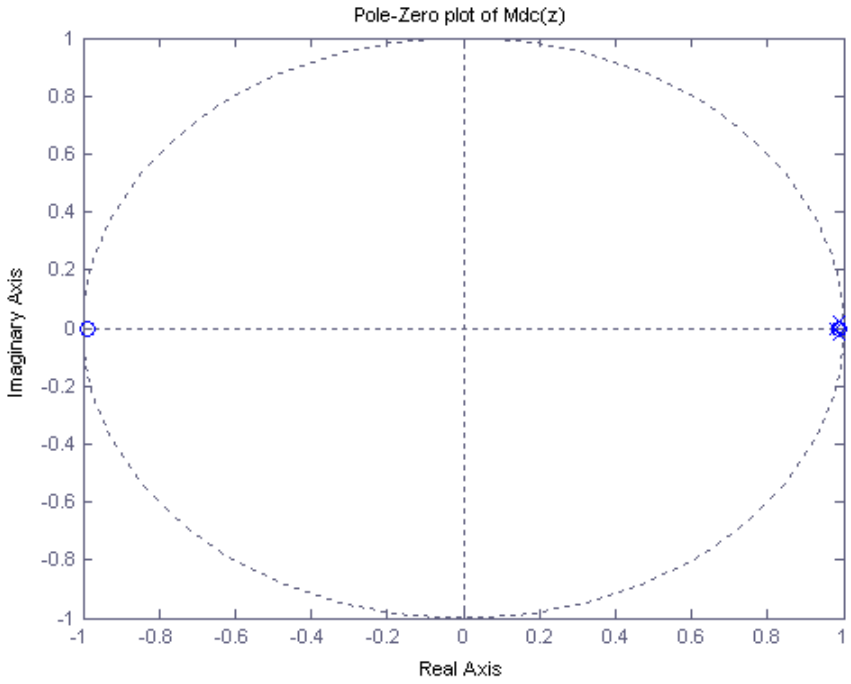

Figure 4.17: Pole-Zero plot of the discrete voltage controller

4.6 Complete control system model

With the controller optimization and model simplifications made in the previous chapters, an overview of the complete control system can be made. This is shown in the figure below

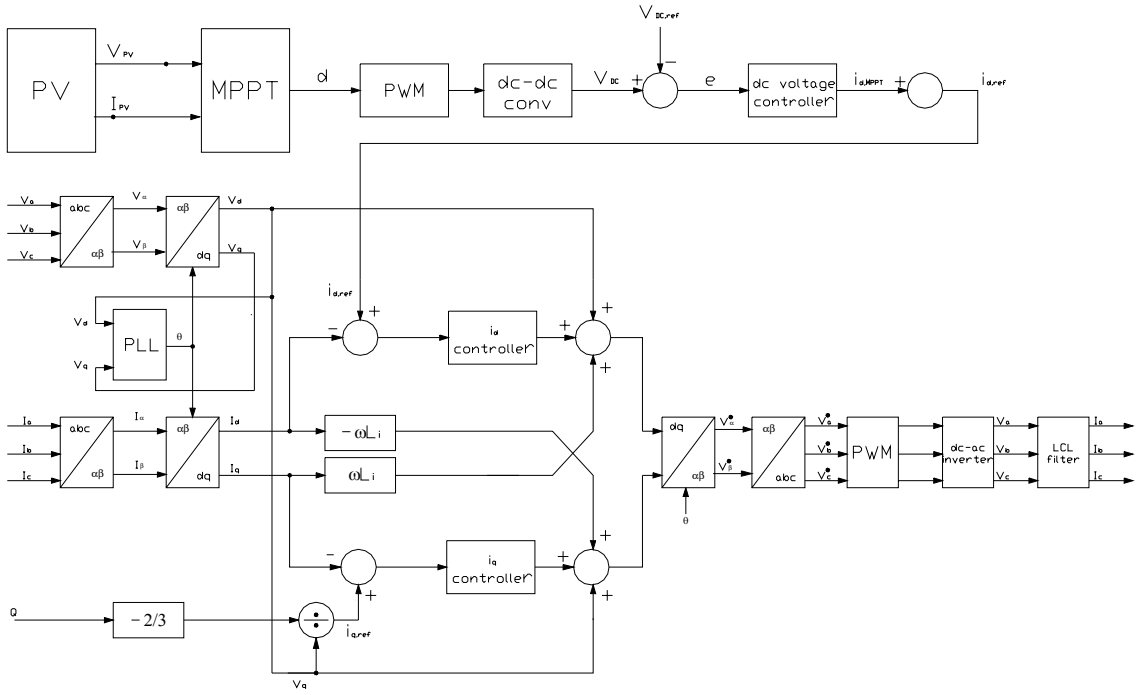

Figure 4.18: Overview of the control system of the DC-DC converter and the DC-AC converter

5 SIMULATION

The simulation of the converters are made in Simulink, which is a simulation program based on the Matlab platform. In the simulation the converters are simulated separately since the DC-DC converter and the DC-AC converter are supposed to work as separate units connected to the same DC-link. A brief description of the simulations can be found in appendix 5.

5.1 DC-DC Converter

In the simulation of the DC-DC converter the MPPT is simulated with a simplified model of the converter, based upon the small signal AC model derived in appendix 1. As the PV panel input the I-V characteristic of a PV panel is incorporated as a look up table. The look up table is loaded from a GUI (Graphical User Interface), in which the user can change the solar panel operating conditions. The look up table values are calculated based on the equations found in chapter 2.2.1

5.1.1 I-V Characteristic

The I-V characteristic of the simulated PV panels under STC is shown in the GUI in figure 5.1.

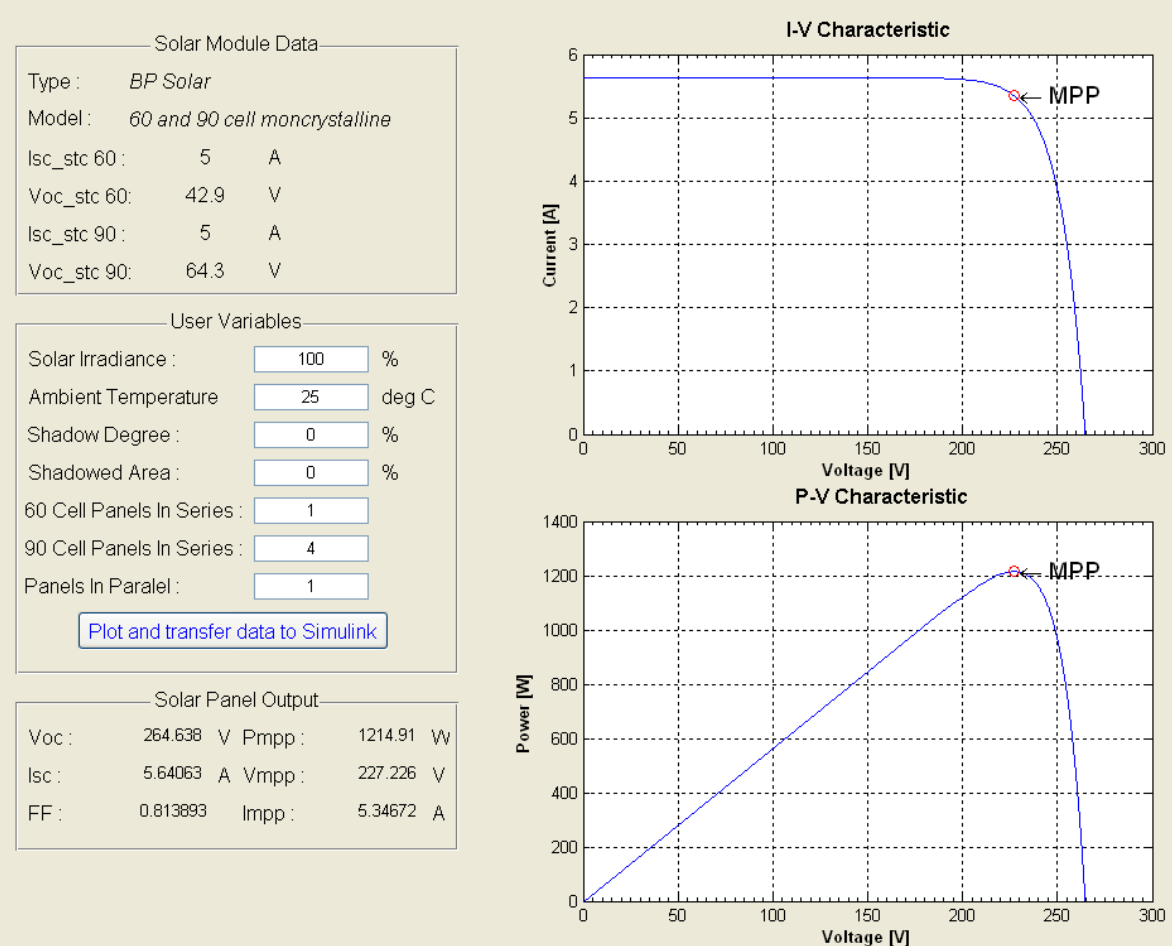

Figure 5.1: GUI of the PV-panel I-V characteristic under STC

The I-V characteristic is based on values from actual solar panels, but it was found that the calculated values are closer to an ideal I-V characteristic than the panels actually are. This is due to the fact that the models found in chapter 2.2.1 does not consider e.g the resistances and other nonidealities in the PV cells. This however will not be of any significance since the model will only be used to simulate the MPPT, and not simulate real cells. This model can easily be made more accurate if needed later, by adding more accurate models of the PV cells.

In the next figure the characteristic of the PV panels is shown under a partial shadow condition. The shadow is across 40% of the cells with 50% shadowing, and all the cells are in series. From the P-V characteristic two maximum power points can be found, and these will confuse the MPPT. The simple algorithm used in the P&O algorithm will not be able to see the difference between these points, and it will find one of these points depending on where the tracker was before the shadowing. In order to test how much this will influence the efficiency of the MPPT, the tracker should be tested over some time with varying degrees of shadowing. No simulations with varying conditions have been made here.

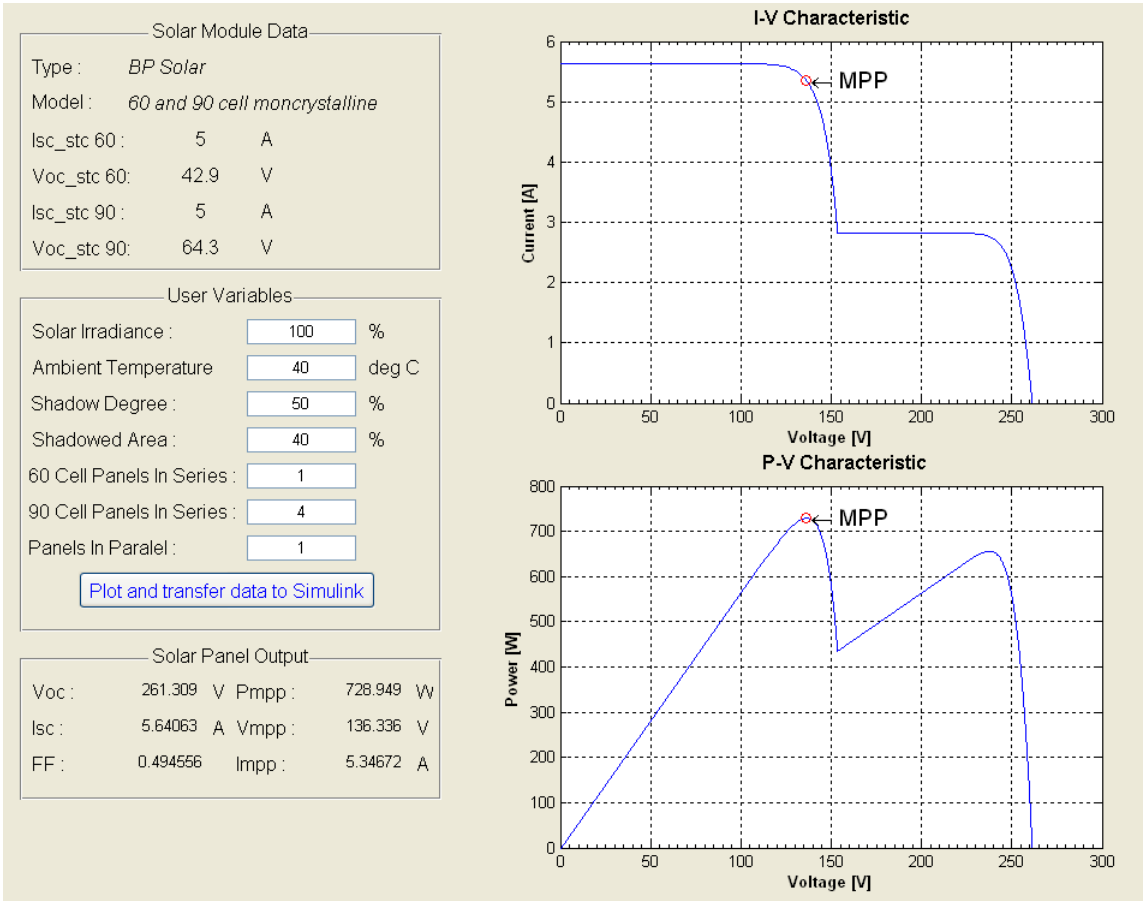

Figure 5.2: GUI of the PV-panel I-V characteristic under partial shadowing

5.1.2 Maximum Power Point Tracker

The simulation of the MPPT was made with the I-V characteristic at STC shown in figure 5.1. No tests where made with shadowing since it is obvious that it will not work as explained in the previous section. In figure 5.3 the duty-cycle steps from the MPPT is shown when a step in the irradiance from 0 to 100% is given. It can here be seen that with the chosen values of sampling time and step size the MPPT reaches steady state in approximately 0.8s.

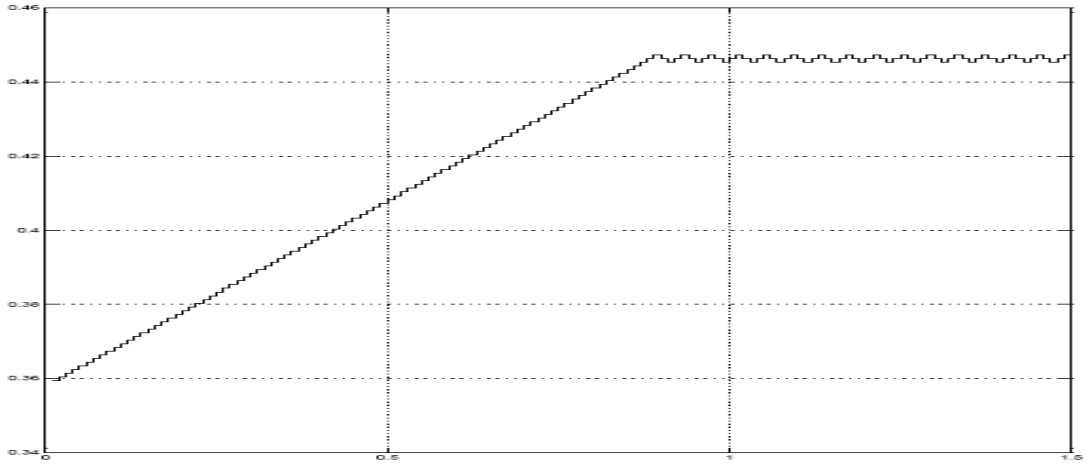

Figure 5.3: Duty-cycle steps due to the MPPT

The current, voltage and power values of the PV panel when the MPPT has reached steady state is shown in figure 5.5. It can here be seen that after each perturbation, there is some transient behaviour in the values as expected, and from figure XX it can be seen that within the next perturbation this is approximately within 10% of the initial value. In the simulations a steady state efficiency of the MPPT of 99.9% was found.

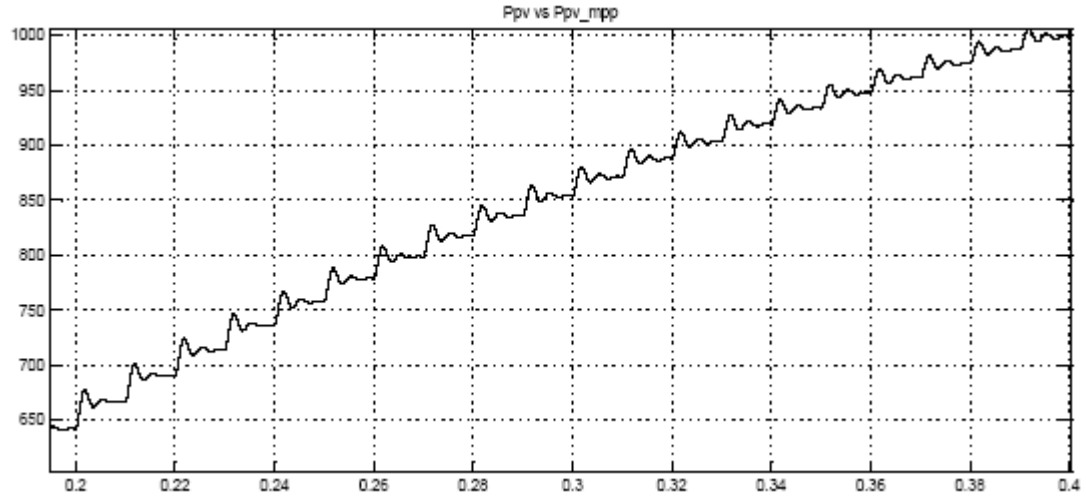

Figure 5.4: Ripple in PV power after a perturbation in the duty cycle

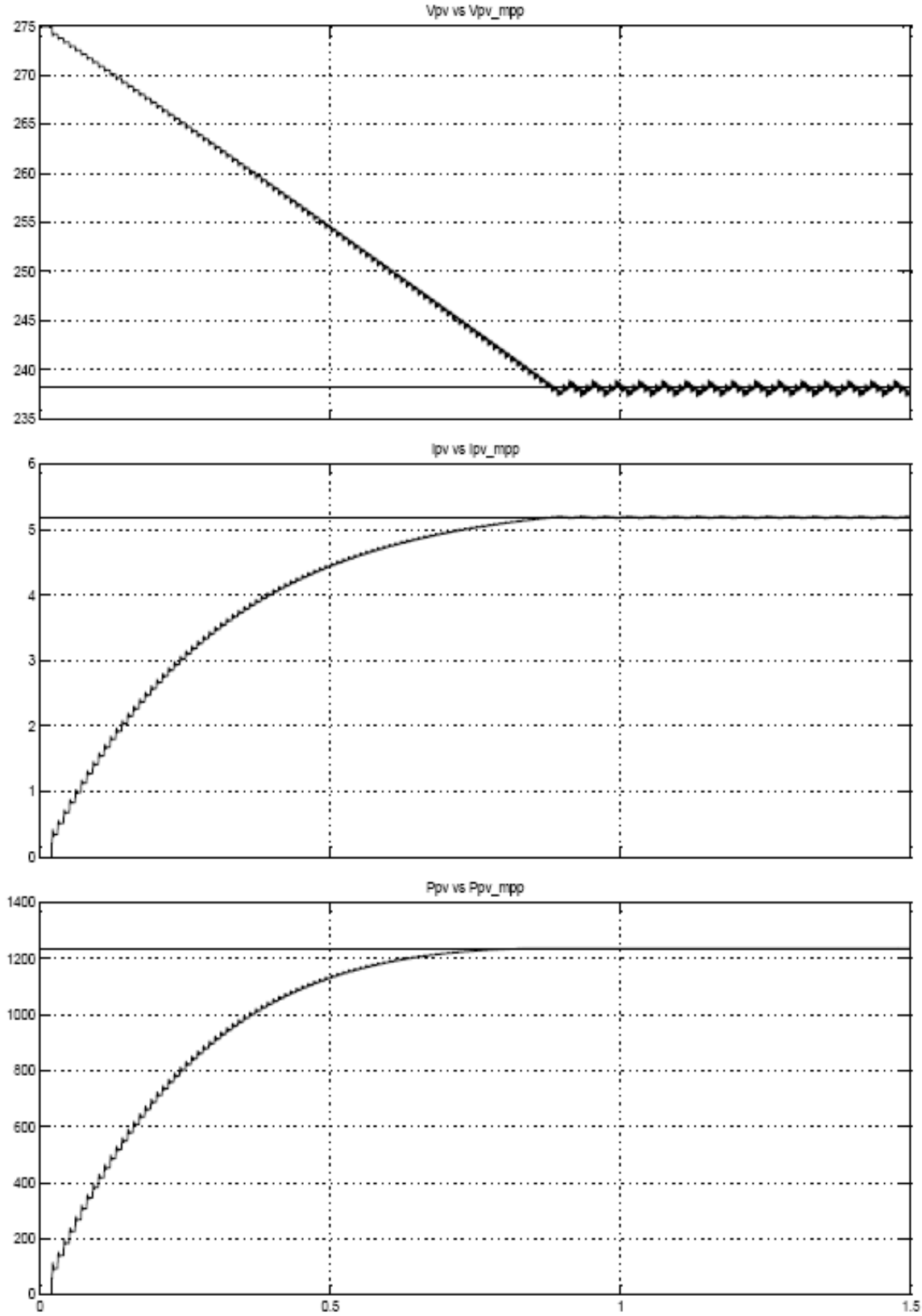

Figure 5.5: PV voltage, current and power during MPP

5.2 DC-AC Converter simulation results

A description of the simulation model can be found in appendix 5. Most of the simulations has been made on a simplified model of the plant with a pure sinusoidal output from the inverter, since the dynamics of the control system will be the same. But in the harmonic analysis full PWM was used in order to test the filtering effect of the LCL filter.

In order to reduce the complexity of the model, carrier based modulation is used instead of space vector modulation. This modulation technique is simpler to implement in Simulink, and by using third harmonic injection with a ZSS signal of 1/4 the amplitude of the fundamental, an equal result to that of SVPWM can be achieved.

5.2.1 PLL

In figure 5.6 the results from the simulation of the PLL is plotted. This shows that the time used to reach the steady state within 2% (settling time) is approximately 10ms, when a phase jump of $30°$ is applied.

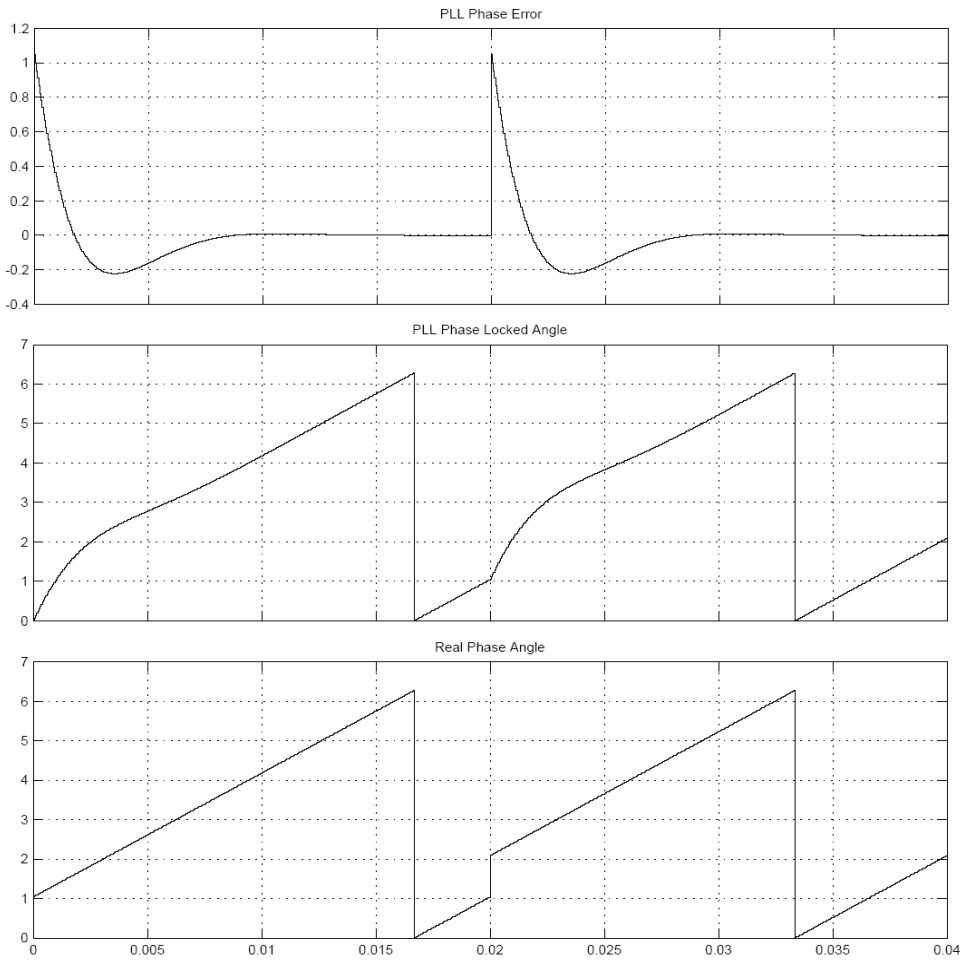

Figure 5.6: Simulation of PLL with a start-up angle of $30°$ and a phase jump of $30°$ at 20ms.

5.2.2 Current control

The current control system is simulated with a fixed DC-link voltage, where the DC-link voltage controller is disconnected. Instead a step of 1A in the d-axis current reference is applied, and the d- and q- axis current response is found. When using the parameters found in chapter 4.4, the step response of the d- and q- axis current becomes as shown in figure 5.7. The step response has a rise time of $8.3T_{eqi}$,an overshoot of ca 1.5% and a settling time equal the rise time

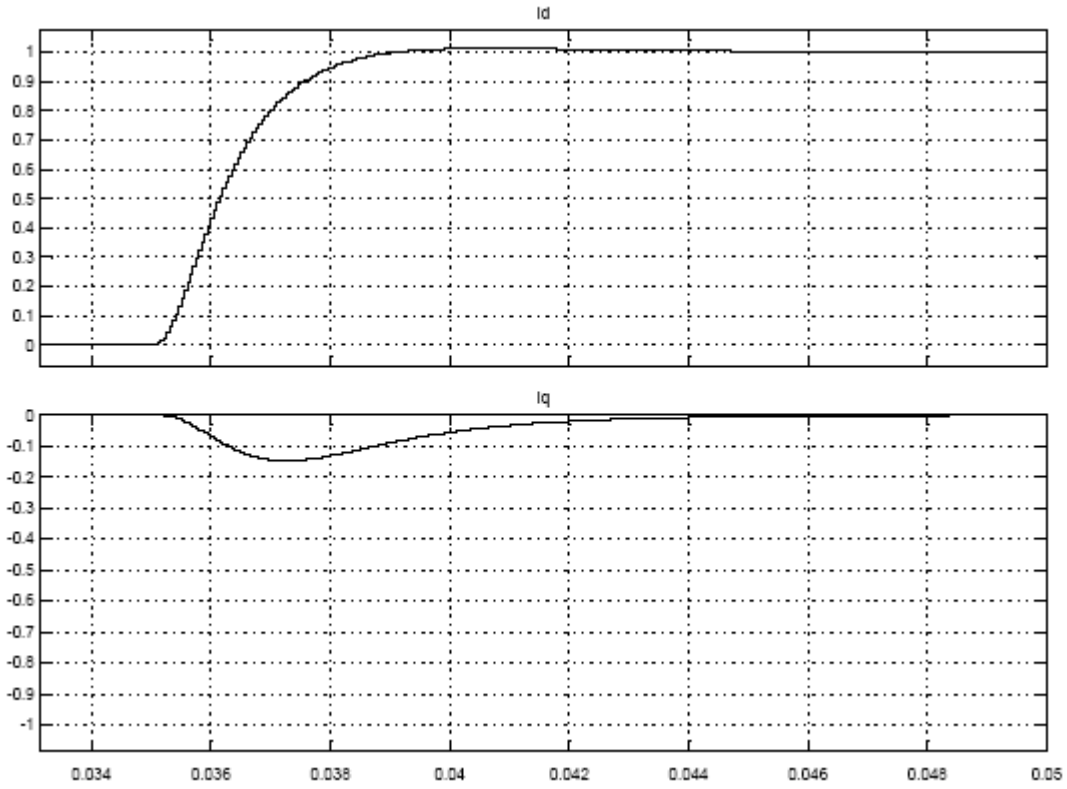

Figure 5.7: Step response of d- and q- axis current with parameters found by modulus optimization

The q-current also reacts to a step in the d-axis current. This shows that the circuit is not completely decoupled as it should be. With the modulus optimized controller parameters the loop become slower than what was predicted, and this had consequences for the cascaded voltage control loop. By adjusting the parameters gain to $1.6K_p$, the control loop acted approximately as it should according to the modulus optimization.

5.2.3 Voltage control

To test the voltage controller a step is applied in the DC-link voltage reference. In figure 5.8 the step response of the DC-link is shown, this is the response to a step of 1V applied at 55ms. The DC-link voltage response has a rise time of $2.7T_{eqv,}$, an overshoot of 34%, and the

time used to reach the steady state within E2% of the step size is $13T_{eqv}$. It was also noted that by running steps larger then approximately 1V, the voltage controller went into saturation.

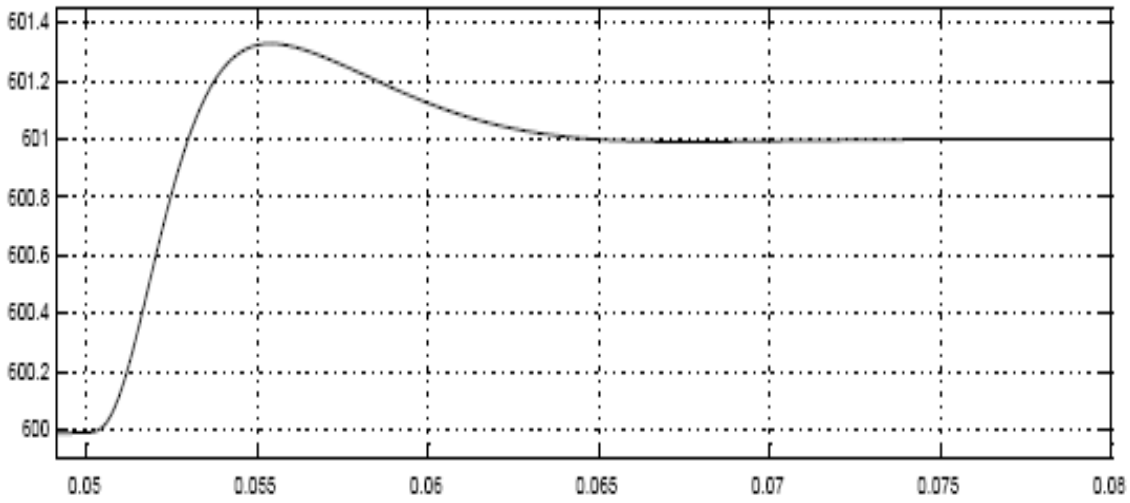

Figure 5.8: DC-link voltage step response after a -2V step at 55ms

5.2.4 The LCL filter

In figure 5.9 the currents and voltages across the different elements of the LCL filter is plotted at start-up. At 0ms the grid is connected to the LCL filter, and at approximately 8ms the inverter is given a current step of 1.85A in the d-axis current regulator. As expected most of the voltage and current ripple can be seen in the inverter side inductor, the grid side inductor has therefore only a small amount of the total ripple, as it was designed for. The voltage across the capacitor is a smoothed sinusoidal voltage with low ripple in the voltage.

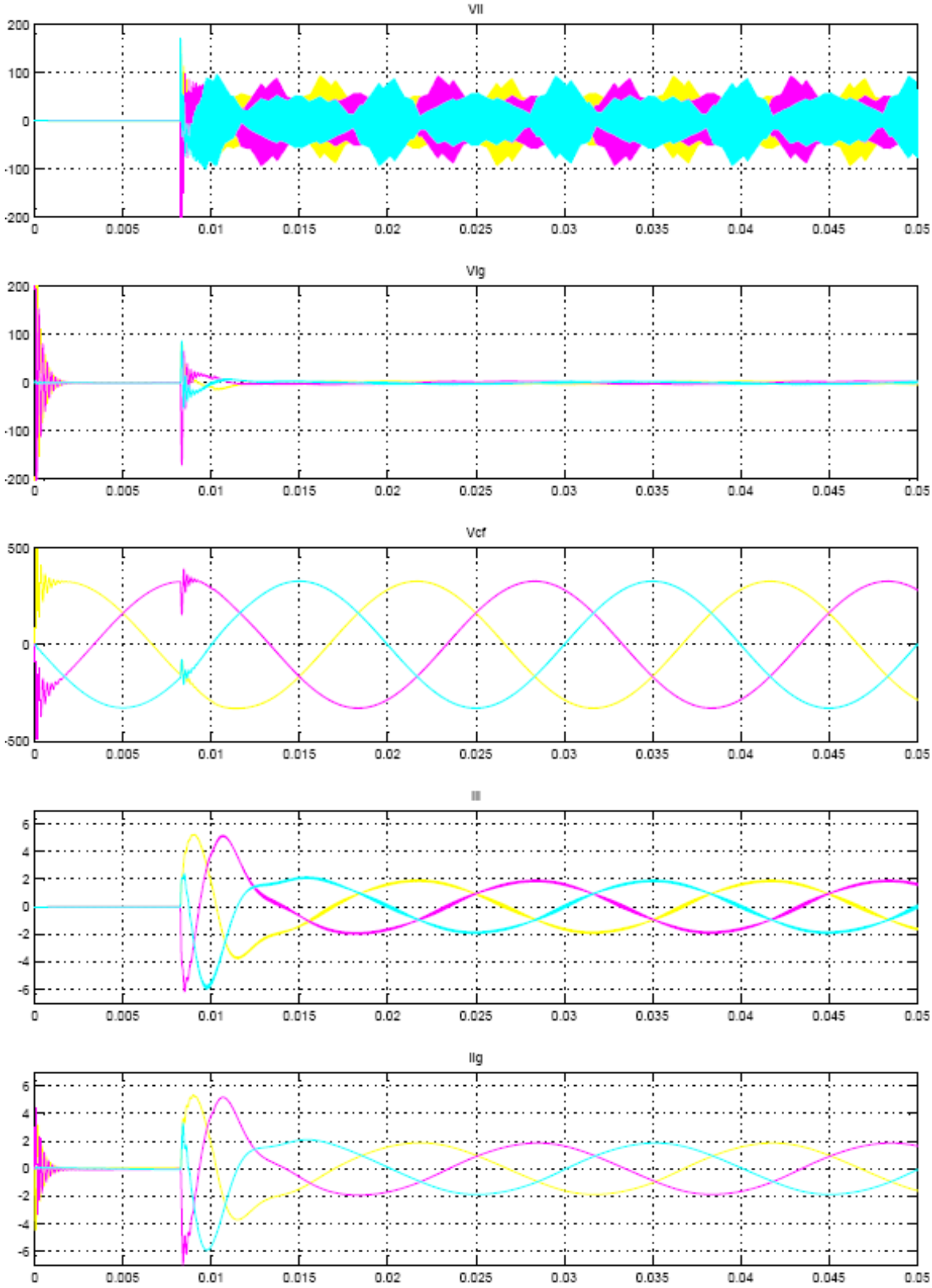

Figure 5.9: LCL filter current and voltage. From top: converter inductor voltage, grid inductor voltage, capacitor voltage, converter inductor current and grid inductor current

Harmonic analysis

In the simulation an analysis of the harmonic content in the grid inductor current of the LCL is made using the Powergui FFT tool. The analysis is made with a phase current of 1.3A rms, and sinusoidal PWM with third harmonic injection with a modulation ratio close to 1.15 is used. In figure 5.10 a spectrum analysis of the grid inductor current is shown, where the harmonics from 1st to 33rd of the fundamental are included.

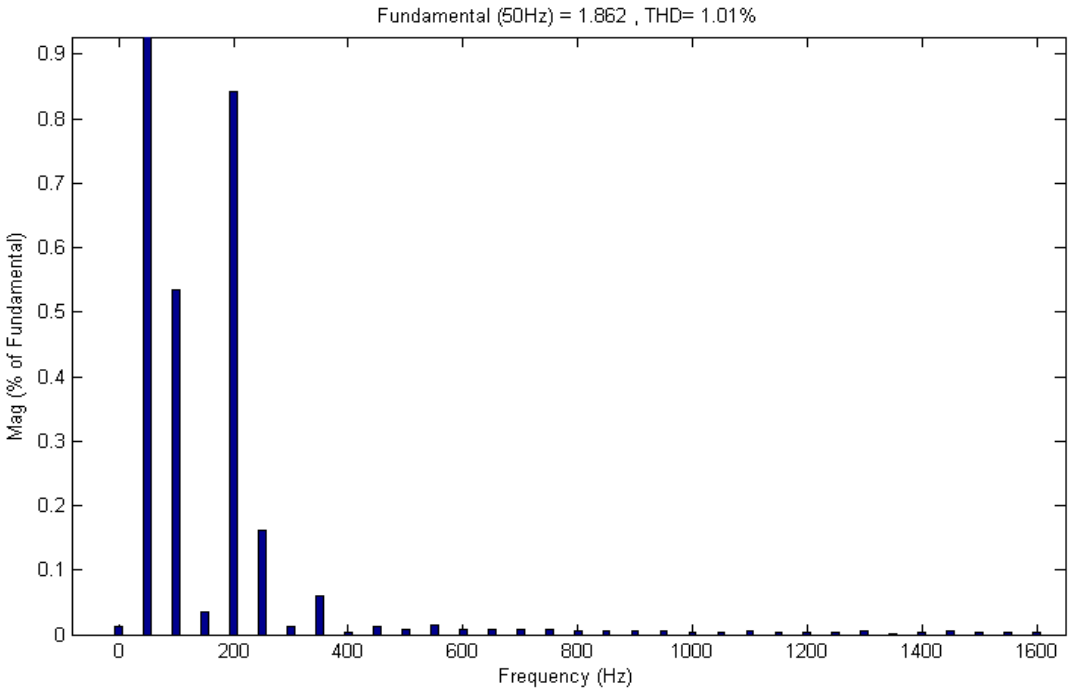

Figure 5.10: Harmonic spectrum of grid side inductor current, from 0 to 1650Hz

The lower harmonics found in figure 5.10 was not expected when using PWM at 20kHz. During the simulation it could be seen that the calculation of the pulse width had to be accurate in order to reduce these lower harmonic components. The calculation of the pulse width is in the simulation made the same way as in the DSP, using a up/down counter and a compare value for each phase. In the harmonic analysis a timer value (resolution) of 7500 was used. This corresponds to a clock frequency of 150MHz, which is the same as in the DSP. If much lower resolutions where used then the lower harmonic content soon crossed the limits of the allowed values, but the distribution of the harmonics changed. Therefore reducing the resolution could reduce the 2nd harmonic but increase the 5th harmonic, and in total increase the THD.

In figure 5.11 the same spectrum analysis is shown, but now including the harmonics up to 50kHz. In this figure harmonics in the side bands of the switching frequency and in the side bands of the multiple of the switching frequency is seen. The highest value of the side band harmonics is the one closest to the switching frequency, having an amplitude of approximately 0.2%.

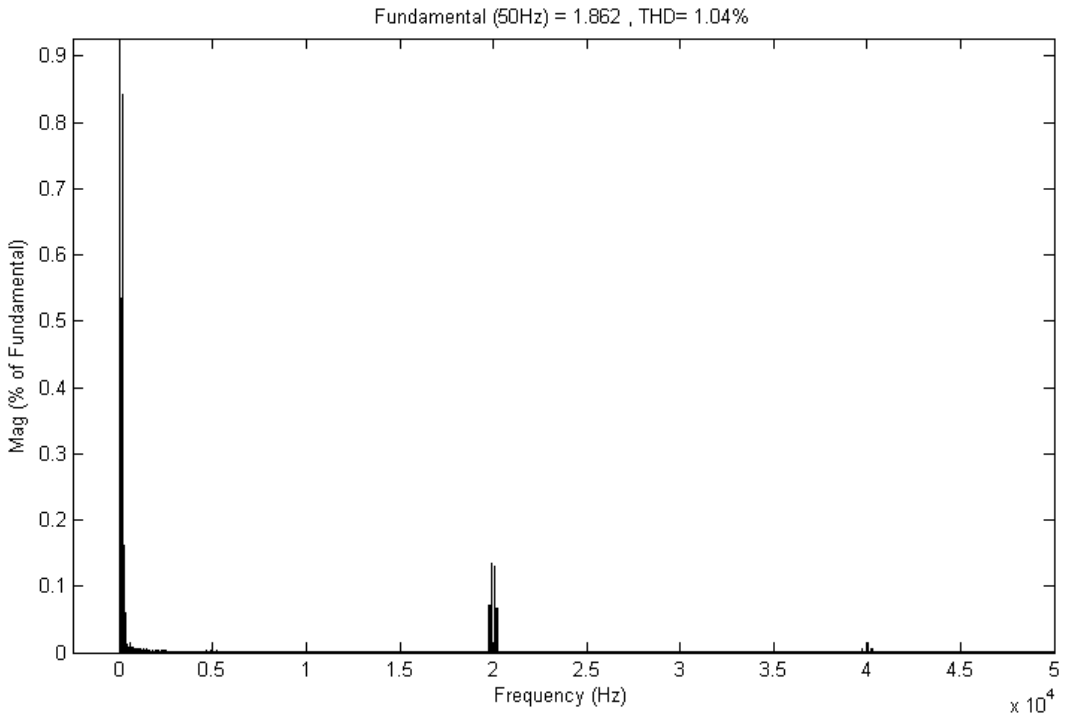

Figure 5.11: Harmonic spectrum of grid side inductor current, from 0 to 50kHz

6 EXPERIMENTAL RESULTS

6.1 DC-DC Converter

During the testing of the DC-DC converter it was several design errors which caused problems for the correct operation of the converter. Some of the most severe problems are explained in appendix 6. It is there shown that since there is a leakage inductance in the transformer, a clamping circuit will be needed in order to reduce the voltage spike which will be generated across the full bridge (see [26] and [27]). Also there where some problems with a very small magnetizing inductance in the transformer, which led to nonlinear operation of the converter. It showed out that the core used had a small gap in the centre leg which it was not supposed to have. When the core was replaced, this problem was solved. It also showed out that when positive duty cycle steps where applied, an inrush current proportional to the step size was experienced. This current was due to the charging of the DC-link capacitor, and could be troublesome because it could become quite large. The problems listed above where solved, but the final problem caused malfunction of the converter, with breakdown of the full bridges as a result. This problem was with high ripple in the gate of two diagonal mosfets already on when the two remaining diagonal switches where turned on, which is probably caused by some large di/dt‘s in the circuit and the problem increased with increased voltage across the bridge. Because of this improper operation of the DC-DC converter, only some limited testing of the MPPT algorithm was made converter.

6.1.1 MPPT

The MPPT was tested on a resistive load with the DC power supply at reduced input voltage since DC-DC converter was not capable of handling higher voltages. The idea was to use the DC-power supply as an ideal PV-power source, by setting a voltage and a current limit. This however was not working because there is one constant current region and one constant voltage region. In the constant current region the MPPT will work, but in the constant voltage region it can not function properly because the MPPT is depending on the direction of the voltage change. Ideally there would not be any change in voltage in the constant voltage region, but due to measurement noise, some inaccuracy of the power supply and rounding errors of the DSP, the voltage measurements fluctuates a little but in an arbitrary direction. These fluctuations confused the MPPT, and made the duty cycle step go in an arbitrary direction.

This was the only tests made before the full bridge was destroyed, and therefore no more effort was put into testing of the DC-DC converter.

6.2 DC-AC Converter

Since the DC-DC converter was not functioning properly the DC-AC converter had to be tested separately. Since no high voltage isolated DC power source was available at the moment of testing, the DC-AC converter was not connected to the grid, but the grid voltage was measured.

Many tests could have been made on this converter, but due to lack of time and the fact that the converter could not be connected to the grid only tests of the controllers, and a harmonic analysis was made. Other tests which would have been of interest is tests of grid standard compatibility, where the requirements in chapter 2.1.1 where put to the test.

6.2.1 PLL

In order to test the PLL it is difficult to apply a step in the angle of the grid voltage, so instead the response at start-up of the PLL is analysed. In figure 6.1 a plot of this response is plotted, where the frequency has a rise time of 2.8ms, with a overshoot of 5.3% and a settling time of approximately 7ms.

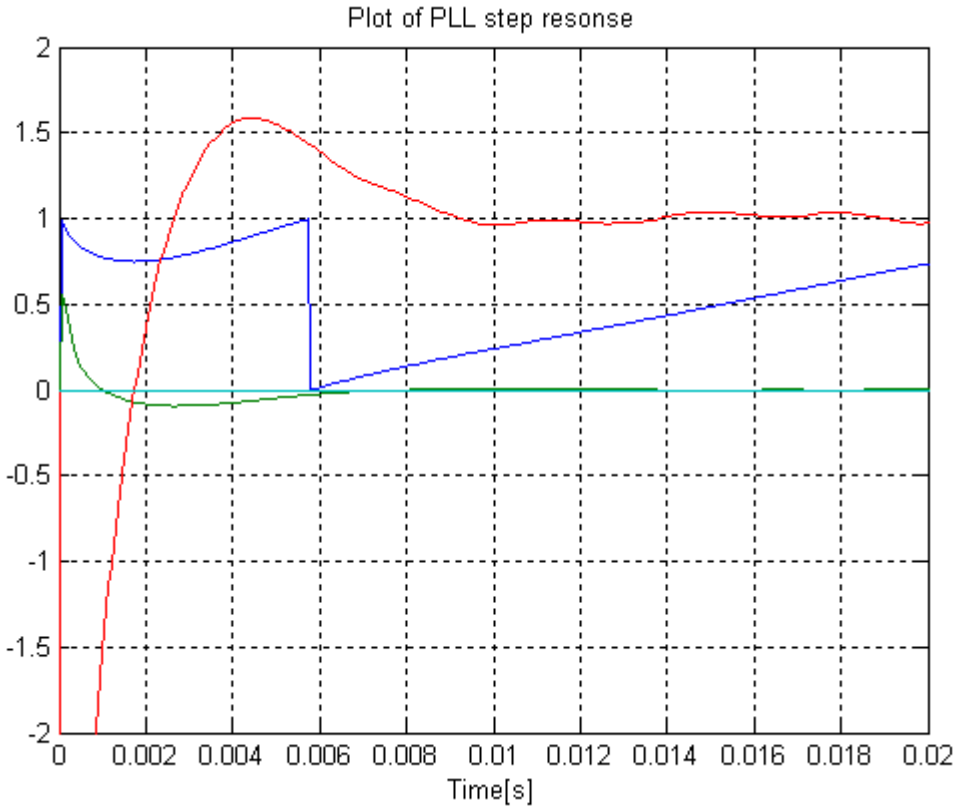

Figure 6.1:
Red: Phase locked frequency in PU
Blue: Phase locked angle in PU
Green: PLL PI controller error

6.2.2 Current control

The step response of the current controllers where tested with the optimized parameters, and a step from 0.1pu of current to 0.7pu of current. The response can be seen in figure 6.2. The response of the d-axis current has more overshoot and shorter rise time than expected from the optimization. By adjusting the controller parameters to $0.5K_p$ and $1.08T_i$, the response became close to what was expected from the modulus optimization.

The q-axis current shows a minor response to the step in the d-axis current. Due to the feedback used, there should ideally not have been any response at all. During steady state it could be seen a ripple of 200Hz superimposed on the d- and q- axis current which the current controllers where not able to reduce to zero.

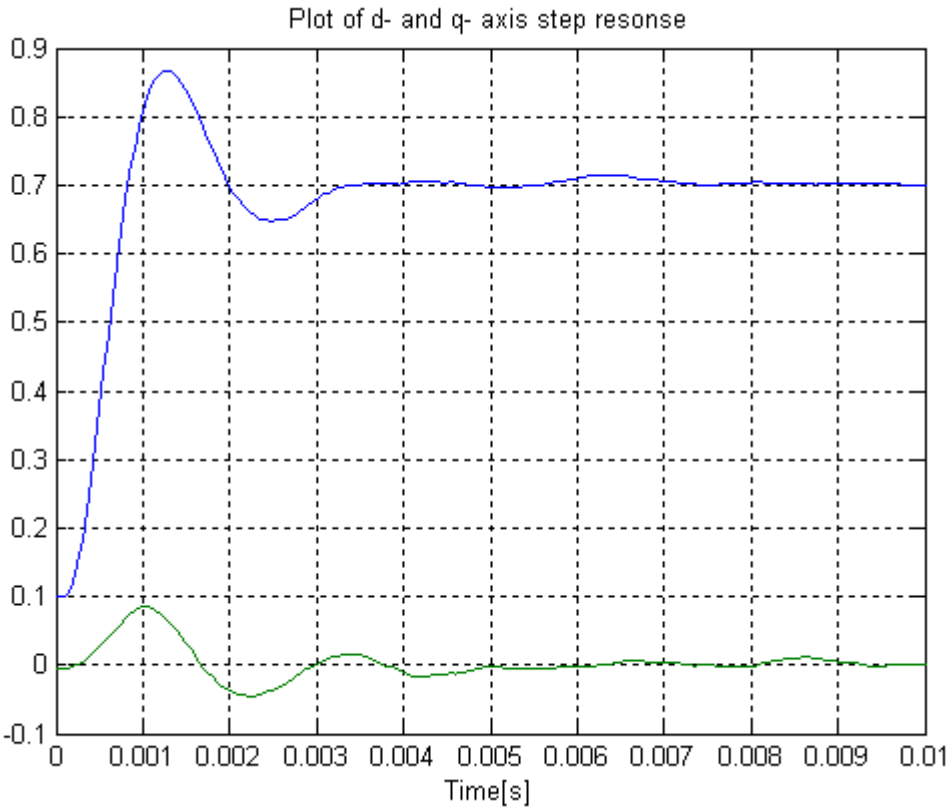

Figure 6.2: Step response of the d- and q-axis current to a step from 0.1 to 0.7pu in the current reference.
Blue: d-axis current
Green: q-axis current

6.2.3 Voltage control

The voltage control was tested with the given controller parameters, but with these parameters the control loop became extremely sensitive to noise and made the controller fluctuate between its upper and lower limit. This was due to the proportional gain being to high compared to the ripple in the measurements. The proportional gain is proportional to

the size of the DC-link capacitance, and since the DC-AC converter in this system is much larger than the rating of the rest of the system, the gain becomes large compared to the system rating.

In order to reduce this problem a filter with a corner frequency of 1kHz was used in the feedback instead of the one with 3kHz, and new controller parameters where calculated based on that. This reduced the noise in the feedback and made the control loop less responsive to the noise, but still the gain of the controller is so large that only a minor step in the DC-link voltage reference could be applied without going into saturation. In the figure below a step of -0.5 V in the reference value is applied, and it can be seen that it has a rise time of approximately 7ms, which equals 3.95 times the new T_{eqv}. The overshoot and the settling time is more difficult to decide since there is still some noise in the measurement.

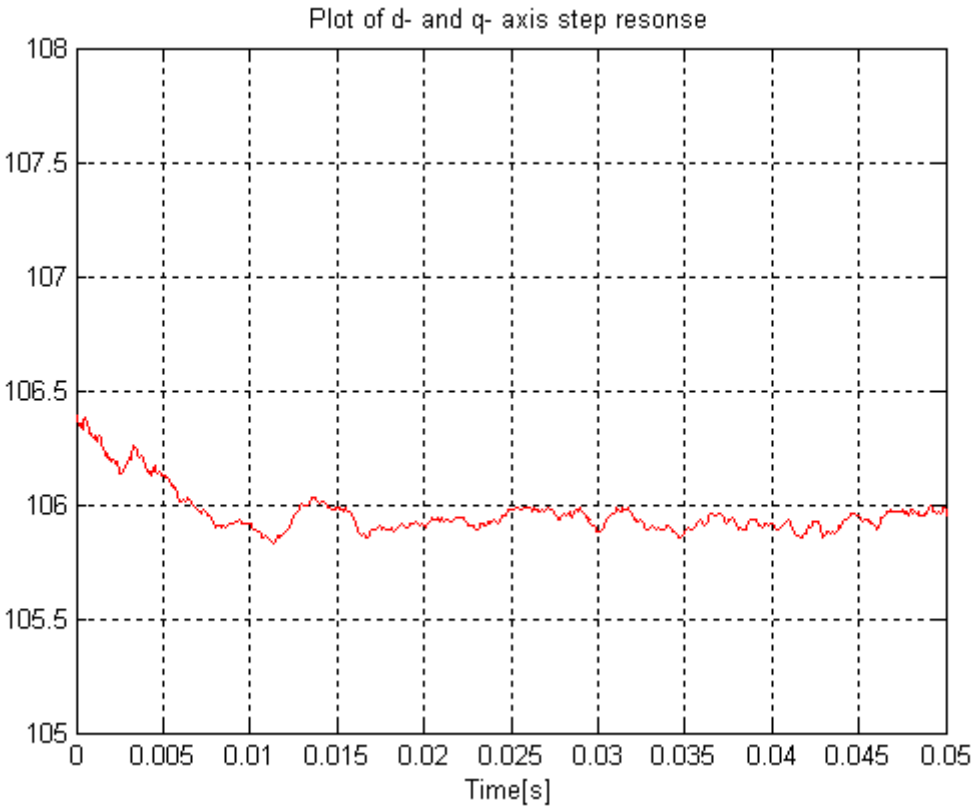

Figure 6.3: Step response in the voltage control loop.

6.2.4 LCL-filter

In figure 6.4 and 6.5 the currents and voltages across the different elements of the LCL filter is plotted during steady state at 1.3A rms phase current. The PWM method used is the SVPWM method at maximum modulation ratio within the continuous mode. As expected most of the voltage and current ripple can be seen in the inverter side inductor, the grid side inductor has therefore only a small amount of the total ripple. The voltage across the capacitor is a smoothed sinusoidal voltage with low ripple in the voltage.

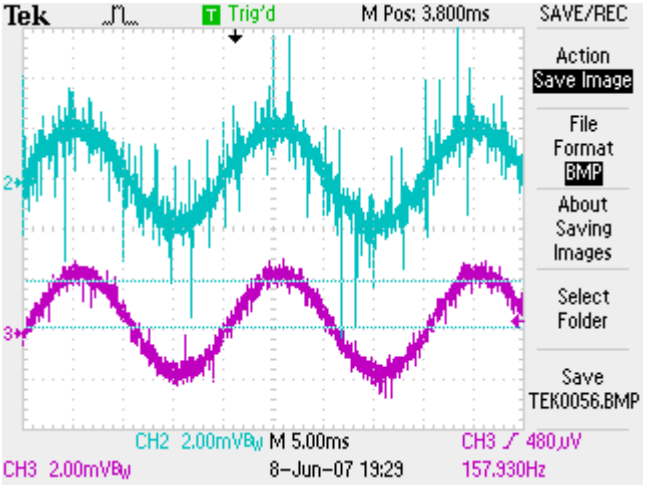

Figure 6.4: Voltage in the LCL filter inductances during steady state
Blue: Inverter side inductor current
Purple: Grid side inductor current

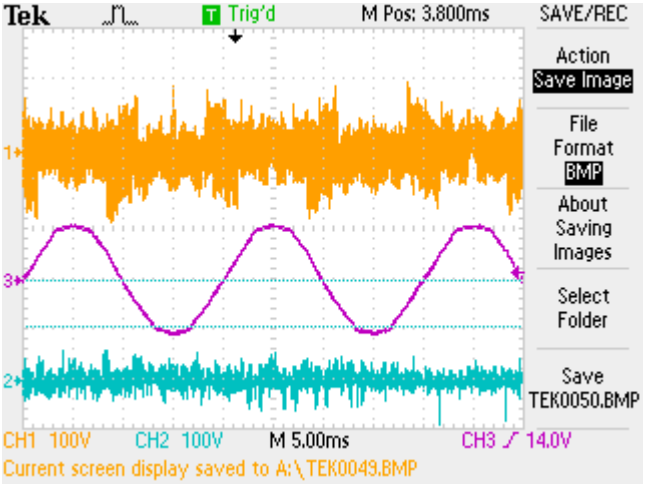

Figure 6.5: Voltage across the LCL filter elements during steady state
Yellow: Inverter side inductor voltage
Purple: Capacitor voltage
Blue: Grid side inductor voltage

Harmonic analysis

The harmonic content of the current in the grid side inductor was measured with three different PWM methods. When measuring the harmonic content the modulation was ran at the maximum modulation ratio within the linear range, and the input voltage was adjusted in order to get the same fundamental current from all of them. The harmonic spectrum was measured with a Fluke 43 Power Quality Analyser, which can measure up to the 50th harmonic. This means the harmonics around the swithcing frequency could not be found. In the figure below the spectrum of the harmonics from 1st to 33rd are shown, above this the harmonic content was neglicible, and was therefore not plotted. The fundamental current had a rms value of 1.3A, and the load was a resistive load of 50Ω.

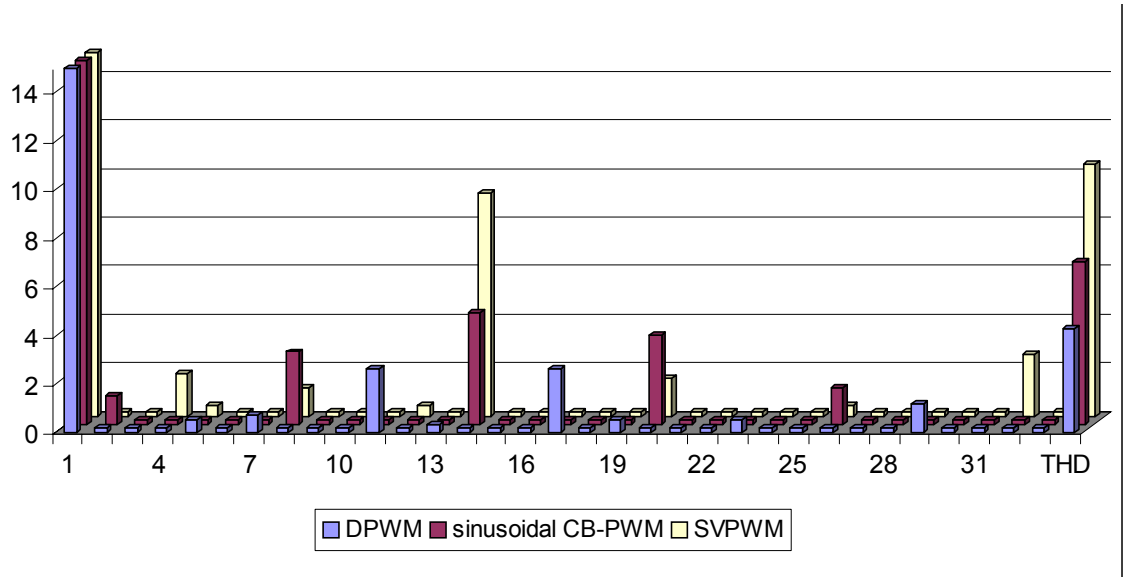

Figure 6.6: Harmonic spectrum in % of fundamental current for three different PWM methods

7 DISCUSSION, CONCLUSION AND FURTHER WORK

7.1 Discussion

In this thesis much of the basic theory on designing a converter for grid connection of PV systems have been explained. Based on the theory described in the first chapters a laboratory setup has been buildt. This setup has been simulated using Simulink and the setup has been tested in the laboratory. The laboratory setup has as far as possible been made with well known solutions and techniques, which are not always the most efficient or reliable but usually easier to implement. It has however made it possible to create a complete system in the time available, instead of focusing on some minor part of the system, which would have been the case if more advanced solutions where to be used.

Even though the system was designed in this manner, not everything worked out easily. The DC-DC converter has caused a lot of problems, as will be explained in the next chapter, and because of this the system could not be tested with this converter. This has made it impossible to run some tests, and the time for testing became very reduced.

7.1.1 DC-DC converter

The DC-DC converter has been the major troublemaker in this design. It showed out that this converter topology was a design very few people had any experience with, and the combination of this being a current fed full bridge with a transformer and a rectifier in cascade, made it much more complex than a converter with only one stage.

Much of the work done in this thesis has been on designing and testing of the DC-DC converter. Lots of time has been used during the design process and on learning how to build a converter, but most of the time is probably spent on testing and correcting design errors in the lab. From the beginning of this assignment it was the intention that as little time as possible should be used on designing and building this converter. It can be seen now that since the converter is not working properly, that either building the converter should not have been a part of this thesis or it should have been a much larger one.

However the isolated current fed full bridge converter is a topology which according to chapter 2.4.2 should be well suited for use with PV-systems, because of its high suitability for high input voltages, high efficiency and bidirectional core excitation. Therefore it is still of interest to do further research on this topology, and a converter for laboratory use and testing should be buildt.

7.1.2 MPPT

In the simulation the MPPT tracked the MPP as it was expected to, but there where some experiences made during the simulations. First it was seen that the model for the PV panels found in chapter 2.2.1 was not very accurate, this was due to the fact that none of the internal resistances and other nonidealities where included in the model. This means the model is not useful for simulating specific solar panels, but for testing a MPPT algorithm it

is adequate. The model also showed that under partially shadowed conditions two or more maximum power points may occur, and this can “confuse” the P&O algorithm so that it does not always find the most efficient power point. Therefore it can be stated that in order to maximize the efficiency during cloudy days, a more advanced power point tracker which is able to track the most efficient power point should be used.

Based on the calculations made when calculating the sampling time of the P&O algorithm, the oscillations should have reached 10% of its initial value before the next perturbation, and it can be seen from in the simulation that this is approximately true.

It was found that with a step in irradiance of 100%, the tracker would use 0.8s before reaching the new power point. This shows that the tracker is not a fast process, but since the operating conditions of the PV panels are also slow, it is suspected that this will not have any large influence on the dynamic tracking error and the efficiency. During steady state operation the efficiency of the algorithm was as high as 99.9% with the optimized MPPT, but this is expected to decline with 1-3% during dynamic conditions. In order to test the tracker during dynamic conditions, the simulation model should be expanded in order to test the system over time, with changing operating conditions for the solar panels.

The MPPT in the experimental setup was not tested, but it was found that an ordinary DC-power supply with the current voltage characteristic of an ideal solar cell can not be used to test if the MPPT tracker works. Therefore in order to make reliable tests, field testing of solar panels must be made, or if possible a DC-power supply which is able to accurately simulate a PV power source should be used. The latter would be an enormous help in testing of the PV converter in order to run accurate and repetitive tests.

7.1.3 PLL

Both in the simulation and in the experimental tests the PLL manages to lock the phase to the grid voltage in approximately 10ms. This shows that the loop is not very fast, so the dynamics of the loop becomes poor, but the filtering effect of the control loop is high. Therefore it will not be so sensitive to harmonics and phase unbalancing. Since both the dynamics and the filtering effect should be as high as possible, and they are inconsistent, the PLL should be tested during different grid conditions to see if the current parameters are the best. It should then be tested with a grid given phase jumps, harmonics and phase unbalance.

7.1.4 Current control

The response from a step in the d-axis current reference led to a to a slow response in the simulation and to fast response in the experimental test. These where only minor errors, and by small adjustments of the controller parameters the response became as expected by modulus optimization. The reason for these small errors can be many, e.g errors due to simplifications made in the model when optimizing, inaccurate values of the components used in the laboratory setup, computational rounding errors and decoupling errors.

The decoupling did not remove the coupling between the axes completely. A probable reason for this is the different time delays in the control loop. In order for the feed forward term to work as expected the q-axis voltage must be updated immediately when the d-axis current changes. This is not possible in a real system and the decoupling will therefore have reduced effect.

Even though the optimization did not give the correct response without adjusting the values, this cannot be expected either from a real system since the models used will only be approximations to the real system. However the system response was so close to the expected, that it can be said that the system models used are sufficient for optimizing the control system.

7.1.5 Voltage control

In the simulation a step in the DC-link voltage led to a faster response with less overshoot then what was expected, but it is so close that it shows that the system models used in the optimization is close to the simulated model.

In the experimental setup the combination of a high gain due to a large capacitor bank and some noise in the measurements, led to the fluctuations between the upper and lower limit in the output of the voltage controller. To reduce the effect of this ripple the feedback filter corner frequency was reduced from 3kHz to 1 kHz, thus reducing the ripple. Still it can be seen from figure 6.3 that there is some ripple which makes the response unclear, but it can be seen that the response is close to the expected, but with less overshoot.

In this control loop it is possible that a filter with an even lower cutoff frequency should have been used, or the controller itself could have been adjusted to have a larger filtering effect, in order to remove even more of the fluctuations in the control loop because of the noise. This would however lead to a slower control loop. If the feedback filter becomes much larger then the other time constants, it could be possible to compensate this phase delay by using a PID controller instead of the PI controller as explained in chapter 3.10.2, which would probably have improved the response.

It should be noted that because of the large capacitor bank and the small current rating of the converter, the voltage controller will saturate by very small changes in the voltage. Therefore the effect of the improved response will only have an influence during small variations in the DC-link voltage.

7.1.6 LCL filter

The plots of the currents and voltages from the LCL filter in the simulations and in the practical case is similar. The amplitude of the high frequency voltage ripple is almost equal in the simulated and in the experimental case. As expected most of the ripple in the output voltage is handled by the inverter side inductor since it is closest to the source and the largest. It can also be seen that the current ripple in the grid side inductor is largely reduced, so the current is almost sinusoidal.

Harmonic analysis

In the harmonic analysis made in the simulation, harmonics where found in the side bands of the switching frequency and in the side bands of the multiples of the switching frequency of the grid side current in the LCL filter. This is as expected from the ideal case, and the highest of these where 0.2% of the fundamental. This is approximately as the LCL filter was dimensioned for, and the attenuation is below the levels stated in table 2.3. The THD is also inside the limit given, but there are some harmonics around the fundamental frequency which is not expected. It was experienced that when reducing the counter value (reducing the resolution of the pulse width), the amount of harmonics of the fundamental increased. It can therefore be concluded that the calculation and implementation of the correct pulse width is important in order to generate the desired waveform.

In the analysis in the experimental setup three PWM methods was tested, and all with very different results. First it can be said that the analysis did not include the higher harmonics of the switching frequency, so the attenuation of these remain unknown. What was not expected was the high content of harmonics of the fundamental frequency, from 2nd harmonic and up. This was so high that the harmonics content becomes higher than allowed by the standards when SVPWM an sinusoidal CB-PWM is used. This must mean that the generated sine wave is not completely sinusoidal, and since the LCL filter is designed with a much higher cutoff frequency, these are not attenuated by the filter.

This is basically the same problem as in the simulations, but the harmonic content is different. In the simulations it was showed that it is very important that the pulse width is calculated correctly in order to generate the wanted waveform. Probably the same is the problem in the DSP, but since the resolution is the same as in the simulations and the harmonic content is much higher, it is probably something else causing the deviation from the ideal pulse width. This problem can also explain the 4th harmonic which is seen in the d- and q- axis current, since the 4th harmonic with the SVPWM is quite noticeable.

The pulse width was generated based on an angle going linearly from 0 to 2π, so the basis should be correct assuming this angle is updated each sampling interval. Based on this angle the pulses are modulated according to the different algorithms used for the PWM methods. Since the calculations are digital, there will be some rounding errors which can contribute to this. Another possibility is that not all the interrupts are executed as they should, and then the angle and the compare values will not be updated. Ideally the new compare values for the generation of the PWM signals should be updated at the underflow or period match of the counter (top or bottom of triangular carrier wave), but because there are some calculations which has to be made that is not always the case. There will also be different time delays and dead times in the loop from the DSP through the gate driver and into the gate. All of this can contribute to making the effective pulse width of the inverter deviate from ideal.

Since this problem occurs in all the three PWM techniques used, it can therefore be assumed that the problem is not with the algorithms them self but more with the timing of the algorithms. Therefore the execution of the algorithms should be controlled and if possible adjusted to make the timing better. It should also be checked if it is possible to reduce the rounding errors, and it should be checked if all the interrupts run as they should. It is also possible that in order to reduce the problem even more, some sort of compensation for the dead time and time delays in the loop should be implemented. The PWM modulation should at least be corrected such that the harmonic content is below the limits of the standards.

7.1.7 The overall system

Even though only limited testing of the system was possible, most of the system that was tested worked as expected. However the system has only been tested under limited operating conditions, with a reduced number of components. In order to see if the system is stable under other operating conditions and as a complete system, more extensive testing should be made.

First of all the system should be made complete with an isolated high output voltage DC-DC converter, and a PV panel or a powersupply able to simulate a PV panel, should be used a power source. This system should then first be tested separately to see if the MPPT tracker works as expected, both during steady state and during different operating conditions. When the testing of the DC-DC converter is finished, the converters can be connected together and to the grid. The overall system can now be tested, and the DC-AC converter should be phased into the grid. When this is done the tests mentioned in the sections above should be made. Also it should be verified if the converter is working according to the requirements given in the standards from chapter 2.1., including anti-islanding and a power quality analysis.

7.2 Conclusion

In this thesis the most basic theory on the design of an *electrical power converter for photo-voltaic systems* has been shown. Based on the theory described a complete system model has been designed. The model is designed with focus on testing of the theoretical models derived for the control systems, and with low focus on hardware efficiency. The system is based on the use of a *multi string inverter,* which consists of an isolated *current fed full bridge DC-DC converter*, a *3-phase full bridge DC-AC converter* with a *LCL filter* as the grid interface. This system has been simulated in Simulink, and an experimental setup has been made.

The DC-DC converter was not available as a laboratory converter, and therefore it had to be designed and constructed. Since the converter topology is not a common one, theoretical models was developed for the converter, and based on this a converter was constructed. However the converter did not function as expected during the testing, because of problems caused by phenomena not included in the ideal models developed. It was also shown that since the converter was buildt on a printed circuit board with an integrated full bridge, it was difficult to apply changes and troubleshoot the circuit. The full bridge in the circuit eventually broke down, so the converter had to be put aside for the rest of the experiments. It is however shown that the *current fed full bridge DC-DC converter* is an interesting topology for use in photo-voltaic systems, and therefore further studies should be made on this converter topology. The *three phase full bridge DC-AC converter* was therefore tested on a resistive load instead of the grid, since isolation was needed.

The simulations of the PV panels showed that the models used in this thesis is to simple to accurately model a real PV panel, but for testing of the a *maximum power point tracker* algorithm they are adequate. The model also showed that during partial shadowing of the solar panels, two or more power points might occur, and then the *perturb & observe* method used would not be able to track the power point with the maximum power. The algorithm showed an efficiency close to 100% during steady state operation, but it is predicted to be lower during dynamic operating conditions. Therefore the efficiency of the algorithm should be simulated with varying operating conditions. The same tests should be made on the experimental setup once a functional DC-DC converter is made.

Both the simulations and the experimental tests showed that the models developed for the control systems was close to the real and simulated system. A *phase locked loop* with a PI controller was used for the synchronization with the grid, and this was able to lock the phase in approximately 10ms. For the power flow into the grid, current controllers in a *rotating reference frame* was used, and when locked to the grid frequency the *active power* could be controlled by the current in direct axis and the *reactive power* by the quadrature axis. The direct current reference was sat by a DC-link voltage controller in cascade. These control systems has been modelled and optimized, and the results from the simulations and the experiments showed that the deviation from the expected result was small. However there was some problems with noise in the feedback to the DC-voltage controller in the experimental setup.

The LCL filter worked as expected, as it attenuated the ripple around the side bands of the switching frequency in the grid side current below the limits in the standards from IEEE and IEC. What was not expected was that the harmonic analysis also showed high levels of harmonics centered around the fundamental frequency, which ideally should not have been there. The reason for these have been found to be inaccurate pulse width causing the output of the inverter to deviate from the ideal sinusoidal shape it should have.

Since the DC-DC converter could not be used, and less time has been available for testing, there is still much work that can be done on this project. First of all the DC-DC converter should be finished, and then more extensive testing of the systems should be made in order to see how it works during grid disturbances and failures. The simulations could also be extended in order to simulate the same problematic.

7.3 Proposed further work

A PV simulator should be made, which is able to give accurate repeatable outputs simulating a given PV panel during different operating conditions. The simulator could be a DC-DC converter with a graphical computer interface, in order to make the adjustments intuitive and simple. In that way the simulator will be a good tool for educational purposes as well as for testing purposes.

Since the isolated current fed DC-DC converter topology is a promising for use with photo-voltaic systems, a more optimal design of the converter used in this project should be made. The new converter should be made for laboratory use, with a wide operating range and more hardware based protection of the circuitry.

Develop the laboratory setup made in this thesis further, with the goal of one day creating a setup which can be used in the renewable energy laboratory at NTNU. This will also include further testing of the setup, with the tests that have been suggested in the discussion. The setup should have a user friendly graphical computer based interface, which is suitable for both research and educational purposes.

LITERATURE

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APPENDIX

1 DC-DC CONVERTER ANALYSIS

In this chapter different calculations and models has been made from the DC-DC shown in figure 1.1. This converter type is called an *isolated full bridge boost converter*.

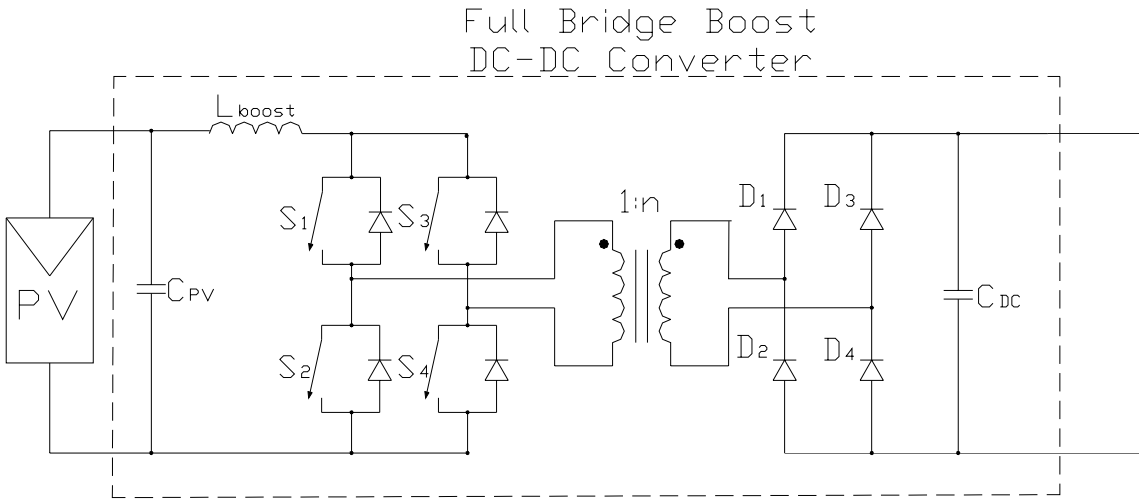

Figure 1.1: Schematic of DC-DC converter

1.1 Steady state analysis

The switching scheme for the DC-DC converter is shown in figure 1.2.

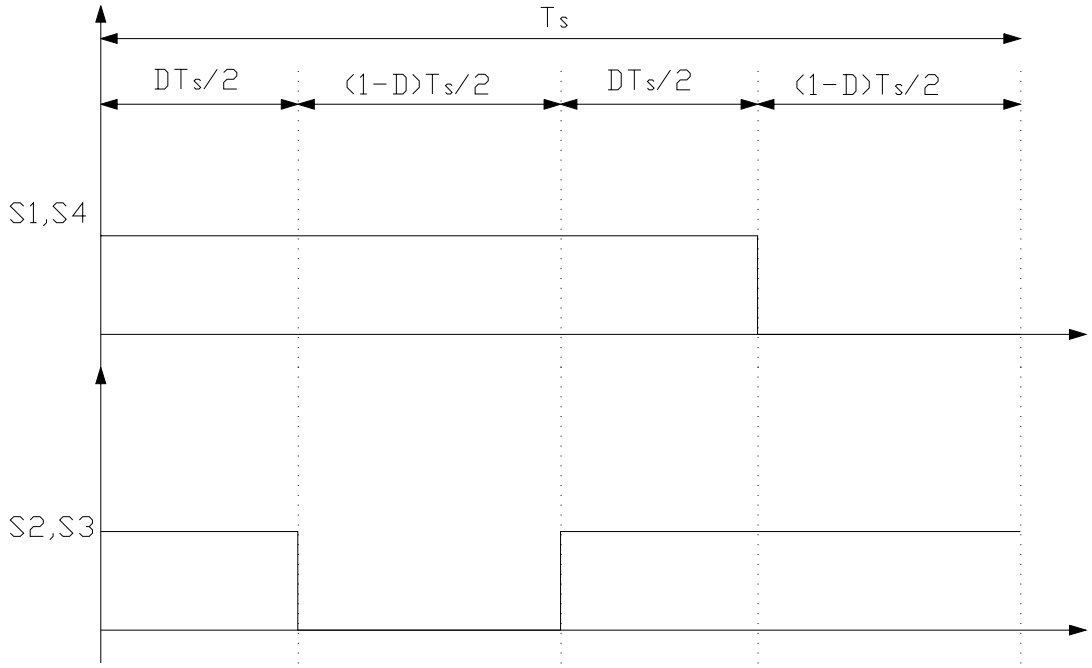

Figure 1.2: DC-DC switching scheme

With this switching scheme, the voltage at the primary side of the transformer $v_p(t)$, and the inductor current $i_L(t)$ and voltage $v_L(t)$ for one period, is shown in the figure below.

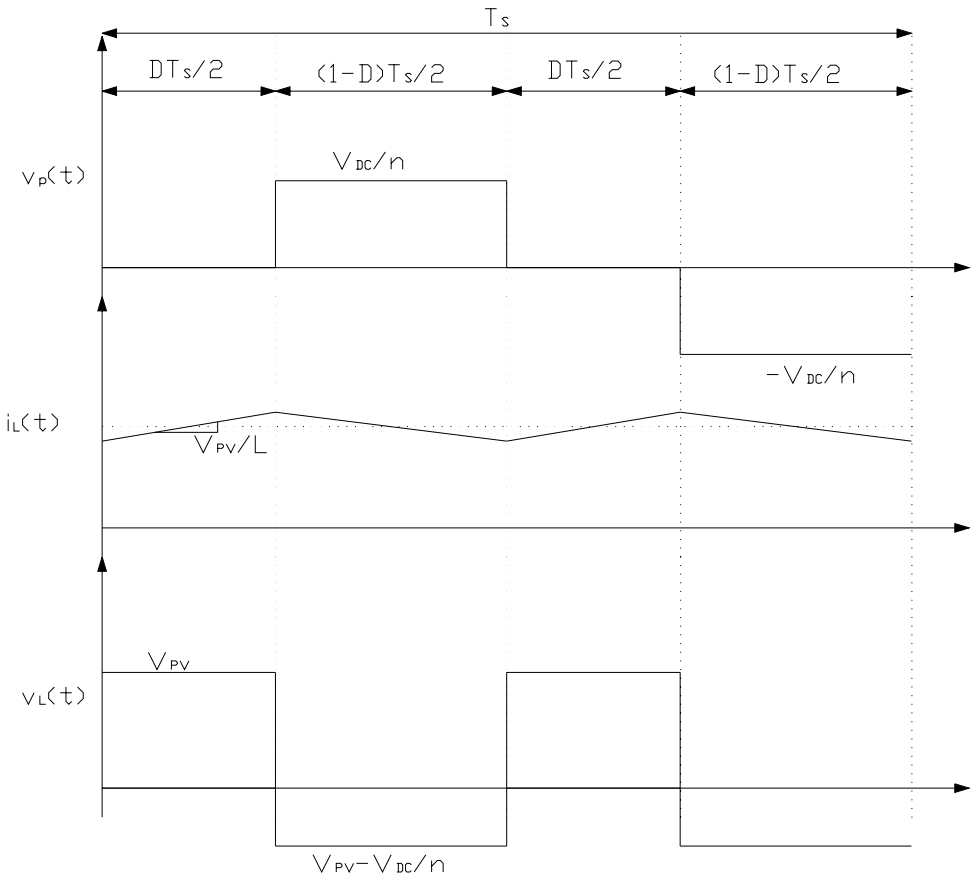

Figure 1.3: Voltage over primary side of HF transformer, and inductor current and voltage.

From figure 1.3 it can be seen that the inductor ripple frequency is.

$$f_L = 2f_s = \frac{2}{T_s} \tag{1.1}$$

1.1.1 DC-link voltage

For $\frac{DT_s}{2} \le t \le \frac{T_s}{2}$ the voltage balance is:

$$v_{PV}(t) + v_L(t) = \frac{v_{DC}(t)}{n} \Rightarrow V_{PV} + V_L = \frac{V_{DC}}{n} \tag{1.2}$$

Sum of voltage over the inductor must equal zero

$$V_{PV}\frac{DT_s}{2} = V_L\frac{(1-D)T_s}{2}$$
$$V_L = V_{PV}\frac{D}{1-D} \tag{1.3}$$

(1.3) inserted in (1.2) gives the steady state DC-link voltage

$$V_L = V_{PV}\frac{D}{1-D}$$
$$V_{DC} = n\left(V_{PV} + V_{PV}\frac{D}{1-D}\right) = n\left(V_{PV}\frac{1-D}{1-D} + V_{PV}\frac{D}{1-D}\right) = V_{PV}\frac{n}{1-D} \tag{1.4}$$

Solving for the duty cycle as a function of output and input voltage

$$D = 1 - \frac{V_{PV}\cdot n}{V_{DC}} \tag{1.5}$$

1.1.2 DC-link current

Solving for the average DC-link current as a function of PV current and duty-cycle

$$I_{DC} = \frac{2}{nT_s}\int_{\frac{DT_s}{2}}^{\frac{T_s}{2}} I_L dt = \frac{2}{nT_s}\int_{\frac{DT_s}{2}}^{\frac{T_s}{2}} I_{PV} dt$$
$$= \frac{2}{nT_s}\left(I_{PV}\frac{T_s}{2} - I_{PV}\frac{DT_s}{2}\right) = I_{PV}\frac{1}{n} - I_{PV}\frac{D}{n}$$
$$= I_{PV}\frac{(1-D)}{n} \tag{1.6}$$

1.1.3 Inductor current ripple

The ripple during steady state is derived using the inductor voltage equation

$$v_L(t) = L_{boost}\frac{di_L(t)}{dt}$$
$$\Delta V_L = L_{boost}\frac{\Delta I_{L\_PP}}{\Delta t}$$
$$\Delta I_{L\_PP} = \frac{1}{L_{boost}}\Delta V_L\cdot\Delta t = V_{PV}\frac{D}{2L_{boost}}T_s = V_{PV}\frac{V_{DC} - V_{PV}\cdot n}{2L_{boost}V_{DC}}T_s$$
$$\Delta I_L = \frac{\Delta I_{L\_PP}}{2} = V_{PV}\frac{V_{DC} - V_{PV}\cdot n}{4L_{boost}V_{DC}}T_s \tag{1.7}$$

1.1.4 Boost inductor

The largest boost inductor will be needed close to the limit between continuous and discontinuous conduction mode, so by inserting I_{LB} into equation (1.7), and solving for the inductor gives

$$L_{boost} = V_{PV} \frac{V_{DC} - V_{PV} \cdot n}{4 I_{LB} V_{DC}} T_s \tag{1.8}$$

1.1.5 PV capacitor

The PV capacitor is calculated based on the assumption that all the inductor current ripple will be delivered by the capacitor.Current ripple in the capacitor is given by.

$$\begin{aligned} i_{C_{PV}} &= C_{PV} \frac{dV_{PV}}{dt} \\ \Delta I_{C_{PV}} &= \Delta I_L = C_{PV} \frac{\Delta V_{PV}}{\Delta t} \end{aligned} \tag{1.9}$$

Having the expression for the inductor current ripple from (1.7), and solving for the PV capacitor.

$$\begin{aligned} C_{PV} &= \Delta I_L \cdot \frac{\Delta t}{\Delta V_{PV}} = \Delta I_L \cdot \frac{D T_S}{2 \Delta V_{PV}} \\ &= V_{PV} \frac{\left(1 - \frac{V_{PV} \cdot n}{V_{DC}}\right)}{4 L_{boost}} T_s \cdot \frac{\left(1 - \frac{V_{PV} \cdot n}{V_{DC}}\right)}{2 \Delta V_{PV}} T_S = V_{PV} \frac{\left(1 - \frac{V_{PV} \cdot n}{V_{DC}}\right)^2}{8 L_{boost} \Delta V_{PV}} T_s^2 \end{aligned} \tag{1.10}$$

Where ΔV_{PV} is the allowed voltage ripple at the PV side during steady state.

1.1.6 DC-link capacitor

Assuming the DC-link current to be constant, the capacitor is given at the PV maximum power. The capacitor must deliver current during the 1st and 3rd interval, and the length of one of these intervals is

$$\Delta t = \frac{D T_S}{2} \tag{1.11}$$

The voltage ripple in the DC-link can be found by

$$i_{C_{DC}} = I_{DC} = C_{DC}\frac{dV_{DC}}{dt} \tag{1.12}$$

From this the capacitor can be derived as

$$C_{DC} = I_{DC}\frac{\Delta t}{\Delta V_{DC}} = I_{DC}\frac{DT_S}{2\Delta V_{DC}} = I_{DC}\frac{\left(1-\frac{V_{PV}\cdot n}{V_{DC}}\right)T_S}{2\Delta V_{DC}} = \frac{I_{DC}}{V_{DC}}\frac{(V_{DC}-V_{PV}\cdot n)T_S}{2\Delta V_{DC}} \tag{1.13}$$

Where ΔV_{DC} is the allowed voltage ripple in the DC-link during steady state.

1.1.7 Limit between continuous and discontinuous conduction

Inductor current at the limit:

$$I_{LB} = \Delta I_{L\_limit} = \left(V_{PV}\frac{V_{DC}-V_{PV}\cdot n}{4L_{boost}V_{DC}}T_s\right)_{limit} \tag{1.14}$$

DC-link current as a limit (by applying (1.6)):

$$I_{DCB} = I_{LB}\cdot\frac{(1-D)}{n} \tag{1.15}$$

1.1.8 Max blocking voltage switches

During the first and third interval the voltage over all the switches is zero, during the second interval the voltage over the switches is:

$$\begin{aligned} V_{S1} &= V_{S4} = 0V \\ V_{S2} &= V_{S3} = \frac{V_{DC}}{n} \end{aligned} \tag{1.16}$$

and during the fourth interval:

$$\begin{aligned} V_{S2} &= V_{S3} = 0V \\ V_{S1} &= V_{S4} = \frac{V_{DC}}{n} \end{aligned} \tag{1.17}$$

The maximum blocking voltage over the switches is therefore:

$$V_{S\_max} = \frac{V_{DC}}{n} = V_{PV}\frac{1}{1-D} \tag{1.18}$$

1.1.9 Max blocking voltage diodes

When reverse biased, the maximum voltage over one diode is the secondary voltage of the transformer, which equals the DC-voltage

$$V_{D\_\max} = V_{DC} \tag{1.19}$$

1.1.10 Current rating switches

Maximum average current through one switch:

$$I_{S\_MAX} = \frac{I_{PV}}{2} \tag{1.20}$$

Max peak current through one switch

$$I_{S\_P\_MAX} = I_{PV\_MAX} + \Delta I_{L\_MAX} = I_{PV\_MAX} + \left(V_{PV} \frac{V_{DC} - V_{PV} \cdot n}{4 L_{boost} V_{DC}} T \right)_{MAX} \tag{1.21}$$

1.1.11 Current rating diodes

Maximum average current through one diode

$$I_{D\_MAX} = \frac{I_{DC}}{2} = I_{PV\_MAX} \frac{(1-D)}{2n} \tag{1.22}$$

Max peak current through one diode:

$$I_{D\_P\_MAX} = \frac{1}{n}\left(I_{PV\_MAX} + \Delta I_{L\_MAX} \right) = \frac{1}{n}\left(I_{PV\_MAX} + \left(V_{PV} \frac{V_{DC} - V_{PV} \cdot n}{4 L_{boost} V_{DC}} T \right)_{MAX} \right) \tag{1.23}$$

1.1.12 Transformer winding ratio

Based on equation (1.4) the transformer winding ratio can be found by

$$n = \frac{V_{DC}}{V_{PV\_\min}}\left(1 - D_{\max}\right) = \frac{V_{DC}}{V_P} \tag{1.24}$$

1.2 Small signal AC modelling

In this chapter an equivalent circuit based on the small signal AC model will be derived. Based on the methods described in [30]

In this derivation the duty cycle is defined as

$$\begin{aligned} d(t) &= \text{dutycycle} \\ d'(t) &= 1 - d(t) \end{aligned} \tag{1.25}$$

The switch intervals are divided into these four, where S_x denotes which switches are on

$$\begin{aligned} Int_1 &: 0 \le t \le \frac{DT_s}{2}(S_1, S_2, S_3, S_4) \\ Int_2 &: \frac{DT_s}{2} \le t \le \frac{T_s}{2}(S_1, S_4) \\ Int_3 &: \frac{T_s}{2} \le t \le \frac{(1+D)T_s}{2}(S_1, S_2, S_3, S_4) \\ Int_4 &: \frac{(1+D)T_s}{2} \le t \le T_s(S_2, S_3) \end{aligned} \tag{1.26}$$

Small ripple approximations of interval 1 and 3:

$$\begin{aligned} v_L(t) &= \langle v_{PV}(t) \rangle_{Ts} - \langle i_L(t) \rangle_{Ts} \cdot R_{on} \\ i_C(t) &= -\frac{\langle v_{DC}(t) \rangle_{Ts}}{R_{DC}} \\ i_{PV}(t) &= \langle i_L(t) \rangle_{Ts} + C_{PV} \frac{d\langle v_{PV}(t) \rangle_{Ts}}{dt} \end{aligned} \tag{1.27}$$

Small ripple approximations of interval 2 and 4:

$$\begin{aligned} v_L(t) &= \langle v_{PV}(t) \rangle_{Ts} - \frac{\langle v_{DC}(t) \rangle_{Ts}}{n} - \langle i_L(t) \rangle_{Ts} \cdot 2R_{on} \\ i_C(t) &= \frac{\langle i_L(t) \rangle_{Ts}}{n} - \frac{\langle v_{DC}(t) \rangle_{Ts}}{R_{DC}} \\ i_{PV}(t) &= \langle i_L(t) \rangle_{Ts} + C_{PV} \frac{d\langle v_{PV}(t) \rangle_{Ts}}{dt} \end{aligned} \tag{1.28}$$

Averaging inductor voltage over one period:

$$
\begin{aligned}
L_{boost}\frac{d\langle i_L(t)\rangle}{dt} &= \langle v_L(t)\rangle_{Ts} = d(t)\left(\langle v_{PV}(t)\rangle_{Ts} - \langle i_L(t)\rangle_{Ts}\cdot R_{on}\right) \\
&\quad + d'(t)\left(\langle v_{PV}(t)\rangle_{Ts} - \frac{\langle v_{DC}(t)\rangle_{Ts}}{n} - \langle i_L(t)\rangle_{Ts}\cdot 2R_{on}\right) \\
&= d(t)\langle v_{PV}(t)\rangle_{Ts} - d(t)\langle i_L(t)\rangle_{Ts}\cdot R_{on} + d'(t)\langle v_{PV}(t)\rangle_{Ts} \\
&\quad - d'(t)\frac{\langle v_{DC}(t)\rangle_{Ts}}{n} - d'(t)\langle i_L(t)\rangle_{Ts}\cdot 2R_{on} \\
&= \langle v_{PV}(t)\rangle_{Ts}\left(d(t)+d'(t)\right) - \langle i_L(t)\rangle_{Ts}\cdot R_{on}\left(d(t)+2d'(t)\right) - d'(t)\frac{\langle v_{DC}(t)\rangle_{Ts}}{n} \\
&= \langle v_{PV}(t)\rangle_{Ts} - \langle i_L(t)\rangle_{Ts}\cdot R_{on}\left(1+d'(t)\right) - d'(t)\frac{\langle v_{DC}(t)\rangle_{Ts}}{n}
\end{aligned}
\tag{1.29}
$$

Averaging capacitor current over one period:

$$
\begin{aligned}
C_{DC}\frac{d\langle v_{DC}(t)\rangle}{dt} = \langle i_C(t)\rangle_{Ts} &= d(t)\left(-\frac{\langle v_{DC}(t)\rangle_{Ts}}{R_{DC}}\right) + d'(t)\left(\frac{\langle i_L(t)\rangle_{Ts}}{n} - \frac{\langle v_{DC}(t)\rangle_{Ts}}{R_{DC}}\right) \\
&= -d(t)\frac{\langle v_{DC}(t)\rangle_{Ts}}{R_{DC}} + d'(t)\frac{\langle i_L(t)\rangle_{Ts}}{n} - d'(t)\frac{\langle v_{DC}(t)\rangle_{Ts}}{R_{DC}} \\
&= -\frac{\langle v_{DC}(t)\rangle_{Ts}}{R_{DC}}\left(d(t)+d'(t)\right) + d'(t)\frac{\langle i_L(t)\rangle_{Ts}}{n} \\
&= -\frac{\langle v_{DC}(t)\rangle_{Ts}}{R_{DC}} + d'(t)\frac{\langle i_L(t)\rangle_{Ts}}{n}
\end{aligned}
\tag{1.30}
$$

Averaging input current over one period:

$$
\langle i_{PV}(t)\rangle_{Ts} = \langle i_L(t)\rangle_{Ts} + C_{PV}\frac{d\langle v_{PV}(t)\rangle_{Ts}}{dt}
\tag{1.31}
$$

1.2.13 Constructing small signal AC equations by perturbing and linearizing

The inputs:

$$
\begin{aligned}
&\langle v_{PV}(t)\rangle_{Ts} = V_{PV} + \hat{v}_{PV}(t) \\
&d(t) = D + \hat{d}(t) \\
&d'(t) = 1 - d(t) = 1 - (D + \hat{d}(t)) = D' - \hat{d}(t)
\end{aligned}
\tag{1.32}
$$

The response to the inputs:

$$\begin{aligned}\left\langle v_{DC}(t)\right\rangle_{Ts} &= V_{DC} + \hat{v}_{DC}(t)\\ \left\langle i_L(t)\right\rangle_{Ts} &= I_L + \hat{i}_L(t)\\ \left\langle i_{PV}(t)\right\rangle_{Ts} &= I_{PV} + \hat{i}_{PV}(t)\end{aligned} \tag{1.33}$$

The averaged inductor equation

Large signal averaged inductor equation:

$$\begin{aligned}L_{boost}\frac{d\left(I_L + \hat{i}_L(t)\right)}{dt} = \left(V_{PV} + \hat{v}_{PV}(t)\right) - \left(I_L + \hat{i}_L(t)\right)\cdot R_{on}\left(1 + D' - \hat{d}(t)\right)\\ -\left(D' - \hat{d}(t)\right)\frac{\left(V_{DC} + \hat{v}_{DC}(t)\right)}{n}\end{aligned} \tag{1.34}$$

Multiplying out and collecting terms (DC terms, 1st and 2nd order terms):

$$\begin{aligned}L_{boost}\left(\frac{dI_L}{dt} + \frac{d\hat{i}_L(t)}{dt}\right) = \left(V_{PV} - I_L R_{on}\left(1 + D'\right) - D'\frac{V_{DC}}{n}\right)\\ +\left(\hat{v}_{PV}(t) + I_L R_{on}\hat{d}(t) - \hat{i}_L(t)R_{on}\left(1 + D'\right) - D'\frac{\hat{v}_{DC}(t)}{n} + \hat{d}(t)\frac{V_{DC}}{n}\right)\\ +\left(\hat{i}_L(t)\hat{d}(t) + \hat{d}(t)\frac{\hat{v}_{DC}(t)}{n}\right)\end{aligned} \tag{1.35}$$

Assuming the second order terms are much smaller in magnitude then the first-order terms, and the DC-terms must equal zero, the small-signal AC equation becomes:

$$L_{boost}\frac{d\hat{i}_L(t)}{dt} = \hat{v}_{PV}(t) - \frac{D'}{n}\hat{v}_{DC}(t) + \left(I_L R_{on} + \frac{V_{DC}}{n}\right)\hat{d}(t) - R_{on}\left(1 + D\right)\hat{i}_L(t) \tag{1.36}$$

The equation for the quiescent value (DC-terms):

$$0 = V_{PV} - R_{on}\left(1 + D'\right)I_L - \frac{D'}{n}V_{DC} \tag{1.37}$$

The averaged capacitor equation

Large signal averaged capacitor equation:

$$C_{DC}\frac{d\left(V_{DC}+\hat{v}_{DC}(t)\right)}{dt}=-\frac{\left(V_{DC}+\hat{v}_{DC}(t)\right)}{R_{DC}}+\left(D'-\hat{d}(t)\right)\frac{\left(I_L+\hat{i}_L(t)\right)}{n} \tag{1.38}$$

Multiplying out and collecting terms (DC terms, 1st and 2nd order terms):

$$C_{DC}\left(\frac{dV_{DC}}{dt}+\frac{d\hat{v}_{DC}(t)}{dt}\right)=\left(D'\frac{I_L}{n}-\frac{V_{DC}}{R_{DC}}\right)+\left(D'\frac{\hat{i}_L(t)}{n}-\hat{d}(t)\frac{I_L}{n}-\frac{\hat{v}_{DC}(t)}{R_{DC}}\right)+\left(-\hat{d}(t)\frac{\hat{i}_L(t)}{n}\right) \tag{1.39}$$

Assuming the second order terms are much smaller in magnitude then the first-order terms, and the DC-terms must equal zero, the small-signal AC equation becomes

$$C_{DC}\frac{d\hat{v}_{DC}(t)}{dt}=\frac{D'}{n}\hat{i}_L(t)-\frac{I_L}{n}\hat{d}(t)-\frac{1}{R_{DC}}\hat{v}_{DC}(t) \tag{1.40}$$

The equation for the quiescent value (DC-terms):

$$0=\frac{D'}{n}I_L-\frac{1}{R_{DC}}V_{DC} \tag{1.41}$$

The averaged input current equation

Large signal averaged capacitor equation:

$$\left(I_{PV}+\hat{i}_{PV}(t)\right)=\left(I_L+\hat{i}_L(t)\right)+C_{PV}\frac{d\left(V_{PV}+\hat{v}_{PV}(t)\right)}{dt} \tag{1.42}$$

The DC terms must be equal in size and therefore the small-signal AC equation becomes

$$\hat{i}_{PV}(t)=\hat{i}_L(t)+C_{PV}\frac{d\hat{v}_{PV}(t)}{dt} \tag{1.43}$$

The equation for the quiescent value (DC-terms):

$$I_{PV}=I_L \tag{1.44}$$

The equivalent circuit based on the averaged inductor, capacitor and input current equations.

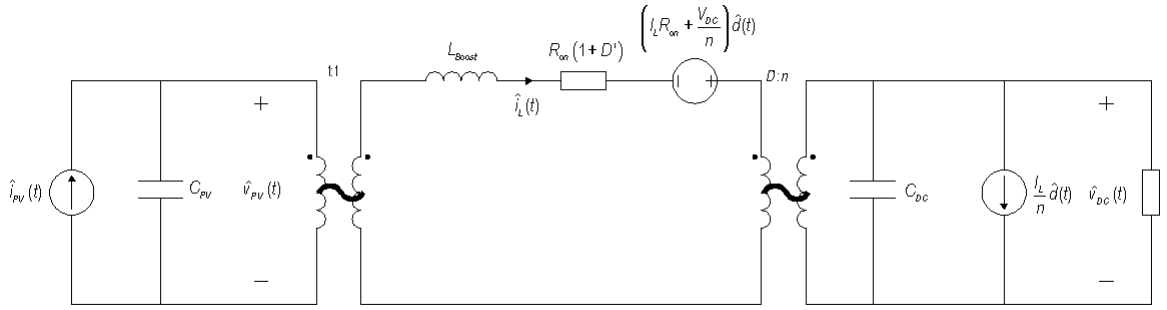

Figure 1.4: Equivalent circuit to the small signal AC equations

The first transformer has a ratio of 1:1, and can therefore be removed, a simplified circuit without the transformer is shown in the figure below.

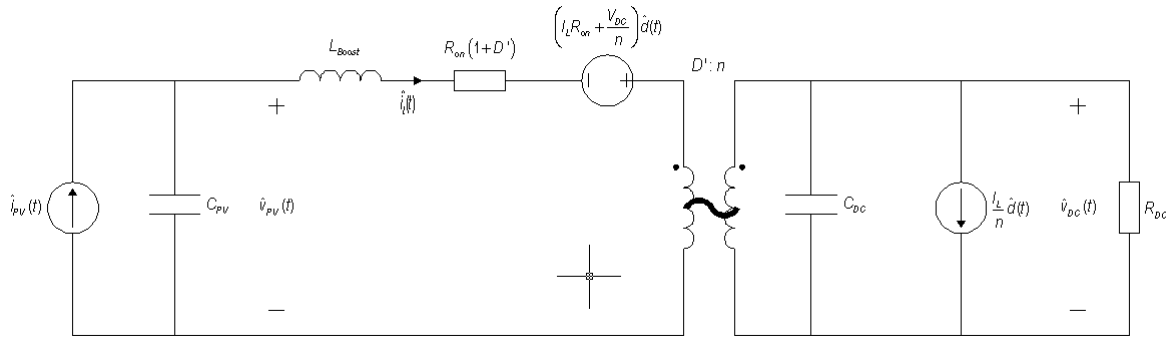

Figure 1.5: Simplified equivalent circuit to the small signal AC equations

1.2.14 State equations:

$$
\begin{aligned}
C_{PV}\frac{d\hat{v}_{PV}(t)}{dt} &= -\hat{i}_L(t) + \hat{i}_{PV}(t) \\
L_{boost}\frac{d\hat{i}_L(t)}{dt} &= \hat{v}_{PV}(t) - R_{on}(1+D)\hat{i}_L(t) - \frac{D'}{n}\hat{v}_{DC}(t) + \left(I_L R_{on} + \frac{V_{DC}}{n}\right)\hat{d}(t) \\
C_{DC}\frac{d\hat{v}_{DC}(t)}{dt} &= \frac{D'}{n}\hat{i}_L(t) - \frac{1}{R_{DC}}\hat{v}_{DC}(t) - \frac{I_L}{n}\hat{d}(t)
\end{aligned}
\tag{1.45}
$$

1.2.15 State-space equations in matrix form

$$\begin{bmatrix} C_{PV} & 0 & 0 \\ 0 & L_{boost} & 0 \\ 0 & 0 & C_{DC} \end{bmatrix} \begin{bmatrix} \frac{d\hat{v}_{DC}(t)}{dt} \\ \frac{d\hat{i}_L(t)}{dt} \\ \frac{d\hat{v}_{DC}(t)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -1 & 0 \\ 1 & -R_{on}(1+D) & -\frac{D'}{n} \\ 0 & \frac{D'}{n} & -\frac{1}{R_{DC}} \end{bmatrix} \begin{bmatrix} \hat{v}_{PV}(t) \\ \hat{i}_L(t) \\ \hat{v}_{DC}(t) \end{bmatrix}$$
$$+ \begin{bmatrix} 1 \\ 0 \\ 0 \end{bmatrix} \left[\hat{i}_{PV}(t) \right] + \left(\begin{bmatrix} 0 & 0 & 0 \\ 0 & R_{on} & \frac{1}{n} \\ 0 & -\frac{1}{n} & 0 \end{bmatrix} \begin{bmatrix} V_{PV} \\ I_L \\ V_{DC} \end{bmatrix} \right) \hat{d}(t) \tag{1.46}$$

1.3 State-Space Averaging

The state equations in matrix form (bold letters denotes matrixes).

$$\begin{aligned} \mathbf{K}\frac{d\mathbf{x}(t)}{dt} &= \mathbf{A}\mathbf{x}(t) + \mathbf{B}\mathbf{u}(t) \\ \mathbf{y}(t) &= \mathbf{C}\mathbf{x}(t) + \mathbf{E}\mathbf{u}(t) \end{aligned} \tag{1.47}$$

The state, input and output vectors are listed below.

$$\begin{aligned} \mathbf{x}(t) &= \begin{bmatrix} v_{PV}(t) \\ i_L(t) \\ v_{DC}(t) \end{bmatrix} \\ \mathbf{u}(t) &= \left[i_{PV}(t) \right] \\ \mathbf{y}(t) &= \left[v_{DC}(t) \right] \end{aligned} \tag{1.48}$$

1.3.16 Linear system equations interval 1 and 3

State equations:

$$\begin{aligned} C_{PV}\frac{dv_{PV}}{dt} &= -i_L(t) + i_{PV}(t) \\ L_{boost}\frac{di_L(t)}{dt} &= v_{PV}(t) - R_{on}i_L(t) \\ C_{DC}\frac{dv_{DC}(t)}{dt} &= -\frac{1}{R_{DC}}v_{DC}(t) \end{aligned} \tag{1.49}$$

Output equations:

$$v_{DC}(t) = \frac{R_{DC}}{n} i_L(t) \tag{1.50}$$

The constants of proportionality matrices for these intervals:

$$\mathbf{A_1} = \begin{bmatrix} 0 & -1 & 0 \\ 1 & -R_{on} & 0 \\ 0 & 0 & -\frac{1}{R_{DC}} \end{bmatrix}$$
$$\mathbf{B_1} = \begin{bmatrix} 1 \\ 0 \\ 0 \end{bmatrix}$$
$$\mathbf{C_1} = \begin{bmatrix} 0 & \frac{R_{DC}}{n} & 0 \end{bmatrix}$$
$$\mathbf{E_1} = [0] \tag{1.51}$$

1.3.17 Linear system equations interval 2 and 4

State equations:

$$C_{PV} \frac{dv_{PV}}{dt} = -i_L(t) + i_{PV}(t)$$
$$L_{boost} \frac{di_L(t)}{dt} = v_{PV}(t) - 2R_{on} i_L(t) - \frac{1}{n} v_{DC}(t)$$
$$C_{DC} \frac{dv_{DC}(t)}{dt} = \frac{1}{n} i_L(t) - \frac{1}{R_{DC}} v_{DC}(t) \tag{1.52}$$

Output equations:

$$v_{DC}(t) = \frac{R_{DC}}{n} i_L(t) \tag{1.53}$$

The constants of proportionality matrices for these intervals:

$$\mathbf{A}_2 = \begin{bmatrix} 0 & -1 & 0 \\ 1 & -2R_{on} & -\frac{1}{n} \\ 0 & \frac{1}{n} & -\frac{1}{R_{DC}} \end{bmatrix}$$
$$\mathbf{B}_2 = \begin{bmatrix} 1 \\ 0 \\ 0 \end{bmatrix}$$
$$\mathbf{C}_2 = \begin{bmatrix} 0 & \frac{R_{DC}}{n} & 0 \end{bmatrix}$$
$$\mathbf{E}_2 = [0] \tag{1.54}$$

1.3.18 Averaged matrices for the constants of proportionality

$$\mathbf{A} = D\mathbf{A}_1 + D'\mathbf{A}_2 = D\begin{bmatrix} 0 & -1 & 0 \\ 1 & -R_{on} & 0 \\ 0 & 0 & -\frac{1}{R_{DC}} \end{bmatrix} + D'\begin{bmatrix} 0 & -1 & 0 \\ 1 & -2R_{on} & -\frac{1}{n} \\ 0 & \frac{1}{n} & -\frac{1}{R_{DC}} \end{bmatrix}$$
$$= \begin{bmatrix} 0 & -1 & 0 \\ 1 & -\left(DR_{on} + D'2R_{on}\right) & -D'\frac{1}{n} \\ 0 & D'\frac{1}{n} & -\frac{1}{R_{DC}} \end{bmatrix}$$
$$\mathbf{B} = D\mathbf{B}_1 + D'\mathbf{B}_2 = D\begin{bmatrix} 1 \\ 0 \\ 0 \end{bmatrix} + D'\begin{bmatrix} 1 \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} 1 \\ 0 \\ 0 \end{bmatrix}$$
$$\mathbf{C} = D\mathbf{C}_1 + D'\mathbf{C}_2 = D\begin{bmatrix} 0 & \frac{R_{DC}}{n} & 0 \end{bmatrix} + D'\begin{bmatrix} 0 & \frac{R_{DC}}{n} & 0 \end{bmatrix} = \begin{bmatrix} 0 & \frac{R_{DC}}{n} & 0 \end{bmatrix}$$
$$\mathbf{E} = D\mathbf{E}_1 + D'\mathbf{E}_2 = D[0] + D'[0] = [0]$$
$$\mathbf{K} = \begin{bmatrix} C_{PV} & 0 & 0 \\ 0 & L_{boost} & 0 \\ 0 & 0 & C_{DC} \end{bmatrix} \tag{1.55}$$

1.3.19 The equilibrium vectors

$$\begin{aligned}\mathbf{X} &= -\mathbf{A}^{-1}\mathbf{B}\mathbf{U} \\ \mathbf{Y} &= \left(-\mathbf{C}\mathbf{A}^{-1}\mathbf{B}+\mathbf{E}\right)\mathbf{U}\end{aligned} \tag{1.56}$$

$$\begin{aligned}\begin{bmatrix} V_{PV} \\ I_{PV} \\ V_{DC} \end{bmatrix} &= \begin{bmatrix} -\dfrac{\mathrm{R}_{on}n^2D+2R_{on}n^2D'+D'^2R_{DC}}{n^2} \\ -1 \\ -\dfrac{D'R_{DC}}{n} \end{bmatrix}\begin{bmatrix} I_{PV} \end{bmatrix} \\ \begin{bmatrix} V_{DC} \end{bmatrix} &= \begin{bmatrix} -\dfrac{R_{DC}}{n} \end{bmatrix}\begin{bmatrix} I_{PV} \end{bmatrix}\end{aligned} \tag{1.57}$$

1.3.20 State equations of small signal AC model

The state, input and output vectors:

$$\begin{aligned}\hat{\mathbf{x}}(t) &= \begin{bmatrix} \hat{v}_{PV}(t) \\ \hat{i}_{L}(t) \\ \hat{v}_{DC}(t) \end{bmatrix} \\ \hat{\mathbf{u}}(t) &= \begin{bmatrix} \hat{i}_{PV}(t) \end{bmatrix} \\ \hat{\mathbf{y}}(t) &= \begin{bmatrix} \hat{v}_{DC}(t) \end{bmatrix}\end{aligned} \tag{1.58}$$

State and output equations on matrix form:

$$\begin{aligned}\mathbf{K}\frac{d\hat{x}(t)}{dt} &= \mathbf{A}\hat{x}(t)+\mathbf{B}\hat{u}(t)+\left[\left(\mathbf{A}_1-\mathbf{A}_2\right)\mathbf{X}+\left(\mathbf{B}_1-\mathbf{B}_2\right)\mathbf{U}\right]\hat{d}(t) \\ \hat{y}(t) &= \mathbf{C}\hat{x}(t)+\mathbf{E}\hat{u}(t)+\left[\left(\mathbf{C}_1-\mathbf{C}_2\right)\mathbf{X}+\left(\mathbf{E}_1-\mathbf{E}_2\right)\mathbf{U}\right]\hat{d}(t)\end{aligned} \tag{1.59}$$

$$\mathbf{A_1}-\mathbf{A_2}=\begin{bmatrix}0 & -1 & 0\\ 1 & -R_{on} & 0\\ 0 & 0 & -\dfrac{1}{R_{DC}}\end{bmatrix}-\begin{bmatrix}0 & -1 & 0\\ 1 & -2R_{on} & -\dfrac{1}{n}\\ 0 & \dfrac{1}{n} & -\dfrac{1}{R_{DC}}\end{bmatrix}=\begin{bmatrix}0 & 0 & 0\\ 0 & R_{on} & \dfrac{1}{n}\\ 0 & -\dfrac{1}{n} & 0\end{bmatrix}$$

$$\mathbf{B_1}-\mathbf{B_2}=\begin{bmatrix}1\\0\\0\end{bmatrix}-\begin{bmatrix}1\\0\\0\end{bmatrix}=\begin{bmatrix}0\\0\\0\end{bmatrix}$$

$$\mathbf{C_1}-\mathbf{C_2}=\begin{bmatrix}0 & \dfrac{R_{DC}}{n} & 0\end{bmatrix}-\begin{bmatrix}0 & \dfrac{R_{DC}}{n} & 0\end{bmatrix}=\begin{bmatrix}0 & 0 & 0\end{bmatrix}$$

$$\mathbf{E_1}-\mathbf{E_2}=[0]-[0]=[0] \qquad (1.60)$$

The state equations:

$$\begin{bmatrix}C_{PV} & 0 & 0\\ 0 & L_{boost} & 0\\ 0 & 0 & C_{DC}\end{bmatrix}\cdot\begin{bmatrix}\dfrac{d\hat{v}_{PV}(t)}{dt}\\ \dfrac{d\hat{i}_L(t)}{dt}\\ \dfrac{d\hat{v}_{DC}(t)}{dt}\end{bmatrix}=\begin{bmatrix}0 & -1 & 0\\ 1 & -R_{on}(1+D') & -\dfrac{D'}{n}\\ 0 & \dfrac{D'}{n} & -\dfrac{1}{R_{DC}}\end{bmatrix}\cdot\begin{bmatrix}\hat{v}_{PV}(t)\\ \hat{i}_L(t)\\ \hat{v}_{DC}(t)\end{bmatrix}$$

$$+\begin{bmatrix}1\\0\\0\end{bmatrix}\cdot\left[\hat{i}_{PV}(t)\right]+\left(\begin{bmatrix}0 & 0 & 0\\ 0 & R_{on} & \dfrac{1}{n}\\ 0 & -\dfrac{1}{n} & 0\end{bmatrix}\begin{bmatrix}V_{PV}\\ I_{PV}\\ V_{DC}\end{bmatrix}\right)\hat{d}(t) \qquad (1.61)$$

The output equation:

$$\left[\hat{v}_{DC}(t)\right]=\begin{bmatrix}0 & \dfrac{R_{DC}}{n} & 0\end{bmatrix}\cdot\begin{bmatrix}\hat{v}_{PV}(t)\\ \hat{i}_L(t)\\ \hat{v}_{DC}(t)\end{bmatrix} \qquad (1.62)$$

The state equations of (1.61) is equal that derived in (1.46), so it should be correct. The output equation is controlled by inspection, and is correct.

1.4 Transfer function of DC-DC converter

Finding the Laplace transformed of the differential equations in (1.45).

$$sC_{PV}\hat{v}_{PV}(s) = -\hat{i}_L(s) + \hat{i}_{PV}(s) \tag{1.63}$$

$$sL_{boost}\hat{i}_L(s) = \hat{v}_{PV}(s) - R_{on}\left(1+D'\right)\hat{i}_L(s) - \frac{D'}{n}\hat{v}_{DC}(s) + \left(I_L R_{on} + \frac{V_{DC}}{n}\right)\hat{d}(s) \tag{1.64}$$

$$sC_{DC}\hat{v}_{DC}(s) = \frac{D'}{n}\hat{i}_L(s) - \frac{1}{R_{DC}}\hat{v}_{DC}(s) - \frac{I_L}{n}\hat{d}(s) \tag{1.65}$$

The photovoltaic voltage:

$$\hat{v}_{PV}(s) = \frac{1}{sC_{PV}}\left(-\hat{i}_L(s) + \hat{i}_{PV}(s)\right) \tag{1.66}$$

Solving (1.63),(1.64) and (1.65) for the DC-link voltage gives these transfer functions

$$\begin{aligned} H_1(s) &= \frac{\hat{v}_{DC}(s)}{\hat{d}(s)} = K_1 \frac{s^2 - s\dfrac{D'V_{DC} - nR_{ON}I_L}{nL_{Boost}I_L} + \dfrac{1}{L_{Boost}C_{PV}}}{s^3 + s^2G_2 + sG_1 + G_0} \\ H_2(s) &= \frac{\hat{v}_{DC}(s)}{\hat{i}_{PV}(s)} = K_2 \frac{1}{s^3 + s^2G_2 + sG_1 + G_0} \end{aligned} \tag{1.67}$$

Doing the same for the $\overline{\text{PV-voltage}}$

$$\begin{aligned} H_3(s) &= \frac{\hat{v}_{PV}(s)}{\hat{d}(s)} = K_3 \frac{s - \dfrac{nV_{DC} + n^2R_{ON}I_L - D'R_{DC}I_L}{nC_{DC}R_{DC}\left(V_{DC} + nR_{ON}I_L\right)}}{s^3 + s^2G_2 + sG_1 + G_0} \\ H_4(s) &= \frac{\hat{v}_{PV}(s)}{\hat{i}_{PV}(s)} = K_4 \frac{s^2 + s\dfrac{L_{Boost} + C_{DC}R_{DC}R_{ON} + D'C_{DC}R_{DC}R_{ON}}{L_{Boost}C_{DC}R_{DC}} + \dfrac{D'^2R_{DC} + n^2R_{ON} + n^2D'R_{ON}}{n^2L_{Boost}C_{DC}R_{DC}}}{s^3 + s^2G_2 + sG_1 + G_0} \end{aligned} \tag{1.68}$$

and the inductor current

$$\begin{aligned} H_5(s) &= \frac{\hat{i}_L(s)}{\hat{d}(s)} = K_5 \frac{s^2 + s\dfrac{n\left(nV_{DC} + n^2R_{ON}I_L + D'R_{DC}I_L\right)}{C_{DC}R_{DC}\left(V_{DC} + nR_{ON}I_L\right)}}{s^3 + s^2G_2 + sG_1 + G_0} \\ H_6(s) &= \frac{\hat{i}_L(s)}{\hat{i}_{PV}(s)} = K_6 \frac{s + \dfrac{1}{C_{DC}R_{DC}}}{s^3 + s^2G_2 + sG_1 + G_0} \end{aligned} \tag{1.69}$$

Where the constants are defined as

$$G_2 = \frac{L_{Boost} + C_{DC}R_{ON}R_{DC} + D'C_{DC}R_{ON}R_{DC}}{L_{Boost}C_{DC}R_{DC}}$$
$$G_1 = \frac{D'^2 C_{PV}R_{DC} + n^2C_{DC}R_{DC} + n^2D'C_{PV}R_{ON} + n^2C_{PV}R_{ON}}{n^2L_{Boost}C_{PV}C_{DC}R_{DC}}$$
$$G_0 = \frac{1}{L_{Boost}C_{PV}C_{DC}R_{DC}} \tag{1.70}$$

and

$$K_1 = -\frac{I_L}{nC_{DC}}$$
$$K_2 = \frac{D'}{nL_{Boost}C_{PV}C_{DC}}$$
$$K_3 = -\frac{V_{DC} + nR_{ON}I_L}{nL_{Boost}C_{PV}}$$
$$K_4 = \frac{1}{C_{PV}}$$
$$K_5 = \frac{V_{DC} + nR_{ON}I_L}{nL_{Boost}}$$
$$K_6 = \frac{1}{L_{Boost}C_{PV}} \tag{1.71}$$

2 LCL FILTER

A figure of the filter is shown in the figure below

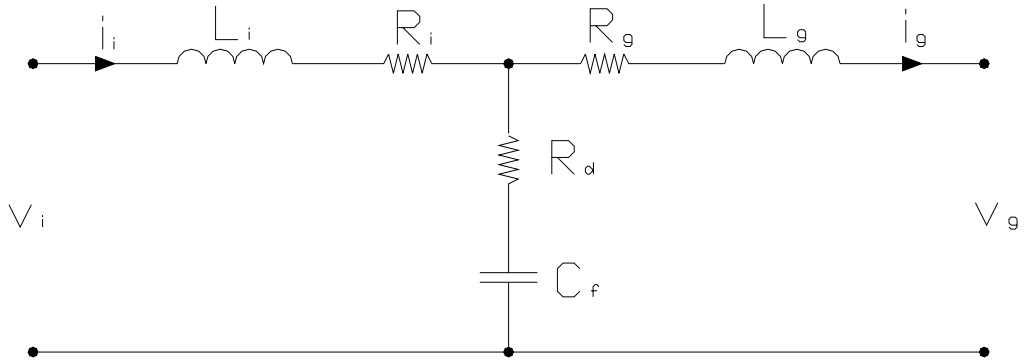

Figure 2.1: LCL filter model

2.1 Differential equations

The differential functions of the LCL filter, which is valid in the stationary abc and αβ reference frame is

$$\begin{aligned}
\frac{di_i(t)}{dt} &= \frac{1}{L_i}\left(v_i(t) - v_c(t) - R_d\left(i_i(t) - i_g(t)\right) - R_i i_i(t)\right) \\
\frac{di_g(t)}{dt} &= \frac{1}{L_g}\left(v_c(t) - v_g(t) + R_d\left(i_i(t) - i_g(t)\right) - R_g i_g(t)\right) \\
\frac{dv_c(t)}{dt} &= \frac{1}{C_f}\left(i_i(t) - i_g(t)\right)
\end{aligned} \tag{2.1}$$

There are no cross couplings between the phases, and thus the equations are equal for all phases. If expressed in matrix form they become.

$$\begin{bmatrix} \frac{di_i(t)}{dt} \\ \frac{di_g(t)}{dt} \\ \frac{dv_c(t)}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{R_i + R_d}{L_i} & \frac{R_d}{L_i} & -\frac{1}{L_i} \\ \frac{R_d}{L_g} & -\frac{R_g + R_d}{L_g} & \frac{1}{L_g} \\ \frac{1}{C_f} & -\frac{1}{C_f} & 0 \end{bmatrix} \begin{bmatrix} i_i(t) \\ i_g(t) \\ v_c(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L_i} & 0 \\ 0 & -\frac{1}{L_g} \\ 0 & 0 \end{bmatrix} \begin{bmatrix} v_i(t) \\ v_g(t) \end{bmatrix} \tag{2.2}$$

This can be transformed into the dq-system by inserting the inverse transformation of the dq currents as shown in equation (2.3) (where X is the current or voltage of interest) into (2.2)

$$X_\alpha = X_d \cos\theta - X_q \sin\theta$$
$$X_\beta = X_d \sin\theta + X_q \cos\theta \tag{2.3}$$

The solving of these equations can be quite tedious if solved by hand, but by using a program like maple, it becomes rather simple. Solving for the dq currents gives the expression in (2.4).

$$\begin{bmatrix} \frac{di_{id}(t)}{dt} \\ \frac{di_{iq}(t)}{dt} \\ \frac{di_{gd}(t)}{dt} \\ \frac{di_{gq}(t)}{dt} \\ \frac{dv_{cd}(t)}{dt} \\ \frac{dv_{cq}(t)}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{R_i+R_d}{L_i} & \omega & \frac{R_d}{L_i} & 0 & -\frac{1}{L_i} & 0 \\ -\omega & -\frac{R_i+R_d}{L_i} & 0 & \frac{R_d}{L_i} & 0 & -\frac{1}{L_i} \\ \frac{R_d}{L_g} & 0 & -\frac{R_g+R_d}{L_g} & \omega & \frac{1}{L_g} & 0 \\ 0 & \frac{R_d}{L_g} & -\omega & -\frac{R_g+R_d}{L_g} & 0 & \frac{1}{L_g} \\ \frac{1}{C_f} & 0 & -\frac{1}{C_f} & 0 & 0 & \omega \\ 0 & \frac{1}{C_f} & 0 & -\frac{1}{C_f} & -\omega & 0 \end{bmatrix} \begin{bmatrix} i_{id}(t) \\ i_{iq}(t) \\ i_{gd}(t) \\ i_{gq}(t) \\ v_{cd}(t) \\ v_{cq}(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L_i} & 0 & 0 & 0 \\ 0 & \frac{1}{L_i} & 0 & 0 \\ 0 & 0 & -\frac{1}{L_g} & 0 \\ 0 & 0 & 0 & -\frac{1}{L_g} \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} v_{id}(t) \\ v_{iq}(t) \\ v_{gd}(t) \\ v_{gq}(t) \end{bmatrix}$$

(2.4)

2.2 Transfer functions

Transfer functions are derived based on the three phase differential equations derived in the previous chapter, but in these equations the inductor resistance is not considered.

$$i_i(s) = \frac{1}{sL_i}\left(-R_d i_i(s) + R_d i_g(s) - v_c(s) + v_i(s)\right)$$
$$i_g(s) = \frac{1}{sL_g}\left(R_d i_i(s) - R_d i_g(s) + v_c(s) - v_g(s)\right)$$
$$v_c(s) = \frac{1}{sC_f}\left(i_i(s) - i_g(s)\right) \tag{2.5}$$

Solving the equations.

$$
\begin{aligned}
i_i(s) &= \frac{s^2 L_g C_f + s C_f R_d + 1}{s\left(s^2 L_i L_g C_f + s\left(L_i C_f R_d + L_g C_f R_d\right) + \left(L_g + L_i\right)\right)} v_i(s) \\
&\quad - \frac{s C_f R_d + 1}{s\left(s^2 L_i L_g C_f + s\left(L_i C_f R_d + L_g C_f R_d\right) + \left(L_g + L_i\right)\right)} v_g(s) \\
i_g(s) &= \frac{s C_f R_d + 1}{s\left(s^2 L_i L_g C_f + s\left(L_i C_f R_d + L_g C_f R_d\right) + \left(L_g + L_i\right)\right)} v_i(s) \\
&\quad - \frac{s^2 L_i C_f + s C_f R_d + 1}{s\left(s^2 L_i L_g C_f + s\left(L_i C_f R_d + L_g C_f R_d\right) + \left(L_g + L_i\right)\right)} v_g(s) \\
v_c(s) &= \frac{L_g}{s^2 L_i L_g C_f + s\left(L_i C_f R_d + L_g C_f R_d\right) + \left(L_g + L_i\right)} v_i(s) \\
&\quad + \frac{L_i}{s^2 L_i L_g C_f + s\left(L_i C_f R_d + L_g C_f R_d\right) + \left(L_g + L_i\right)} v_g(s)
\end{aligned}
\tag{2.6}
$$

Defining the resonant frequency

$$
\omega_{res}^2 = \frac{1}{C_f}\left(\frac{1}{L_i} + \frac{1}{L_g}\right) \tag{2.7}
$$

and the impedances

$$
z_{LC}^2 = \frac{1}{L_g C_f} \quad \text{and} \quad z_{LCg}^2 = \frac{1}{L_i C_f} \tag{2.8}
$$

Inserting the definition of the resonant frequency into the solutions

$$
\begin{aligned}
i_i(s) &= \frac{1}{s L_i L_g C_f} \frac{s^2 L_g C_f + s C_f R_d + 1}{\left(s^2 + s R_d C_f \omega_{res}^2 + \omega_{res}^2\right)} v_i(s) - \frac{1}{s L_i L_g C_f} \frac{s C_f R_d + 1}{\left(s^2 + s R_d C_f \omega_{res}^2 + \omega_{res}^2\right)} v_g(s) \\
i_g(s) &= \frac{1}{s L_i L_g C_f} \frac{s C_f R_d + 1}{\left(s^2 + s R_d C_f \omega_{res}^2 + \omega_{res}^2\right)} v_i(s) - \frac{1}{s L_i L_g C_f} \frac{s^2 L_i C_f + s C_f R_d + 1}{\left(s^2 + s R_d C_f \omega_{res}^2 + \omega_{res}^2\right)} v_g(s) \\
v_c(s) &= \frac{1}{L_i L_g C_f} \frac{L_g}{\left(s^2 + s R_d C_f \omega_{res}^2 + \omega_{res}^2\right)} v_i(s) - \frac{1}{L_i L_g C_f} \frac{L_i}{\left(s^2 + s R_d C_f \omega_{res}^2 + \omega_{res}^2\right)} v_g(s)
\end{aligned}
\tag{2.9}
$$

The transfer functions of the damped system.

$$
\begin{aligned}
H_{iivi} &= \frac{i_i(s)}{v_i(s)} = \frac{1}{sL_i}\frac{s^2 + sC_fR_dz_{LC}^2 + z_{LC}^2}{\left(s^2 + sR_dC_f\omega_{res}^2 + \omega_{res}^2\right)} \\
H_{iivg} &= \frac{i_i(s)}{v_g(s)} = \frac{1}{sL_i}\frac{sC_fR_dz_{LC}^2 + z_{LC}^2}{\left(s^2 + sR_dC_f\omega_{res}^2 + \omega_{res}^2\right)} \\
H_{igvi} &= \frac{i_g(s)}{v_i(s)} = \frac{1}{sL_i}\frac{sC_fR_dz_{LC}^2 + z_{LC}^2}{\left(s^2 + sR_dC_f\omega_{res}^2 + \omega_{res}^2\right)} \\
H_{igvg} &= \frac{i_g(s)}{v_g(s)} = \frac{1}{sL_g}\frac{s^2 + sC_fR_dz_{LCg}^2 + z_{LCg}^2}{\left(s^2 + sR_dC_f\omega_{res}^2 + \omega_{res}^2\right)} \\
H_{vcvi} &= \frac{v_c(s)}{v_i(s)} = \frac{z_{LCg}^2}{\left(s^2 + sR_dC_f\omega_{res}^2 + \omega_{res}^2\right)} \\
H_{vcvg} &= \frac{v_c(s)}{v_g(s)} = \frac{z_{LC}^2}{\left(s^2 + sR_dC_f\omega_{res}^2 + \omega_{res}^2\right)}
\end{aligned}
\tag{2.10}
$$

By considering the inverter as a harmonic generator at high frequencies, and the grid as a short circuit, the converter voltage harmonic at the switching frequency becomes $v_i(h_{sw}) \neq 0$, and the grid voltage harmonic at the switching frequency becomes $v_g(h_{sw}) \neq 0$. With these assumptions the current equations becomes

$$
\begin{aligned}
i_i(h_{sw}) &= \frac{1}{sL_i}\frac{s^2 + sC_fR_dz_{LC}^2 + z_{LC}^2}{\left(s^2 + sR_dC_f\omega_{res}^2 + \omega_{res}^2\right)}v_i(h_{sw}) \\
i_g(h_{sw}) &= \frac{1}{sL_i}\frac{sC_fR_dz_{LC}^2 + z_{LC}^2}{\left(s^2 + sR_dC_f\omega_{res}^2 + \omega_{res}^2\right)}v_i(h_{sw})
\end{aligned}
\tag{2.11}
$$

The transfer function between the inverter side and grid side current at switching frequency becomes

$$
\begin{aligned}
v_i(h_{sw}) &= \frac{sL_i\left(s^2 + sR_dC_f\omega_{res}^2 + \omega_{res}^2\right)}{s^2 + sC_fR_dz_{LC}^2 + z_{LC}^2}i_i(h_{sw}) \\
i_g(h_{sw}) &= \frac{1}{sL_i}\frac{sC_fR_dz_{LC}^2 + z_{LC}^2}{\left(s^2 + sR_dC_f\omega_{res}^2 + \omega_{res}^2\right)}v_i(h_{sw}) = \frac{1}{sL_i}\frac{sC_fR_dz_{LC}^2 + z_{LC}^2}{\left(s^2 + sR_dC_f\omega_{res}^2 + \omega_{res}^2\right)}\frac{sL_i\left(s^2 + sR_dC_f\omega_{res}^2 + \omega_{res}^2\right)}{s^2 + sC_fR_dz_{LC}^2 + z_{LC}^2}i_i(h_{sw}) \\
\frac{i_g(h_{sw})}{i_i(h_{sw})} &= \frac{sC_fR_dz_{LC}^2 + z_{LC}^2}{s^2 + sC_fR_dz_{LC}^2 + z_{LC}^2}
\end{aligned}
\tag{2.12}
$$

Transfer functions of the undamped system.

$$
\begin{aligned}
H_{iivi} &= \frac{i_i(s)}{v_i(s)} = \frac{1}{sL_i}\frac{s^2 + z_{LC}^2}{\left(s^2 + \omega_{res}^2\right)} \\
H_{iivg} &= \frac{i_i(s)}{v_g(s)} = \frac{1}{sL_i}\frac{z_{LC}^2}{\left(s^2 + \omega_{res}^2\right)} \\
H_{igvi} &= \frac{i_g(s)}{v_i(s)} = \frac{1}{sL_i}\frac{z_{LC}^2}{\left(s^2 + \omega_{res}^2\right)} \\
H_{igvg} &= \frac{i_g(s)}{v_g(s)} = \frac{1}{sL_g}\frac{s^2 + z_{LCg}^2}{\left(s^2 + \omega_{res}^2\right)} \\
H_{vcvi} &= \frac{v_c(s)}{v_i(s)} = \frac{z_{LCg}^2}{\left(s^2 + \omega_{res}^2\right)} \\
H_{vcvg} &= \frac{v_c(s)}{v_g(s)} = \frac{z_{LC}^2}{\left(s^2 + \omega_{res}^2\right)}
\end{aligned}
\tag{2.13}
$$

With the same assumptions as for the damped system the transfer function between the inverter side current and the grid side current at switching frequency becomes.

$$
\frac{i_g(h_{sw})}{i_i(h_{sw})} = \frac{z_{LC}^2}{s^2 + z_{LC}^2} \tag{2.14}
$$

3 SYSTEM RATING

A multi-string converter with full bridge boost converters on the input, and a three-phase full bridge inverter on the output is to be used. The converters will be dimensioned to be used on the solar panels at NTNU, and should be able to connect to a 400V grid. Each string will have its own full bridge boost converter, and the DC-DC converter will therefore be dimensioned for one string only. The DC-AC inverter on the other hand, must be dimensioned to withstand the power delivered from all the strings.

3.1 Description of solar panels at NTNU

The solar panels at NTNU are mounted on the southern wall of electro building b, and cover 192m^2. They are integrated in a 455m^2 double glass facade mounted on the outside of the buildings existing cladding. The solar modules are delivered from BP Solar, and the modules consist of series of 60 or 90 monocrystalline silicone cells from Saturn Technology. These modules are arranged in strings with four 90 cell modules and one 60 cell module, with a total peak power of 14.56kW.

Electrical data for one PV string

Open circuit voltage V_{OC_STC}	300V
Short circuit current I_{SC_STC}	5A
Maximum power P_{MAX_STC}	910W
Voltage at maximum power V_{MAX_STC}	210V
Current at maximum power I_{MAX_STC}	4.3A

All data is given at STC (Standard Test Condition), with irradiance of 1 kW/m^2, air mass (AM) of 1.5, and a cell temperature of 25ºC.

3.2 DC-DC converter

In this chapter the DC-DC converter will be rated, and most of the calculations made here are based on equations derived in appendix 1.1.

3.2.1 Switching

The switching scheme of this converter is shown in the DCDC converter appendix, and to reduce the size of the magnetic components the DC-DC converter will be switched at a high frequency. A switching frequency of $f_S = 50kHz$ will be used, and therefore mosfets will be a natural choice of switches.

3.2.2 Voltage rating

The inverter will be connected to a three-phase 400V grid, and this will therefore be the rated output voltage of the full bridge inverter, that is V_{LL} = 400V. Based on this the needed DC-link voltage can be calculated. To achieve the maximum output voltage without overmodulation, the inverter must run at approximately unity modulation ratio, that is m_a = 1. Once the modulation ratio is known, then the DC-link voltage can be calculated based on the maximum voltage with space vector modulation, given in equation (3.9) in the master thesis.

$$V_{DC} = \sqrt{2}V_{LL} = \sqrt{2} \cdot 400 = 565V$$

This is the minimum voltage on the DC-link, but because there will be a voltage drop across the LCL filter the voltage is sat to 600V. Based on the DC-link voltage and the PV panel voltage, the transformer winding ratio and the DC-DC converter can be dimensioned. The input voltage is a function of the temperature, and the input voltage range of one string can be calculated by using equation (2.1) from the master thesis. Assuming the temperature of the cells can vary from $-30°C$ to $60°C$, and the number of cells in series per string is $n_c = 1 \cdot 60 + 4 \cdot 90 = 420$, the open circuit voltage range is:

$$\begin{aligned} V_{OC\_max} &= -2.3 \cdot 10^{-3} \cdot n_c \cdot (T_{min} - T_{STC}) + V_{OC\_STC} \\ &= -2.3 \cdot 10^{-3} \cdot 420 \cdot (-30 - 25) + 300 \\ &= 353V \end{aligned}$$

$$\begin{aligned} V_{OC\_min} &= -2.3 \cdot 10^{-3} \cdot n_c \cdot (T_{max} - T_{STC}) + V_{OC\_STC} \\ &= -2.3 \cdot 10^{-3} \cdot 420 \cdot (60 - 25) + 300 \\ &= 266V \end{aligned}$$

This is the maximum and minimum voltages at open circuit, and the converter should be able to handle the maximum open circuit voltage even though it is not the normal operating voltage at MPP. So the maximum operating voltage of the DC-DC converter becomes:

$$V_{PV\_max} = V_{OC\_max} = 353V$$

Since the converter will be working at the MPP voltage, which is lower then the open circuit voltage, the minimum voltage the DC-DC converter must handle will be lower then V_{OC_min}. By finding the MPP voltage at max temperature, and a voltage 10% below this value will give an approximation of the lowest allowable operating voltage. The minimum operating voltage of the DC-DC converter is then:

$$V_{PV\_\min} = \frac{V_{MAX\_STC}}{V_{OC\_STC}} \cdot V_{OC\_MIN} \cdot 0.9 = \frac{210}{300} \cdot 266 \cdot 0.9 = 168V$$

Should the voltage be above or below these values, the converter must cease to energize the DC-link.

3.2.3 Current rating

Since the converter will operate in continuous conduction mode (CCM), a lower current limit must be set, which also will become the limit between continuous and discontinuous conduction mode (DCM). It is desired to have a large operating range of the converter, and thus a low limit, but at the same time it is desired to keep the boost inductor as small as possible, and thus a higher limit. So a minimum input current limit of 10% of I_{SC} is therefore used, and the maximum input current is equal the short circuit current of the PV panels. Giving an operating range of:

$$0.5A \le I_{PV} \le 5.0A$$

The lower limit equals the limit between CCM and DCM, I_{LB}.

3.2.4 Transformer ratio

To be able to use mosfets in the DC-DC converter the voltage over the switches must be kept at an acceptable level. The highest voltage over the switches will be equal to the primary voltage of the transformer, and is therefore a direct function of the winding ratio and the DC-link voltage. A 500V mosfet is assumed used, and there should be some safety margins, so the primary voltage of the transformer should never exceed 400V. Based on this the transformer ratio becomes:

$$n = \frac{V_{DC}}{V_P} = \frac{565}{400} = 1.4$$

3.2.5 Duty cycle limits

Based on the previous calculations, the duty cycle limits becomes

$$D_{\max} = 1 - \frac{V_{PV\_\min} \cdot n}{V_{DC}} = 1 - \frac{168 \cdot 1.4}{565} = 0.58$$

$$D_{\min} = 1 - \frac{V_{PV\_\max} \cdot n}{V_{DC}} = 1 - \frac{353 \cdot 1.4}{600} = 0.17$$

3.2.6 Boost inductor

The inductance of the boost inductor is governed by the minimum current the circuit must deliver in CCM, the PV voltage and the DC-link voltage. This is shown in equation (1.14) in appendix 1.1, so the boost inductor becomes:

$$L_{boost} = V_{PV} \frac{V_{DC} - V_{PV} \cdot n}{4 I_{LB} V_{DC}} T_s \tag{3.1}$$

As seen from the equation, the only variable is the PV voltage. In the figure below the boost inductor is shown as a function of the PV voltage.

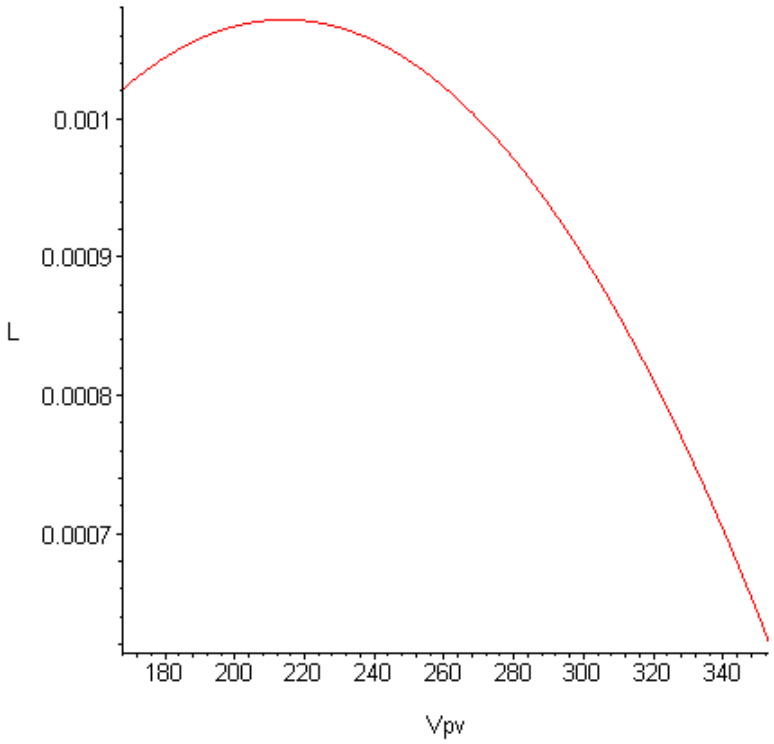

Figure 3.1: Boost inductor as function of the PV voltage

It can be shown that the maximum inductor appears at:

$$V_{PV\_\max L} = \frac{V_{DC}}{2n} \tag{3.2}$$

By inserting this into equation (3.1), the boost inductor needed is:

$$L_{boost} = \frac{V_{DC}}{16n \cdot I_{LB}} T_s = \frac{600}{16 \cdot 1.4 \cdot 0.5} \cdot 20 \cdot 10^{-6} = 1.1mH$$

3.2.7 PV Capacitor

The PV panel can be seen as a current source, and as mentioned in the master thesis, it is needful to convert it to a voltage source by adding a capacitor in parallel. In this way the capacitor will handle the ripple current from the boost inductor, smooth the current from the PV panel, and keep the PV panel voltage ripple at a minimum. The capacitor can be found as shown in appendix 1.1

$$C_{PV} = V_{PV} \frac{\left(1 - \frac{V_{PV} \cdot n}{V_{DC}}\right)^2}{8 L_{boost} \Delta V_{PV}} T_s^2 \tag{3.3}$$

Choosing a maximum voltage ripple of 0.1V, and plotting

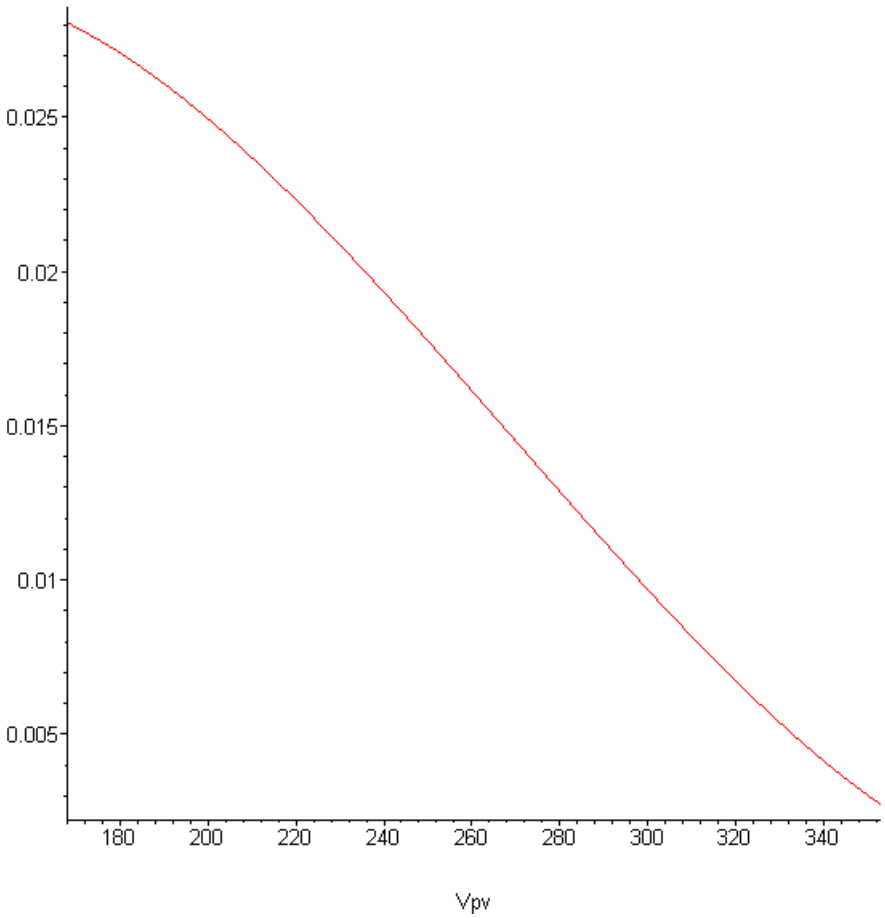

Figure 3.2: PV condensator as function of PV voltage

It can be seen from the plot that the capacitor needs to be highest at the lowest input voltage, and using equation (3.4) gives a capacitor value of approximately $30\mu F$. But if a electrolytic capacitor is to be used the maximum current ripple must also be considered. In appendix 1.1 an expression for the current ripple is derived

$$\Delta I_L = V_{PV} \frac{V_{DC} - V_{PV} \cdot n}{4 L_{boost} V_{DC}} T_s \tag{3.4}$$

Solving this equation for the highest current ripple, gives a maximum ripple of 0.50A, with an rms value of 0.29A.

3.2.8 DC Capacitor

The instantaneous power drawn from the DC-link is constant and equal the power drawn from the PV panels, as shown in figure 2.8 in the master thesis. Assuming the DC-link voltage is held constant, the current drawn from the DC-link is also constant, so therefore the capacitor must deliver all the current during switching intervals 1 and 3 (see appendix 1.1 for switching schemes). Based on this the capacitor size is in appendix 1.1 derived as

$$C_{DC} = \frac{I_{DC\_MAX}}{V_{DC}} \frac{\left(V_{DC} - V_{MAX\_STD} \cdot n\right) T_S}{2 \Delta V_{DC}} \tag{3.5}$$

At the maximum power, the DC current is 1.6A, and setting a maximum voltage ripple of 1V, the capacitor size becomes $C_{DC} = 7.7 \mu F$. If an electrolytic capacitor is to be used, then the current ripple must also be taken into consideration, and in this case the rms current ripple is the same as the maximum DC-link current.

3.2.9 Circuit design

Based on the calculations made in the previous chapters, the DC-DC converter has been designed. For the design of the circuit, the OrCad 10.5 program pack was used, where the circuit design was made in Capture CIS, and the PCB layout was done in Layout. A schematic of the circuit is shown in the figure 3.3, and the component specification can be found in table .3.1

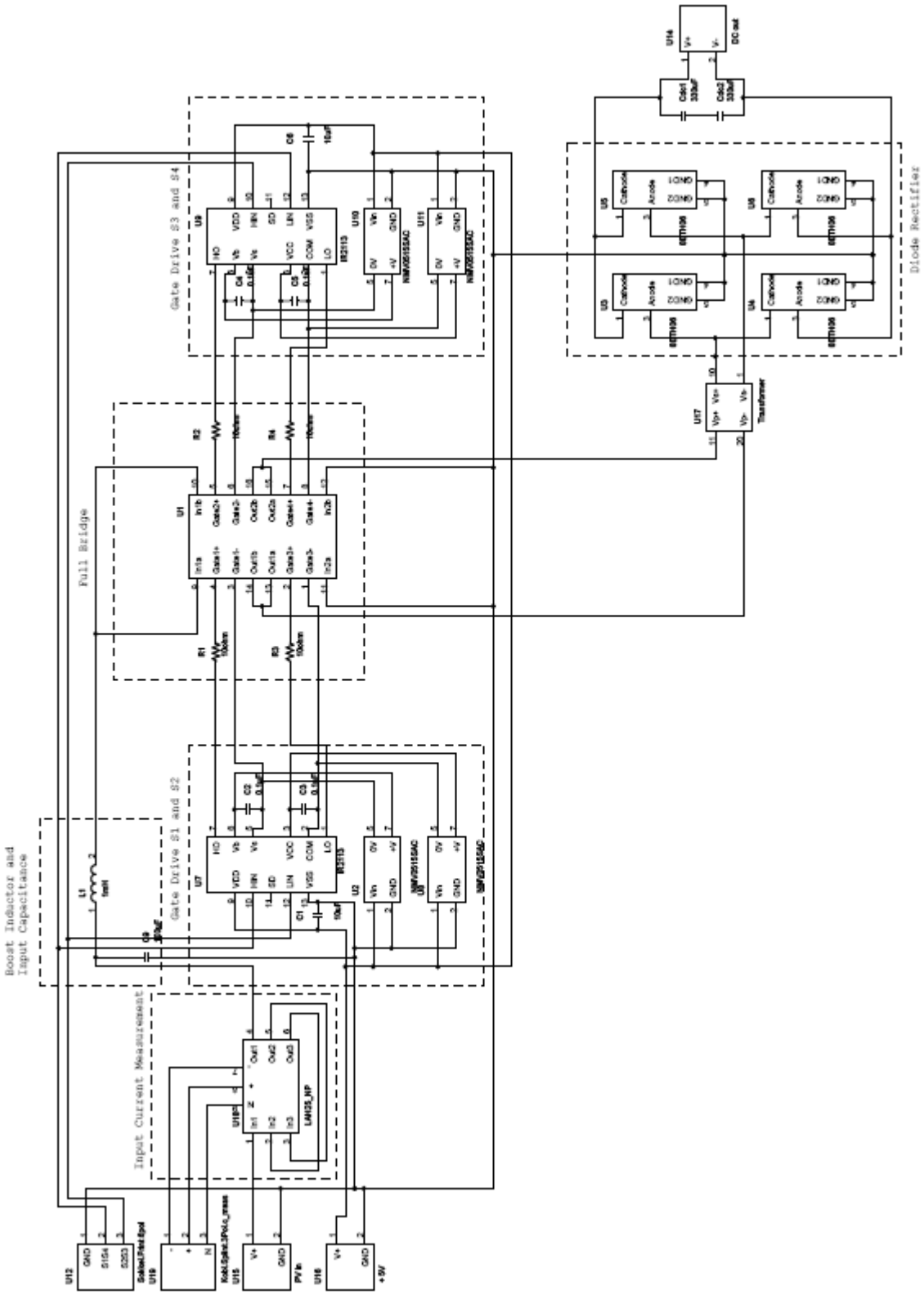

Figure 3.3: DC-DC converter schematics from OrCad Capture

Table 3.1 - Component list

Type	Brand	Description	Size	Count
19MT050XF	International Rectifier	Mosfet full bridge	500V	1
IR2113	International Rectifier	High and low side driver	2A	2
8ETH06	International Rectifier	High speed diode	600V, 18ns	4
ETD49/25/16	Ferroxcube	3F3 ferrite core		2
55109A2	Magnetics	Kool mu toroid	77110	1
FA-NR: 607418	Block	Litz wire	0.1mm2	
LAH 25-NP	LEM	Current transducer	25A	1
NMV0515SAC	Newport Components	Isolated DC-DC converter	1W	4
EETED2G331DA	Panasonic	Electrolyte capacitor	400VDC, 330uF	3
		Tantal condensator	0.1uF, 35V	4
		Tantal condensator	10uF, 16V	2
		Surface mounted resistor	10Ω	

A circuit board with standard copper layer thickness of 35µm is used, and the track width of the high power tracks is 5mm. According to [21], a track width of 5mm gives a 10° temperature rise at a current of 7A.

A boost inductor was built on the Kool mu toroid, and a high frequency transformer on the 3F3 ferrite core. The calculations is shown in appendix 4, and the leakage inductance of the buildt transformer is shown in the table below.

Table 3.2 - HF Transformer leakage inductance and resistance at 50kHz

Transformer	Leakage Inductance	Resistance
Litz wire - partitioned (S-P-S-P-S)	1.3µH	1.4Ω

Also some test points where added to the design, these are shown in the table below.

Table 3.3 - Test Points on DC-DC converter

Name	Description	Additional information
GND	Ground	
V_C	Input capacitor voltage and PV voltage	
V_i	Voltage boost inductor	
V_p	Primary voltage of transformer	
V_s	Secondary voltage of transformer	
V_{dc}	Voltage DC-link	
V_{g2}	Voltage gate 2	
V_{g4}	Voltage gate 4	
I_{g2}	Current gate 2	Voltage across gate resistance
I_{g4}	Current gate 4	Voltage across gate resistance

3.3 DC-AC inverter

3.3.1 Switching

To decrease the lower harmonic content, a high switching frequency will be applied, even though it reduces the effectivity of the inverter. It also reduces the size of the capacitive and inductive components connected to the inverter, and enables faster response of the controller. A switching frequency of 20kHz will be used.

3.3.2 Inverter specifications

An IGBT converter which is designed as a general building block for DC-DC converters, DC-AC converters and motor drives will be used. The converter is designed for laboratory use at NTNU SEfAS, and the converter rating is

Power	20kW
DC-Voltage:	0-650V
Switching frequency	0-25kHz, 0-100% pulse width modulation

The total peak power of all the solar panels at NTNU is 14.56kW, so the converter is oversized. Therefore no further calculations will be made in the DC-AC inverter.

3.4 LCL filter

The goal when designing an LCL filter is to reduce high-order harmonics on the grid side. But when designing the filter care must be shown, or the attenuation can become lower than expected, or it can even lead to a distortion increase because of oscillation effects. The inverter current harmonics can in fact cause saturation of the filter inductors or give filter resonance. So it is important to design the inductors correct considering current ripple, and the filter should be damped to avoid resonance. The LCL filter with damping resistor is shown in the figure below.

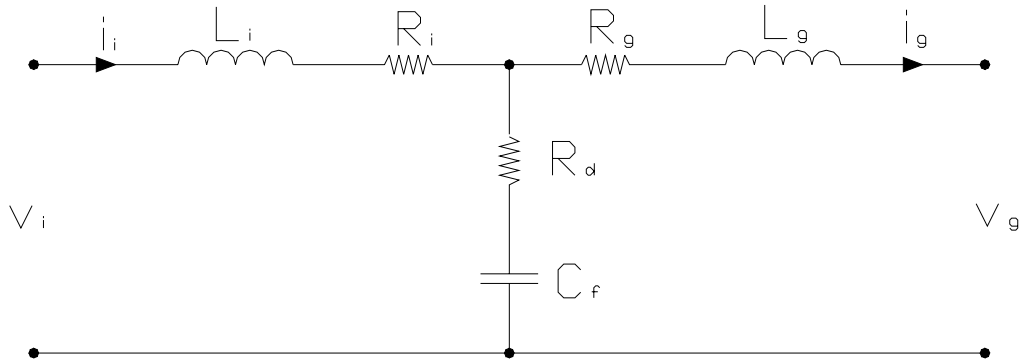

Figure 3.4: LCL filter with damping resistor

3.4.1 Design

The design is based on some of the design considerations given in [19,20], and the goal is to lower the current harmonics below the limits given by the standards. In [23] it is shown that the highest harmonic voltage occurs at $m_f \pm 2$ at unity modulation ratio, where

$$m_f = \frac{f_s}{f_g}$$

At these frequencies, the amplitude of the harmonic voltages is shown to be 0.32pu of the fundamental when using sinusoidal PWM. For space vector modulation, the harmonics will become different, but in order to find the amplitude of these harmonic voltages the PWM scheme should be simulated. In order to avoid simulating the SVM scheme, it is instead assumed that the harmonics with this scheme is the same as with sinusoidal PWM. This can be justified by the fact that the harmonics produced by SVM is lower than those produced by sinusoidal PWM, as stated in chapter 3.3.2 of the master thesis.

In table 2.3 of the master thesis the harmonic current limit is sat to 0.3% of the fundamental for harmonics above the 33rd, therefore the filter should be designed to reduce the harmonics around the switching frequency below this limit. Since the highest amplitude of the harmonics occur close to the switching frequency, it should be adequate to calculate the attenuation of the currents at the switching frequency, and design the filter according to this.

Base values

Base voltage, power, current and frequency.

$$E_n = V_g = 400V$$
$$P_n = P_{MAX\_STC} = 910W$$
$$I_g = \frac{P_n}{\sqrt{3}V_g} = 1.31A$$
$$\omega_n = 2\pi f_g = 2\pi 50 = 314\,{}^{rad}\!/_{s}$$

Base impedance and base capacitance

$$Z_b = \frac{E_n^2}{P_n} = \frac{400^2}{910} = 176\Omega$$
$$C_b = \frac{1}{\omega_n Z_b} = \frac{1}{314 \cdot 176} = 18\mu F$$

Inverter side inductor

The harmonic current at switching frequency should be limited to

$$I_{399} = 0.3\% \cdot I_g = 0.003 \cdot 1.31 = 3.93mA$$

The selection of an appropriate limit for the current harmonics through the converter side inductor, is a trade-off among inductor size, switching and conduction losses, and inductor coil and core losses (from [20]). Higher limits gives lower switching and conduction losses, but a larger inductor, resulting in larger coil and core losses. In this case a current limit of 20 times the limit at the output of the filter is used, giving an inductor size of

$$L_i = \frac{V_{399}}{399 \cdot \omega_n \cdot I_{399}} = \frac{0.32 \cdot 400}{\sqrt{3} \cdot 399 \cdot 314 \cdot 0.0039 \cdot 20} = 4.3mH$$

Capacitor

The maximum reactive power of the capacitor should be 5% of the rated power, this gives a maximum capacitor size of

$$Q_f = k_{pf} P_{rated} = 3\omega_g C_f V_{gf}^2$$
$$C_{f\_\max} = k_{pf} \frac{P_{rated}}{3\omega_g V_{gf}^2} = 0.05 \frac{910}{3 \cdot 314 \cdot 230^2} = 0.9\mu F$$

k_{pf}: percentage reactive power of rated power
V_{gf}: grid phase voltage

This demand is equal to $C_f \le 0.05 C_{base}$, and the largest standard size capacitor below this value is 0.68µF. Therefore this size will be used.

Grid side inductance

In a two level VSI the current harmonics is centred around the switching frequency and above, with the highest harmonic in the vicinity of the switching frequency. The ripple attenuation at switching frequency from the inverter current to the grid current, without considering the damping resistor, can be expressed as (see appendix 2.2 for derivation of this transfer function)

$$\left|H_{igii}(\omega_{sw})\right| = \left|\frac{i_g(\omega_{sw})}{i_i(\omega_{sw})}\right| = \frac{z_{LC}^2}{\sqrt{\left(z_{LC}^2 - \omega_{sw}^2\right)^2}} = \frac{\frac{1}{L_g C_f}}{\sqrt{\left(\frac{1}{L_g C_f} - \omega_{sw}^2\right)^2}} = \frac{1}{\sqrt{\left(L_g C_f \omega_{sw}^2 - 1\right)^2}} = k_a \quad (3.6)$$

k_a: current attenuation from i_{L1} to i_{L2}

In order to comply with the standards, the harmonic current at switching frequency has to be reduced to 5% of the inverter side current.

$$L_g = \frac{\sqrt{\frac{1}{k_a^2}} + 1}{C_f \omega_{sw}^2} = \frac{\sqrt{\frac{1}{0.05^2}} + 1}{0.68 \cdot 10^{-6} \cdot (2\pi \cdot 19950)^2} = 2mH$$

Total inductance value

The total inductance value should be less then 0.1pu to limit the AC-voltage drop during operation.

$$\frac{Z_{Lf}}{Z_b} = \frac{\omega_n (L_i + L_g)}{Z_b} = \frac{2\pi 50 (4.3 + 2) \cdot 10^{-3}}{176} = 0.011pu$$

Resonant frequency

The resonant frequency should be in the range of $10f_g \le f_{res} \le 0.5f_{sw} \Rightarrow 500Hz \le f_{res} \le 9975Hz$

$$f_{res} = \frac{1}{2\pi}\sqrt{\omega_{res}^2} = \frac{1}{2\pi}\sqrt{\frac{1}{C_f}\left(\frac{1}{L_i}+\frac{1}{L_g}\right)} = \frac{1}{2\pi}\sqrt{\frac{1}{0.68\cdot10^{-6}}\left(\frac{1}{4.3\cdot10^{-3}}+\frac{1}{2\cdot10^{-3}}\right)} = 5224\text{Hz}$$

Damping resistor

A large resistor gives effective damping, but it also tends to reduce the attenuation above the resonant frequency, and increase the losses. When using a resistor in series with the capacitor, the resistor size is often sat to one third of the capacitor impedance at resonant frequency.

$$X_{cf} = \frac{1}{\omega_{res}C_f} = \frac{1}{2\pi\cdot6762\cdot0.68\cdot10^{-6}} = 34.6\Omega$$

$$R_d = \frac{X_{cf}}{3} = \frac{34.6}{3} \approx 10\Omega$$

LCL filter specifications

In table 3.4 the filter specifications is summarized, and in table 3.5 the components used are listed, and the inductance values are measured using an RLC meter.

Table 3.4 - LCL filter specifications

Parameter	Value
Inverter side inductance L_i	4.3mH
Filter capacitance C_f	0.68µF
Grid side inductance L_g	2.0mH
Damping resistor R_d	10Ω
Resonance frequency f_{res}	5224Hz

Table 3.5 - Component list LCL-filter

Type	Brand	Description	#
Resistor		10Ω, 50W	3
Capacitor	Epcos	0.68µF	3

Table 3.5 - Component list LCL-filter

Type	Brand	Description	#
Inductor	Magnetics KoolMu	2.06mH, 1.1Ω(at 50Hz) 2.07mH, 2.2Ω(at 20kHz)	3
Inductor	Magnetics KoolMu	4.45mH, 1.8Ω(at 50Hz) 4.47mH, 3.9Ω(at 20kHz	3

4 MAGNETIC DESIGN

4.1 LCL Filter inductance

4.1.1 Specifications

The required specifications of the inductor is:

$$L_i = 4.3mH$$
$$L_g = 2.0mH$$
$$I_{DC} = I_{RMS} = \frac{P_{PV}}{V_{RMS}} = \frac{910}{400} = 2.3A$$
$$I_{DC\_bias} = 0A$$

A KoolMu core from Magnetics will be used, and in the design of the inductor a design procedure described in “Magnetics Powder Core Catalogue” (found at www.mag-inc.com) is used.

4.1.2 Design of converter side inductance

1. $LI_{DC}^{\ 2} = 4.3 \cdot 10^{-3} \cdot 2.3^2 = 22.7mHA^2$

2. From a Core Selector Chart a core with a permeability of 60µ and core number 77110 is found.

3. a) Calculating the number of turns
   Worst case:
   $$A_L = 75 \cdot 0.92 = 69 \, {mH}/{1000turns}$$
   $$N_{\min} = \sqrt{\frac{L_n \cdot 10^6}{A_L}} = \sqrt{\frac{4.3 \cdot 10^6}{69}} = 250turns$$
   b) The dc-bias
   No DC-bias
   c) Determine the rolloff in per unit from dc-bias curves
   No roll off
   d) Increasing the number of turns
   No increase in number of turns

4. Choosing wire size using a wire table
   $$J_L = 6 \, {A}/{mm^2}$$
   $$A_{CU} = 0.41mm^2$$

The skin depth at 20kHz is 0.53mm^2 (table 30-2 in [29]), and therefore an ordinary single conductor wire is adequate.

4.1.3 Design of grid side inductance

1. $LI_{DC}^{\ 2} = 2.0 \cdot 10^{-3} \cdot 2.3^2 = 10.6 mHA^2$

2. From a Core Selector Chart a core with a permeability of 60m and core number 77071 is found. Because 77110 is in stock this will be used instead.

3. a) Calculating the number of turns
   Worst case:

   $A_L = 75 \cdot 0.92 = 69 {}^{mH}\!/_{1000 turns}$

   $N_{\min} = \sqrt{\frac{L_n \cdot 10^6}{A_L}} = \sqrt{\frac{2.0 \cdot 10^6}{69}} = 170 turns$

   b) The dc-bias
   No DC-bias
   c) Determine the rolloff in per unit from dc-bias curves
   No roll off
   d) Increasing the number of turns
   No increase in number of turns

4. Choosing wire size using a wire table

   $J_L = 6 {}^{A}\!/_{mm^2}$

   $A_{CU} = 0.41 mm^2$

The skin depth at 20kHz is 0.53mm² (table 30-2 in [29]), and therefore an ordinary single conductor wire is adequate.

4.2 High frequency transformer

4.2.4 Specification

The design criteria of the transformer is.

$f_s = 50 kHz$

$n = 1.4$

$S = 910 W$

$$V_{pri} = \sqrt{\frac{2}{T_s}\int_0^{(1-D_{\min})T_s/2} \hat{V}_{pri}^{\ 2}\, dt} = \sqrt{\frac{2}{T_s}\left(\frac{\hat{V}_{pri}^{\ 2}(1-D_{\min})T_s}{2} - 0\right)} = \sqrt{\hat{V}_{pri}^{\ 2}(1-D\min)} = \sqrt{400^2(1-0.12)} = 375V$$

$$I_{pri} = \frac{S}{V_{pri}} = \frac{910}{375} = 2.4A$$

$k_{cu} = 0.3$ (litz wire)

4.2.5 Design

In the design of the transformer, a simplified calculation will be used. Losses in the transformer will be neglected, and instead the transformer will be made sufficiently large.

The core chosen is a Ferroxcube ETD 49/25/16 with these specifications:

$$A_{core} = 2.11cm^2$$
$$A_w = 3.1cm^2 \text{ (2.73 in datasheet)}$$
$$AP = 5.76cm^4$$
$$\hat{B} = 0.2T \text{ (at 50kHz)}$$

The number of turns needed is

$$N_p = \frac{\hat{V}_p}{2\pi f \cdot A_{core}\hat{B}} = \frac{400}{2\pi \cdot 50e3 \cdot 2.11e-4 \cdot 0.2} = 30turns$$
$$N_s = N_p \cdot n = 30 \cdot 1.4 = 42turns$$

In order to fill the window completely the optimal wire sizes becomes

$$A_{CUp} = \frac{k_{cu}A_W}{2N_p} = \frac{0.3 \cdot 273}{2 \cdot 37} = 1.1mm^2$$
$$A_{CUs} = \frac{k_{cu}A_W}{2N_s} = \frac{0.3 \cdot 273}{2 \cdot 60} = 0.68mm^2$$

Using a wire size of $A_{CU} = 0.94mm^2$ for both windings utilizes $226mm^2$ of the total window, and leaves some place for isolation. Estimating the maximum rating of the transformer

$$J_{rms} = \frac{2.4}{0.94} = 2.55 \, A/mm^2$$
$$S_{\max} = 2.22 \cdot k_{cu} \cdot f \cdot J_{rms} \cdot \hat{B} \cdot A_{core}A_w = 2.22 \cdot 0.3 \cdot 50e3 \cdot 2.55 \cdot 0.2 \cdot 6.54e-2 = 1.1kVA$$

The maximum rating of the transformer is larger than the rating of the PV panels, and should therefore be sufficiently large. It should also be noted that the PV panels almost never work at maximum rating, and therefore the transformer will normally have some capacity left.

Reduction of leakage inductance

In order to reduce the leakage inductance the windings has to be partitioned into multiple sections, and thus the leakage inductance is reduced. This arrangement also reduces the eddy current losses, but increases the interwinding capacitance and increases the amount of safety insulation between the sections. The increased amount of insulation is not a problem since the windings themselves does not fill the whole window. In the figure below the partitioning is shown.

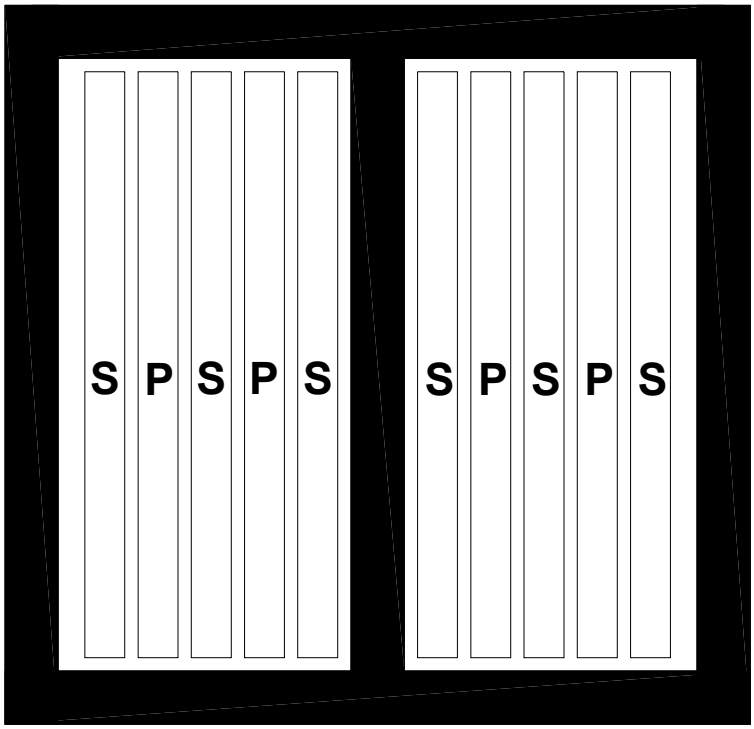

Figure 4.1: Partitioning of the transformer windings

4.3 High frequency boost inductor Design

4.3.6 Specification

The required specifications of the inductor is:

$$L_{Boost} = 1.02mH$$
$$I_{DC} = 4.3A$$
$$I_{DC\_bias} = 0.43A \text{ (at required inductance)}$$

4.3.7 Design

A KoolMu core from Magnetics will be used, and in the design of the inductor a design procedure described in "Magnetics Powder Core Catalogue" (found at www.mag-inc.com) is used.

1. $LI_{DC}{}^2 = 1.02 \cdot 10^{-3} \cdot 4.3^2 = 18.9 mHA^2$

2. From a Core Selector Chart a core with a permeability of 60μ and core number 77716 is found, one size larger is used (77110) to increase the number of turns per layer and thus reduce the capacitive coupling between input and output.

3. a) Calculating the number of turns
   Worst case:

   $$A_L = 75 \cdot 0.92 = 69 \, {}^{mH}\!/_{1000 turns}$$

   $$N_{\min} = \sqrt{\frac{L_n \cdot 10^6}{A_L}} = \sqrt{\frac{1.1 \cdot 10^6}{69}} = 126 turns$$

   b) The dc-bias:

   $$H = \frac{0.4\pi N I_{DC\_bias}}{l_e} = \frac{0.4\pi \cdot 126 \cdot 0.43}{14.3} = 4.8 oersteds$$

   c) Determine the rolloff in per unit from dc-bias curves
   Rolloff=0.97
   d) Increasing the number of turns

   $$N_{adj} = \frac{N_{\min}}{Rolloff} = \frac{126}{0.97} = 130 turns$$

4. Finding the wire size

$$J_L = 2 \, {}^{A}\!/_{mm^2}$$

$$A_{CU} = 2.0 mm^2$$

5 BRIEF DESCRIPTION OF CONVERTER SIMULATION

5.1 DC-AC Converter

The converter is simulated in simulink, and this appendix contains a brief description of how the simulation is made. The simulink model consists of three major blocks as shown in figure 5.1.1. These three blocks are described in the following chapters. All variables are defined in a m-file called constants.m, and from this file all process and controller variables can be changed. This file must be executed before the simulation is started.

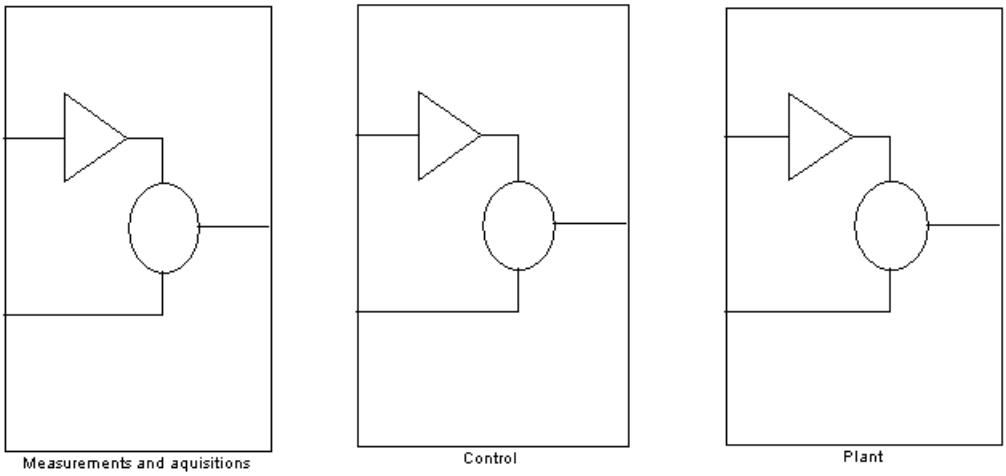

Figure 5.1: The three main blocks in the simulink model

This description of the model is very brief, but there is also added more detailed information in the model itself.

5.1.1 Measurements and Acquisitions

This block handles the measurements of the process variables. First the block filters the signals, and then it samples the filtered signals at the specified sampling interval T_s. The content of this block is shown in figure 5.2.

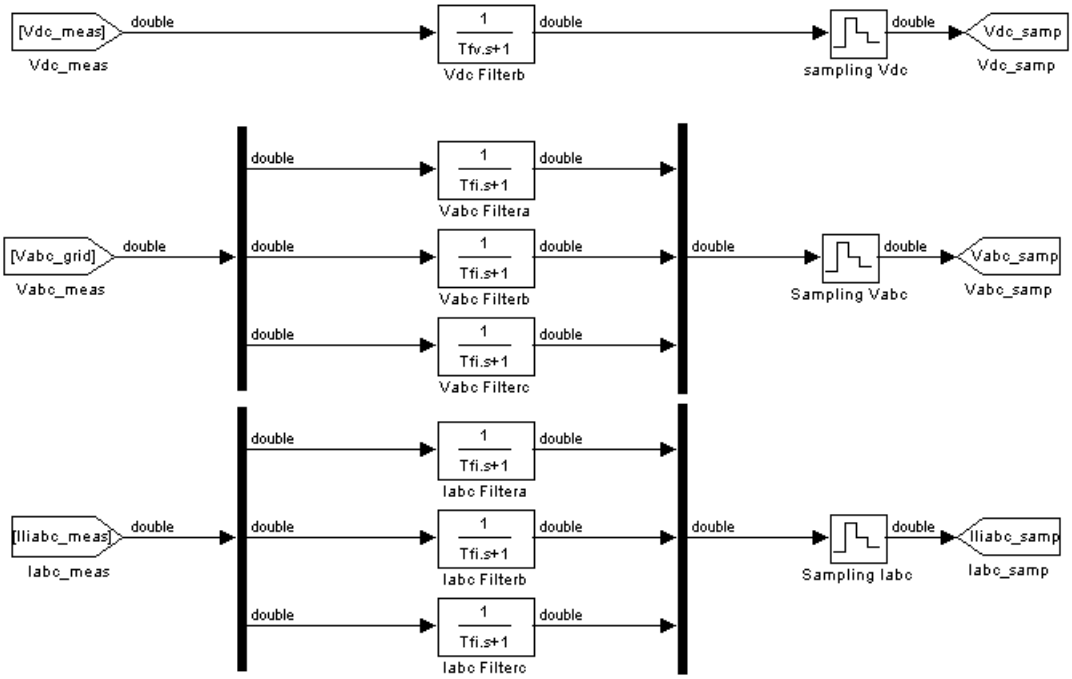

Figure 5.2: Content of measurement and acquisitions block

5.1.2 Control

In this block all transformations, phase synchronization and control of current and voltage is handled. Instead of using SVM, CB-PWM with third harmonic injection is used. They give equal output, but the carrier based is easier to implement in simulink.The content of this block is shown in figure 5.3

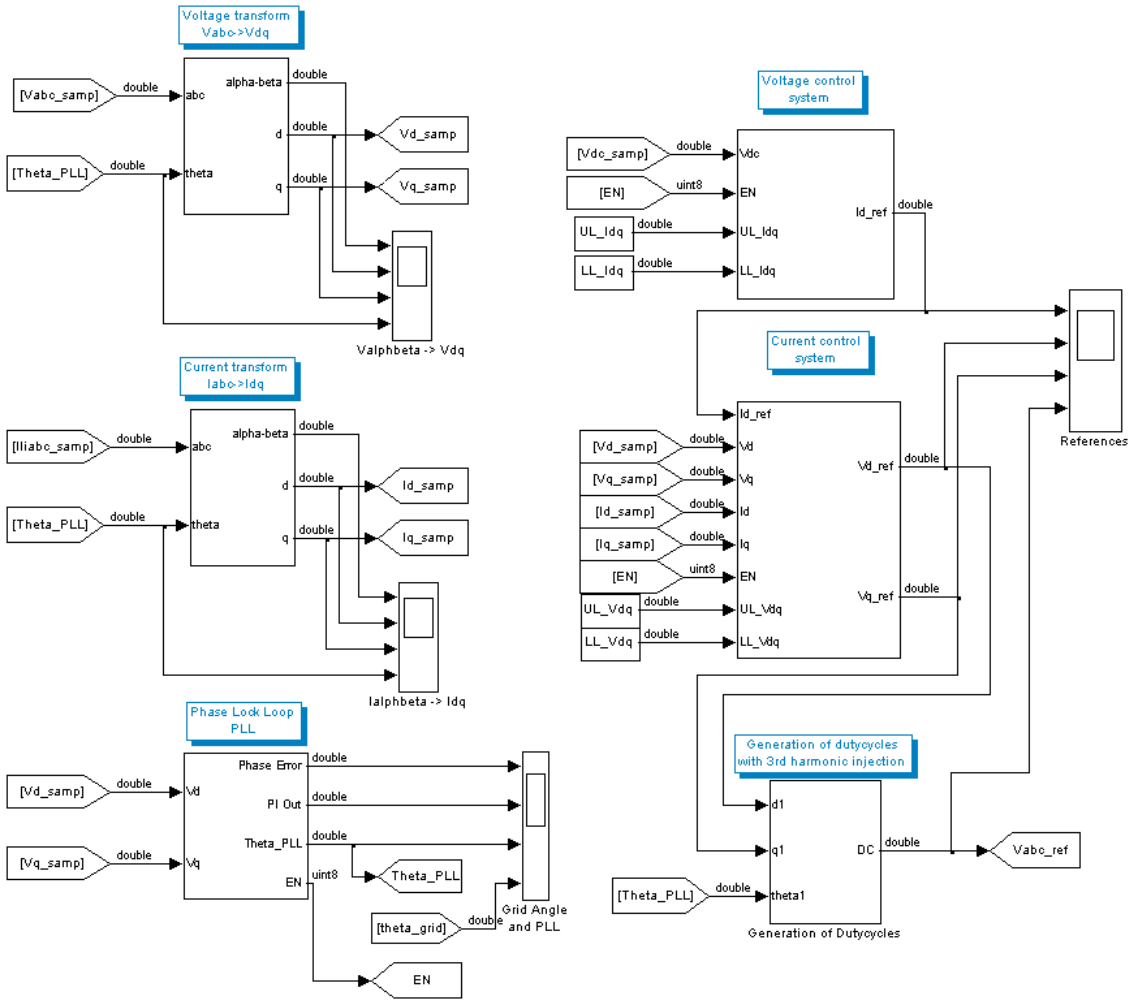

Figure 5.3: Content of control block

5.1.3 Plant

The last block is the plant block, and in this block all the physical processes are simulated. The content of this block is shown in figure 5.4. The grid voltage is in this model simulated as a pure sinusoidal three phase voltage, without any harmonics. It is possible to set the initial voltage angle, and to give the voltage a phase jump at a specified instant.

The DC-link is modelled as a capacitor with currents as input and the DC-link voltage as output. The current drawn from the DC-link is the d-axis current multiplied with a constant K_{DC}, which relates the d-axis current and the current from the DC-link. The source feeding the DC-link, is a source having similar current voltage characteristics as a solar panel.

The model of the inverter includes full PWM, and the switch signals are generated at a similar way as they are generated in a DSP. As an interface to the grid a model of the LCL filter is used.

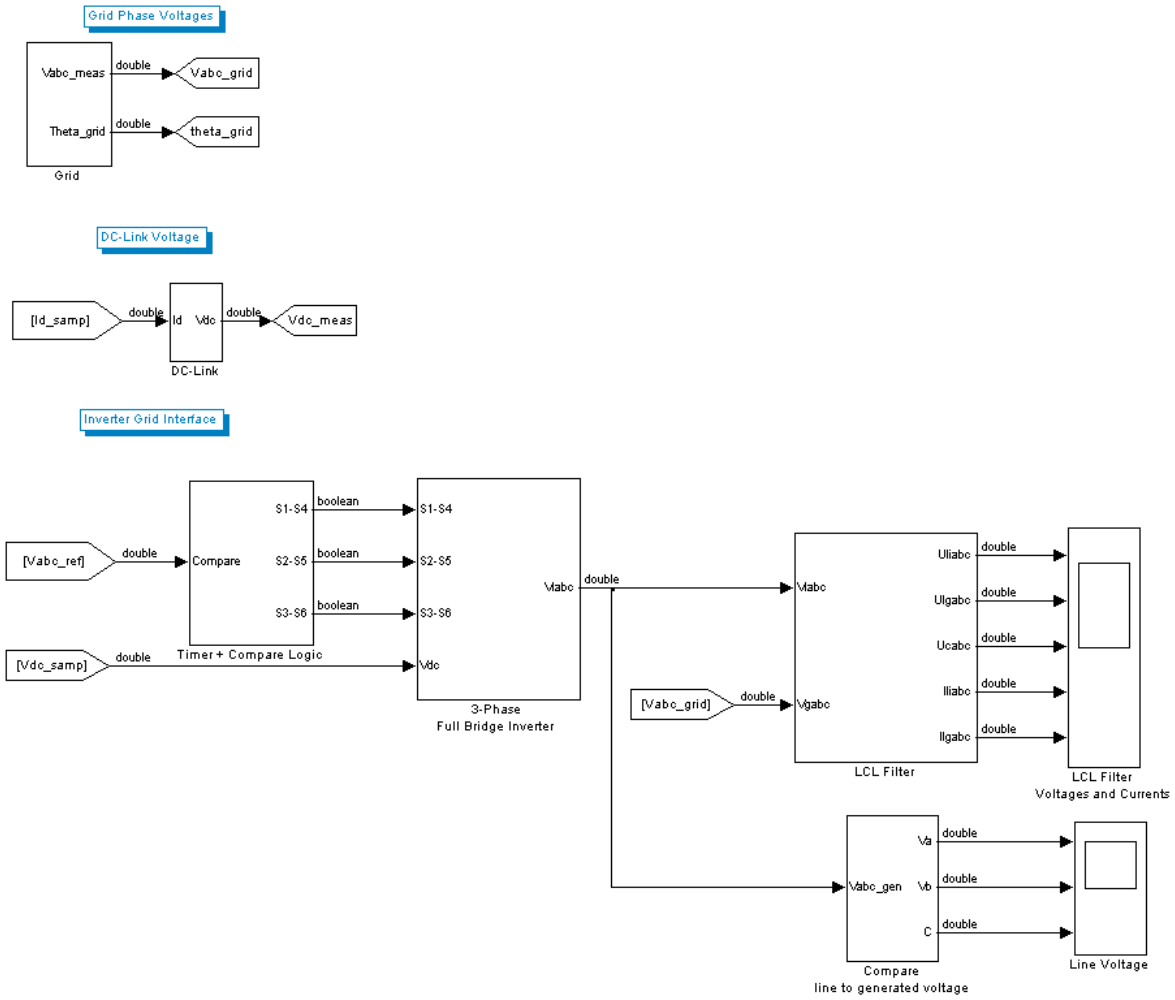

Figure 5.4: Content of plant block

5.2 DCDC Converter

The converter is simulated in simulink, and this appendix contains a brief description of how the simulation is made. The simulink model consists of four major blocks as shown in figure 5.5, which are described in the following chapters. All variables are defined in a m-file called DCDC_constants.m, and from this file all process and controller variables can be changed. This file must be executed before the simulation is started.

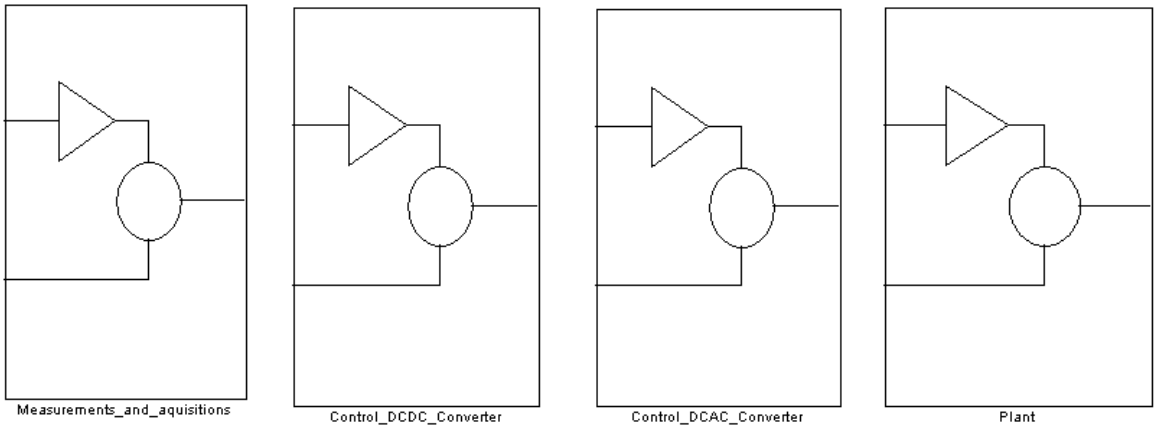

Figure 5.5: The four main blocks in the simulink model

This description of the model is very brief, but there is also added more detailed information in the model itself.

5.2.4 Measurements and Acquisitions

This block handles the measurements of the process variables. First the signals are filtered, then it samples the filtered signals at the specified sampling interval. The content of this block is shown in figure 5.6. The measurements made here corresponds to the measurements made in a real system.

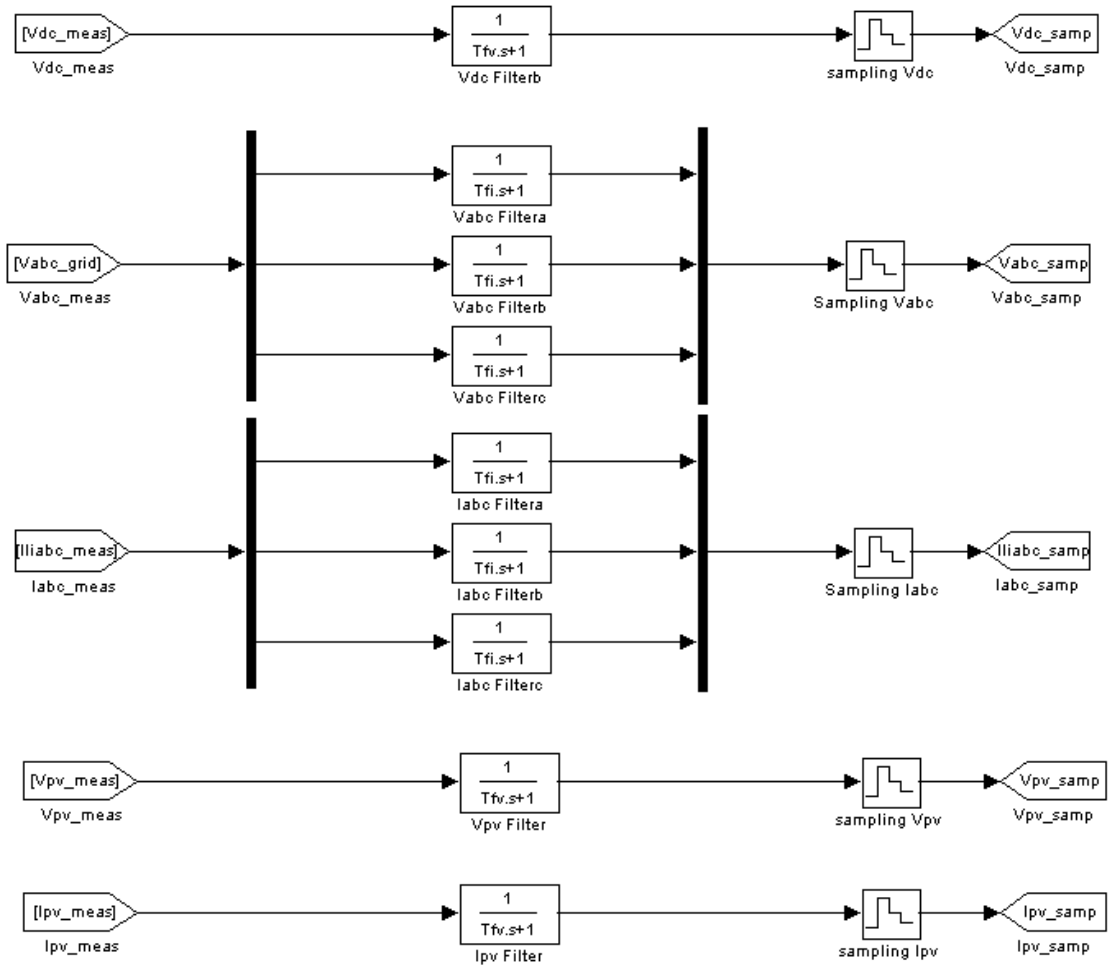

Figure 5.6: Content of measurement and acquisitions block

5.2.5 Control DC-AC Converter

This block is the same as the control block of the DCAC simulation, see chapter 5.1.2.

5.2.6 Control DC-DC Converter

The control of the DCDC converter is in this case only the MPP tracker. The MPPT is based on the P&O algorithm, and this algorithm is executed at a specified sampling interval.

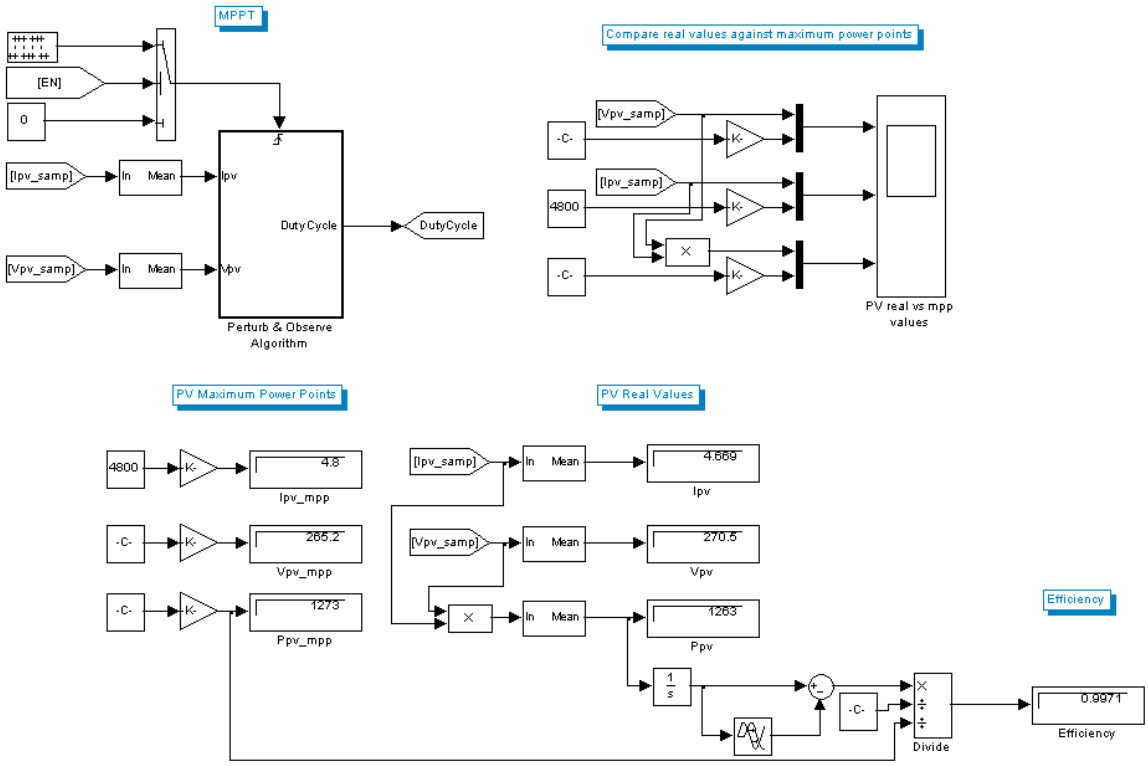

Figure 5.7: Content of Control_DCDC_Converter block

5.2.7 Plant

In this block all the physical processes are simulated. The content of this block is shown in figure 5.8

In the DCAC simulation a very simple model of the PV array was used, but in this model the full I-V characteristic, with a model of the DCDC converter is added. The I-V characteristic comes from the GUI “PV_Panel.fig”, and is transferred to and stored in the simulink model as a look up table.

The DCDC converter model is based on the small signal model derived in the preliminary project. This model is averaged across one switching interval, and this is considered an adequate approximation since the converter is much faster than the MPPT.

The DC-link is modelled as a capacitor with currents as input and the DC-link voltage as output. The current drawn from the DC-link is the d-axis current multiplied with a constant K_{DC}, which relates the d-axis current and the current from the DC-link.

The grid voltage is in this model simulated as a pure sinusoidal three phase voltage, without any harmonics. It is possible to set the initial voltage angle, and to give the voltage a phase jump at a specified instant.

In this model a simplified converter model is used in the grid interface compared to the one used in the DCAC simulation. Instead of using full PWM, it is assumed that the output from the inverter is a pure sine wave. This reduces the need for running the model at a sampling rate higher than specified sampling rate T_S. The LCL filter is the same as the one used in the DCAC simulation.

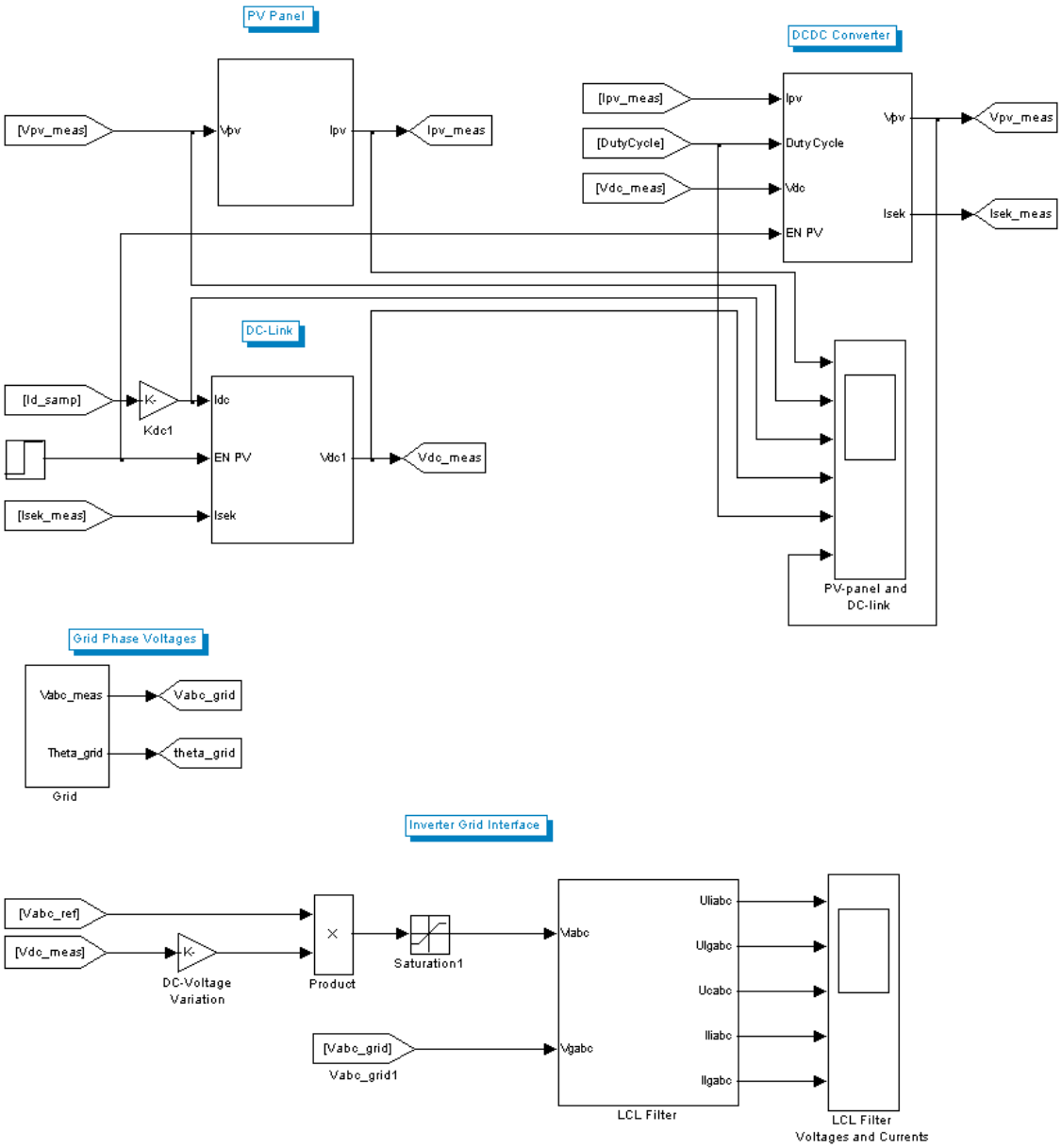

Figure 5.8: Content of plant block

6 DC-DC CONVERTER PROBLEMS

The DC-DC converter topology wanted was not available, and a new converter was therefore built and tested. It can be mentioned before reading this appendix that the design was not a success, as it ended with two broken mosfet full bridges. This chapter will deal with some of the problems and solutions found during the testing, and will finish off with some unsolved problems.

6.1 Voltage spikes

During turn off of two of the diagonal switches a voltage spike was encountered across the full bridge during the commutation of the current from the bridge and into the transformer. This voltage spike is not wanted, but unfortunately in current fed designs with transformers this is a normal problem. This spike is known from the isolated flyback topology, and is there called a *leakage spike*. The name is due to the fact that this spike is caused by the leakage inductance of the transformer, when the current is forced into the transformer windings.

The circuit can be analysed by looking at the transformer equivalent circuit in figure 6.1. In this figure the parasitic elements and the magnetizing inductance is taken into consideration. When S_1 is turned on (equivalent to turning off two diagonal switches), the current will be forced into C_p and then gradually into L_{lp}. On the secondary side the same will happen. The transformer capacitance combined with other parasitic capacitances in parallel, together with the leakage inductance will mainly decide the switching speed and the peak value of the voltage spike.

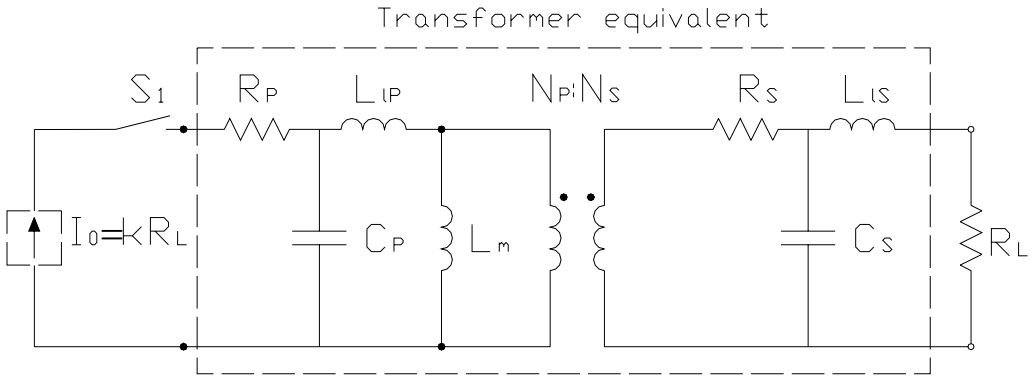

Figure 6.1: Transformer equivalent circuit with a resistive load, and a switched current source at the input

This spike can cause problems if it is not reduced, because it can outgo the SOA of the switch and cause breakdown. It can also cause some oscillations across the bridge, which can be a source to noise. The di/dt of the leakage inductance will also influence the switching speed, and thus increase the switching losses. In figure 6.2 the voltage across the bridge is shown in a setup where the leakage inductance is considerable. In the positive pulse two diagonal switches without snubber is turned off, and in the negative pulse two switches with a RC snubber is turned off.

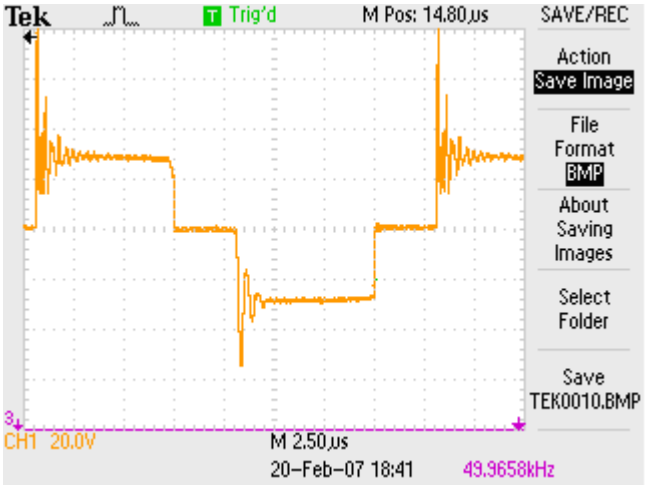

Figure 6.2: Transformer primary voltage with leakage spike. In the positive pulse two diagonal switches without snubber is turned off, and in the negative pulse two switches with a RC snubber is turned off.

In order to reduce this problem there are several methods, but the first thing to address is reduction of the leakage inductance. In an ideal case this would be zero and there would not be a voltage spike, therefore an optimization of the transformer is the first one should do.

Transformer optimization

This section will only give some general design tips on how to reduce the leakage inductance, for further information the reader is referred to the literature. First one should make sure a core with no air gap is used (E-cores come with gap in the centre leg, which had been used by a mistake in the transformer design here), this will lead to an increased leakage, but also reduced magnetizing inductance which causes other problems (these are described later in this chapter).

Another solution is to partition the windings, where the primary and secondary winding is interleaved. This is often done to reduce the eddy current losses, but there will also be a reduction in the leakage inductance because of the reduction in stored magnetostatic energy resulting from the smaller peak magnetic fields. It should be noted that this method is not without its disadvantages. It increases the complexity of the transformer, and the interwinding capacitances is increased in proportion to the number of sections. There is also an increased need for isolation between the layers, which in turn leads to a decrease in reliability of the insulation and the copper fill factor. In [29] a general expression for the leakage inductance of a partitioned winding arrangement is found.

$$L_{Leak} \approx \frac{\mu_0 \left(N_{Pri}\right)^2 l_w b_w}{3p^2 h_w} \tag{6.1}$$

N_{Pri} : Number of primary turns
l_w : Mean turn length of the windings
b_w : Bobbin window depth
h_w : Bobbin window height
p : Number of interfaces between winding sections

From this expression it can be seen that by reducing the mean turn length of the windings the leakage inductance is reduced. For an E-core this can be done by using e.g a core with a round centre leg instead of a square leg. It is also important to increase the magnetic coupling between the windings and the core, this is done by reducing the amount of air and insulation between the windings and the core to a minimum.

Clamping circuit

Sometimes it is not enough to reduce the leakage inductance of the transformer, and then other alternatives must be found. Some sort of snubber circuit can be utilized. Since the voltage across the to switches at turn off is the same as the voltage across the bridge, it is adequate to have a snubber circuit across the bride and not one in parallel with each switch as would be normal in an h-bridge. Several different solutions has been tested for this purpose, both active and passive circuits.

A passive clamping circuit (described in [26]) is implemented in the circuit in figure 6.3, which consists of a diode and a capacitor in series connected across the bridge. The idea of this circuit is to let the capacitor clamp the voltage across the bridge, so during turn off of the two diagonal switches the current is fed into the capacitor first and then gradually into the transformer. The excess energy in the clamping capacitor is discharged across a resistor. This will however lead to extra losses due to the resistor and diode losses, and the reactive energy absorbed in the capacitor due to the leakage inductance will also lead to increased current rating loss and current rating due to energy circulation in the current-fed side of the converter. The resistor has to be designed to burn off the maximum excess energy the capacitor has take up, and therefore the losses will be close to the maximum losses during any load condition. These losses will be proportional to the leakage inductance, and again a low leakage inductance is desirable.

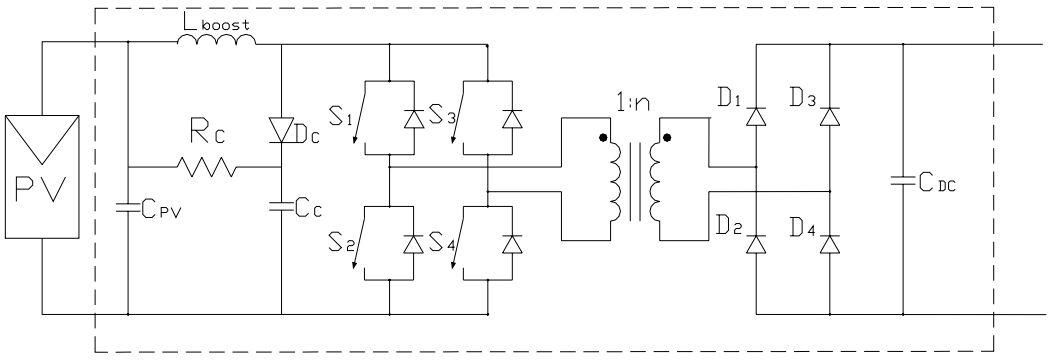

Figure 6.3: Full bridge boost converter with a passive clamp circuit

Other methods to avoid the inductor energy to be force commutated over to the leakage inductance involves active clamping circuits or more sophisticated soft switching control schemes. A method is proposed in [27] which utilizes a switch instead of the diode in the passive voltage clamp, and thus the energy can be transferred back to the circuit instead of being dissipated in the resistor.

6.2 Magnetizing inductance

In one of the tests made the load voltage is highly depending on the load resistance, which it according to the ideal case should not be. With lower loads (higher resistance) the voltage across the load becomes higher, and with higher loads it becomes lower. In figure 6.4 a plot of the boost inductor voltage, and the primary voltage and current of the transformer is shown. In the left figure it can be seen how the voltage across the primary winding of the transformer is on during the time the switch is off, but in the right the voltage across the primary goes to zero before the switch is turned on again. In figure 6.5 the primary values have been changed with the secondary values, and here it can be seen how the secondary voltage is on for the same duration as the primary voltage. The secondary current is also on for the same duration as the voltage, where the current is going from its peak value at the beginning, and falling gradually reaching zero the same instant the primary and secondary voltage collapses.

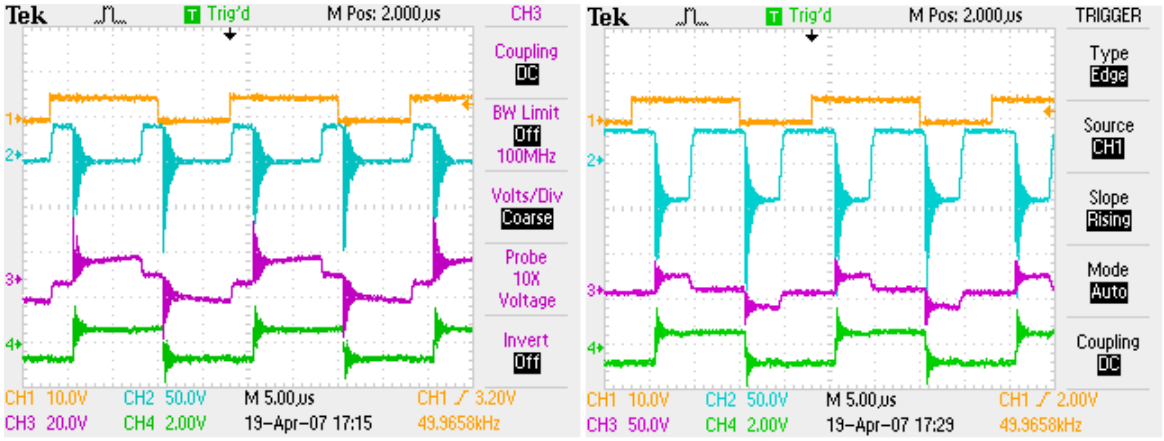

Figure 6.4: Left: High load (low resistance)
Right: Low load (high resistance)
Yellow: Switch signal, Blue: Inductor voltage, Purple: Primary voltage, Green: Primary current

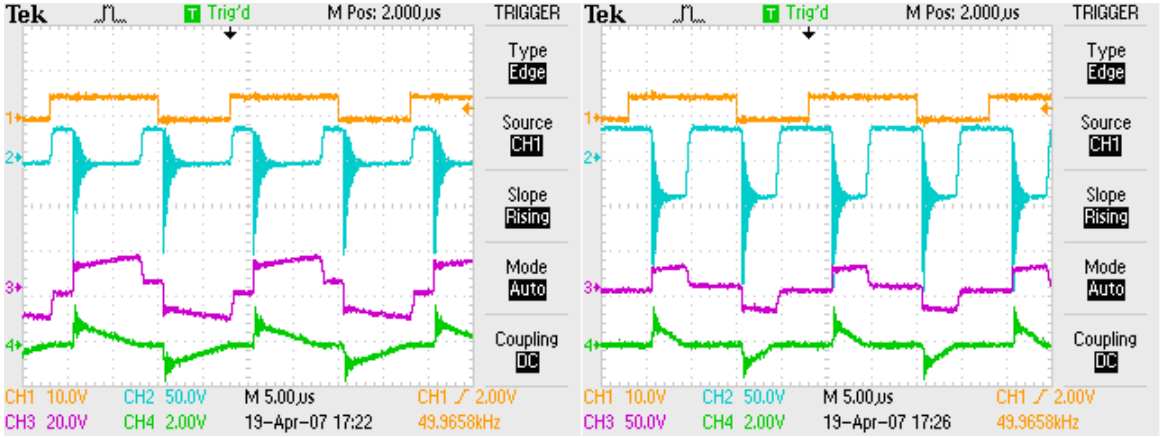

Figure 6.5: Left: High load (low resistance)
Right: Low load (high resistance)
Yellow: Switch signal, Blue: Inductor voltage, Purple: Secondary voltage, Green: Secondary current

In order to analyse this phenomena, the equivalent circuit of figure 6.1 can be simplified to the circuit in figure 6.6, assuming all transients from the parasitics are neglected.

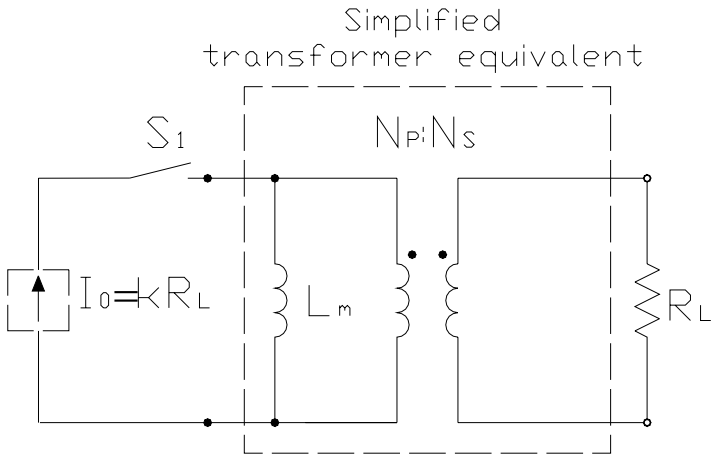

Figure 6.6: Simplified transformer equivalent circuit with a resistive load, and a switched current source at the input

By analysing how the currents in this circuit will behave if the switch is turned on end left on for an infinite amount of time. The currents will in principle be as shown in the figure below.

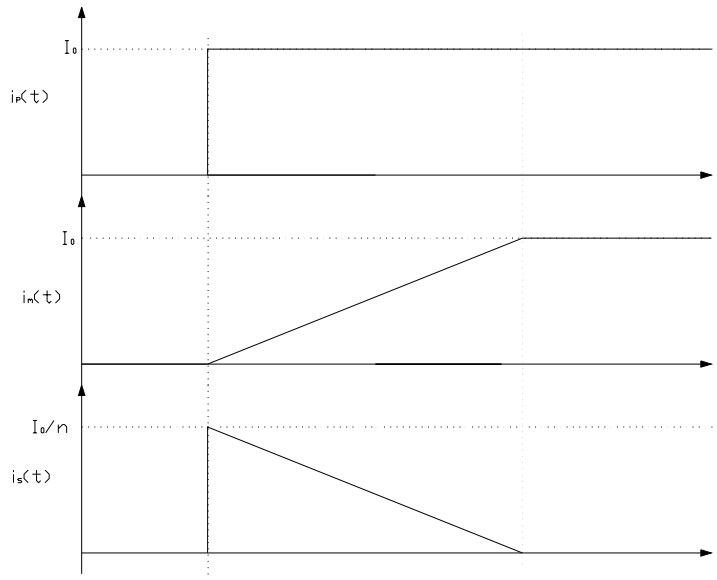

Figure 6.7: Currents in transformer after the switch is turned on for a finite time

As shown in figure 6.7 the current in the magnetizing inductance reaches I_0 after a finite time, and during the same time the secondary current reaches zero. The time it takes for the magnetizing current reaches to reach the input current, is depending on the size of the magnetizing inductance. If figure 6.7 is compared to figure 6.4 and 6.5, it can be seen that they behave in the same way. This means that in the converter circuit which switches at 50kHz, the magnetizing inductance must be very small in order for this to happen. Normally the magnetizing inductance should be so large that it can be ignored during the switching interval, but in this case it could not.

The solution to the magnetizing inductance problem in this case was simple, but hard to figure out. When buying a the core it was assumed that the core was gap-less, but upon further investigations it showed out that the core could also be delivered with a gap in the centre leg. This was not discovered upon receiving the core and after it was mounted it is impossible to see. But by replacing this the magnetizing current became much smaller, and the problem with load dependency was removed.

6.3 Gate drive ripple

During turn on of two diagonal switches it was noticed that as voltage increased across the bridge, ripple across the gate terminals becomes noticable. At high voltage levels this led to unstable behaviour of the mosfets, as they began an uncontrolled turn on/off cycle. Breakdown of the mosfets was another consequence of the high voltage, but it was not necessarly connected to the unstable behaviour, as breakdown occurred without the unstable behaviour. The breakdown was always two diagonal mosfets.

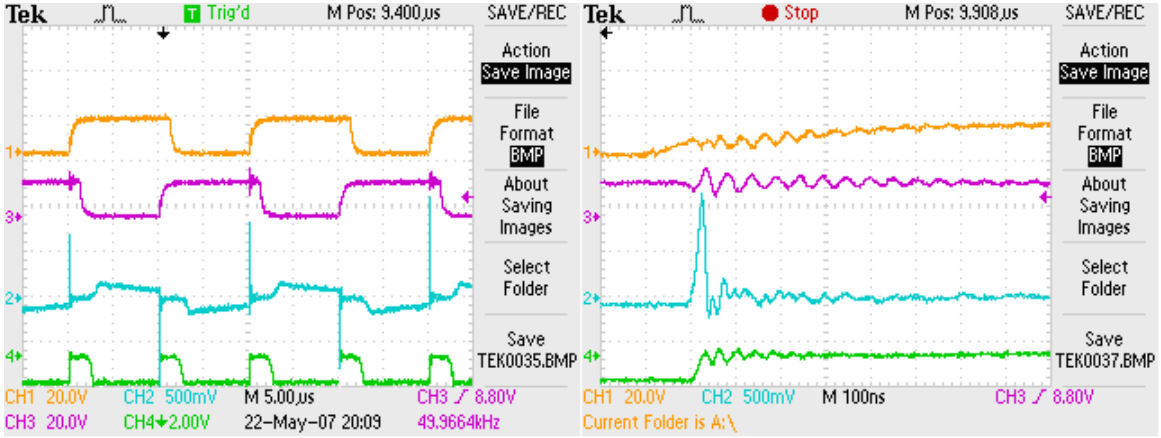

Figure 6.8: Gate drive ripple, right scope is a close up of the left during the gate ripple. Yellow: Gate signal lower left switch, Blue: Transformer primary current 2mA/mV, Purple: Gate signal upper left gate, Green: Voltage across bridge

No solution was found to this problem, but some ideas of the origin of this problem was found. It should be mentioned however that there was some problems with noise in the measurements, and that possibly the probes led to an increase in the amount of noise. This seemed to be reduced when using differential probes, but some noise might still be a problem.

- High di/dt of the mosfets can lead to malfunction of the level shifting inside the bootstrap drive circuits, and this might in turn lead to the unstable behaviour. Drivers with optocouplers where also tried, and these did not seem to have the same problem.
- Large di/dt of the reverse recovery currents of the rectifier diodes are reflected into the primary when the switches are turned on. This can be seen as the blue signal of figure 6.8. Where this current ends up in the bridge is unknown since the bridge is an integrated circuit, and the currents can't be measured through each of the switches. With the high di/dt this current can probably find its way through some of the parasitic capacitances of the mosfets, and possibly disrupt the gate signal.

The origin of this problem is not known, so care should be taken in a possible new design. First of all the circuit should be made especially for testing with lots of test points, and the mosfets should be discrete components so one can be able to measure the currents through them. It is also a good idea to have the gate drive circuit on a separate card, as this makes it easier to change drivers. It can also be smart to have the full bridge, the transformer and the rectifier bridge as separate units, with the transformer as a plug in module. This will make it easier to see the effects of the transformer in the circuit. Noise should also be considered in the new design, and probes which are resistant to noise should be used.

6.4 Duty-cycle steps

During this testing it was discovered that when a large positive step in duty cycle was applied the protective circuit in the software triggered on overcurrent. An analysis of the current and voltage during a positive duty cycle step is shown below. When a large negative step is applied, the current will be reduced and the voltage across the bridge is clamped to the DC-link voltage. Therefore no problems will arise due to a negative step.

Positive step in duty cycle

If a positive step is applied to the duty cycle, it can be seen from equation (6.2) that the DC-link voltage will rise.

$$V_{DC} = V_{PV}\frac{n}{1-D} \tag{6.2}$$

Since the DC-link voltage is clamped with a capacitor, the output voltage can not rise instantaneously. During this charging period the input current to the converter will only be limited by the boost inductor, and the series resistance of the circuit. If one assumes the input is an ideal voltage source, and the transformer is ideal, then an equivalent circuit during the positive duty cycle change is

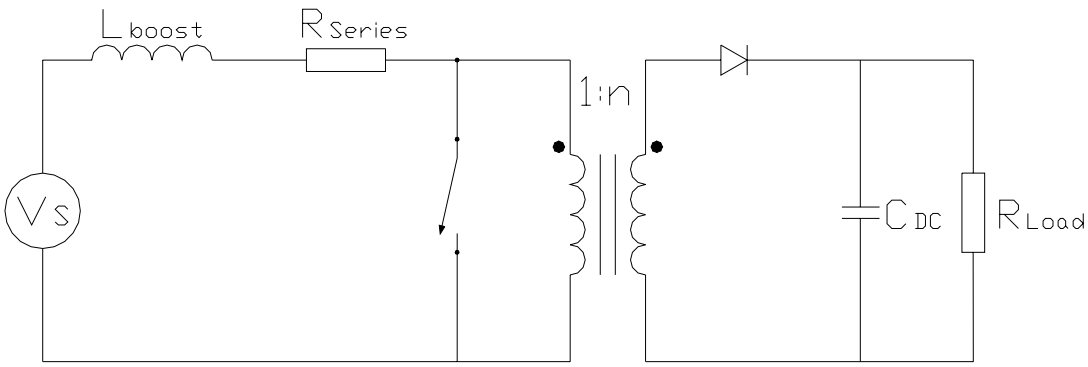

Figure 6.9: Equivalent circuit of converter during a positive duty cycle step

As long as one assumes that only positive steps in deducible occurs (due to the diode), and assuming that the input voltage is constant, a small signal AC model of the circuit can be made (see [30] for description of method). The response of the boost inductor current and the DC-link voltage due to a small step in the duty cycle can than be described as.

$$H_{IL}(s) = \frac{\hat{i}_L(s)}{\hat{d}'(s)} = -\frac{\left(nV_{DC} + R_{load}I_L D'\right) + \left(nC_{DC}R_{load}V_{DC}\right)s}{n^2 C_{DC}R_{Load}L_{Boost}s^2 + n^2\left(C_{DC}R_{Load}R_{Series} + L_{Boost}\right)s + \left(n^2R_{Series} + R_{Load}D'^2\right)} \tag{6.3}$$

$$H_{VDC}(s) = \frac{\hat{v}_{DC}(s)}{\hat{d}'(s)} = \frac{R_{Load}\left(nR_{Series}I_L - V_{DC}D'\right) + \left(nL_{Boost}R_{load}I_L\right)s}{n^2C_{DC}R_{Load}L_{Boost}s^2 + n^2\left(C_{DC}R_{Load}R_{Series} + L_{Boost}\right)s + \left(n^2R_{Series} + R_{Load}D'^2\right)} \quad (6.4)$$

where $\hat{d}'(s) = 1 - \hat{d}(s)$

Since this model is only valid for small variations of the duty cycle, only a step response of 0.01 will be applied. The step response of these functions then become as shown in figure 6.10. It can be seen that the current has a peak value which is much larger then the steady state value. The value of this peak is depending on the system values and the step size.

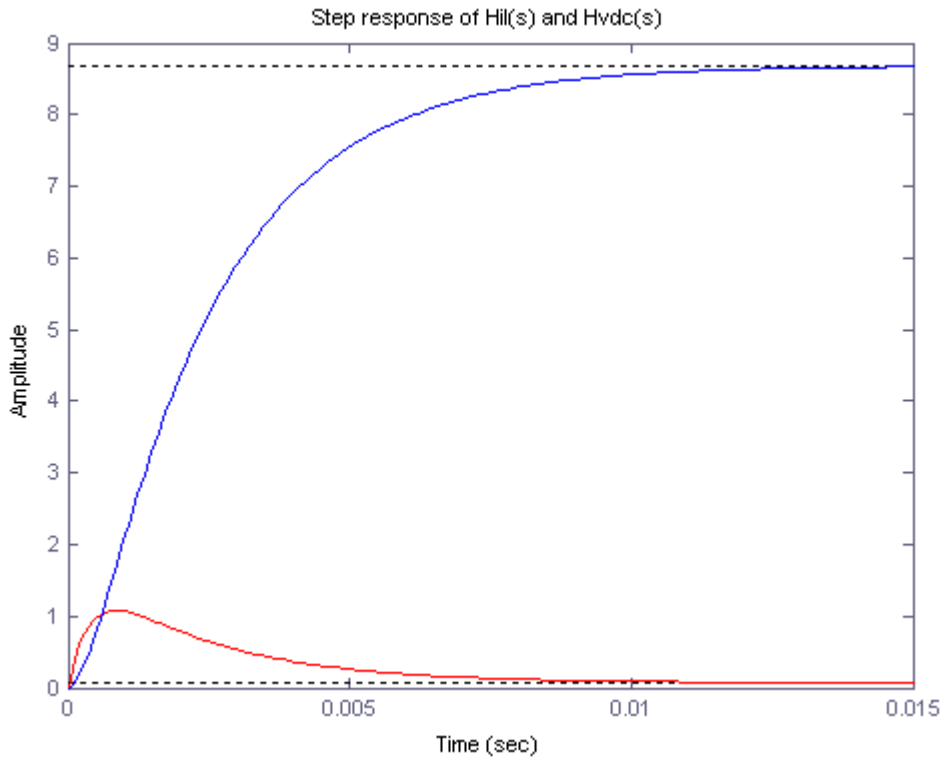

Figure 6.10: Step response after perturbing the duty cycle
Red: Current in boost inductor
Blue: Voltage DC-link

With a larger value of the DC-link capacitance the peak value will increase some, and the duration of the pulse will increase. This pulse will have influence on the speed of the MPPT tracker, and this has already been considered in the optimization of the MPPT tracker. Another problem is how the protective circuits reacts, and if the circuit can handle this overcurrent for the duration of the pulse. This will usually not be a problem when the MPPT tracker is used since the duty cycle step will be small, but during turn on and during manual control care must be taken not to overload the circuit. Therefore this type of converter should always have a charging circuit, and there should be some ramp function or a current controller should be used during manual control.

Another solution to this problem is to use current control of the converter instead of duty cycle control. This was described in the preliminary project, and will control the current through the switches instead of the duty cycle. This however will require that the current through the switches is measured.